# A80603 and A80603-1

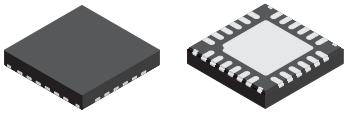
## LED Driver with Pre-Emptive Boost for Ultra-High Dimming Ratio and Low Output Ripple

## FEATURES AND BENEFITS

- Automotive AEC-Q100 qualified
- Enhanced fault handling for ASIL B system compliance
- Wide input voltage range of 4.5 to 40 V for start/stop, cold crank, and load dump requirements
- Fully integrated LED current sinks and boost converter with internal power MOSFET
- Operate in Boost or SEPIC mode for flexible output
- Drives up to 11 series white LED in 4 parallel strings, at up to 120 mA per string ($V_F$ = 3.3 V max).
- Boost switching frequency synced externally or programmed from 260 kHz to 2.3 MHz
- Clock-Out feature for internal switching frequency
- Adjustable boost frequency dithering to reduce EMI
- Advanced control allows minimum PWM on-time down to 0.3 µs, and avoids MLCC audible noises
- LED contrast ratio: 15,000:1 at 200 Hz using PWM dimming alone, 150,000:1 when combining PWM and analog dimming

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## PACKAGE:



**24-Pin 4 mm × 4 mm QFN with Wettable Flank**

*Not to scale*

## DESCRIPTION

The A80603 and A80603-1 are multi-output LED drivers that integrate a current-mode boost converter with an internal power switch and four current sinks. The boost converter can drive four strings of LEDs at up to 120 mA, or LED sinks can be paralleled together to achieve higher currents up to 480 mA total.

The devices operate from single power supply from 4.5 to 40 V; once started, they can continue to operate down to 3.9 V. This allows the parts to withstand stop/start, cold crank, and load dump conditions encountered in automotive systems. By using patented Pre-Emptive Boost control, an LED brightness contrast ratio of 15,000:1 can be achieved using PWM-only dimming at 200 Hz. Higher ratios are possible when using a combination of PWM and analog dimming.

Switching frequency can be either above or below the AM band, set by either a resistor or the synchronization pin to between 260 kHz and 2.3 MHz. A programmable dithering feature further reduces EMI. The Clock-Out pin allows other converters to be fed the clock frequency, including programmed dithering—even when the LED output is turned off.

The A80603 provides protection against application faults and external component open/short. Current sense/gate drive functions allow optional use of an input supply disconnect FET in case of output to ground short fault in boost configuration. The A80603-1 is identical to the A80603 except for soft start timer and FAULT pin behavior (see Fault Table section for details).

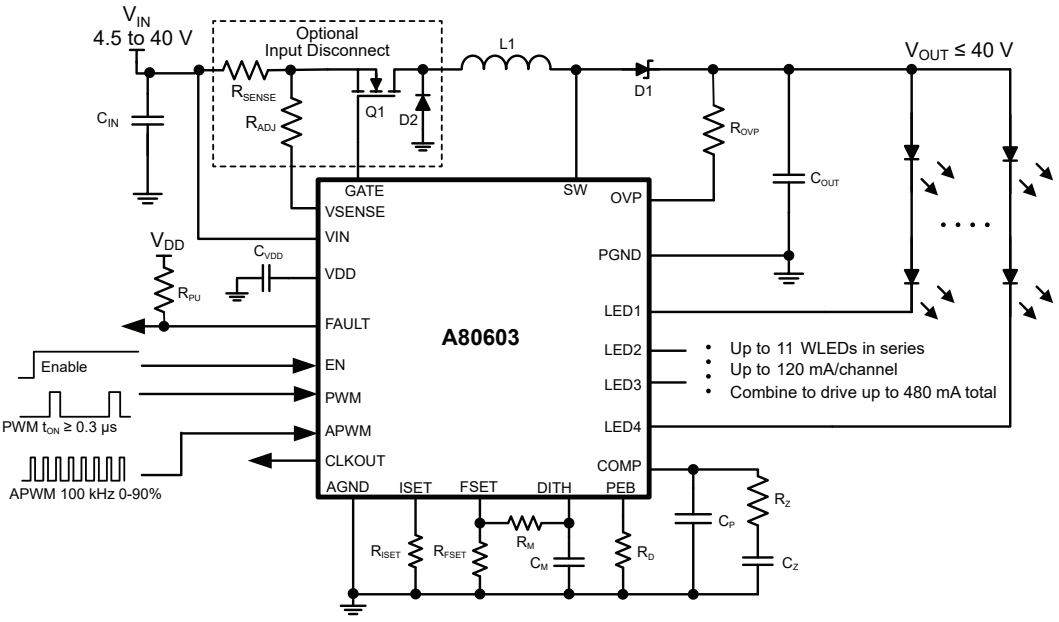



**Figure 1: A80603 Simplified Circuit Configuration.**
**See APPENDIX A and B for detailed design examples.**

## FEATURES AND BENEFITS (continued)

- Excellent input voltage transient response even at lowest PWM duty cycle
- Gate driver for optional P-channel MOSFET input disconnect switch
- Extensive protection against:
  - □ Shorted boost switch, inductor or output capacitor
  - □ Shorted FSET or ISET resistor
  - □ Open or shorted LED pins and LED strings
  - □ Open boost Schottky diode
  - □ Overtemperature

## APPLICATIONS

- Automotive infotainment backlighting
- Automotive cluster
- Automotive center stack
- Automotive exterior lighting

### SELECTION GUIDE [1]

| Part Number | Soft Start Timer | Package | Packing | Leadframe Plating |
|---|---|---|---|---|
| A80603KESJSR | 8 ms | 24-pin 4 × 4 mm wettable flank QFN with exposed thermal pad and sidewall plating | 6000 pieces per reel | 100% matte tin |
| A80603KESJSR-1 [2] | 16 ms | | | |

[1] Contact Allegro for additional packing options.
[2] Contact Allegro factory for availability of A80603KESJSR-1.

### ABSOLUTE MAXIMUM RATINGS [3]

| Characteristic | Symbol | Notes | Rating | Unit |
|---|---|---|---|---|
| LEDx Pin | $V_{LEDx}$ | x = 1..4 | –0.3 to 40 | V |
| OVP pin | $V_{OVP}$ | | –0.3 to 40 | V |
| VIN | $V_{IN}$ | | –0.3 to 40 | V |
| VSENSE, GATE | $V_{SENSE}$, $V_{GATE}$ | | Higher of –0.3 and ($V_{IN}$ – 7.4) to $V_{IN}$ +0.4 | V |
| SW | $V_{SW}$ | Continuous | –0.6 to 50 | V |
| | | t < 50 ns (repetitious, <2.5 MHz) | –1.0 to 54 | V |
| | | Single-event in case of Fault [4] | –1.5 to 60 | V |
| FAULT | $V_{FAULT}$ | | –0.3 to 40 | V |
| APWM, EN, PWM, CLKOUT, COMP, DITH, FSET, ISET, VDD, PEB | | | –0.3 to 5.5 | V |
| Operating Ambient Temperature | $T_A$ | Range K | –40 to 125 | °C |
| Maximum Junction Temperature | $T_{J(max)}$ | | 150 | °C |
| Storage Temperature | $T_{stg}$ | | –55 to 150 | °C |

[3] Stresses beyond those listed in this table may cause permanent damage to the device. The absolute maximum ratings are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the Electrical Characteristics table is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
[4] SW DMOS is self-protecting and will conduct when $V_{SW}$ exceeds 60 V.

### THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

| Characteristic | Symbol | Test Conditions [5] | Value | Unit |
|---|---|---|---|---|
| Package Thermal Resistance | $R_{\theta JA}$ | ES package measured on 4-layer PCB based on JEDEC standard | 37 | °C/W |

[5] Additional thermal information available on the Allegro website.



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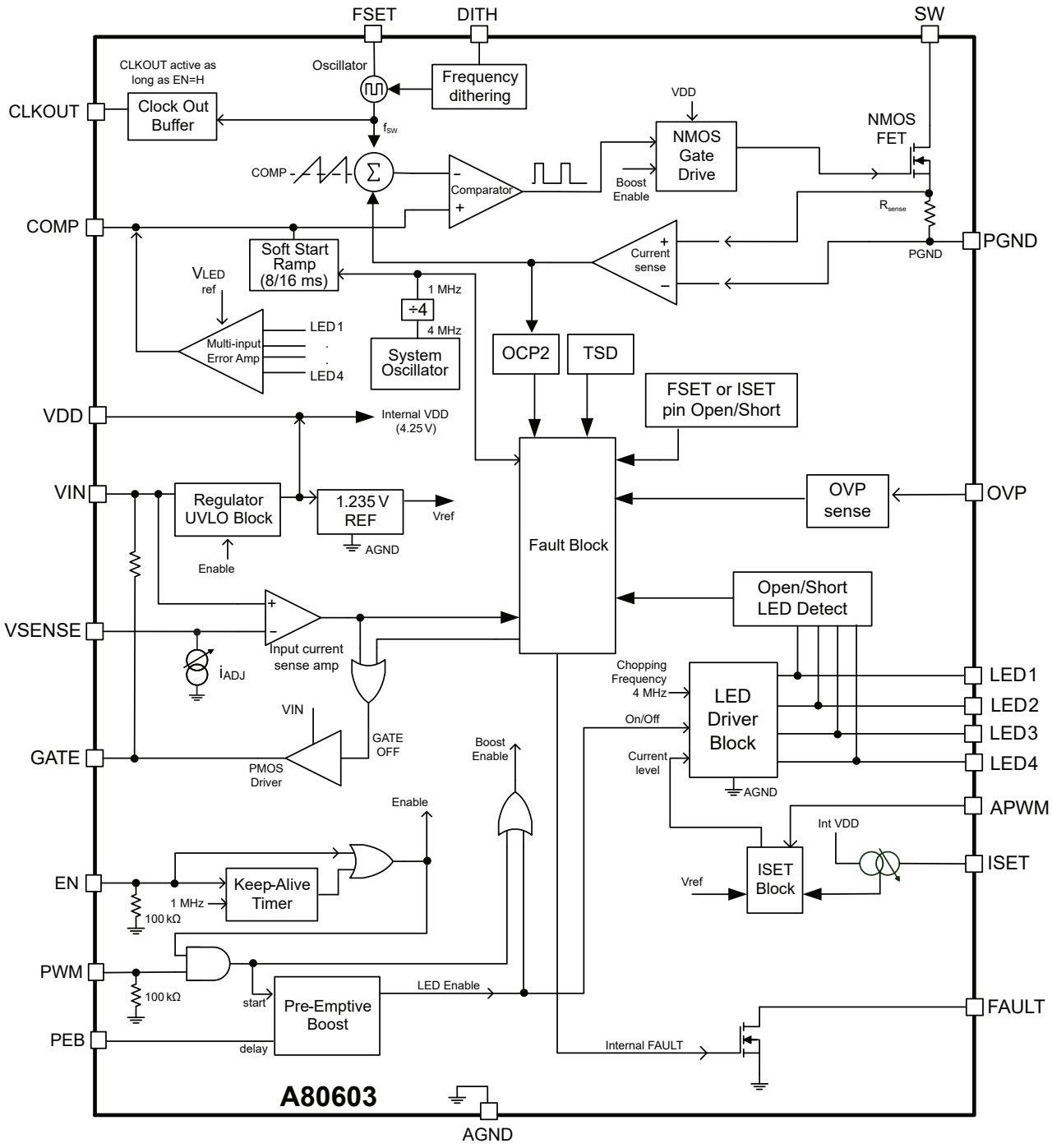
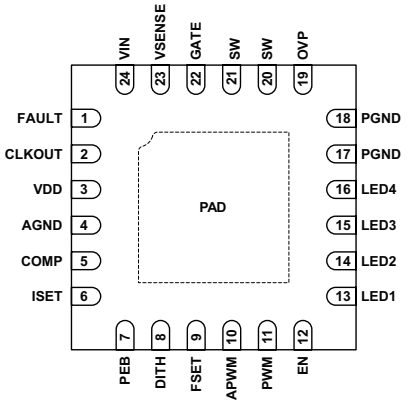



**Figure 2: Functional Block Diagram**



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## PINOUT DIAGRAM AND TERMINAL LIST




**Package ES, 24-Pin QFN Pinouts**

### Terminal List Table

| Number | Name | Function |
|---|---|---|
| 1 | FAULT | The pin is an open-drain type configuration that will be pulled low when a fault occurs. Connect a 10 kΩ resistor between this pin and desired logic level voltage. |
| 2 | CLKOUT | Logic output representing the switching frequency of internal boost oscillator. This allows other converters to be synchronized to the same $f_{SW}$ with the same dithering modulation, if applicable. Output is active as long as EN = H. |
| 3 | VDD | Output of internal LDO (bias regulator). Connect a 1 µF decoupling capacitor between this pin and GND. |
| 4 | AGND | LED current ground. Also serves as 'quiet' ground for analog signals. |
| 5 | COMP | Output of the error amplifier and compensation node. Connect a series RC network from this pin to GND for control loop compensation. |
| 6 | ISET | Connect $R_{ISET}$ resistor between this pin and GND to set the 100% LED current. |
| 7 | PEB | Connect resistor to GND to adjust delay time (~2 to 9 µs) for Pre-Emptive Boost. Leave pin open for minimum PEB delay of 1 µs. |
| 8 | DITH | Dithering control: connect a capacitor to GND to set the dithering modulation frequency (typically 1 to 3 kHz). Connect a resistor between DITH and FSET pins to set the dithering range (such as ±5% of $f_{SW}$). |
| 9 | FSET/SYNC | Frequency/synchronization pin. A resistor $R_{FSET}$ from this pin to GND sets the switching frequency $f_{SW}$ (with dithering super-imposed) between 260 kHz and 2.3 MHz. It can also be used to synchronize $f_{SW}$ to an external frequency between 260 kHz and 2.3 MHz (dithering is disabled in this case). |
| 10 | APWM | Analog dimming. Apply APWM clock (40 kHz to 1 MHz) to this pin and the duty cycle of this clock determines the LED current. Leave open or connect to GND for 100%. |
| 11 | PWM | Controls the on/off state of LED current sinks to reduce the light intensity by using pulse-width modulation. Typical PWM dimming frequency is in the range of 200 Hz to 2 kHz. EN and PWM pins may be tied together to allow single-wire dimming control. |
| 12 | EN | Enables the IC when this pin is pulled high. If EN goes low, the IC remains in standby mode for up to 16 ms, then shuts down completely. |
| 13-16 | LED1-4 | LED current sinks #1 to 4. Connect the cathode of each LED string to pin. Unused LED pin must be terminated to GND through a 6.19 kΩ resistor. |
| 17-18 | PGND | Power ground for internal NMOS switching device. |
| 19 | OVP | Overvoltage protection. Connect external resistor from $V_{OUT}$ to this pin to adjust the over voltage protection level. |
| 20-21 | SW | The drain of the internal NMOS switching device of the boost converter. |
| 22 | GATE | Output gate driver pin for external P-channel FET control. |
| 23 | VSENSE | Connect this pin to the negative sense side of the current sense resistor $R_{SC}$. The threshold voltage is measured as $V_{IN} - V_{SENSE}$. There is also a fixed ~20 µA current sink to allow for trip threshold adjustment. |
| 24 | VIN | Input power to the IC as well as the positive input used for current sense resistor. |
| – | PAD | Exposed pad of the package providing enhanced thermal dissipation. Must be connected to the ground plane(s) of the PCB with at least 8 vias, directly in the pad. |



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**ELECTRICAL CHARACTERISTICS [1]: Unless otherwise noted, specifications are valid at $V_{IN}$ = 16 V, $T_J$ = 25°C, • indicates specifications guaranteed over the full operating temperature range with $T_J$ = –40°C to 125°C, typical specifications are at $T_J$ = 25°C**

| Characteristics | Symbol | Test Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| **INPUT VOLTAGE SPECIFICATIONS** | | | | | | | |
| Operating Input Voltage Range [3] | $V_{IN}$ | | • | 4.5 | – | 40 | V |
| VIN UVLO Start Threshold | $V_{UVLO(rise)}$ | $V_{IN}$ rising | • | – | – | 4.35 | V |
| VIN UVLO Stop Threshold | $V_{UVLO(fall)}$ | $V_{IN}$ falling | • | – | – | 3.95 | V |
| UVLO Hysteresis [2] | $V_{UVLO_HYS}$ | | | 300 | 450 | 600 | mV |
| **INPUT CURRENTS** | | | | | | | |
| VIN Pin Operating Current | $I_{OP}$ | EN and PWM = H, $f_{SW}$ = 2 MHz | • | – | 13 | 18 | mA |
| VIN Pin Quiescent Current | $I_Q$ | EN = H and PWM = L, $f_{CLKOUT}$ = 2 MHz | • | – | 10 | – | mA |
| VIN Pin Sleep Current | $I_{QSLEEP}$ | $V_{IN}$ = 16 V, $V_{EN}$ = 0 V | • | – | 2 | 10 | µA |
| **INPUT LOGIC LEVELS (EN, PWM, APWM)** | | | | | | | |
| Input Logic Level-Low | $V_{IL}$ | | • | – | – | 0.4 | V |
| Input Logic Level-High | $V_{IH}$ | | • | 1.5 | – | – | V |
| Input Pull-Down Resistor | $R_{EN}$, $R_{PWM}$, $R_{APWM}$ | Input = 5 V | | 60 | 100 | 140 | kΩ |
| **OUTPUT LOGIC LEVELS (CLKOUT)** | | | | | | | |
| Output Logic Level-Low | $V_{OL}$ | 5 V < $V_{IN}$ < 40 V | • | – | – | 0.3 | V |
| Output Logic Level-High | $V_{OH}$ | 5 V < $V_{IN}$ < 40 V | • | 1.8 | – | – | V |
| CLKOUT Duty Cycle | $D_{CLKOUT}$ | $f_{SW}$ = 2 MHz, no external sync | • | 33 | 50 | 67 | % |
| CLKOUT Negative Pulse Width [2] | $t_{CLKNPW}$ | External sync = 260 kHz to 2.3 MHz | | – | 200 | – | ns |
| **APWM PIN** | | | | | | | |
| APWM Frequency Range [2] | $f_{APWM}$ | Clock signal applied to pin | • | 40 | – | 1000 | kHz |
| APWM Duty Cycle Range [2] | $D_{APWM}$ | Clock signal applied to pin | • | 0 | – | 90 | % |
| **VDD REGULATOR** | | | | | | | |
| Regulator Output Voltage | $V_{DD}$ | $V_{IN}$ > 4.5 V, $i_{LOAD}$ < 1 mA | | 4.05 | 4.25 | 4.45 | V |
| VDD UVLO Start Threshold | $V_{DDUVLOrise}$ | $V_{DD}$ rising, no external load | | – | 3.2 | – | V |
| VDD UVLO Stop Threshold | $V_{DDUVLOfall}$ | $V_{DD}$ falling, no external load | | – | 2.65 | – | V |
| **ERROR AMPLIFIER** | | | | | | | |
| Amplifier Gain [2] | gm | $V_{COMP}$ = 1.5 V | | – | 1000 | – | µA/V |
| Source Current | $I_{EA(SRC)}$ | $V_{COMP}$ = 1.5 V | | – | –500 | – | µA |
| Sink Current | $I_{EA(SINK)}$ | $V_{COMP}$ = 1.5 V | | – | +500 | – | µA |
| COMP Pin Pull Down Resistance | $R_{COMP}$ | FAULT = 0, $V_{COMP}$ = 1.5 V | | – | 1.4 | – | kΩ |

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| Characteristics | Symbol | Test Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| **DITHERING CONTROL** | | | | | | | |
| DITH Pin Source Current | $i_{DITH(src)}$ | Output current when $V_{DITH}$ < 0.8 V | | – | 20 | – | µA |
| DITH Pin Sink Current | $i_{DITH(sink)}$ | Output current when $V_{DITH}$ > 1.2 V | | – | –20 | – | µA |
| **OVERVOLTAGE PROTECTION** | | | | | | | |
| OVP Pin Voltage Threshold | $V_{OVP(th)}$ | OVP pin connected to $V_{OUT}$ | • | 2.2 | 2.5 | 2.8 | V |
| OVP Pin Sense Current Threshold | $i_{OVP(th)}$ | Current into OVP pin at 125ºC | | 140 | 146.5 | 153 | µA |
| | | Measured over temperature | • | 140 | 150 | 160 | µA |
| OVP Sense Current Temperature Coefficient [2] | $\Delta i_{OVP}$ | Current into OVP pin | | – | –36 | – | nA/ºC |
| OVP Pin Leakage Current | $I_{OVPLKG}$ | $V_{OUT}$ = 16 V, EN = L | • | – | 0.1 | 1 | µA |
| OVP Variation at Output | $\Delta_{OVP}$ | Measured at $V_{OUT}$ when $R_{OVP}$ = 249 kΩ | | – | – | 5 | % |
| Undervoltage Detection Threshold | $V_{UVP(th)}$ | Measured at $V_{OUT}$ when $R_{OVP}$ = 249 kΩ [2] | | – | 3.3 | 4.2 | V |
| | | Measured at $V_{OUT}$ when $R_{OVP}$ = 0 Ω | | – | 0.2 | 0.25 | V |
| Secondary Overvoltage Protection | $V_{OVP2}$ | Measured at SW pin; part latches when OVP2 is detected | • | 51 | 55 | 59 | V |
| **BOOST SWITCH** | | | | | | | |
| Switch On Resistance | $R_{SW}$ | $I_{SW}$ = 0.75 A, $V_{IN}$ = 16 V | • | – | 250 | 500 | mΩ |
| Switch Pin Leakage Current | $I_{SWLKG25}$ | $V_{SW}$ = 13.5 V, $V_{PWM}$ = $V_{IL}$, $T_J$ = 25°C | | – | 0.1 | 1 | µA |
| | $I_{SWLKG85}$ [2] | $V_{SW}$ = 13.5 V, $V_{PWM}$ = $V_{IL}$, $T_J$ = 85°C | | – | – | 10 | µA |
| Switch Pin Current Limit | $I_{SW(LIM)}$ | IC truncates present switching cycle when primary limit is reached | • | 3.0 | 3.75 | 4.5 | A |
| Secondary Switch Current Limit [2] | $I_{SW(LIM2)}$ | IC latches off when secondary limit is reached | | – | 5.1 | – | A |
| Minimum Switch On-Time | $t_{SW(ON)}$ | | • | 45 | 65 | 85 | ns |
| Minimum Switch Off-Time | $t_{SW(OFF)}$ | | • | – | 50 | 66 | ns |
| **OSCILLATOR FREQUENCY** | | | | | | | |
| Oscillator Frequency | $f_{SW}$ | $R_{FSET}$ = 10 kΩ | • | 1.95 | 2.15 | 2.35 | MHz |
| | | $R_{FSET}$ = 110 kΩ | | – | 260 | – | kHz |
| FSET Pin Voltage | $V_{FSET}$ | $R_{FSET}$ = 10 kΩ | | – | 1.00 | – | V |
| **SYNCHRONIZATION** | | | | | | | |
| Sync Input Logic Level | $V_{SYNCL}$ | FSET/SYNC pin logic Low | • | – | – | 0.4 | V |
| | $V_{SYNCH}$ | FSET/SYNC pin logic High | • | 1.5 | – | – | V |
| Synchronized PWM Frequency | $f_{SWSYNC}$ | | • | 260 | – | 2300 | kHz |
| Synchronization Input Min Off-Time | $t_{PWSYNCOFF}$ | | • | 150 | – | – | ns |
| Synchronization Input Min On-Time | $t_{PWSYNCON}$ | | • | 150 | – | – | ns |

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| Characteristics | Symbol | Test Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| **LED CURRENT SINKS** | | | | | | | |
| LEDx Accuracy [4] | $Err_{LED}$ | $i_{ISET}$ = 120 µA ($R_{ISET}$ = 8.33 kΩ), $R_{FSET}$ = 10 kΩ, $V_{APWM}$ = 0 V | • | – | 0.7 | 3 | % |
| LEDx Matching | $\Delta_{LEDx}$ | $i_{ISET}$ = 120 µA, $R_{FSET}$ = 10 kΩ, $V_{APWM}$ = 0 V | • | – | 0.8 | 2 | % |
| LEDx Regulation Voltage | $V_{LED}$ | Measured individually with all other LED pins tied to ≥1 V, $i_{ISET}$ = 120 µA, $V_{APWM}$ = 0 V | • | 600 | 700 | 800 | mV |
| $I_{ISET}$ to $I_{LEDx}$ Current Gain | $A_{ISET}$ | $i_{ISET}$ = 120 µA, $V_{APWM}$ = 0 V | • | 812 | 832 | 852 | A/A |
| ISET Pin Voltage | $V_{ISET}$ | | | 0.97 | 1 | 1.03 | V |
| Allowable ISET Current | $i_{ISET}$ | | • | 20 | – | 144 | µA |
| LED String Partial-Short-Detect Voltage | $V_{LEDSC}$ | Sensed from each LED pin to GND while its current sink is in regulation; all other LED pins tied to 1 V | • | 4.5 | 5.2 | 6 | V |
| LED String Partial-Short-Detect Duration | $t_{LEDSC}$ | Time required to confirm LED string partial-short and pull FAULT = L | | – | – | 6.6 | µs |
| LED Pin Shorted-to-GND Check Duration | $t_{LEDSTG}$ | Wait time before proceeding with Soft-Start (if no LED pin is shorted to GND) | | – | 1.5 | – | ms |
| Soft-Start Ramp Up Time | $t_{SSRU}$ | A80603 | | 6.5 | 8 | 9.5 | ms |
| | | A80603-1 | | 13 | 16 | 19 | ms |
| Enable Pin Shut Down Delay | $t_{EN(OFF)}$ | EN goes from High to Low; exceeding $t_{EN(OFF)}$ results in IC shutdown | • | 10 | 16 | 22 | ms |
| Minimum PWM Dimming On-Time | $t_{PWMH}$ | First and subsequent PWM pulses | • | – | 0.3 | 0.4 | µs |
| Minimum PWM Off-Time (for PWM ≠ 100%) [2] | $t_{PWMLOW}$ | Externally pulsing PWM pin | • | – | – | 1 | µs |
| **GATE PIN** | | | | | | | |
| Gate Pin Sink Current | $I_{GSINK}$ | $V_{GS}$ = $V_{IN}$, no input OCP fault | | – | −113 | – | µA |
| Gate Pin Source Current | $I_{GSOURCE}$ | $V_{GS}$ = $V_{IN}$ – 6 V, input OCP fault tripped | | – | 6 | – | mA |
| Gate Shutdown Delay When Over-Current Fault Is Tripped [2] | $t_{FAULTT}$ | $V_{IN}$ – $V_{SENSE}$ = 200 mV; monitored at FAULT pin | | – | – | 3 | µs |
| Gate Voltage | $V_{GS}$ | Measured between GATE and VIN when gate is fully on | | – | −6.7 | – | V |
| **VSENSE PIN** | | | | | | | |
| VSENSE Pin Sink Current | $i_{ADJ}$ | | • | 16 | 20 | 24 | µA |
| VSENSE Trip Point | $V_{SENSETRIP}$ | Measured between $V_{IN}$ and $V_{SENSE}$, $R_{ADJ}$ = 0 Ω | • | 88 | 100 | 110 | mV |
| **PEB PIN** | | | | | | | |
| PEB Delay Time | $t_{PEB}$ | $i_{PEB}$ = 60 µA | | 2.4 | 3.2 | 4.0 | µs |
| **FAULT PIN** | | | | | | | |
| FAULT Pull Down Voltage | $V_{FAULT}$ | $I_{FAULT}$ = 1 mA | | – | – | 0.5 | V |
| FAULT Pin Leakage Current | $i_{FAULT-LKG}$ | $V_{FAULT}$ = 5 V | | – | – | 1 | µA |

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| Characteristics | Symbol | Test Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| **THERMAL PROTECTION (TSD)** | | | | | | | |
| Thermal Shutdown Threshold [2] | TSD | Temperature rising | | 155 | 170 | – | °C |
| Thermal Shutdown Hysteresis [2] | $TSD_{HYS}$ | | | – | 20 | – | °C |

[1] For input and output current specifications, negative current is defined as coming out of the node or pin (sourcing); positive current is defined as going into the node or pin (sinking).
[2] Ensured by design and characterization; not production tested.
[3] Minimum $V_{IN}$ = 4.5 V is only required at startup. After startup is completed, IC can continue to operate down to $V_{IN}$ = 4 V.
[4] LED current is trimmed to cancel variations in both Gain and ISET voltage.



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## FUNCTIONAL DESCRIPTION

The A80603 is a multistring LED regulator with an integrated boost switch and four precision current sinks. It incorporates a patented Pre-Emptive Boost (PEB) control algorithm to achieve PWM dimming ratio over 15,000:1 at 200 Hz under nominal application conditions. PEB control also minimizes output ripple to avoid audible noise from output ceramic capacitors.

The switching frequency can be either synchronized to an external clock or generated internally. Spread-spectrum technique (with user-programmable dithering range and modulation frequency) is provided to reduce EMI. A clock-out signal (CLKOUT) allows other converters to be synchronized to the switching frequency of A80603.

### Enabling the IC

The A80603 wakes up when EN pin is pulled above logic high level, provided that VIN pin voltage is over the VIN_UVLO threshold. The boost stage and LED channels are enabled separately by PWM = H signal after the IC powers up.

The IC performs a series of safety checks at power up, to determine if there are possible fault conditions that might prevent the system from functioning correctly. Power-up checks include:

- VOUT shorted to GND
- LED pin shorted to GND
- FSET pin open/shorted
- ISET pin open/shorted to GND, etc.

Only if no faults were detected, then the IC can proceed to start switching.

As long as EN = H, the PWM pin can be toggled to control the brightness of LED channels by using PWM dimming. Alternatively, EN and PWM can be tied together to allow single-wire control for both power on/off and PWM dimming. If EN is pulled low for longer than 16 ms, the IC shuts off.

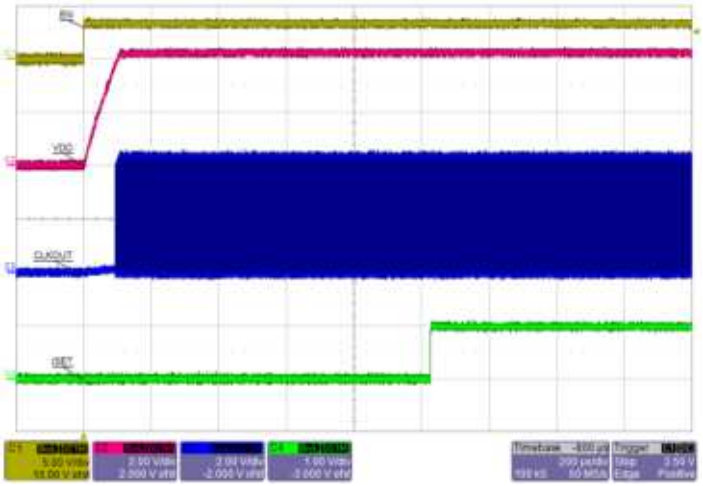



**Figure 3: Startup showing EN, VDD, CLKOUT, and ISET (PWM = L). Note that CLKOUT is available as soon as $V_{DD}$ ramps up, even though Boost stage and LED drivers are not yet enabled.**



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## Powering Up: LED Detection Phase

The VIN pin has an undervoltage lockout (UVLO) function that prevents the A80603 from powering up until the UVLO threshold is reached. Once the VIN pin goes above UVLO and a high signal is present on the EN pin, the IC proceeds to power up. At this point, the A80603 is going to enable the disconnect switch and will try to check if any LED pins are shorted to GND and/or are not used. The LED detection phase starts when PWM = H and the GATE voltage of the input disconnect PMOS switch is pulled down to 3.3 V below $V_{IN}$.

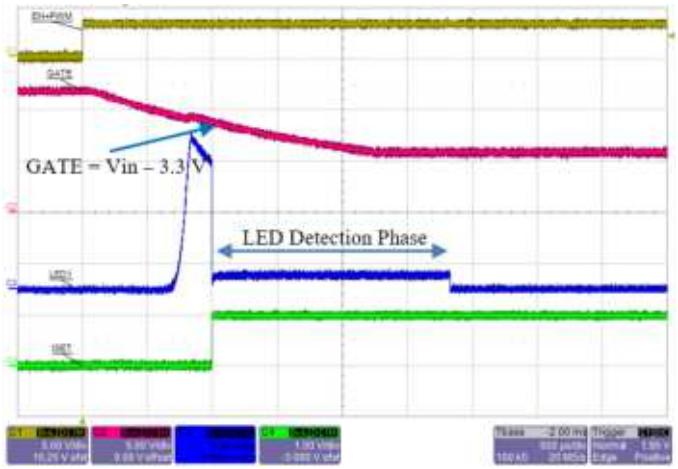



**Figure 4: Startup showing EN+PWM, GATE, LED1, and ISET. Switching frequency = 2.15 MHz. Note that LED Detection Phase starts as soon as GATE pin is pulled down to 3.3 V below $V_{IN}$ (provided that PWM = H).**

Once the voltage threshold on VLED pins exceeds ~120 mV, a delay of approximately 1.5 ms is used to determine the status of the pins.

Unused LED pin should be terminated with a 6.19 kΩ resistor to GND. At the end of LED detection phase, any channel with pull down resistor is then disabled and will not contribute to the boost regulation loop.

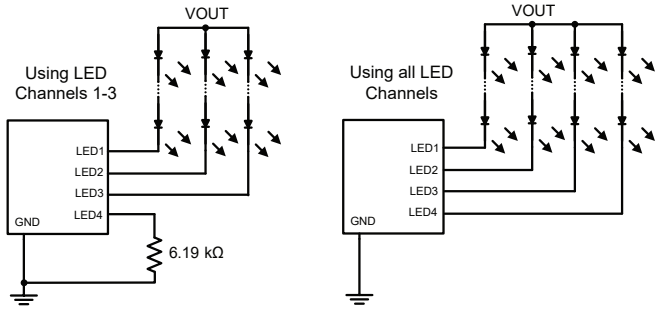



**Figure 5: How to signal an unused LED channel during startup LED detection phase**

**Table 1: LED Detection phase voltage threshold levels**

| LED Pin Voltage Measured | Interpretation | Outcome |
|---|---|---|
| < 120 mV | LED pin shorted to GND fault | Cannot proceed with soft-start unless fault is removed |
| ~ 230 mV | LED channel not in use | LED channel is removed from operation |
| > 340 mV | LED channel in use | Proceed with soft-start |

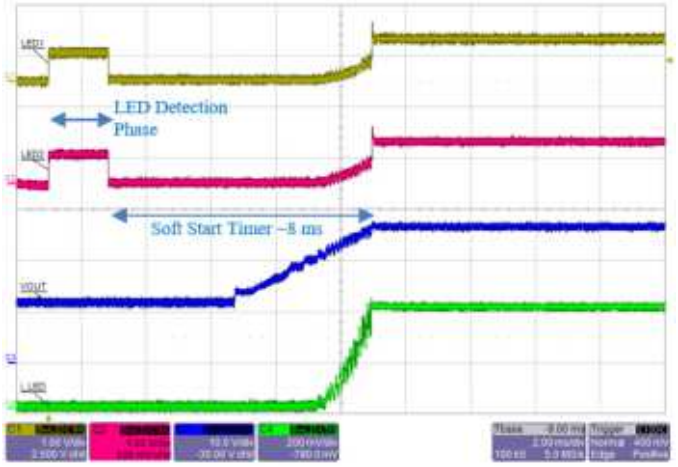



**Figure 6: A80603 normal startup showing all channels passed LED Detection phase. Total LED current = 100 mA × 4 (only LED1 and LED2 pin voltages are shown).**



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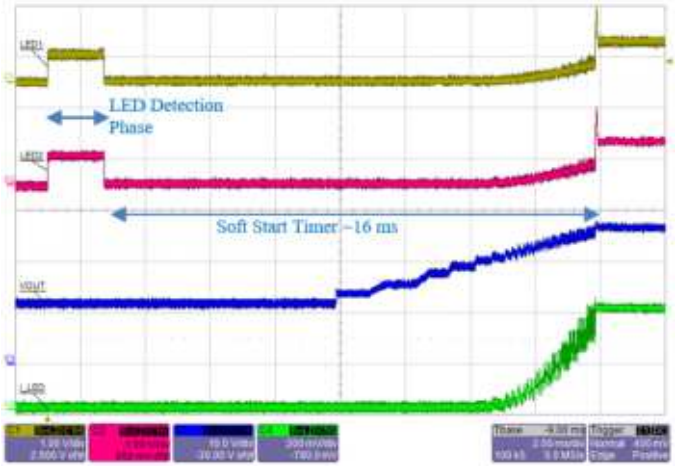



**Figure 7: A80603-1 normal startup showing all channels passed LED Detection phase. Note longer soft start timer.**

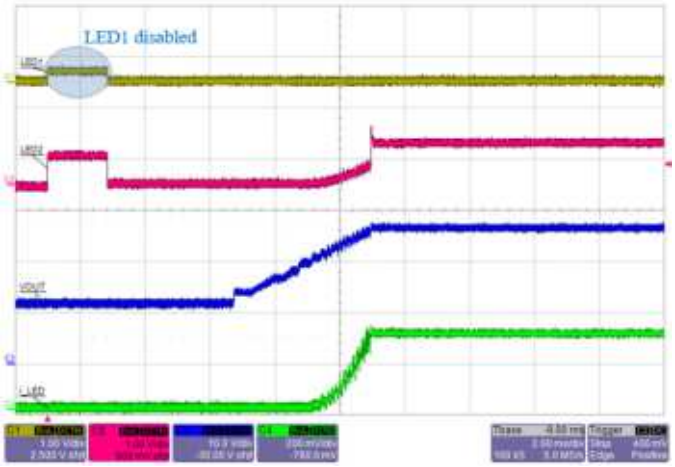



**Figure 8: A80603 normal startup showing LED1 channel is disabled with a 6.19 kΩ resistor to GND. Total LED current = 100 mA × 3.**

If an LED pin is shorted to ground, the A80603 will not proceed with soft start until the short is removed from the LED pin. This prevents the A80603 from ramping up the output voltage and putting an uncontrolled amount of current through the LEDs.

The FAULT pin is pulled low in case of LED pin shorted-to-GND fault (A80603 only), but the IC continues to retry. Once the fault is removed, the soft-start process will continue. The same applies in case of FSET or ISET pin is shorted to GND.

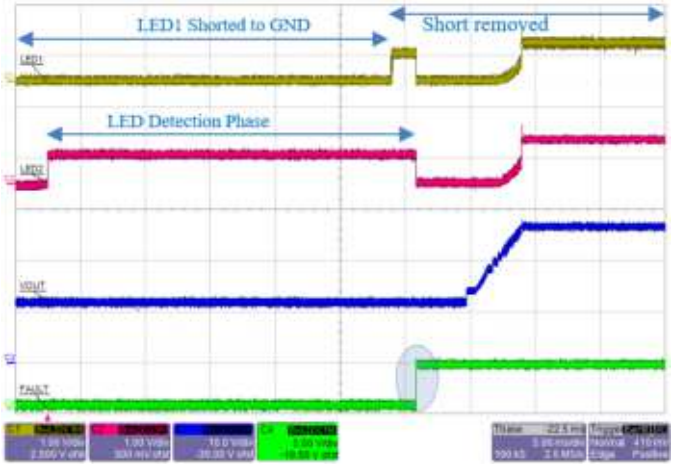



**Figure 9: A80603; LED1 is shorted-to-GND initially, then released. After the fault is removed, the IC auto-recovers and proceeds with soft-start. FAULT is released at the end of LED detection phase.**

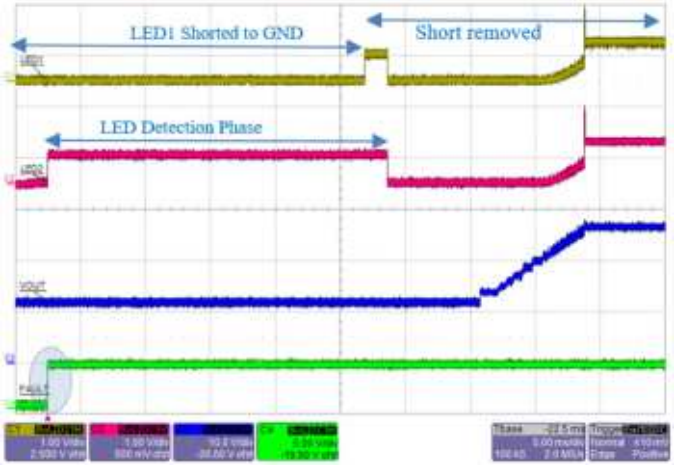



**Figure 10: A80603-1, LED1 is shorted-to-GND initially, then released. After the fault is removed, the IC auto-recovers and proceeds with soft-start. FAULT is released at the beginning of LED detection phase.**



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## Power Up: Boost Output Undervoltage

During startup, after the input disconnect switch has been enabled, the output voltage is checked through the OVP (over-voltage protection) pin. If the sensed voltage does not rise above $V_{UVP(th)}$, the output is assumed to be at fault and the IC will not proceed with soft start. Output UVP level is linked to the OVP level programmed according to the equation:

$$V_{UVP} = V_{OVP} / 12$$

Undervoltage protection may be caused by one of the following faults:

- Output capacitor shorted to GND
- Boost inductor or diode open
- OVP sense resistor open

After an UVP (undervoltage protection) fault, the A80603 is immediately shutdown and latched off. To enable the IC again, the latched fault must be cleared. This can be achieved by powering-cycling the IC, which means either:

- $V_{IN}$ falls below falling UVLO threshold, or
- EN = L for >16 ms.

Alternatively, latched fault can be cleared by keeping EN = H but pulling PWM = L for >16 ms. This method has the advantage that it does not interrupt the CLKOUT signal.

## Soft Start Function

During startup, the A80603 ramps up its boost output voltage following a fixed slope, as determined by OVP set point and Soft-Start Timer. This technique limits the input inrush current, and ensures consistent startup time regardless of the PWM dimming duty cycle.

The soft-start process is completed when any one of the following conditions is met:

- All enabled LED channels have reached their regulation current,
- Output voltage has reached 93% of its OVP threshold, or
- Soft-start ramp time ($t_{SSRU}$) has expired.

To summarize, the complete startup process of A80603 consists of:

- Power-up error checking
- Enabling input disconnect switch
- LED pin open/short detection
- Soft-start ramp

This is illustrated by the following startup timing diagram (not to scale):

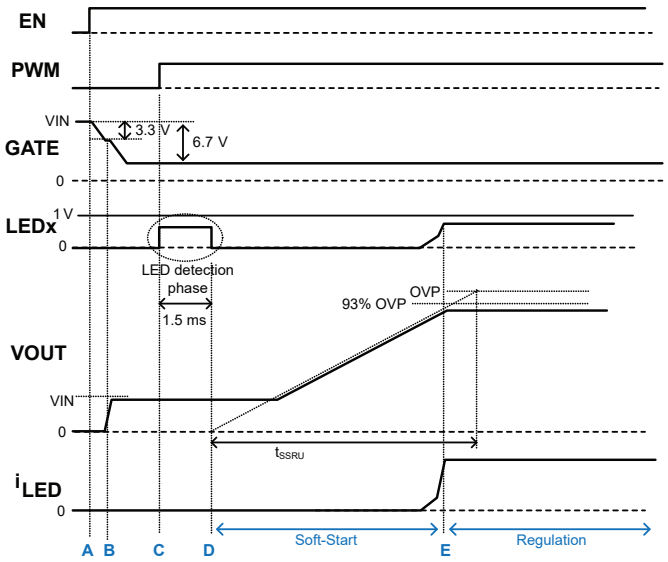



**Figure 11: Complete startup process of A80603**

Explanation of Events:

**A**: EN = H wakes up the IC. $V_{DD}$ ramps up and CLKOUT becomes available. IC starts to pull down GATE slowly.

**B**: When GATE is pulled down to 3.3 V below $V_{IN}$, $I_{SET}$ becomes enabled. IC is now waiting for PWM = H to startup.

**C**: Once PWM = H, the IC checks each LEDx pins to determine if it is in use, disabled, or shorted to GND.

**D**: Soft-Start begins at the completion of LED pin short-detect phase of 1.5 ms. $V_{OUT}$ ramps up following a fixed slope set by OVP and soft-start timer of ~8 ms (16 ms for the A80603-1).

**E**: Soft-start terminates when all LED currents reached regulation, $V_{OUT}$ reached 93% OVP, or soft-start timer expired.



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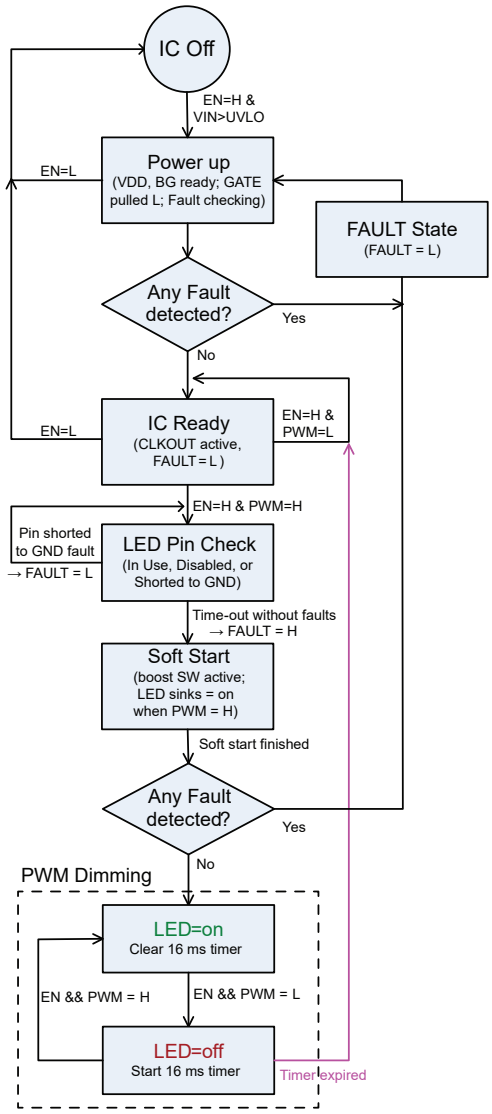



**Figure 12: A80603 Startup Flow Chart**

## Frequency Selection

The switching frequency of the boost regulator is programmed by a resistor connected to FSET pin. The switching frequency can be selected anywhere from 260 kHz to 2.3 MHz. The chart below shows the typical switching frequency verses FSET resistor value.

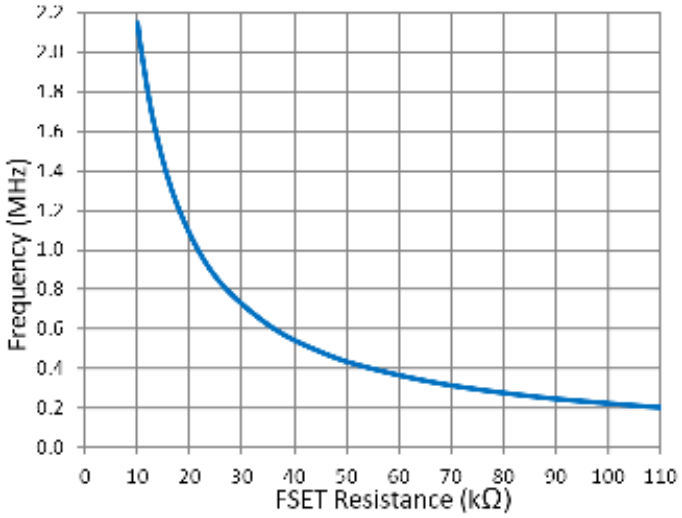



**Figure 13: Switching Frequency as a function of FSET Resistance**

Alternatively, the following empirical formula can be used:

Equation 1: $R_{FSET} = (21.5 / f_{SW}) - 0.2$

where $f_{SW}$ is in MHz and $R_{FSET}$ is in kΩ.

If a fault occurs during operation that will increase the switching frequency, the internal oscillator frequency is clamped to a maximum of 3.5 MHz. If the FSET pin is shorted to GND, the part will shut down. For more details, refer to the Fault Mode Table section.



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## Synchronization

The A80603 can also be synchronized using an external clock. At power up, if the FSET pin is held low, the IC will not start. Only when the FSET pin is tristated to allow for the pin to rise to about 1 V, or when a sync clock is detected, the A80603 will then try to power up.

The basic requirement of the external sync signal is 150 ns minimum on-time and 150 ns minimum off time. The diagram below shows the timing restrictions for a synchronization clock at 2.2 MHz.

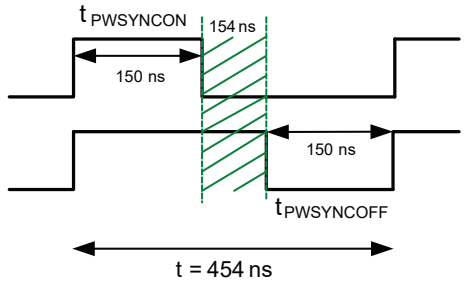



**Figure 14: Pulse width requirements for an External Sync clock at 2.2 MHz**

Based on the above, any clock with a duty cycle between 33% and 66% at 2.2 MHz can be used. The table below summarizes the allowable duty cycle range at various synchronization frequencies.

**Table 2: Acceptable Duty Cycle range for External Sync clock at various frequencies**

| Sync. Pulse Frequency | Duty Cycle Range |
|---|---|
| 2.2 MHz | 33% to 66% |
| 2 MHz | 30% to 70% |
| 1 MHz | 15% to 85% |
| 600 kHz | 9% to 91% |
| 300 kHz | 4.5% to 95.5% |

If it is necessary to switch over between internal oscillator and external sync during operation, ensure the transition takes place at least 500 ns after the previous PWM = H rising edge. Alternatively, execute the switchover during PWM = L only. This restriction does not apply if PWM dimming is not being used.

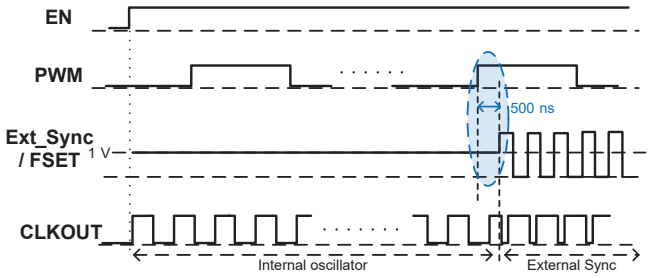



**Figure 15: Avoid switching over between Internal Oscillator and External Sync in highlighted region**

## Loss of External Sync Signal

Suppose the A80603 started up with a valid external SYNC signal, but the SYNC signal is lost during normal operation. In that case, one of the following happens:

- If the external SYNC signal is high impedance (open), the IC continues normal operation after approximately 5 µs, at the switching frequency set by $R_{FSET}$. No FAULT flag is generated.
- If the external SYNC signal is stuck low (shorted to ground), the IC will detect an FSET-shorted-to-GND fault. FAULT pin is pulled low after approximately 10 µs, and switching is disabled. Once the FSET pin is released or SYNC signal is detected again, the IC will proceed to soft-start.

To prevent generating a fault when the external SYNC signal is stuck at low, the circuit shown below can be used. When the external SYNC signal goes low, the IC will continue to operate normally at the switching frequency set by the $R_{FSET}$. No FAULT flag is generated.

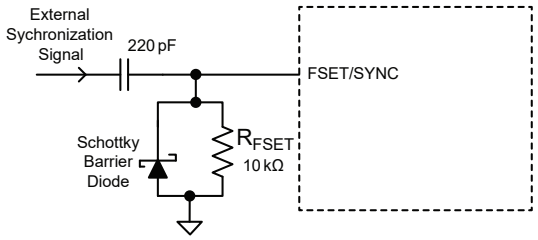



**Figure 16: Countermeasure for External Sync Stuck-at-Low Fault**

It is important to use a small capacitance for the AC-coupling capacitor (220 pF in the above example). If the capacitance is too large, the IC may incorrectly declare a FSET-shorted-to-GND fault and restart.



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## Switching Frequency Dithering

To minimize the peak EMI spikes at switching frequency harmonics, the A80603 offers the option of frequency dithering, or spread-spectrum clocking. This feature simplifies the input filters needed to meet the automotive CISPR 25 conducted and radiated emission limits.

For maximum flexibility, the A80603 allows both dithering range and modulation frequency to be independently programmable using two external components.

The Dithering Modulation Frequency is given by the approximate equation:

Equation 2: $C_{DITH}\ (nF) = 25 / f_{DM}\ (kHz)$

where $C_{DITH}$ is the value of capacitor connected from DITH pin to GND.

The resistor that sets the dithering range is calculated using:

Equation 3: $R_{DITH} = 20 \times R_{FSET} / Range\ (\pm\%)$

where $R_{FSET}$ is the resistor from FSET pin to GND, $R_{DITH}$ is the resistor between DITH and FSET pins.

As an example, by using $R_{FSET}$ = 10 kΩ, $R_{DITH}$ = 40.2 kΩ, and $C_{DITH}$ = 22 nF, the resulted switching frequency is $f_{SW}$ = 2.15 MHz ±5% modulated at 1.1 kHz. This is illustrated by the following diagram.

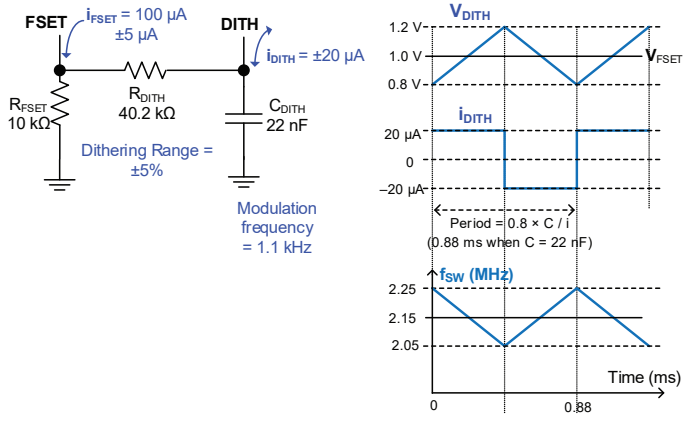



**Figure 17: How to Program Switching Frequency Dithering Range and Modulation Frequency**

There are no hard limits on dithering range and modulation frequency. As a general guideline, pick a dithering range between ±5% and 10%, with the modulation frequency between 1 kHz and 3 kHz. In practice, using a larger dithering range and/or higher modulation frequency do not generate any noticeable benefits.

If dithering function is not desired, it can be disabled by disconnecting the $R_{DITH}$ between DITH and FSET pins. Connect DITH pin to VDD if $C_{DITH}$ is not populated. Dithering is always disabled when $f_{SW}$ is controlled by external sync. $R_{DITH}$ and $C_{DITH}$ have no effects in this case even if they were populated.

## Clock Out Function

The A80603 allows other ICs to be synchronized to its internal switching frequency through the CLKOUT pin.

The CLKOUT signal is available as soon as the IC is enabled (EN = H), even when the boost stage is not active (PWM = L). Its frequency is the same as that of the internal oscillator. Its duty cycle, however, depends on how the switching frequency is generated:

- If $f_{SW}$ is programmed by FSET resistor, the CLKOUT duty cycles is approximately 50%.
- If $f_{SW}$ is controlled by external sync, the output signal has a fixed 200 ns negative pulse width (CLKOUT = L), regardless of the external sync frequency.

This is illustrated by the following waveforms:

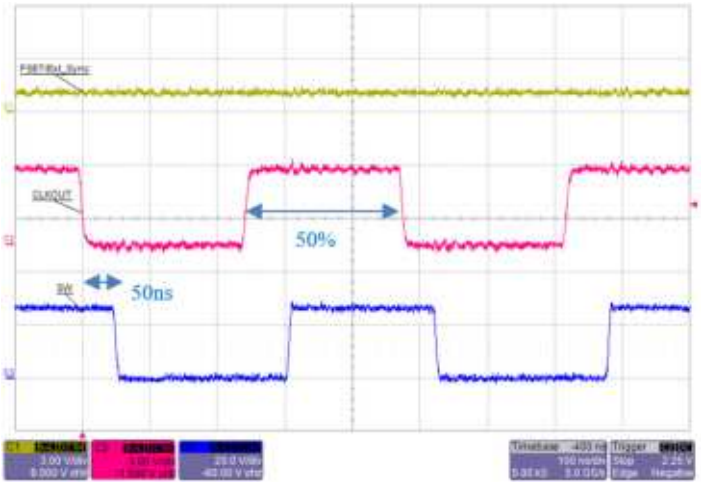



**Figure 18: Without external sync, the CLKOUT signal has a fixed duty cycle of 50%. Delay from CLKOUT falling edge to SW falling edge is approximately 50 ns.**



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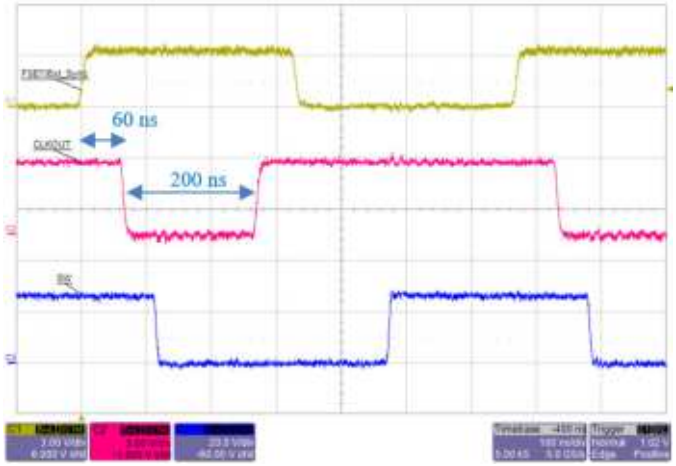



**Figure 19: With external sync, the CLKOUT signal has a fixed negative pulse width of 200 ns. Delay from SYNC rising edge to CLKOUT falling edge is approximately 60 ns.**

## LED Current Setting

The maximum LED current can be up to 120 mA per channel, and is set through the ISET pin. Connect a resistor $R_{ISET}$ between this pin and GND. The relation between $I_{LED}$ and $R_{ISET}$ is given below:

Equation 4:

$$I_{LED} = I_{SET} \times A_{ISET}$$

$$I_{SET} = V_{ISET} / R_{ISET}$$

$$Therefore\ R_{ISET} = (V_{ISET} \times A_{ISET}) / I_{LED}$$

$$= 832 / I_{LED}$$

where $I_{LED}$ current is in mA and $R_{ISET}$ is in kΩ.

This sets the maximum current through the LEDs, referred to as the '100% current'. The average LED current can be reduced from the 100% current level by using either PWM dimming or analog dimming.

**Table 3: ISET resistor values vs. LED current. Resistances are rounded to the nearest E-96 (1%) resistor value.**

| Standard Closest RISET Resistor Value | LED current per channel |
|---|---|
| 6.98 kΩ | 120 mA |
| 8.25 kΩ | 100 mA |
| 10.5 kΩ | 80 mA |
| 13.7 kΩ | 60 mA |
| 21.0 kΩ | 40 mA |

## PWM Dimming

When both EN and PWM pins are pulled high, the A80603 turns on all enabled LED current sinks. When either EN or PWM is pulled low, all LED current sinks are turned off. The compensation (COMP) pin is floated, and critical internal circuits are kept active.

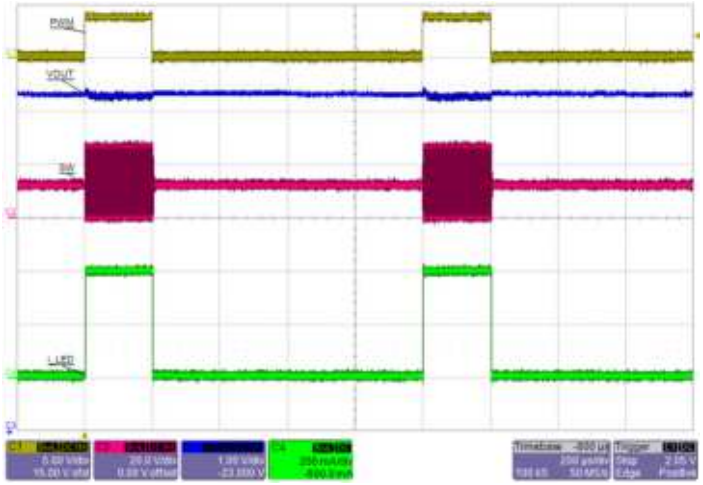


**Figure 20: PWM dimming operation at 20% 1 kHz. CH1 = PWM (5 V/div), CH2 = SW (20 V/div), CH3 = $V_{OUT}$, CH4 = $i_{LED}$ (200 mA/div).**

By using the patented Pre-Emptive Boost (PEB) control algorithm, the A80603 is able to achieve minimum PWM dimming on-time down to 300 ns. This translates to PWM dimming ratio up to 15,000:1 at the PWM dimming frequency of 200 Hz. Technical details on PEB will be explained in the next section.

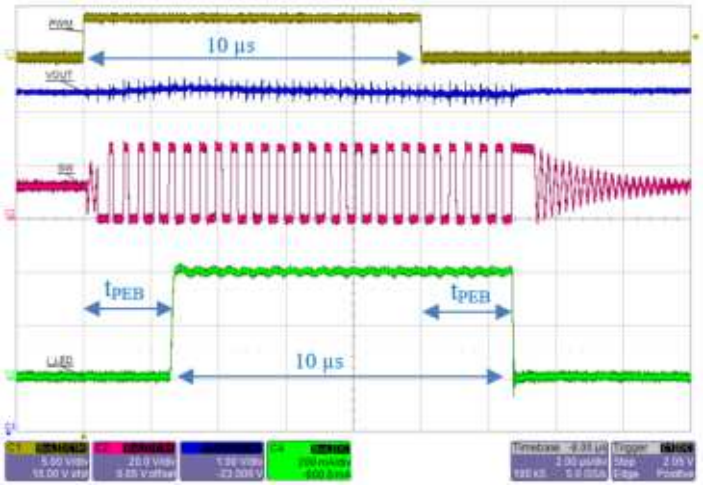



**Figure 21: Zoom in view for PWM on-time = 10 µs. Notice that the LED current is shifted with respect to PWM signal. Ripple at $V_{OUT}$ is ~0.2 V when using 2 × 4.7 µF MLCC as output capacitors.**



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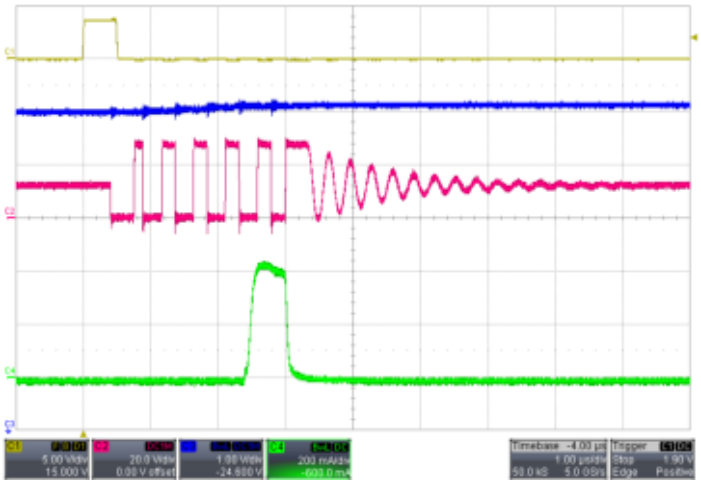


**Figure 22: Zoom-in view showing A80603 is able to regulate LED current at PWM on-time down to 500 ns.**

The typical PWM dimming frequencies fall between 200 Hz and 1 kHz. There is no hard limit on the highest PWM dimming frequency that can be used. However at higher PWM frequency, the maximum PWM dimming ratio will be reduced. This is shown in the following table:

**Table 4: Maximum PWM Dimming Ratio that can be achieved when operating at different PWM Dimming Frequency**

| PWM Frequency | PWM Period | Maximum PWM Dimming Ratio |
|---|---|---|
| 200 Hz | 5 ms | 15,000:1 |
| 1 kHz | 1 ms | 3,000:1 |
| 3.3 kHz | 300 µs | 1,000:1 |
| 20 kHz | 50 µs | 150:1 |

While it is possible to operate with very high PWM duty cycle for subtle dimming, it is important to avoid PWM pulse low periods that are shorter than the Minimum PWM Off-Time ($t_{PWM-LOW}$), which is 1 µs. Driving PWM at 100% is acceptable.

## Pre-Emptive Boost

The basic principle of pre-emptive boost (PEB) can be best explained by the following two waveforms. The first one shows how a conventional LED driver operates during PWM dimming operation. The second one shows that of the A80603.

Common test conditions for both cases:

PWM = 1% at 1 kHz (on-time=10 µs), $f_{SW}$ = 2.15 MHz, L = 10 µH, $V_{IN}$ = 12 V, LED load = 8 series ($V_{OUT}$ = ~25 V) at 100 mA × 4. $C_{OUT}$ = 2 × 4.7 µF 50 V 1210 MLCC. COMP: $R_Z$ = 280 Ω, $C_Z$ = 68 nF.

Common scope settings:

CH1 (Yellow) = PWM (5 V/div); CH2 (Red) = Inductor current (500 mA/div); CH3 (Blue) = $V_{OUT}$ (1 V/div); CH4 (Green) = LED current (200 mA/div); time scale = 2 µs/div.

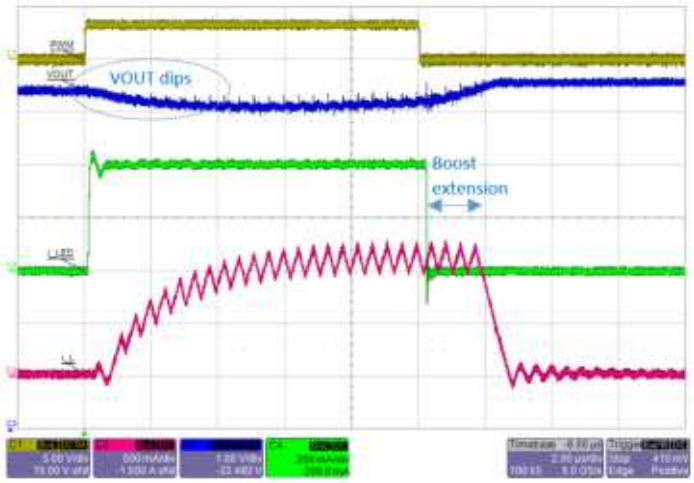



**Figure 23: Traditional PWM Dimming operation where boost switch and LED current are enabled at the same time. Note that $V_{OUT}$ shows overall ripple of ~0.5 V**

When PWM signal goes high, a conventional LED driver turns on its boost switching at the time with LED current sinks. The problem is that the inductor current takes several switching cycles to ramp up to its steady-state value before it can deliver full power to the output load. During the first few cycles, energy to the LED load is mainly supplied by the output capacitor, which results in noticeable dip in output voltage.

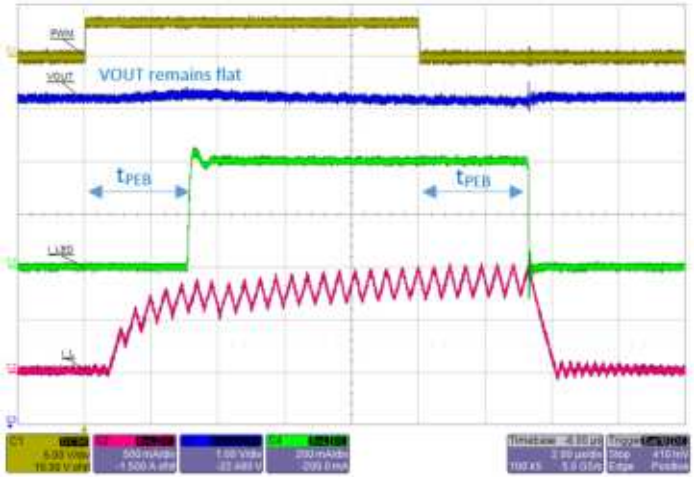



**Figure 24: A80603 PWM dimming operation with PEB delay set to 3 µs. Note that $V_{OUT}$ ripple is reduced to ~0.2 V.**



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In the A80603, the boost switch is also enabled when PWM goes high. However, the LED current is not turned on until after a short delay of $t_{PEB}$. This allows the inductor current to build up before it starts to deliver the full power to LED load. During the pre-boost period, $V_{OUT}$ actually bumps up very slightly, while the following dip is essentially eliminated. When PWM goes low, both boost switching and LED remains active for the same delay of $t_{PEB}$. Therefore the PWM on-time is preserved in LED current.

PEB delay can be programmed using an external resistor, $R_{PEB}$, from PEB pin to GND. Their relationship is shown in the following chart:

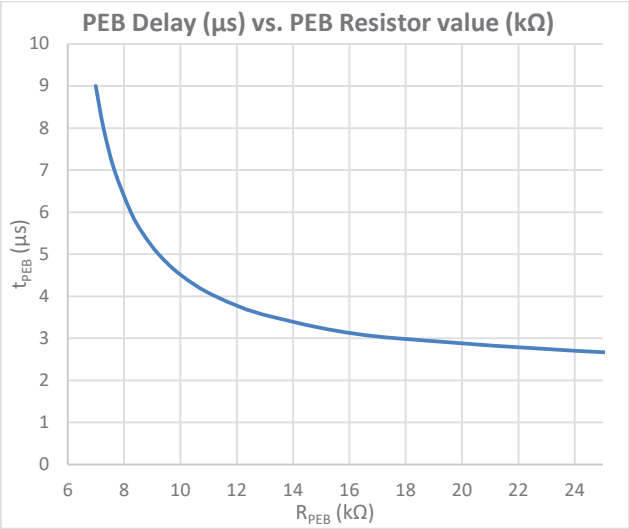



**Figure 25: How PEB delay time varies with value of PEB pin resistor to GND.**

Ideally, $t_{PEB}$ is equal to the inductor current ramp up time. But the latter is affected by many external parameters, such as switching frequency, inductance, $V_{IN}$ and $V_{OUT}$ ratio, etc. Therefore, some experimentation is required to optimize the PEB delay time. In general for switching frequency at 2 MHz, $t_{PEB}$ = 2.5 to 4 µs is a good starting point.

The advantage of PEB is that even a non-optimized delay time can significantly reduce the output ripple voltage compared to a conventional LED driver.

## Analog Dimming with APWM Pin

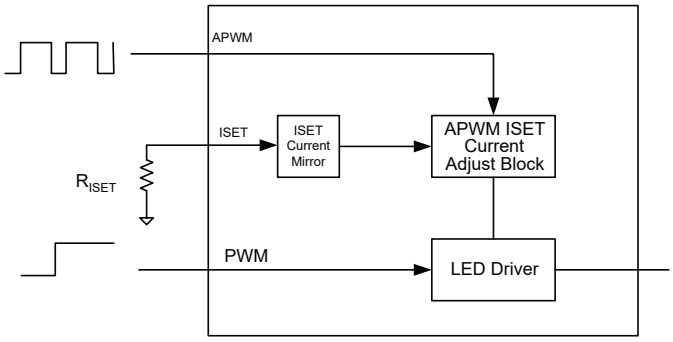



**Figure 26: Simplified block diagram of APWM function**

The APWM pin is used in conjunction with the ISET pin to achieve analog dimming. This is a digital signal pin that internally adjusts the $I_{SET}$ current. The typical input signal frequency is between 40 kHz and 1 MHz. The duty cycle of this signal is inversely proportional to the percentage of current delivered to the LED. The relationship is shown below:

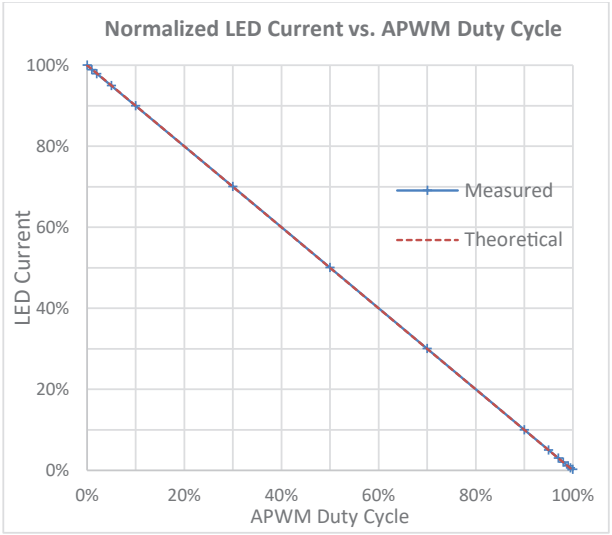



**Figure 27: Showing LED current is inversely proportional to the APWM duty cycle. Test conditions: $V_{IN}$ =12 V, $V_{OUT}$ = 25 V (8 × WLED), total LED current = 100 mA × 4, APWM frequency = 100 kHz**

As an example, a system that delivers a full LED current of 100 mA per channel would deliver 75 mA when an APWM signal with a duty-cycle of 25% is applied (because analog dimming level is 100% – 25% = 75%). This is demonstrated by the following waveforms.



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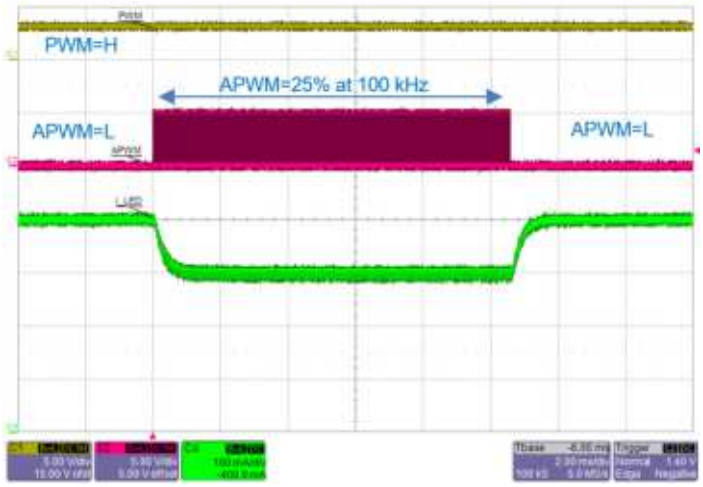



**Figure 28: PWM = H. Total LED current drops from 400 mA (4 × 100 mA/ch) to 300 mA when APWM of 25% duty cycle is applied. Note that LED current takes ~0.5 ms to settle after change in APWM.**

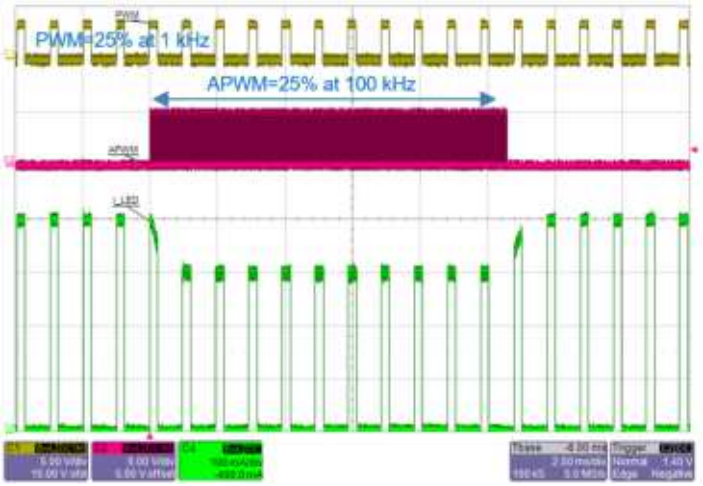



**Figure 29: PWM = 25% at 1 kHz. Peak LED current drops from 400 mA (4 × 100 mA/ch) to 300 mA when APWM of 25% duty cycle is applied**

One popular application of analog dimming is for LED brightness calibration, commonly known as 'LED Binning'. LEDs from the same manufacturer and series are often grouped into different 'bins' according to their light efficacy (lumens per watt). It is therefore necessary to calibrate the '100% current' for each LED bin, in order to achieve uniform luminosity.

To use APWM pin as a trim function, the user should first set the 100% current based on efficacy of LED from the lowest bin. When using LED with higher efficacy, the required current is then trimmed down to the appropriate level using APWM duty cycle.

As an example, assume that:

- LED from lowest bin has an efficacy of 80 lm/W
- LED highest bin has an efficacy of 120 lm/W

Suppose the maximum LED current was set at 100 mA based LEDs from lowest bin. When using LEDs from highest bin, the current should then be reduces to 67% (80/120). This can be achieved by sending APWM clock with 33% duty cycle.

When analog dimming is not used, APWM pin should be either tied to GND or left floating (there is an internal pull-down resistor to GND).

## Extending LED Dimming Ratio

The dynamic range of LED brightness can be further extended, by using a combination of PWM duty cycle, APWM duty cycle, and analog dimming method.

For example, the following approach can be used to achieve a 100,000:1 dimming ratio at 200 Hz:

- Vary PWM duty cycle from 100% down to 0.01% to give 10,000:1 dimming. This requires PWM dimming on-time be reduced down to 0.5 µs.
- With PWM dimming on-time fixed at 0.5µs, vary APWM duty from 0% to 90% to reduce peak LED current from 100% down to 10%. This gives a net effect of 100,000:1 dimming.

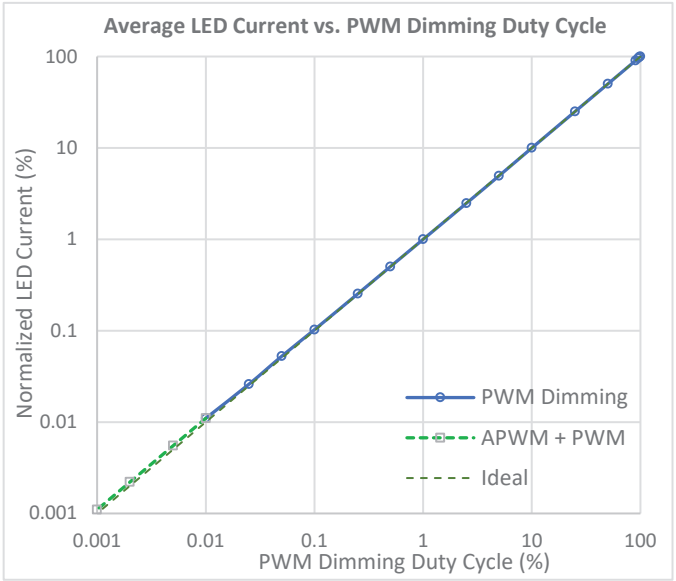



**Figure 30: How to achieve 100,000:1 dimming ratio by using both PWM and APWM. Test conditions: $V_{IN}$ = 12 V, $V_{OUT}$ = 25 V (8 × WLED), total LED current = 400 mA, PWM frequency = 200 Hz, APWM frequency = 100 kHz.**



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Note that the A80603 is capable of providing analog dimming range greater than 10:1. By applying APWM with 96% duty cycle, for example, an analog dimming range of 25:1 can be achieved. However, this requires the external APWM signal source to have very fine pulse-width resolution. At 200 kHz APWM frequency, a resolution of 50 ns is required to adjust its duty cycle by 1%.

## Analog Dimming with External Voltage

Besides using APWM signal, the LED current can also be reduced by using an external voltage source applied through a resistor to the ISET pin. The dynamic range of this type of dimming is dependent on the ISET pin current. The recommended $i_{SET}$ range is from 20 µA to 144 µA for the A80603. Note that the IC will continue to work at $i_{SET}$ below 20 µA, but the relative error in LED current becomes larger at lower dimming level.

Below is a typical application circuit using a DAC (digital-analog converter) to control the LED current. The ISET current (which directly controls the LED current) is normally set as $V_{ISET}/R_{ISET}$. The DAC voltage can be higher or lower than $V_{ISET}$, thus adjusting the LED current to a lower or higher value.

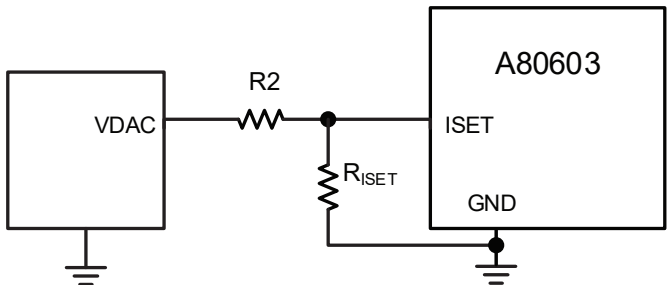



**Figure 31: Adjusting LED current with an external voltage source**

Equation 5:

$$i_{ISET} = \frac{V_{ISET}}{R_{ISET}} - \left[\frac{VDAC - V_{ISET}}{R2}\right]$$

where $V_{ISET}$ is the ISET pin voltage (typically 1.0 V), and VDAC is the DAC output voltage.

When VDAC is higher than 1.00 V, the LED current is reduced.

When VDAC is lower than 1.00 V, the LED current is increased.

Some common applications for the above scheme include:

- LED binning
- Thermal fold-back using external NTC (negative temperature coefficient) thermistor

In the following application example, the thermistor used is NTCS0805E3684JXT (680 kΩ @ 25°C). R1 = 336 kΩ, R2 = 20 kΩ, and R3 = 8.45 kΩ. The LED current per channel is reduced from 97 mA at 25°C to 34 mA at 125°C.

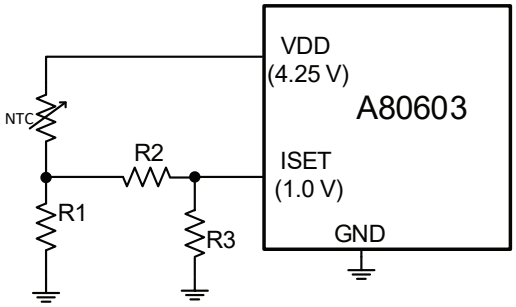



**Figure 32: Thermal foldback of LED current using NTC thermistor**

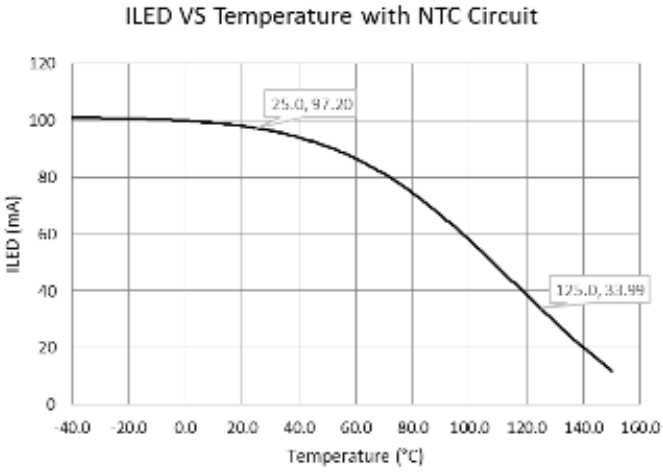



**Figure 33: LED current varies with temperature when using thermistor NTCS0805E3684JXT for thermal foldback**



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## VDD

The VDD pin provides regulated bias supply for internal circuits. Connect a $C_{VDD}$ capacitor with a value of 1 µF or greater to this pin. The internal LDO can deliver up to 2 mA of current with a typical VDD voltage of about 4.25 V. This allows it to serve as the pull up voltage for FAULT pin.

## Shutdown

If EN pin is pulled low for longer than $t_{EN(OFF)}$ (~16 ms), the A80603 enters shutdown (sleep mode). The next time EN pin goes high, all internal fault registers are cleared. The IC needs to go through a complete soft start process after PWM goes high.

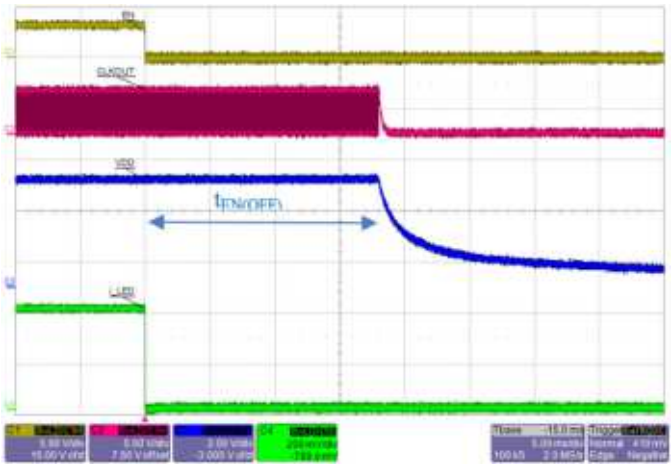



**Figure 34: After EN = L for ~16 ms, the IC completely shuts down so VDD (Blue) decays.**

There is an alternative way to reset the internal fault status registers. By keeping EN = H and PWM = L for longer than 16 ms, the A80603 clears all internal fault registers but does not go into sleep mode. The next time PWM pin goes high, the IC will still go through soft start process. The difference is that VDD voltage and CLKOUT signal are always available as long as EN = H.

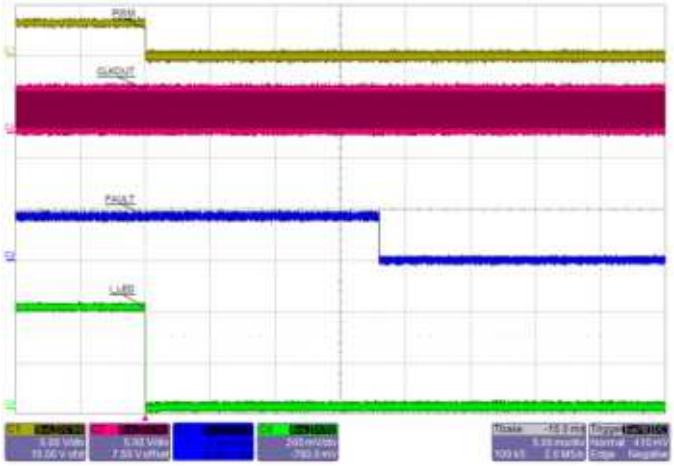



**Figure 35: As long as EN = H, the IC does not shut down VDD and CLKOUT. But internal latched faults are cleared by PWM = L for ~16 ms.**



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## FAULT DETECTION AND PROTECTION

### LED String Partial-Short Detect

All LED current sink pins (LED1 to LED4) are designed to withstand the maximum output voltage, as specified in the Absolute Maximum Ratings table. This prevents the IC from being damaged if $V_{OUT}$ is directly applied to an LED pin due to an output connector short.

In case of direct-short or partial-shorted fault in any LED string during operation, the LED pin with voltage exceeding $V_{LEDSC}$ will be removed from regulation. This prevents the IC from dissipating too much power due to large voltage drop across the LED current sink.

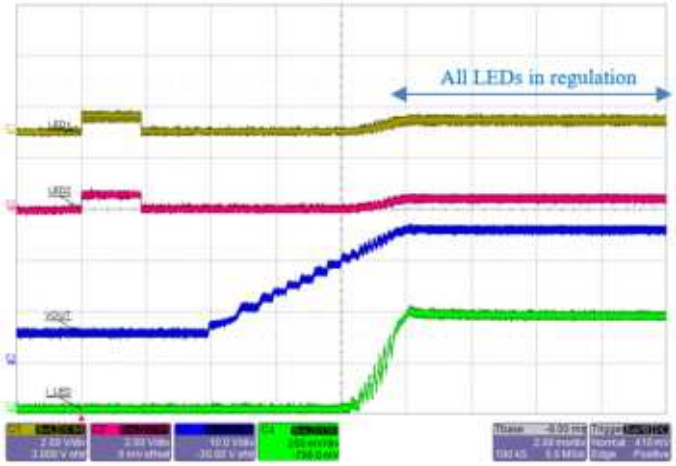



**Figure 36: A80603 Normal startup sequence showing voltage at LED1 and LED2 pins. $V_{IN}$ = 6 V, output = 8 × WLED in series, current = 4 × 100 mA**

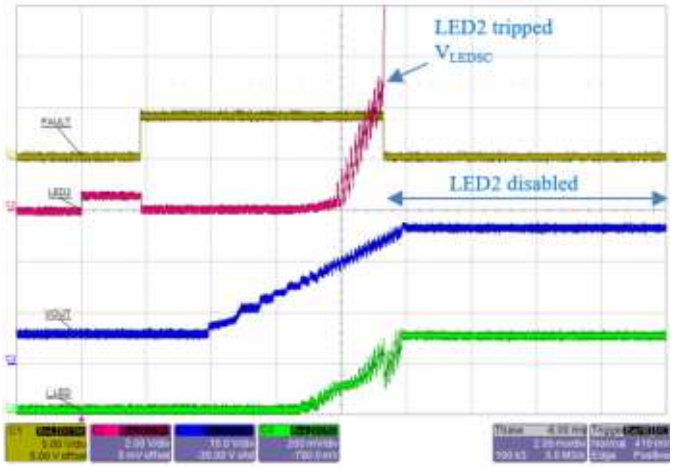



**Figure 37: A80603 startup sequence when LED string#2 has a partial-short fault (6 × WLED instead of 8). As soon as LED2 pin rises above $V_{LEDSC}$ (~5 V), the channel is disabled and FAULT = Low.**

For the A80603 only, the FAULT pin is pulled low in case any LED string is directly or partially shorted. However, the rest of the LED strings continue to operate. The FAULT pin is latched at low until it is reset by either EN = L or PWM = L for >16 ms.

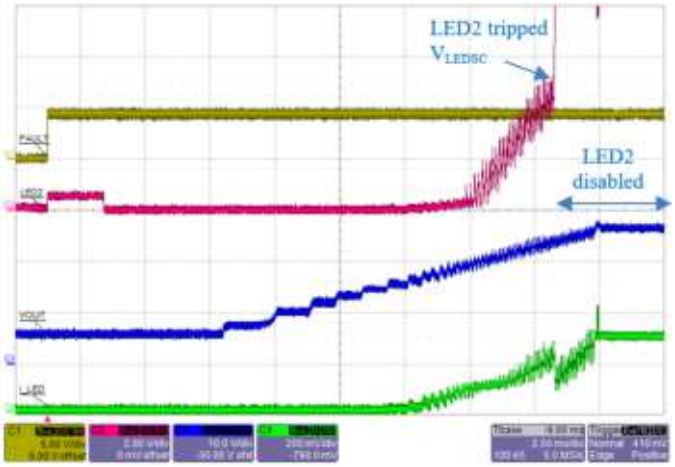



**Figure 38: A80603-1 startup sequence when LED string#2 has a partial-short fault (6 × WLED instead of 8). As soon as LED2 pin rises above $V_{LEDSC}$ (~5 V), the channel is disabled but FAULT remains High.**

At least one LED pin must be at regulation voltage (below ~1.2 V) for the LED string partial-short detection to activate. In case all of the LED pins are above regulation voltage (this could happen when the input voltage rises too high for the LED strings), they will continue to operate normally.

### Overvoltage Protection

The A80603 offers a programmable output overvoltage protection (OVP), plus a fixed secondary overvoltage protection (OVP2).

The OVP pin has a threshold level of 2.5 V typical. Overvoltage protection is tripped when current into this pin exceeds ~150 µA. A resistor can be used to set the OVP threshold up to 40 V approximately. This is sufficient for driving 11 white LEDs in series.

The formula for calculating the OVP resistor is shown below:

Equation 6: $$R_{OVP} = (V_{OVP} - V_{OVP(th)}) / i_{OVP(th)}$$

where $V_{OVP}$ is the desired OVP threshold, $V_{OVP(th)}$ = 2.5 V typical, $i_{OVP(th)}$ = 150 µA typical.

To determine the desired OVP threshold, take the maximum LED string voltage at cold and add ~10% margin on top of it.



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The OVP event is not a latched fault and, by itself, does not pull the FAULT pin to low. If the OVP condition occurs during a load dump, for example, the IC will stop switching but not shut down.

There are several possibilities of why an OVP condition is encountered during operation. The two most common being an open LED string and a disconnected output connector.

The waveform below shows a typical OVP condition. When one LED string becomes open, current through its LED driver drops to zero. The A80603 responses by boosting the output voltage higher. When output reaches OVP threshold, the LED string without current is removed from regulation. The rest of LED strings continue to draw current and drain down $V_{OUT}$. Once $V_{OUT}$ falls below ~97% OVP, boost will resume switching to power the remaining LED strings.

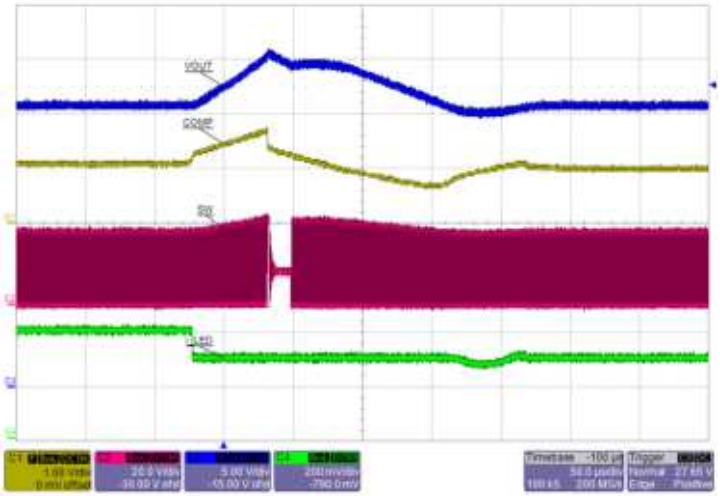



**Figure 39: An open-LED string faults causes $V_{OUT}$ to ramp up and trip OVP. The A80603 then disables the open LED string and continues with remaining strings.**

The A80603 also has a fixed secondary overvoltage protection to protect its internal switch. If the boost Schottky diode suddenly becomes open during normal operation, the energy stored in the inductor will force SW node voltage to increase rapidly. Once voltage on the SW pin exceeds OVP2, switching and all LED drivers are disabled. The IC remains latched off until it is reset.

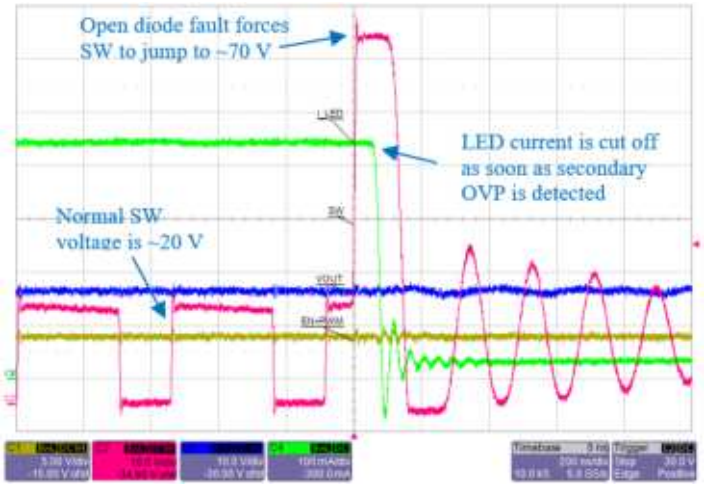



**Figure 40: An open-diode fault is introduced during normal operation. SW voltage jumps to ~70 V, causing the MOSFET to self-conduct and dissipate energy in the inductor.**

It should be noted that the SW MOSFET in A80603 is designed to avalanche and dissipate the excess energy safely in case of open-diode fault. Therefore the IC is not damaged even though SW node rises above AbsMax rating momentarily.

## Boost Switch Overcurrent Protection

The boost switch is protected with cycle-by-cycle current limiting set at typical 3.75 A, minimum 3.0 A. The waveform below shows normal switching at $V_{IN}$ = 6 V, $V_{OUT}$ = 25 V, and total LED current 400 mA.

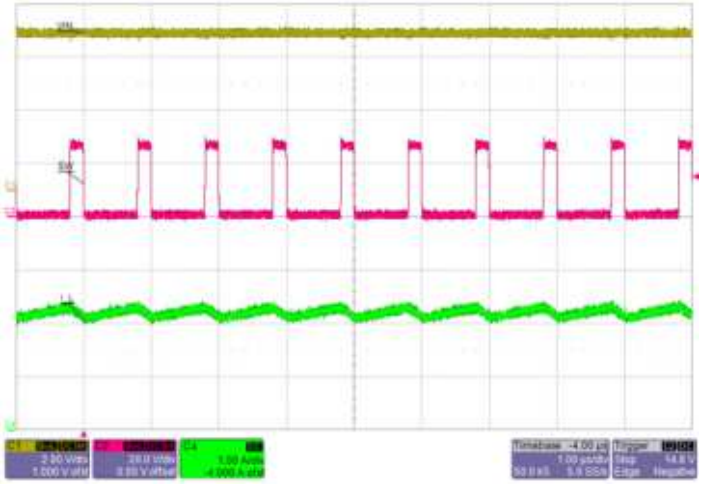



**Figure 41: Normal switching waveform at $V_{IN}$ = 6 V showing the SW node voltage (Red) and inductor current (Green).**



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When the input voltage is reduced further, input current increases and peak switch current reaches 3.2 A. SW_OCP is tripped and the IC skips a switching cycle to reduce the current

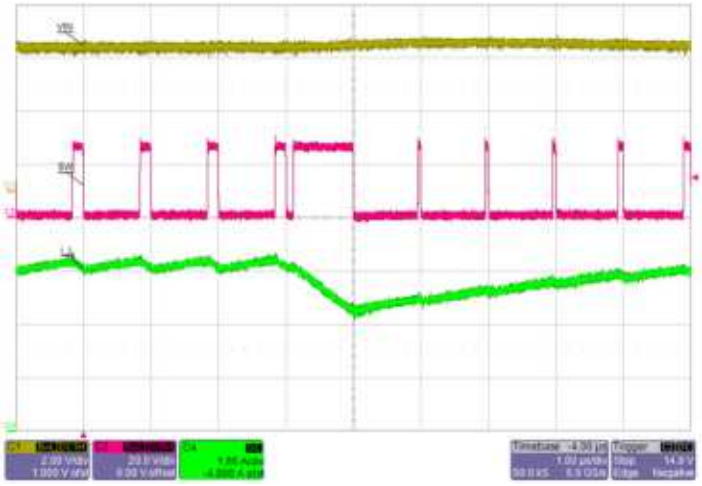
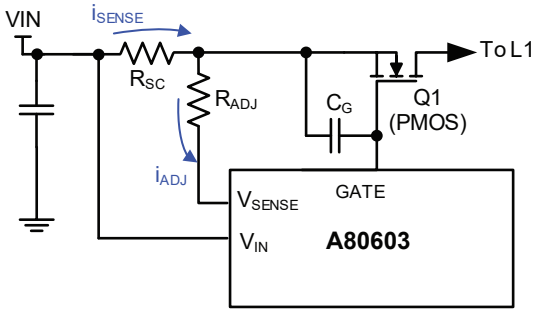


**Figure 42: When peak current in SW pin reaches ~3.2 A, overcurrent protection kicks in and the IC skips a switching cycle.**

There is also a secondary current limit ($I_{SW(LIM2)}$) that is sensed on the boost switch. This current limit once detected immediately shuts down the A80603. This current limit is set at about 33% higher than the pulse-by-pulse current limit. It is to protect the switch from destructive current spikes in case the boost inductor is shorted. Once this limit is tripped, the A80603 will immediately shut down and latch off.

## Input Overcurrent Protection and Disconnect Switch




$$V_{IN} - V_{SENSE} = R_{SC} \times i_{SENSE} + R_{ADJ} \times i_{ADJ}$$

**Figure 43: Optional input disconnect switch using a PMOSFET**

The primary function of the input disconnect switch is to protect the system and the device from catastrophic input currents during a fault condition.

If the input current level goes above the preset current limit threshold, the part will be shut down in less than 3 µs. This is a latched condition. The fault flag is also set to indicate a fault. This feature protects the input from drawing too much current during heavy load. It also prevents catastrophic failure in the system due to a short of the inductor or output capacitors shorted to GND.

The waveform below illustrates the typical input overcurrent fault condition. As soon as input OCP limit is reached, the part disables the gate of the disconnect switch Q1 and latches off.

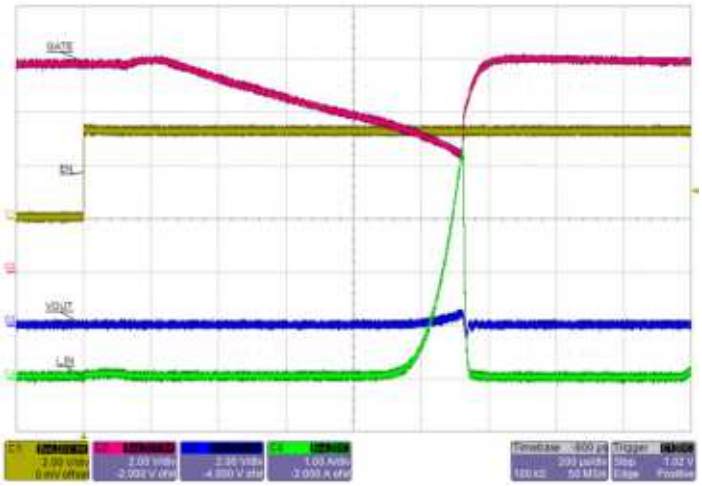


**Figure 44: Startup into an output shorted-to-GND fault. Input OCP is tripped when current (Green trace) exceeds 4 A. PMOS Gate (Red) is turned off immediately and IC latches off.**

During startup when Q1 first turns on, an inrush current flows through Q1 into the output capacitance. If Q1 turns on too fast (due to its low gate capacitance), the inrush current may trip input OCP limit. In this case, an external gate capacitance $C_G$ is added to slow down the turn-on transition. Typical value for $C_G$ is around 4.7 to 22 nF. Do not make $C_G$ too large, since it also slows down the turn-off transient during a real input OCP fault.

## Setting the Current Sense Resistor

The typical threshold for the current sense is 100 mV when $R_{ADJ}$ is 0 Ω. The A80603 can have this voltage trimmed using the $R_{ADJ}$ resistor. The typical trip point should be set to at least 3.75 A, which coincides with the cycle-by-cycle peak current limit typical threshold. A sample calculation is done below for 4.2 A of input current.

When $R_{ADJ}$ is not used:

Equation 7: $$V_{SENSETRIP} = R_{SC} \times i_{SENSE} = 100\ mV$$



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The desired sense resistor is $R_{SC}$ = 100 mV / 4.2 A = 23.8 mΩ. But this is not a standard E-24 resistor value. Pick the closest lower value which is 22 mΩ.

When $R_{ADJ}$ is used:

Equation 8: $V_{SENSETRIP} = R_{SC} \times i_{SENSE} + R_{ADJ} \times i_{ADJ}$

Therefore

$$R_{ADJ} = [V_{SENSETRIP} - (R_{SC} \times i_{SENSE})] / i_{ADJ}$$
$$= [100\ mV - 92.4\ mV] / 20\ \mu A = 380\ \Omega$$

## Input UVLO

When $V_{IN}$ and $V_{SENSE}$ rise above $V_{UVLOrise}$ threshold, the A80603 is enabled. The IC is disabled when $V_{IN}$ falls below $V_{UVLOfall}$ threshold for more than 50 µs. This small delay is used to avoid shutting down because of momentary glitches in the input power supply.

## Fault Protection During Operation

The A80603 constantly monitor the state of the system to determine if any fault conditions occur during normal operation. The response to a triggered fault condition is summarized in the table below. It is important to note that there are several points at which the A80603 monitors for faults during operation. The locations are input current, switch current, output voltage, switch voltage, and LED pins. Some of the protection features might not be active during startup to prevent false triggering of fault conditions.

The possible fault conditions that the part can detect include:

- Open LED Pin or open LED string
- Shorted or partially shorted LED string
- LED pin shorted to GND
- Open or shorted boost diode
- Open or shorted boost inductor
- VOUT short to GND
- SW shorted to GND
- ISET shorted to GND
- FSET shorted to GND
- Input disconnect switch drain shorted to GND

Note that some of these faults will not be protected if the input disconnect switch is not being used. An example of this is VOUT short to GND fault.



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**Table 5: A80603 Fault Mode Table**

| Fault Name | Type | Active | Fault Flag Set | Description | Boost Switch | Disconnect Switch | LED Sink drivers |
|---|---|---|---|---|---|---|---|
| Primary Switch Overcurrent Protection (Cycle-By-Cycle Current Limit) | Auto-restart | Always | NO | This fault condition is triggered when the SW current exceeds the cycle-by-cycle current limit, $I_{SW(LIM)}$.The present SW on-time is truncated immediately to limit the current. Next switching cycle starts normally. | Off for a single cycle | ON | ON |
| Secondary Switch Current Limit | Latched Off | Always | YES | When current through boost switch exceeds secondary SW current limit ($i_{SW(LIM2)}$) the device immediately shuts down the disconnect switch, LED drivers and boost. The Fault flag is set. To reset the fault the EN or PWM pin needs to be pulled low for 16 ms. | OFF | OFF | OFF |
| Input Disconnect Current Limit | Latched Off | Always | YES | The device is immediately shut off if the voltage across the input sense resistor is above the $V_{SENSEtrip}$ threshold. To reset the fault the EN or PWM pin must be pulled low for 16 ms. | OFF | OFF | OFF |
| Secondary OVP | Latched Off | Always | YES | Secondary overvoltage protection is used for open diode detection. When diode D1 opens, the SW pin voltage will increase until $V_{OVP(SEC)}$ is reached . This fault latches the IC. The input disconnect switch and LED drivers are disabled. To reset the fault the EN or PWM pin needs to be pulled low for 16 ms. | OFF | OFF | OFF |
| LEDx Pin Shorted to GND | Auto-restart | Startup | YES | If any of the LED pins is determined to be shorted to GND when PWM first goes high, soft-start process is halted. Only when the short is removed, then soft-start is allowed to proceed. | OFF | ON | OFF |
| LEDx Pin Open | Auto-restart | Normal operation | YES | If an LED string is not getting enough current, the device will first respond by increasing the output voltage until OVP is reached. Any LED string that is still not in regulation will be disabled. The device will then go back to normal operation by reducing the output voltage to the appropriate voltage level. | ON | ON | OFF for open pins. ON for all others. |
| ISET Short Protection | Auto-restart | Always | YES | Fault occurs when the ISET current goes above 150% of max current. The boost will stop switching and the IC will disable the LED sinks until the fault is removed. When the fault is removed, the IC will try to regulate to the preset LED current. | OFF | ON | OFF |
| FSET/SYNC Short Protection | Auto-restart | Always | YES | Fault occurs when the FSET current goes above 150% of max current. The boost will stop switching, Disconnect switch will turn off and the IC will disable the LED sinks until the fault is removed. When the fault is removed, the IC will try to restart with soft-start. | OFF | OFF | OFF |
| Overvoltage Protection | Auto-restart | Always | NO | Fault occurs when current into OVP pin exceeds $i_{OVP(th)}$ (typically 150 µA). The IC will immediately stop switching but keep the LED drivers active, to drain down the output voltage. Once the output voltage decreases to ~97% OVP level, the IC will restart switching to regulate the output current. | STOP during OVP event. | ON | ON |
| Undervoltage Protection | Auto-restart | Always | YES | Device immediately shuts off boost and current sinks if the voltage at VOUT is below $V_{UVP(th)}$. This may happen if VOUT is shorted to GND, or boost diode is open before startup. It will auto-restart once the fault is removed. | OFF | ON | OFF |
| LED String Partial Short Detection | Latched and Continue | Always | YES | Fault occurs if an LED pin voltage exceeds $V_{LEDSC}$ with its current sink in regulation, while at least one other LED pin is below ~1.2 V. This may happen when two or more LEDs are shorted within a string. The LED string exceeding the threshold will then be disabled and removed from operation. This fault cannot be detected if PWM on-time is < $t_{LEDSD}$ (5.5 µs max) | ON | ON | OFF for shorted string. ON for all others. |
| Overtemperature Protection | Auto-restart | Always | YES | Fault occurs when the die temperature exceeds the over-temperature threshold, typically 170°C. IC will restart after temperatures drops lower by $T_{SDHYS}$ | OFF | OFF | OFF |
| $V_{IN}$ UVLO | Auto-restart | Always | NO | Fault occurs when $V_{IN}$ drops below $V_{UVLO(fall)}$, which is 3.9 V max. This fault resets all latched faults. | OFF | OFF | OFF |



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**Table 6: A80603-1 Fault Mode Table**

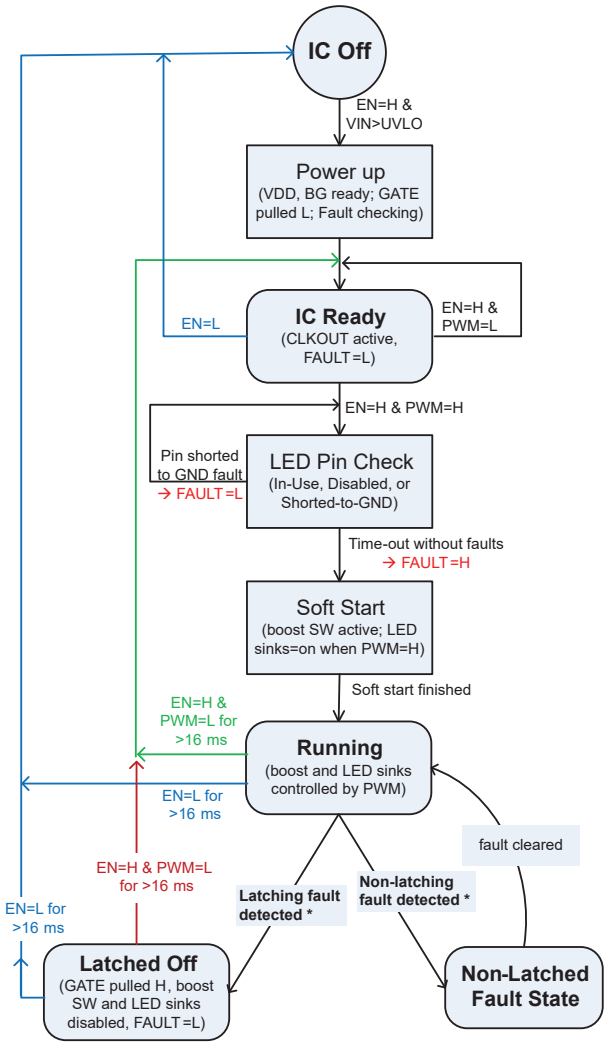
| Fault Name | Type | Active | Fault Flag Set | Description | Boost Switch | Disconnect Switch | LED Sink drivers |
|---|---|---|---|---|---|---|---|
| Primary Switch Overcurrent Protection (Cycle-By-Cycle Current Limit) | Auto-restart | Always | NO | This fault condition is triggered when the SW current exceeds the cycle-by-cycle current limit, $I_{SW(LIM)}$.The present SW on-time is truncated immediately to limit the current. Next switching cycle starts normally. | Off for a single cycle | ON | ON |
| Secondary Switch Current Limit | Latched Off | Always | YES | When current through boost switch exceeds secondary SW current limit ($i_{SW(LIM2)}$) the device immediately shuts down the disconnect switch, LED drivers and boost. The Fault flag is set. To reset the fault the EN or PWM pin needs to be pulled low for 16 ms. | OFF | OFF | OFF |
| Input Disconnect Current Limit | Latched Off | Always | YES | The device is immediately shut off if the voltage across the input sense resistor is above the $V_{SENSEtrip}$ threshold. To reset the fault the EN or PWM pin must be pulled low for 16 ms. | OFF | OFF | OFF |
| Secondary OVP | Latched Off | Always | YES | Secondary overvoltage protection is used for open diode detection. When diode D1 opens, the SW pin voltage will increase until $V_{OVP(SEC)}$ is reached . This fault latches the IC. The input disconnect switch and LED drivers are disabled. To reset the fault the EN or PWM pin needs to be pulled low for 16 ms. | OFF | OFF | OFF |
| LEDx Pin Shorted to GND | Auto-restart | Startup | NO * | If any of the LED pins is determined to be shorted to GND when PWM first goes high, soft-start process is halted. Only when the short is removed, then soft-start is allowed to proceed. | OFF | ON | OFF |
| LEDx Pin Open | Auto-restart | Normal operation | NO * | If an LED string is not getting enough current, the device will first respond by increasing the output voltage until OVP is reached. Any LED string that is still not in regulation will be disabled. The device will then go back to normal operation by reducing the output voltage to the appropriate voltage level. | ON | ON | OFF for open pins. ON for all others. |
| ISET Short Protection | Auto-restart | Always | YES | Fault occurs when the ISET current goes above 150% of max current. The boost will stop switching and the IC will disable the LED sinks until the fault is removed. When the fault is removed, the IC will try to regulate to the preset LED current. | OFF | ON | OFF |
| FSET/SYNC Short Protection | Auto-restart | Always | YES | Fault occurs when the FSET current goes above 150% of max current. The boost will stop switching, Disconnect switch will turn off and the IC will disable the LED sinks until the fault is removed. When the fault is removed, the IC will try to restart with soft-start. | OFF | OFF | OFF |
| Overvoltage Protection | Auto-restart | Always | NO | Fault occurs when current into OVP pin exceeds $i_{OVP(th)}$ (typically 150 µA). The IC will immediately stop switching but keep the LED drivers active, to drain down the output voltage. Once the output voltage decreases to ~97% OVP level, the IC will restart switching to regulate the output current. | STOP during OVP event. | ON | ON |
| Undervoltage Protection | Auto-restart | Always | YES | Device immediately shuts off boost and current sinks if the voltage at VOUT is below $V_{UVP(th)}$. This may happen if VOUT is shorted to GND, or boost diode is open before startup. It will auto-restart once the fault is removed. | OFF | ON | OFF |
| LED String Partial Short Detection | Auto-restart | Always | NO * | Fault occurs if an LED pin voltage exceeds $V_{LEDSC}$ with its current sink in regulation, while at least one other LED pin is below ~1.2 V. This may happen when two or more LEDs are shorted within a string. The LED string exceeding the threshold will then be disabled and removed from operation. This fault cannot be detected if PWM on-time is < $t_{LEDSD}$ (5.5 µs max) | ON | ON | OFF for shorted string. ON for all others. |
| Overtemperature Protection | Auto-restart | Always | YES | Fault occurs when the die temperature exceeds the over-temperature threshold, typically 170°C. IC will restart after temperatures drops lower by $T_{SDHYS}$ | OFF | OFF | OFF |
| $V_{IN}$ UVLO | Auto-restart | Always | NO | Fault occurs when $V_{IN}$ drops below $V_{UVLO(fall)}$, which is 3.9 V max. This fault resets all latched faults. | OFF | OFF | OFF |

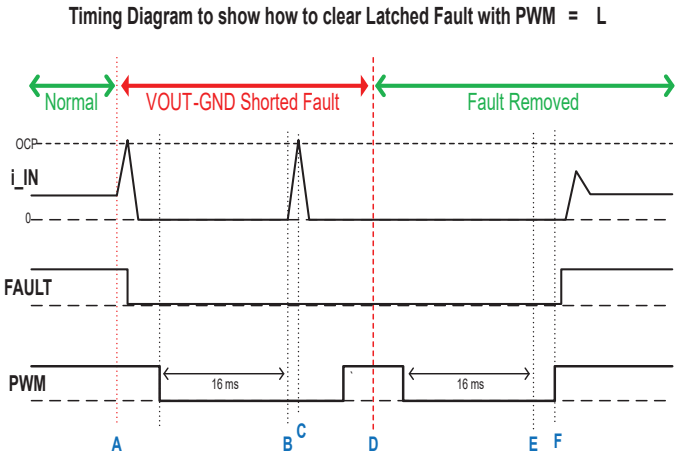
* Indicates different behavior between A80603 and A80603-1.



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## A80603 Fault Recovery Mechanism




**Explanation of events** :

**A**: VOUT-to-GND Short fault introduced. IC trips input OCP which is a latched fault. FAULT is then pulled Low and IC stays in Latched mode (CLKOUT remains available).

**B**: After PWM=L for 16 ms, IC clears the latched fault internally but FAULT stays Low.

**C**: Input OCP is tripped again since VOUT is still shorted to GND. So IC returns to Latched mode again and FAULT remains Low.

**D**: PWM=H and VOUT-to-GND Short fault is removed, but IC cannot restart since it is still in Latched mode.

**E**: After PWM=L for 16 ms, IC clears the latched fault internally again

**F**: At the next PWM=H, IC restarts and detected no faults, so FAULT finally goes High

* Note: Fault conditions may be detected in any state or during any state transition. Most faults are non-latching, meaning the IC will auto-restart as soon as the fault is removed. Only the following faults are latching: Input Disconnect Overcurrent, SW Secondary OCP, and SW Secondary OVP.

Latching faults can only be cleared by:

1. Reset the IC by bring VIN below UVLO,
2. Reset the IC by bring EN=L for >16 ms, or
3. EN=H and PWM=L for >16 ms.

The last method has the advantage that it does not interrupt the CLKOUT signal. In case the fault condition (e.g. VOUT shorted to GND) is still present when the latching fault is cleared by PWM=L for >16 ms, the IC will trip fault once again and stay latched off.

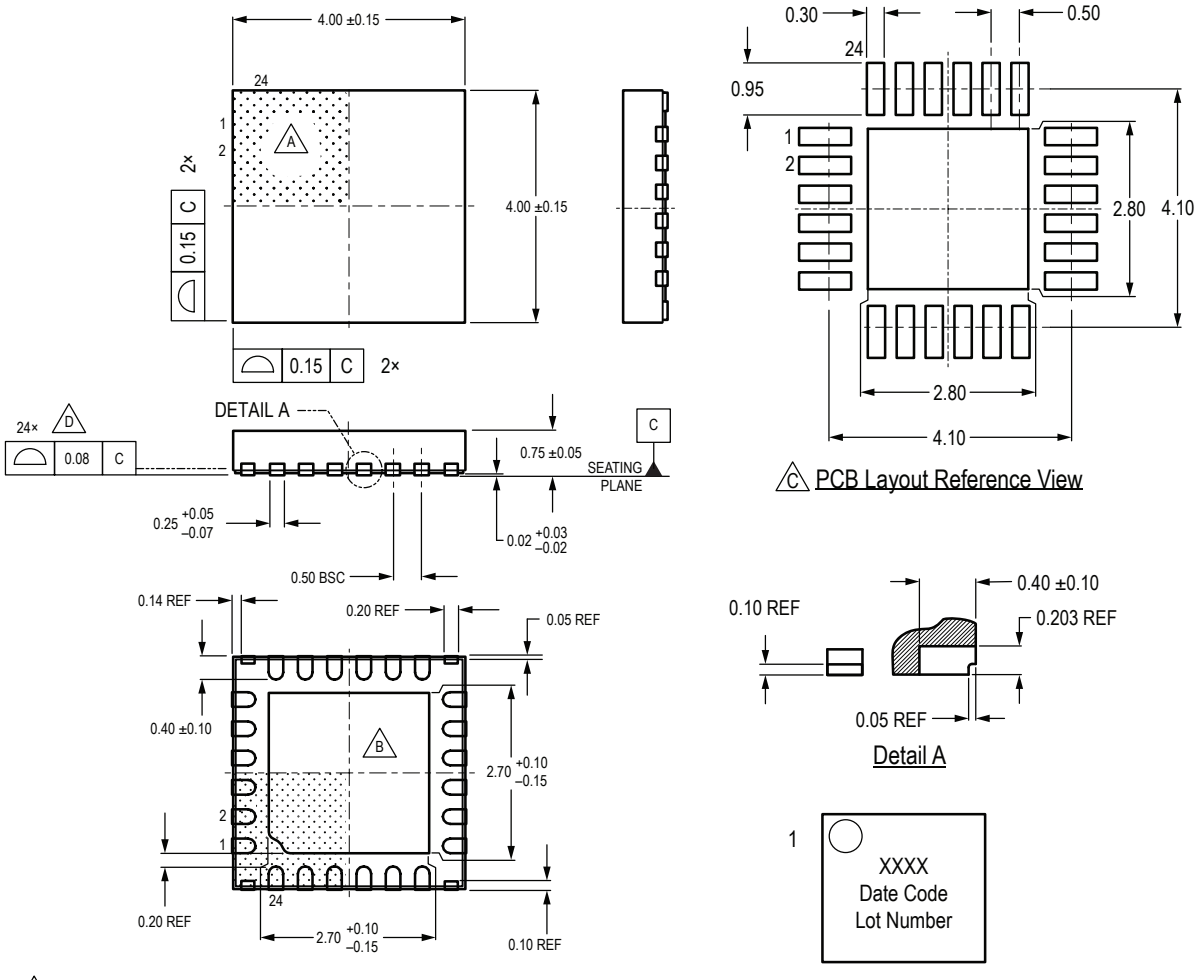


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## PACKAGE OUTLINE DRAWING

**For Reference Only – Not for Tooling Use**

(Reference Allegro DWG-0000222 Rev. 6 or JEDEC MO-220WGGD)
Dimensions in millimeters – NOT TO SCALE.
Exact case and lead configuration at supplier discretion within limits shown.




A Terminal #1 mark area.

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion).

C Reference land pattern layout (reference IPC7351 QFN50P400X400X80-25W6M); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5).

D Coplanarity includes exposed thermal pad and terminals.

E Branding scale and appearance at supplier discretion.

E Standard Branding Reference View

Line 1: Part Number
Line 2: 4-digit Date Code
Line 3: Characters 5, 6, 7, 8 of Assembly Lot Number

Pin 1 Dot top left
Center align

**Figure 45: Package ES, 24-Pin 4 mm × 4 mm QFN with Exposed Thermal Pad and Wettable Flank**



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## APPENDIX A: DESIGN EXAMPLE

This section provides step-by-step instructions to select component values for an A80603 application.

For the purposes of this example, the following operating conditions are assumed:

- $V_{IN}$ = 12 V nominal (6 V min, 18 V max)
- Number of LED channels nc = 4
- Number of series LEDs per channel n = 7
- LED current per channel $I_{LED}$ = 120 mA
- LED forward drop $V_f$ = 3.2 V max at cold
- Switching frequency $f_{SW}$ = 2.15 MHz
- Dithering modulation frequency $f_{DITH}$ = 1 kHz
- Dithering frequency range $\Delta f_{SW}$ = ±5%
- Max ambient temperature $T_{A(max)}$ = 65°C
- PWM dimming frequency $f_{PWM}$ = 200 Hz

**Step 1:** Program the Switching Frequency from Equation 1:

$$R_{FSET} = (21.5 / f_{SW}) - 0.2$$

where $f_{SW}$ is in MHz and $R_{FSET}$ is in kΩ.

Substitute $f_{SW}$ = 2.15 MHz to get $R_{FSET}$ = 9.8 kΩ (pick 10 kΩ).

**Step 1a:** Program the Dithering Modulation Frequency from Equation 3:

$$C_{DITH}\,(nF) = 25 / f_{DM}\,(kHz)$$

Substitute $f_{DM}$ = 1 kHz to get $C_{DITH}$ = 25 nF (pick 22 nF).

**Step 1b:** Select Dithering Range from Equation 4:

$$R_{DITH} = 20 \times R_{FSET} / Range\ (\pm\%)$$

Substitute Range = 5 and $R_{FSET}$ = 10 kΩ to get $R_{DITH}$ = 40 kΩ (pick 40.2 kΩ). The switching frequency now linearly sweeps between 2.04 and 2.26 MHz.

**Step 2:** Determine the LED current set Resistor $R_{ISET}$ from Equation 2:

$$R_{ISET} = 832 / I_{LED}$$

Substitute $I_{LED}$ = 120 mA to get $R_{ISET}$ = 6.93 kΩ (pick 6.98 kΩ).

**Step 3:** Determining the OVP resistor according to Equation 7:

$$R_{OVP} = (V_{OVP} - V_{OVP(th)}) / i_{OVP(th)}$$

The nominal output voltage is:

$$V_{OUT_nom} = n \times V_f + V_{REG}$$

where $V_{REG}$ is the LED pin regulation voltage. Substitute n = 7, $V_f$ = 3.2 V, and $V_{REG}$ = 0.85 V to get $V_{OUT_nom}$ = 23.25 V. $V_{OVP(th)}$ = 2.5 V and $I_{ovp(th)}$ = 150 µA.

Set the OVP threshold voltage approximately 10% higher, to account for error margin and component tolerances:

$$V_{OVP} = V_{OUT_nom} \times 1.1 = 25.6\ V$$

The OVP resistor is therefore:

$$R_{OVP} = (25.6\ V - 2.5\ V) / 150\ \mu A = 154\ k\Omega$$

**Step 3a:** Check to ensure the maximum boost duty cycle is sufficient to achieve the required conversion ratio.

$$D_{MAX(boost)} = 1 - t_{SW(off)} \times f_{SW(max)}$$

where $t_{SW(off)}$ is the worst-case minimum SW off-time, and $f_{SW(max)}$ is the maximum switching frequency with dithering.

Substitute $t_{SW(off)}$ = 66 ns and $f_{SW(max)}$ = 2.26 MHz to get $D_{MAX(boost)}$ = 0.851.

Theoretical maximum output voltage at the lowest input voltage is:

$$V_{OUT(max)} = V_{IN(min)} / (1 - D_{MAX(boost)}) - V_D$$

where $V_D$ is the forward drop of boost Schottky diode.

Substitute $V_{IN(min)}$ = 6 V, $D_{MAX(boost)}$ = 0.851, and $V_D$ = 0.4 V to get $V_{OUT(max)}$ = 39.9 V.

Theoretical $V_{OUT(max)}$ has to be greater than $V_{OVP}$. If this is not the case, then switching frequency of the boost converter must be reduced to meet the maximum duty cycle requirement.

**Step 4 – Inductor selection:** The inductor must be chosen based on ripple current requirement. In most applications due to stringent EMI requirements, the system also needs to operate in continuous conduction mode (CCM) throughout the whole input voltage range. A simple guideline is to start with 30% peak-to-peak ripple current at nominal input and output voltages.

**Step 4a:** Determine the Boost Duty Cycle:

$$D = 1 - V_{IN} / (V_{OUT} + V_D)$$

For nominal operation, substitute $V_{IN_nom}$ = 12 V, $V_{OUT_nom}$ = 23.25 V and $V_D$ = 0.4 V to get $D_{nom}$ = 0.493.

**Step 4b:** Calculate the nominal Input Current based on estimated efficiency:

$$i_{IN} = V_{OUT} \times i_{OUT} / (V_{IN} \times \eta)$$

where η = efficiency of the converter (typically in the 85% to 90% range).

For nominal operation, substitute $V_{OUT}$ = 23.25 V, $i_{OUT}$ = 0.6 A, $V_{IN}$ = 12 V, and η = 0.85 to get $i_{IN}$ = 1.09 A.



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**Step 4c:** Select Boost Inductance based on 30% Ripple Current.

For nominal operation, $\Delta i_L = 0.3 \times i_{IN} = 0.327$ A.

$$\Delta i_L = t_{ON} \times V_{IN} / L = D \times V_{IN} / (f_{SW} \times L)$$

Therefore:

$$L = D \times V_{IN} / (f_{SW} \times \Delta i_L)$$

Substitute $D_{nom} = 0.493$, $V_{IN_nom} = 12$ V, and $f_{SW} = 2.15$ MHz to get L = 7.1 µH (pick 6.8 µH).

**STEP 4d:** Determine the maximum and minimum input current to the system. The maximum current determines the inductor's saturation current rating. The minimum current determines its critical inductance.

Maximum input current occurs at minimum $V_{IN}$ and maximum $V_{OUT}$ (OVP).

$$i_{IN_max} = V_{OVP} \times i_{OUT} / (V_{IN_min} \times \eta)$$

Substitute $V_{OVP} = 25.6$ V, $V_{IN_min} = 6$ V, and $\eta = 0.85$ to get $i_{IN_max} = 2.41$ A.

Peak inductor current:

$$i_{L_peak} = i_{IN_max} + \Delta i_L / 2$$

At minimum $V_{IN} = 6$ V, D = 0.769 (using equation in step 4a), $\Delta i_L = 0.316$ A (using equation in step 4c), and so $i_{L_peak} = 2.41 + 0.316 / 2 = 2.57$ A. Therefore, the inductor should have a saturation current of at least 3.1 A (20% higher than $i_{L_peak}$).

Minimum input current occurs at maximum $V_{IN}$ and nominal $V_{OUT}$.

$$i_{IN_min} = V_{OUT_nom} \times i_{OUT} / (V_{IN_max} \times \eta)$$

Substitute $V_{OUT_nom} = 23.25$ V, $I_{OUT} = 480$ mA, $V_{IN_max} = 18$ V, and $\eta = 0.9$ to get $i_{IN_min} = 0.689$ A.

At maximum $V_{IN} = 18$ V, D = 0.239 (using equation in step 4a), $\Delta i_L = 0.294$ A (using equation in step 4c), and so $i_{L_valley} = 0.689 - 0.294 / 2 = 0.542$ A. Therefore, the converter operates in CCM throughout the input voltage range.

**Step 5:** Verify that there is sufficient slope compensation for the inductor chosen. The A80603 generates a variable internal Slope Comp according to $f_{SW}$ and $V_{IN}$.

- If $V_{IN}$ is between 9 V and 15 V:
  $$SC = 3 \times f_{SW} \times V_{IN} / 12$$
- If $V_{IN} < 9$ V:
  $$SC = 3 \times f_{SW} \times 9 / 12$$
- If $V_{IN} > 15$ V:
  $$SC = 3 \times f_{SW} \times 15 / 12$$

where $f_{SW}$ is in MHz and SC is in A/µs.

For example, at $f_{SW} = 2.15$ MHz and $V_{IN} = 6$ V, SC = 4.84 A/µs

The falling slope of inductor current is given as:

$$di_L/dt = -\Delta i_L / t_{OFF} = -\Delta i_L \times f_{SW} / (1 - D)$$

Based on equations from previous section, at $V_{IN} = 6$ V and $V_{OUT(OVP)} = 25.6$ V, D = 0.769 and $\Delta i_L = 0.316$ A. Therefore $|di_L/dt| = 2.94$ A/µs, which is slower than the internal slope. That means there is sufficient slope compensation.

In case the negative slope of inductor current is faster than the internal slope comp, a higher inductance value must be used.

**Step 6:** Choose the input disconnect switch components.

Set the input disconnect switch current limit at least 20% above the SW cycle-by-cycle current limit:

$$i_{SENSE} = 4.5\ A \times 1.2 = 5.4\ A$$

$$R_{SC} = V_{SENSETRIP} / i_{SENSE} = 18.5\ m\Omega$$

where $V_{SENSETRIP} = 100$ mV.

Pick the closest lower resistance value, which is 18 mΩ.

$$R_{ADJ} = [V_{SENSETRIP} - (R_{SC} \times i_{SENSE})] / i_{ADJ} = 140\ \Omega$$

where $i_{ADJ} = 20$ µA.

Select the input disconnect switch P-channel MOSFET based on its drain-source breakdown voltage and on-resistance.

The SQJ459EP can be used in this case. It has $V_{DS} = -60$ V and $R_{DS(ON)} = 24$ mΩ at $V_{GS} = -4.5$ V.



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**Step 7:** Select the switching diode.

A Schottky barrier diode (SBD) is typically selected based on its voltage and current ratings:

- The reverse voltage rating must be higher than the maximum voltage stress, which is equal to the OVP threshold in this case.
- The average forward current rating must be higher than the total LED current. The peak current rating of the diode must exceed the secondary current limit, $I_{CS(LIM2)}$, which is $1.4 \times I_{CS(LIM1)}$.

Another critical parameter is the diode's reverse leakage current at hot. This is especially important when using PWM dimming. During PWM off time, the boost converter is not switching, so voltage at output capacitor decays due to leakage current. This increases output ripple voltage, which may generate audible noise from ceramic capacitors.

Make sure to verify the diode's reverse current at hot (such as 125°C) and at the nominal $V_{OUT}$. As a general guideline, look for a diode with leakage of 100 µA or less. If necessary, consider using a diode with higher voltage rating (such as 100 V instead of 50 V). Doing so can significantly reduce the leakage current at nominal $V_{OUT}$.

For this design example, a 100 V, 3 A Schottky diode SS3H10 is selected. It has a very low $i_R$ = 50 µA at $T_J$ = 125°C and $V_R$ = 30 V.

**Step 8:** Selection of output capacitors.

The use of multilayer ceramic capacitor (MLCC) is recommended. MLCC has extremely low ESR, which is necessary to reduce output switching ripple for boost converter. In addition, the total output capacitance needs to be sufficient to reduce output droop during PWM dimming operation.

The biggest contributing factors for total output capacitance are PWM off-time and leakage current ($i_{LK}$). This current is mainly due to the reverse current of switching diode, plus a small/negligible leakage current into the OVP pin.

In this design example, the PWM dimming frequency is 200 Hz with minimum duty cycle of 0.01%. So the maximum PWM off-time is essentially $t_{OFF}$ = 5 ms. A typical goal is to keep the output voltage variation at 250 mV or less to avoid audible noise.

$$\Delta V_{OUT} = t_{OFF} \times i_{LK} / C_{OUT}$$

Therefore:

$$C_{OUT} = t_{OFF} \times i_{LK} / \Delta V_{OUT}$$

Substitute $t_{OFF}$ = 5 ms, $i_{LK}$ = 110 µA, and $\Delta V_{OUT}$ = 0.25 V to get $C_{OUT}$ = 2.2 µF.

A major problem with multilayer ceramic capacitor (MLCC) is that its actual capacitance drops with respect to DC bias. For example, the capacitance of a 4.7 µF, 50 V, 0805 MLCC may be derated by 80% when it is biased at 25 V. That means its real capacity is less than 1 µF in actual application.

An MLCC of larger physical size and higher voltage rating typically suffers less derating problem. For example, a 4.7 µF, 50 V, 1210 MLCC may retain 3.3 µF of capacitance at 25 V. This is shown in the table below:

| Part Number | Package | Rated Capacitance at 0 V (µF) | Derating at 25 V | Actual Capacitance at 25 V (µF) |
|---|---|---|---|---|
| GRM21BC71H475KE11 | 0805 | 4.7 | –80% | 0.94 |
| GRM31CR71H475MA12 | 1206 | 4.7 | –45% | 2.59 |
| GRM32ER71H475KA88 | 1210 | 4.7 | –30% | 3.29 |

**Step 9:** Selection of input capacitor.

A combination of MLCC and electrolytic capacitor is recommended. The MLCC provides low ESR to reduce input switching ripple. The electrolytic capacitor provides larger capacitance to stabilize input voltage during PWM dimming operation.

A good rule of thumb is to set the input voltage ripple $\Delta V_{IN}$ to be 1% of the minimum input voltage. The minimum input capacitor requirements are as follows.

$$C_{IN} = \Delta i_L / (8 \times f_{SW} \times \Delta V_{IN})$$

Substitute $\Delta i_L$ = 0.316 A at $V_{IN}$ = 6 V (from step 4d), $\Delta V_{IN}$ = 0.06 V, and $f_{SW}$ = 2.15 MHz to get $C_{IN}$ = 0.306 µF. Due to the DC bias derating, the actual MLCC selected should be rated 1 µF or higher. For this design, a 2.2 µF capacitor is used.

A much larger input capacitance is required to provide the inrush current during PWM dimming operation. The exact requirement depends on many external factors, such as length of power cables and response time of the power supply. As a first-order estimate: assume the power supply takes 25 µs to response, and the input capacitor must keep the $V_{IN}$ dip under 0.2 V while input current ramps up from zero to full load. The following is needed:

$$C_{IN} = i_{IN} \times t_{PS} / (8 \times \Delta V_{IN})$$

Substitute $i_{IN}$ = 3.01 A at $V_{IN}$ = 6 V (from step 4d), $\Delta V_{IN}$ = 0.2 V and $t_{PS}$ = 25 µs to get $C_{IN}$ = 47 µF. Use an electrolytic capacitor of 47 µF in parallel with the MLCC.



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**Step 10:** Selection of Compensation Components.

For most applications, the compensation network shown in Figure 46 is sufficient for stable circuit performance.

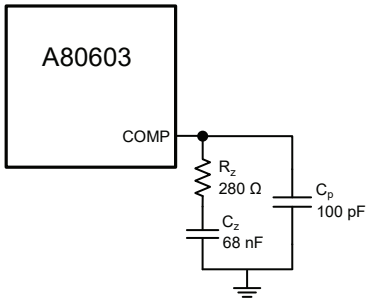



**Figure 46: Compensation Network Schematic**

This application will use the following compensation values: $R_z$ = 280 Ω, $C_z$ = 68 nF, $C_p$ = 100 pF.

For applications where a higher voltage control loop crossover frequency is desired, $R_z$ can be increased. To increase phase margin at the crossover frequency, $C_z$ can be increased, but exceeding 470 nF is not recommended. Control loop stability should be evaluated in any application to ensure proper performance.

The following schematic diagram shows calculated component values from the design example. The other components that are not discussed in this design example are recommended for proper circuit performance.

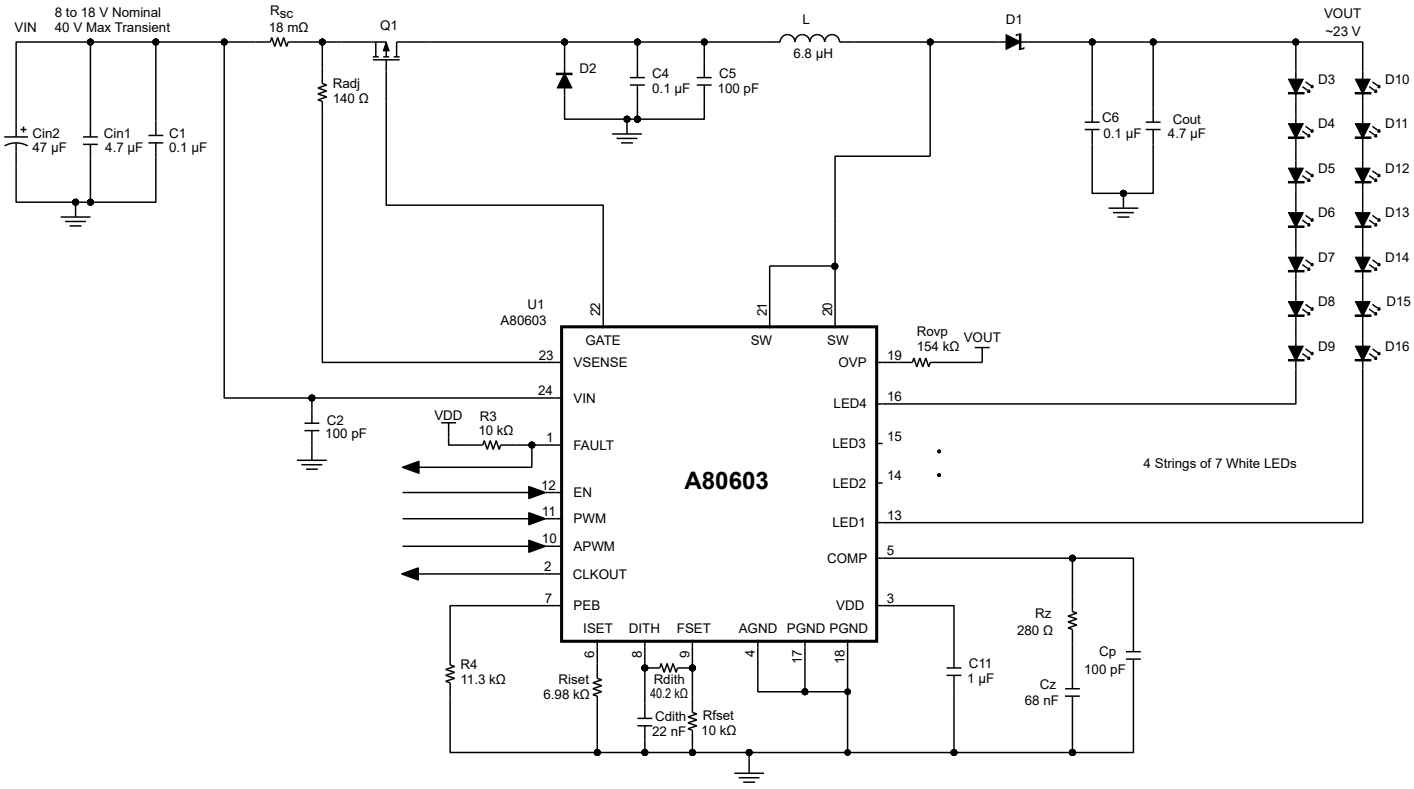



**Figure 47: Boost Design Example Schematic**



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**Table 7: Boost Design Example Bill of Materials**

| Designator | Quantity | Value | Description | Footprint | Comment |
|---|---|---|---|---|---|
| Cin1, Cout | 2 | 4.7 µF | CAP CER, 50V, X7R | 1210 | |
| Cin2 | 1 | 47 µF | POLARIZED CAP (RADIAL) | Cap Radial 8 mm surface mount | Panasonic EEE-TG1H470UP |
| C1, C4, C6 | 3 | 0.1 µF | CAP CER, 50 V, X7R | 0603 | |
| C2, C5, Cp | 3 | 100 pF | CAP CER, 50 V, COG/NPO | 0603 | |
| C11 | 1 | 1 µF | CAP CER, 16 V, X7R | 0603 | |
| Cdith | 1 | 22 nF | CAP CER, 25 V, X7R | 0603 | |
| Cz | 1 | 68 nF | CAP CER, 10 V, X7R | 0603 | |
| D1 | 1 | | DIODE SCHOTTKY, 100 V, 3 A | DO-214AB | Vishay SS3H10-E3/9AT |
| D2 | 1 | | DIODE GENERAL PURPOSE, 100 V, 300 mA | SOD123 | Diodes Incorporated 1N4148W-7 |
| D3-D31 | 28 | | LED, WHITE, 3.2 V FORWARD VOLTAGE DROP | | Total of 28 for 4 strings of 7 LEDs |
| L | 1 | 6.8 µH | Inductor, 6 A, 27 mΩ | | Coilcraft XEL5050-682 |
| Q1 | 1 | | MOSFET P-CHANNEL, 60 V, 52 A | PowerPAK SO-8L | Vishay Siliconix SQJ459EP-T1_GE3 |
| R3, Rfset | 2 | 10 kΩ | RES, 1% | 0603 | |
| R4 | 1 | 11.3 kΩ | RES, 1% | 0603 | |
| Radj | 1 | 140 Ω | RES, 1% | 0603 | |
| Rdith | 1 | 40.2 kΩ | RES, 1% | 0603 | |
| Riset | 1 | 6.98 kΩ | RES, 1% | 0603 | |
| Rovp | 1 | 154 kΩ | RES, 1% | 0603 | |
| Rsc | 1 | 18 mΩ | RES, 1% | 1206 | |
| Rz | 1 | 280 Ω | RES, 1% | 0603 | |
| U1 | 1 | | Allegro MicroSystems A80603 | ES, 24-Pin, 4 mm × 4 mm QFN with Exposed Thermal Pad and Wettable Flank | High Power LED Driver with Pre-Emptive Boost for Ultra-High Dimming Ratio and Low Output Ripple |



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## APPENDIX B: REFERENCE DESIGNS

### SEPIC Configuration

A SEPIC architecture can be employed to allow the converter to regulate with the input voltage below, equal to, or above the output voltage. While a coupled inductor is not necessary for this design to function, a coupled inductor will generally reduce the overall solution size and component count and may reduce the solution cost.

Figure 48 shows the A80603 in a SEPIC configuration driving four strings of four white LEDs. Each string has a forward voltage drop of about 14 V and the current in each string is regulated to 80 mA. The SEPIC converter switching frequency is set to 400 kHz. This design can be employed as-is or can be modified to accommodate different circuit requirements as needed.

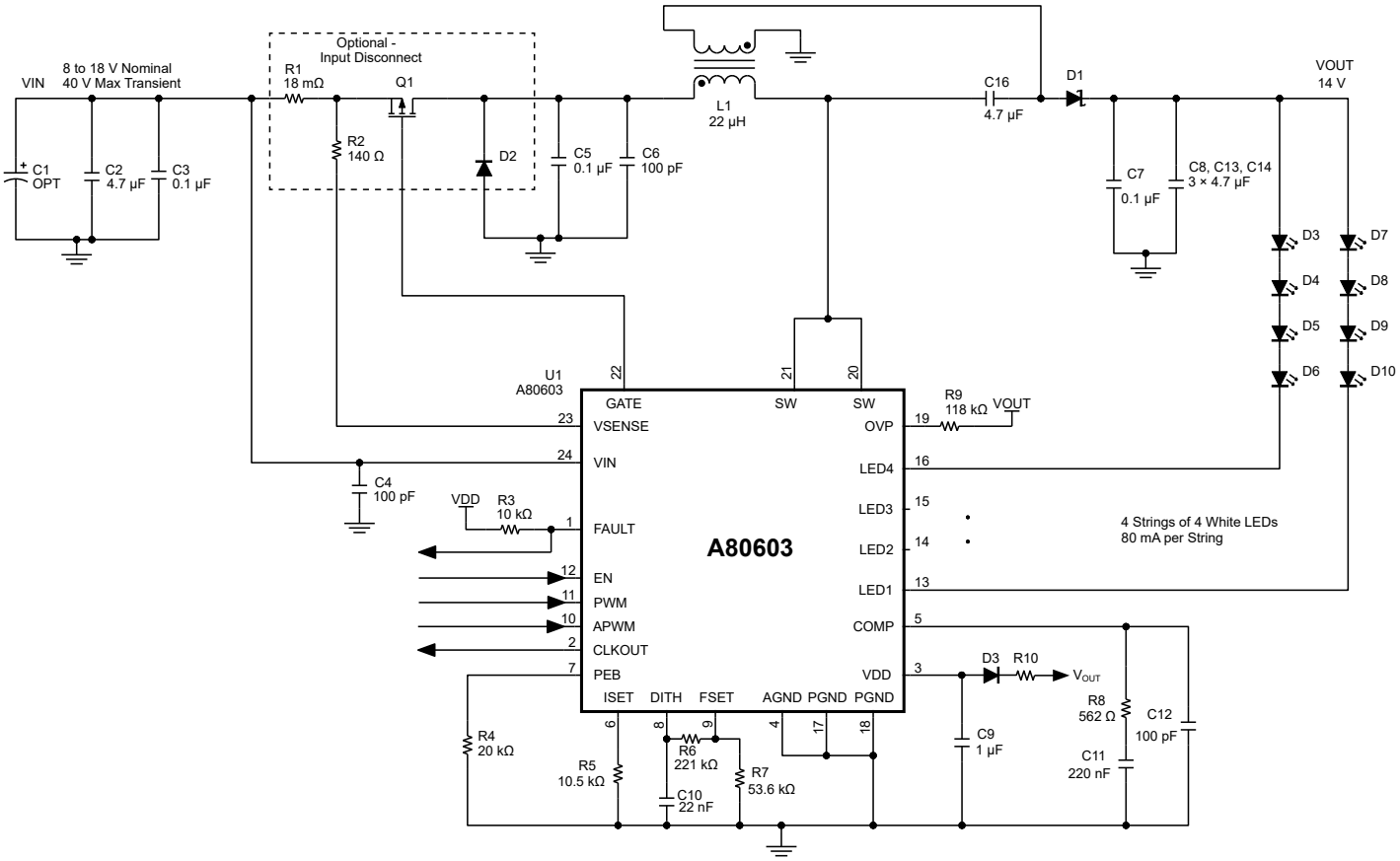



**Figure 48: SEPIC configuration. Allows operation with $V_{IN}$ both above and below $V_{OUT}$.**



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**Table 8: SEPIC Configuration Bill of Materials**

| Designator | Quantity | Value | Description | Footprint | Comment |
|---|---|---|---|---|---|
| C1 | 0 (OPT) | 47 µF | POLARIZED CAP (RADIAL) | Cap Radial 8 mm surface mount | Panasonic EEE-TG1H470UP |
| C2, C8, C13, C14, C16 | 5 | 4.7 µF | CAP CER, 50 V, X7R | 1210 | |
| C3, C5, C7 | 3 | 0.1 µF | CAP CER, 50 V, X7R | 0603 | |
| C4, C6, C12 | 3 | 100 pF | CAP CER, 50 V, COG/NPO | 0603 | |
| C9 | 1 | 1 µF | CAP CER, 16 V, X7R | 0603 | |
| C10 | 1 | 22 nF | CAP CER, 25 V, X7R | 0603 | |
| C11 | 1 | 220 nF | CAP CER, 10 V, X7R | 0603 | |
| D1 | 1 | | DIODE SCHOTTKY, 100 V, 3 A | DO-214AB | Vishay SS3H10-E3/9AT |
| D2. D3 | 2 | | DIODE GENERAL PURPOSE, 100 V, 300 mA | SOD123 | Diodes Incorporated 1N4148W-7 |
| D3, D4, D5, D6, D7, D8, D9, D10... | 16 | | LED, WHITE, 3.5 V FORWARD VOLTAGE DROP | | Total of 16 for 4 strings of 4 LEDs |
| L1 | 1 | 22 µH | COUPLED INDUCTOR FOR SEPIC CONVERTER APPLICATIONS | Coupled-Inductor 2 | Wurth 7448990220 |
| Q1 | 1 | | MOSFET N-CHANNEL, 60 V, 52 A | PowerPAK SO-8L | Vishay Siliconix SQJ459EP-T1_GE3 |
| R1 | 1 | 18 mΩ | RES, 1% | 1206 | |
| R2 | 1 | 140 Ω | RES, 1% | 0603 | |
| R3 | 1 | 10 kΩ | RES, 1% | 0603 | |
| R4 | 1 | 20 kΩ | RES, 1% | 0603 | |
| R5 | 1 | 10.5 kΩ | RES, 1% | 0603 | |
| R6 | 1 | 221 kΩ | RES, 1% | 0603 | |
| R7 | 1 | 53.6 kΩ | RES, 1% | 0603 | |
| R8 | 1 | 562 Ω | RES, 1% | 0603 | |
| R9 | 1 | 118 kΩ | RES, 1% | 0603 | |
| R10 | 1 | 1 kΩ | RES, 1% | 0603 | |
| U1 | 1 | | Allegro MicroSystems A80603 | ES, 24-Pin, 4 mm × 4 mm QFN with Exposed Thermal Pad and Wettable Flank | High Power LED Driver with Pre-Emptive Boost for Ultra-High Dimming Ratio and Low Output Ripple |



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## Cascode-Protected LED Pins Design

The A80603's LEDx pins have an absolute maximum voltage rating of 40 V. For applications where $V_{OUT}$ exceeds 40 V, it is important to protect the LEDx pins if part or all of an LED string is shorted. Figure 49 shows a circuit that protects the LEDx pins by using cascode transistors to disconnect LEDx from $V_{OUT}$ in this event. A voltage rail, $V_{GCAS}$ must be provided externally or generated from an available voltage such as $V_{OUT}$. One simple way to derive $V_{GCAS}$ from $V_{OUT}$ is by using a resistor and Zener diode as shown in Figure 49.

For proper LEDx pin protection, $V_{GCAS}$ must be sufficiently large to ensure that upon an LED short event the corresponding LEDx pin exceeds its LED String Partial-Short Detect Threshold, $V_{LEDSD}$. Also, $V_{GCAS}$ must not exceed the maximum gate-to-source rating of the transistor. Minimum $V_{GCAS}$ can be calculated as follows:

$$V_{GCAS_min} = V_{GP} + V_{LEDSD_max}$$

where $V_{GCAS_min}$ is the minimum suitable gate voltage, $V_{GP}$ is the cascode transistor's plateau voltage (see gate threshold voltage versus total gate charge curve in the transistor's datasheet), and $V_{LEDSD_max}$ is the maximum LED String Partial-Short Detect threshold ($V_{LEDSD_max}$ = 6.1 V).

Figure 49 shows the A80603 driving 4 strings of 12 white LEDs. Each string has a forward voltage drop of about 42 V and the current in each string is regulated to 120 mA. Each LED string has a cascode transistor that will protect the respective LEDx pin from overvoltage in the event of an LED string short.

Output overvoltage protection of the boost converter is set to 45.5 V. Note that the absolute maximum continuous voltage rating of the boost converter's power MOSFET is 50 V, so the output overvoltage protection level must be set below 50 V to protect this MOSFET.

The cascode transistors can be any small-signal N-channel MOSFETs rated for the maximum output voltage and LED current per channel. As an example, consider T2N7002BK in SOT23 package. This device has a 60 V breakdown rating and 400 mA continuous current rating.

This design can be employed as-is or can be modified to accommodate different circuit requirements as needed. Note that the maximum number of LEDs is limited by the minimum input voltage and the minimum boost power switch gate driver off-time ($t_{SW(OFF)}$). This design has a switching frequency of 2 MHz. Reducing the switching frequency of the converter will allow operation with a lower input voltage for a given number of LEDs.

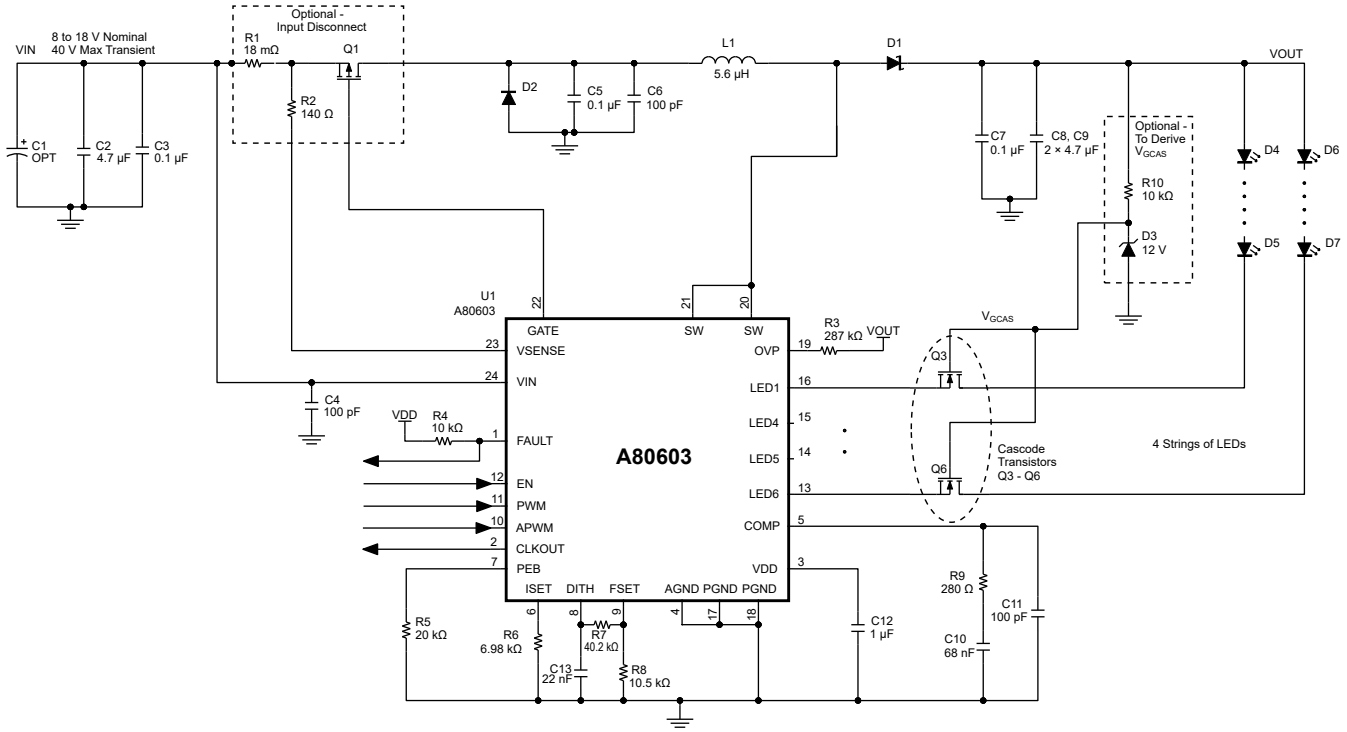



**Figure 49: Cascode-Protected LED Pins Design**



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**Table 9: Cascode-Protected LED Pins Design Bill of Materials**

| Designator | Quantity | Value | Description | Footprint | Comment |
|---|---|---|---|---|---|
| C1 | 0 (OPT) | 47 µF | POLARIZED CAP (RADIAL) | Cap Radial 8 mm surface mount | Panasonic EEE-TG1H470UP |
| C2, C8, C9 | 3 | 4.7 µF | CAP CER, 50 V, X7R | 1210 | |
| C3, C5, C7 | 3 | 0.1 µF | CAP CER, 50 V, X7R | 0603 | |
| C4, C6, C11 | 3 | 100 pF | CAP CER, 50 V, COG/NPO | 0603 | |
| C10 | 1 | 68 nF | CAP CER, 10 V, X7R | 0603 | |
| C12 | 1 | 1 µF | CAP CER, 16 V, X7R | 0603 | |
| C13 | 1 | 22 nF | CAP CER, 25 V, X7R | 0603 | |
| D1 | 1 | | DIODE SCHOTTKY, 100 V, 3 A | DO-214AB | Vishay SS3H10-E3/9AT |
| D2 | 1 | | DIODE GENERAL PURPOSE, 100 V, 300 mA | SOD123 | Diodes Incorporated 1N4148W-7 |
| D3 | 1 | | DIODE ZENER, 12 V, 300 MW | SOD323 | ON Semiconductor SZMM3Z12VT1G |
| D4, D5, D6, D7 ... | 48 | | LED, WHITE, 3.5 V FORWARD VOLTAGE DROP | | Total of 48 for 4 strings of 12 LEDs |
| L1 | 1 | 5.6 µH | INDUCTOR, 5.5 A, 23 mΩ | | Coilcraft XEL5050-562ME |
| Q1 | 1 | | MOSFET N-CHANNEL, 60 V, 52 A | PowerPAK SO-8L | Vishay Siliconix SQJ459EP-T1_GE3 |
| Q3 - Q6 | 4 | | MOSFET N-CHANNEL, 60 V, 400 mA | SOT23 | Toshiba T2N7002BK. LM |
| R1 | 1 | 18 mΩ | RES, 1% | 1206 | |
| R2 | 1 | 140 Ω | RES, 1% | 0603 | |
| R3 | 1 | 287 kΩ | RES, 1% | 0603 | |
| R4 | 1 | 10 kΩ | RES, 1% | 0603 | |
| R5 | 1 | 20 kΩ | RES, 1% | 0603 | |
| R6 | 1 | 6.98 kΩ | RES, 1% | 0603 | |
| R7 | 1 | 40.2 kΩ | RES, 1% | 0603 | |
| R8 | 1 | 10.5 kΩ | RES, 1% | 0603 | |
| R9 | 1 | 280 Ω | RES, 1% | 0603 | |
| R10 | 1 | 10 kΩ | RES, 1% | 0603 | |
| U1 | 1 | | Allegro MicroSystems A80603 | ES, 24-Pin, 4 mm × 4 mm QFN with Exposed Thermal Pad and Wettable Flank | High Power LED Driver with Pre-Emptive Boost for Ultra-High Dimming Ratio and Low Output Ripple |



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## Revision History

| Number | Date | Description |
|---|---|---|
| – | March 4, 2019 | Initial release |
| 1 | March 6, 2020 | Minor editorial updates |
| 2 | September 29, 2020 | Updated Features and Benefits, Description, and Simplified Circuit figure (pages 1-2);<br>Updated Table of Contents and removed SEPIC Configuration figure (page 3);<br>Updated Functional Block Diagram (page 4);<br>Updated Oscillator Frequency value (page 7);<br>Removed Minimum PWM On-Time (page 8);<br>Added Minimum PWM Off-Time (page 8);<br>Updated Functional Description (pages 9, 13, 15-17);<br>Added Appendix A (pages 30-34);<br>Added Appendix B (pages 35-38) |
| 3 | December 1, 2020 | Corrected diode D2 direction in Figure 1 (page 1); updated drawing number in Figure 45 (page 29). |
| 4 | September 30, 2021 | Updated Features and Benefits, Description, and Simplified Circuit figure (page 1);<br>Added Minimum PWM Dimming On-Time characteristic (page 8);<br>Updated Minimum PWM Off-Time characteristic (page 8);<br>Updated Functional Description (page 10, 16-18);<br>Updated SEPIC Configuration Block Diagram (page 36). |
| 5 | April 28, 2022 | Corrected SEPIC circuit, adding D3 and R10 from VDD to VOUT (pages 36-37) |
| 6 | April 28, 2023 | Updated package drawing (page 30) |

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