GS6042

6G UHD-SDI/3G/HD/SD Adaptive Cable Equalizer

Gennum Products

Key Features

- Supports data rates from 125Mb/s to 6.25Gb/s
- SMPTE ST 2081 (proposed), SMPTE ST 424, SMPTE ST 292, and SMPTE ST 259 compliant
- Automatic cable equalization
- Typical equalized length of Belden 1694A cable:
  - 80m at 5.94Gb/s
  - 210m at 2.97Gb/s
  - 300m at 1.485Gb/s
  - 500m at 270Mb/s
- Supports DVB-ASI at 270Mb/s
- Supports MADI at 125Mb/s
- Manual bypass control
- Programmable carrier detect with squelch threshold adjustment
- Automatic power-down on loss of signal
- Differential output supports DC-coupling from +1.2V to +3.3V CML logic
- Optional 6dB flat band gain on input
- Selectable output de-emphasis: 2dB, 6dB, and 8dB
- Standard EIA/JEDEC logic for control/status signals
- Single +3.3V power supply operation
- 180mW power consumption (35mW in sleep)
- Operating temperature range: -40°C to +85°C
- Small footprint QFN package (4mm x 4mm)
  - Footprint compatible with the GS2974A, GS2974B, GS2984, GS2994, and GS3440
- Pb-free and RoHS compliant

Applications

- SMPTE ST 2081 (proposed), SMPTE ST 424, SMPTE ST 292, and SMPTE ST 259 coaxial cable serial digital interfaces
- Serialized 8b/10b encoded video streams up to 6.25Gb/s

Description

The GS6042 is a high-speed BiCMOS device designed to optimally equalize and restore signals received over 75Ω coaxial cable.

The device supports data rates up to 6.25Gb/s while being optimized for the proposed SMPTE ST 2081, as well as SMPTE ST 424, SMPTE ST 292, and SMPTE ST 259.

The GS6042 features DC restoration to compensate for the DC content of SMPTE pathological signals.

The Carrier Detect output pin ($\overline{CD}$) indicates whether an input signal has been detected. It can be connected directly to the SLEEP pin to enable automatic sleep on loss of input.

A $\overline{CD}$ threshold is set via the SQ_ADJ pin, allowing the GS6042 to distinguish between small amplitude SDI signals and noise at the input of the device.

The equalizing and DC restore stages are disengaged and no equalization occurs when the BYPASS pin is HIGH. This is useful for signals launched at the signal source with low data rates and/or slow rise/fall times.

The GS6042 features a gain selection pin (GAIN_SEL) which can be used to compensate for 6dB flat attenuation prior to the input of the device.

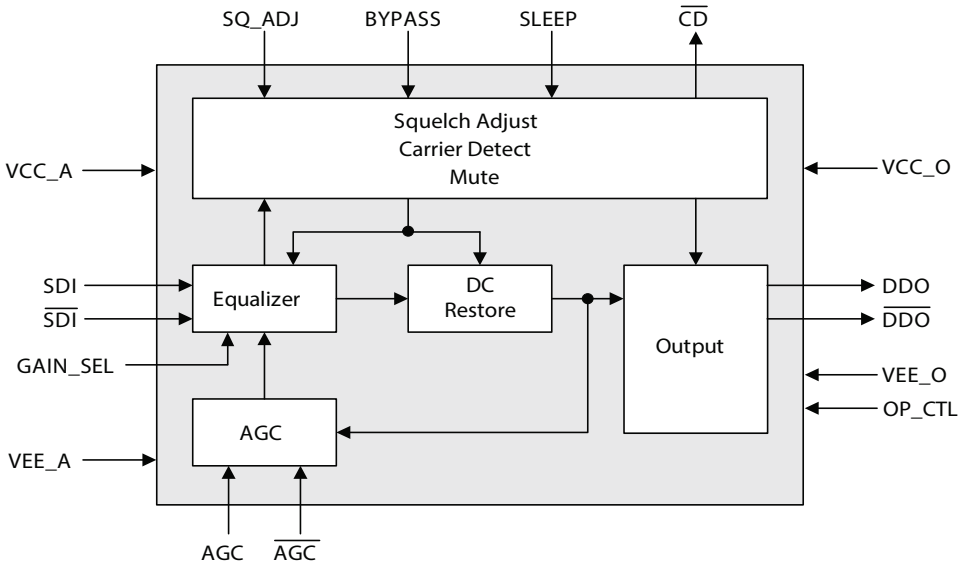
The differential output can be DC-coupled to Semtech's reclockers and cable drivers, as well as industry-standard CML logic by changing the voltage applied to the VCC_O pin. In general, DC-coupling to any termination voltage between +1.2V and +3.3V is supported.

The GS6042 also features programmable output de-emphasis with three user-selectable operating levels to support long PCB traces at the output of the device.

Power consumption of the GS6042 is typically 180mW when its output is DC-coupled at +1.2V.

The GS6042 is Pb-free, and the encapsulation compound does not contain halogenated flame retardant. This component and all homogeneous subcomponents are RoHS compliant.

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GS6042 Functional Block Diagram

Revision History

Version	ECO	PCN	Date	Changes and/or Modifications
3	019547	—	May 2014	Corrected the values for the de-emphasis levels
2	017789	—	February 2014	Converted to Final Data Sheet. Modified Section 4.3. Included reference to 6G SMPTE standard.
1	016407	—	November 2013	Converted to Final Data Sheet. Included information on 6.25G support. Updated Jitter characteristics. Updates throughout.
0	012658	—	June 2013	New document

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Contents

Key Features 1
Applications 1
Description 1
Revision History 2
1. Pin Out 4
    1.1 GS6042 Pin Assignment 4
    1.2 GS6042 Pin Descriptions 4
2. Electrical Characteristics 6
    2.1 Absolute Maximum Ratings 6
    2.2 DC Electrical Characteristics 6
    2.3 AC Electrical Characteristics 8
3. Input/Output Circuits 10
4. Detailed Description 11
    4.1 Serial Digital Inputs 11
    4.2 Automatic (Adaptive) Cable Equalization 11
    4.3 Differential Digital Data Output 11
    4.4 Programmable Squelch Adjust (SQ_ADJ) 12
    4.5 Carrier Detect, Sleep, and Auto-Sleep 13
    4.6 GAIN_SEL 13
    4.7 Adjustable Output Swing, De-emphasis, and Mute 14
5. Application Information 16
    5.1 High-Gain Adaptive Cable Equalizers 16
    5.2 PCB Layout 16
    5.3 Typical Application Circuit 17
6. Package & Ordering Information 18
    6.1 Package Dimensions 18
    6.2 Packaging Data 18
    6.3 Recommended PCB Footprint 19
    6.4 Marking Diagram 19
    6.5 Solder Reflow Profiles 20
    6.6 Ordering Information 20

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1. Pin Out

1.1 GS6042 Pin Assignment

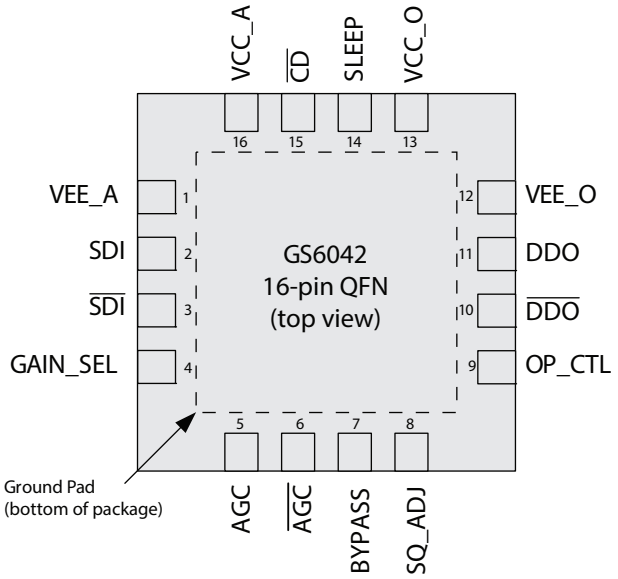


Figure 1-1: GS6042 Pin Out

1.2 GS6042 Pin Descriptions

Table 1-1: GS6042 Pin Descriptions

Pin Number	Name	Type	Description
1	VEE_A	Power	Most negative power supply connection for the input buffer, core, and control circuits. Connect to ground.
2, 3	SDI, $\overline{SDI}$	Input	Serial digital differential input.
4	GAIN_SEL	Input	Flat Band Gain Control. Please refer to the DC Electrical Characteristics table for logic level threshold and compatibility. This pin is a +2.5V input that is tolerant to +3.3V levels. When HIGH, the device compensates for an additional 6dB of loss across the entire operating band. This pin has an internal pull-down resistor.
5, 6	AGC, $\overline{AGC}$	—	External AGC capacitor connection.
7	BYPASS	Input	EQ Bypass Control. Please refer to the DC Electrical Characteristics table for logic level threshold and compatibility. This pin is a +2.5V input that is tolerant to +3.3V levels. Forces the equalizer and DC-restore stages into Bypass mode when HIGH. No equalization occurs in this mode. This pin has an internal pull-down resistor.

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Table 1-1: GS6042 Pin Descriptions (Continued)

Pin Number	Name	Type	Description
8	SQ_ADJ	Input	Squelch Threshold Adjust. Adjusts the input signal amplitude threshold of the carrier detect function. The serial data output of the device can be muted when the serial data input signal amplitude is too low by connecting the $\overline{CD}$ and OP_CTL pins using a suitable resistor network (see Figure 4-4 and Figure 4-5). This pin has an internal pull-down resistor. **Note:** The SQ_ADJ function is only available when the device is not configured for auto-sleep mode. Reference Section 4.5 for more detail.
9	OP_CTL	Input	Output Swing, De-emphasis and Mute Control. When this pin is connected to GND, the output swing is 850mV$_{ppd}$ with no de-emphasis applied to the output signal. With this pin connected to +2.5V, the output is muted. Intermediate voltages and functions are shown in Table 4-5. These voltages can be achieved as shown in Figure 4-4 and Figure 4-5. This pin has an internal pull-down resistor.
10, 11	$\overline{DDO}$, DDO	Output	Serial digital differential output.
12	VEE_O	Power	Most negative power supply connection for the output buffer. Connect to ground.
13	VCC_O	Power	Most positive power supply connection for the output buffer. Connect to 1.2V - 3.3V DC.
14	SLEEP	Input	SLEEP Control. Please refer to the DC Electrical Characteristics table for logic level threshold and compatibility. This pin is a +2.5V input that is tolerant to +3.3V levels. When HIGH the part is powered-down except for the Carrier Detect function. This pin can be connected directly to the $\overline{CD}$ pin to automatically put the device to sleep (low-power operation) on loss of carrier. This pin has an internal pull-down resistor. **Note**: When SLEEP is connected to $\overline{CD}$ for automatic power reduction on loss of carrier, the SQ_ADJ pin will not modify the $\overline{CD}$ threshold. The $\overline{CD}$ threshold will revert to the default value used when SQ_ADJ is pulled LOW.
15	$\overline{CD}$	Output	Carrier Detect Status Output. Please refer to the DC Electrical Characteristics table for logic level threshold and compatibility. This pin is a +2.5V output. Indicates presence of an input signal. When the $\overline{CD}$ pin is LOW, a signal has been detected at the input. When this pin is HIGH, this indicates loss of input signal.
16	VCC_A	Power	Most positive power supply connection for the input buffer, core and control circuits. Connect to +3.3V DC.
—	Center Pad	Power	Internally bonded to VEE_A. Connect to GND with at least 5 vias.

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2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2-1: Absolute Maximum Ratings

Parameter	Value
Supply Voltage - Core/Output Driver	-0.5V to +3.6V DC
Input ESD Voltage (HBM)	5kV
Storage Temperature Range (T_s)	-50°C to +125°C
Input Voltage Range (any input)	-0.3 to (V_{CC_A} +0.3)V
Operating Temperature Range	-40°C to +85°C
Solder Reflow Temperature	260°C

Note: Absolute Maximum Ratings are those values beyond which damage may occur. Functional operation outside of the ranges shown in the AC and DC Electrical Characteristics is not guaranteed.

2.2 DC Electrical Characteristics

Table 2-2: DC Electrical Characteristics

V_{CC_A} = +3.3V ±5%, T_A = -40°C to +85°C, unless otherwise shown.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Supply Voltage - Core	V_{CC_A}	—	3.135	3.3	3.465	V	—
Supply Voltage - Output Driver	V_{CC_O}	—	1.14	1.2	1.26	V	1
		—	2.375	2.5	2.625	V	1
		—	3.135	3.3	3.465	V	1

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Table 2-2: DC Electrical Characteristics (Continued)

V_{CC_A} = +3.3V ±5%, T_A = -40°C to +85°C, unless otherwise shown.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Power Consumption	P_D	V_{CC_O} = 1.2V ΔV_{DDO} = 425mV$_{ppd}$	—	180	—	mW	2
		V_{CC_O} = 1.2V ΔV_{DDO} = 850mV$_{ppd}$	—	195	—	mW	2
		V_{CC_O} = 2.5V ΔV_{DDO} = 425mV$_{ppd}$	—	196	—	mW	2
		V_{CC_O} = 2.5V ΔV_{DDO} = 850mV$_{ppd}$	—	221	—	mW	2
		V_{CC_O} = 3.3V ΔV_{DDO} = 425mV$_{ppd}$	—	202	—	mW	2
		V_{CC_O} = 3.3V ΔV_{DDO} = 850mV$_{ppd}$	—	240	—	mW	2
		Sleep Mode SLEEP = HIGH	—	35	—	mW	—
Supply Current - Core	I_s	—	—	55	—	mA	2, 3
Supply Current - Output Driver	I_{Out}	ΔV_{DDO} = 850mV$_{ppd}$	—	20	—	mA	2
		ΔV_{DDO} = 425mV$_{ppd}$	—	10	—	mA	2
Input Common Mode Voltage	V_{CMIN}	—	—	1.7	—	V	—
Output Common Mode Voltage	V_{CMOUT}	Refer to Section 4.3					
$\overline{CD}$ Output Voltage Logic Levels	$V_{\overline{CD}(OH)}$	Signal not present	2.0	—	—	V	—
	$V_{\overline{CD}(OL)}$	Signal present	—	—	0.4	V	—
Input Voltage Logic Levels: GAIN_SEL, BYPASS, SLEEP	V_{IH}	Minimum to assert	1.7	—	—	V	4
	V_{IL}	Maximum to de-assert	—	—	0.7	V	4

Notes:

1. V_{CC_O} operates from +1.2V through +3.3V (+/-5%).
2. De-emphasis off.
3. An additional 3mA when de-emphasis is enabled.
4. GAIN_SEL, BYPASS, SLEEP pins are +2.5V, but +3.3V tolerant.

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2.3 AC Electrical Characteristics

Table 2-3: AC Electrical Characteristics

V_{CC_A} = +3.3V ±5%, T_A = -40°C to +85°C, unless otherwise shown

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Serial input Data Rate	DR_{DDO}	—	125	—	6250	Mb/s	1
Input Voltage Swing	ΔV_{SDI}	Differential, 270Mb/s and 1.485Gb/s	720	800	950	mV_{ppd}	2
		Differential, 2.97Gb/s and 5.94Gb/s	720	800	880	mV_{ppd}	2
Output Voltage Swing	ΔV_{DDO}	100Ω differential load, OP_CTL set for high swing	700	850	1000	mV_{ppd}	—
		100Ω differential load, OP_CTL set for low swing	350	425	500	mV_{ppd}	—
Output Jitter at Various Cable Lengths and Data Rates		6.25Gb/s Belden 1694A: 0-50m	—	0.35	—	UI	4, 5
		5.94Gb/s Belden 1694A: 0-80m	—	0.35	0.5	UI	4, 5
		2.97Gb/s Belden 1694A: 0-100m	—	—	0.2	UI	3, 4, 5
		2.97Gb/s Belden 1694A: 100-150m	—	—	0.3	UI	3, 4, 5
		2.97Gb/s Belden 1694A: 150-170m	—	—	0.4	UI	3, 4, 5
		2.97Gb/s Belden 1694A: 170-200m	—	—	0.5	UI	3, 4, 5
		2.97Gb/s Belden 1694A: 210m	—	0.5	—	UI	4, 5
		1.485Gb/s Belden 1694A: 0-200m	—	—	0.2	UI	3, 4, 5
		1.485Gb/s Belden 1694A: 200-260m	—	—	0.3	UI	3, 4, 5
		1.485Gb/s Belden 1694A: 260-300m	—	0.3	—	UI	4, 5
		270Mb/s Belden 1694A: 0-300m	—	0.1	0.15	UI	3, 4, 5
		270Mb/s Belden 1694A: 300-500m	—	—	0.25	UI	3, 4, 5

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Table 2-3: AC Electrical Characteristics (Continued)

V_{CC_A} = +3.3V ±5%, T_A = -40°C to +85°C, unless otherwise shown

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Output Rise/Fall time	t_r, t_f	5.94Gb/s, 2.97Gb/s, and 1.485Gb/s 20% - 80%	—	75	—	ps	—
		270Mb/s 20% - 80%	—	150	—	ps	—
Mismatch in Rise/Fall time	Δt_r, Δt_f	—	—	—	30	ps	—
Duty Cycle Distortion		—	—	—	30	ps	—
Overshoot		—	—	—	10	%	—
Input Return Loss		5MHz - 1.485GHz	15	—	—	dB	—
		1.485GHz - 2.97GHz	10	—	—	dB	—
Input Resistance		single-ended	—	1.9	—	kΩ	—
Input Capacitance		single-ended	—	1.3	—	pF	—
Output Resistance		single-ended	—	50	—	Ω	—

Notes:

1. Device performance is optimized for standard data rates (SD = 270Mb/s, HD = 1.485Gb/s, 3G = 2.970Gb/s, 6G = 5.94Gb/s).
2. 0m cable length.
3. All parts are production tested. In order to guarantee maximum jitter over the full range of specification (V_{CC_A} = +3.3V ±5%, T_A = -40°C to +85°C, and 720-880mV_{pp} launch swing from the SDI cable driver), the recommended applications circuit must be used.
4. Based on validation data using the recommended applications circuit, with V_{CC_A} = +3.3V, T_A = -40°C to +85°C and 800mV_{pp} launch swing from the SDI cable driver.
5. GAIN_SEL = 0.

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3. Input/Output Circuits

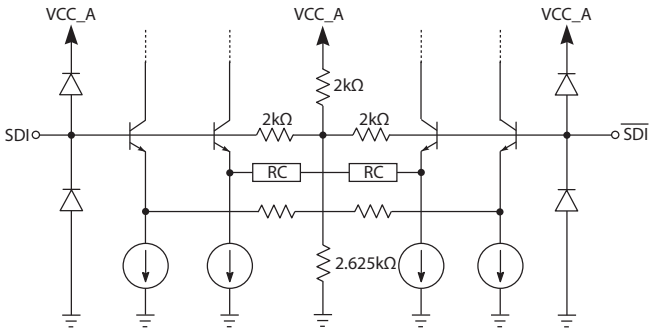


Figure 3-1: Input Circuit

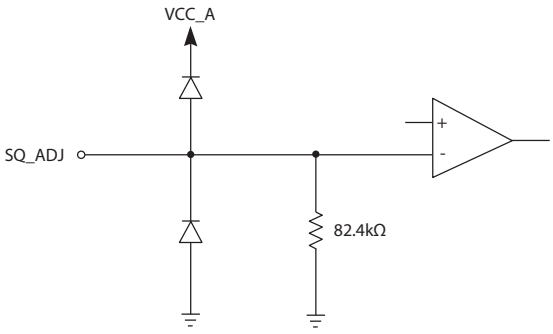


Figure 3-2: SQ_ADJ Circuit

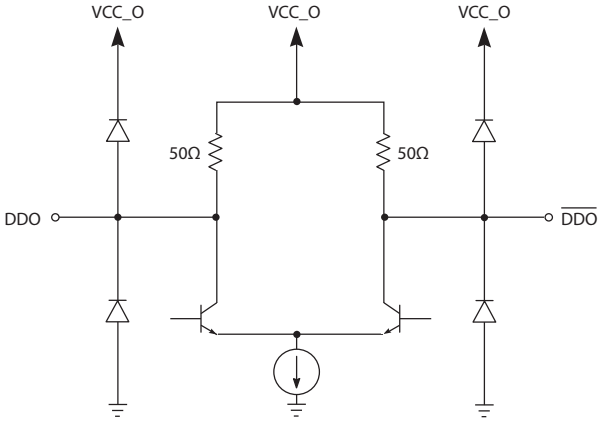


Figure 3-3: Output Circuit

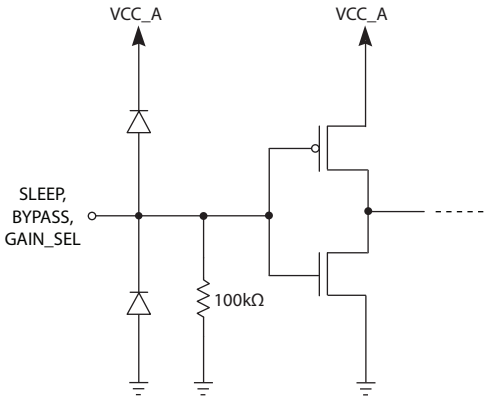


Figure 3-4: SLEEP, BYPASS, and GAIN_SEL Circuits

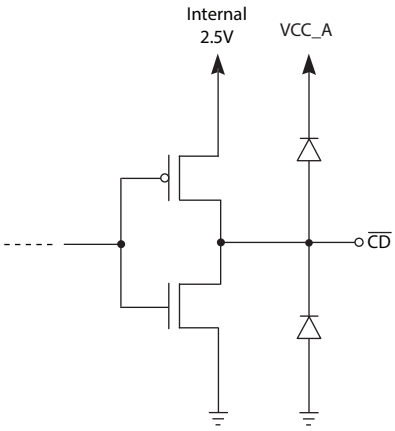


Figure 3-5: $\overline{CD}$ Circuit

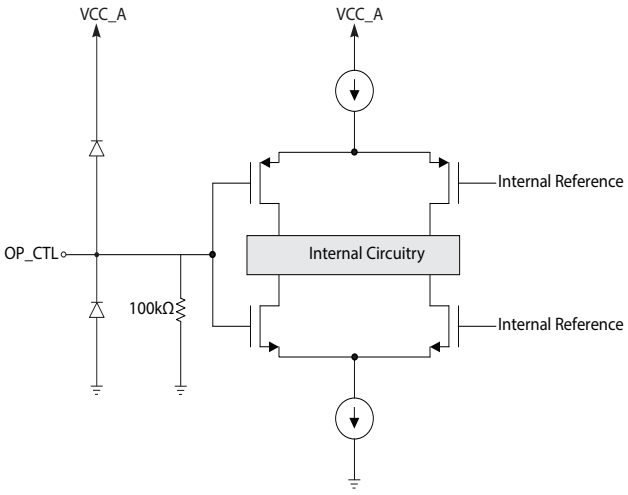


Figure 3-6: OP_CTL

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4. Detailed Description

The GS6042 is a high-speed BiCMOS IC designed to automatically equalize high-bandwidth serial digital video signals.

The GS6042 can equalize data rates up to 6.25Gb/s including 6G UHD-SDI, 3G SDI, HD SDI, and SD SDI serial digital signals. The GS6042 is optimized to equalize up to 80m of Belden 1694A cable at 5.94Gb/s (UHD-SDI), 210m at 2.97Gb/s (3G-SDI), 300m at 1.485Gb/s (HD-SDI), and 500m at 270Mb/s (SD-SDI).

The GS6042 can be powered from a single +3.3V DC power supply, and is footprint-compatible with Semtech's GS2974A, GS2974B, GS2984, GS2994, and GS3440 equalizers.

4.1 Serial Digital Inputs

The received serial data signal is connected to the input pins (SDI/$\overline{\text{SDI}}$) in either a differential or single-ended configuration. AC-coupling of the inputs is recommended because the SDI and $\overline{\text{SDI}}$ inputs are internally biased to approximately 1.71V.

See Figure 5-1 for the recommended input applications circuit when using a single-ended 75Ω coax cable.

4.2 Automatic (Adaptive) Cable Equalization

The input signal passes through a variable gain equalizing stage, whose frequency response closely matches the inverse of the Belden 1694A cable loss characteristic for any given attached cable length within the supported ranges.

The equalized signal is DC-restored, effectively restoring the logic threshold of the equalized signal to its correct level independent of shifts due to AC-coupling.

4.3 Differential Digital Data Output

The digital data output signals (DDO/$\overline{\text{DDO}}$) have a nominal output voltage swing of either 850mV$_{ppd}$ or 425mV$_{ppd}$ (ΔV_{DDO}), as set by the OP_CTL pin. Table 4-1 shows the typical output common mode voltage levels (V_{CMOUT}) related to the two output swing options and the type of output transmission termination as shown in Figure 4-1 and Figure 4-2.

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Table 4-1: Typical Common Mode Output Voltage Levels (V_{CMOUT})

Supply Voltage (VCC_O)	Termination Type 1 (See Figure 4-1) (See 1)		Termination Type 2 (See Figure 4-2)	
	$425mV_{ppd}$ Swing	$850mV_{ppd}$ Swing	$425mV_{ppd}$ Swing	$850mV_{ppd}$ Swing
3.3V	3.19V	3.09V	3.09V	2.88V
2.5V	2.39V	2.29V	2.29V	2.08V
1.8V	1.69V	1.59V	1.59V	1.38V
1.2V	1.09V	0.99V	0.99V	0.78V

Note:

1. The values shown for termination type 1 only apply when V_{TERM} = VCC_O

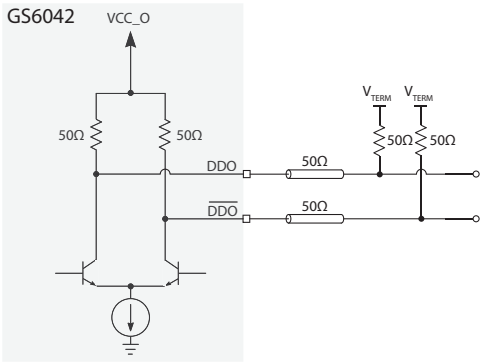


Figure 4-1: 50Ω Termination to V_{TERM}

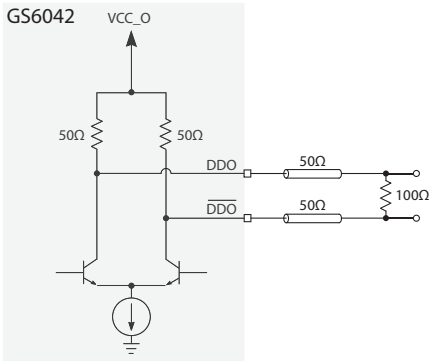


Figure 4-2: 100Ω Parallel Output Termination

4.4 Programmable Squelch Adjust (SQ_ADJ)

The GS6042 features a programmable Squelch Adjust (SQ_ADJ) threshold.

This feature can be useful in applications where there are multiple input channels using the GS6042 and the maximum gain of each device must be limited to avoid crosstalk.

The SQ_ADJ pin acts to change the threshold of the Carrier Detect ($\overline{CD}$) pin. When the input signal level drops below the threshold set by SQ_ADJ, the $\overline{CD}$ pin will be driven HIGH, indicating that there is not a valid input signal.

This feature has been designed for use in applications such as routers, where signal crosstalk and circuit noise cause the equalizer to output erroneous data when no input signal is present. The use of a Carrier Detect function with a fixed internal reference does not solve this problem since the signal-to-noise ratio on the circuit board could be significantly less than the default signal detection level set by the on-chip reference.

In applications where programmable squelch adjust is not required, the SQ_ADJ pin can be left unconnected.

Note: When using SQ_ADJ to limit the maximum gain of the GS6042, $\overline{CD}$ should not be connected to SLEEP.

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4.5 Carrier Detect, Sleep, and Auto-Sleep

The Carrier Detect output pin ($\overline{CD}$) indicates the presence of a valid signal at the input of the GS6042. When $\overline{CD}$ is LOW, the device has detected a valid input on SDI/$\overline{SDI}$. When $\overline{CD}$ is HIGH, the device considers the input invalid.

Note 1: $\overline{CD}$ will only detect loss of signal for data rates greater than 19Mb/s.

Note 2: If SQ_ADJ is being used to limit the maximum gain of the device, and the maximum cable length is exceeded, the $\overline{CD}$ pin will be set to HIGH even if an input is present.

Table 4-2: $\overline{CD}$ Output

$\overline{CD}$	Input Status
0	Valid input on SDI/$\overline{SDI}$ pins
1	Input is not valid

The GS6042 also includes a SLEEP input pin, which can be used to put the device into a low-power sleep mode. In this mode, the outputs are high impedance and will be pulled high by the on-chip termination. Set the SLEEP pin HIGH to place the chip in this low-power state. In this mode, the Carrier Detect output will still function to facilitate the detection of a valid serial input data signal.

Auto-Sleep is enabled by connecting $\overline{CD}$ to SLEEP. When connected, the GS6042 will automatically go into low-power sleep mode when there is a loss of input signal.

Note 3: If the $\overline{CD}$ pin is connected to the SLEEP pin, SQ_ADJ must be either left open, or connected to ground.

Table 4-3: SLEEP Input

SLEEP	Function
0	Normal operation
1	Low-power sleep mode; $\overline{CD}$ output remains valid

4.6 GAIN_SEL

The GS6042 provides the option of compensating for 6dB of flat attenuation prior to the equalizer.

Table 4-4: GAIN_SEL Input Table

GAIN_SEL	Function
0	No flat band gain is applied
1	6dB of flat band gain applied to input signal

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4.7 Adjustable Output Swing, De-emphasis, and Mute

The OP_CTL input pin determines the output swing and de-emphasis settings for DDO and $\overline{DDO}$.

The OP_CTL pin is an analog input, allowing different combinations of output swing, de-emphasis, and mute. The possible values are listed in Table 4-5.

Table 4-5: OP_CTL Functions and Levels

Level	Swing	De-emphasis	Mute	Voltage (V)
0	$850mV_{ppd}$	Off	N	0.000 - 0.083
1	$850mV_{ppd}$	2dB	N	0.234 - 0.394
2	$850mV_{ppd}$	6dB	N	0.545 - 0.704
3	$850mV_{ppd}$	8dB	N	0.856 - 1.015
4	$425mV_{ppd}$	Off	N	1.166 - 1.333
5	$425mV_{ppd}$	2dB	N	1.484 - 1.644
6	$425mV_{ppd}$	6dB	N	1.795 - 1.954
7	$425mV_{ppd}$	8dB	N	2.106 - 2.265
8	$425mV_{ppd}$	N/A	Y	2.416 - 2.500

When muted, the output swing is set to $425mV_{ppd}$ and the outputs are latched.

Automatic muting of the output can be enabled by connecting the $\overline{CD}$ pin to the OP_CTL pin.

If the connection is made directly, as shown in Figure 4-3, the output would be in its default mode ($850mV_{ppd}$ swing with no de-emphasis) when there is signal present.

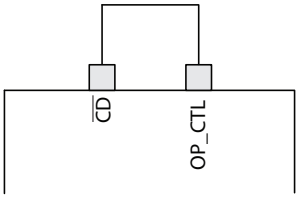


Figure 4-3: Direct Loopback

To enable automatic muting while the output is configured for other settings, a resistor network can be used between $\overline{CD}$ and VCC_A. The intermediate voltages of this resistor ladder can set the output to any one of the nine different settings as shown in the examples given in Figure 4-4 and Figure 4-5.

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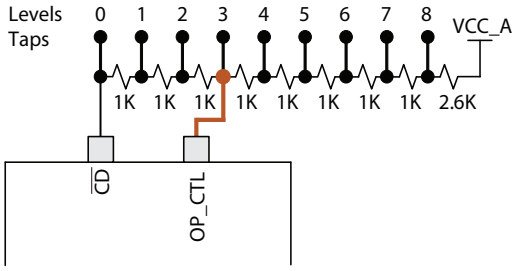


Figure 4-4: Resistor Divider Loopback Example #1 (Function Level 3 from Table 4-5)

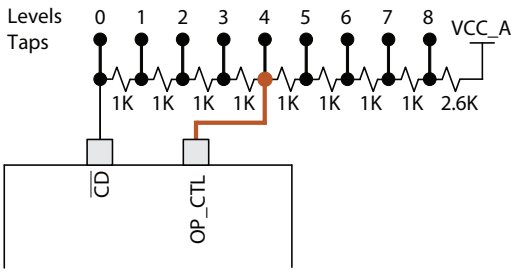


Figure 4-5: Resistor Divider Loopback Example #2 (Function Level 4 from Table 4-5)

In Figure 4-4, the automatic muting of the output is established by connecting node 3 to the OP_CTL pin. In this scenario, the output would be 850mV$_{ppd}$ with 8dB of de-emphasis when there is a signal present.

In Figure 4-5, the OP_CTL pin is connected to node 4. In this scenario, the output would be 425mV$_{ppd}$ with no de-emphasis when there is a signal present.

In both cases, the output would be muted when no carrier is detected.

Note: When the device is in SLEEP mode, automatic muting and SQ_ADJ do not function. Asserting the SLEEP pin manually overrides all other functionality.

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5. Application Information

5.1 High-Gain Adaptive Cable Equalizers

The GS6042 is a multi-rate Adaptive Cable Equalizer. In order to extend the cable lengths that the device can support, it is necessary to have high-gain in the equalizer.

In particular, an SDI video cable equalizer must provide wide band gain over a range of frequencies in order to accommodate the range of data rates and signal patterns that are present in a SMPTE-compliant serial video stream.

Small levels of signal or noise present at the input pins of the equalizer may cause chatter at the output. In order to prevent this from happening, particular attention must be paid to board layout.

5.2 PCB Layout

Special attention must be paid to component layout when designing serial digital interfaces for HDTV and other high-speed video applications.

An FR-4 dielectric can be used, however, controlled impedance transmission lines are required for PCB traces longer than approximately 1cm. Note the following PCB artwork features used to optimize performance:

- PCB trace width for high data rate signals should be closely matched to SMT component width to minimize reflections due to changes in trace impedance
- High-speed traces should be curved to minimize impedance changes
- Cutouts in the inner layers should be used under the GS6042 input and output components to minimize parasitic capacitance

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5.3 Typical Application Circuit

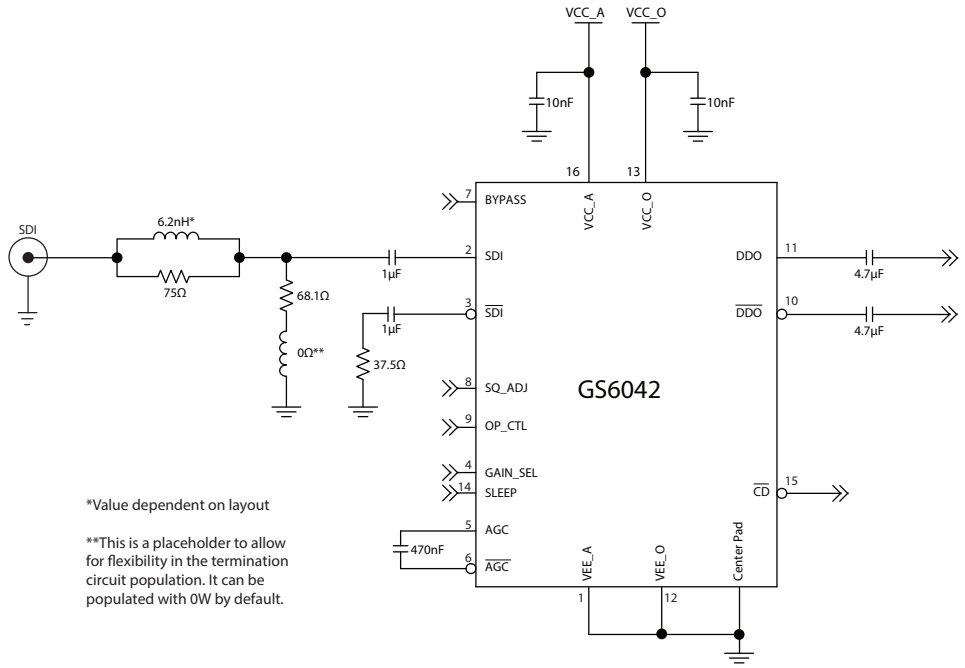


Figure 5-1: GS6042 Typical Application Circuit Recommended for Extended Cable Reach Applications

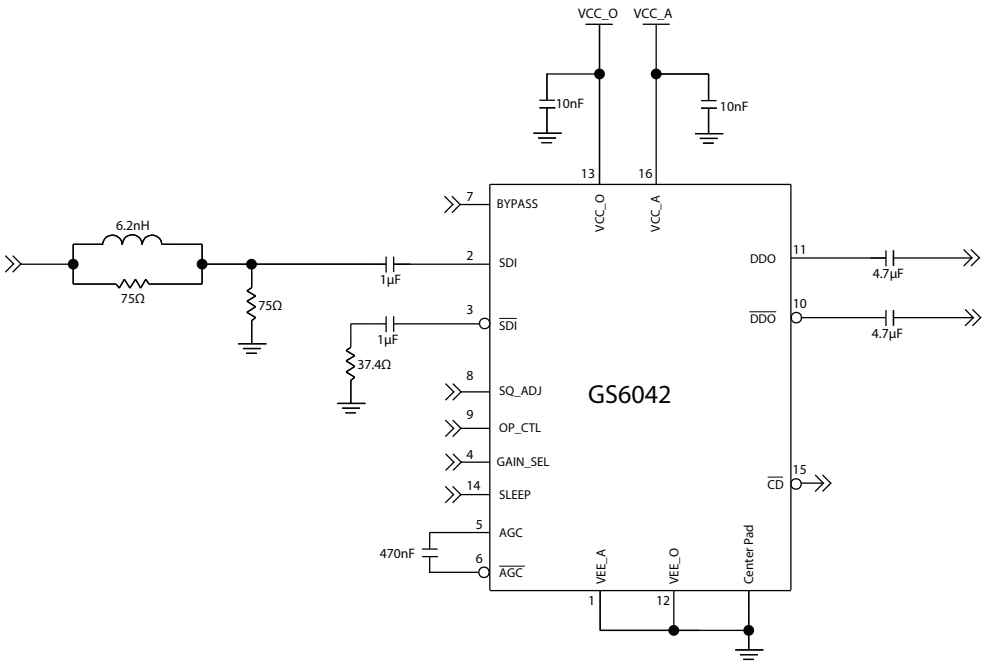
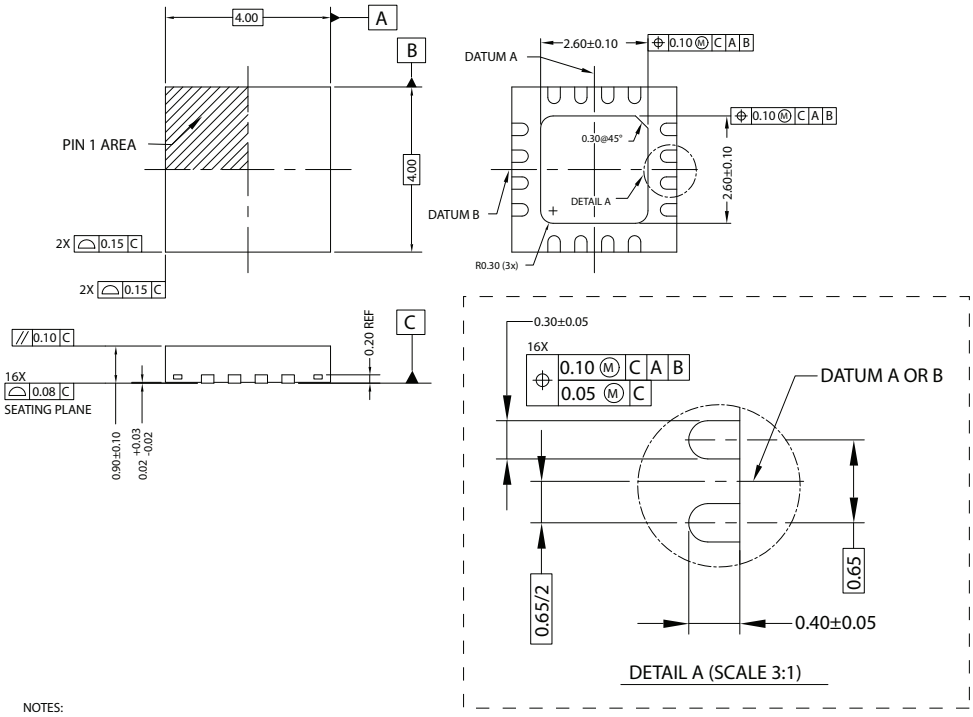


Figure 5-2: GS6042 Alternate Application Circuit Recommended for Drop in Replacement Applications

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6. Package & Ordering Information

6.1 Package Dimensions



NOTES:

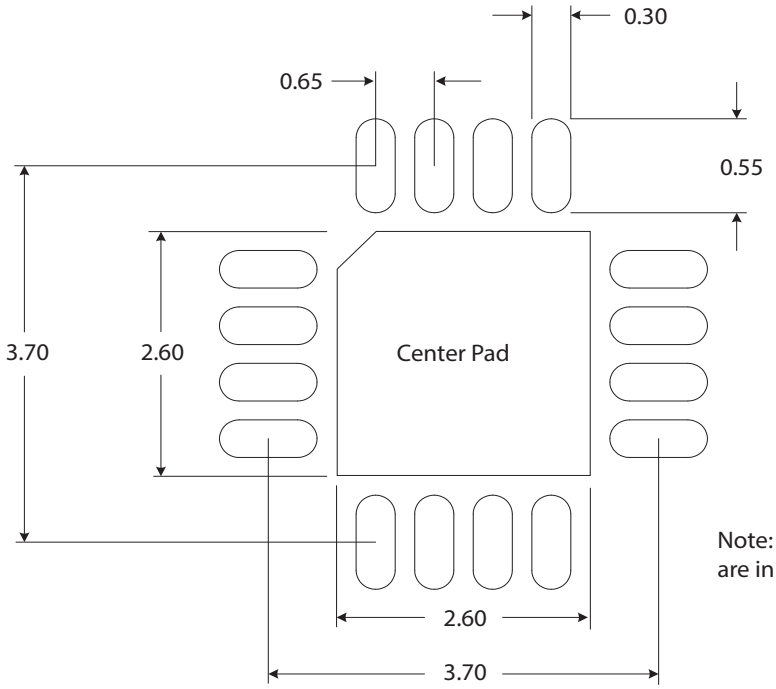
1. DIMENSIONING AND TOLERANCE IS IN CONFORMANCE TO ASME Y14.5-1994
   ALL DIMENSIONS ARE IN MILLIMETERS ° IN DEGREES
2. DIMENSION OF LEAD WIDTH APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP (BOTH ROWS). IF THE TERMINAL HAS OPTIONAL RADIUS ON THE END OF THE TERMINAL, THE LEAD WIDTH DIMENSION SHOULD NOT BE MEASURED IN THAT RADIUS AREA

6.2 Packaging Data

Parameter	Value
Package Type	4mm x 4mm 16-pin QFN
Package Drawing Reference	JEDEC M0220
Moisture Sensitivity Level	1
Junction to Case Thermal Resistance, θ_{j-c}	31.0°C/W
Junction to Air Thermal Resistance, θ_{j-a} (at zero airflow)	43.8°C/W
Psi, ψ	11.0°C/W
Pb-free and RoHS compliant	Yes

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6.3 Recommended PCB Footprint



Note: All dimensions are in millimeters.

The Center Pad should be connected to the most negative power supply plane for analog circuitry in the device (VEE_A) by a minimum of 5 vias.

Note: Suggested dimensions only. Final dimensions should conform to customer design rules and process optimizations.

6.4 Marking Diagram



XXXX - Last 4 digits (excluding decimal) of SAP Batch Assembly (FIN) as listed on Packing Slip.
E3 - Pb-free & Green indicator
YYWW - Date Code

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6.5 Solder Reflow Profiles

The GS6042 is available in a Pb-free package. It is recommended that the Pb-free package be soldered with Pb-free paste using the reflow profile shown in Figure 6-1.

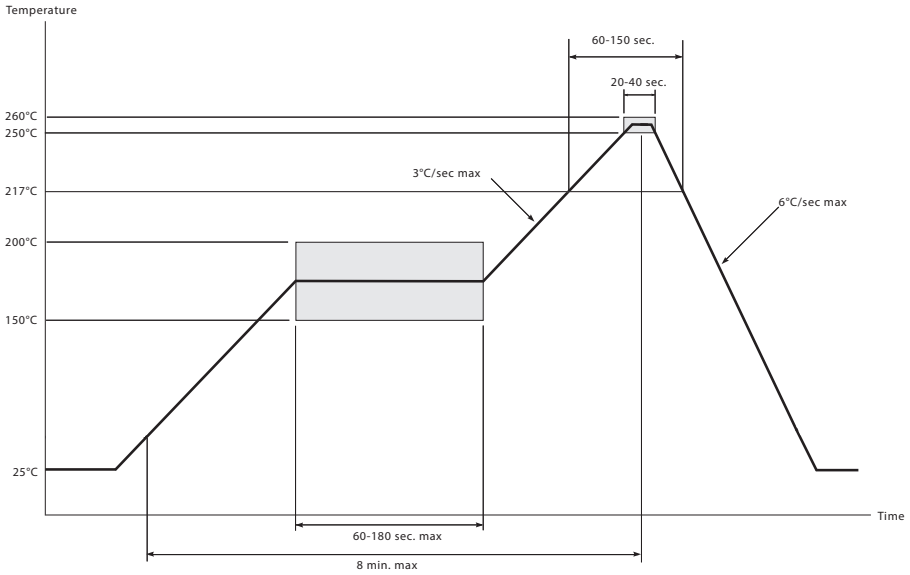


Figure 6-1: Maximum Pb-free Solder Reflow Profile

6.6 Ordering Information

Part Number	Package	Temperature Range
GS6042-INE3	16-pin QFN	-40°C to +85°C

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DOCUMENT IDENTIFICATION
FINAL DATA SHEET
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