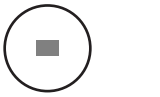
A1304

Linear Hall-Effect Sensor IC with Analog Output, Available in a Miniature, Low-Profile Surface Mount Package

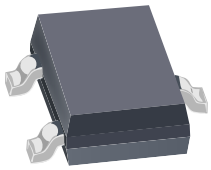
FEATURES AND BENEFITS

- 3.3 V supply operation
- Allegro factory-programmed offset and sensitivity
- Miniature package
- High-bandwidth, low-noise analog output
- High-speed chopping scheme minimizes QVO drift across operating temperature range
- Temperature-stable quiescent voltage output and sensitivity
- Precise recoverability after temperature cycling
- Wide ambient temperature range: –40°C to 85°C
- Immune to mechanical stress

Package: 3-Pin Surface Mount SOT23-W (suffix LH)



Approximate footprint
Not to scale



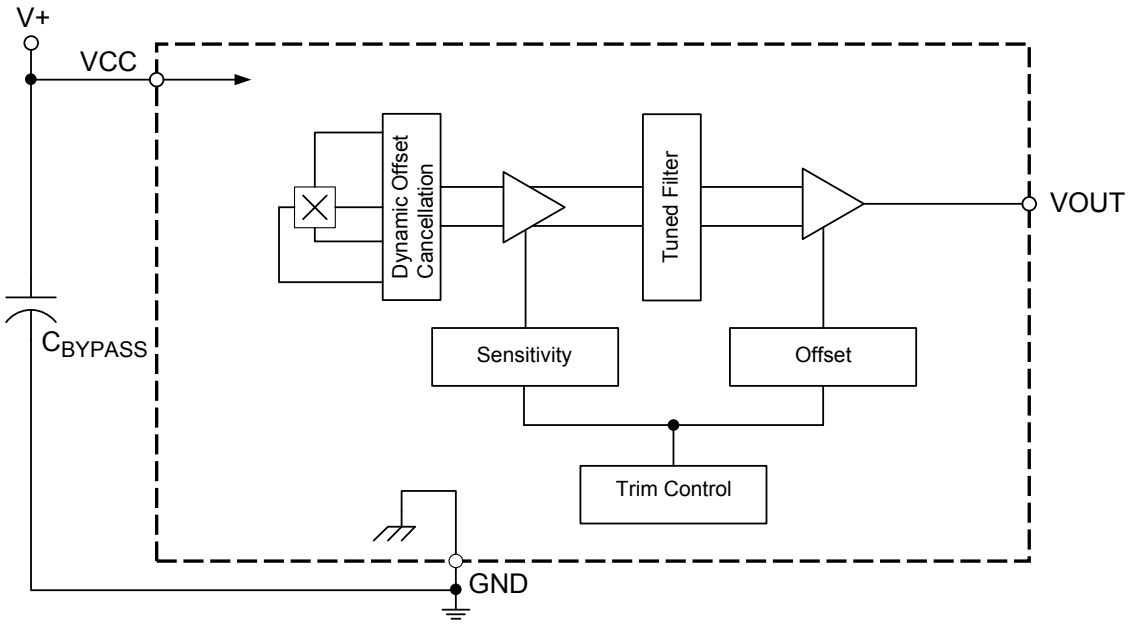
DESCRIPTION

New applications for linear output Hall-effect sensors require medium accuracy and smaller package size. The Allegro A1304 linear Hall-effect sensor IC has been designed specifically to achieve both goals. This temperature-stable device is available in a miniature surface mount package (SOT23-W).

This ratiometric Hall-effect sensor provides a voltage output that is proportional to the applied magnetic field and features a quiescent voltage output of 50% of the supply voltage.

Each BiCMOS monolithic circuit integrates a Hall element, offset and sensitivity trim circuitry to correct for the variation in the Hall element, a small-signal high-gain amplifier, and a proprietary dynamic offset cancellation technique.

The A1304 sensor IC is available in a 3-pin surface mount SOT-23W style package (LH suffix). The package is lead (Pb) free, with 100% matte tin leadframe plating.



Functional Block Diagram

SELECTION GUIDE

Part Number	Sensitivity (typ)(mV/G)	Packing*	Package
A1304ELHLX-T	4.0	10,000 pieces per reel	3-pin SOT-23W surface mount
A1304ELHLX-05-T	0.5	10,000 pieces per reel	3-pin SOT-23W surface mount

*Contact Allegro™ for additional packing options

ABSOLUTE MAXIMUM RATINGS

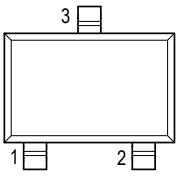
Characteristic	Symbol	Notes	Rating	Unit
Forward Supply Voltage	V_{CC}		5.5	V
Reverse Supply Voltage	V_{RCC}		–0.1	V
Forward Output Voltage	V_{OUT}	For $I_{OUT} < I_{OUT(SINK)}$	7	V
Reverse Output Voltage	V_{ROUT}		–0.1	V
Output Source Current	$I_{OUT(SOURCE)}$	V_{OUT} to GND	1	mA
Output Sink Current	$I_{OUT(SINK)}$	V_{CC} to V_{OUT}	5	mA
Operating Ambient Temperature	T_A	Range E	–40 to 85	°C
Maximum Junction Temperature	T_J(max)		165	°C
Storage Temperature	T_{stg}		–65 to 170	°C

THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

Characteristic	Symbol	Test Conditions*	Value	Units
Package Thermal Resistance	$R_{\theta JA}$	Package LH, 1-layer PCB with copper limited to solder pads	228	°C/W
		Package LH, 2-layer PCB with 0.463 in^2 of copper area each side connected by thermal vias	110	°C/W

*Additional thermal information available on the Allegro website

PINOUT DRAWING AND TERMINAL LIST



LH Package, 3-Pin SOT23-W Pinout Diagram

Terminal List Table

Name	Number	Description
VCC	1	Input power supply; tie to GND with bypass capacitor
VOUT	2	Output signal
GND	3	Ground

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OPERATING CHARACTERISTICS: Valid across T_A, C_{BYPASS} = 0.1 µF, V_{CC} = 3.3 V, unless otherwise noted

Characteristic	Symbol	Test Conditions		Min.	Typ.	Max.	Unit [1]
ELECTRICAL CHARACTERISTICS							
Supply Voltage	V_{CC}			3	–	3.6	V
Supply Current	I_{CC}	No load on VOUT		–	7.7	9	mA
Power-On Time [2][3]	t_{PO}	T_A = 25°C, C_L = 10 nF		–	50	70	µs
V_{CC} Ramp Time [2][3]	t_{VCC}	T_A = 25°C		0.005	–	100	ms
V_{CC} Off Level [2][3]	V_{CCOFF}	T_A = 25°C		0	–	0.33	V
Internal Bandwidth [3]	BW_i	Small signal –3 dB		–	20	–	kHz
OUTPUT CHARACTERISTICS							
Output Referred Noise [3]	V_N	A1304ELHLX-T	T_A = 25°C; C_{BYPASS} = open; no load on VOUT	–	13	–	mV(p–p)
		A1304ELHLX-05-T		–	13	–	mV(p–p)
Input Referred RMS Noise Density [3]	V_{NRMS}	A1304ELHLX-T	T_A = 25°C; C_{BYPASS} = open; no load on VOUT; f << BW_i	–	2.3	–	mG/√Hz
		A1304ELHLX-05-T		–	4.6	–	mG/√Hz
DC Output Resistance [3]	R_{OUT}			–	<1	–	Ω
Output Load Resistance [3]	R_L	VOUT to GND		4.7	–	–	kΩ
Output Load Capacitance [3]	C_L	VOUT to GND		–	–	10	nF
Saturation Voltage [3]	$V_{SAT(HIGH)}$	T_A = 25°C, R_L = 10 kΩ, (VOUT to GND)		2.87	–	–	V
	$V_{SAT(LOW)}$	T_A = 25°C, R_L = 10 kΩ, (VOUT to GND)		–	–	0.38	V
MAGNETIC CHARACTERISTICS							
Sensitivity [4]	Sens	A1304ELHLX-T	T_A = 25°C	3.76	4.0	4.24	mV/G
		A1304ELHLX-05-T		0.2	0.5	0.8	mV/G
Sensitivity Temperature Coefficient [3]	TC_{Sens}	T_A = 85°C, relative to Sens at 25°C		0.04	0.12	0.2	%/°C
Quiescent Voltage Output (QVO)	$V_{OUT(Q)}$	T_A = 25°C, B = 0 G		1.625	1.65	1.675	V
Delta QVO	$\Delta V_{OUT(Q)}$	A1304ELHLX-T	T_A = 85°C, relative to QVO at 25°C	–	±40	–	mV
		A1304ELHLX-05-T		–	±40	–	mV
Ratiometry Quiescent Voltage Output Error	$Rat_{VOUT(Q)}$	Across specified supply voltage range (relative to V_{CC} = 3.3 V)		–	±1.5	–	%
Ratiometry Sensitivity Error	Rat_{Sens}	Across specified supply voltage range (relative to V_{CC} = 3.3 V)		–	±1.5	–	%
Linearity Sensitivity Error	Lin_{ERR}	A1304ELHLX-T	Typ. Sensitivity, ±300 G	–	±1.5	–	%
		A1304ELHLX-05-T	Typ. Sensitivity, ±2250 G	–	±1.5	–	%
Sensitivity Drift Due to Package Hysteresis	$\Delta Sens_{PKG}$	T_A = 25°C, after temperature cycling		–	±2	–	%
Magnetic Field Range	B	A1304ELHLX-T	Range of Input Field	–	±375	–	G
		A1304ELHLX-05-T		–	±3000	–	G

[1] 1 gauss (G) is exactly equal to 0.1 millitesla (mT).
[2] See Characteristic Definitions section.
[3] Based on design simulations and/or characterization data. Not tested at Allegro end-of-line.
[4] Sensitivity drift through the life of the part, $\Delta Sens_{LIFE}$, can have a typical error value ±3% in addition to package hysteresis effects.

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CHARACTERISTIC DEFINITIONS

Power-On Time. When the supply is ramped to its operating voltage, the device output requires a finite time to react to an input magnetic field. Power-On Time, t_{PO}, is defined as the time it takes for the output voltage to begin responding to an applied magnetic field after the power supply has reached its minimum specified operating voltage, V_{CC}(min), as shown in Figure 1.

Quiescent Voltage Output. In the quiescent state (no significant magnetic field: B = 0 G), the output, $V_{OUT(Q)}$, is at a constant ratio to the supply voltage, V_{CC}, across the entire operating ranges of V_{CC} and Operating Ambient Temperature, T_A.

Quiescent Voltage Output Drift Across Temperature Range. Due to internal component tolerances and thermal considerations, the Quiescent Voltage Output, $V_{OUT(Q)}$, may drift due to temperature changes within the Operating Ambient Temperature, T_A. For purposes of specification, the Quiescent Voltage Output Drift Across Temperature Range, $\Delta V_{OUT(Q)}$ (mV), is defined as:

$$\Delta V_{OUT(Q)} = V_{OUT(Q)(TA)} - V_{OUT(Q)(25°C)} \quad (1)$$

Sensitivity. The amount of the output voltage change is proportional to the magnitude and polarity of the magnetic field applied. This proportionality is specified as the magnetic sensitivity, Sens (mV/G), of the device and is defined as:

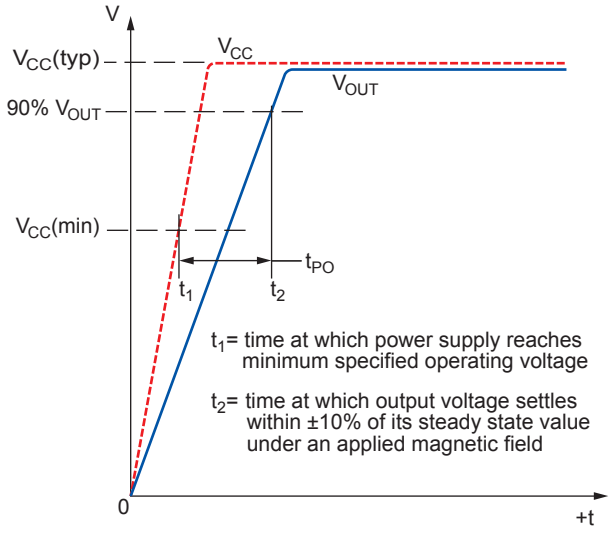


Figure 1: Definition of Power-On Time, t_{PO}

$$\text{Sens} = \frac{V_{OUT(B+)} - V_{OUT(B-)}}{(B+) - (B-)} \quad (2)$$

where B+ is the magnetic flux density in a positive field (south polarity) and B– is the magnetic flux density in a negative field (north polarity).

Sensitivity Temperature Coefficient. The device sensitivity changes as temperature changes, with respect to its Sensitivity Temperature Coefficient, TC_{SENS}. TC_{SENS} is defined as:

$$TC_{Sens} = \left(\frac{Sens_{T2} - Sens_{T1}}{Sens_{T1}} \times 100\right)\left(\frac{1}{T2 - T1}\right) \quad (\%/°C) \quad (3)$$

where T1 is the baseline Sens programming temperature of 25°C, and T2 is the sensitivity at another temperature.

The ideal value of Sens across the full ambient temperature range, $Sens_{IDEAL(TA)}$, is defined as:

$$Sens_{IDEAL(TA)} = Sens_{T1} \times [100\ (\%) + TC_{SENS}\ (T_A - T1)] \quad (4)$$

Linearity Sensitivity Error. The A1304 is designed to provide linear output in response to a ramping applied magnetic field. Consider two magnetic fields, B1 and B2. Ideally, the sensitivity of a device is the same for both fields, for a given supply voltage and temperature. Linearity error is present when there is a difference between the sensitivities measured at B1 and B2.

Linearity Sensitivity Error, LIN_{ERR}, is calculated separately for positive (Lin_{ERR+}) and negative (Lin_{ERR-}) applied magnetic fields. LIN_{ERR} (%) is measured and defined as:

$$Lin_{ERR+} = \left(1 - \frac{Sens_{(B+)(2)}}{Sens_{(B+)(1)}}\right) \times 100 \quad (\%) \quad (5)$$

$$Lin_{ERR-} = \left(1 - \frac{Sens_{(B-)(2)}}{Sens_{(B-)(1)}}\right) \times 100 \quad (\%)$$

where:

$$Sens_{Bx} = \frac{|V_{OUT(Bx)} - V_{OUT(Q)}|}{B_x} \quad (6)$$

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and Bx are positive and negative magnetic fields, with respect to the quiescent voltage output, such that

$$|B_{(+)(2)}| > |B_{(+)(1)}| \text{ and } |B_{(-)(2)}| > |B_{(-)(1)}|$$

The effective linearity error is:

$$\text{Lin}_{ERR} = \max(|\text{Lin}_{ERR+}|, |\text{Lin}_{ERR-}|) \quad (7)$$

The saturation of the output at $V_{SAT(HIGH)}$ and $V_{SAT(LOW)}$ will limit the operating magnetic range of the applied field in which the device provides a linear output. The maximum positive and negative applied magnetic fields in the operating range can be calculated:

$$|B_{MAX(+)}| = \frac{V_{SAT(HIGH)} - V_{OUT(Q)}}{\text{Sens}}$$

$$|B_{MAX(-)}| = \frac{V_{OUT(Q)} - V_{SAT(LOW)}}{\text{Sens}} \quad (8)$$

Ratiometry Error. The A1304 provides ratiometric output. This means that the Quiescent Voltage Output, $V_{OUT(Q)}$, and the magnetic sensitivity, Sens, are proportional to the supply voltage, V_{CC}. In other words, when the supply voltage increases or decreases by a certain percentage, each characteristic also increases or decreases by the same percentage. Error is the difference between the measured change in the supply voltage relative to 3.3 V, and the measured change in each characteristic.

The ratiometric error in quiescent voltage output, $\text{Rat}_{VOUT(Q)}$ (%), for a given supply voltage, V_{CC}, is defined as:

$$\text{Rat}_{VOUT(Q)} = \left(1 - \frac{V_{OUT(Q)(VCC)} / V_{OUT(Q)(3.3V)}}{V_{CC} / 3.3\ (V)}\right) \times 100 \quad (\%) \quad (9)$$

The ratiometric error in magnetic sensitivity, Rat_{Sens} (%), for a given supply voltage, V_{CC}, is defined as:

$$\text{Rat}_{Sens} = \left(1 - \frac{\text{Sens}_{(VCC)} / \text{Sens}_{(3.3V)}}{V_{CC} / 3.3\ (V)}\right) \times 100 \quad (\%) \quad (10)$$

V_{CC} Ramp Time. The time taken for V_{CC} to ramp from 0 V to V_{CC}(typ), 3.3 V (see figure 3).

V_{CC} Off Level. For applications in which the VCC pin of the A1304 is being power-cycled (for example using a multiplexer to toggle the part on and off), the specification of V_{CC} Off Level, V_{CCOFF}, determines how high a V_{CC} off voltage can be tolerated while still ensuring proper operation and startup of the device (see Figure 3).

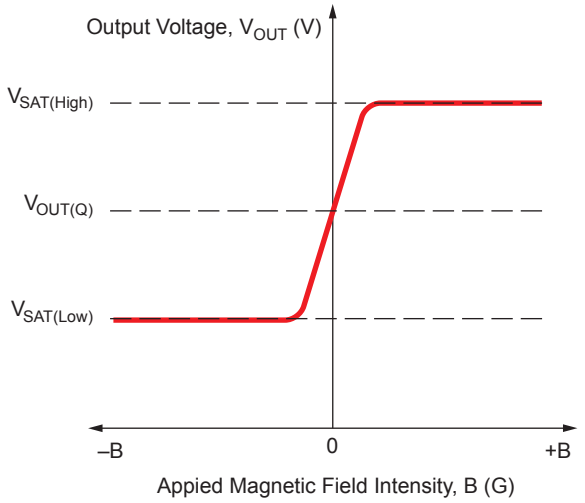


Figure 2: Effect of Saturation

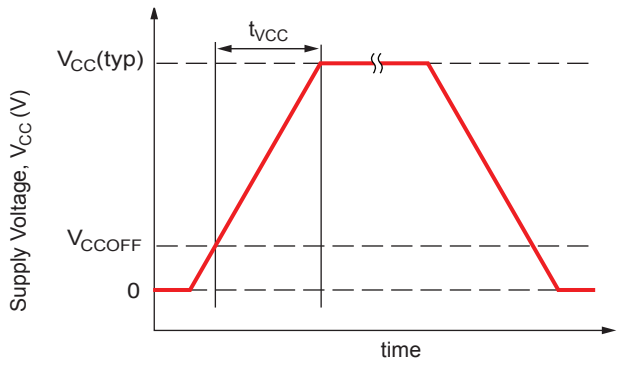


Figure 3: Definition of V_{CC} Ramp Time, t_{VCC}

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Undervoltage Lockout. The A1304 provides an undervoltage lockout feature which ensures that the device outputs a VOUT signal only when V_{CC} is above certain thresholds. The undervoltage lockout feature provides a hysteresis of operation to eliminate indeterminate output states.

The output of the A1304 is held low (GND) until V_{CC} exceeds the V_{CC} rising UVLO reset threshold. After that, the device VOUT output is enabled, providing a ratiometric output voltage that is proportional to the input magnetic signal and V_{CC}. If V_{CC} should drop back down below the V_{CC} falling UVLO trip threshold after the device is powered up, the output would be pulled low (see Figure 4) until V_{CC} rising UVLO reset threshold is reached again and VOUT would be reenabled.

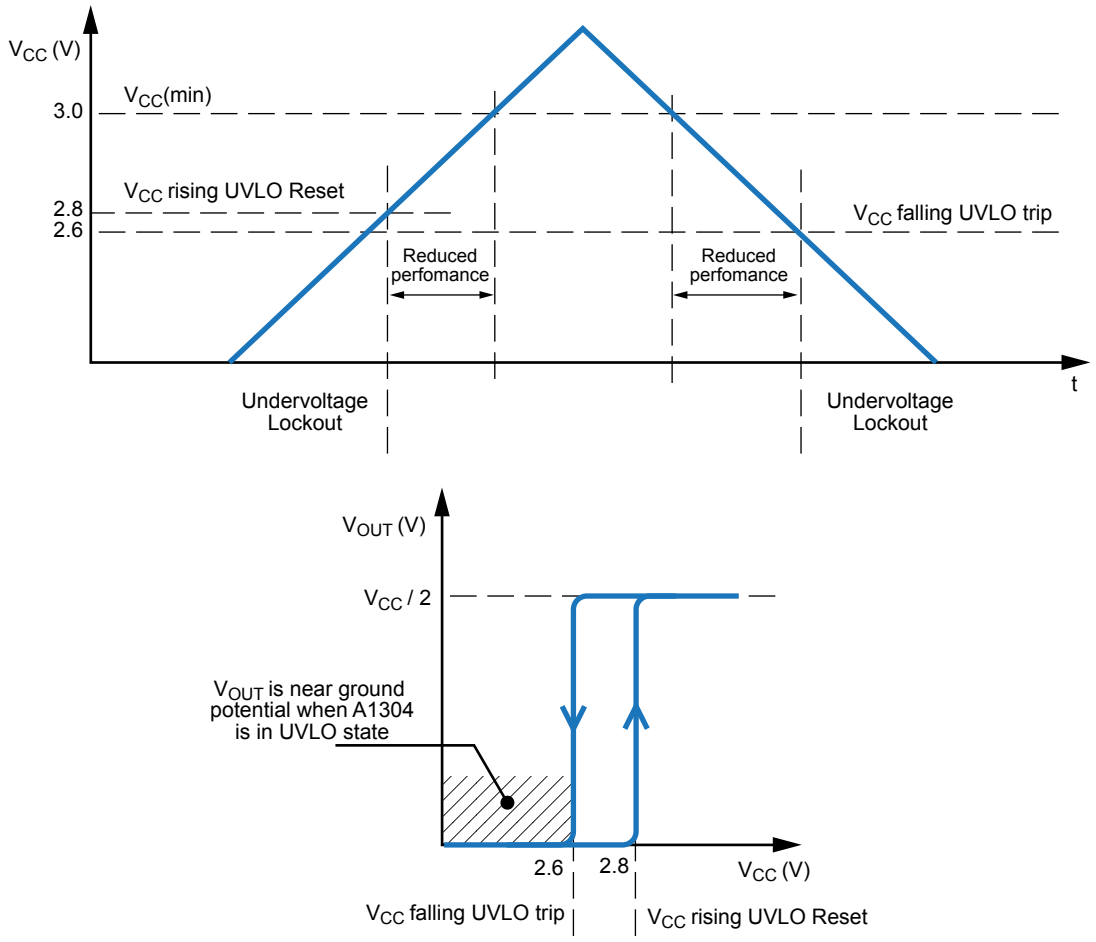


Figure 4: UVLO Operation

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APPLICATION INFORMATION

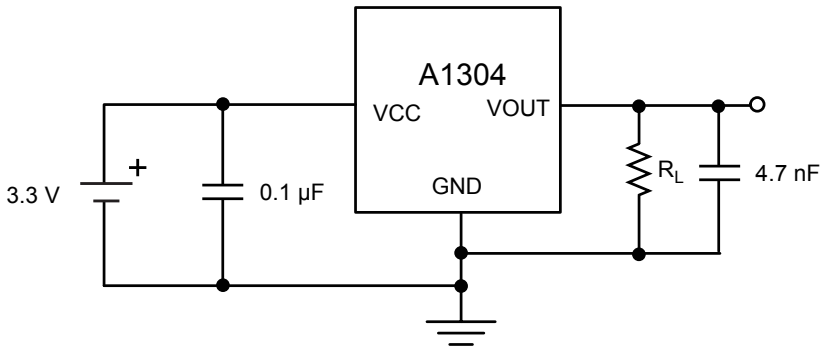


Figure 5: Typical Application Circuit

Chopper Stabilization Technique

When using Hall-effect technology, a limiting factor for switchpoint accuracy is the small signal voltage developed across the Hall element. This voltage is disproportionally small relative to the offset that can be produced at the output of the Hall sensor IC. This makes it difficult to process the signal while maintaining an accurate, reliable output over the specified operating temperature and voltage ranges. Chopper stabilization is a unique approach used to minimize Hall offset on the chip. Allegro employs a technique to remove key sources of the output drift induced by thermal and mechanical stresses. This offset reduction technique is based on a signal modulation-demodulation process. The undesired offset signal is separated from the magnetic field-induced signal in the frequency domain, through modulation. The subsequent demodulation acts as a modulation process for the offset, causing the magnetic field-induced signal to recover its original spectrum at base band, while the DC offset becomes a high-frequency signal. The magnetic-sourced signal then can pass through a low-pass filter, while the modulated DC offset is suppressed. In addition to the removal of the thermal and mechanical stress related offset, this novel technique also reduces the amount of thermal noise in the Hall sensor IC while completely removing the modulated residue resulting from the chopper operation. The chopper stabilization technique uses a high frequency sampling clock. For demodulation process, a sample and hold technique is used. This high-frequency operation allows a greater sampling rate, which results in higher accuracy and faster signal-processing capability. This approach desensitizes the chip to the effects of thermal and mechanical stresses, and produces devices that have extremely stable quiescent Hall output voltages and precise recoverability after temperature cycling. This technique is made possible through the use of a BiCMOS process, which allows the use of low-offset, low-noise amplifiers in combination with high-density logic integration and sample-and-hold circuits.

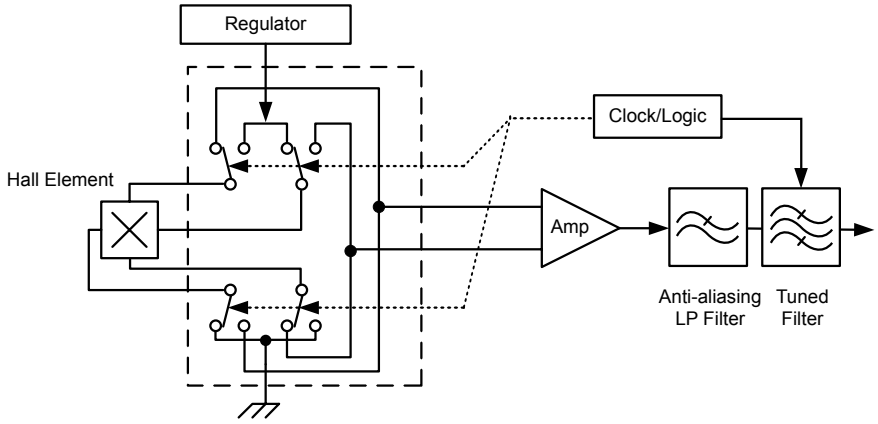


Figure 6: Chopper Stabilization Technique

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PACKAGE OUTLINE DIAGRAM

For Reference Only – Not for Tooling Use

(Reference Allegro DWG-0000628, Rev. 1)
NOT TO SCALE
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

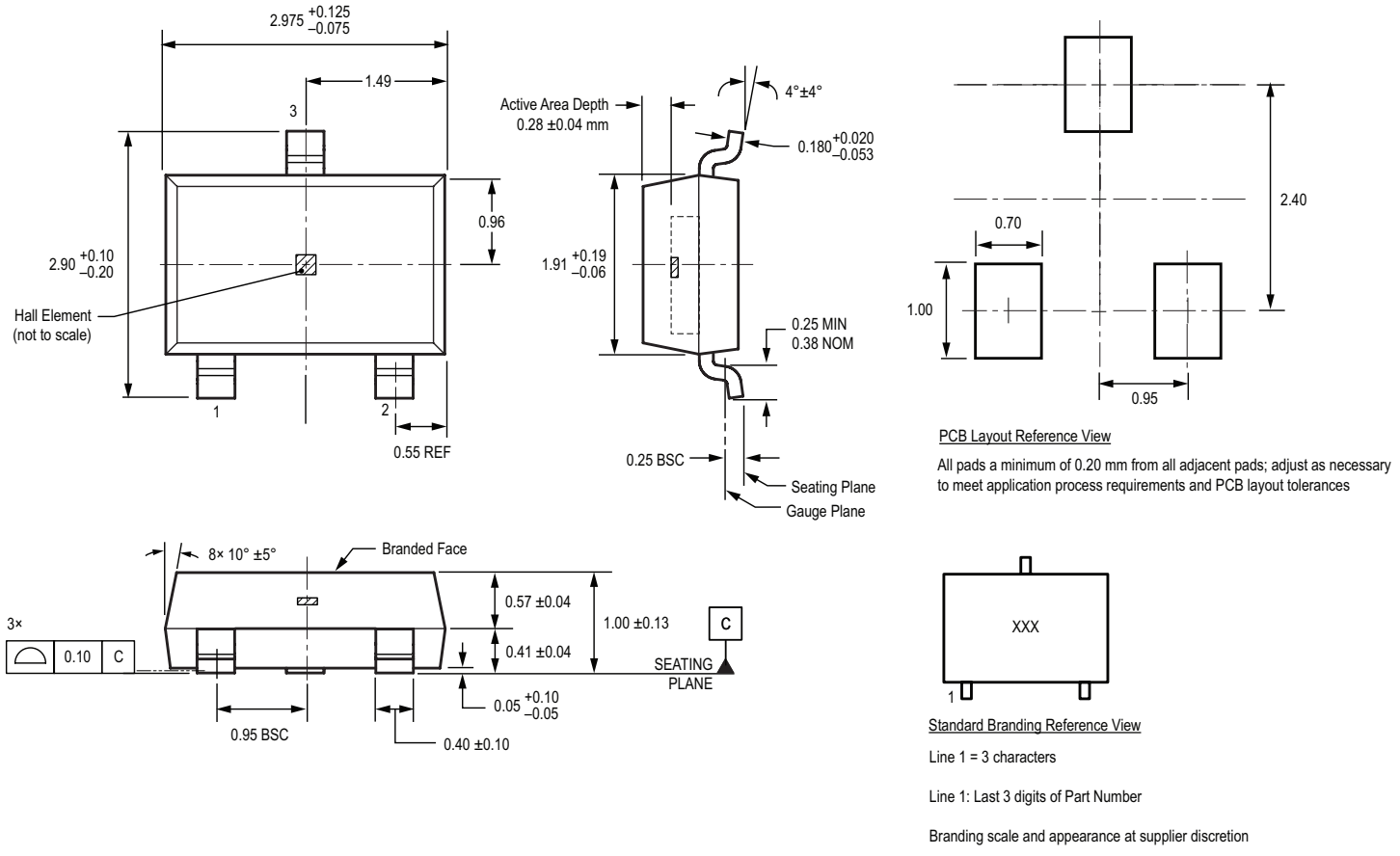


Figure 7: Package LH, 3-Pin (SOT-23W)

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Revision History

Number	Date	Description
–	June 16, 2014	Initial Release
1	July 13, 2015	Corrected LH package Active Area Depth value
2	September 18, 2018	Clarified Absolute Maximum Ratings; minor editorial updates
3	September 30, 2019	Minor editorial updates
4	November 18, 2021	Updated package drawing (page 8)

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