EClamp2515K
ESD Protection Device for T-Flash/MicroSD Interfaces

PROTECTION PRODUCTS - EMIClamp®

Description

EClamp®2515K is combination EMI filter and line termination device with integrated TVS diodes for use on Multimedia Card interfaces. This device utilizes solid-state silicon-avalanche technology for superior clamping performance and DC electrical characteristics. They have been optimized for **protection of T-Flash/MicroSD interfaces** in cellular phones and other portable electronics.

The device consists of six circuits that include series impedance matching resistors and pull up resistors as required by the SD specification. TVS diodes are included on each line for ESD protection. Each data line has a typical capacitance of 22pF while the clock line has a typical capacitance of only 12pF. An additional TVS diode connection is included for protection of the voltage (Vdd) bus. A 45 Ohm termination resistor is included on the DAT0, DAT1, DAT2, DAT3, CMD, and CLK lines. Pull up resistors of 15k Ohms are included on DAT0, DAT1, DAT2, DAT3, and CMD lines. TVS diodes provide effective suppression of ESD voltages in excess of ±15kV (air discharge) and ±12kV (contact discharge) per IEC 61000-4-2.

EClamp2515K is in a 16-pin SLP3313P16 package. It measures 3.3 x 1.3 x 0.50mm. The leads are spaced at a pitch of 0.4mm and are finished with lead-free NiPdAu.

Features

- EMI/RFI filtering and line termination with integrated ESD protection
- ESD protection to **IEC 61000-4-2 (ESD), ±15kV (air), ±12kV (contact)** on input lines
- TVS working voltage: 5V
- Termination Resistors: 45Ω
- Pull Up Resistors: 15kΩ (4 each)
- Typical capacitance on DAT and CMD lines: 22pF (VR = 0V)
- Typical capacitance on CLK line: 12pF (VR=0V)
- Solid-state technology

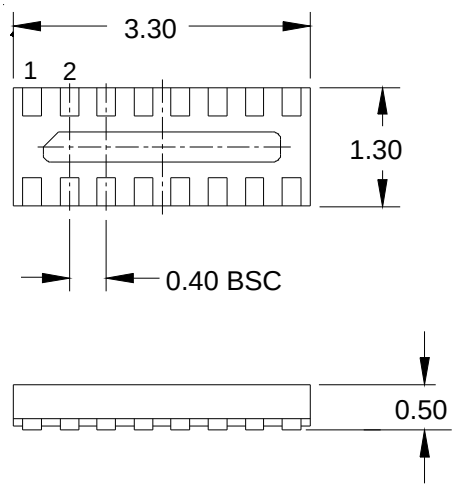
Mechanical Characteristics

- SLP3313P16 16-pin package
- Pb-Free, Halogen Free, RoHS/WEEE Compliant
- Nominal Dimensions: 3.3 x 1.3 x 0.50 mm
- Lead Pitch: 0.4mm
- Lead finish: NiPdAu
- Marking: Marking Code
- Packaging: Tape and Reel

Applications

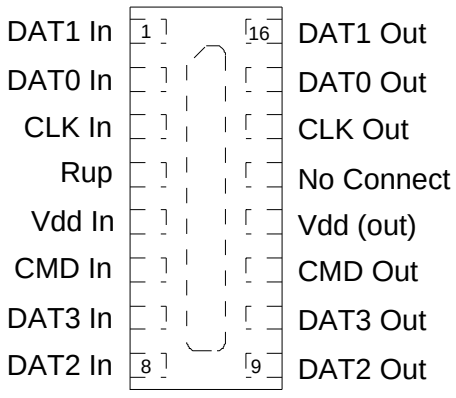
- T-Flash / MicroSD Interfaces
- MMC Interfaces
- CDMA, GSM, 3G Cell Phones

Package Dimensions



Nominal Dimensions in mm (Bottom View)

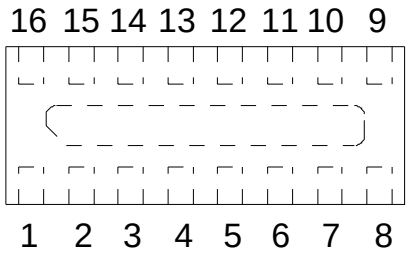
Pin Configuration



Pin Designation (Top View)

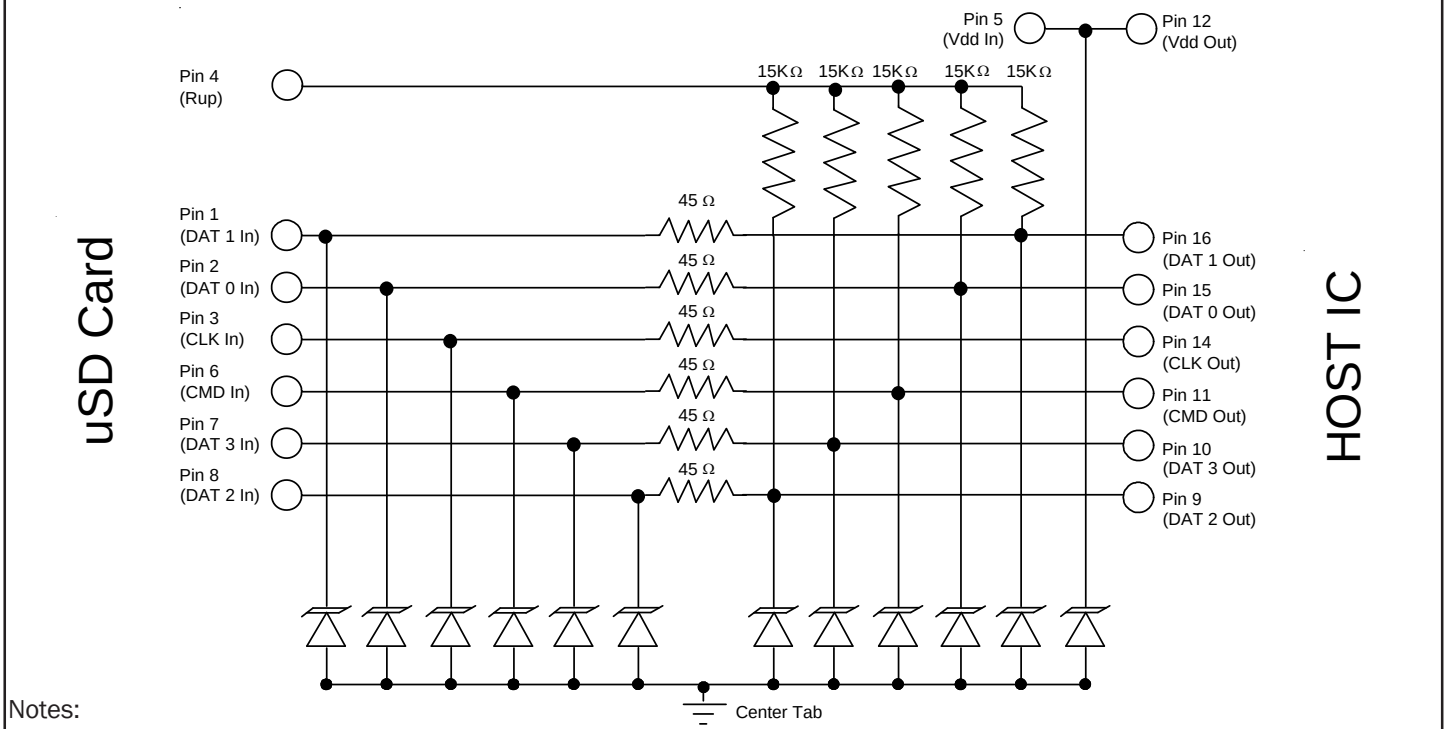
Pin Identification and Configuration

Pin	Symbol	Identification
1, 16	DAT1	Data line #1 input/output
2, 15	DAT0	Data line #0 Input/Output
3, 14	Clock	Clock line Input/Output
4	Rup	15K Pull-up resistors
5, 12	Vdd	Power Supply ESD Protection in/output
6, 11	CMD	Command Line Input/Output
7, 10	DAT3	Data line #3 input/output
8, 9	DAT2	Data line #2 input/output
13	NC	Not connected
Center tab	GND	Ground connection



Pin Configuration (Top View)

Schematics & Component Values



Notes:
In = Connector (uSD Card) Side
Out = Protected (Host) IC Side

Absolute Maximum Rating

Parameter	Symbol	Value	Units
Junction Temperature	T_J	125	°C
Operating Temperature	T_{op}	-40 to +85	°C
Storage Temperature	T_{STG}	-55 to +150	°C
ESD per IEC 61000-4-2			
Input Pins 1, 2, 3, 5, 6, 7, 8, 12 (Contact)[1] Input Pins 1, 2, 3, 5, 6, 7, 8, 12 (Air)[1]	V_{ESD}	+/- 12 +/- 15	kV
Output Pins 4, 9, 10, 11, 14, 15, 16 (Contact)[1] Output Pins 4, 9, 10, 11, 14, 15, 16 (Air)[1]	V_{ESD}	+/- 10 +/- 10	kV

Electrical Characteristics (T = 25°C)

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
TVS Reverse Stand-Off Voltage	V_{RWM}				5	V
TVS Reverse Breakdown Voltage	V_{BR}	I_t = 1mA	6	8	10	V
TVS Reverse Leakage Current	I_R	V_{RWM} = 3.0V			0.1	µA
Series Resistors	R	Each Line	38	45	52	Ohms
DAT Pull Up Resistor	R_{up}		12	15	18	k Ohms
Dynamic Resistance[2, 3]	R_{DYN}	tp = 100ns, Measured from 4A to 16A		0.40		Ohms
Total Capacitance	C_{in}	Input to Gnd, Pins 1, 2, 6, 7, 8 V_R = 0V, f = 1MHz	10	22	25	pF
Total Capacitance	C_{in}	Input to Gnd, Pin 3, 5, 12 V_R = 0V, f = 1MHz	6	12	15	pF

Notes

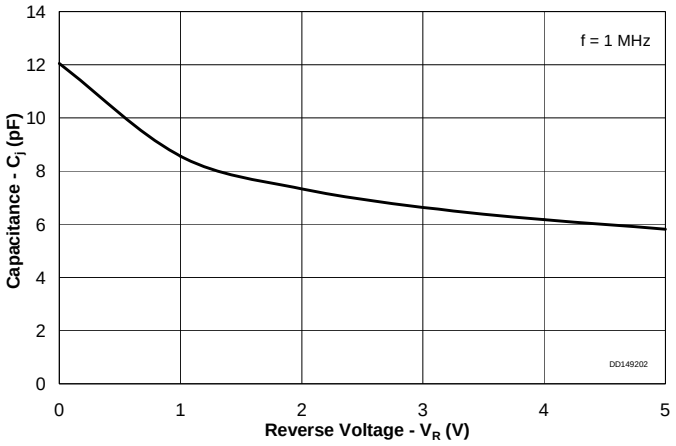
1)Measured with a 20dB attenuator, 50 Ohm scope input impedance, 2GHz bandwidth. ESD gun return path connected to ESD ground plane.

2)Transmission Line Pulse Test (TLP) Settings: t_p = 100ns, t_r = 0.2ns, I_{TLP} and V_{TLP} averaging window: t_1 = 70ns to t_2 = 90ns.

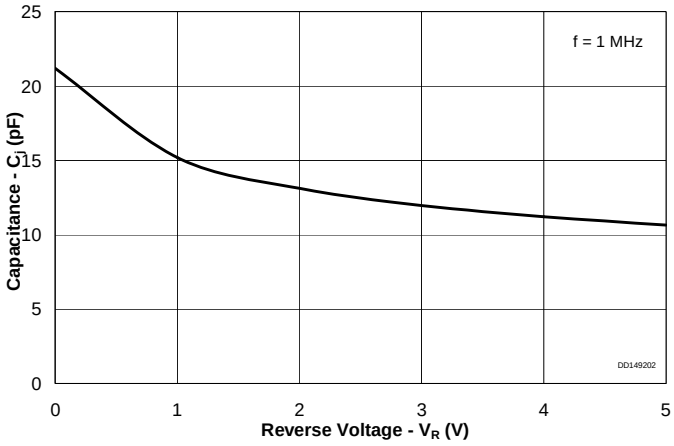
3) Dynamic resistance calculated from I_{TLP} = 4A to I_{TLP} = 16A

Typical Characteristics

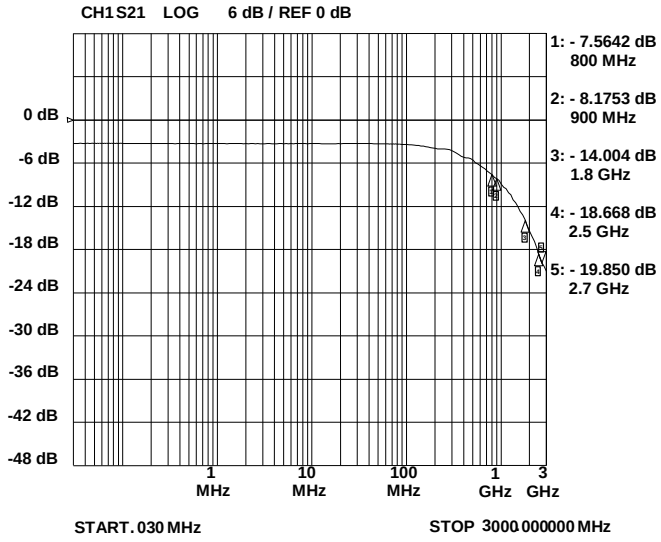
Capacitance vs. Reverse Voltage (CLK & VDD)



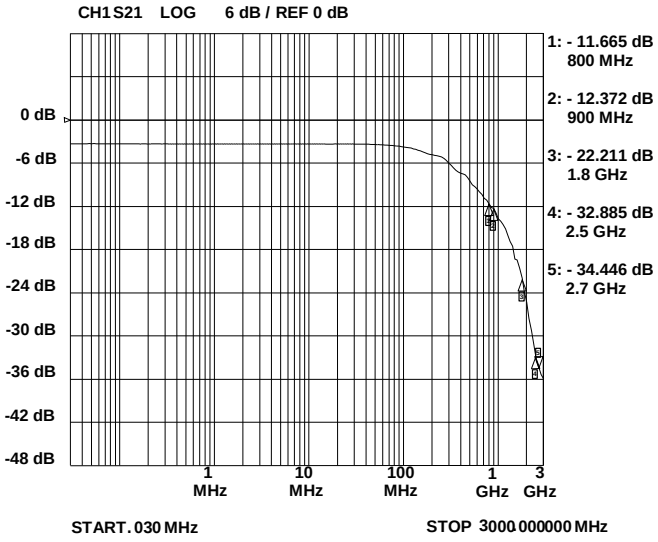
Capacitance vs. Reverse Voltage (DAT & CMD Lines)



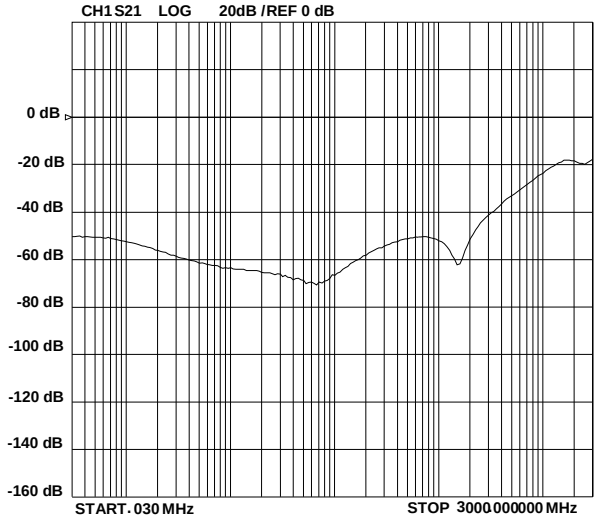
Typical Insertion Loss S21 (CLK Line)



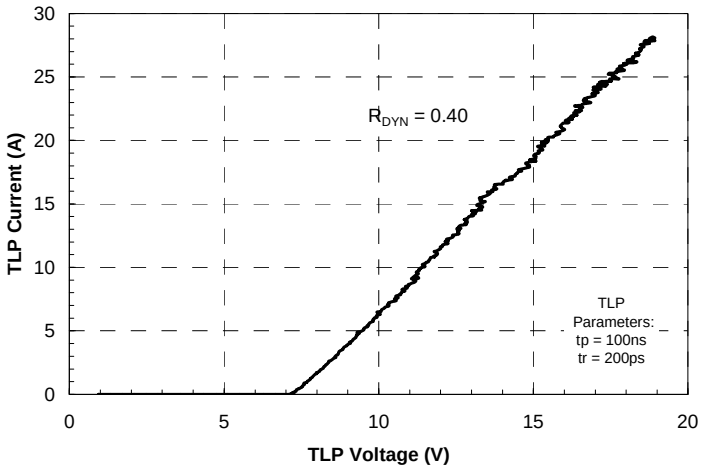
Typical Insertion Loss S21 (Each DAT Line)



Analog Crosstalk

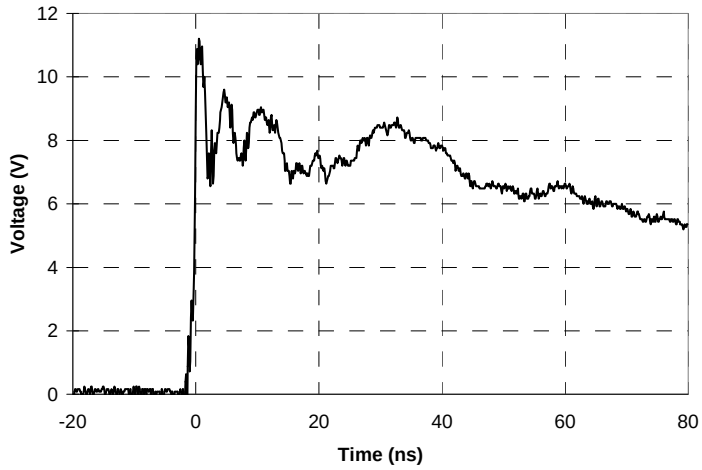


TLP Characteristic

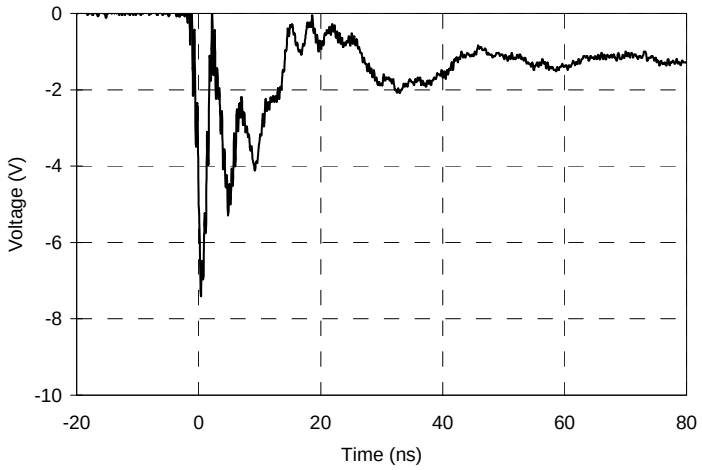


Typical Characteristics

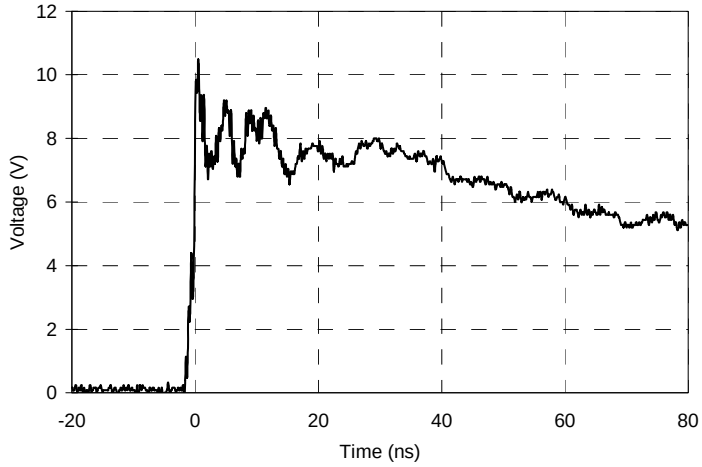
ESD Clamping (+8kV Contact per IEC 61000-4-2)
DAT Lines



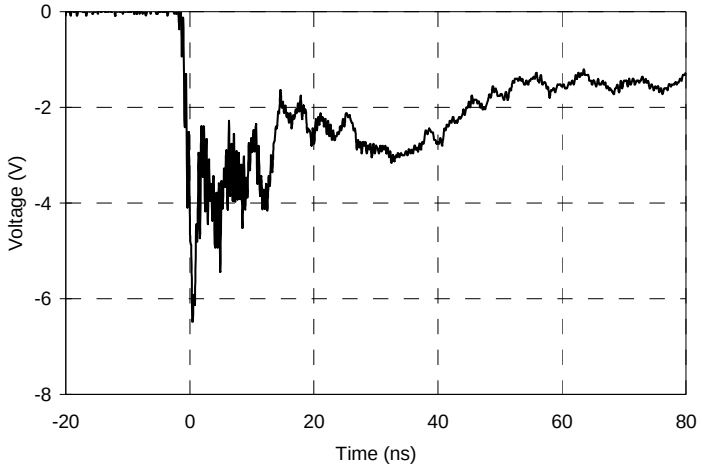
ESD Clamping (-8kV Contact per IEC 61000-4-2)
DAT Lines



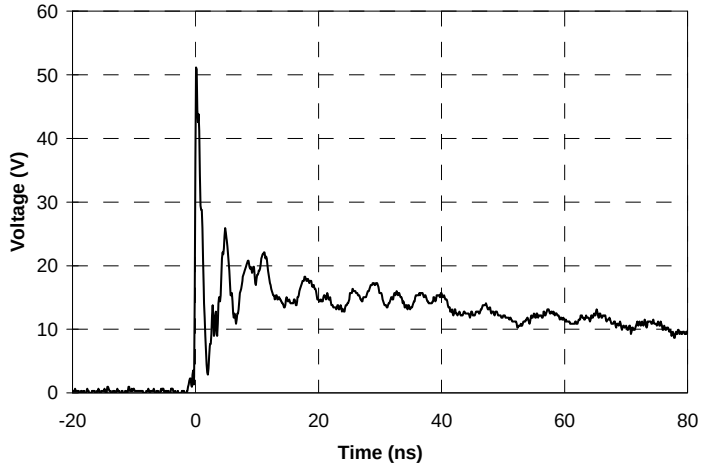
ESD Clamping +8kV Contact per IEC 61000-4-2)
CLK Line



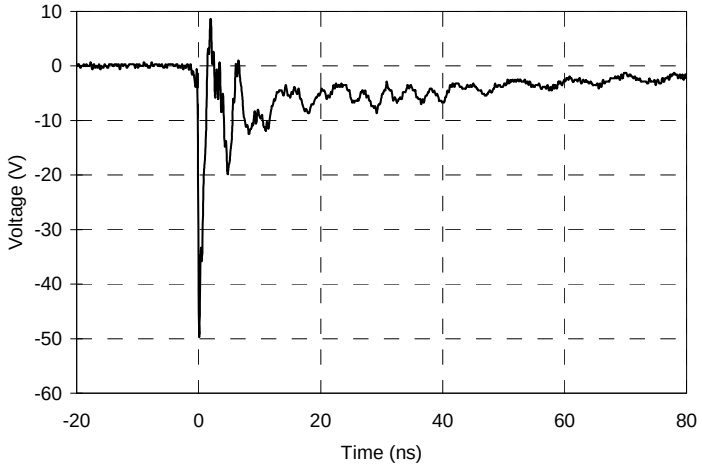
ESD Clamping -8kV Contact per IEC 61000-4-2)
CLK Line



ESD Clamping +8kV Contact per IEC 61000-4-2)
VDD Line



ESD Clamping -8kV Contact per IEC 61000-4-2)
VDD Line



Applications Information

Device Connection

The EClamp2515K is a microSD/T-Flash interface device designed for use in cell phones and other portable electronic devices. The EClamp2515K is comprised of series and pull up resistors required on the microSD interface. Each line also includes TVS diodes for ESD protection.

The EClamp2515K is in a 16-pin SLP package. Electrical connection is made to the 16 pins located at the bottom of the device. The device has a flow through design for easy layout. Pin connections are noted in Figure 1. A center tab serves as the ground connection. Recommendations for the ground connection are given below.

Ground Connection Recommendation

Parasitic inductance present in the board layout will affect the filtering and ESD performance of the device. Ground loop inductance can be reduced by using multiple vias to make the connection to the ground plane. Figure 2 shows the recommended device layout. The ground pad vias have a diameter of 0.008 inches (0.20 mm) while the two external vias have a diameter of 0.010 inches (0.250mm). The internal vias are spaced approximately evenly from the center of the pad. The designer may choose to use more vias with a smaller diameter (such as 0.005 inches or 0.125mm) since changing the diameter of the via will result in little change in inductance.

Figure 1 - Pin Identification and Configuration (Top Side View)

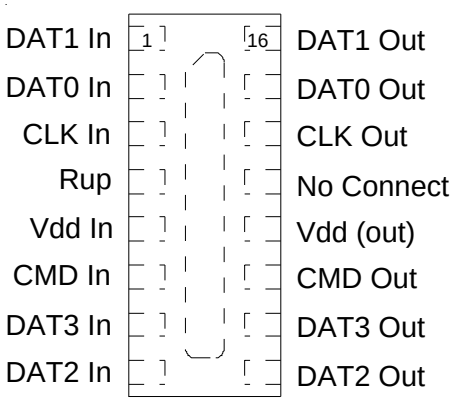
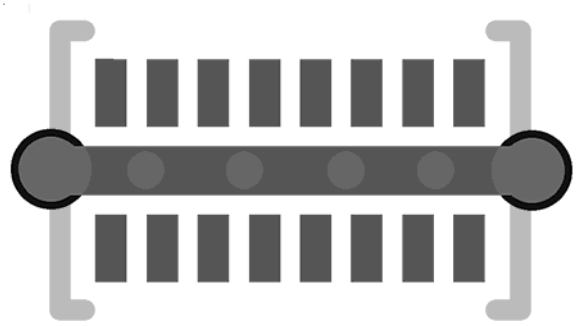
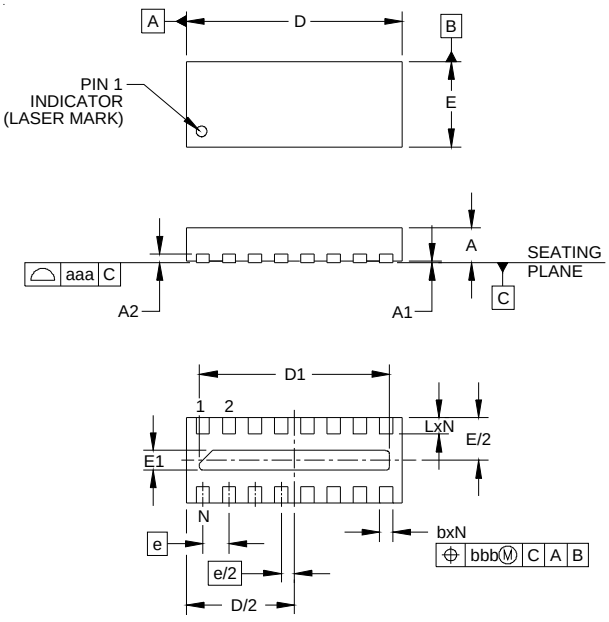


Figure 2 - Recommended Layout using Ground Vias



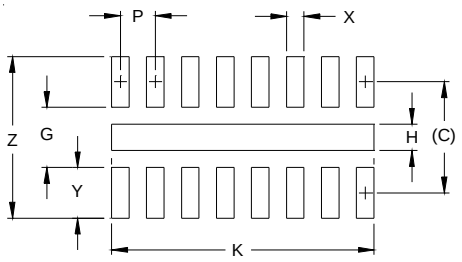
Outline Drawing - SLP3313P16T



DIMENSIONS						
DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.018	.020	.022	0.45	0.50	0.55
A1	.000	.001	.002	0.00	0.02	0.05
A2		(.005)			(0.13)	
b	.006	.008	.010	0.15	0.20	0.25
D	.128	.130	.133	3.25	3.30	3.375
D1	.110	.114	.118	2.80	2.90	3.00
E	.049	.051	.054	1.25	1.30	1.375
E1	.008	.012	.016	0.20	0.30	0.40
e		.016 BSC			0.40 BSC	
L	.008	.010	.012	0.20	0.25	0.30
N		16			16	
aaa		.003			0.08	
bbb		.004			0.10	

NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

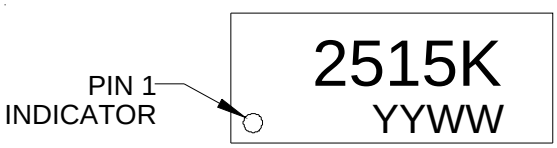
Land Pattern - SLP3313P16T



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.050)	(1.27)
G	.027	0.69
H	.012	0.30
K	.118	3.00
P	.016	0.40
X	.008	0.20
Y	.023	0.58
Z	.073	1.85

NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

Marking Code



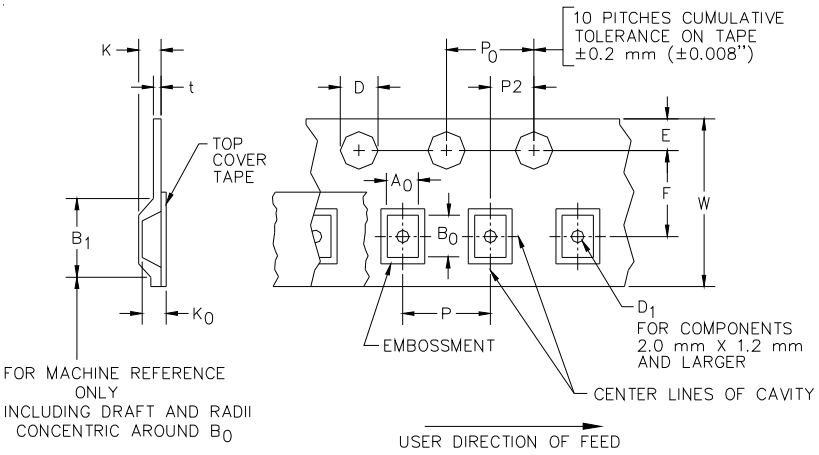
YYWW = Date Code

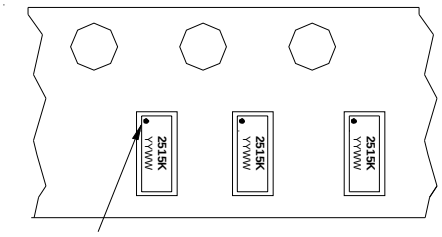
Ordering Information

Part Number	Qty per Reel	Reel Size
EClamp2515K.TCT	3000	7 Inch

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Tape and Reel Specification





Device Orientation in Tape

A0	B0	K0
1.51 +/-0.10 mm	3.51 +/-0.10 mm	0.66 +/-0.10 mm

Tape Width	B, (Max)	D	D1	E	F	K (MAX)	P	P0	P2	T(MAX)	W
12 mm	8.2 mm (.476)	1.5 + 0.1 mm - 0.0 mm (0.59 +.005 - .000)	1.0 mm ±0.05 (.039)	1.750±.10 mm (.069±.004)	5.5±0.05 mm (.217±.002)	4.5 mm (.177)	4.0±0.1 mm (.157±.00-4)	4.0±0.1 mm (.157±.00-4)	2.0±0.05m-m (.079±.002)	0.4 mm (.016)	12.0 mm + 0.3 mm - 0.1 mm (.472±.012)

Contact Information

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