Brief Description

The ZSC31010 is a sensor signal conditioner integrated circuit, which enables easy and precise calibration of resistive bridge sensors via EEPROM. When mated to a resistive bridge sensor, it will digitally correct offset and gain with the option to correct offset and gain coefficients and linearity over temperature. A second-order compensation can be enabled for temperature coefficients of gain or offset or bridge linearity. The ZSC31010 communicates via IDT's ZACwire™ serial interface to the host computer and is easily mass calibrated in a Windows® environment. Once calibrated, the output pin Sig™ can provide selectable 0 to 1 V, rail-to-rail ratiometric analog output, or digital serial output of bridge data with optional temperature data.

Features

- Digital compensation of sensor offset, sensitivity, temperature drift, and non-linearity
- Accommodates differential sensor signal spans, from 3 mV/V to 105 mV/V
- ZACwire™ One-Wire Interface (OWI)
- Internal temperature compensation and detection via bandgap PTAT (proportional to absolute temperature)
- Output options: rail-to-rail analog output voltage, absolute analog voltage, digital ZACwire™ One-Wire Interface (OWI)
- Optional sequential output of both temperature and bridge readings on ZACwire™ digital output
- Fast response time, 1 ms (typical)
- High voltage protection up to 30 V with external JFET
- Chopper-stabilized true differential ADC
- Buffered and chopper-stabilized output DAC

Benefits

- No external trimming components required
- Simple PC-controlled configuration and calibration via ZACwire™ One-Wire Interface
- High accuracy (±0.1% FSO @ -25 to 85°C; ±0.25% FSO @ -50 to 150°C)
- Single pass calibration – quick and precise
- Suitable for battery-powered applications
- Small SOP8 package

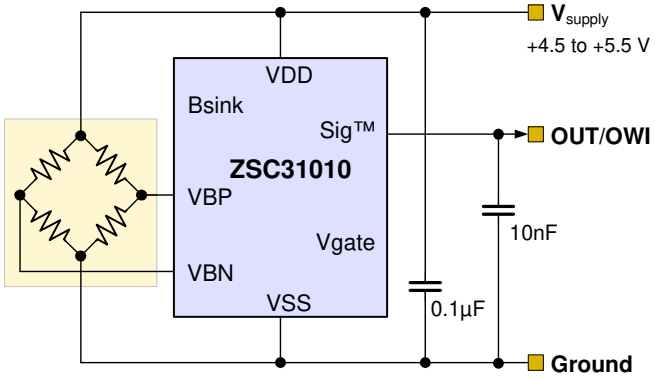
Available Support

- Development Kit available
- Mass Calibration Kit available
- Support for industrial mass calibration available
- Quick circuit customization possible for large production volumes

Physical Characteristics

- Supply voltage 2.7 to 5.5 V, with external JFET 5.5V to 30 V
- Current consumption depending on adjusted sample rate: 0.25 mA to 1 mA
- Wide operational temperature: –50 to +150°C

ZSC31010 Application Circuit – Digital Output

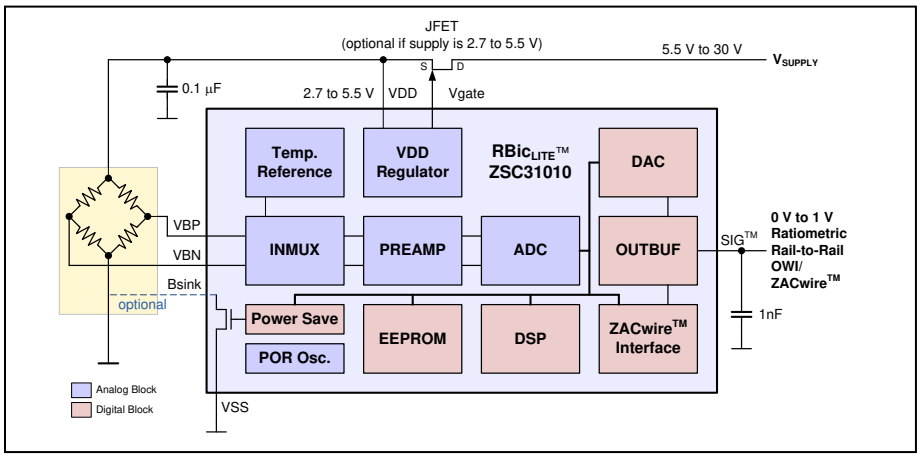


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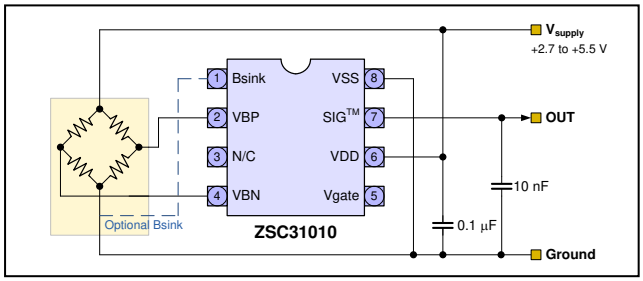
ZSC31010 Block Diagram

Highly Versatile Applications in Many Markets Including

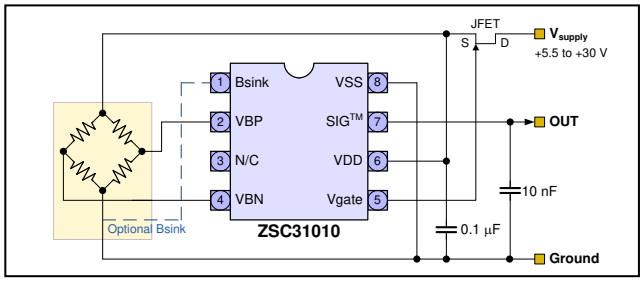
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- *Office Automation*
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- *Automotive*
- *Portable Devices*
- *Your Innovative Designs*



Rail-to-Rail Ratiometric Voltage Output Applications



Absolute Analog Voltage Output Applications



Ordering Examples *(Please see section 11 in the data sheet for additional options.)*

Sales Code	Description	Package
ZSC31010CEB	ZSC31010 Die — Temperature range: -50°C to +150°C	Unsawn on Wafer
ZSC31010CEC	ZSC31010 Die — Temperature range: -50°C to +150°C	Sawn on Wafer Frame
ZSC31010CEG1	ZSC31010 SOP8 (150 mil) — Temperature range: -50°C to +150°C	Tube: add “-T” to sales code Reel: add “-R”
ZSC31010KIT	ZSC31010 ZACwire™ SSC Evaluation Kit: Communication Board, SSC Board, Sensor Replacement Board, USB Cable, 5 IC Samples	Kit

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1 Electrical Characteristics

1.1. Absolute Maximum Ratings

Note: The absolute maximum ratings are stress ratings only. The device might not function or be operable above the operating conditions given in section 1.2. Stresses exceeding the absolute maximum ratings might also damage the device. In addition, extended exposure to stresses above the recommended operating conditions might affect device reliability. IDT does not recommend designing to the “Absolute Maximum Ratings.”

Parameter	Symbol	Conditions	Min	Max	Unit
Analog Supply Voltage	V_{DD}		-0.3	6.0	V
Voltages at Analog I/O – In Pin	V_{INA}		-0.3	VDD+0.3	V
Voltages at Analog I/O – Out Pin	V_{OUTA}		-0.3	VDD+0.3	V
Storage Temperature Range	T_{STG}		-50	150	°C
Storage Temperature Range	$T_{STG <10h}$	For periods < 10 hours	-50	170	°C

Note: Also see Table 6.1 regarding soldering temperature and storage conditions for the SOP-8 package.

1.2. Recommended Operating Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Analog Supply Voltage to Ground	V_{DD}		2.7	5.0	5.5	V
Analog Supply Voltage (with external JFET Regulator)	V_{SUPP}		5.5	7	30	V
Common Mode Voltage	V_{CM}		1		V_{DDA} - 1.3	V
Ambient Temperature Range [1, 2)]	T_{AMB}		-50		150	°C
External Capacitance between V_{DD} and Ground	C_{VDD}		100	220	470	nF
Output Load Resistance to V_{DD}	$R_{L,OUT}$		2.5	10		kΩ
Output Load Resistance to V_{SS} [3) 4)]	$R_{L,OUT}$		2.5	20		kΩ
Output Load Capacitance [5)]	$C_{L,OUT}$		1	10	15	nF
Bridge Resistance [6)]	R_{BR}		0.2		100	kΩ
Power ON Rise Time	t_{PON}				100	ms

1) Note that the maximum EEPROM programming temperature is 85°C.

2) If buying die, designers should use caution not to exceed maximum junction temperature by proper package selection.

3) When using the output for digital calibration, no pull down resistor is allowed.

4) For loads less than 20 kΩ to VSS an equivalent strength (or lower) pull-up resistor must be added.

5) Using the output for digital calibration, $C_{L,OUT}$ is limited by the maximum rise time $T_{ZAC,rise}$.

6) Note: Minimum bridge resistance is only a factor if using the Bsink feature. The nominal R_{DS}(ON) of the Bsink transistor is 10 Ω when operating at V_{DD} = 5 V, and 15 Ω when operating at V_{DD} = 3.0 V. This does give rise to a ratiometricity inaccuracy that becomes greater with low bridge resistances.

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1.3. Electrical Parameters

See important table notes at the end of the table. Note: For parameters marked with an asterisk, there is no verification in mass production; the parameter is guaranteed by design and/or quality observation.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
1.3.1. Supply/Regulation Characteristics						
Supply Voltage	V_{DD}		2.7	5.0	5.5	V
Supply Current (varies with update rate and output mode)	I_{DD}	At minimum update rate		0.25		mA
		At maximum update rate		1.0	1.2	
Temperature Coefficient – Regulator (worst case) *	TC_{REG}	Tem. -10°C to 120°C			35	ppm/K
		Temp. < -10°C and > 120°C			100	
Power Supply Rejection Ratio *	PSRR	DC < 100 Hz (JFET regulation loop using mmbf4392 and 0.1 µF decoupling cap)	60			dB
		AC < 100 kHz (JFET regulation loop using mmbf4392 and 0.1 µF decoupling cap)	45			dB
Power-On Reset Level	POR		1.4		2.6	V
1.3.2. Analog Front-End (AFE) Characteristics						
Leakage Current Pin VBP,VBN	I_{IN_LEAK}				±10	nA
1.3.3. EEPROM Parameters						
Number Write Cycles	n_{WRI_EEP}	At 150°C At 85°C			100 100k	Cycles
Data Retention	t_{WRI_EEP}	At 100°C			10	Years
1.3.4. A/D Converter Characteristics						
ADC Resolution	r_{ADC}			14		Bit
Integral Nonlinearity (INL) [1)]	INL_{ADC}		-4		+4	LSB
Differential Nonlinearity (DNL) *	DNL_{ADC}		-1		+1	LSB
Response Time	$T_{RES,ADC}$	Varies with update rate. Value given at fastest rate.		1		ms
1.3.5. Analog Output (DAC and Buffer) Characteristics						
Max. Output Current	I_{OUT}	Max. current maintaining accuracy	2.2			mA
Resolution	r_{OUT}	Referenced to V_{DD}			11	Bit
Absolute Error	E_{ABS}	DAC input to output	-10		+10	mV
Differential Nonlinearity *	DNL	No missing codes	-0.9		+1.5	LSB_{11Bit}
Upper Output Voltage Limit	V_{OUT}	R_L = 2.5 kΩ	95%			V_{DD}
Lower Output Voltage Limit	V_{OUT}				16.5	mV

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Parameter	Symbol	Conditions	Min	Typ	Max	Unit
1.3.6. ZACwire™ Serial Interface						
ZACwire™ Line Resistance *	$R_{ZAC,line}$	The rise time $T_{ZAC,rise}$ must be $2 * R_{ZAC,line} * C_{ZACload} \leq 5\mu s$. If using a pull-up resistor instead of a line resistor, it must meet this specification.			3.9	kΩ
ZACwire™ Load Capacitance *	$C_{ZAC,load}$		0	1	15	nF
ZACwire™ Rise Time *	$T_{ZAC,rise}$				5	µs
Voltage Level Low *	$V_{ZAC,low}$			0	0.2	V_{DD}
Voltage Level High *	$V_{ZAC,low}$		0.8	1		V_{DD}
1.3.7. System Response Characteristics						
Start-Up-Time	t_{STA}	Power-up to output			10	ms
Response Time	t_{RESP}	Update_rate = 1 kHz (1 ms)		1	2	ms
Sampling Rate	f_S	Update_rate = 1 kHz (1 ms)		1000		Hz
Overall Linearity Error	E_{LIND}	Bridge input to output – Digital		0.025	0.04	%
Overall Linearity Error	E_{LINA}	Bridge input to output – Analog		0.1	0.2	%
Overall Ratiometricity Error	RE_{out}	±10%VDD, not using Bsink feature			0.035	%
Overall Accuracy – Digital (only IC, without sensor bridge)	AC_{outD}	-25°C to 85°C			±0.1%	%FSO
		-50°C to 150°C			±0.25%	
Overall Accuracy – Analog (only IC, without sensor bridge) [2), 3)]	AC_{outA}	-25°C to 85°C			±0.25%	%FSO
		-40°C to 125°C			±0.35%	
		-50°C to 150°C			±0.5%	

[1)] Note: This is ± 4 LSBs to the 14-bit A-to-D conversion. This implies absolute accuracy to 12 bits on the A-to-D result. Non-linearity is typically better at temperatures less than 125°C.

[2)] Not included is the quantization noise of the DAC. The 11-bit DAC has a quantization noise of ± ½ LSB = 1.22 mV (5V VDD) = 0.025%

[3)] Analog output range 2.5% to 95%.

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1.4. Analog Inputs versus Output Resolution

The ZSC31010 incorporates an extended 14-bit charge-balanced ADC, which allows for a single gain setting on the pre-amplifier to handle bridge sensitivities from 1.2 to 36 mV/V while maintaining 8 to 12 bits of output resolution with a default analog gain of 24. Selectable gain settings allow accommodating bridges with different sensitivities. The tables below illustrate the minimum resolution achievable for a variety of bridge sensitivities. The yellow shadowed fields indicate that for these input spans with the selected analog gain setting, the quantization noise is higher than 0.1% FSO.

Table 1.1 ADC Resolution Characteristics for an Analog Gain of 6

Analog Gain 6				
Input Span [mV/V]			Allowed Offset (+/- % of Span) [1]	Minimum Guaranteed Resolution [Bits]
Min	Typ	Max		
57.3	80.0	105.8	38%	13.3
50.6	70.0	92.6	53%	13.1
43.4	60.0	79.4	73%	12.9
36.1	50.0	66.1	101%	12.6
28.9	40.0	52.9	142%	12.3
21.7	30.0	39.7	212%	11.9

[1] In addition to Tco, Tcg

Table 1.2 ADC Resolution Characteristics for an Analog Gain of 12

Analog Gain 12				
Input Span [mV/V]			Allowed Offset (+/- % of Span) [1]	Minimum Guaranteed Resolution [Bits]
Min	Typ	Max		
43.3	60.0	79.3	3%	13.0
36.1	50.0	66.1	17%	12.7
25.3	35.0	46.3	53%	12.2
18.0	25.0	33.0	101%	11.7
14.5	20.0	26.45	142%	11.4
7.2	10.0	13.22	351%	10.4
3.6	5.0	6.6	767%	9.4

[1] In addition to Tco, Tcg

Note: Yellow shadowing indicates that for these input spans with the selected analog gain setting, the quantization noise is > 0.1% FSO.

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Table 1.3 ADC Resolution Characteristics for an Analog Gain of 24

Analog Gain 24				
Input Span [mV/V]			Allowed Offset (+/- % of Span) [1]	Minimum Guaranteed Resolution [Bits]
Min	Typ	Max		
16	25.0	36	25%	12.6
12.8	20.0	28.8	50%	12
6.4	10.0	14.4	150%	11
3.2	5.0	7.2	400%	10
1.6	2.5	3.6	900%	9
0.8	1.2	1.7	2000%	8

[1] In addition to Tco,Tcg

Note: Yellow shadowing indicates that for these input spans with the selected analog gain setting, the quantization noise is > 0.1% FSO.

Table 1.4 ADC Resolution Characteristics for an Analog Gain of 48

Analog Gain 48				
Input Span [mV/V]			Allowed Offset (+/- % of Span) [1]	Minimum Guaranteed Resolution [Bits]
Min	Typ	Max		
10.8	15.0	19.8	3%	13
7.2	10.0	13.2	35%	12.4
4.3	6.0	7.9	100%	11.7
2.9	4.0	5.3	190%	11.1
1.8	2.5	3.3	350%	10.4
1.0	1.4	1.85	675%	9.6
0.72	1.0	1.32	975%	9.1

[1] In addition to Tco,Tcg

Note: Yellow shadowing indicates that for these input spans with the selected analog gain setting, the quantization noise is > 0.1% FSO.

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2 Circuit Description

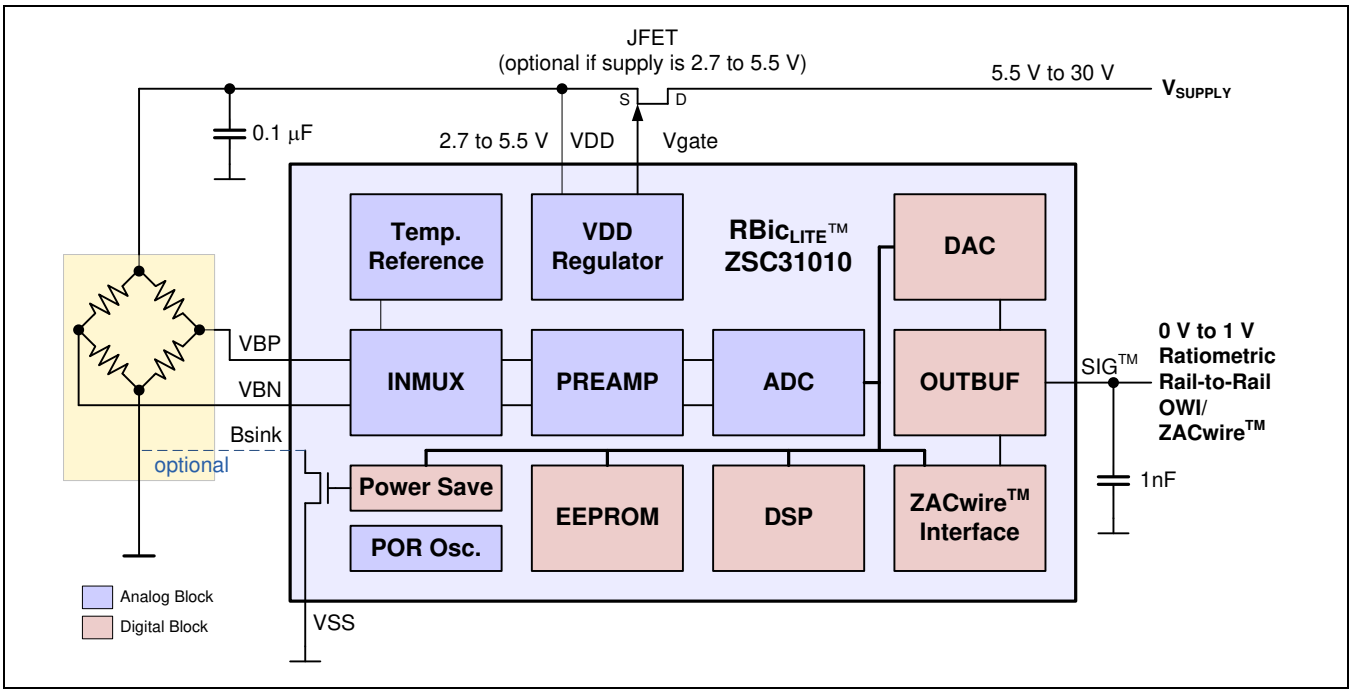
2.1. Signal Flow and Block Diagram

The ZSC31010 resistive bridge sensor interface ICs were specifically designed as a cost-effective solution for sensing in building automation, industrial, office automation, and white goods applications. The RBic$_{Lite}$™ employs IDT's high precision bandgap with proportional-to-absolute temperature (PTAT) output; a low-power 14-bit analog-to-digital converter (ADC, A2D, A-to-D); and an on-chip DSP core with EEPROM to precisely calibrate the bridge output signal. Three selectable output modes, two analog and one digital, offer the ultimate in versatility across many applications.

The ZSC31010 rail-to-rail ratiometric analog output Vout signal (0 to 5 V, Vout @ VDD = 5 V) suits most building automation and automotive requirements. Typical office automation and white goods applications require the 0 to 1 Vout signal, which in the ZSC31010 is referenced to the internal bandgap. Direct interfacing to microprocessor controllers is facilitated via IDT's single-wire serial ZACwire™ digital interface.

The ZSC31010 is capable of running in high-voltage (5.5 to 30 V) systems when combined with an external JFET.

Figure 2.1 ZSC31010 Block Diagram



2.2. Analog Front End

2.2.1. Bandgap/PTAT and PTAT Amplifier

The highly linear Bandgap/PTAT provides the PTAT signal to the ADC, which allows accurate temperature conversion. In addition, the ultra-low ppm-Bandgap provides a stable voltage reference over temperature for the operation of the rest of the IC.

The PTAT signal is amplified through a path in the pre-amplifier (PREAMP) and fed to the ADC for conversion. The most significant 12 bits of this converted result are used for temperature measurement and temperature correction of bridge readings. When temperature is output in Digital Mode, only the most significant 8 bits are given.

2.2.2. Bridge Supply

The voltage driven bridge is usually connected to V_{DD} and ground. As a power savings feature, the ZSC31010 also includes a switched transistor to interrupt the bridge current via the Bsink pin. The transistor switching is synchronized to the A/D-conversion and released after finishing the conversion. To utilize this feature, the low supply of the bridge should be connected to Bsink instead of ground.

Depending on the programmable update rate, the average current consumption (including bridge current) can be reduced to approximately 20%, 5% or 1%.

2.2.3. PREAMP Block

The differential signal from the bridge is amplified through a chopper-stabilized instrumentation amplifier with very high input impedance, designed for low noise and low drift. This PREAMP provides gain for the differential signal and re-centers its DC to $V_{DD}/2$. The output of the PREAMP block is fed into the A/D-converter. The calibration sequence performed by the digital core includes an auto-zero sequence to null any drift in the PREAMP state over temperature.

The PREAMP is nominally set to a gain of 24. Other possible gain settings are 6, 12, and 48.

The inputs to the PREAMP from the VBN/VBP pins can be reversed via an EEPROM configuration bit.

2.2.4. Analog-to-Digital Converter (ADC)

A 14-bit/1 ms 2^{nd}-order charge-balancing ADC is used to convert signals coming from the PREAMP. The converter, designed in full differential switched-capacitor technique, is used for converting the various signals to the digital domain. This principle offers the following advantages:

- High noise immunity because of the differential signal path and integrating behavior
- Independent from clock frequency drift and clock jitter
- Fast conversion time owing to second order mode

Four selectable values for the zero point of the input voltage allow the conversion to adapt to the sensor's offset parameter. The conversion rate varies with the programmed update rate. The fastest conversion rate is 1 k samples/s; the response time is then 1 ms. Based on a best fit, the Integral Nonlinearity (INL) is < 4 LSB_{14Bit}.

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2.3. Digital Signal Processor

A digital signal processor (DSP) is used for processing the converted bridge data as well as for performing temperature correction and for computing the temperature value for output on the digital channel.

The DSP reads correction coefficients from the EEPROM and can correct for

- Bridge Offset
- Bridge Gain
- Variation of Bridge Offset over Temperature (Tco)
- Variation of Bridge Gain over Temperature (Tcg)
- A Single Second Order Effect (SOT - Second Order Term)

The EEPROM contains a single SOT that can be applied to correct one and only one of the following:

- 2^{nd} order behavior of bridge measurement
- 2^{nd} order behavior of Tco
- 2^{nd} order behavior of Tcg

(For more details, see section 3.6.1.)

If the SOT applies to correcting the bridge reading, then the correction formula for the bridge reading is represented as a two step process as follows:

$$ZB = Gain_B(1 + \Delta T * Tcg) * (BR_Raw + Offset_B + \Delta T * Tco) \quad (1)$$

$$BR = ZB(1.25 + SOT * ZB) \quad (2)$$

Where:

BR	= Corrected Bridge reading that is fed as digital or analog output on Sig™ pin
ZB	= Intermediate result in the calculations
BR_Raw	= Raw Bridge reading from ADC
T_Raw	= Raw Temperature reading converted from PTAT signal
Gain_B	= Bridge gain term
Offset_B	= Bridge offset term
Tcg	= Temperature coefficient gain
Tco	= Temperature coefficient offset
ΔT	= (T_Raw - T_{SETL})
T_Raw	= Raw Temperature reading converted from PTAT signal
T_{SETL}	= Raw PTAT reference value (See *Technical Note—ZSC31010, ZSC31015, and ZSSC3015 Calibration Sequence, DLL, and EXE* for details.*)*
SOT	= Second Order Term

Note: See section 3.6.2.7 for limitations when SOT applies to the bridge reading.

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If the **SOT** applies to correcting the 2nd order behavior of **Tco**, then the formula for bridge correction is as follows:

$$BR = Gain_B(1 + \Delta T * Tcg) * [BR_Raw + Offset_B + \Delta T(SOT * \Delta T + Tco)] \quad (3)$$

Note: See section 3.6.2.7 for limitations when SOT applies to Tco.

If the SOT applies to correcting the 2nd order behavior of Tcg, then the formula for bridge correction is as follows:

$$BR = Gain_B[1 + \Delta T(SOT * \Delta T + Tcg)] * [BR_Raw + Offset_B + \Delta T * Tco] \quad (4)$$

The bandgap reference gives a very linear PTAT signal, so temperature correction can always simply be accomplished with a linear gain and offset term.

Corrected Temp Reading:

$$T = Gain_T(T_Raw + Offset_T) \quad (5)$$

Where:

T_Raw = Raw Temperature reading converted from PTAT signal

Offset_T = Temperature sensor offset coefficient

Gain_T = Temperature gain coefficient

2.3.1. EEPROM

The EEPROM contains the calibration coefficients for gain and offset, etc., and the configuration bits, such as output mode, update rate, etc. When programming the EEPROM, an internal charge-pump voltage is used, so a high voltage supply is not needed. The EEPROM is implemented as a shift register. During an EEPROM read, the contents are shifted 8 bits before each transmission of one byte occurs.

The charge-pump is internally regulated to 12.5 V, and the programming time is typically 6 ms.

Note: EEPROM writing can only be performed at temperatures lower than 85°C.

2.3.2. One-Wire Interface—ZACwire™

The IC communicates via a One-Wire Serial Interface (OWI, ZACwire™). There are different commands available for the following:

- Reading the conversion result of the ADC (Get_BR_Raw, Get_T_Raw)
- Calibration commands
- Reading from the EEPROM (dump of entire contents)
- Writing to the EEPROM (trim setting, configuration, and coefficients)

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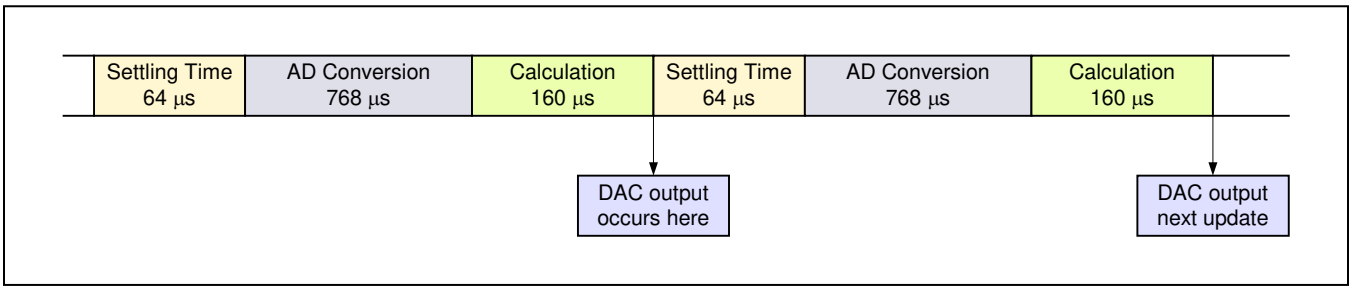
2.4. Output Stage

2.4.1. Digital to Analog Converter (Output DAC)

An 11-bit DAC, based on sub-ranging resistor strings, is used for the digital-to-analog output conversion in the analog ratiometric and absolute analog voltage modes. Selection during calibration configures the system to operate in either of these modes. The design allows for excellent testability as well as low power consumption.

Figure 2.2 shows the data timing of the DAC output with the 1 kHz update rate setting.

Figure 2.2 DAC Output Timing for Highest Update Rate



2.4.2. Output Buffer

A rail-to-rail operational amplifier (OpAmp) configured as a unity gain buffer can drive resistive loads (whether pull-up or pull-down) as low as 2.5 kΩ and capacitances up to 15 nF. To limit the error due to amplifier offset voltage, an error compensation circuit is included which tracks and reduces the offset voltage to < 1 mV.

2.4.3. Voltage Reference Block

A linear regulator control circuit is included in the Voltage Reference Block to interface with an external JFET to allow operation in systems where the supply voltage exceeds 5.5 V. This circuit can also be used for over-voltage protection. The regulator set point has a coarse adjustment via an EEPROM bit (see section 2.3.1), which can adjust the set point around 5.0 V or 5.5 V. In addition, the 1 V trim setting (see below) can also act as a fine adjustment for the regulation set point.

Note: If using the external JFET for over-voltage protection purposes (i.e., 5 V at JFET drain and expecting 5 V at JFET source), there will be a voltage drop across the JFET; therefore ratiometricity will be compromised somewhat depending on the rds(on) of the chosen JFET. A Vishay J107 is the best choice, because it has only an 8 mV drop worst case. If using as regulation instead of over-voltage, an MMBF4392 also works well.

The Voltage Reference Block uses the absolute reference voltage provided by the Bandgap to produce two regulated on-chip voltage references. A 1 V reference is used for the output DAC high reference, when the part is configured for 0 to 1 V analog output. For this reason, the 1 V reference must be very accurate and includes trim, such that its value can be trimmed within +/-3 mV of 1.0 V. The 1 V reference is also used as the on-chip reference for the JFET regulator block, so the regulation set point of the JFET regulator can be fine-tuned, using the 1 V trim. The 5 V reference can be trimmed within +/-15 mV. Table 2.1 shows the order of trim codes with 0111_B for the lowest reference voltage, and 1000_B for the highest reference voltage.

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Table 2.1 Order of Trim Codes

Order	1Vref/5Vref__trim3	1Vref/5Vref_trim2	1Vref/5Vref_trim1	1Vref/5Vref_trim0
Highest Reference Voltage	1	0	0	0
...	1	0	0	1
...	1	0	1	0
...	1	0	1	1
...	1	1	0	0
...	1	1	0	1
...	1	1	1	0
...	1	1	1	1
...	0	0	0	0
...	0	0	0	1
...	0	0	1	0
...	0	0	1	1
...	0	1	0	0
...	0	1	0	1
...	0	1	1	0
Lowest Reference Voltage	0	1	1	1

2.5. Clock Generator / Power-On Reset (CLKPOR)

If the power supply exceeds 2.5 V (maximum), the reset signal de-asserts, and the clock generator starts operating at a frequency of approximately 512 kHz (+17% / -22%). The exact value only influences the conversion cycle time and the communication to the outside world, but not the accuracy of signal processing. In addition, to minimize the oscillator error as the V_{DD} voltage changes, an on-chip regulator is used to supply the oscillator block.

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2.5.1. Trimming the Oscillator

Trimming is performed at wafer level, and it is strongly recommended that this is not to be changed during calibration, because ZACwire™ communication is no longer guaranteed at different oscillator frequencies.

Table 2.2 Oscillator Trimming

Trimming Bits	Delta Frequency (kHz)
100	+385
101	+235
110	+140
111	+65
000	Nominal
001	-40
010	-76
011	-110

Example: Programming $011_B \rightarrow$ the trimmed frequency = nominal value - 110 kHz.

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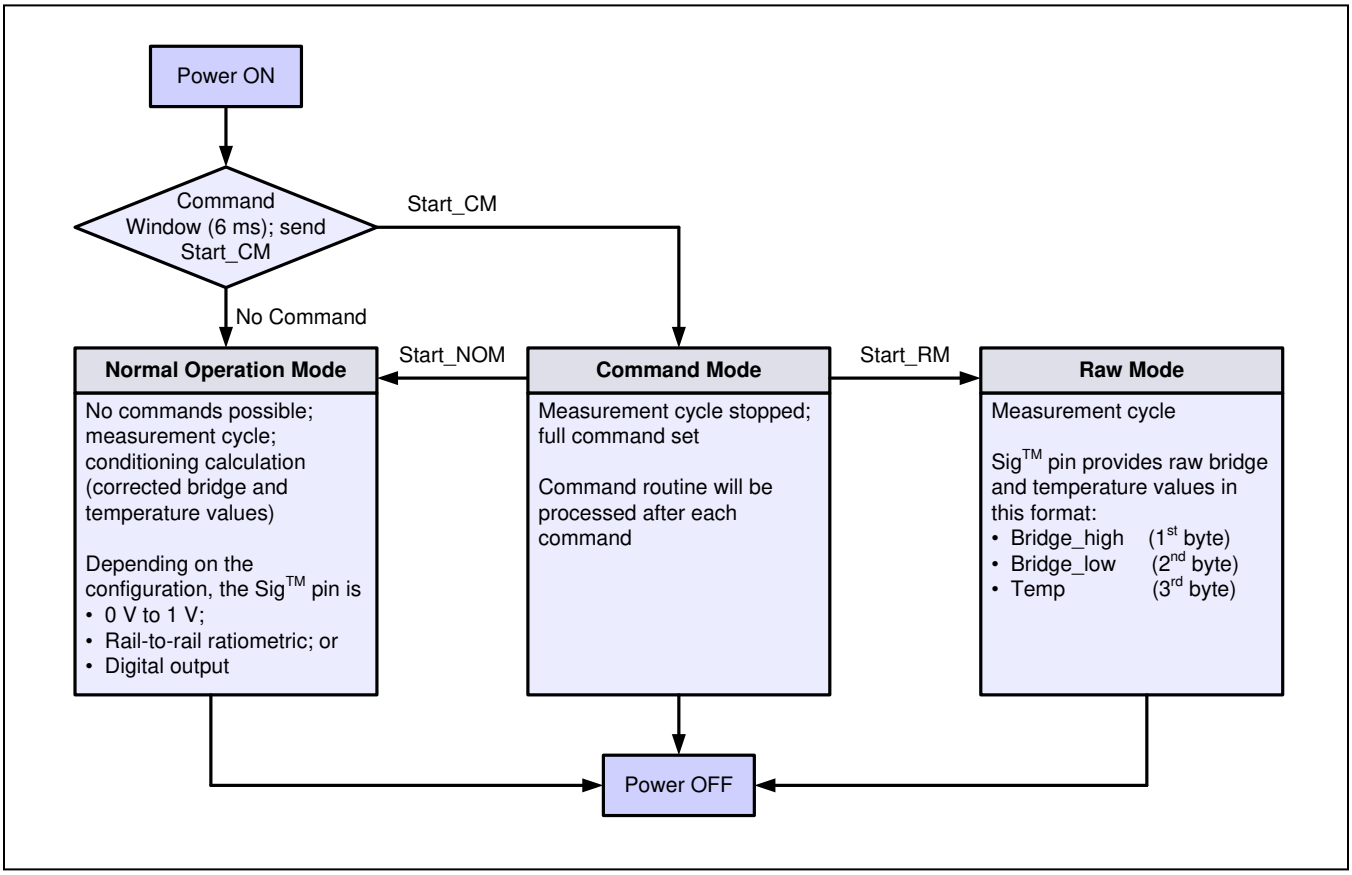
3 Functional Description

3.1. General Working Mode

The command/data transfer takes place via the one-wire Sig™ pin, using the ZACwire™ serial communication protocol. After power-on, the IC waits for 6 ms (i.e., the command window) for the Start_CM command. Without this command, the Normal Operation Mode (NOM) starts. In this mode, raw bridge values are converted, and the corrected values are presented on the output in analog or digital format (depending on the configuration stored in EEPROM).

Command Mode (CM) can only be entered during the 6 ms command window after power-on. If the IC receives the Start_CM command during the command window, it remains in the Command Mode. The CM allows changing to one of the other modes via command. After command Start_RM, the IC is in the Raw Mode (RM). Without correction, the raw values are transmitted to the digital output in a predefined order. The RM can only be stopped by power-off. Raw Mode is used by the calibration software for collection of raw bridge and temperature data, so the correction coefficients can be calculated.

Figure 3.1 General Working Mode



3.2. ZACwire™ Communication Interface

3.2.1. Properties and Parameters

Table 3.1 Pin Configuration and Latch-Up Conditions

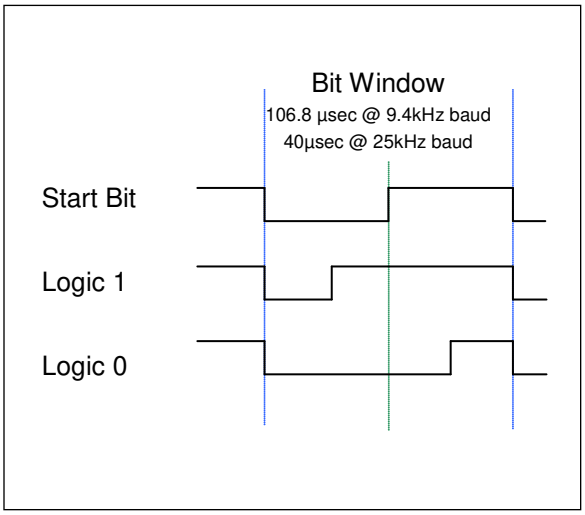
No.	Parameter	Symbol	Min	Typ	Max	Unit	Comments
1	Pull-up resistor (on-chip)	$R_{ZAC,pu}$		30		kΩ	On-chip pull-up resistor switched on during Digital Output Mode and during CM Mode (first 6 ms after power up)
2	Pull-up resistor (external)	R_{ZAC,pu_ext}	150			Ω	If the master communicates via a push-pull stage, no pull-up resistor is needed; otherwise, a pull-up resistor with a value of at least 150 Ω must be connected.
3	ZACwire™ rise time	$T_{ZAC,rise}$			5	µs	Any user RC network included in Sig™ path must meet this rise time
4	ZACwire™ line resistance [1)]	$R_{ZAC,line}$			3.9	kΩ	Also see section 1.3.6 in the specification tables.
5	ZACwire™ load capacitance[1)]	$C_{ZAC,load}$	0	1	15	nF	Also see section 1.3.6 in the specification tables.
6	Voltage low level	$V_{ZAC,low}$		0	0.2	V_{DD}	Rail-to-rail CMOS driver
7	Voltage high level	$V_{ZAC,high}$	0.8	1		V_{DD}	Rail-to-rail CMOS driver

1) The rise time must be $T_{ZAC,rise} = 2 * R_{ZAC,line} * C_{ZACload} \leq 5$ µs . If using a pull-up resistor instead of a line resistor, it must meet this specification.

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3.2.2. Bit Encoding

Figure 3.2 Manchester Duty Cycle



Start bit = 50% duty cycle used to set up strobe time

Logic 1 = 75% duty cycle

Logic 0 = 25% duty cycle

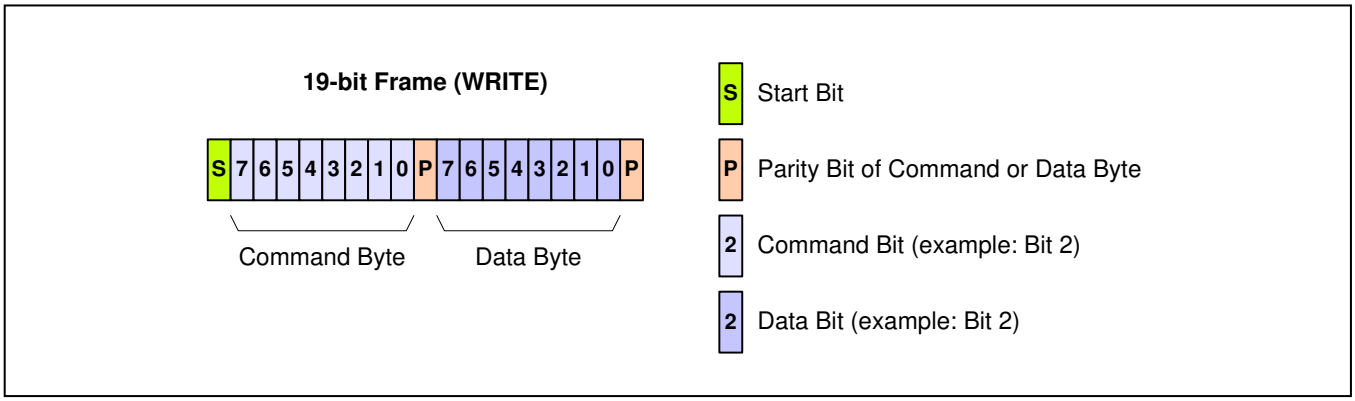
Stop Time

The ZACWire™ bus will be held high for 32 µs (nominal) between consecutive data packets regardless of baud rate.

3.2.3. Write Operation from Master to ZSC31010

The calibration master sends a 19-bit packet frame to the ZSC31010.

Figure 3.3 19-Bit Write Frame



The incoming serial signal will be sampled at a 512 kHz clock rate. This protocol is very tolerant to clock skew and can easily tolerate baud rates in the 6 kHz to 48 kHz range.

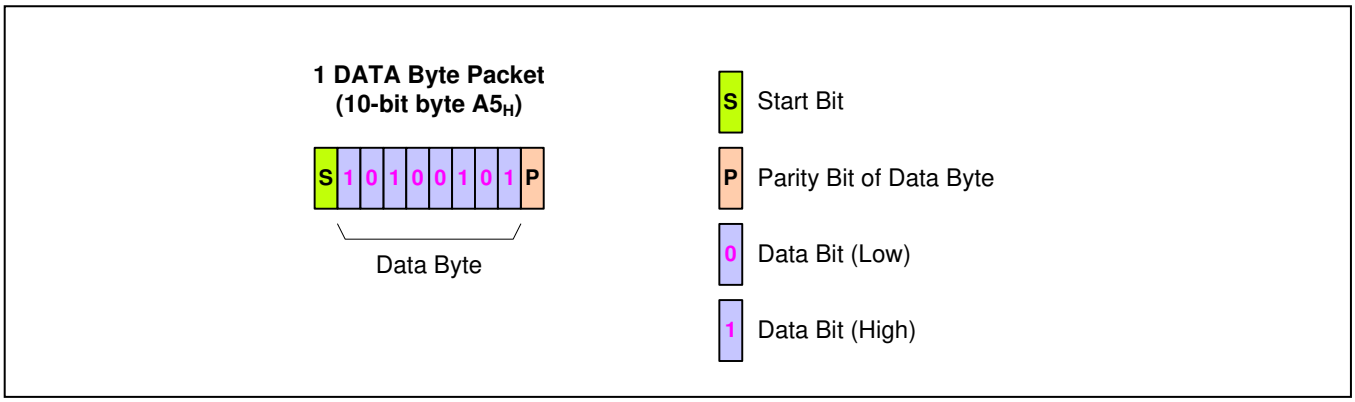
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3.2.4. ZSC31010 Read Operations

The incoming frame will be checked for proper parity on both, command and data bytes, as well as for any edge time-outs prior to a full frame being received.

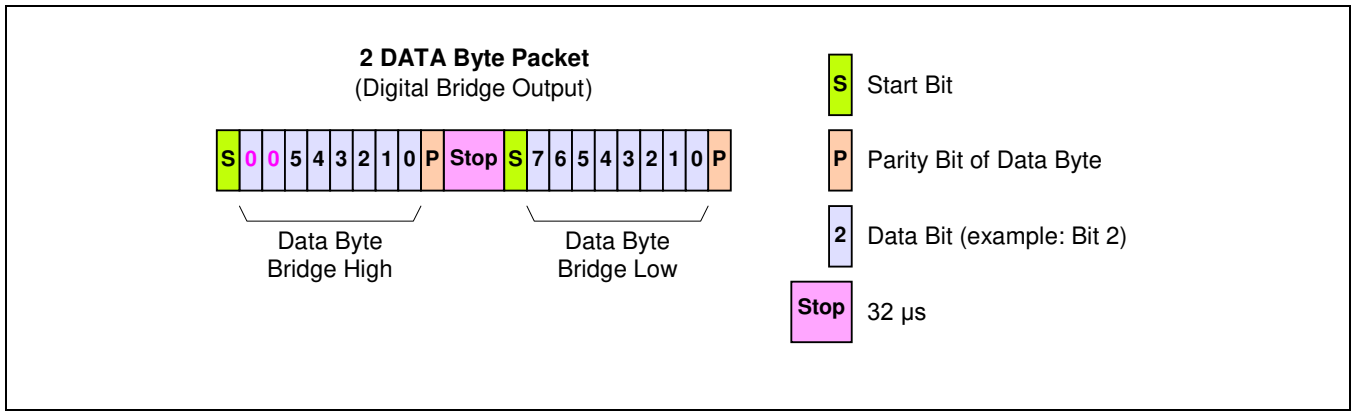
Once a command/data pair is received, the ZSC31010 will perform that command. After the command has been successfully executed by the IC, the IC will acknowledge success by a transmission of an $A5_H$-byte back to the master. If the master does not receive an $A5_H$ transmission within 130 ms of issuing the command, it must assume the command was either improperly received or could not be executed.

Figure 3.4 Read Acknowledge



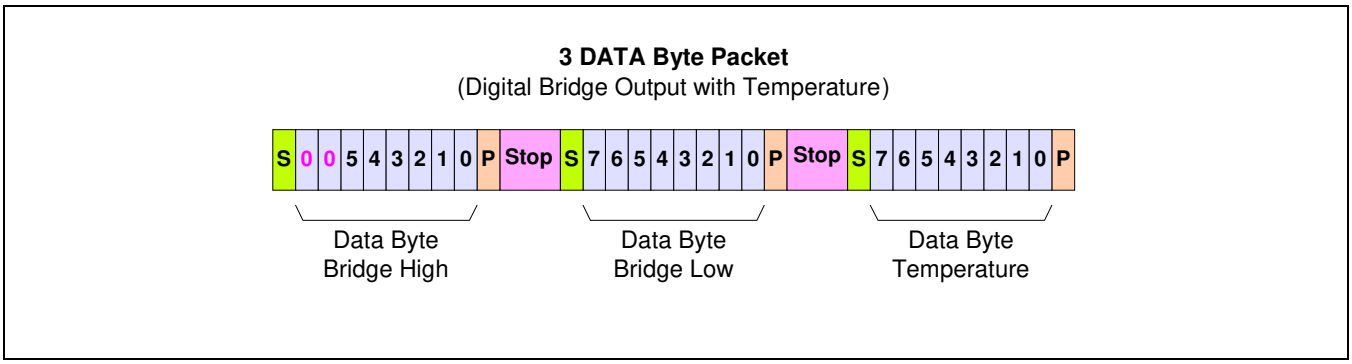
The ZSC31010 transmits 10-bit bytes (1 start bit, 8 data bits, 1 parity bit). During calibration and configuration, transmissions are normally either $A5_H$ or data. $A5_H$ indicates successful completion of a command. There are two different digital output modes configurable (digital output with temperature, and digital output with only bridge data). During Normal Operation Mode, if the part is configured for digital output of the bridge reading, it first transmits the high byte of bridge data, followed by the low byte. The bridge data is 14 bits in resolution, so the upper two bits of the high byte are always zero-padded. There is a 32 µs stop time when the bus is held high between bytes in a packet.

Figure 3.5 Digital Output (NOM) Bridge Readings



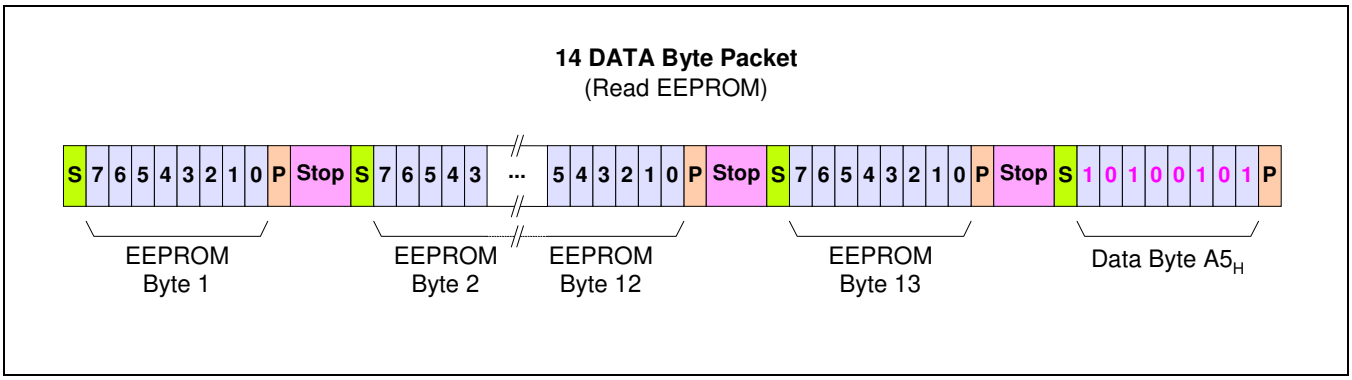
The second digital output mode is digital output bridge reading with temperature. It will be transmitted as a 3-data-byte packet. The temperature byte represents an 8-bit temperature quantity, spanning from -50 to 150°C.

Figure 3.6 Digital Output (NOM) Bridge Readings with Temperature



The EEPROM transmission occurs in a packet with 14 data bytes, as shown below.

Figure 3.7 Read EEPROM Contents



There is a variable idle time between packets, which varies with the update rate setting in the EEPROM.

Figure 3.8 Transmission of a Number of Data Packets

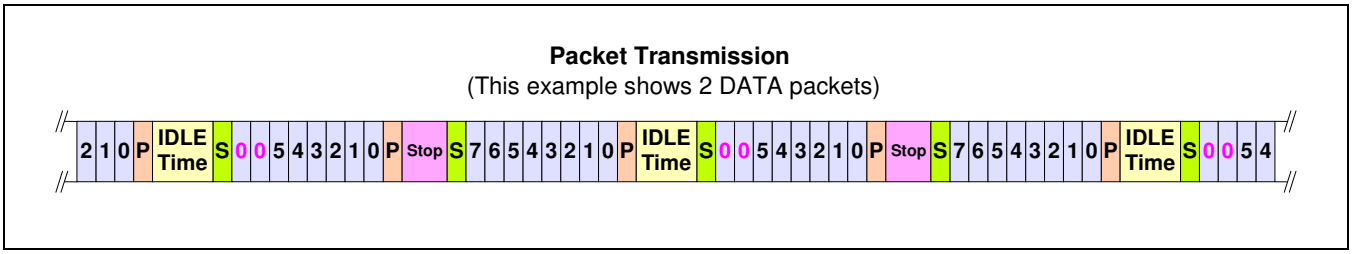


Table 3.2 shows the idle time between packets versus the update rate. This idle time can vary by nominal +/-15% between parts, and over a temperature range of -50 to 150ºC.

Transmissions from the IC occur at one of two speeds depending on the update rate programmed in EEPROM. If the user chooses one of the two fastest update rates (1 ms or 5 ms) then the baud rate of the digital transmission will be 32 kHz (minimum 25 kHz). If, however, the user chooses one of the two slower update rates (25 ms or 125 ms), then the baud rate of the digital transmission will be 8 kHz (maximum 9.4 kHz).

The total transmission time for both digital output configurations is shown in Table 3.2.

Table 3.2 Total Transmission Time for Different Update Rate Settings and Output Configuration

Update Rate	Baud Rate*	Idle Time	Transmission Time – Bridge Only Readings			Transmission Time – Bridge & Temperature Readings		
1 ms (1 kHz)	32 kHz	1.0 ms	20.5 bits	31.30 µs	1.64 ms	31.0 bits	31.30 µs	1.97 ms
5 ms (200 Hz)	32 kHz	4.85 ms	20.5 bits	31.30 µs	5.49 ms	31.0 bits	31.30 µs	5.82 ms
25 ms (40 Hz)	8 kHz	22.5 ms	20.5 bits	125.00 µs	25.06 ms	31.0 bits	125.00 µs	26.38 ms
125 ms (8 Hz)	8 kHz	118.0 ms	20.5 bits	125.00 µs	120.56 ms	31.0 bits	125.00 µs	121.88 ms
* Typical values. Minimum baud rate for 1 ms or 5 ms: 26kHz; maximum baud rate for 25 ms or 125 ms: 9.4kHz.								

The temperature raw reading is performed less often than a bridge reading, because the temperature changes more slowly.

Table 3.3 shows the timing for the special measurements (temperature and bridge measurement) in the different update rate modes.

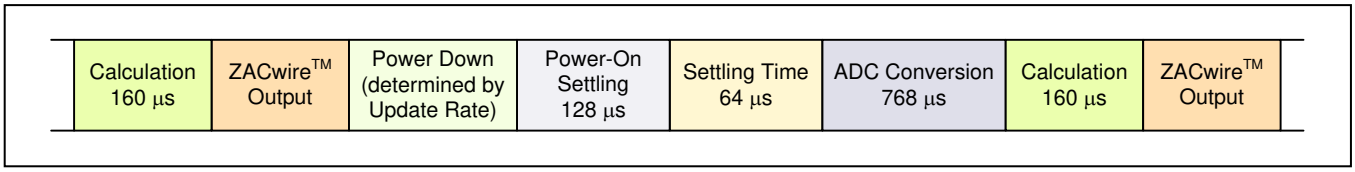
Table 3.3 Special Measurement versus Update Rate

Update Rate Setting	Special Measurement
00	Every 128 bridge measurements
01	Every 64 bridge measurements
10	Every 16 bridge measurements
11	Every 8 bridge measurements

It is easy to program any standard microcontroller to communicate with the ZSC31010. IDT can provide sample code for a MicroChip® PIC microcontroller.

For update rates less than 1 kHz, the output is followed by a power-down, as shown below.

Figure 3.9 ZACwire™ Output Timing for Lower Update Rates



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3.2.5. High Level Protocol

The ZSC31010 will listen for a command/data pair to be transmitted for the 6 ms after the de-assertion of its internal Power-On Reset (POR). If a transmission is not received within this time frame, then it will transition to Normal Operation Mode (NOM). In NOM, it will output bridge data in 0 to 1 V analog, rail-to-rail ratiometric analog output, or digital output, depending on how the part is currently configured.

If the ZSC31010 receives a Start CM command within the first 6 ms after the de-assertion of POR, then it will go into Command Mode (CM). In this mode, calibration/configuration commands will be executed. The ZSC31010 will acknowledge successful execution of commands by transmission of an $A5_H$. The calibrating/ configuring master will know that a command was not successfully executed if no response is received after 130 ms of issuing the command. Once in command interpreting/executing mode, the ZSC31010 will stay in this mode until power is removed, or a Start NOM (Start Normal Operation Mode) command is received. The Start CM command is used as an interlock mechanism, to prevent a spurious entry into command mode on power-up. The first command received within the 6 ms window of POR must be a Start CM command to enter into command interpreting mode. Any other commands will be ignored.

3.3. Command/Data Bytes Encoding

The 16-bit command/data stream sent to the ZSC31010 can be broken into 2 bytes, shown in Table 3.4. The most significant byte encodes the command byte. The least significant byte represents the data byte.

Table 3.4 Command/Data Bytes Encoding

Command Byte	Data Byte	Description
00_H	XX_H	Read EEPROM command via Sig™ pin; for more details, refer to section 3.7.
20_H	$5X_H$	Enter Test Mode (subset of Command Mode for test purposes only): Sig™ pin will assume the value of different internal test points depending on the most significant nibble of data sent. DAC Ramp Test Mode. Gain_B[13:3] contains the starting point, and the increment is (Offset_B/8). The increment will be added every 125 µsec.
30_H	dd_H	Trim/Configure: higher nibble of data byte determines what is trimmed/configured. Lower nibble is data to be programmed. See Table 3.5 for configuration details of data byte dd_H.
40H	00_H	Start NOM => Ends Command Mode, transition to Normal Operation Mode
	10_H	Start Raw Mode (RM) In this mode, if Gain_B = 800_H and Gain_T = 80_H, then the digital output will simply be the raw values of the ADC for the Bridge reading and the PTAT conversion.
50_H	XX_H	Start_CM => Start the Command Mode; used to enter command interpret mode
60_H	dd_H	Program SOT (2^{nd} order term)
70_H	dd_H	Program T_{SETL}
80_H	dd_H	Program Gain_B, upper 7 bits (set MSB of dd_H to 0_B)
90_H	dd_H	Program Gain_B, lower 8 bits
$A0_H$	dd_H	Program Offset_B, upper 6 bits (set the two MSBs of dd_H to 00_B)
$B0_H$	dd_H	Program Offset_B, lower 8 bits
$C0_H$	dd_H	Program Gain_T
$D0_H$	dd_H	Program Offset_T

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Command Byte	Data Byte	Description
$E0_H$	dd_H	Program Tco
$F0_H$	dd_H	Program Tcg

Table 3.5 Programming Details for Command 30_H

3rd Nibble	4th Nibble	Description
0_H	$Xbbb_B$	Trim oscillator; only least significant 3 bits of data used ($Xbbb_B$).
1_H	$bbbb_B$	Trim 1 V reference; least significant 4 bits of data used ($bbbb_B$).
2_H	$XXbb_B$	Offset Mode; only least significant 2 bits of data used ($XXbb_B$).
3_H	$XXbb_B$	Set output mode; only least significant 2 bits of data used ($XXbb_B$).
4_H	$XXbb_B$	Set update rate; only least significant 2 bits of data used ($XXbb_B$).
5_H	$bbbb_B$	Configure JFET regulation
6_H	$bbbb_B$	Program the Tc_cfg register.
7_H	$bbbb_B$	Program bits [99:96] of EEPROM. (SOT_cfg, Pamp_Gain)

3.4. Calibration Sequence

Although the ZSC31010 can function with many different types of resistive bridges, assume it is connected to a pressure bridge for the following calibration example.

In this case, calibration essentially involves collecting raw bridge and temperature data from the ZSC31010 for different known pressures and temperatures. This raw data can then be processed by the calibration master (the PC), and the calculated coefficients can then be written to the EEPROM of the ZSC31010.

IDT can provide software and hardware with samples to perform the calibration.

There are three main steps to calibration:

1. Assigning a unique identification to the ZSC31010. This identification is programmed into the EEPROM and can be used as an index into the database stored on the calibration PC. This database will contain all the raw values of bridge readings and temperature reading for that part, as well as the known pressure and temperature the bridge was exposed to. This unique identification can be stored in a combination of the following EEPROM registers: T_{SETL}, Tcg, Tco. These registers will be overwritten at the end of the calibration process, so this unique identification is not a permanent serial number.
2. Data collection. Data collection involves getting raw data from the bridge at different known pressures and temperatures. This data is then stored on the calibration PC using the unique identification of the IC as the index to the database.
3. Coefficient calculation and write. Once enough data points have been collected to calculate all the desired coefficients, then the coefficients can be calculated by the calibrating PC and written to the IC.

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Step 1: Assigning Unique Identification

Assigning a unique identification number is as simple as using the commands Program T_{SETL}, Program Tcg, and Program Tco. These three 8-bit registers will allow for 16M unique devices. In addition, Gain_B must be programmed to 800_H (unity), and Gain_T must be programmed to 80_H (unity).

Step 2: Data Collection

The number of different unique (pressure, temperature) points that calibration needs to be performed at depends on the customer's needs. The minimum is a 2-point calibration, and the maximum is a 5-point calibration. To acquire raw data from the part, instruct the ZSC31010 to enter Raw Mode. This is done by issuing a Start_CM (Start Command Mode, 5000_H) command to the IC, followed by a Start_RM (Start Raw Mode, 4010_H) command with the LSB of the upper data nibble set. Now, if the Gain_B term was set to unity (800_H) and the Gain_T term was also set to unity (80_H), then the part will be in Raw Mode and will be outputting raw data on its Sig™ pin, instead of corrected bridge and temperature values. The calibration system should now collect several of these data points (16 each of bridge and temperature is recommended) and average them. These raw bridge and temperature measurements should be stored in the database, along with the known pressure and temperature. The output format during Raw Mode is Bridge_High, Bridge_Low, Temp, each of these being 8-bit quantities. The upper 2 bits of Bridge_High are zero-filled. The Temp data (8-bit only) would not really be enough data for accurate temperature calibration. Therefore, the upper 3 bits of temperature information are not given, but rather assumed known. Therefore, effectively 11 bits of temperature information are provided in this mode.

Step 3: Coefficient Calculations

The mathematical equations used to perform the coefficient calculation are quite complicated; therefore only a basic overview is provided in section 3.6. IDT will, however, provide software to perform the coefficient calculation and the source code algorithms in a C-code format upon request. Once the coefficients are calculated, the final step is to write them to the EEPROM of the ZSC31010.

The number of calibration points required can be as few as two or as many as five. This depends on the precision desired, and the behavior of the resistive bridge in use.

- 2-point calibration would be used to obtain only a gain and offset term for bridge compensation with no temperature compensation for either term.
- 3-point calibration would be used to also obtain the Tco term for 1st order temperature compensation of the bridge offset term.
- 3-point calibration could also be used to obtain the additional term SOT for 2nd order correction for the bridge (SOT_BR), but no temperature compensation of the bridge output; see section 3.6.2.7 for limitations.
- 4-point calibration would be used to also obtain both, the Tco term and the Tcg term, which provides 1st order temperature compensation of the bridge offset gain term.
- 4-point calibration could also be used to obtain the Tco term and the SOT_BR term; see section 3.6.2.7 for limitations.
- 5-point calibration would be used to obtain Tco, Tcg, and an SOT term that provides 2nd order correction applied to one and only one of the following: 2nd order Tco (SOT_Tco), 2nd order Tcg (SOT_Tcg), or 2nd order bridge (SOT_BR); see section 3.6.2.7 for limitations.

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3.5. EEPROM Bits

Table 3.6 shows the bit order in the EEPROM, which are programmed through the serial interface. See Table 5.1 for the ZSC31010 default settings.

Table 3.6 ZSC31010 EEPROM Bits

EEPROM Range	Description	Notes
2:0	Osc_Trim	See the table in section 2.5.1 for complete data. 100 => Fastest 101 => 3 clicks faster than nominal 110 => 2 clicks faster than nominal 111 => 1 click faster than nominal 000 => Nominal 001 => 1 click slower than nominal 010 => 2 clicks slower than nominal 011 => Slowest
6:3	1V_Trim/JFET_Trim	See the table in section 2.4.3.
8:7	A2D_Offset	Offset selection: 11 => [-1/2,1/2] mode bridge inputs 10 => [-1/4,3/4] mode bridge inputs 01 => [-1/8,7/8] mode bridge inputs 00 => [-1/16,15/16] mode bridge inputs To change the bridge signal polarity, set Tc_cfg[3](=Bit 87).
10:9	Output_Select	00 => Digital (3-bytes with parity): Bridge High {00,[5:0]} Bridge Low [7:0] Temp [7:0] 01 => 0-1 V Analog 10 => Rail-to-rail ratiometric analog output 11 => Digital (2-bytes with parity) (No Temp) Bridge High {00,[5:0]} Bridge Low [7:0]
12:11	Update_Rate	00 => 1 msec (1 kHz) 01 => 5 msec (200 Hz) 10 => 25 msec (40 Hz) 11 => 125 msec (8 Hz)
14:13	JFET_Cfg	00 => No JFET regulation (lower power) 01 => No JFET regulation (lower power) 10 => JFET regulation centered around 5.0 V 11 => JFET regulation centered around 5.5 V (i.e. over-voltage protection).

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EEPROM Range	Description	Notes
29:15	Gain_B	Bridge Gain: Gain_B[14] => multiply x 8 Gain_B[13:0] => 14-bit unsigned number representing a number in the range [0,8)
43:30	Offset_B	Signed 14-bit offset for bridge correction
51:44	Gain_T	Temperature gain coefficient used to correct PTAT reading.
59:52	Offset_T	Temperature offset coefficient used to correct PTAT reading.
67:60	T_{SETL}	Raw PTAT reference value. (See *Technical Note — ZSC31010, ZSC31015, and ZSSC3015 Calibration Sequence, DLL, and EXE* for details.*)*
75:68	Tcg	Coefficient for temperature correction of bridge gain term. Tcg = 8-bit magnitude of Tcg term. Sign is determined by Tc_cfg (bits 87:84).
83:76	Tco	Coefficient for temperature correction of bridge offset term. Tco = 8-bit magnitude of Tco term. Sign and scaling are determined by Tc_cfg (bits 87:84).
87:84	Tc_cfg	This 4-bit term determines options for temperature compensation of the bridge: Tc_cfg[3] => If set, bridge signal polarity flips. Tc_cfg[2] => If set, Tcg is negative. Tc_cfg[1] => Scale magnitude of Tco term by 8, and if SOT applies to Tco, scale SOT by 8. Tc_cfg[0] => If set, Tco is negative.
95:88	SOT	2nd Order Term. This term is a 7-bit magnitude with sign. SOT[7] = 1 ➔ negative SOT[7] = 0 ➔ positive SOT[6:0] = magnitude [0-127] This term can apply to a 2nd order Tcg, Tco or bridge correction*. (See Tc_cfg above.)

* The SOT range for the bridge correction is limited for the negative value to 0xC0 by the *MathLib.DLL*. See *Technical Note — ZSC31010, ZSC31015, and ZSSC3015 Calibration Sequence, DLL, and EXE* for details.

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EEPROM Range	Description	Notes
99:96	{SOT_cfg, Pamp_Gain}	Bits [99:98] = SOT_cfg (For more details, see section 3.6.1.) 00 = SOT applies to Bridge 01 = SOT applies to Tcg 10 = SOT applies to Tco 11 = Prohibited Bits [97:96] = PreAmp Gain 00 => 6 01 => 24 (default setting) 10 => 12 11 => 48 (Only the default gain setting (24) is tested at the factory; all other gain settings are not guaranteed.)

3.6. Calibration Math

3.6.1. Correction Coefficients

All terms are calculated external to the IC and then programmed to the EEPROM through the serial interface.

Table 3.7 Correction Coefficients

Coefficient	Description
Gain_B	Gain term used to compensate span of Bridge reading
Offset_B	Offset term used to compensate offset of Bridge reading
Gain_T	Gain term used to compensate span of Temp reading
Offset_T	Offset term used to compensate offset of Temp reading
SOT	Second Order Term. The SOT can be applied as a second order correction term for the following: - Bridge measurement - Temperature coefficient of offset (Tco) - Temperature coefficient of gain (Tcg) The EEPROM bits 99:98 determine what SOT applies to. Note: There are limitations for the SOT for the bridge measurement and for the SOT for the Tco, which are explained in section 3.6.2.7.
T_{SETL}	RAW PTAT reference value. (See *Technical Note—ZSC31010, ZSC31015, and ZSSC3015 Calibration Sequence, DLL, and EXE* for details.*)*
Tcg	Temperature correction coefficient of bridge gain term (this term has an 8-bit magnitude and a sign bit (Tc_cfg[2]).
Tco	Temperature correction coefficient of bridge offset term (this term has an 8-bit magnitude, a sign bit (Tc_cfg[0]), and a scaling bit (Tc_cfg[1]), which can multiply its magnitude by 8).

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3.6.2. Interpretation of Binary Numbers for Correction Coefficients

BR_Raw should be interpreted as an unsigned number in the set [0, 16383] with a resolution of 1.

T_Raw should be interpreted as an unsigned number in the set [0, 16383], with a resolution of 4.

3.6.2.1. Gain_B Interpretation

Gain_B should be interpreted as a number in the set [0, 64]. The MSB (bit 14) is a scaling bit that will multiply the effect of the remaining bits Gain_B[13:0] by 8. Bits Gain_B[13:0] represent a number in the range of [0, 8], with Gain_B[13] having a weighting of 4, and each subsequent bit has a weighting of ½ the previous bit.

Table 3.8 Gain_B[13:0] Weightings

Bit Position	Weighting
13	$2^2 = 4$
12	$2^1 = 2$
11	$2^0 = 1$
10	2^{-1}
...	...
3	2^{-8}
2	2^{-9}
1	2^{-10}
0	2^{-11}

Examples:

The binary number: $010010100110001_B = 4.6489$; Gain_B[14] is 0_B, so the number represented by Gain_B[13:0] is not multiplied by 8.

The binary number: $101100010010110_B = 24.586$; Gain_B[14] is 1_B, so the number represented by Gain_B[13:0] is multiplied by 8.

Limitation: Using the 5-point calibration 5pt-Tcg&Tco&SOT_Tco (including the second order SOT_Tco), the Gain_B is limited to a value equal or less than 8 (instead of 64).

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3.6.2.2. Offset_B Interpretation

Offset_B is a 14-bit signed binary number in two's complement form. The MSB has a weighting of -8192. The following bits then have a weighting of 4096, 2048, 1024, …

Table 3.9 Offset_B Weightings

Bit Position	Weighting
13	-8192
12	$2^{12} = 4096$
11	$2^{11} = 2048$
10	$2^{10} = 1024$
...	...
3	$2^{3} = 8$
2	$2^{2} = 4$
1	$2^{1} = 2$
0	$2^{0} = 1$

For example, the binary number $11111111111100_B = -4$

3.6.2.3. Gain_T Interpretation

Gain_T should be interpreted as a number in the set [0,2]. Gain_T[7] has a weighting of 1, and each subsequent bit has a weighting of ½ the previous bit.

Table 3.10 Gain_T Weightings

Bit Position	Weighting
7	$2^{0} = 1$
6	2^{-1}
5	2^{-2}
4	2^{-3}
3	2^{-4}
2	2^{-5}
1	2^{-6}
0	2^{-7}

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3.6.2.4. Offset_T Interpretation

Offset_T is an 8-bit signed binary number in two's complement form. The MSB has a weighting of -128. The following bits then have a weighting of 64, 32, 16 …

Table 3.11 Offset_T Weightings

Bit Position	Weighting
7	-128
6	$2^6 = 64$
5	$2^5 = 32$
4	$2^4 = 16$
3	$2^3 = 8$
2	$2^2 = 4$
1	$2^1 = 2$
0	$2^0 = 1$

For example, the binary number $00101001_B = 41$.

3.6.2.5. Tco Interpretation

Tco is specified as an 8-bit magnitude with an additional sign bit (Tc_cfg[0]), and a scalar bit (Tc_cfg[1]). When the scalar bit is set, the signed Tco is multiplied by 8.

Tco Resolution: 0.175 µV/V/°C (input referred)
Tco Range: ± 44.6 µV/V/°C (input referred)

If the scaling bit is used, then the above resolution and range are scaled by 8 to give the following results:

Tco Scaled Resolution: 1.40 µV/V/°C (input referred)
Tco Scaled Range: ± 357 µV/V/°C (input referred)

3.6.2.6. Tcg Interpretation

Tcg is specified as an 8-bit magnitude with an additional sign bit (Tc_cfg[2]).

Tcg Resolution: 17.0 ppm/°C
Tcg Range: ±4335 ppm/°C

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3.6.2.7. SOT Interpretation

SOT is a 2nd order term that can apply to one and only one of the following: bridge non-linearity correction, Tco non-linearity correction, or Tcg non-linearity correction.

As it applies to bridge non-linearity correction:

Resolution: 0.25% @ Full Scale

2nd order correction SOT_BR is possible up to +5%/-6.2% full scale difference from the ideal fit (straight line), because the SOT coefficient values are limited to the range of (0xC0 = -0.25_{dec}) to (0x7F = 0.4960938_{dec}). (Saturation in internal arithmetic will occur at greater negative non-linearities.)

Limitation: Using any calibration method for which SOT is applied to the bridge measurement (SOT_BR), there is a possibility of calibration math overflow. This only occurs if the sensor input exceeds 200% of the calibrated full span, which means the highest applied sensor input should never go higher than this value.

Example: This example of the limitation when SOT is applied to the bridge reading uses a pressure sensor bridge that outputs -10 mV at the lowest pressure of interest. That point is calibrated to read 0%. The same sensor outputs +40 mV at the highest pressure of interest. That point is calibrated to read 100%. This sensor has a 50 mV span over the pressure range of interest. If the sensor were to experience an over-pressure event that took the sensor output up to 90 mV (200% of span), the internal calculations could overflow. The result would be a corrected bridge reading that would not be saturated at 100% as expected, but instead read a value lower than 100%. This problem only occurs when SOT is applied to correct the bridge reading.

As SOT applies to Tcg:

Resolution: 0.3 ppm/(^oC)^2
Range: ±38 ppm/(^oC)^2

As it applies to Tco:

Two settings are possible. It is possible to scale the effect of SOT by 8. If Tc_cfg[1] is set, then both, Tco and SOT's contribution to Tco, are multiplied by 8.

Resolution at unity scaling:	1.51 nV/V/(^oC)^2	(input referred)
Range:	±0.192 μV/V/(^oC)^2	(input referred)
Resolution at 8x scaling:	12.1 nV/V/(^oC)^2	(input referred)
Range:	±1.54 μV/V/(^oC)^2	(input referred)

Limitation: If the second order term SOT applies to Tco, the bridge gain Gain_B is limited to values equal or less than 8 (instead of 64).

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3.7. Reading EEPROM Contents

The contents of the entire EEPROM memory can be read using the Read EEPROM command (00_H). This command causes the IC to output consecutive bytes on the ZACwire™. After each transmission, the EEPROM contents are shifted by 8 bits. The bit order of these bytes is given in Table 3.12.

Table 3.12 EEPROM Read Order

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 1	Offset_B[7:0]							
Byte 2	Gain_T[1:0]		Offset_B[13:8]					
Byte 3	Offset_T[1:0]		Gain_T[7:2]					
Byte 4	T_{SETL}[1:0]		Offset_T[7:2]					
Byte 5	Tcg[1:0]		T_{SETL}[7:2]					
Byte 6	Tco[1:0]		Tcg[7:2]					
Byte 7	Tc_cfg[1:0]		Tco[7:2]					
Byte 8	SOT[5:0]						Tc_cfg[3:2]	
Byte 9	Osc_Trim[1:0]		SOT_cfg[3:0] *				SOT[7:6]	
Byte 10	Output_ Select[0]	A2D_Offset[1:0]		1V_Trim[3:0] **				Osc_Trim[2]
Byte 11	Gain_B[2:0]			JFET_Cfg[1:0]		Update_Rate[1:0]		Output_ Select[1]
Byte 12	Gain_B[10:3]							
Byte 13	Offset_B[3:0] ***				Gain_B[14:11]			
Byte 14	$A5_H$							

* SOT_cfg/Pamp_Gain
** 1V_Trim/JFET_Trim
*** Duplicates first 4 bits of Byte 1

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4 Application Circuit Examples

Note: The typical output analog load resistor R_L = 10 kΩ (minimum 2.5 kΩ). This optional load resistor can be configured as a pull-up or pull-down. If it is configured as a pull-down, it cannot be part of the module to be calibrated because this would prevent proper operation of the ZACwire™. If a pull-down load is desired, it must be added to the system after module calibration.

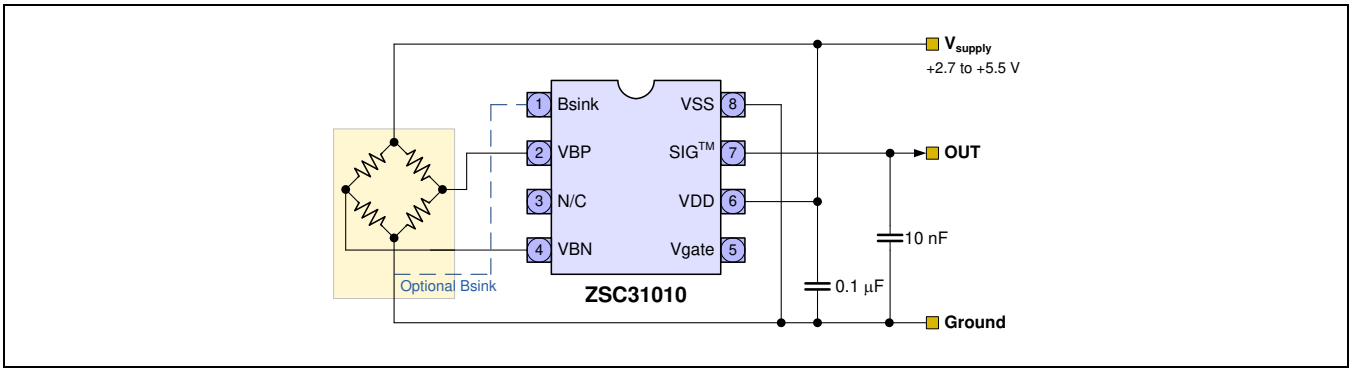
There is no output load capacitance needed.

EEPROM contents: OUTPUT_select, JFET_Cfg, 1V_Trim/JFET-Trim

4.1. Three-Wire Rail-to-Rail Ratiometric Output

This example shows an application circuit for rail-to-rail ratiometric voltage output configuration with temperature compensation via internal PTAT. The same circuitry is applicable for a 0 to 1 V absolute analog output.

Figure 4.1 Rail-to-Rail Ratiometric Voltage Output



The optional bridge sink allows power savings switching off the bridge current. The output voltage can be one of the following options:

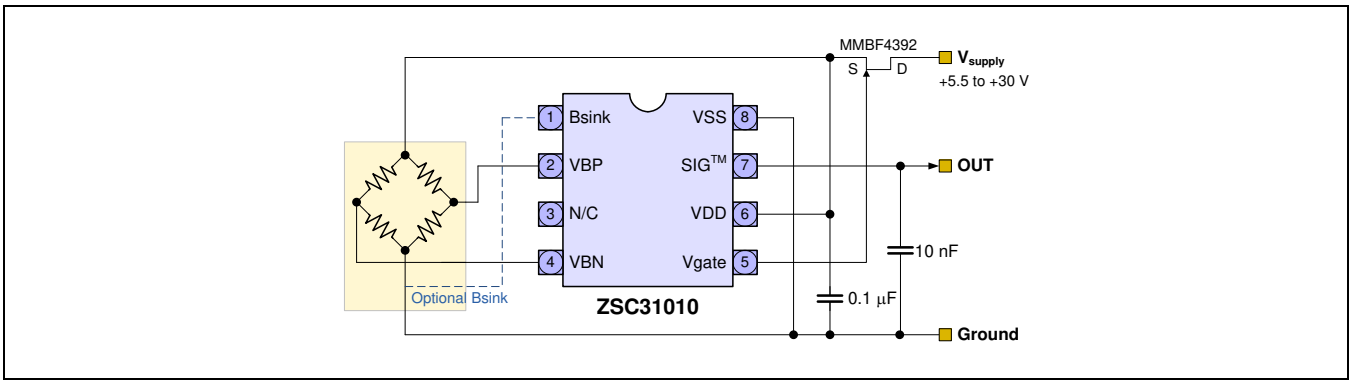
- Rail-to-rail ratiometric analog output V_{DD} (= V_{supply}).
- 0 to 1 V absolute analog output. The absolute voltage output reference is trimmable 1 V (±3 mV) in the 1 V output mode via a 4-bit EEPROM field (see section 2.4.3).

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4.2. Absolute Analog Voltage Output

The figure below shows an application circuit for an absolute voltage output configuration with temperature compensation via internal temperature PTAT, and external JFET regulation for all industry standard applications. The gate-source cutoff voltage (V_{GS}) of the selected JFET must be ≤ -2 V.

Figure 4.2 Absolute Analog Voltage Output



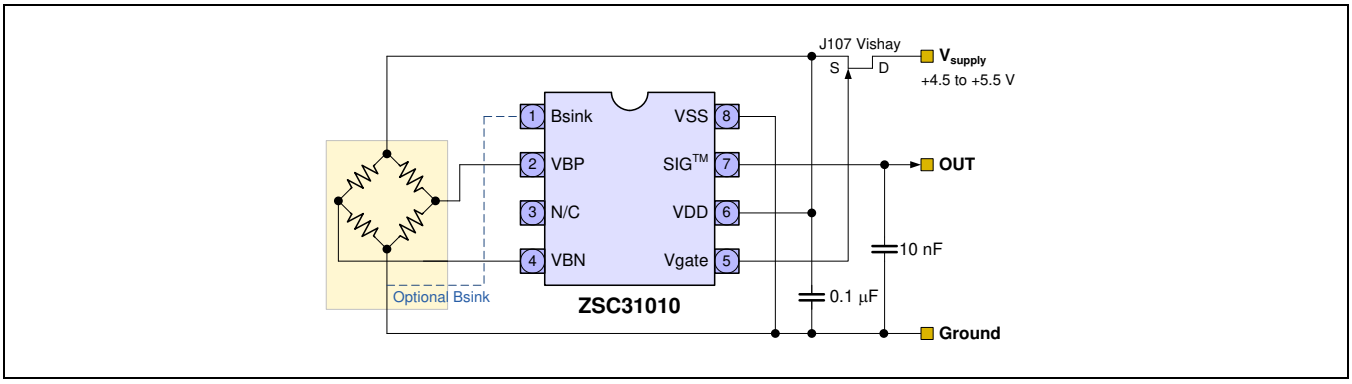
The output signal range can be one of the following options:

- 0 to 1 V analog output. The absolute voltage output reference is trimmable: 1 V (± 3 mV) in the 1 V output mode via a 4-bit EEPROM field (see section 2.4.3).
- Rail-to-rail analog output. The on-chip reference for the JFET regulator block is trimmable: 5 V (± 15 mV) in the ratiometric output mode via a 4-bit EEPROM field (see section 2.4.3).

4.3. Three-Wire Ratiometric Output with Over-Voltage Protection

The figure below shows an application circuit for a ratiometric output configuration with temperature compensation via an internal diode. In this application, the JFET is used for over-voltage protection. JFET_Cfg bits [14:13] in EEPROM are configured to 5.5 V. There is an additional maximum error of 8 mV caused by the non-zero r_{ON} of the limiter JFET.

Figure 4.3 Ratiometric Output, Temperature Compensation via Internal Diode



4.4. Digital Output

For all three circuits, the output signal can also be digital. Depending on the output select bits, the bridge signal, or the bridge signal and temperature signal are sent.

For the digital output, no load resistor, or load capacity are necessary. No pull-down resistor is allowed. If a line resistor or pull-up resistor is used, the requirement for the rise time must be met (≤ 5 µs). The IC output includes a pull-up resistor of about 30 kΩ. The digital output can easily be read by firmware from a microcontroller, and IDT can provide the customer with software in developing the interface.

4.5. Output Short Protection

The output of the ZSC31010 has no short protection. Therefore, a resistor RSP in series with the output must be added in the application module. Refer to Table 4.1 to determine the value of RSP [†].

To minimize additional error caused by this resistor for the analog output voltage, the load impedance must meet the following requirement:

$$R_L >> R_{SP}$$

Table 4.1 Resistor Values for Short Protection

Temperature Range (T_{AMBMAX})	Resistor R_{SP}	Note
Up to 85°C	51 Ω	$R_{SP} = V_{DD}/I_{max}$ with $I_{max} = ([(170°C - T_{AMBMAX})/(163°C/W)] - V_{DD} * I_{DD})/VDD$
Up to125°C	100 Ω	
Up to 150°C	240 Ω	

[†] Tested at V_{DD} =5V for 20 minutes for T_{AMBMAX}.

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5 Default EEPROM Settings

If needed, the default setting for the ZSC31010 can be reprogrammed as described in section 3.

Table 5.1 Factory Settings for the ZSC31010 EEPROM

EEPROM Range	Name	Default Values (Hex) Until Week 9/2006	Default Values (Hex) Since Week 10/2006	Default Values (Hex) Since Week 48/2008
2:0	Osc_Trim	0xX	0xX	0xX
6:3	1V_Trim/JFET_Trim	0xX	0xX	0xX
8:7	A2D_Offset	0x0	0x3	0x3
10:9	Output_Select	0x3	0x2	0x2
12:11	Update_Rate	0x2	0x1	0x1
14:13	JFET_Cfg	0x1	0x2	0x2
29:15	Gain_B	0x800	0x0	0x3FFF
43:30	Offset_B	0x0	0x203	0x00FF
51:44	Gain_T	0x80	0x80	0x80
59:52	Offset_T	0x0	0x0	0x0
67:60	T_{SETL}	0x0	0x0	0x0
75:68	Tcg	0x0	0x0	0x0
83:76	Tco	0xE	0x0	0x0
87:84	Tc_cfg	0x0	0x0	0x0
95:88	SOT	0x0	0x0	0x0
99:96	{SOT_cfg, Pamp_Gain}	0x1	0x5	0x5

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6 Pin Configuration and Package

The standard package of the ZSC31010 is an SOP-8 (3.81 mm / 150 mil body) with a lead-pitch 1.27 mm / 50 mil.

Table 6.1 Storage and Soldering Conditions for the SOP-8 Package

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Maximum Storage Temperature	$T_{max_storage}$	Less than 10hrs, before mounting			150	°C
Minimum Storage Temperature	$T_{min_storage}$	Store in original packing only	-50			°C
Maximum Dry-Bake Temperature	$T_{drybake}$	Less than100 hrs total, before mounting			125	°C
Soldering Peak Temperature	T_{peak}	Less than 30s (IPC/JEDEC-STD-020 Standard)			260	°C

Figure 6.1 ZSC31010 Pin-Out Diagram

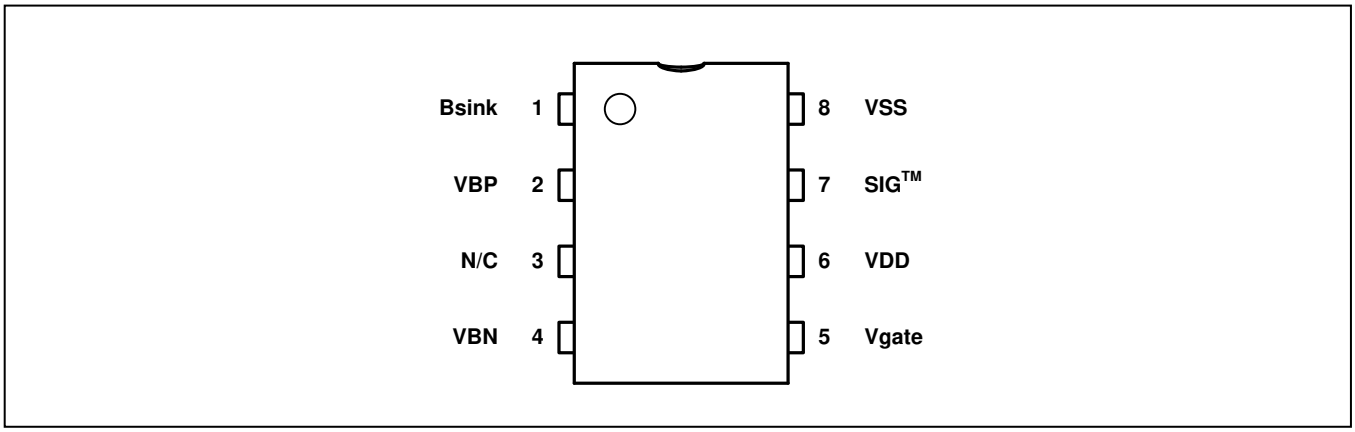


Table 6.2 ZSC31010 Pin Configuration

Pin No.	Name	Description
1	Bsink	Optional ground connection for bridge ground. Used for power savings.
2	VBP	Positive bridge connection
3	N/C	No connection
4	VBN	Negative bridge connection
5	Vgate	Gate control for external JFET regulation/over-voltage protection
6	VDD	Supply voltage (2.7 - 5.5 V)
7	SIG™	ZACwire™ interface (analog out, digital out, calibration interface)
8	VSS	Ground supply

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7 ESD/Latch-Up-Protection

All pins have an ESD protection of > 4000 V and a latch-up protection of ±100 mA or of +8V/-4 V (to VSS/VSSA). ESD protection referred to the Human Body Model is tested with devices in SOP-8 packages during product qualification. The ESD test follows the Human Body Model with 1.5 kΩ/100 pF based on MIL 883, Method 3015.7.

8 Test

The test program is based on this datasheet. The final parameters that will be tested during series production are listed in the tables of section 1. The digital part of the IC includes a scan path, which can be activated and controlled during wafer test. It guarantees failure coverage of more than 98%. Further test support for testing of the analog parts on wafer level is included in the DSP.

9 Quality and Reliability

A reliability investigation according to the in-house non-automotive standard has been performed.

10 Customization

For high-volume applications which require an upgraded or downgraded functionality compared to the ZSC31010, IDT can customize the circuit design by adding or removing certain functional blocks. IDT can provide a custom solution quickly because it has a considerable library of sensor-dedicated circuitry blocks. Please contact IDT for further information.

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11 Ordering Codes

Sales Code	Description	Package
ZSC31010CEB	ZSC31010 Die — Temperature range:-50°C to +150°C	Unsawn on Wafer
ZSC31010CEC	ZSC31010 Die — Temperature range:-50°C to +150°C	Sawn on Wafer Frame
ZSC31010CEG1	ZSC31010 SOP8 (150 mil) — Temperature range:-50°C to +150°C	Tube: add “-T” to sales code; reel: add “-R”
ZSC31010CIB	ZSC31010 Die — Temperature range: -40°C to 85°C	Unsawn on Wafer
ZSC31010CIC	ZSC31010 Die — Temperature range: -40°C to 85°C	Sawn on Wafer Frame
ZSC31010CIG1	ZSC31010 SOP8 (150 mil) — Temperature range: -40°C to 85°C	Tube: add “-T” to sales code Reel: add “-R”
ZSC31010KIT	ZSC31010 ZACwire™ SSC Evaluation Kit: Communication Board, SSC Board, Sensor Replacement Board, USB Cable, 5 IC Samples	Kit

Contact IDT Sales for support and sales of IDT’s ZSC31010 Mass Calibration System.

12 Related Documents

Document
ZACwire™ SSC Evaluation Kit Documentation for ZSC31010 and ZSC31015
SSC Kits Feature Sheet (includes ordering codes and prices)
Technical Note—ZSC31010, ZSC31015, and ZSSC3015 Calibration Sequence, DLL, and EXE

Visit the ZSC31010 product page at www.IDT.com/ZSC31010 or contact your nearest sales office for the latest version of these documents.

13 Definitions of Acronyms

Term	Description
ADC	Analog-to-Digital Converter
AFE	Analog Front-End
BUF	Buffer
CM	Command Mode
CMC	Calibration Microcontroller
DAC	Digital-to-Digital Converter
DNL	Differential Nonlinearity
DSP	Digital Signal Processor
DUT	Device Under Test
ESD	Electrostatic Discharge

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Term	Description
FSO	Full-Scale Output
INL	Integrated Nonlinearity
LSB	Least Significant Bit
MUX	Multiplexer
NOM	Normal Operation Mode
OWI	One-Wire Interface
POC	Power-On Clear
POR	Power-On Reset Level
PSRR	Power Supply Rejection Ratio
PTAT	Proportional To Absolute Temperature
RM	Raw Mode
SOT	Second Order Term

14 Document Revision History

Revision	Date	Description
2.44	08-Apr-2010	Clarification of part ordering codes and addition of document revision history.
2.50	27-Jul-2010	Revision of product name from ZMD31010 to ZSC31010.
2.60	11-Nov-2010	Removed reference to mass calibration kit; added footnote to short protection; added special measurement information (Table 3.3): revised stop bit definition; added EEPROM specifications to section 1.3 “Electrical Parameters.” Added Table 6.1 “Storage and Soldering Conditions” to section 6 “Pin Configuration and Package.” Corrected equation (2). Revised trim tolerances in section 2.4.3.
2.70	30-Mar-2011	Revision in “Related Documents” table for the name of the kit document. Revision in Table 6.1 to match the maximum temperature range in section 1.1. Updated trim tolerances in sections 4.1 and 4.2. Correction of formula in Table 4.1.
2.80	25-May-2011	Revision of Table 5.1 to add column for defaults as of 48/2008. Revisions to description of T_{SETL}.
2.81	07-Oct-2011	Revision to sales contact information and product title. Minor edit to “Benefits” section on page 2
2.82	06-Jul-2012	Revision to sales contact information for ZMD America, Inc.
2.83	05-Dec-2012	Revision to sales contact information for Zentrum Mikroelektronik Dresden AG, Korea Office. Revision to phone numbers for USA office.

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Revision	Date	Description
2.84	15-Aug-2013	Update for part codes on page 3 and in section 11. Update for contact information and images for cover and headers. Update for related documents section. Update for specification for sensor signal span to 3mV/V to 105mV/V. Clarification of EEPROM programming temperature specification in table note in section 1.2.
2.90	29-Aug-2013	Revision of certification status in section 9 “Quality and Reliability.” Minor edits.
2.91	01-Nov-2013	Revision of specifications in section 1.2 for “Output Load Capacitance” to add minimum specification. Revision of specifications in section 1.2 for “Output Load Resistance.” Added table note to section 1.2 regarding pull-down resistor. Added 10nF output cap to all application figures. Minor edits for clarity.
	20-Jan-2016	Changed to IDT branding.

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
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