Description

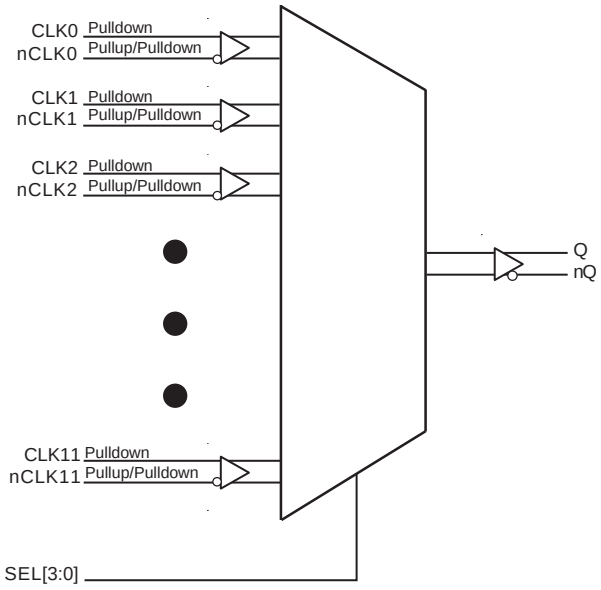
The ICS853S012I is an 12:1 Differential-to-3.3V or 2.5V LVPECL Clock/Data Multiplexer which can operate up to 3.2GHz. The ICS853S012I has twelve differential selectable clock inputs. The CLK, nCLK input pairs can accept LVPECL, LVDS or CML levels.

The fully differential architecture and low propagation delay make the device ideal for use in clock distribution circuits. The select pins have internal pull-down resistors.

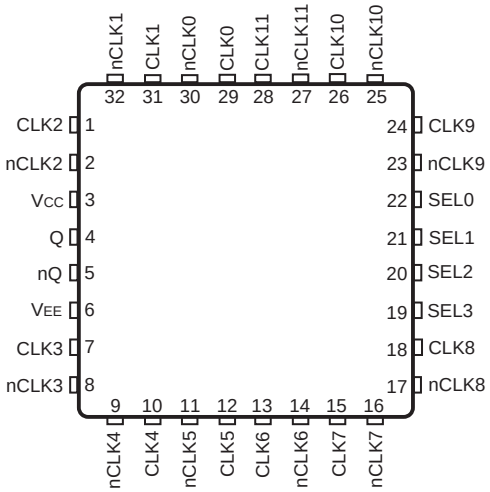
Features

- High speed 12:1 differential multiplexer
- One differential 3.3V or 2.5V LVPECL output
- Twelve selectable differential clock or data inputs
- CLKx, nCLKx pairs can accept the following differential input levels: LVPECL, LVDS, CML
- Maximum output frequency: 3.2GHz
- Translates any single ended input signal to LVPECL levels with resistor bias on nCLKx input
- Additive phase jitter, RMS: 0.144ps (typical)
- Part-to-part skew: 250ps (maximum)
- Propagation delay: 1.15ns (maximum)
- Full 3.3V or 2.5V operating supply modes
- -40°C to 85°C ambient operating temperature
- Available lead-free (RoHS 6) package

Block Diagram



Pin Assignment



ICS853S012I

32-Lead VFQFN
5mm x 5mm x 0.925mm package body
K Package
Top View

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Table 1. Pin Descriptions

Number	Name	Type		Description
1	CLK2	Input	Pulldown	Non-inverting differential clock input.
2	nCLK2	Input	Pullup/ Pulldown	Inverting differential clock input. $V_{CC}/2$ default when left floating.
3	V_{CC}	Power		Positive supply pin.
4, 5	Q, nQ	Output		Differential output pair. LVPECL interface levels.
6	V_{EE}	Power		Negative supply pin.
7	CLK3	Input	Pulldown	Non-inverting differential clock input.
8	nCLK3	Input	Pullup/ Pulldown	Inverting differential clock input. $V_{CC}/2$ default when left floating.
9	nCLK4	Input	Pullup/ Pulldown	Inverting differential clock input. $V_{CC}/2$ default when left floating.
10	CLK4	Input	Pulldown	Inverting differential clock input.
11	nCLK5	Input	Pullup/ Pulldown	Inverting differential clock input. $V_{CC}/2$ default when left floating.
12	CLK5	Input	Pulldown	Inverting differential clock input.
13	CLK6	Input	Pulldown	Non-inverting differential clock input.
14	nCLK6	Input	Pullup/ Pulldown	Inverting differential clock input. $V_{CC}/2$ default when left floating.
15	CLK7	Input	Pulldown	Non-inverting differential clock input.
16	nCLK7	Input	Pullup/ Pulldown	Inverting differential clock input. $V_{CC}/2$ default when left floating.
17	nCLK8	Input	Pullup/ Pulldown	Inverting differential clock input. $V_{CC}/2$ default when left floating.
18	CLK8	Input	Pulldown	Inverting differential clock input.
19, 20, 21, 22	SEL3, SEL2, SEL1, SEL0	Input	Pulldown	Clock select input pins. LVCMOS/LVTTL interface levels.
23	nCLK9	Input	Pullup/ Pulldown	Inverting differential clock input. $V_{CC}/2$ default when left floating.
24	CLK9	Input	Pulldown	Inverting differential clock input.
25	nCLK10	Input	Pullup/ Pulldown	Inverting differential clock input. $V_{CC}/2$ default when left floating.
26	CLK10	Input	Pulldown	Inverting differential clock input.
27	nCLK11	Input	Pullup/ Pulldown	Inverting differential clock input. $V_{CC}/2$ default when left floating.
28	CLK11	Input	Pulldown	Inverting differential clock input.
29	CLK0	Input	Pulldown	Inverting differential clock input.
30	nCLK0	Input	Pullup/ Pulldown	Inverting differential clock input. $V_{CC}/2$ default when left floating.
31	CLK1	Input	Pulldown	Inverting differential clock input.
32	nCLK1	Input	Pullup/ Pulldown	Inverting differential clock input. $V_{CC}/2$ default when left floating.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

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Table 2. Pin Characteristics

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
$R_{PULLDOWN}$	Input Pulldown Resistor				50		kΩ
R_{PULLUP}	Input Pullup Resistor				50		kΩ
C_{IN}	Input Capacitance	SEL[3:0]			2		pF

Function Table

Table 3. Control Input Function Table

Inputs				Outputs	
SEL3	SEL2	SEL1	SEL0	Q	nQ
0	0	0	0	CLK0	nCLK0 (default)
0	0	0	1	CLK1	nCLK1
0	0	1	0	CLK2	nCLK2
0	0	1	1	CLK3	nCLK3
0	1	0	0	CLK4	nCLK4
0	1	0	1	CLK5	nCLK5
0	1	1	0	CLK6	nCLK6
0	1	1	1	CLK7	nCLK7
1	0	0	0	CLK8	nCLK8
1	0	0	1	CLK9	nCLK9
1	0	1	0	CLK10	nCLK10
1	0	1	1	CLK11	nCLK11
1	1	X	X	L	H

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Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, I_O Continuous Current Surge Current	 50mA 100mA
Package Thermal Impedance, θ_{JA}	39.5°C/W (1 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{CC} = 3.3V ± 5%; V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Power Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current				70	mA

Table 4B. Power Supply DC Characteristics, V_{CC} = 2.5V ± 5%; V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Power Supply Voltage		2.375	2.5	2.625	V
I_{EE}	Power Supply Current				67	mA

Table 4C. LVCMOS/LVTTL DC Characteristics, V_{CC} = 3.3V ± 5% or 2.5V ± 5%; V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{CC} = 3.3V	2.2		V_{CC} + 0.3	V
			V_{CC} = 2.5V	1.7		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage		V_{CC} = 3.3V	-0.3		0.8	V
			V_{CC} = 2.5V	-0.3		0.7	V
I_{IH}	Input High Current	SEL[3:0]	V_{CC} = V_{IN} = 3.465V or 2.625V			150	µA
I_{IL}	Input Low Current	SEL[3:0]	V_{CC} = 3.465V or 2.625V, V_{IN} = 0V	-10			µA

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Table 4D. Differential DC Characteristics, V_{CC} = 3.3V ± 5% or 2.5V ± 5%; V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK[0:11], nCLK[0:11]	V_{CC} = V_{IN} = 3.465 or 2.625V			150	µA
I_{IL}	Input Low Current	CLK[0:11]	V_{CC} = 3.465 or 2.625V, V_{IN} = 0V	-10			µA
		nCLK[0:11]	V_{CC} = 3.465 or 2.625V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Voltage			0.15		1.5	V
V_{CMR}	Common Mode Range; NOTE 1			1.2		V_{CC}	V

NOTE 1: Common mode input voltage is defined as V_{IH}.

Table 4E. LVPECL DC Characteristics, V_{CC} = 3.3V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CC} – 1.125		V_{CC} – 0.935	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CC} – 1.895		V_{CC} – 1.670	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs termination with 50Ω to V_{CC} – 2V.

Table 4F. LVPECL DC Characteristics, V_{CC} = 2.5V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CC} – 1.125		V_{CC} – 0.835	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CC} – 1.895		V_{CC} – 1.670	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs termination with 50Ω to V_{CC} – 2V.

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AC Electrical Characteristics

Table 5. AC Electrical Characteristics, V_{CC} = 3.3V ± 5% or 2.5V ± 5%; V_{EE} = 0V, T_A = -40°C to 85°C

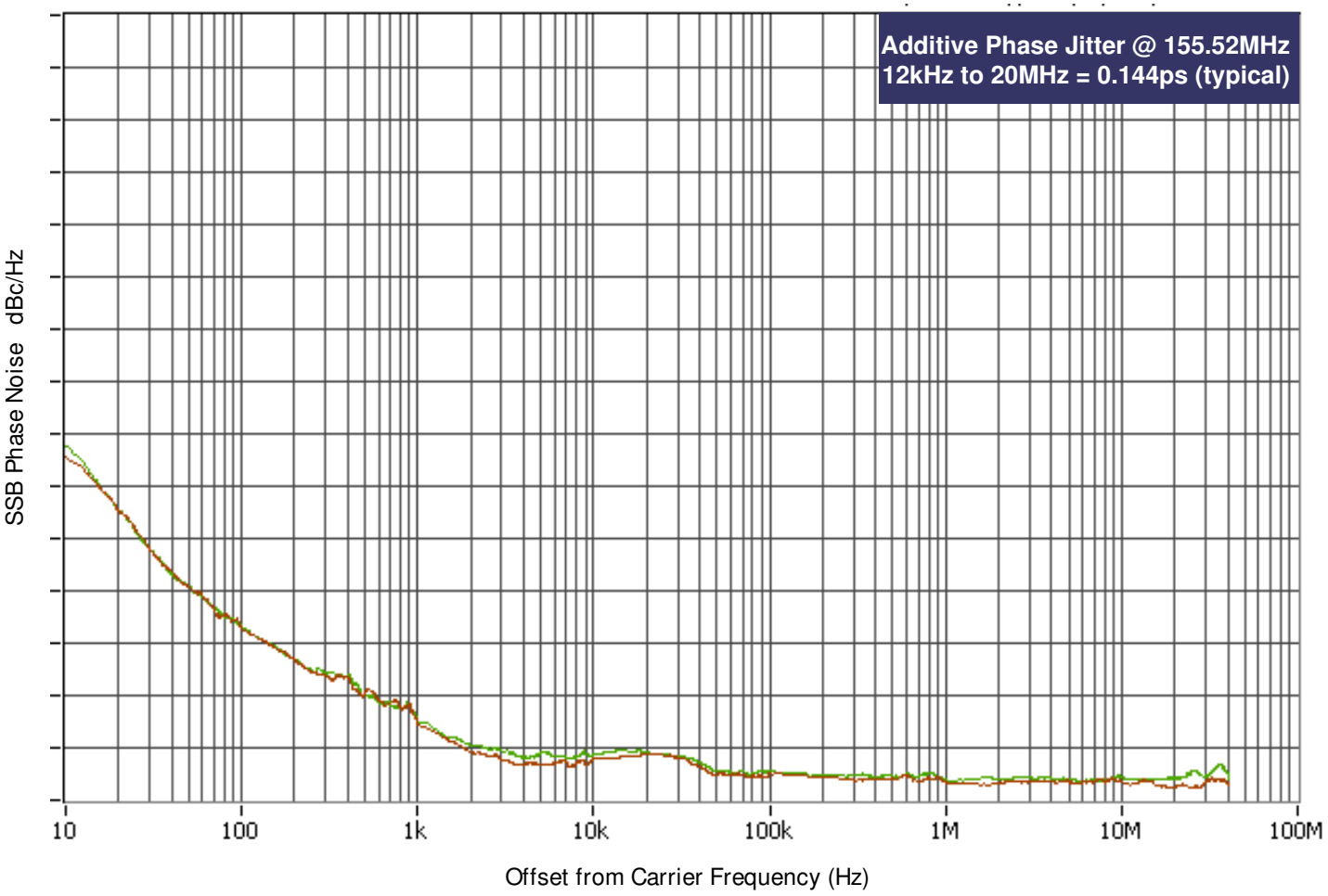
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency				3.2	GHz
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	f_{OUT} = 155.52MHz, V = 3.3V Integration Range: 12kHz – 20MHz		0.144		ps
		f_{OUT} = 155.52MHz, V = 2.5V Integration Range: 12kHz – 20MHz		0.164		ps
t_{PD}	Propagation Delay; NOTE 1	CLKx, nCLKx to Q, nQ	425		875	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 2, 3				250	ps
*t*sk(i)	Input Skew				60	ps
t_R / t_F	Output Rise/ Fall Time	20% to 80%	75		225	ps
$MUX_{ISOLATION}$	Mux Isolation; NOTE 4	f_{OUT} = 155.52MHz, Input Peak-to-Peak = 800mV		75		dB

NOTE: All parameters characterized up to 1GHz unless noted otherwise.
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs on different devices operating at the same supply voltage, same frequency, same temperature and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 3: This parameter is defined in accordance to JEDEC Standard 65.
NOTE 4: Qx, nQx outputs measured differentially. See *MUX Isolation diagram* in the *Parameter Measurement Information section.*

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Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the *dBc Phase Noise*. This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a *dBc* value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



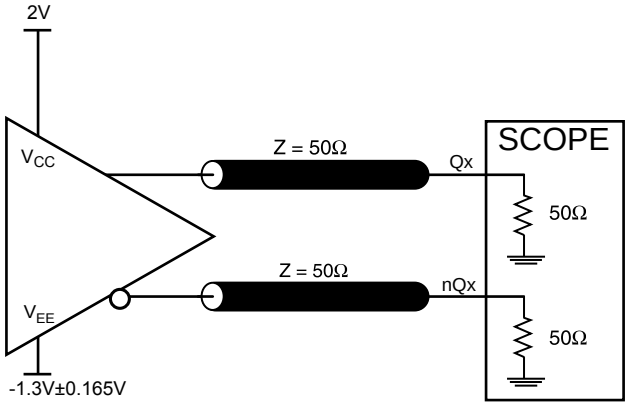
As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

Measured using a Rohde & Schwarz SMA100 as the input source.

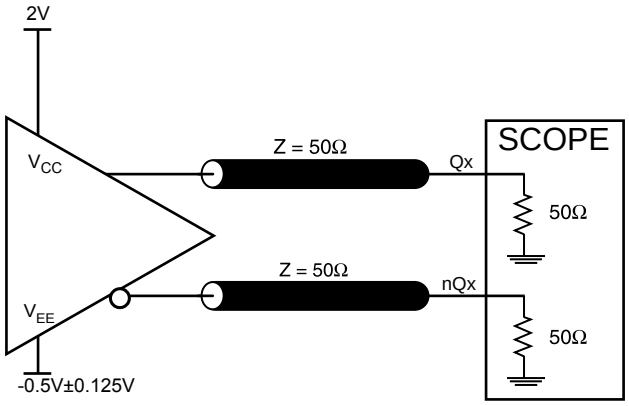
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Parameter Measurement Information

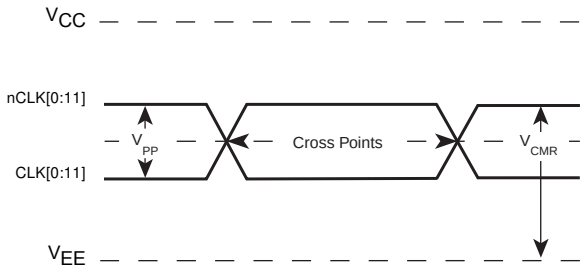
3.3V LVPECL Output Load AC Test Circuit



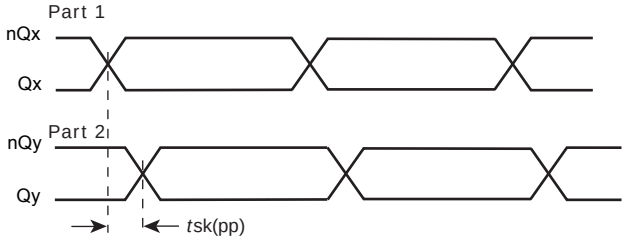
2.5V LVPECL Output Load AC Test Circuit



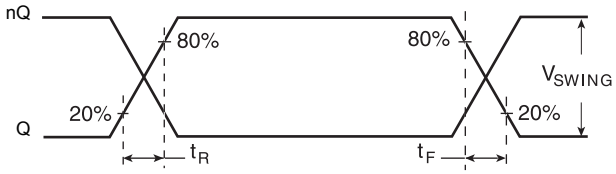
Differential Input Level



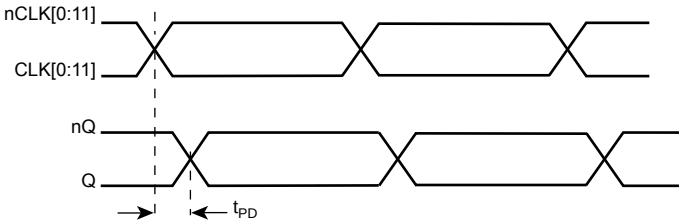
Part-to-Part Skew



Output Rise/Fall Time

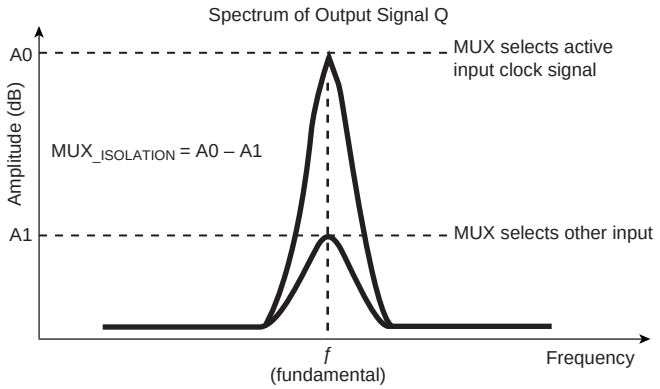


Propagation Delay

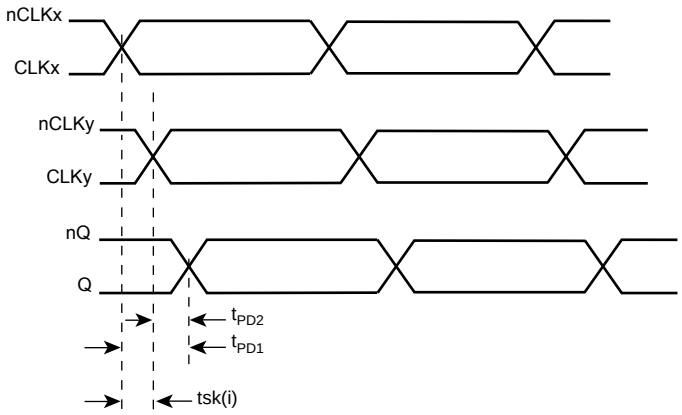


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MUX Isolation



Input Skew



$tsk(i) = |t_{PD1} - t_{PD2}|$

x, y = 0 to 11

Applications Information

Wiring the Differential Input to Accept Single-Ended Levels

Figure 1 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_{REF} = V_{CC}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_{REF} in the center of the input voltage swing. For example, if the input clock swing is 2.5V and V_{CC} = 3.3V, R1 and R2 value should be adjusted to set V_{REF} at 1.25V. The values below are for when both the single ended swing and V_{CC} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance.

For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than V_{CC} + 0.3V. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

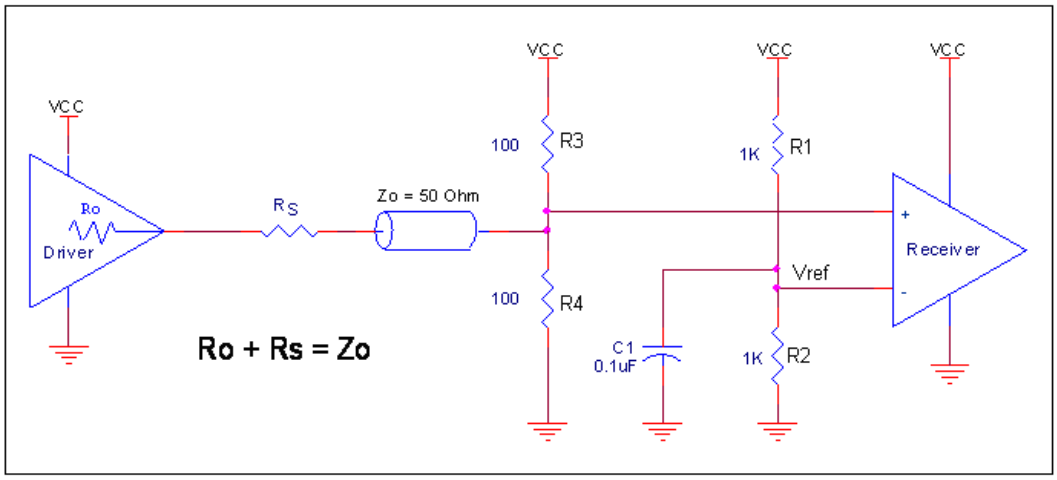


Figure 1. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

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3.3V Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, CML and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 2A to 2E* show interface examples for the IN/nIN input with built-in 50Ω terminations driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

Figure 2A. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

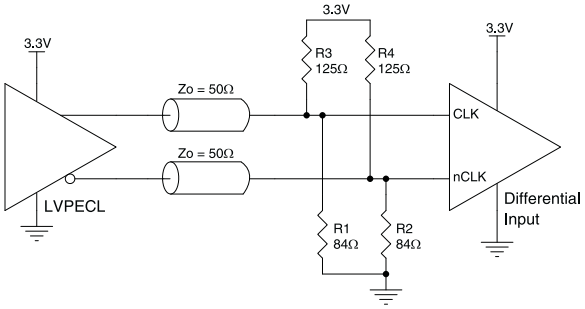


Figure 2B. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

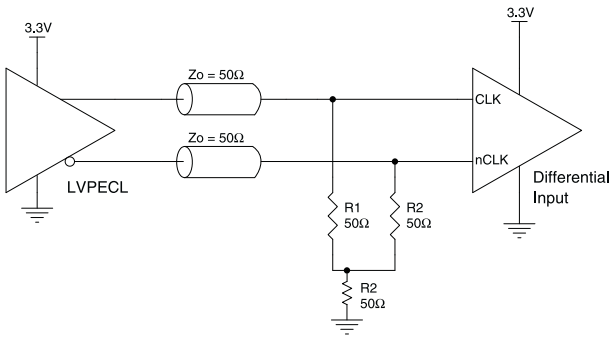


Figure 2C.CLK/nCLK Input Driven by a 3.3V LVDS Driver

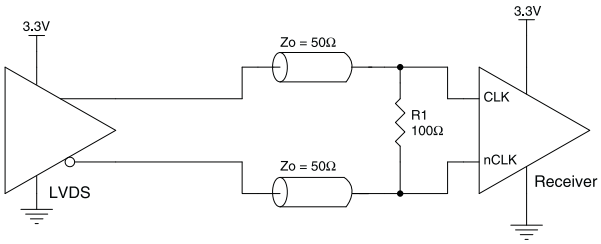


Figure 2D. CLK/nCLK Input Driven by a Built-In Pullup CML Driver

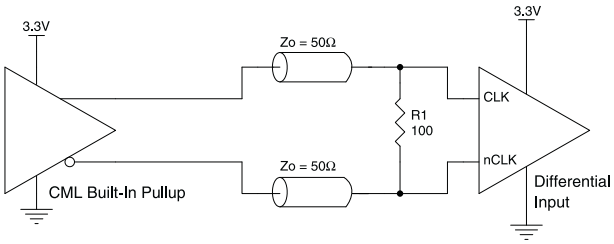
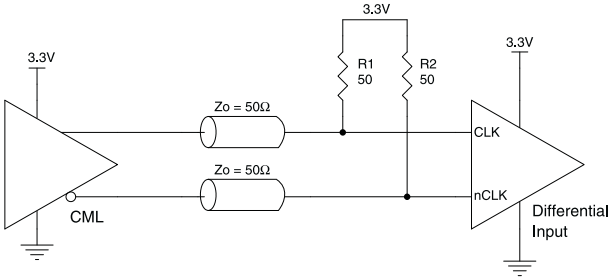


Figure 2E. CLK/nCLK Input Driven by an IDT Open Collector CML Driver



2.5V Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, CML and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 3A to 3E* show interface examples for the IN/nIN input with built-in 50Ω terminations driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

Figure 3A.CLK/nCLK Input Driven by a 2.5V LVPECL Driver

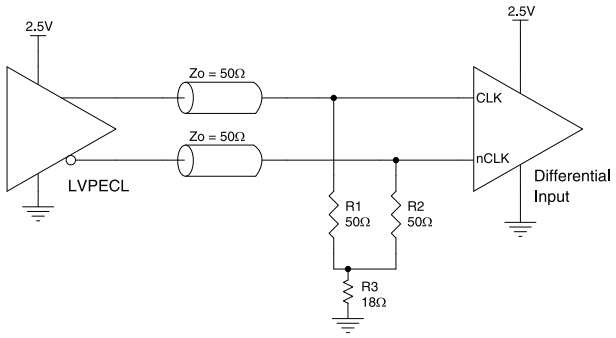


Figure 3B.CLK/nCLK Input Driven by a 2.5V LVPECL Driver

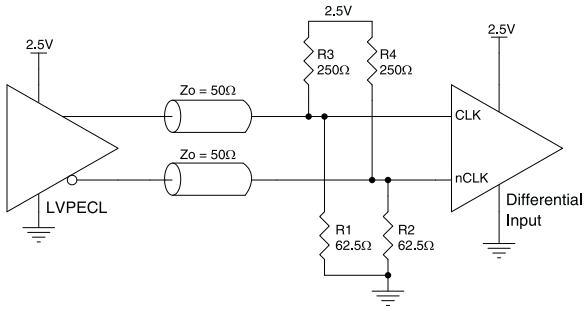


Figure 3C.CLK/nCLK Input Driven by a 2.5V LVDS Driver

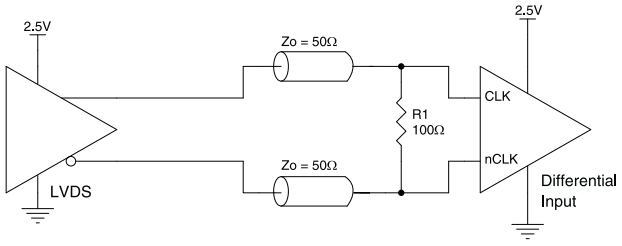


Figure 3D.CLK/nCLK Input Driven by a Built-In Pullup CML Driver

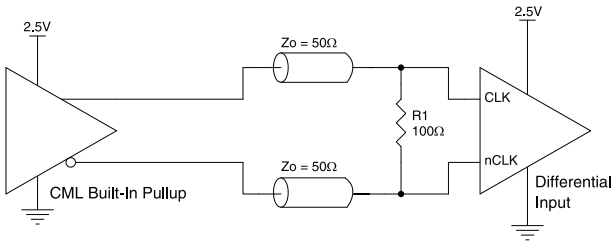
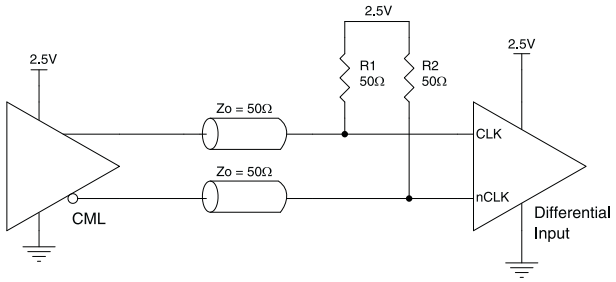


Figure 3E.CLK/nCLK Input Driven by an IDT Open Collector CML Driver



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Recommendations for Unused Output Pins

Inputs

CLK/nCLK Inputs

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

LVCMOS Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs

LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 4A and 4B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

Figure 4A. 3.3V LVPECL Output Termination

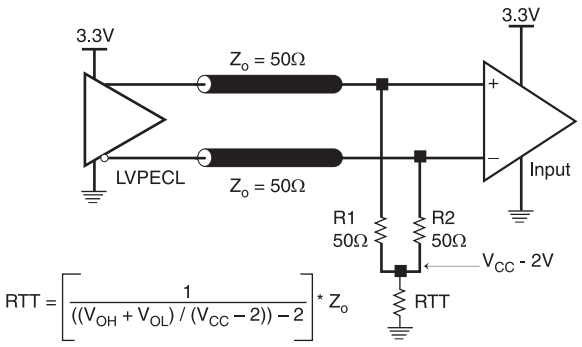
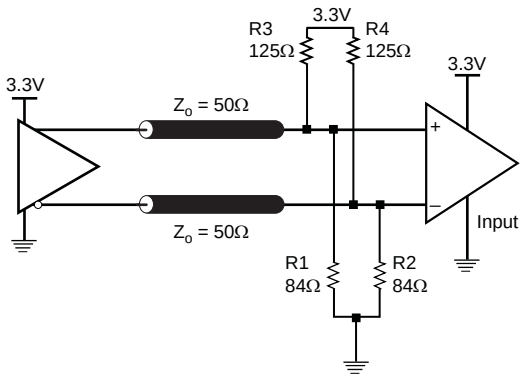


Figure 4B. 3.3V LVPECL Output Termination



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Termination for 2.5V LVPECL Outputs

Figure 5A and *Figure 5B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CC} – 2V. For V_{CC} = 2.5V, the V_{CC} – 2V is very close to ground level. The R3 in Figure 5B can be eliminated and the termination is shown in *Figure 5C.*

Figure 5A. 2.5V LVPECL Driver Termination Example

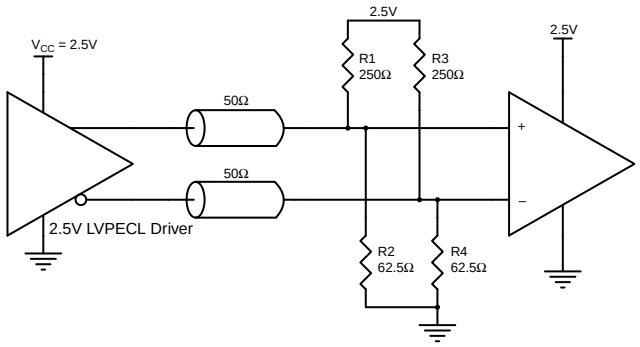


Figure 5B. 2.5V LVPECL Driver Termination Example

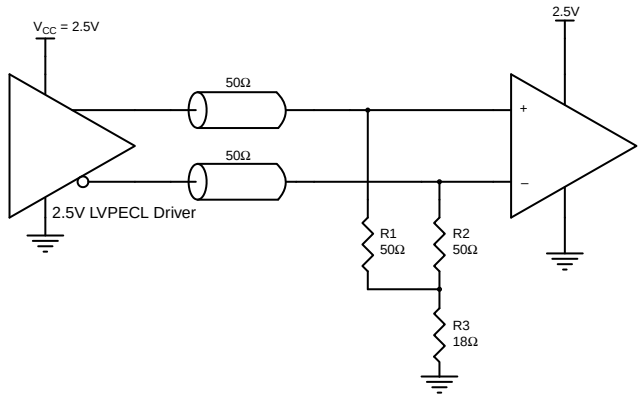
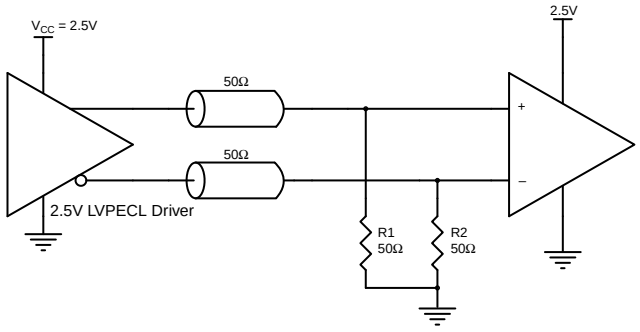


Figure 5C. 2.5V LVPECL Driver Termination Example



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VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 6.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Leadframe Base Package, Amkor Technology.

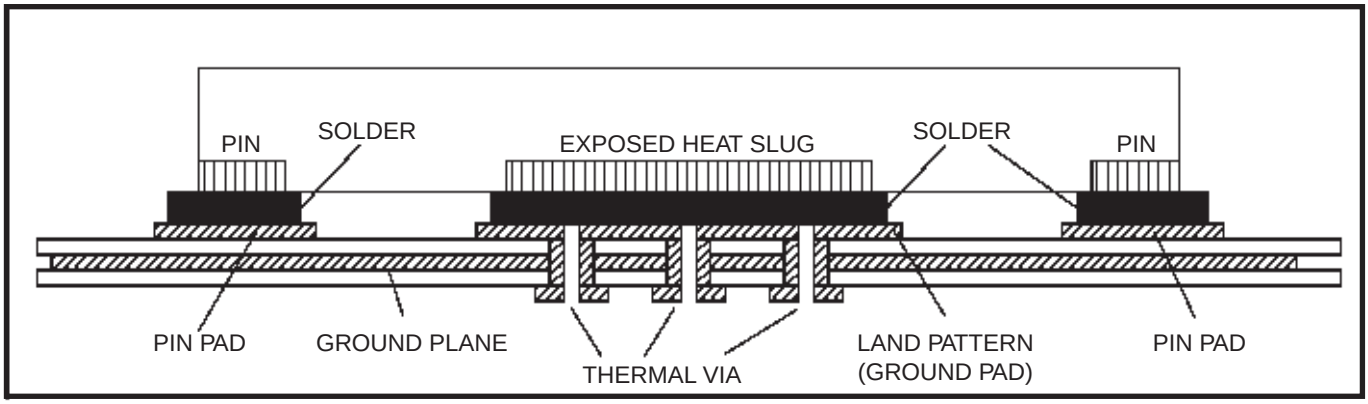


Figure 6. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

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Power Considerations

This section provides information on power dissipation and junction temperature for the ICS853S031I.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS853S031I is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = V_{CC_MAX} * I_{EE_MAX} = 3.465V * 70mA = **242.55mW**
- Power (outputs)$_{MAX}$ = **31.12mW/Loaded Output pair**

Total Power$_{_MAX}$ (3.465V, with all outputs switching) = 242.55mW + 31.12mW = **273.67mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 1 meter per second and a multi-layer board, the appropriate value is 39.5°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.274W * 39.5°C/W = 95.8°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resistance θ_{JA} for 32 Lead VFQFN, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	39.5°C/W	34.5°C/W	31.0°C/W

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3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pairs.

LVPECL output driver circuit and termination are shown in *Figure 7.*

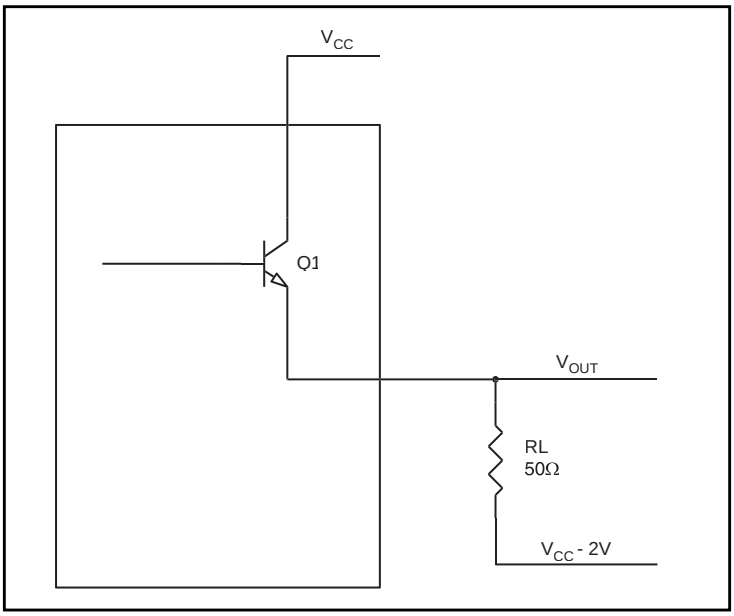


Figure 7. LVPECL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CC} – 2V.

- For logic high, $V_{OUT} = V_{OH_MAX} =$ **V_{CC_MAX} – 0.935V**
  ($V_{CC_MAX} – V_{OH_MAX}$) = **0.935V**
- For logic low, $V_{OUT} = V_{OL_MAX} =$ **V_{CC_MAX} – 1.67V**
  ($V_{CC_MAX} – V_{OL_MAX}$) = **1.67V**

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd_H = [(V_{OH_MAX} – (V_{CC_MAX} – 2V))/R_L] * (V_{CC_MAX} – V_{OH_MAX}) = [(2V – (V_{CC_MAX} – V_{OH_MAX}))/R_L] * (V_{CC_MAX} – V_{OH_MAX}) =$
$[(2V – 0.935V)/50\Omega] * 0.935V =$ **19.92mW**

$Pd_L = [(V_{OL_MAX} – (V_{CC_MAX} – 2V))/R_L] * (V_{CC_MAX} – V_{OL_MAX}) = [(2V – (V_{CC_MAX} – V_{OL_MAX}))/R_L] * (V_{CC_MAX} – V_{OL_MAX}) =$
$[(2V – 1.67V)/50\Omega] * 1.67V =$ **11.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **31.12mW**

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Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 32 Lead VFQFN

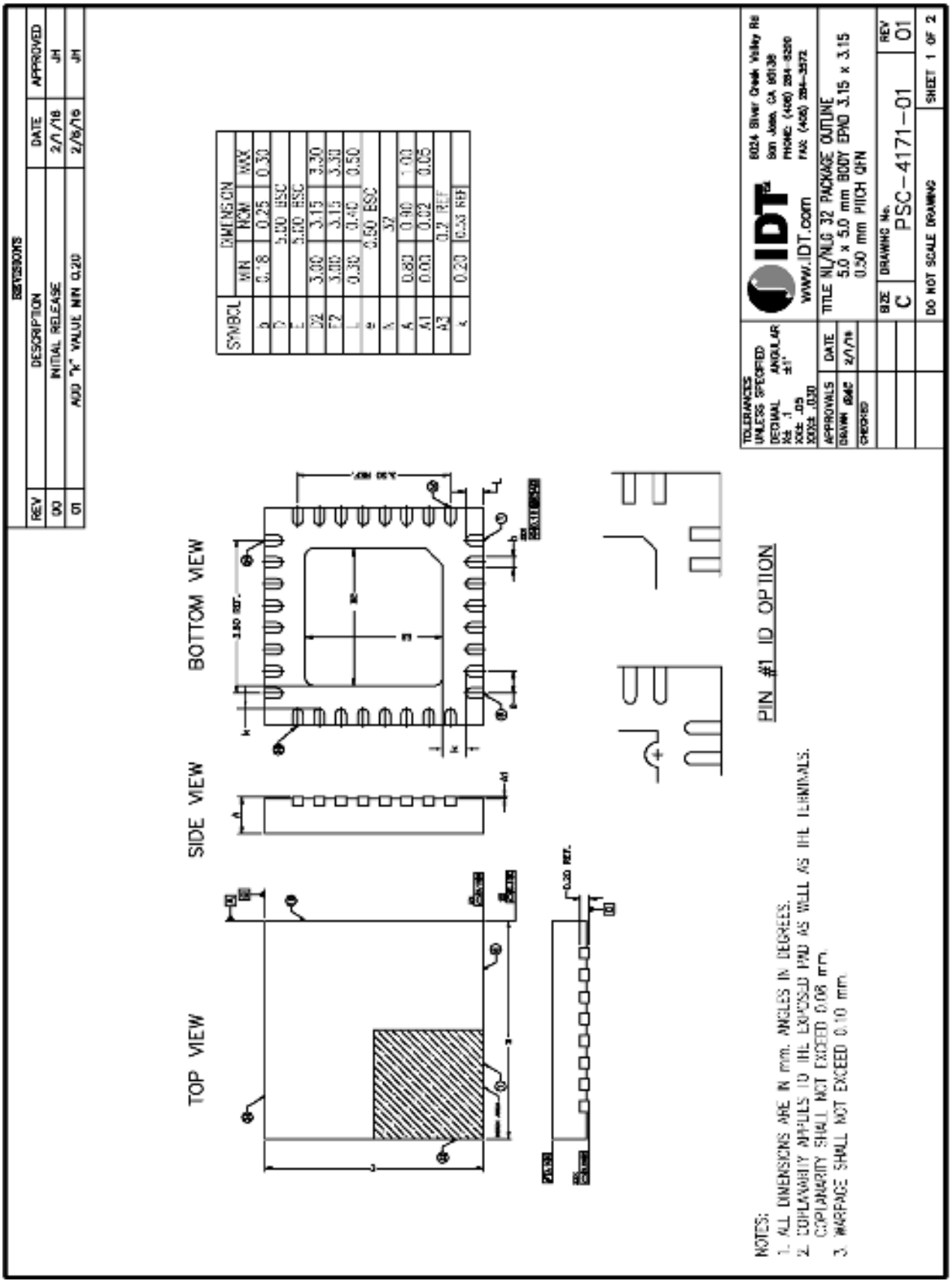
θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	39.5°C/W	34.5°C/W	31.0°C/W

Transistor Count

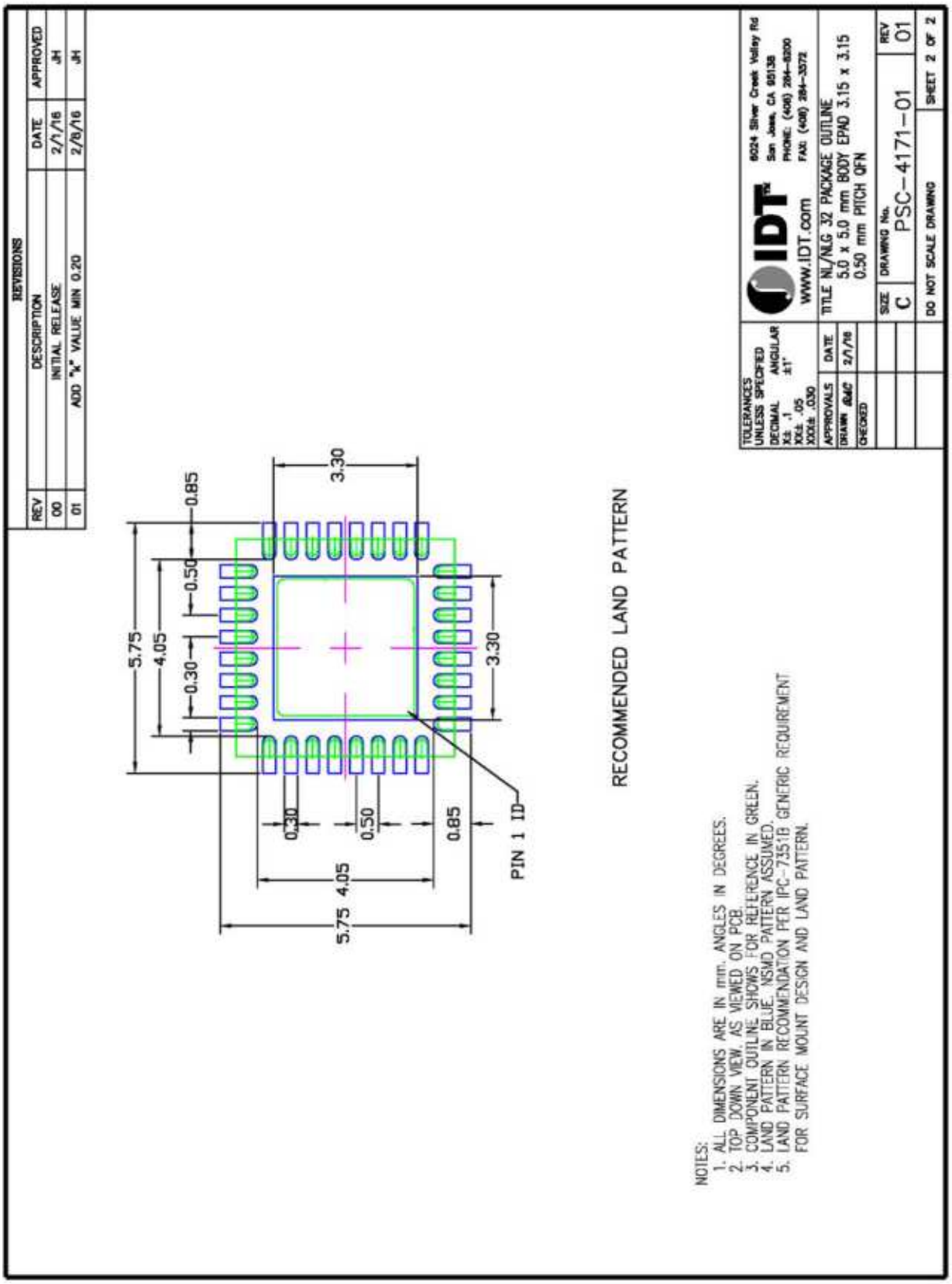
The transistor count for ICS853S031I is: 8264

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Package Outline Drawings – Page 1



Package Outline Drawings – Page 2



Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
853S012AKILF	ICS3S012AIL	Lead-Free, 32 Lead VFQFN	Tray	-40°C to 85°C
853S012AKILFT	ICS3S012AIL	Lead-Free, 32 Lead VFQFN	Tape & Reel	-40°C to 85°C

Revision History

Date	Description of Change
August 23, 2017	Updated the electrical characteristics for t_{PD} in Table 5. Updated the package outline drawings; however, no mechanical changes.
September 28, 2012	Figures 2E, 3E corrected misspelling on Driver
	Removed quantity from Tape and Reel

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

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