A8591

Wide Input Voltage, 2 A Buck Regulator Family with Low-IQ Mode

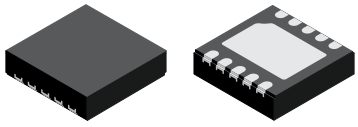
FEATURES AND BENEFITS

- Automotive AEC-Q100 qualified
- Withstands surge input to 40 V_{IN} for load dump
- Operates down to 3.4 V_{IN} (typ), 3.6 V_{IN} (max) for idle stop
- Utilizes pulse-frequency modulation (PFM) for low-IQ mode
- 10 µA Sleep mode (automatic PWM / Low-IQ PFM mode selection)
- Fixed output voltage options: 3.3 or 5 V with ±1% accuracy
- Delivers up to 2 A of output current
- Integrated 110 mΩ high-side MOSFET
- Adjustable switching frequency from 300 kHz to 2.4 MHz
- EMI reduction features:
  - Frequency dithering
  - Controlled switching node
- External synchronization capability
- Maximum duty cycle for low dropout
- Active low NPOR output with 7.5 ms delay
- Pre-bias startup capable: V_{OUT} increases monotonically, does not cause a reset

Continued on the next page…

PACKAGE

10-Pin, 3 × 3 mm Wettable Flank DFN with Exposed Thermal Pad (suffix EJ)



Not to scale

DESCRIPTION

The A8591 is designed to provide the power-supply requirements of next-generation car audio and infotainment systems. The A8591 provides all the control and protection circuitry to produce a high-current regulator with ±1% output voltage accuracy.

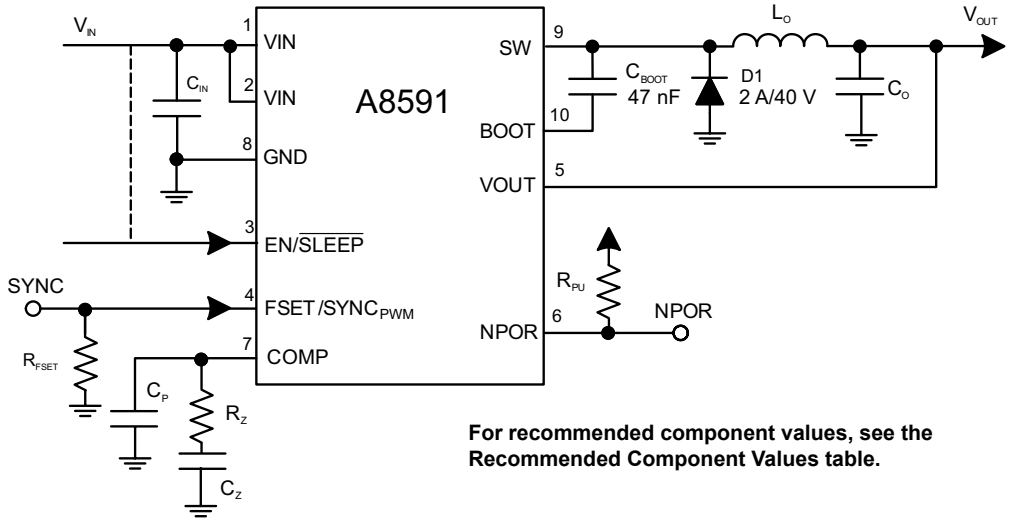
The A8591 employs current-mode control to provide simple compensation, excellent stability, and fast transient response. The A8591 employs pulse-frequency modulation (PFM) to draw less than 33 µA from 12 V_{IN} while supplying 5 V/40 µA (A8591, 5 V_{OUT}), or less than 24 µA from 12 V_{IN} while supplying 3.3 V/40 µA (A8591-1, 3.3 V_{OUT}). When operational, the A8591 operates down to at least 3.6 V_{IN} (V_{IN} falling). The Sleep feature allows for very low standby current.

Features of the A8591 include a programmable PWM switching frequency. The regulator switching frequency can be synchronized to an external clock. The A8591 has external compensation to optimize stability and transient response for a wide range of external components and applications. The A8591 has a fixed soft-start time of 5 ms.

Continued on the next page…

APPLICATIONS

- Automotive:
  - Instrument clusters
  - Audio systems
  - Navigation
  - HVAC
- Home audio
- Network and telecom
- Industrial



For recommended component values, see the Recommended Component Values table.

Typical Application Diagram

FEATURES AND BENEFITS (CONTINUED)

- External compensation for maximum flexibility
- Stable with ceramic or electrolytic output capacitors
- Internally fixed soft-start time of 5 ms
- Pulse-by-pulse current limit, hiccup mode short-circuit, and thermal protections
- Pin open/short and component fault tolerant
- –40°C to 150°C operating junction temperature range
- Thermally enhanced DFN-10 surface-mount package

DESCRIPTION (CONTINUED)

Extensive protection features of the A8591 include pulse-by-pulse current limit, hiccup mode short-circuit protection, open/short asynchronous diode protection, BOOT open/short voltage protection, V_{IN} undervoltage lockout, and thermal shutdown.

The A8591 is supplied in a 10-pin wettable-flank dual-flat no-leads (DFN) package (suffix EJ) with exposed power pad. It is lead (Pb) free, with 100% matte tin leadframe plating.

Selection Guide

Part Number	Packing [1]	Output Voltage Option
A8591KEJTR-J	1500 pieces per 7-in. reel	5 V compatible
A8591KEJTR-J-1	1500 pieces per 7-in. reel	3.3 V compatible

[1] For additional packing options, contact Allegro.

Table of Contents

Features and Benefits 1
Description 1
Package 1
Applications 1
Typical Application Diagram 1
Selection Guide 2
Specifications 3
  Absolute Maximum Ratings 3
  Thermal Characteristics 3
Functional Block Diagram 4
Pinout Diagram and Terminal List Table 5
Electrical Characteristics 6
Characteristic Performance 10
  Overview 13
  Reference Voltage 13
  PWM Switching Frequency 13
  EN/SLEEP Input 13
  PWM Synchronization 14
  Transconductance Error Amplifier 14
  Slope Compensation 14
  Current-Sense Amplifier 14
  Power MOSFETs 14
  BOOT Regulator 14
  Pulse-Width Modulation (PWM) Mode 15
  Low-IQ Pulse-Frequency Modulation (PFM) Mode 15
  Soft-Start (Startup) and Inrush Current Control 16
  Pre-Biased Startup 17
  Active-Low Power-On Reset (NPOR) Output 17
  Slope Compensation 17
Design and Component Selection 21
  PWM Switching Frequency (R_{FSET}) 21
  Output Inductor (L_O)Output 21
  Output Capacitors 22
  Low-IQ PFM Output Voltage Ripple Calculation 23
  Input Capacitors 24
  Asynchronous Diode (D1) 25
  Bootstrap Capacitor 25
  Compensation Components (R_Z, C_Z, and C_P) 25
  Generalized Tuning Procedure 27
Power Dissipation and Thermal Calculations 29
PCB Component Placement and Routing 30
Package Outline Drawing 32
Revision History 33

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

SPECIFICATIONS

Absolute Maximum Ratings [1]

Characteristic	Symbol	Notes	Rating	Unit
Input Voltage (VIN pins)	V_{IN}		–0.3 to 40	V
Switching Node Voltage (SW pin)	V_{SW}	Continuous; rating is a function of temperature	–0.3 to V_{IN} + 0.3	V
		t < 50 ns	–1.0 to V_{IN} + 3	V
BOOT Pin Voltage	V_{BOOT}	Continuous	V_{SW} – 0.3 to V_{SW} + 5.5	V
		BOOT pin overvoltage fault condition	V_{SW} – 0.3 to V_{SW} + 7	V
VOUT Pin Voltage	V_{OUT}	Continuous	–0.3 to 5.5	V
		VOUT pin overvoltage fault condition	–0.3 to 7	V
EN/$\overline{\text{SLEEP}}$ Pin Voltage	$V_{EN/\overline{SLEEP}}$		–0.3 to V_{IN} + 0.3	V
All other pins			–0.3 to 5.5	V
Maximum Junction Temperature	T_J(max)		150	°C
Storage Temperature	T_{stg}		–55 to 150	°C

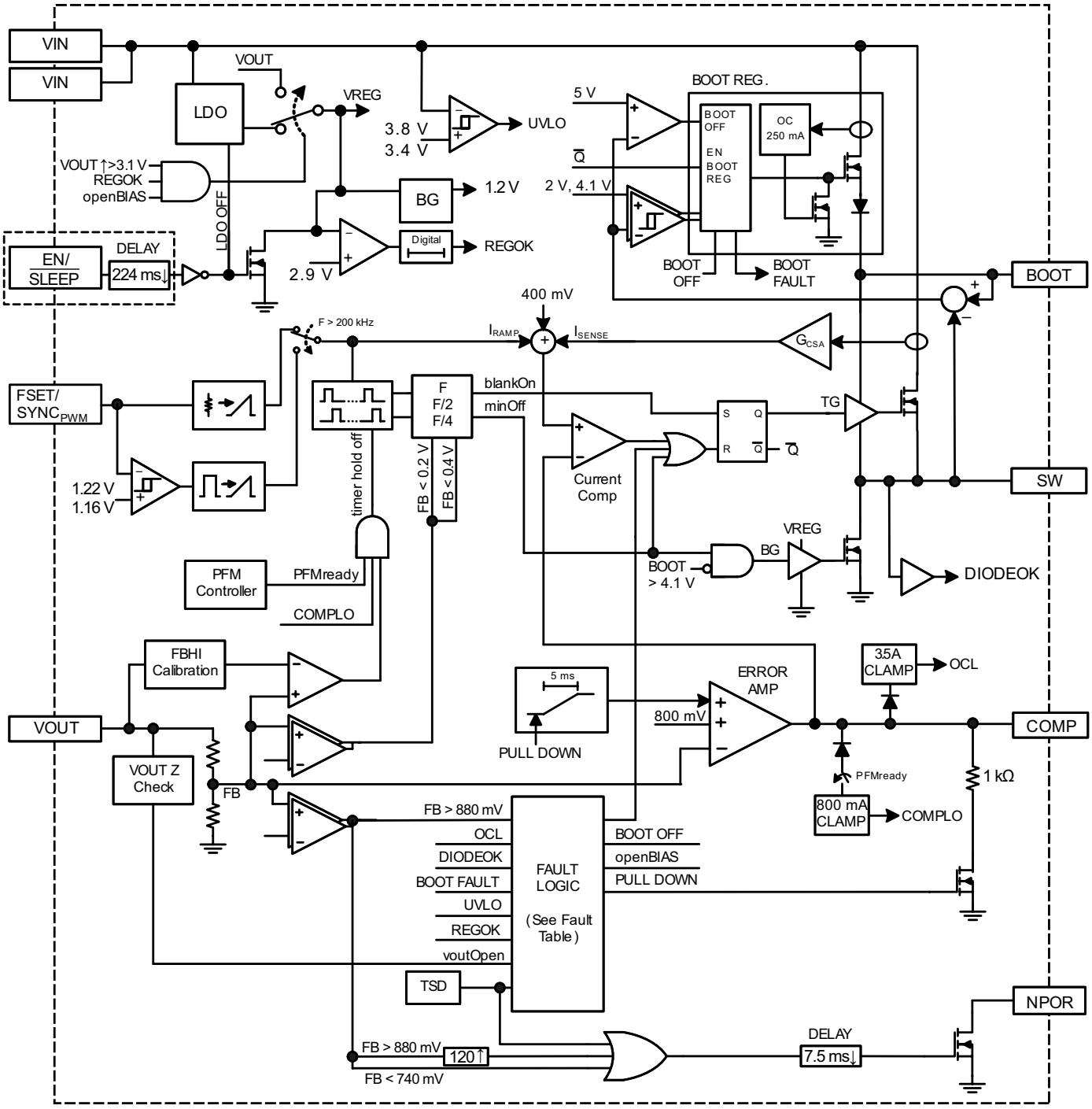
[1] Operation at levels beyond the ratings listed in this table may cause permanent damage to the device. The absolute maximum ratings are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the Electrical Characteristics table is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

Thermal Characteristics: May require derating at maximum conditions; see Power Dissipation and Thermal Calculations section

Characteristic	Symbol	Test Conditions [1]	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	On 4-layer PCB based on JEDEC standard	45	°C/W

[1] Additional thermal information available on the Allegro website.

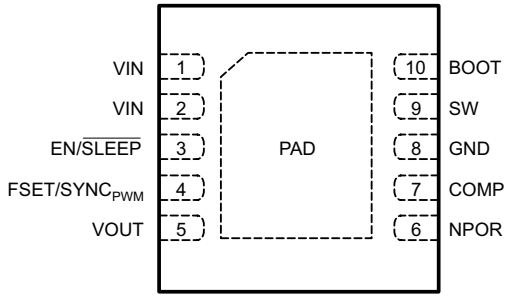
Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com



Functional Block Diagram

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

PINOUT DIAGRAM AND TERMINAL LIST TABLE



EJ Package, 10-Pin 3 × 3 mm DFN Pinouts

Terminal List Table

Number	Name	Function
1, 2	VIN	Power input for the control circuits and the drain of the internal high-side N-channel MOSFET. Connect this pin to a power supply of 4 to 35 V. A high-quality, high-frequency ceramic capacitor should be placed and grounded very close to this pin.
3	EN/$\overline{\text{SLEEP}}$	This pin must be set high to enable the device. If this pin is set low, the device enters a very-low-current shutdown or sleep state (V_{OUT} = 0 V). If the application does not require a sleep mode, this pin can be tied directly to VIN. Do not float this pin.
4	FSET/SYNC$_{PWM}$	Frequency setting and PWM synchronization pin. A resistor, R_{FSET}, from this pin to GND sets the PWM switching frequency. To determine the value of R_{FSET}, see the Design and Component Selection section (Figure 11 and/or Equation 1). Applying a clock signal to this pin forces PWM mode and synchronizes the PWM switching frequency.
5	VOUT	Connect this pin to the output of the regulator. This pin supplies internal circuitry when its voltage level is high enough. Also, through an on-chip voltage divider, this pin connects to the negative feedback input of the error amplifier. Keep the VOUT pin quiet and Kelvin connect.
6	NPOR	Active-low, power-on reset output signal. This pin is an open-drain output that transitions from low to high impedance after the output has maintained regulation for t_{dPOR}.
7	COMP	Output of the error amplifier, and compensation node for the current-mode control loop. For loop compensation, connect a series RC network from this pin to GND. For further details, see the Design and Component Selection section of this datasheet.
8	GND	Ground pin.
9	SW	The source for the internal high-side N-channel MOSFET. The external freewheeling diode (D_1) and output inductor (L_O) should be connected to this pin. Both D_1 and L_O should be placed close to this pin and connected with relatively wide traces.
10	BOOT	High-side gate drive boost input. This pin supplies the drive for the high-side N-channel MOSFET. Connect a 47 nF ceramic capacitor from BOOT to SW.
–	PAD	Exposed pad of the package providing enhanced thermal dissipation. This pad must be connected to the ground plane(s) of the PCB with at least six vias, directly in the pad.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

ELECTRICAL CHARACTERISTICS: Valid at 4 V ≤ V_{IN} ≤ 35 V, −40°C ≤ T_A = T_J ≤ 150°C, typical values at T_J = 25°C, unless otherwise specified

Characteristic	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
INPUT VOLTAGE							
Input Voltage Range [1]	V_{IN}			4	–	35	V
VIN Undervoltage Lockout Start Threshold [2]	$V_{UVLO(ON)}$	V_{IN} rising		3.6	3.8	4	V
VIN Undervoltage Lockout Stop Threshold	$V_{UVLO(OFF)}$	V_{IN} falling		3.2	3.4	3.6	V
VIN Undervoltage Hysteresis	$V_{UVLO(HYS)}$			–	400	–	mV
INPUT SUPPLY CURRENT							
Input Supply Current (Not in PFM) [1]	I_{IN}	I_{OUT} = 0 mA		–	2.5	3.5	mA
Input Supply Current (Low-IQ PFM) [1][3][4]	I_{LO_IQ}	A8591, V_{IN} = 12 V, V_{OUT} = 5 V	I_{OUT} = no load, T_A = 25°C	–	10	14	µA
			I_{OUT} = no load, T_A = 65°C	–	15	–	µA
			I_{OUT} = 40 µA, T_A = 25°C	–	28	33	µA
			I_{OUT} = 40 µA, T_A = 65°C	–	33	–	µA
		A8591-1, V_{IN} = 12 V, V_{OUT} = 3.3 V	I_{OUT} = no load, T_A = 25°C	–	7	10	µA
			I_{OUT} = no load, T_A = 65°C	–	12	–	µA
			I_{OUT} = 40 µA, T_A = 25°C	–	20	24	µA
			I_{OUT} = 40 µA, T_A = 65°C	–	25	–	µA
Input Supply Current (Sleep Mode) [1]	$I_{IN(SLEEP)}$	$V_{EN/\overline{SLEEP}}$ = 0 V, T_J ≤ 85°C, V_{IN} = 16 V		–	5	15	µA
		$V_{EN/\overline{SLEEP}}$ = 0 V, T_J ≤ 85°C, V_{IN} = 35 V		–	7	25	µA
VOLTAGE REGULATION							
Output Voltage Accuracy [4]	E_{VOUT} (5.0V)	A8591	0°C < T_J < 85°C, V_{OUT} = 4 × V_{COMP}	4.95	5	5.05	V
			–40°C < T_J < 150°C, V_{OUT} = 4 × V_{COMP}	4.925	5	5.075	V
	E_{VOUT} (3.3V)	A8591-1	0°C < T_J < 85°C, V_{OUT} = 2 × V_{COMP}	3.267	3.3	3.333	V
			–40°C < T_J < 150°C, V_{OUT} = 2 × V_{COMP}	3.25	3.3	3.35	V
Low IQ Ripple [3][4]	$V_{PP(LO_IQ)}$	8 V < V_{IN} < 12 V		–	25	65	mV_{PP}
Low IQ Peak Current Threshold	$I_{PEAK(LO_IQ)}$			640	800	930	mA_{PEAK}
Output Dropout Voltage [4]	$V_{OUT(SAT)}$	T_A = 85°C, DCR_{LO} ≤ 75 mΩ, V_{IN} = 4 V, I_{OUT} = 1 A, f_{SW} = 425 kHz		3.27	3.295	–	V
		T_A = 85°C, DCR_{LO} ≤ 75 mΩ, V_{IN} = 5.75 V, I_{OUT} = 1 A, f_{SW} = 425 kHz		4.94	5	–	V
		T_A = 85°C, DCR_{LO} ≤ 50 mΩ, V_{IN} = 4.25 V, I_{OUT} = 1 A, f_{SW} = 2 MHz		3.25	3.3	–	V
		T_A = 85°C, DCR_{LO} ≤ 50 mΩ, V_{IN} = 6 V, I_{OUT} = 1 A, f_{SW} = 2 MHz		4.89	5	–	V

Continued on the next page…

[1] Negative current is defined as coming out of the node or pin, positive current is defined as going into the node or pin.
[2] Thermally limited depending on input voltage, output voltage, duty cycle, regulator load currents, PCB layout, and airflow.
[3] Configured as shown in Typical Application Diagram.
[4] Ensured by design and characterization, not production tested.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

ELECTRICAL CHARACTERISTICS (continued): Valid at 4 V ≤ V_{IN} ≤ 35 V, −40°C ≤ T_A = T_J ≤ 150°C, typical values at T_J = 25°C, unless otherwise specified

Characteristic	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
ERROR AMPLIFIER							
Open-Loop Voltage Gain	A_{VOL}	V_{COMP} = 1.2 V		–	65	–	dB
Transconductance with On-Chip Resistor Divider Included	$g_{m(5V)}$	A8591	2.5 V < V_{OUT}	88	120	152	µA/V
			0 V < V_{OUT} < 2.5 V	46.4	64	81.6	µA/V
	$g_{m(3.3V)}$	A8591-1	1.65 V < V_{OUT}	133.3	181.8	230.3	µA/V
			0 V < V_{OUT} < 1.65 V	70.3	97	123.6	µA/V
Output Current	I_{EA}	V_{COMP} = 1.2 V		–	±75	–	µA
INTERNAL MOSFET PARAMETERS [1]							
High-Side MOSFET On-Resistance	$R_{DS(on)HS}$	T_J = 25°C, V_{BOOT} – V_{SW} = 4.5 V, I_{DS} = 1 A		–	110	–	mΩ
High-Side MOSFET Leakage Current [2][3]	I_{LKGHS}	T_J < 85°C, $V_{EN/\overline{SLEEP}}$ ≤ 0.8 V, V_{SW} = 0 V, V_{IN} = 16 V		–	–	10	µA
SW Node Rising/Falling Slew Rate [3]	SR	V_{IN} = 12 V, I_{OUT} = 1 A		–	0.72	–	V/ns
Low-Side MOSFET On-Resistance	$R_{DS(on)LS}$	T_J = 25°C, V_{IN} ≥ 6 V, I_{DS} = 0.1 A		–	–	10	Ω
BOOT REGULATOR							
BOOT Voltage Enable Threshold	$V_{BOOT(TH)}$	V_{BOOT} rising		1.8	2	2.2	V
BOOT Voltage Enable Hysteresis	$V_{BOOT(HYS)}$			–	400	–	mV
OSCILLATOR AND PWM TIMING							
PWM Switching Frequency	f_{OSC}	R_{FSET} = 86.6 kΩ		270	300	330	kHz
		R_{FSET} = 61.9 kΩ		373	415	457	kHz
		R_{FSET} = 9.31 kΩ		1.8	2	2.2	MHz
PWM Frequency Dithering	f_{DITHER}	No dithering with synchronization		–	±7.5	–	%
Minimum Controllable On-Time	$t_{ON(MIN)}$	V_{IN} = 12 V, I_{OUT} = 1 A		–	85	125	ns
Minimum Switch Off-Time	$t_{OFF(MIN)}$	V_{IN} = 12 V, I_{OUT} = 1 A		–	85	125	ns
FSET/SYNC$_{PWM}$ SYNCHRONIZATION TIMING							
Synchronization Frequency Range	f_{SW_MULT}			0.375	–	2.4	MHz
Synchronization Input Duty Cycle	D_{SYNC}			–	–	80	%
Synchronization Input Pulse Width	t_{wSYNC}			200	–	–	ns
Synchronization Input Rise Time [3]	t_{rSYNC}			–	10	15	ns
Synchronization Input Fall Time [3]	t_{fSYNC}			–	10	15	ns
Synchronization Rising Threshold [3]	$V_{SYNC(LO)}$	$V_{FSET/SYNCPWM}$ rising		–	–	1.5	V
Synchronization Falling Threshold [3]	$V_{SYNC(HI)}$	$V_{FSET/SYNCPWM}$ falling		0.9	–	–	V

Continued on the next page…

[1] Thermally limited depending on input voltage, output voltage, duty cycle, regulator load currents, PCB layout, and airflow.
[2] Negative current is defined as coming out of the node or pin, positive current is defined as going into the node or pin.
[3] Ensured by design and characterization, not production tested.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

ELECTRICAL CHARACTERISTICS (continued): Valid at 4 V ≤ V_{IN} ≤ 35 V, −40°C ≤ T_A = T_J ≤ 150°C, typical values at T_J = 25°C, unless otherwise specified

Characteristic	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
CURRENT CONTROL LOOP							
PWM Pulse-by-Pulse Limit	$I_{LIM(TONMIN)}$	t_{ON} = $t_{ON(MIN)PWM}$, 4 V ≤ V_{IN} ≤ 16 V		3	3.5	4	A
	$I_{LIM(TONMAX)}$	t_{ON} = (1 / f_{SW}) – $t_{OFF(MIN)PWM}$, no PWM synchronization		2	2.6	3	A
COMP to SW Current Gain	g_{mPOWER}			–	3	–	A/V
Slope Compensation	S_E	During synchronization		–	0.35	–	A/µs
		R_{FSET} = 86.6 kΩ		0.18	0.25	0.34	A/µs
		R_{FSET} = 61.9 kΩ		0.25	0.34	0.45	A/µs
		R_{FSET} = 9.31 kΩ		1.6	2	2.4	A/µs
SOFT-START							
Soft-Start Ramp Time	t_{SS}			2.5	5	7.5	ms
Soft-Start Switching Frequency	$f_{SS(5.0V)}$	A8591	0 V < V_{OUT} < 1.25 V	–	f_{OSC}/4	–	–
			1.25 V < V_{OUT} < 2.5 V	–	f_{OSC}/2	–	–
			2.5 V < V_{OUT}	–	f_{OSC}	–	–
	$f_{SS(3.3V)}$	A8591-1	0 V < V_{OUT} < 0.825 V	–	f_{OSC}/4	–	–
			0.825 V < V_{OUT} < 1.65 V	–	f_{OSC}/2	–	–
			1.65 V < V_{OUT}	–	f_{OSC}	–	–
HICCUP MODE							
Hiccup Off-Time	HIC_{OFF}	All hiccup faults such as VOUT shorted to GND		–	20	–	ms
Hiccup Overcurrent Protection (OCP) Count	OCP_{LIM}	t > t_{SS}, OCP pulses		–	120	–	counts
Hiccup BOOT Shorted Count	$BOOT_{UV}$			–	64	–	counts
Hiccup BOOT Open Count	$BOOT_{OV}$			–	7	–	counts
THERMAL PROTECTION							
Thermal Shutdown Threshold (Rising) [1]	T_{SDth}	PWM stops immediately, COMP is pulled low, and soft-start is reset		155	170	–	°C
Thermal Shutdown Hysteresis [1]	T_{SDHYS}			–	20	–	°C

Continued on the next page…

[1] Ensured by design and characterization; not production tested.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

ELECTRICAL CHARACTERISTICS (continued): Valid at 4 V ≤ V_{IN} ≤ 35 V, −40°C ≤ T_A = T_J ≤ 150°C, typical values at T_J = 25°C, unless otherwise specified

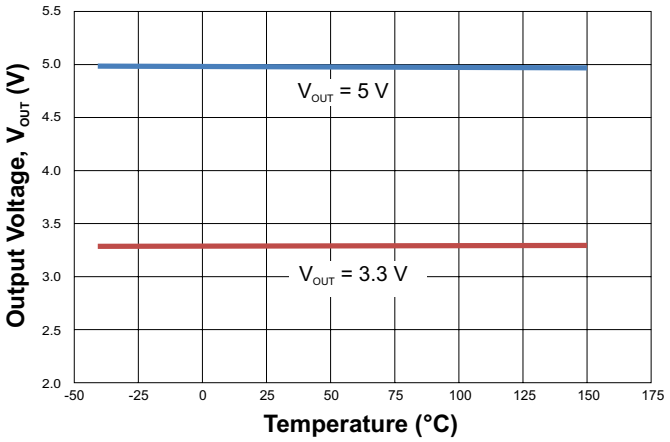
Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Power-On Reset (NPOR) Output						
NPOR Overvoltage Threshold, 5 V	$V_{NPOROV(5V)}$	V_{OUT} rising	5.37	5.5	5.75	V
NPOR Overvoltage Hysteresis, 5 V	$V_{NPOROV(HYS)(5V)}$	V_{OUT} falling, relative to V_{NPOROV}	–	–60	–	mV
NPOR Undervoltage Threshold, 5 V	$V_{NPORUV(5V)}$	V_{OUT} falling	4.45	4.62	4.75	V
NPOR Undervoltage Hysteresis, 5 V	$V_{NPORUV(HYS)(5V)}$	V_{OUT} rising, relative to V_{NPORUV}	–	60	–	mV
NPOR Overvoltage Threshold, 3.3 V	$V_{NPOROV(3.3V)}$	V_{OUT} rising	3.54	3.63	3.75	V
NPOR Overvoltage Hysteresis, 3.3 V	$V_{NPOROV(HYS)(3.3V)}$	V_{OUT} falling, relative to V_{NPOROV}	–	–40	–	mV
NPOR Undervoltage Threshold, 3.3 V	$V_{NPORUV(3.3V)}$	V_{OUT} falling	2.93	3.05	3.14	V
NPOR Undervoltage Hysteresis, 3.3 V	$V_{NPORUV(HYS)(3.3V)}$	V_{OUT} rising, relative to V_{NPORUV}	–	40	–	mV
NPOR Overvoltage Delay	t_{dPOV_POR}	V_{OUT} falling beyond V_{NPOROV}	–	120	–	counts
NPOR Delay to Rising Edge	t_{dPOR}	V_{OUT} rising only	5	7.5	10	ms
NPOR Low Output Voltage	V_{POROL}	I_{NPOR} = 4 mA	–	200	400	mV
NPOR Leakage	I_{LKGPOR}	V_{NPOR} = 5.5 V	–	–	1.2	µA
EN/$\overline{\text{SLEEP}}$ PIN INPUT THRESHOLDS						
EN/$\overline{\text{SLEEP}}$ Threshold (High) [1]	$V_{SLEEPVIH}$	$V_{EN/\overline{SLEEP}}$ rising	–	1.3	2.1	V
EN/$\overline{\text{SLEEP}}$ Threshold (Low)	$V_{SLEEPVIL}$	$V_{EN/\overline{SLEEP}}$ falling	0.5	1.2	–	V
EN/$\overline{\text{SLEEP}}$ Delay	t_{dSLEEP}	$V_{EN/\overline{SLEEP}}$ transitioning low	115	224	400	µs
EN/$\overline{\text{SLEEP}}$ Input Bias Current [1]	$I_{BIASSLEEP}$	$V_{EN/\overline{SLEEP}}$ = 5 V	–	500	–	nA

[1] Negative current is defined as coming out of the node or pin, positive current is defined as going into the node or pin.

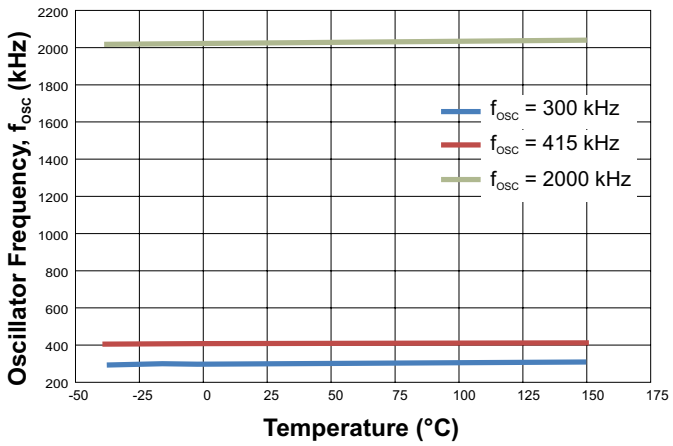
Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

CHARACTERISTIC PERFORMANCE

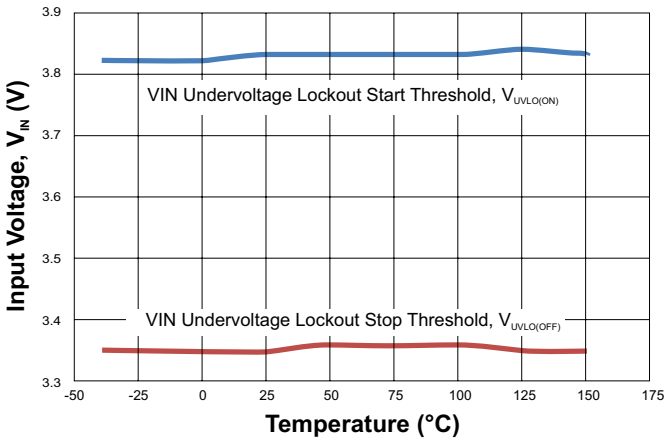
Output Voltage versus Temperature



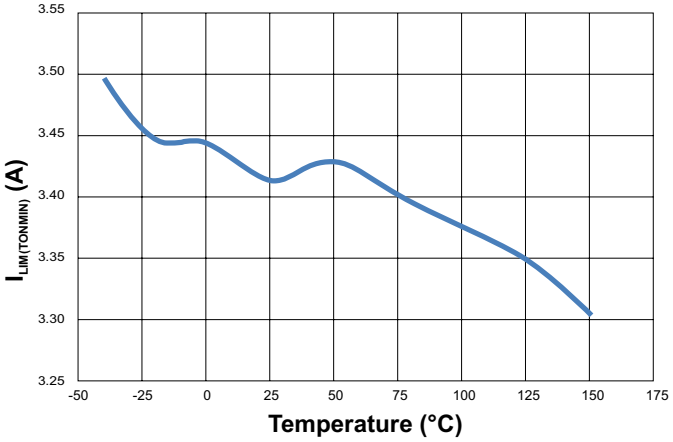
Switching Frequency versus Temperature



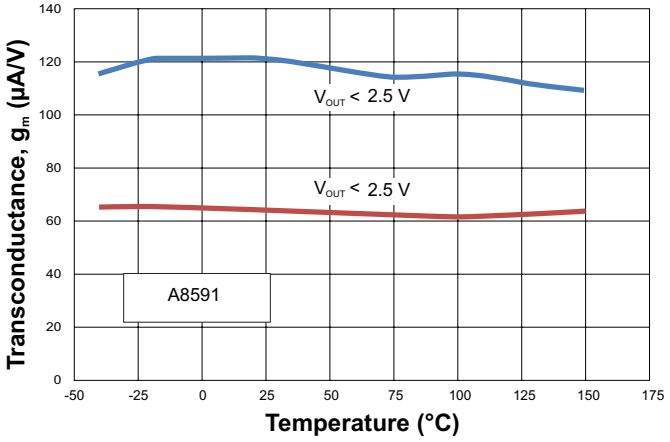
VIN UVLO Start and Stop Thresholds versus Temperature



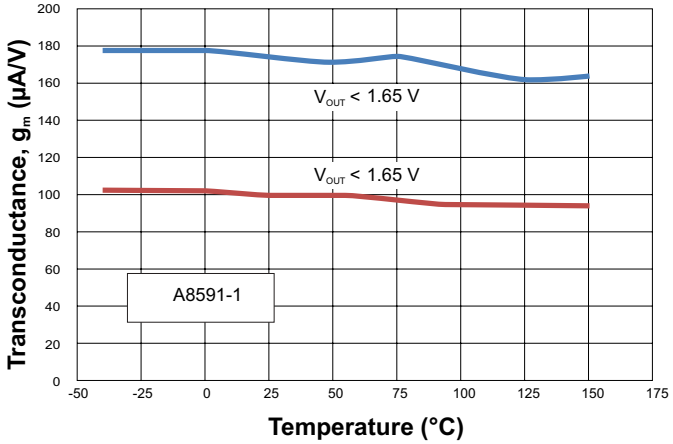
Pulse-by-Pulse Current Limit at $t_{ON(MIN)}$ versus Temperature



Error Amplifier Transconductance versus Temperature

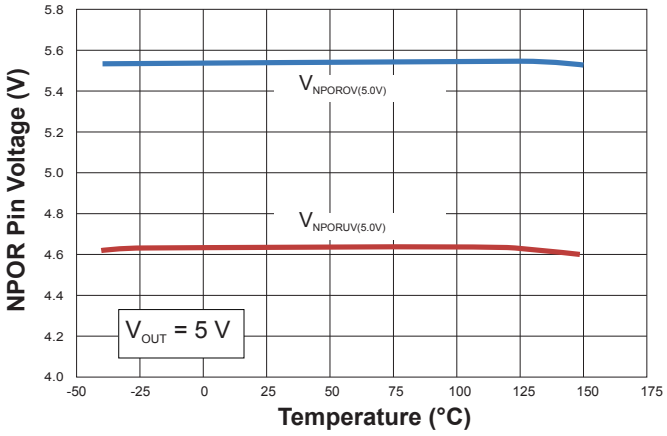


Error Amplifier Transconductance versus Temperature

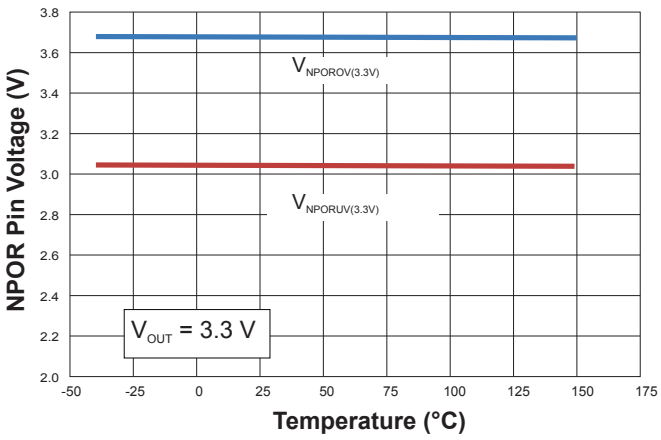


Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

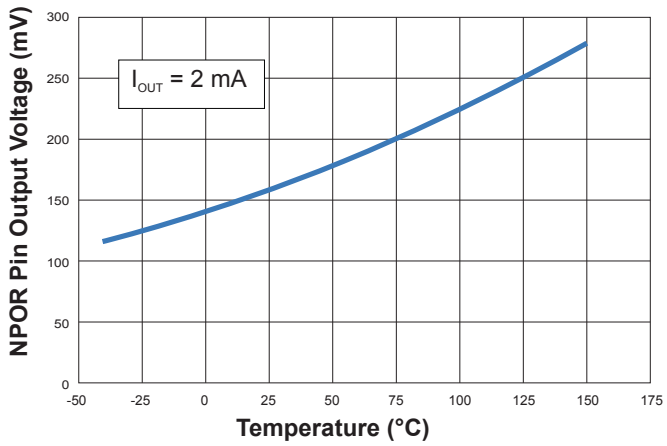
NPOR Overvoltage and Undervoltage Thresholds versus Temperature



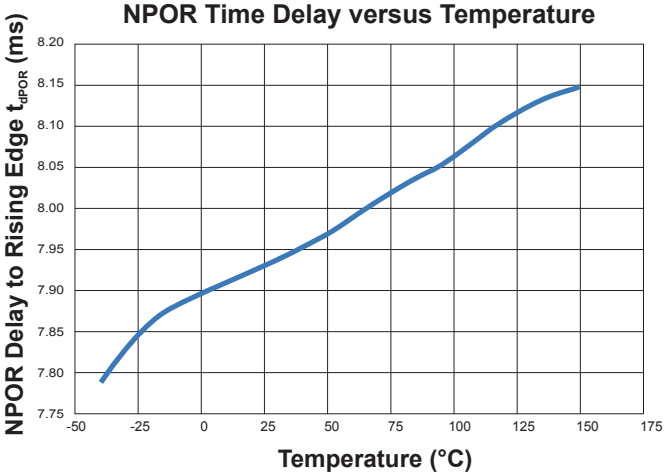
NPOR Overvoltage and Undervoltage Thresholds versus Temperature



NPOR Low Output Voltage versus Temperature



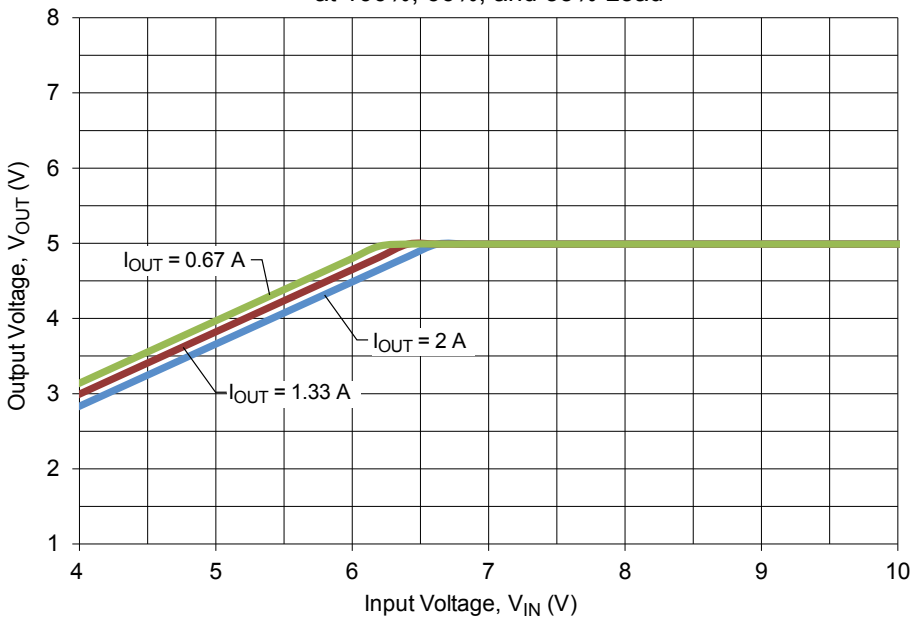
NPOR Time Delay versus Temperature



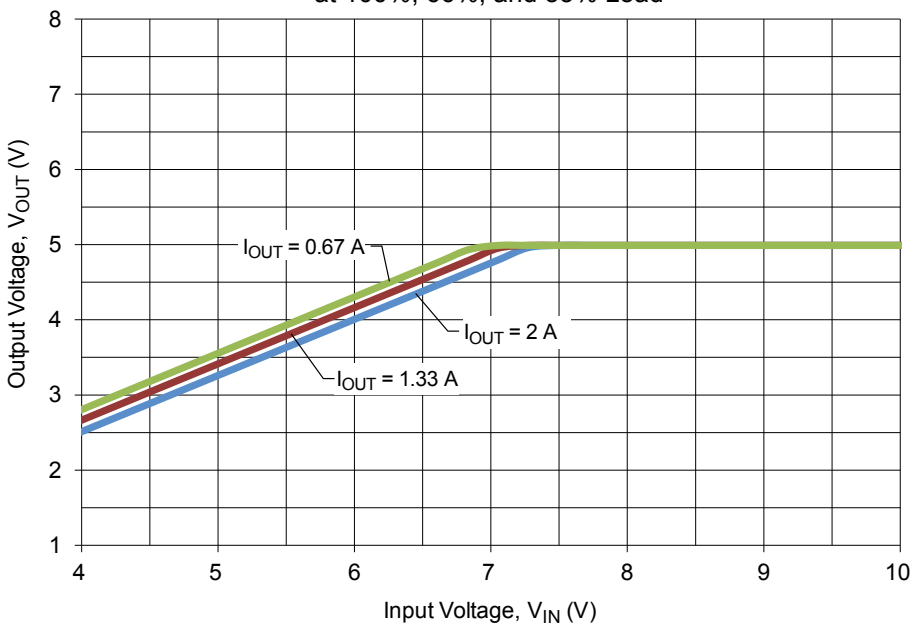
Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

DROPOUT OPERATION—TYPICAL AND WORST-CASE OPERATION

Typical Output Voltage versus Input Voltage at High Ambient
at 100%, 66%, and 33% Load



Worst-Case Output Voltage versus Input Voltage at High Ambient
at 100%, 66%, and 33% Load



Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

FUNCTIONAL DESCRIPTION

Overview

The A8591 family of current-mode buck regulators incorporates all the control and protection circuitry necessary to provide the power-supply requirements of car audio and infotainment systems.

The A8591 family consists of two parts:

- A8591 (5 V output voltage)
- A8591-1 (3.3 V output voltage)

The A8591 family has three modes of operation:

- Pulse-width modulation (PWM) mode, delivering up to 2 A.
- Low-IQ pulse-frequency modulation (PFM) mode, drawing only approximately 10 µA from V_{IN} while maintaining V_{OUT} (at no load). Under most conditions, Low-IQ PFM mode is typically capable of supporting up to approximately 100 mA, depending on applications.
- The third mode of operation is entered when the EN/$\overline{\text{SLEEP}}$ pin is set to 0. The device enters an ultralow-current shutdown mode. V_{OUT} = 0 V and the total current drawn from V_{IN} is less than 10 µA (typ).

In PFM mode, the device operates with lower switching frequency to achieve higher efficiency at light load. When the load is heavy, the device automatically transitions into PWM mode to support a relatively higher current.

The A8591 family is designed to support up to 2 A output. However, the exact amount of current it supplies before possible thermal shutdown depends heavily on duty cycle, ambient temperature, airflow, PCB layout, and PCB construction. Calculated current ratings versus ambient temperature is shown in Figure 3 for V_{IN} = 12 V and V_{OUT} = 3.3 V, and for V_{IN} = 12 V and V_{OUT} = 5 V, each at 300 kHz and 2 MHz. This analysis assumes a 4-layer PCB according to the JEDEC standard (45°C/W), no nearby heat sources, and no airflow.

Reference Voltage

The output voltage from the device regulator is directly connected to the VOUT pin and is divided down internally to 800 mV by an internal resistor divider inside the regulator, as shown in the Functional Block Diagram. The A8591 has a fixed 5 V output voltage; the A8591-1 has a fixed 3.3 V output voltage.

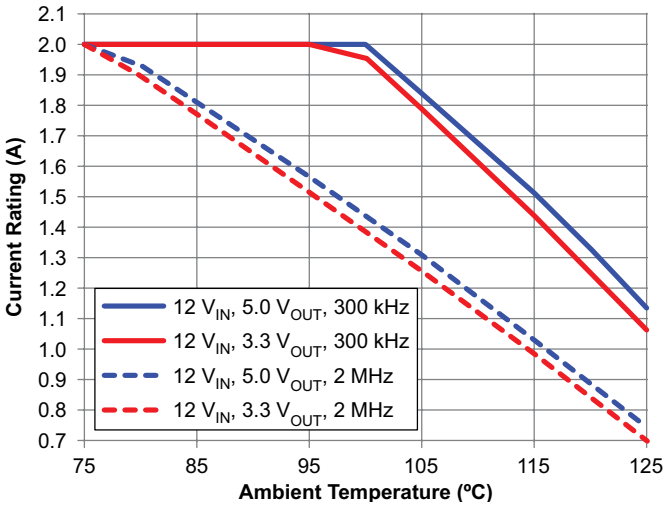


Figure 3: Typical Current Derating

PWM Switching Frequency

The PWM switching frequency of the A8591 family is adjustable from 300 kHz to 2.4 MHz and has an accuracy of ±10% over the operating temperature range. The switching frequency is dithered to help reduce EMI between –7.5% and 7.5% according to a random sequence.

During startup, the PWM switching frequency changes from 25%, to 50%, and finally to 100% of f_{SW} as V_{OUT} rises from 0 V to the regulation voltage. The startup switching frequency is described in detail in the Soft-Start (Startup) and Inrush Current Control section of this datasheet.

If the regulator output is shorted to ground, $V_{FB} \approx 0$ V and the PWM frequency is 25% of f_{SW}. In this case, the low switching frequency allows extra off-time between SW pulses. The extra off-time allows the inductor current to remain under control (remaining well above 0 A) before the next SW pulse occurs. This prevents the inductor current from ratcheting up, or rising, to a value that could damage the device or the output inductor.

The FSET pin includes protection features that disable the regulator when the FSET pin is shorted to GND, shorted high (to NPOR), or when R_{FSET} is mis-selected.

EN/$\overline{\text{SLEEP}}$ Input

The A8591 family has the EN/$\overline{\text{SLEEP}}$ logic level input pin. To enable the device, the EN/$\overline{\text{SLEEP}}$ pin must be a logic high (>2.1 V). The EN/$\overline{\text{SLEEP}}$ pin is rated to 40 V, so this EN/$\overline{\text{SLEEP}}$ pin may be connected directly to V_{IN} if there is no suitable logic signal available to wake up the regulator.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

When EN/$\overline{\text{SLEEP}}$ transitions low, the device waits approximately 224 µs before shutting down. This delay provides plenty of filtering to prevent the device from prematurely entering sleep mode because of any small glitches that might couple onto the PCB trace or EN/$\overline{\text{SLEEP}}$ pin.

PWM Synchronization

If an external clock is applied to the FSET/SYNC_{PWM} pin, the device is forced into PWM mode and synchronizes its PWM frequency to the external clock. Synchronization is independent of R_{FSET}; it only needs to satisfy the range requirement in the Electrical Characteristics table. When synchronizing, the external clock pulses must satisfy the pulse-width, duty cycle, and rise/fall time requirements shown in the Electrical Characteristics table in this datasheet. During synchronization, frequency dithering is disabled.

The A8591 synchronizes to the SYNC input when the FSET/SYNC_{PWM} pin is driven above the 1.2 V threshold. Synchronization must occur within 16 µs; else, a fault may be declared, causing SW to halt operation. The A8591 transitions back to using the RFSET resistor after a rising has not crossed the 1.2 V threshold for ~8 µs, resulting in the high-side switch remaining off for ~8 µs and causing some V_{OUT} droop.

Transconductance Error Amplifier

The primary function of the transconductance error amplifier is to control the regulator output voltage. The error amplifier is shown in the Functional Block Diagram. It is shown as a three-terminal input device with two positive inputs and one negative input. An on-chip resistor divider is included. The negative input is simply connected to the internal resistor divider and is used to sense the feedback voltage for regulation. The two positive inputs are used for soft-start and steady-state regulation. The error amplifier performs an analog OR selection between the two positive inputs. The error amplifier regulates to either the internal soft-start voltage or the device internal reference, whichever is lower.

To stabilize the regulator, a series RC compensation network (R_Z and C_Z) must be connected from the error amplifier output (the COMP pin) to GND, as shown in the Typical Application Diagram. In most instances, an additional relatively low-value capacitor (C_P) should be connected in parallel with the R_Z-C_Z components to reduce the loop gain at very high frequencies. However, if the C_P capacitor is too large, the phase margin of the converter can be reduced. Calculating R_Z, C_Z, and C_P is detailed in the Design and Component Selection section of this datasheet.

If a fault occurs or the regulator is disabled, the COMP pin is pulled to GND via approximately 1 kΩ and SW switching is inhibited.

Slope Compensation

The A8591 family incorporates internal slope compensation (S_E) to allow PWM duty cycles in excess of 50% for a wide range of input/output voltages and inductor values. The slope compensation signal is added to the sum of the current-sense amplifier output and the PWM ramp offset. As shown in the Electrical Characteristics table, the amount of slope compensation scales with the nominal switching frequency (f_{SW}) set by R_{FSET}. The amount of slope compensation scales with the SYNC input frequency centered around 0.35 A/µs at 425 kHz in a similar way with R_{FSET}.

The value of the output inductor should be chosen such that S_E is between 0.5× and 1× the falling slope of the inductor current (S_F).

Current-Sense Amplifier

The A8591 family incorporates a high-bandwidth current-sense amplifier to monitor the current in the high-side MOSFET. This current signal is used by both the PWM and PFM control circuitry to regulate the MOSFET peak current. The current signal is also used by the protection circuitry to prevent damage to the device.

Power MOSFETs

The A8591 family includes a 40 V, 110 mΩ high-side N-channel MOSFET capable of delivering at least 2 A. The device also includes a 10 Ω, low-side MOSFET to help ensure the boot capacitor is always charged. The typical $R_{DS(on)}$ increase versus temperature is shown in Figure 4.

BOOT Regulator

The A8591 family contains a regulator to charge the boot capacitor. The voltage across the BOOT capacitor typically is 5 V. If the boot capacitor is missing, the device detects a boot overvoltage. Similarly, if the BOOT capacitor is shorted, the device detects a boot undervoltage. Also, the boot regulator has a current limit to protect itself during a short-circuit condition. The details of how each type of boot fault is handled by the A8591 are shown in the Summary of A8591 Family Fault Modes and Operation section.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

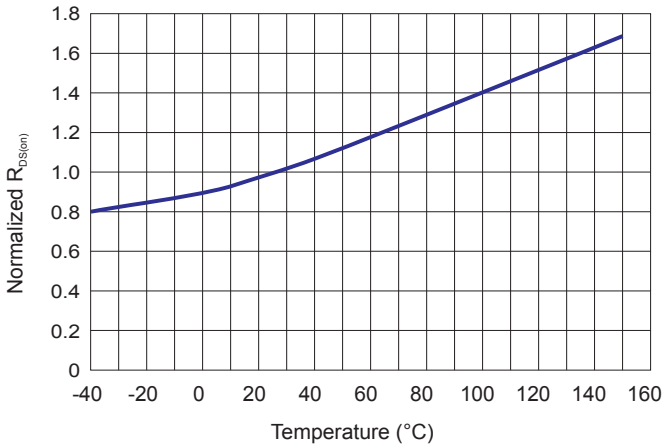


Figure 4: Typical MOSFET $R_{DS(on)}$ versus Temperature

Pulse-Width Modulation (PWM) Mode

The A8591 family utilizes fixed-frequency, peak current-mode control to provide excellent load and line regulation, fast transient response, and ease of compensation.

A high-speed comparator and control logic, capable of typical pulse widths down to $t_{ON(MIN)}$, are included in the device. The inverting input of the PWM comparator is connected to the output of the error amplifier. The noninverting input is connected to the sum of the current-sense signal, the slope compensation, and a DC offset voltage ($V_{PWMOFFS}$, nominally 400 mV).

At the beginning of each PWM cycle, the CLK signal sets the PWM flip-flop and the high-side MOSFET is turned on. When the summation of the DC offset, slope compensation, and current-sense signal, rises above the error amplifier voltage, the PWM flip-flop is reset and the high-side MOSFET is turned off.

The PWM flip-flop is reset-dominant, so the error amplifier may override the CLK signal in certain situations. For example, at very light loads or extremely high input voltages, the error amplifier (temporarily) reduces its output voltage to less than the 400 mV DC offset and the PWM flip-flop ignores one or more of the incoming CLK pulses. The high-side MOSFET does not turn on and the regulator skips pulses to maintain output voltage regulation.

In PWM mode, and when SW is switching in PFM mode, all of the device fault detection circuits are active. See Figure 1 showing how faults are handled during PWM mode. Also, the Protection Features section of this datasheet provides a detailed description of each fault and the Summary of A8591 Family Fault Modes and Operation section presents a summary.

Low-IQ Pulse-Frequency Modulation (PFM) Mode

The A8591 and the A8591-1 enter low-IQ PFM, provided that a fault is not present, the load is light, NPOR = 1, an external clock is not applied to the FSET/$SYNC_{PWM}$ pin, and the EN/$\overline{SLEEP}$ pin is high. At light loads, the PFM comparator, which is connected to the VOUT pin through the internal feedback resistor divider (which is the internal FB point), modulates the frequency of the SW node to regulate the output voltage with very high efficiency.

The reference for the PFM comparator is calibrated approximately 1% above the PWM regulation point. When the voltage at the internal FB point rises above the PFM comparator threshold and peak inductor current falls below $I_{PEAK(LO_IQ)}$ minus slope compensation, the device enters PFM coast mode, tri-stating the SW node and drawing extremely low current from V_{IN}. When voltage at the FB point falls below the PFM comparator threshold, the device fully powers up after approximately a 2.5 µs delay and the high-side MOSFET is repeatedly turned on, operating at the PWM switching frequency until the voltage at the FB pin rises above the PFM comparator threshold. The rise rate and voltage ripple of V_{OUT} are respectively determined by and dependent on the input voltage, output voltage, inductor value, output capacitance, and load.

When the COMP pin falls to a voltage corresponding to the low-IQ peak current threshold ($I_{PEAK(LO_IQ)}$) value, an internal clamp prevents the COMP voltage from falling further. This results in the output voltage rising slightly, which causes the PFM comparator to trip and the device to enter the PFM coast mode. Thus, when the load demands a peak inductor current that corresponds to less than the low-IQ peak current threshold ($I_{PEAK(LO_IQ)}$) minus the impact of slope compensation at the given duty cycle, the device operates in PFM mode. This transition point from PWM to PFM mode is defined by the input voltage, output voltage, slope compensation, and inductor value.

PFM mode operation for a light load (5 mA) is demonstrated in Figure 5. PWM and low-IQ PFM transitions are demonstrated in Figure 6. In PFM mode, the load steps from 0.05 A (PFM operation) to 1.05 A (PWM operation), then transitions back to 0.05 A PFM mode.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

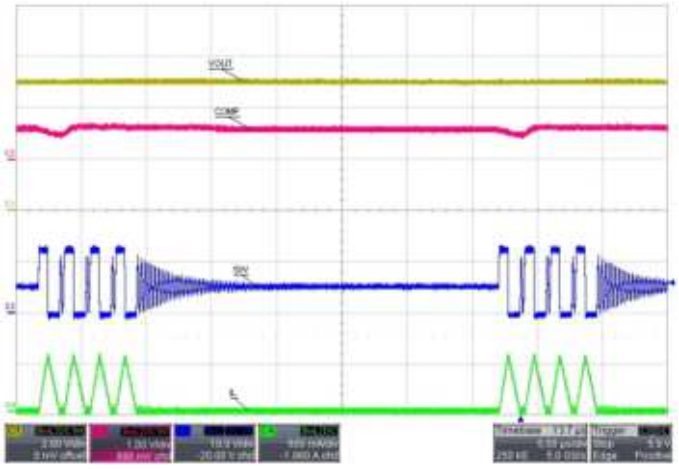


Figure 5: PFM Mode at Light Load (5 mA)

V_{IN} = 12 V, V_{OUT} = 5 V

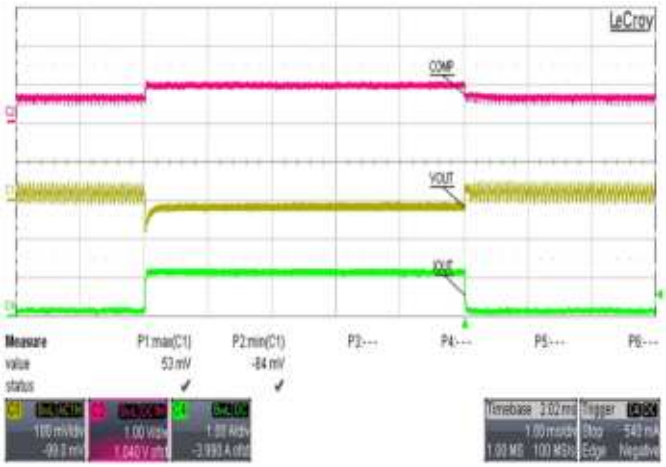


Figure 6: Load Steps Between 0.05 A and 1.05 A in PFM Mode

Soft-Start (Startup) and Inrush Current Control

Inrush current is controlled by the internal embedded soft-start function. The soft-start time of the A8591 family is fixed at 5 ms. When the device is enabled and all faults are cleared, the internal soft-start voltage ramps upward from 0 V. When the soft-start voltage exceeds the equivalent VOUT voltage, the error amplifier output slews above the 400 mV pedestal, initiating PWM switching.

When the device begins switching, the error amplifier regulates the internal FB voltage to be the soft-start voltage. During the active portion of soft-start, the regulator output voltage rises from 0 V to the nominal value.

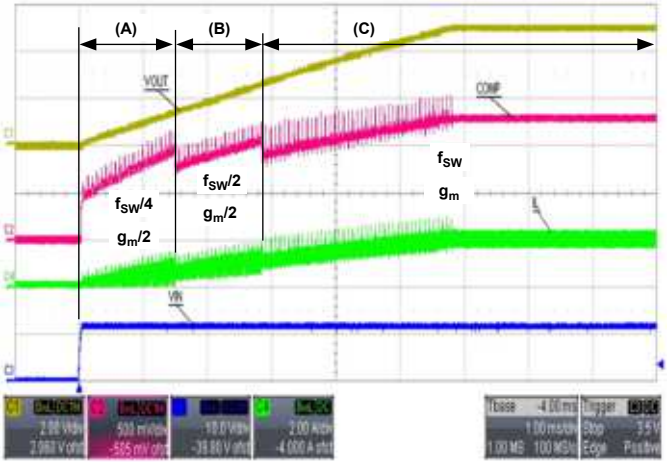
The startup sequence with the soft-start operation is shown in Figure 7. During startup, while VOUT voltage is below 25% (interval A in Figure 7), the PWM switching frequency is reduced to ¼ of f_{SW}. This corresponds to V_{OUT} < 1.25 V (for nominal 5 V output: A8591) or < 0.825 V (for nominal 3.3 V output: A8591-1). While V_{OUT} is above 25% but below 50% (interval B), the switching frequency is reduced to ½ of f_{SW}, and when V_{OUT} is above 50% (at C), the switching frequency is f_{SW}.

The error amplifier gain (g_m) also changes. While V_{OUT} is below 50% (at A through B), g_m is reduced to $g_m/2$. While V_{OUT} is above 50% (at C), the error amplifier gain is g_m.

The reduced switching frequencies and error amplifier gain are necessary to help improve output regulation and stability when V_{OUT} is very low. When V_{OUT} is very low, the PWM control loop requires on-times near the minimum controllable on-time and extra-low duty cycles that are not possible at the nominal switching frequency. When the soft-start voltage reaches approximately 800 mV, the error amplifier switches over to referencing the device-internal 800 mV reference for regulating the internal (resistor divider) FB voltage.

If the device is disabled or a fault occurs, the internal fault latch is set, and the soft-start voltage is discharged to ground very quickly. When the soft-start voltage decays to approximately 200 mV, the device clears the internal fault latch.

The soft-start voltage is discharged slowly when the device is in hiccup mode. Therefore, the soft-start not only determines the startup time but also the time between soft-start attempts in hiccup mode. Hiccup mode operation is discussed in more detail in the Protection Features section of this datasheet.



V_{OUT} Ramps from Startup (V_{IN} powered) to Nominal (5 V at 2 A, for A8591, shown)

Figure 7: Soft-Start Operation

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Pre-Biased Startup

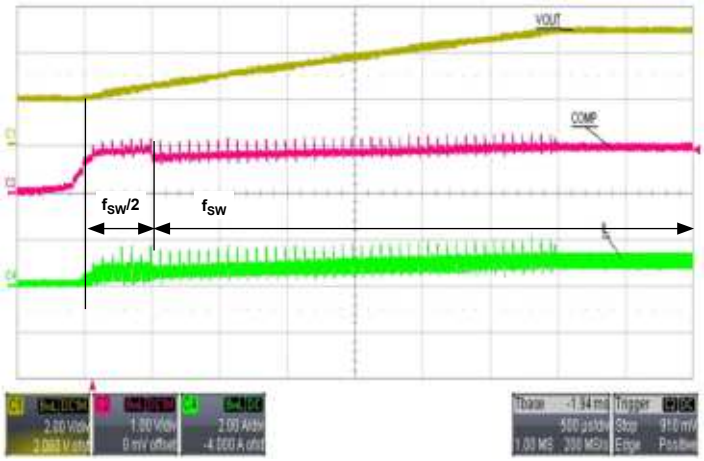
If the output of the regulator is pre-biased to some voltage, the A8591 family modifies the typical startup routine to prevent discharging the output capacitors. As described previously, the error amplifier usually becomes active when the soft-start voltage starts to ramp. If the output is pre-biased, the internal FB voltage is at some non-zero voltage. The COMP pin remains low and SW is tri-stated until the soft-start voltage rises above the V_{FB}. The startup when the output voltage is pre-biased to 2 V is shown in Figure 8.

Active-Low Power-On Reset (NPOR) Output

The A8591 family has an inverted power-on reset output (NPOR) with a fixed delay (t_{dPOR}) before the rising edge. The NPOR output is an open-drain output, so an external pull-up resistor must be used, as shown in the Typical Application Diagram. NPOR transitions high when the output voltage is within regulation. In PWM mode, NPOR is high when the output voltage is typically within 92.5% to 110% of the target value. The NPOR overvoltage and undervoltage comparators incorporate a small amount of hysteresis ($V_{NPORUV(HYS)(xV)}$), 40 mV(typ) for 3.3 V output (A8591-1) and 60 mV (typ) for 5 V output (A8591), and filtering (5 µs, typical) to help reduce chattering.

The NPOR output is immediately pulled low if either an overvoltage or an undervoltage condition occurs, or if the device junction temperature exceeds the thermal shutdown threshold (T_{SDth}). For other faults, NPOR depends on the output voltage. All A8591 family fault modes and their effects on NPOR are summarized in the Summary of A8591 Family Fault Modes and Operation section. When powering down, if V_{IN} goes low before V_{OUT}, NPOR is pulled low when the undervoltage condition occurs, but only remains low while V_{OUT} remains above ~3 V.

When the EN/$\overline{\text{SLEEP}}$ pin goes low, switching stops after 224 µs (typ) (t_{dSLEEP}), and NPOR goes low (even if $V_{OUT} > V_{NPORUV}$) and stays low until V_{OUT} drops to approximately 25% of nominal value. When V_{OUT} falls to approximately 25% of its nominal value, the device enters sleep mode, consuming $I_{IN(SLEEP)}$ on VIN; shortly after that, NPOR is released (no longer pulled low). Given this operation, the time that NPOR remains low is dependent on the current consumption on VOUT and the output capacitance. It is important to note that the high-side switch leakage can overwhelm the load current on VOUT, especially because the IC current on VOUT is very low in this mode. Therefore, for reliable operation in this situation, the user should select an NPOR resistor (if connected to VOUT) with a value low enough to overwhelm any high-side switch leakage.



V_{OUT} Prebiased at 2 V, Ramps to Nominal (5 V at 2 A, for A8591, shown)

Figure 8: Soft-Start Prebiased Startup

Protection Features

The A8591 was designed to satisfy the most demanding automotive and nonautomotive applications. In this section, a description of each protection feature is provided, and the protection operation is summarized in the Summary of A8591 Family Fault Modes and Operation section. All faults are available in both PWM and PFM mode. In PFM mode, all faults are monitored just before and while switching is active but are ignored while V_{OUT} remains above the PFM comparator threshold and below the NPOR OV threshold.

UNDERVOLTAGE LOCKOUT (UVLO)

An undervoltage lockout (UVLO) comparator monitors the voltage at the VIN pin and keeps the regulator disabled if the voltage is below the stop threshold ($V_{UVLO(OFF)}$). The UVLO comparator incorporates some hysteresis ($V_{UVLO(HYS)}$) to help reduce on-off cycling of the regulator due to resistive or inductive drops in the V_{IN} path during heavy loading or during startup.

PULSE-BY-PULSE OVERCURRENT PROTECTION (OCP)

The A8591 family monitors the current of the high-side MOSFET and, if the current exceeds the pulse-by-pulse overcurrent threshold (I_{LIM}), the high-side MOSFET is turned off. Typical PWM operation resumes on the next clock pulse from the oscillator. The device includes leading-edge blanking (as defined by the $t_{ON(MIN)}$ specification) to prevent false triggering of the pulse-by-pulse current limit when the high-side MOSFET is turned on initially.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Because the slope compensation ramp is added to the inductor current, the A8591 family delivers more current at lower duty cycles and less current at higher duty cycles. The relationship between the current limit and duty cycle is shown in Figure 9. As shown, the current limit at the minimum and maximum duty cycle remains fixed, but the relationship vs. duty cycle is skewed with frequency due to the fixed minimum off-time. Given the relationship, it is best to use the $I_{LIM(tonmin)}$ and $I_{LIM(toffmin)}$ to calculate the current limit at a given duty cycle.

During synchronization, the slope compensation scales in a fashion similar to R_{FSET}, with slightly less accuracy.

The exact current the buck regulator can support is heavily dependent on duty cycle (V_{IN}; V_{OUT}; and diode forward voltage, V_f), ambient temperature, thermal resistance of the PCB, airflow, component selection, and nearby heat sources.

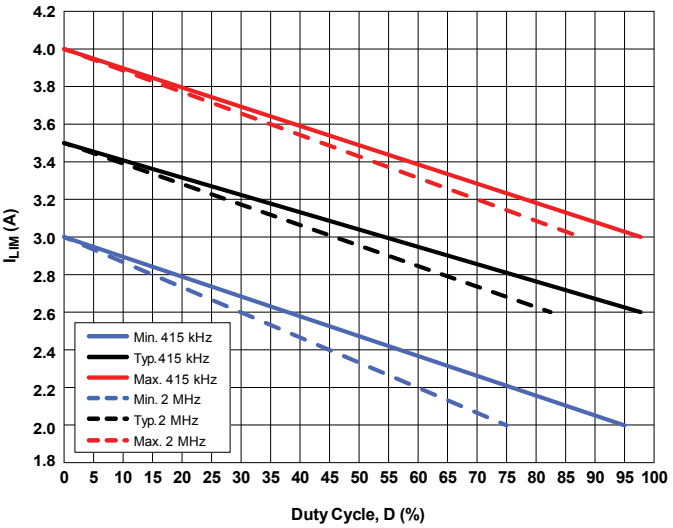


Figure 9: Pulse-by-Pulse Current Limit vs. Duty Cycle at 415 kHz (solid lines) and 2 MHz (dashed lines)

OVERCURRENT PROTECTION (OCP) AND HICCUP MODE

An OCP counter and hiccup mode circuit protect the buck regulator when the output of the regulator is shorted to ground or when the load is too high. When the soft-start ramp is active ($t < t_{SS}$), the OCP hiccup counter is disabled. Two conditions must be met for the OCP counter to be enabled and begin counting:

- $t > t_{SS}$, and
- V_{COMP} clamped at its maximum voltage (OCL = 1)

As long as these two conditions are met, the OCP counter remains enabled and counts pulses from the overcurrent comparator. If the COMP voltage decreases (OCL = 0), the OCP counter is cleared.

If the OCP counter reaches OCP_{LIM} counts (120), a hiccup latch is set and the COMP pin is quickly pulled down by a relatively low resistance (1 kΩ), and switching is halted for 20 ms to provide time for the IC to cool down. After the hiccup off-time expires (20 ms), the soft-start ramp starts, marking the beginning of a new, typical soft-start cycle, as described earlier.

When the soft-start voltage crosses the effective output voltage, the error amplifier forces the voltage at the COMP pin to quickly slew upward and PWM switching resumes. If the short-circuit at the regulator output remains, another hiccup cycle occurs. Hiccups repeat until the short-circuit is removed or the converter is disabled. If the short-circuit has been removed, the device completes a typical soft-start and the output voltage automatically recovers to the target level, as shown in Figure 10.

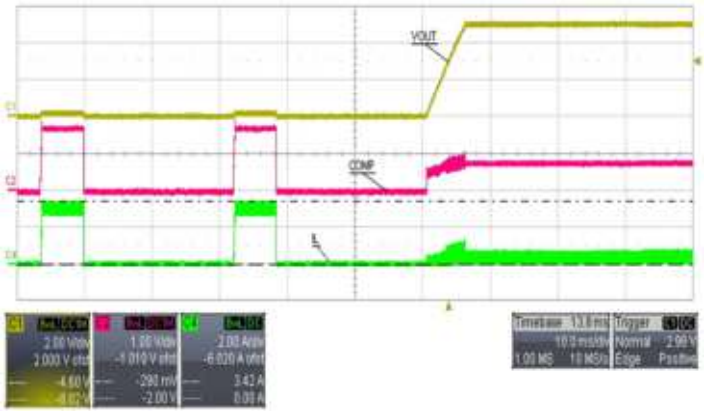


Figure 10: Hiccup Mode and Recovery (to 5 V at 0.5 A, for A8591, shown)

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

BOOT CAPACITOR PROTECTION

The A8591 family monitors the voltage across the BOOT capacitor to detect if the capacitor is missing or short-circuited. If the BOOT capacitor is missing, the regulator enters hiccup mode after seven PWM cycles. If the BOOT capacitor is shorted, the regulator enters hiccup mode after 120 to 64 PWM cycles.

For a BOOT fault, hiccup mode operates virtually the same as described previously for an output short-circuit fault (OCP), having a hiccup off-time of 20 ms, followed by a soft-start retry with repeated attempts until the fault clears. However, OCP is the only fault that is ignored during the soft-start ramp time (t_{SS}). A BOOT fault is a nonlatched condition, so the device automatically recovers when the fault is corrected.

ASYNCHRONOUS DIODE PROTECTION

If the asynchronous diode is missing or damaged (open), the SW pin is subject to unusually high negative voltages. This negative voltage may cause the device to malfunction and could lead to damage. The A8591 family includes protection circuitry to detect when the asynchronous diode is missing. If the SW pin is below −1.25 V typically, for more than 50 ns typically, the device enters hiccup mode after detecting 1 missing diode fault.

Also, if the asynchronous diode is shorted, the device experiences extremely high currents through the high-side MOSFET. If this occurs, the device enters hiccup mode after detecting one shorted diode fault.

OVERVOLTAGE PROTECTION (OVP)

The A8591 family provides an always-on overvoltage protection that monitors V_{OUT}, to protect against V_{OUT} rising at light loads due to high-side switch leakage. In this case, the high-side switch is forced off and the low-side switch continues to operate and can correct the OVP condition, provided only a few milliamperes of pull-down current are required. When the condition causing the overvoltage is corrected, the regulator automatically recovers.

During an output overvoltage condition, the device tries for up to 120 counts (t_{dPOV_POR}) to clear the overvoltage condition. If the overvoltage condition is successfully cleared within this time period, NPOR does not go low and the device continues to operate in PFM mode. If the overvoltage fault is not cleared during this time, an NPOR = 0 is declared and the device works indefinitely to reduce the output overvoltage fault. If it is successful in clearing this fault, a delay of approximately 7.5 ms (t_{dPOR}) occurs before the NPOR pin returns to the high state. Note that the size of the regulator output capacitor may have an effect on whether the overvoltage condition is cleared within the t_{dPOV_POR} time period.

PIN-TO-GROUND AND PIN-TO-PIN SHORT PROTECTIONS

The A8591 family is designed to satisfy the most demanding automotive applications. For example, the device is carefully designed fundamentally to withstand a short-circuit to ground at each pin without suffering damage.

In addition, care was taken when defining the device pin-out to optimize protection against adjacent pin-to-pin short-circuits. For example, logic pins and high-voltage pins are separated as much as possible. Inevitably, some low-voltage pins had to be located adjacent to high-voltage pins; however, in these instances the low-voltage pins are designed to withstand increased voltages, with clamps and/or series input resistance, to prevent damage to the device.

THERMAL SHUTDOWN (TSD)

The A8591 family monitors internal junction temperature and stops switching and pulls NPOR low if it becomes too hot. Also, to prepare for a restart, the internal soft-start voltage (V_{SS}) and the voltage at the COMP pin are pulled low until $V_{SS} < V_{SSRST}$. TSD is a nonlatched fault, so the device automatically recovers if the junction temperature decreases by approximately 20°C.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

SUMMARY OF A8591 FAMILY FAULT MODES AND OPERATION

Fault Mode	Internal Soft-Start	During Fault Counting, Before Hiccup Mode			Boot Charging	NPOR	Latched Fault	Reset Condition
		V_{COMP}	High-Side Switch	Low-Side Switch				
Output shorted to ground	Hiccup, after 120 OCL faults	Clamped for I_{LIM}, then pulled low for hiccup	$f_{OSC}/4$ due to V_{OUT} < 25%, responds to V_{COMP}	Can be activated if BOOT voltage is too low	Not affected	Depends on V_{OUT}	No	Automatic, remove the short
Output overcurrent, V_{OUT} > 50%	Hiccup, after 120 OCL faults	Clamped for I_{LIM}, then pulled low for hiccup	f_{OSC}, responds to V_{COMP}	Can be activated if BOOT voltage is too low	Not affected	Depends on V_{OUT}	No	Automatic, decrease load current
VOUT pin open	Pulled low after 32 cycles	Pulled low after 32 cycles	Forced off by COMP low	Can be activated if BOOT voltage is to low	Not affected	Stays low	No	Automatic, V_{OUT} pin reconnected
Boot capacitor missing	Hiccup, after 7 boot OV faults	Not affected but pulled low for hiccup	Forced off when boot OV fault occurs	Forced off when boot OV fault occurs	Off after boot fault occurs	Depends on V_{OUT}	No	Automatic, replace capacitor
Boot capacitor shorted	Hiccup, after 64 boot UV faults	Not affected but pulled low for hiccup	Forced off when boot UV fault occurs	Forced off only during hiccup	Off only during hiccup	Depends on V_{OUT}	No	Automatic, unshort capacitor
Asynchronous diode missing	Hiccup after 1 fault	Not affected but pulled low for hiccup	Forced off after 1 fault	Can be activated if BOOT voltage is too low	Not affected	Depends on V_{OUT}	No	Automatic, install diode
Asynchronous diode (or SW) hard short-to-ground	Hiccup after 1 fault	Clamped for I_{LIM}, then pulled low for hiccup	Forced off after 1 fault	Can be activated if BOOT voltage is too low	Not affected	Depends on V_{OUT}	No	Automatic, remove short
Asynchronous diode (or SW) soft short-to-ground	Hiccup, after 120 OCL faults	Clamped for I_{LIM}, then pulled low for hiccup	Active, responds to V_{COMP}	Can be activated if BOOT voltage is too low	Not affected	Depends on V_{OUT}	No	Automatic, remove short
Output overvoltage, (V_{OUT} > 3.6 V/5.5 V)	Not affected	Transitions low via loop response	Forced off	Active during $t_{OFF(MIN)}$	Off when V_{OUT} is too high	Pulled low when V_{OUT} is too high for 120 counts	No	Automatic, V_{OUT} returns to normal range
Output undervoltage	Not affected	Transitions high via loop response	Active, responds to V_{COMP}	Can be activated if BOOT voltage is too low	Not affected	Pulled low when V_{OUT} is too low	No	Automatic, V_{OUT} returns to normal range
FSET shorted to GND or above 1 V	Pulled low	Pulled low	Forced off	Forced off	Forced off	Depends on V_{OUT}	No	Auto
Thermal shutdown (TSD)	Pulled low until V_{SS} < V_{SSRST} and TSD = 0	Pulled low until V_{SS} < V_{SSRST} and TSD = 0	Forced off	Disabled	Off	Pulled low	No	Auto, part cools down

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

DESIGN AND COMPONENT SELECTION

PWM Switching Frequency (R_{FSET})

The PWM switching frequency is set by connecting a resistor from the FSET/$SYNC_{PWM}$ pin to ground. A graph showing the relationship between the typical switching frequency (y-axis) and the FSET resistor (x-axis) is shown in Figure 11. For a required switching frequency (f_{SW}), the FSET resistor value can be calculated as follows:

Equation 1:

$$R_{FSET} = \frac{27770}{f_{SW}} - 4.78$$

where f_{SW} is in kHz and R_{FSET} is in kΩ.

When the PWM switching frequency is chosen, the user should be aware of the minimum controllable on-time ($t_{ON(MIN)}$) and minimum off-time of the A8591 family. If the system-required on-time is less than $t_{ON(MIN)}$, switch node jitter occurs and the output voltage has increased ripple or oscillations.

The PWM switching frequency should be calculated as follows:

Equation 2:

$$f_{SW} < \frac{V_{OUT}}{t_{ON(MIN)} \times V_{IN(MAX)}}$$

where V_{OUT} is the output voltage, $t_{ON(MIN)}$ is the minimum controllable on-time of the A8591 family, and $V_{IN(MAX)}$ is the maximum required operational input voltage (not the peak surge voltage).

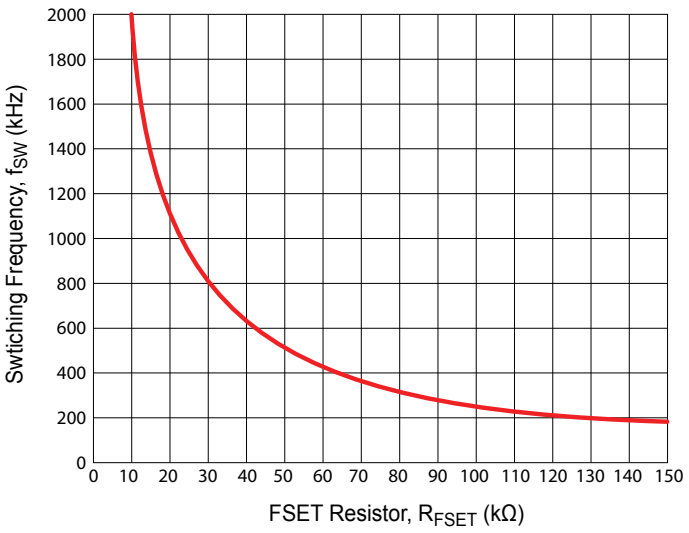


Figure 11: PWM Switching Frequency versus RFSET

If the device synchronization function is employed, the base switching frequency should be chosen such that jitter does not result in the maximum synchronized switching frequency according to Equation 2.

Output Inductor (L_O)

For a peak current mode regulator, it is common knowledge that, without adequate slope compensation, the system becomes unstable when the duty cycle is near or above 50%. However, the slope compensation in the A8591 family is a fixed value (S_E). Therefore, it is important to calculate an inductor value such that the falling slope of the inductor current (S_F) works well with the device slope compensation. A range of values for the output inductor can be calculated using Equation 3a and Equation 3b, based on the well-known approach of providing slope compensation that matches 50% to 100% of the down slope of the inductor current.

Equation 3a:

$$\frac{V_{OUT} + V_f}{2 \times S_E} \leq L_O \leq \frac{V_{OUT} + V_f}{S_E}$$

where L_O is in µH, V_f is the forward voltage of the asynchronous diode, and the slope compensation (S_E) is a function of switching frequency, as follows:

Equation 3b:

$$S_E = 0.13 \times f_{SW}^2 + 0.69 \times f_{SW} + 0.031$$

where S_E is in A/µs and f_{SW} is in MHz.

More recently, Dr. Raymond Ridley presented a formula to calculate the amount of slope compensation required to critically damp the double poles at half the PWM switching frequency (this approach includes the duty cycle (D), which should be calculated at the minimum input voltage to ensure optimal stability):

Equation 4:

$$L_O \geq \frac{V_{OUT} + V_f}{S_E} \left(1 - 0.18 \times \frac{V_{IN(MIN)} + V_f}{V_{OUT} + V_f}\right)$$

To avoid dropout (saturation of the buck regulator), $V_{IN(MIN)}$ must be approximately 1 to 1.5 V above V_{OUT} when calculating the inductor value with Equation 4.

If Equation 3a or Equation 4 yields an inductor value that is not a standard value, the next closest available value should be used. The final inductor value should allow for 10% to 20% of initial tolerance and 20% to 30% of inductor saturation.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

The saturation current of the inductor should exceed the peak current capability of the device. Ideally, for output short-circuit conditions, the inductor should not saturate given the highest pulse-by-pulse current limit at minimum duty cycle ($I_{LIM(0)}$), 4 A (max). This may be too costly. At the very least, the inductor should not saturate given the peak operating current according to:

Equation 5:

$$I_{PEAK} = 4.1 - \frac{S_E \times (V_{OUT} + V_f)}{1.15 \times f_{SW} \times (V_{IN(MAX)} + V_f)}$$

where $V_{IN(MAX)}$ is the maximum continuous input voltage, such as 18 V (not a surge voltage, like 40 V).

Starting with Equation 5 and subtracting half of the inductor ripple current provides an interesting equation to predict the typical DC load capability of the regulator at a given duty cycle (D):

Equation 6:

$$I_{OUT(DC)} \leq 4.1 - \frac{S_E \times D}{f_{SW}} - \frac{V_{OUT} \times (1 - D)}{2 \times f_{SW} \times L_O}$$

After an inductor is chosen, it should be tested during output short-circuit conditions. The inductor current should be monitored using a current probe. A good design should ensure the inductor or the regulator are not damaged when the output is shorted to ground at maximum input voltage and the highest expected ambient temperature.

Output Capacitors

The output capacitors filter the output voltage to provide an acceptable level of ripple voltage, and they also store energy to help maintain voltage regulation during a load transient. The voltage rating of the output capacitors must support the output voltage with sufficient design margin.

The output voltage ripple (ΔV_{OUT}) is a function of the output capacitor parameters: C_O, ESR_{CO}, and ESL_{CO}:

Equation 7:

$$\Delta V_{OUT} = \Delta I_L \times ESR_{CO} + \frac{V_{IN} - V_{OUT}}{L_O} \times ESL_{CO} + \frac{\Delta I_L}{8 f_{SW} C_O}$$

The type of output capacitors determines which terms of Equation 7 are dominant. For ceramic output capacitors, the ESR_{CO} and ESL_{CO} are virtually zero, so the output voltage ripple is dominated by the third term of Equation 7:

Equation 8:

$$\Delta V_{OUT} \leq \frac{\Delta I_L}{8 f_{SW} C_O}$$

To reduce the voltage ripple of a design using ceramic output capacitors, simply increase the total capacitance, reduce the inductor current ripple (that is, increase the inductor value), or increase the switching frequency.

For electrolytic output capacitors, the value of capacitance is relatively high, so the third term in Equation 7 is very small and the output voltage ripple is determined primarily by the first two terms of Equation 7:

Equation 9:

$$\Delta V_{OUT} = \Delta I_L \times ESR_{CO} + \frac{V_{IN} - V_{OUT}}{L_O} \times ESL_{CO}$$

To reduce the voltage ripple of a design using electrolytic output capacitors, simply decrease the equivalent ESR_{CO} and ESL_{CO} by using a high(er) quality capacitor or adding more capacitors in parallel, or reduce the inductor current ripple (that is, increase the inductor value).

The ESR of some electrolytic capacitors can be quite high, so Allegro recommends choosing a quality capacitor for which the ESR or the total impedance is clearly documented in the capacitor datasheet. Also, the ESR of electrolytic capacitors usually increases significantly at cold ambients, as much as 10×, which increases the output voltage ripple and, in most cases, reduces the stability of the system.

The transient response of the regulator depends on the quantity and type of output capacitors. In general, minimizing the ESR of the output capacitance results in a better transient response. The ESR can be minimized by simply adding more capacitors in parallel or by using higher quality capacitors. At the instant of a fast load transient (di/dt), the output voltage changes by the amount:

Equation 10:

$$\Delta V_{OUT} = \Delta I_L \times ESR_{CO} + \frac{di}{dt} \times ESL_{CO}$$

After the load transient occurs, the output voltage deviates from its nominal value for a short period of time. The length of this

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

time depends on the system bandwidth, the output inductor value, and the output capacitance. Eventually, the error amplifier returns the output voltage to its nominal value.

The speed at which the error amplifier returns the output voltage to the set point depends mainly on the closed-loop bandwidth of the system. A higher bandwidth usually results in a shorter time to return to the nominal voltage. However, for a higher-bandwidth system, it may be more difficult to obtain acceptable gain and phase margins. Selection of the compensation components (R_Z, C_Z, and C_P) are discussed in more detail in the Compensation Components section of this datasheet.

Low-IQ PFM Output Voltage Ripple Calculation

After choosing the output inductor and output capacitor(s), it is important to calculate the output voltage ripple ($\Delta V_{OUT(PFM)}$) during low-IQ PFM mode. With ceramic output capacitors, the output voltage ripple in PWM mode is usually negligible, but that is not the case during low-IQ PFM mode.

The PFM mode comparator requires approximately 20 mV or greater of voltage ripple on the VOUT pin and generates groups of pulses to meet this requirement. However, if a single pulse results in a voltage ripple greater than 20 mV, the voltage ripple becomes dictated by that single pulse. To calculate the voltage ripple from that single pulse, first the peak inductor current must be calculated with slope compensation accounted for. The $I_{PEAK(LO_IQ)}$ specification does not include slope compensation, so the peak inductor current operating point is calculated as:

Equation 11:

$$I_{PEAK_L} = \frac{I_{PEAK(LO_IQ)}}{1 + \frac{S_E \times L_O}{V_{IN} - V_{OUT}}}$$

Then, calculate the MOSFET on-time and off-time (Figure 12). The on-time is defined as the time it takes for the inductor current to reach I_{PEAK_L}:

Equation 12:

$$t_{ON} = \frac{I_{PEAK_L} \times L_O}{V_{IN} - V_{OUT} - I_{PEAK_L} \times (R_{DS(on)HS} + L_{O(DCR)})}$$

where $R_{DS(on)}$ is the on-resistance of the internal high-side MOSFET (110 mΩ (typ)) and $L_{O(DCR)}$ is the DC resistance of the output inductor, L_O.

During this rising time interval, the length of time for the inductor current to rise from 0 A to I_{OUT} is:

Equation 13:

$$t_1 = \frac{I_{OUT} \times L_O}{V_{IN} - V_{OUT} - I_{PEAK_L} \times (R_{DS(on)HS} + L_{O(DCR)})}$$

The off-time is defined as the time it takes for the inductor current to decay from I_{PEAK_L} to 0 A:

Equation 14:

$$t_{OFF} = \frac{I_{PEAK_L} \times L_O}{V_{OUT} + V_f}$$

During this falling time interval, the length of time for the inductor current to fall from I_{OUT} to 0 A is:

Equation 15:

$$t_2 = \frac{I_{OUT} \times L_O}{V_{OUT} + V_f}$$

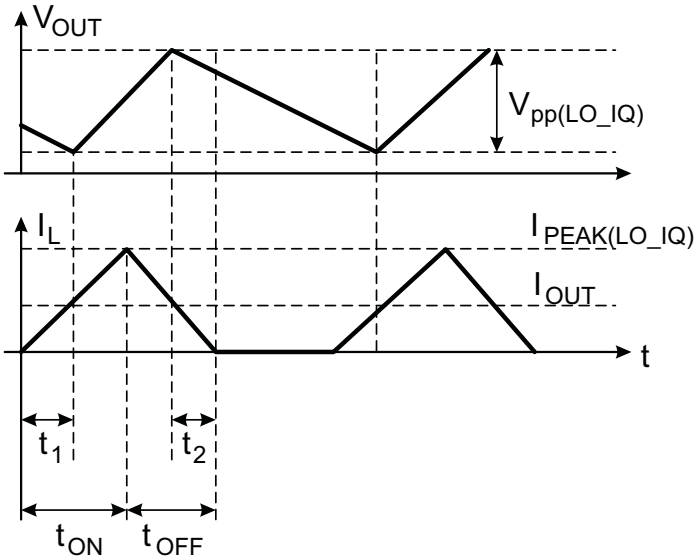


Figure 12: Calculating the Output Ripple Voltage in PFM Mode

Given the peak inductor current (I_{PEAK_L}) and the rise and fall times (t_{ON} and t_{OFF}) for the inductor current, the output voltage ripple can be calculated for a signal pulse as:

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Equation 16:

$$V_{PP(LO_IQ)} = \frac{I_{PEAK_L} - I_{OUT}}{2 \times C_{OUT}} \times (t_{ON} + t_{OFF} - t_1 - t_2)$$

If $V_{PP(LO_IQ)}$ is greater than the ~20 mV ripple that the PFM comparator requires, the output capacitance or inductor can be adjusted to reduce the PFM mode voltage ripple. In PFM mode, decreasing the inductor value reduces the PFM ripple, but may negatively impact the PWM voltage ripple or maximum load current in PWM mode, or it may change the mode of operation from CCM to DCM.

If $V_{PP(LO_IQ)}$ is less than the ~20 mV requirement, the A8591 operates with multiple pulses at the PWM frequency to meet the ripple requirement. The fixed-frequency operation may result in DCM or CCM operation during the multiple pulses.

Input Capacitors

Three factors should be considered when choosing the input capacitors. First, the capacitors must be chosen to support the maximum expected input surge voltage with adequate design margin. Second, the capacitor rms current rating must exceed the expected rms input current to the regulator. Third, the capacitors must have enough capacitance and a sufficiently low ESR to limit the input voltage dV/dt to much less than the hysteresis of the UVLO circuitry (nominally 400 mV for the A8591 family) at maximum loading and minimum input voltage.

The input capacitors must deliver an rms current (I_{RMS}) according to:

Equation 17:

$$I_{RMS} = I_{OUT} \sqrt{D \times (1 - D)}$$

where the duty cycle (D) is defined as:

Equation 18:

$$D \approx (V_{OUT} + V_f) / (V_{IN} + V_f)$$

and V_f is the forward voltage of the asynchronous diode, D1.

The normalized input capacitor rms current versus duty cycle is shown in Figure 13. To use this graph, simply find the operational duty cycle (D) on the x-axis and determine the input/output current multiplier on the y-axis. For example, at a 20% duty cycle, the input/output current multiplier is 0.40. Therefore, if the regulator is delivering 2 A of steady-state load current, the input capacitor(s) must support 0.40 × 2 A or 0.8 A(rms).

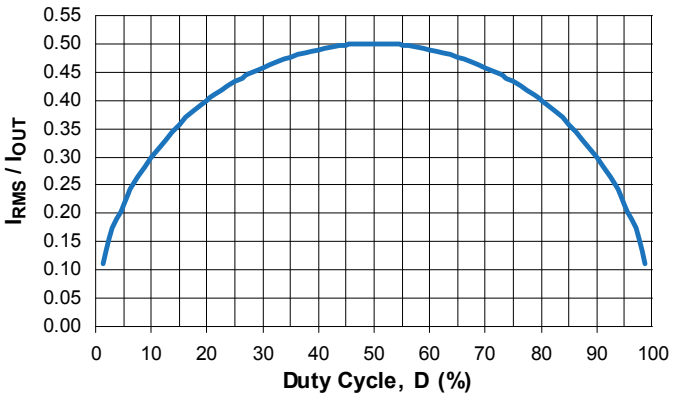


Figure 13: Normalized Input Capacitor Ripple versus Duty Cycle

The input capacitor(s) must limit the voltage deviations at the VIN pin to significantly less than the device UVLO hysteresis during maximum load and minimum input voltage. The minimum input capacitance can be calculated using:

Equation 19:

$$C_{IN} \geq \frac{I_{OUT} \times D \times (1 - D)}{0.85 \times f_{SW} \times \Delta V_{IN(MIN)}}$$

where $\Delta V_{IN(MIN)}$ is chosen to be much less than the hysteresis of the V_{IN} UVLO comparator ($\Delta V_{IN(MIN)} \leq 150$ mV is recommended), and f_{SW} is the nominal PWM frequency.

The $D \times (1 - D)$ term in Equation 17 has an absolute maximum value of 0.25 at 50% duty cycle. So, for example, a very conservative design based on $I_{OUT} = 2$ A, $f_{SW} = 85\%$ of 425 kHz, $D \times (1 - D) = 0.25$, and $\Delta V_{IN} = 150$ mV yields:

Equation 20:

$$C_{IN} \geq \frac{2.0\ (A) \times 0.25}{361\ (kHz) \times 150\ (mV)} = 9.2\ \mu F$$

A good design should consider the DC-bias effect on a ceramic capacitor: As the applied voltage approaches the rated value, the capacitance value decreases. This effect is very pronounced with the Y5V and Z5U temperature-characteristic devices (as much as

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

90% reduction), so these types should be avoided. The X5R and X7R type capacitors should be the primary choices due to their stability versus both DC bias and temperature.

For all ceramic capacitors, the DC-bias effect is even more pronounced on smaller sizes of device case, so a good design uses the largest affordable case size (such as 1206 or 1210). Also, it is advisable to select input capacitors with plenty of design margin in the voltage rating to accommodate the worst-case transient input voltage (such as a load dump as high as 40 V for automotive applications).

Asynchronous Diode (D1)

There are three requirements for the asynchronous diode. First, the asynchronous diode must be able to withstand the regulator input voltage when the high-side MOSFET is on. Therefore, choose a diode with a reverse voltage rating (V_R) that exceeds the maximum expected input voltage (that is, the surge voltage). Second, the forward voltage of the diode (V_f) should be minimized or the regulator efficiency suffers. Also, if V_f is too high, the missing-diode protection in the A8591 family could be inappropriately activated. A Schottky-type diode that can maintain a very low V_f when the regulator output is shorted to ground at the coldest ambient temperature is highly recommended. Third, the asynchronous diode must conduct the output current when the high-side MOSFET is off. Therefore, the average forward-current rating of this diode ($I_{f(av)}$) must be high enough to deliver the load current according to:

Equation 21:

$$I_{f(av)} \geq I_{OUT(MAX)} \, (1 - D_{MIN})$$

where D_{MIN} is the minimum duty cycle, as defined in Equation 19, and $I_{OUT(MAX)}$ is the maximum continuous output current of the regulator.

Bootstrap Capacitor

A bootstrap capacitor must be connected between the BOOT and SW pins to provide floating gate drive to the high-side MOSFET. Usually, 47 nF is an adequate value. This capacitor should be a high-quality ceramic capacitor, such as an X5R or X7R, with a voltage rating of at least 16 V.

The A8591 family incorporates a 10 Ω low-side MOSFET to ensure that the bootstrap capacitor is always charged, even when the converter is lightly loaded or pre-biased.

Compensation Components (R_Z, C_Z, and C_P)

To properly compensate the system, it is important to understand where the buck power stage, load resistance, and output capacitance form their poles and zeros in frequency. Also, it is important to understand that the (Type II) compensated error amplifier introduces a zero and two more poles, and where these should be placed to maximize system stability, provide a high bandwidth, and optimize the transient response.

First, consider the power stage of the A8591 family, the output capacitors, and the load resistance. This circuitry is commonly referred as the *control-to-output* transfer function. The low-frequency gain of this circuitry depends on the COMP to SW current gain (g_{mPOWER}), and the value of the load resistor (R_L). The DC gain ($G_{CO(0HZ)}$) of the control-to-output is:

Equation 22:

$$G_{CO(0Hz)} = g_{mPOWER} \times R_L$$

The control-to-output transfer function has a pole (f_{P1}), formed by the output capacitance (C_{OUT}) and load resistance (R_L), located at:

Equation 23:

$$f_{P1} = \frac{1}{2\pi \times R_L \times C_{OUT}}$$

The control-to-output transfer function also has a zero (f_{Z1}) formed by the output capacitance (C_{OUT}) and its associated ESR:

Equation 24:

$$f_{Z1} = \frac{1}{2\pi \times ESR \times C_{OUT}}$$

For a design with very low ESR-type output capacitors (such as ceramic or OSCON output capacitors), the ESR zero, f_{Z1}, is usually at a very high frequency, so it can be ignored. On the other hand, if the ESR zero falls below or near the 0 dB crossover frequency of the system (as happens with electrolytic output capacitors), it should be cancelled by the pole formed by the C_P capacitor and the R_Z resistor (discussed and identified later as f_{P3}).

A Bode plot of the control-to-output transfer function for the configuration shown in the Typical Application Diagram, with V_{OUT} = 5 V, I_{OUT} = 2 A, and R_L = 2.5 Ω, is shown in Figure 14. The pole at f_{P1} can easily be seen at 1.2 kHz, while the ESR zero, f_{Z1}, occurs at a very high frequency, 600 kHz (this is typical for a design using ceramic output capacitors).

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

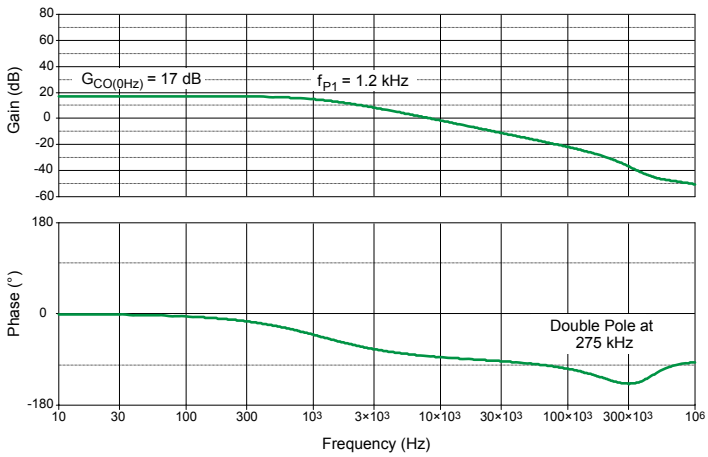


Figure 14: Control-to-Output Bode Plot

NOTE: Due to the double-pole at half the switching frequency, there is more than 90° of total phase shift.

Next, consider the error amplifier (g_m), and the compensation network R_Z-C_Z-C_P. It greatly simplifies the transfer function derivation if $R_O >> R_Z$, and $C_Z >> C_P$. In most cases, $R_O > 2$ MΩ, 1 kΩ < R_Z < 100 kΩ, 220 pF < C_Z < 47 nF, and C_P < 50 pF, so the following equations are very accurate.

The low-frequency gain of the control section ($G_{C(0Hz)}$) is calculated as:

Equation 25:

$$G_{C(0\,Hz)} = g_m \times R_0 = A_{VOL}$$

where

V_{OUT} is the output voltage,
V_{FB} is the reference voltage (0.8 V),
g_m is the error amplifier transconductance, and
R_O is the error amplifier output impedance (A_{VOL}/g_m).

The transfer function of the Type-II compensated error amplifier has a (very) low-frequency pole (f_{P2}) dominated by the output error amplifier output impedance (R_O) and the C_Z compensation capacitor:

Equation 26:

$$f_{P2} = \frac{1}{2\pi \times R_O \times C_Z}$$

The transfer function of the Type-II compensated error amplifier also has frequency zero (f_{Z2}) dominated by the R_Z resistor and the C_Z capacitor:

Equation 27:

$$f_{Z2} = \frac{1}{2\pi \times R_Z \times C_Z}$$

Last, the transfer function of the Type-II compensated error amplifier has a (very) high-frequency pole (f_{P3}) dominated by the R_Z resistor and the C_P capacitor:

Equation 28:

$$f_{P3} = \frac{1}{2\pi \times R_Z \times C_P}$$

A Bode plot of the error amplifier and its compensation network is shown in Figure 15, where f_{P2}, f_{P3}, and f_{Z2} are indicated on the gain plot. Notice that the zero (f_{Z2} at 2.6 kHz) has been placed so that it is just above the pole at f_{P1} previously shown at 1.2 kHz in the control-to-output Bode plot (Figure 14). Placing f_{Z2} just above f_{P1} results in excellent phase margin, but relatively slow transient recovery time, as shown later.

Finally, consider the combined Bode plot of both the control-to-output and the compensated error amplifier (Figure 16). Careful examination of this plot shows that the magnitude and phase of the entire system (red curve) are simply the sum of the error amplifier response (blue curve) and the control-to-output response (green curve). As shown in Figure 16, the bandwidth of this system (f_c) is 60 kHz, the phase margin is 69 degrees, and the gain margin is 14 dB.

Complete designs for several common output voltages at 2 MHz, 425 kHz, and 300 kHz are provided in the Recommended Component Values table.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

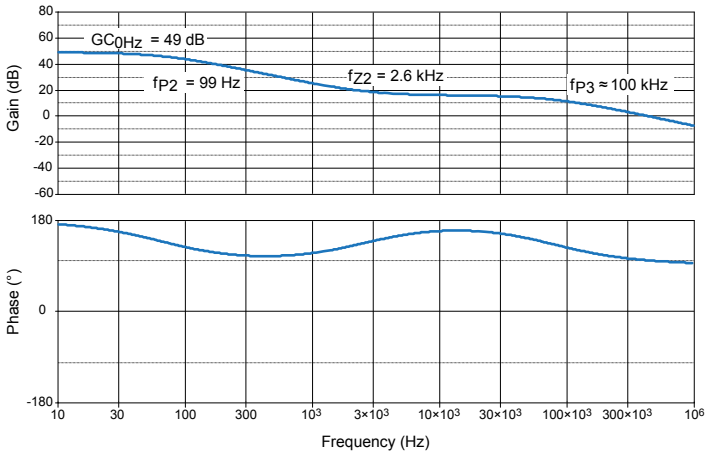


Figure 15: Type-II Compensated Error Amplifier Bode Plot

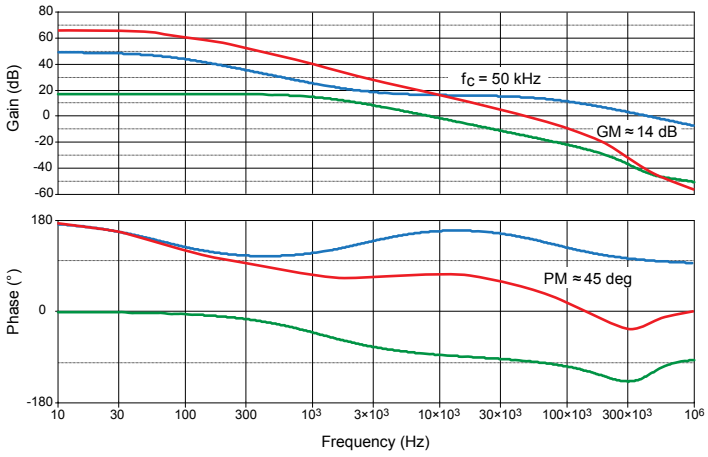


Figure 16: Bode Plot of the Complete System (red curve)

Generalized Tuning Procedure

This section presents a methodology to systematically apply design considerations provided above.

1. Choose the system bandwidth (f_C). This is the frequency at which the magnitude of the gain crosses 0 dB. Recommended values for f_C, based on the PWM switching frequency, are in the range $f_{SW}/20 < f_C < f_{SW}/7.5$. A higher value of f_C generally provides a better transient response, while a lower value of f_C generally makes it easier to obtain higher gain and phase margins.
2. Calculate the R_Z resistor value. This sets the system bandwidth (f_C):

   Equation 29:

$$R_Z = f_C \times \frac{2\pi \times C_{OUT}}{g_{mPOWER} \times g_m}$$

3. Determine the frequency of the pole (f_{P1}). This pole is formed by C_{OUT} and R_L. Use Equation 23 (repeated here):

$$f_{P1} = \frac{1}{2\pi \times R_L \times C_{OUT}}$$

Recommended Component Values

V_{OUT} (V)	f_{SW} (kHz)	R_{FSET} (kΩ)	L_O (µH)	C_O [1] (µF)	$R_Z + C_Z // C_P$		
					R_Z (kΩ)	C_Z (pF)	C_P (pF)
3.3 (A8591-1)	300	86.6	10 (DR-1050-100-R)	38	24.9	1500	22
5 (A8591)			22 (744770122)	53	35.7	1500	15
3.3 (A8591-1)	425	59	10 (DR-1050-100-R)	38	34	560	15
5 (A8591)			10 (DR-1050-100-R)	53	47.5	680	8
3.3 (A8591-1)	2000	9.31	3.3 (74437346033)	32	39.2	1000	3.3
5 (A8591)			4.7 (74437346047)	32	54.9	1000	3.3

[1] The user must consider negative tolerance and DC-bias effect when choosing components to obtain C_O.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

4. Calculate a range of values for the C_Z capacitor using:

   Equation 30:

$$\frac{4}{2\pi \times R_Z \times f_C} < C_Z < \frac{1}{2\pi \times R_Z \times 1.5 \times f_{P1}}$$

To maximize system stability (that is, to have the greatest gain margin), use a higher value of C_Z. To optimize transient recovery time, although at the expense of some phase margin, use a lower value of C_Z.

5. Calculate the frequency of the ESR zero (f_{Z1}) formed by the output capacitor(s) by using Equation 24 (repeated here):

$$f_{Z1} = \frac{1}{2\pi \times \text{ESR} \times C_{OUT}}$$

If f_{Z1} is at least 1 decade higher than the target crossover frequency (f_C), f_{Z1} can be ignored. This is usually the case for a design using ceramic output capacitors. Use Equation 28 to calculate the value of C_P by setting f_{P3} to either $5 \times f_C$ or $f_{SW}/2$, whichever is higher.

Alternatively, if f_{Z1} is near or below the target crossover frequency (f_C), use Equation 28 to calculate the value of C_P by setting f_{P3} equal to f_{Z1}. This is usually the case for a design using high-ESR electrolytic output capacitors.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

POWER DISSIPATION AND THERMAL CALCULATIONS

The power dissipated in the A8591 family is the sum of the power dissipated from the VIN supply current (P_{IN}), the power dissipated due to the switching of the high-side power MOSFET (P_{SW}), the power dissipated due to the rms current being conducted by the high-side MOSFET (P_{COND}), and the power dissipated by the gate drivers (P_{DRIVER}).

The power dissipated from the VIN supply current can be calculated using:

Equation 31:

$$P_{IN} = V_{IN} \times I_Q + (V_{IN} - V_{GS}) \times Q_G \times f_{SW}$$

where:

V_{IN} is the input voltage,
I_Q is the input quiescent current drawn by the device (nominally 2.5 mA),
V_{GS} is the MOSFET gate drive voltage (typically 5 V),
Q_G is the MOSFET gate charge (approximately 2.5 nC), and
f_{SW} is the PWM switching frequency.

The power dissipated by the internal high-side MOSFET during PWM switching can be calculated using:

Equation 32:

$$P_{SW} = \frac{V_{IN} \times I_{OUT} \times (t_r + t_f) \times f_{SW}}{2}$$

where:

V_{IN} is the input voltage,
I_{OUT} is the output current,
f_{SW} is the PWM switching frequency, and
t_r and t_f are the rise and fall times measured at the SW node.

The exact rise and fall times at the SW node depend on the external components and PCB layout, so each design should be measured at full load. Approximate values for both t_r and t_f range from 10 to 15 ns.

The power dissipated by the high-side MOSFET while it is conducting can be calculated using:

Equation 33:

$$P_{COND} = I^2_{rms(FET)} \times R_{DS(on)HS} = \left(\frac{V_{OUT}+V_f}{V_{IN}+V_f}\right) \times \left(I^2_{OUT} + \frac{\Delta I_L^2}{12}\right) \times R_{DS(on)HS}$$

where:

I_{OUT} is the regulator output current,
ΔI_L is the peak-to-peak inductor ripple current, and
$R_{DS(on)HS}$ is the on-resistance of the high-side MOSFET.

The $R_{DS(on)}$ of the MOSFET has some initial tolerance plus an increase from self-heating and elevated ambient temperatures. A conservative design should accommodate an $R_{DS(on)}$ with at least a 15% initial tolerance plus 0.39%/°C increase due to temperature.

The power dissipated by the internal gate drivers can be calculated using:

Equation 34:

$$P_{DRIVER} = Q_G \times V_{GS} \times f_{SW}$$

where:

Q_G is the gate charge to drive the MOSFET to V_{GS} = 5 V (about 2.5 nC),
V_{GS} is the gate drive voltage (typically 5 V), and
f_{SW} is the PWM switching frequency.

Bias power dissipation at VOUT pin:

Equation 35:

$$P_{bias} = V_{OUT} \times I_{IN} = 5\ V\ (or\ 3.3\ V) \times 2.5\ mA$$

Finally, the total power dissipated by the device (P_{TOTAL}) is the sum of the previous equations:

Equation 36:

$$P_{TOTAL} = P_{IN} + P_{SW} + P_{COND} + P_{DRIVER} + P_{bias}$$

The average junction temperature can be calculated using:

Equation 37:

$$T_J = P_{TOTAL} + R_{\theta JA} + T_A$$

where:

P_{TOTAL} is the total power dissipated as described in Equation 36,
$R_{\theta JA}$ is the junction-to-ambient thermal resistance (34°C/W on a 4-layer PCB), and
T_A is the ambient temperature.

The maximum junction temperature is dependent on how efficiently heat can be transferred from the PCB to ambient air. It is critical that the thermal pad on the bottom of the IC is connected to at least one ground plane using multiple vias.

As with any regulator, there are limits to the amount of heat that can be dissipated before risking thermal shutdown. There are trade-offs among ambient operating temperature, input voltage, output voltage, output current, switching frequency, PCB thermal resistance, airflow, and other nearby heat sources. Even a small amount of airflow reduces the junction temperature considerably.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

PCB COMPONENT PLACEMENT AND ROUTING

A good PCB layout is critical if the A8591 family is to provide clean, stable output voltages. Follow these guidelines to ensure a good PCB layout.

A typical buck converter schematic with the critical power paths/loops is shown in Figure 17. An example PCB component placement and routing with the same critical power paths/loops from the schematic is shown in Figure 18.

1. By far, the highest dI/dt in the asynchronous buck regulator occurs at the instant the high-side MOSFET turns on and the capacitance of the asynchronous Schottky diode (200 to 1000 pF) is quickly charged to V_{IN}. The ceramic input capacitors must deliver this fast, short pulse of current. Therefore, the loop—from the ceramic input capacitors through the high-side MOSFET and into the asynchronous diode to ground—must be minimized. Ideally, these components are all connected using only the top metal (that is, do not use vias to other power/signal layers).
2. When the high-side MOSFET is on, current flows from the input supply and capacitors, through the high-side MOSFET, into the load via the output inductor, and back to ground. This loop should be minimized and have relatively wide traces.
3. When the high-side MOSFET is off, freewheeling current flows from ground, through the asynchronous diode, into the load via the output inductor, and back to ground. This loop should be minimized and have relatively wide traces.
4. The voltage on the SW node transitions from 0 V to V_{IN} very quickly and is the root cause of many noise issues. It is best to place the asynchronous diode and output inductor close to the device to minimize the size of the SW polygon. Also, keep low-level analog signals (like FB and COMP) away from the SW polygon.
5. To have the highest output voltage accuracy, the output voltage sense trace should be connected as close as practical to the load.
6. Place the compensation components (R_Z, C_Z, and CP) as close as practical to the COMP pin. Place vias to the GND plane as close as practical to these components.
7. Place the bootstrap capacitor (C_{BOOT}) near the BOOT pin and keep the routing from this capacitor to the SW polygon as short as practical.
8. When connecting the input and output ceramic capacitors, use multiple vias to GND and place the vias as close as practical to the pads of the components.
9. To minimize PCB losses and improve system efficiency, the input and output traces should be as wide as practical and be duplicated on multiple layers, if practical.
10. To improve thermal performance, place multiple vias to the GND plane around the anode of the asynchronous diode.
11. The thermal pad under the device must connect to the GND plane using multiple vias. More vias ensure the lowest junction temperature and highest efficiency.
12. EMI/EMC issues are always a concern. Allegro recommends having component locations for an RC snubber from SW to ground. The resistor should be 1206 size.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

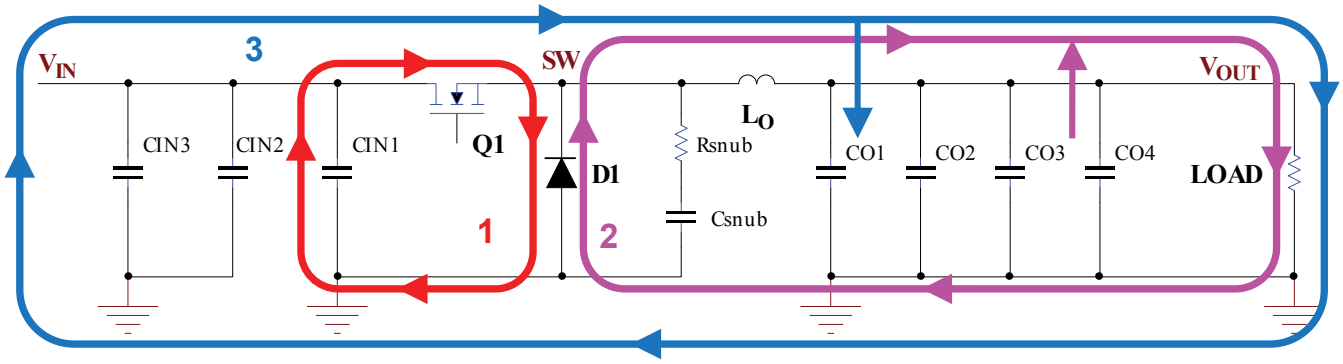


Figure 17: Typical Buck Converter with Critical Paths/Loops Shown

Loop 1 (red): At the instant Q1 turns on, Schottky diode D1, which is very capacitive, must be very quickly shut off (only 5 to 15 ns of charging time). This spike of charging current must come from the local input ceramic capacitor, CIN1. This spike of current is quite large and can be an EMI/EMC issue if the loop is not minimized. Therefore, the input capacitor CIN1 and Schottky diode D1 must be placed on the same (top) layer, be located near each other, and be grounded at virtually the same point on the PCB.

Loop 2 (magenta): When Q1 is off, freewheeling inductor current must flow from ground through diode D1 (SW is at $-V_f$), into the output inductor, out to the load and return via ground. While Q1 is off, the voltage on the output capacitors decreases. The output capacitors and Schottky diode D1 should be placed on the same (top) layer, be located near each other, and be sharing a good, low-inductance ground connection.

Loop 3 (blue): When Q1 is on, current flows from the input supply and input capacitors through the output inductor and into the load and the output capacitors. At this time, the voltage on the output capacitors increases.

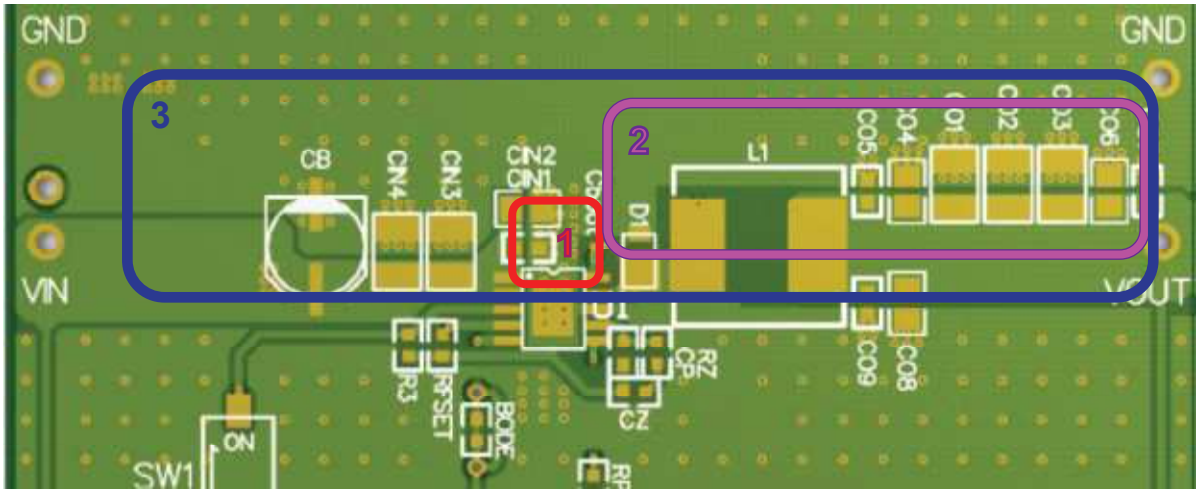


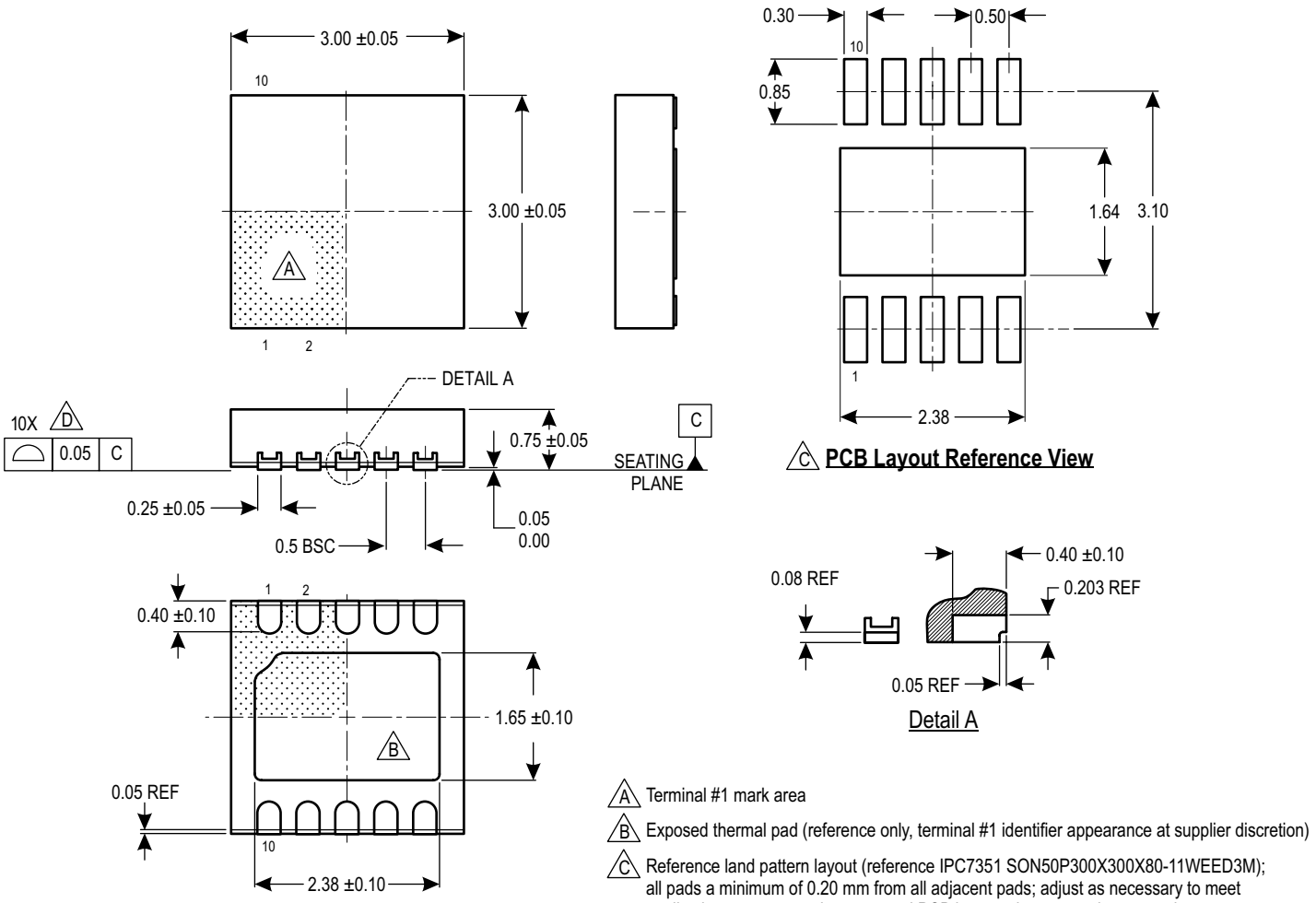
Figure 18: Example PCB Component Placement and Routing

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use

(Reference JEDEC MO-229)
Dimensions in millimeters – NOT TO SCALE
Exact case and lead configuration at supplier discretion within limits shown



A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 SON50P300X300X80-11WEED3M); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed thermal pad and terminals

Figure 19: Package EJ, Wettable Flank DFN-10 with Exposed Thermal Pad

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Revision History

Number	Date	Description
–	December 17, 2015	Initial Release
1	May 1, 2020	Minor editorial updates
2	June 26, 2025	Updated electrical characteristic conditions (pages 6–9) and made minor editorial changes throughout (all pages), including: addition of hyperlinks for cross references (figures, tables, equations, and sections), minimization of use of uppercase letters, elimination of the use of the future tense (“will”) where appropriate, removal of offensive language (“normal” changed to “typical”), use of numbers for footnotes instead of symbols, removal of footnotes from pages where they are not mentioned, enclosure of footnote reference in the text within brackets, and formatting of table grid lines (not marked).

Copyright 2025, Allegro MicroSystems.

Allegro MicroSystems reserves the right to make, from time to time, such departures from the detail specifications as may be required to permit improvements in the performance, reliability, or manufacturability of its products. Before placing an order, the user is cautioned to verify that the information being relied upon is current.

Allegro’s products are not to be used in any devices or systems, including but not limited to life support devices or systems, in which a failure of Allegro’s product can reasonably be expected to cause bodily harm.

The information included herein is believed to be accurate and reliable. However, Allegro MicroSystems assumes no responsibility for its use; nor for any infringement of patents or other rights of third parties which may result from its use.

Copies of this document are considered uncontrolled documents.

For the latest version of this document, visit our website:
www.allegromicro.com

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com