FM4: S6E2C Series Microcontroller Datasheet

200 MHz Arm® Cortex®-M4F High-Performance MCU

The FM4 S6E2C Series provides a highly integrated single chip solution with 200 MHz of CPU power, up to 2 Mbytes of dual banked high speed on chip flash memory, up to 256 Kbytes of on chip SRAM, and integrated peripheral features including IEEE 1588 compliant 10/100 base Ethernet, CAN, CAN-FD, USB and inverter control timers.

S6E2C Series Features

High Performance MCU Subsystem

- 675 CoreMark®, 200 MHz Arm® Cortex®-M4F CPU
- 365 µA/MHz active current with 2.7 V to 5.5 V operating voltage
- Ultra-low power 1.0 µA real-time clock (RTC) operating current
- Up to 2 MB flash and 256 KB SRAM with 16 KB flash accelerator
- Error-Correcting Code (ECC) support, hardware WDT1, low-voltage detect, and clock supervisor blocks for safety-critical applications

Analog Subsystem

- 3x independent 12-bit, 2-Msps ADCs with a 32-channel multiplexer input
- 2x dedicated 12-bit digital-to-analog converters (DACs)

Digital Subsystem

- 3x Multi-Function Timers (MFT)
- 9x Programmable Pulse Generators (PPG)
- 16x Base Timers, 4x Quadrature Position/Revolution Counters (QPRC)
- 1x Dual Timer, 2x CRC, and Watch Counter
- 16 channels of Multi-Function Serial (MFS) interfaces configurable as SPI, UART, I2C, or LIN
- 2x USB, 2x CAN, CAN-FD, IEEE 1588 Ethernet, High-Speed Quad-SPI (HS-QSPI), I^2S, and External Bus Interfaces

Ecosystem for Cypress FM4 MCUs

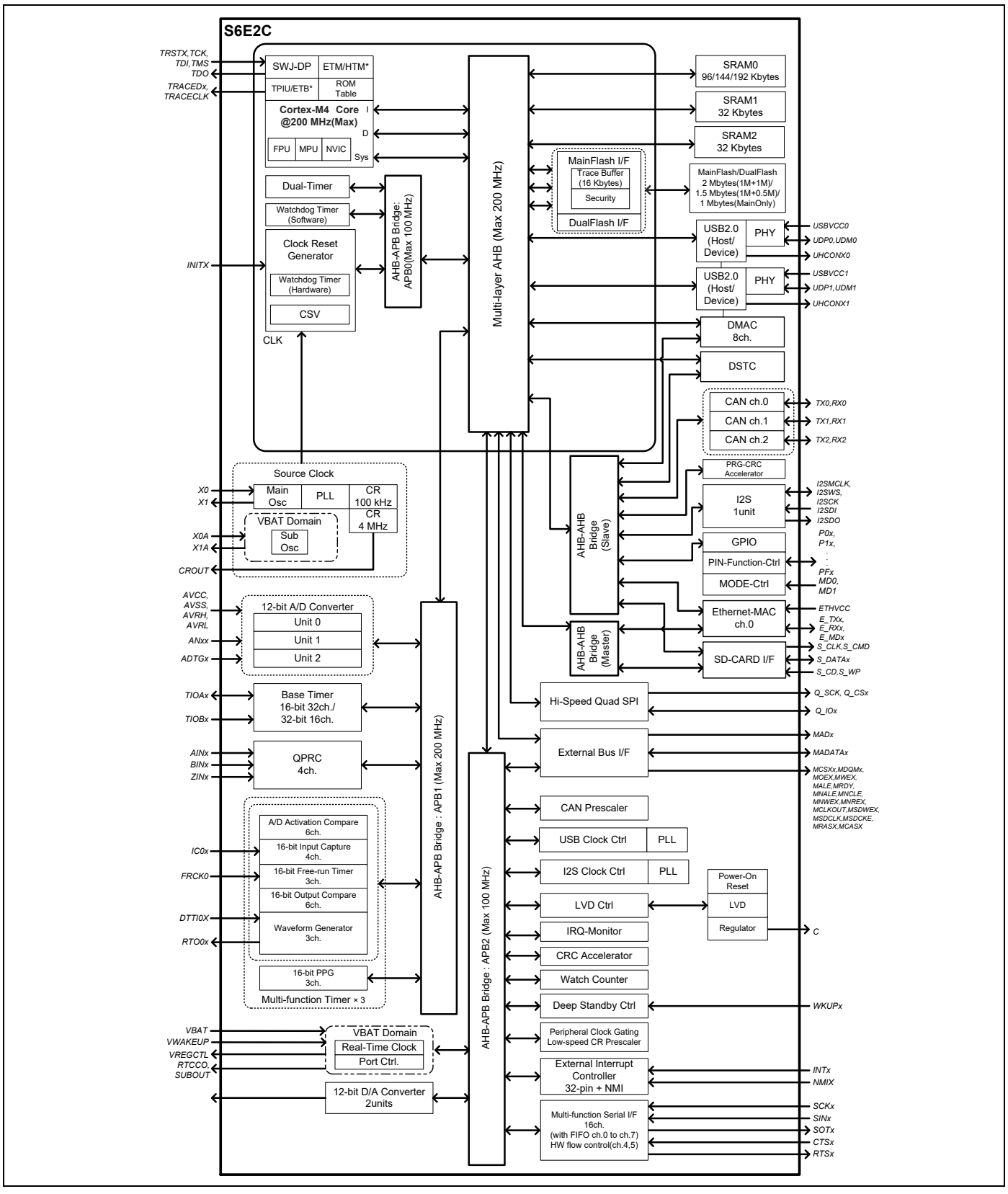
Cypress provides a wealth of data at http://www.cypress.com to help you to select the right MCU for your design, and to help you to quickly and effectively integrate the device into your design. Following is an abbreviated list for FM4 MCUs:

- Overview: Product Portfolio, Product Roadmap
- Product Selectors: FM4 MCUs
- Application notes: Cypress offers a large number of FM4 application notes covering a broad range of topics, from basic to advanced level. Recommended application notes for getting started with FM4 family of MCUs are:
  - AN204468 - FM4 I2S USB MP3 Player Application 32-Bit Microcontroller FM4 Family: This application note describes the general structure of the I²S USB MP3Player software example, its single modules in detail and how it is used.
  - AN204471 - FM4 S6E2CC Series External Memory Programmer: This document describes use of the MCU Universal Programmer as an off-line programmer for Quad SPI flash memory programming on the S6E2CC Series SK.
  - AN203277 - FM 32-Bit Microcontroller Family Hardware Design Considerations: This application note reviews several topics for designing a hardware system around FM0+, FM3, and FM4 family MCUs. Subjects include power system, reset, crystal, and other pin connections, and programming and debugging interfaces.
  - AN202488 - FM4 MB9BF56x and S6E2HG Series MCU - Servo Motor Speed Control: This document covers servo motor speed control solution on FM4 MCU - MB9BF56x and S6E2HG.
  - AN99235 - FM4 S6E2HG Series MCU - 16-Bit PWM Using a Base Timer: Cypress FM4 Family of 32-bit Arm® Cortex®-M4 Microcontrollers FM4 S6E2H Series Motor Control Arm® Cortex®-M4 MCU
  - AN202487 - Differences Among FM0+, FM3, and FM4 32-Bit Microcontrollers: Highlights the peripheral differences in Cypress's FM family MCUs. It provides dedicated sections for each peripheral and contains lists, tables, and descriptions of peripheral feature and register differences.
  - AN204438 - How to Setup Flash Security for FM0+, FM3 and FM4 Families: This application note describes how to setup the Flash Security for FM0+, FM**3**, and FM4 devices
- Development kits:
  - FM4-U120-9B560 - Arm® Cortex®-M4 MCU Starter Kit with USB and CMSIS-DAP
  - FM4-216-ETHERNET Arm® Cortex®-M4 MCU Development Kit with Ethernet, CAN and USB Host
  - FM4-176L-S6E2CC-ETH - Arm® Cortex®-M4 MCU Starter Kit with Ethernet and USB Host
  - FM4-176L-S6E2GM - Arm® Cortex®-M4 MCU Pioneer Kit with Ethernet and USB Host
- Peripheral Manuals

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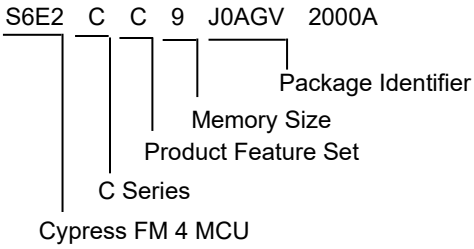
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1. Block Diagram



2. Product Lineup

Here is the information used in the tables below:



Memory Size

Memory Size		S6E2Cx8	S6E2Cx9	S6E2CxA
On-chip flash memory		1024 Kbytes	1536 Kbytes	2048 Kbytes
On-chip	SRAM	128 Kbytes	192 Kbytes	256 Kbytes
	SRAM0	64 Kbytes	128 Kbytes	192 Kbytes
	SRAM1	32 Kbytes	32 Kbytes	32 Kbytes
	SRAM2	32 Kbytes	32 Kbytes	32 Kbytes

Package Dependent Features

Feature	H0AGV	J0AGV	J0AGB	L0AGL
Pin count and package type	144 LQFP: LQS144 (0.5 mm pitch)	176 LQFP: LQP176 (0.5 mm pitch)	192 BGA: LBE192 (0.8 mm pitch)	216 LQFP: LQQ216 (0.4 mm pitch)
High-speed quad SPI	N/A	1 unit		
External bus interface	Addr: 25-bit, Data: 8-/16-bit CS: 8, SRAM, NOR flash NAND flash 4-bit ETM/HTM	Addr: 25-bit, Data: 8-/16-bit CS: 9, SRAM, NOR flash, NAND flash SDRAM 8-bit ETM/HTM		Addr: 25-bit, Data: 8-/16-/**32**-bit CS: 9, SRAM, NOR flash, NAND flash, SDRAM 16-bit ETM/HTM
I^2S	N/A	1 unit		
I/O ports	120	152		190
12-bit A/D converter	24 ch (3 units)	32 ch (3 units)		

Note:

- *See 15 Package Dimensions for detailed information on each package.*

Product Feature Set

Feature			S6E2CC	S6E2C5	S6E2C4	S6E2C3	S6E2C2	S6E2C1
CPU			Cortex-M4F, MPU, NVIC 128 ch					
	Freq.		200 MHz					
Power supply voltage range			2.7V to 5.5V					
USB2.0 (device/host)			2 ch	2 ch	N/A	2 ch	2 ch	N/A
Ethernet-MAC			1ch. MII: 1 ch /RMII: 1 ch	N/A	N/A	N/A	1ch. MII: 1 ch /RMII: 1 ch	N/A
CAN			2 ch	2 ch	2 ch	N/A	N/A	N/A
CAN-FD (non-ISO CAN FD)			1 ch	1 ch	1 ch	N/A	N/A	N/A
DMAC			8ch					
DSTC			256 ch					
Multi-function serial interface (UART/CSIO/LIN/I^{2}C)			16ch (Max) ch 0 to ch 7 : FIFO, ch 8 to ch 15 : No FIFO					
Base timer (PWC/Reload timer/PWM/PPG)			16 ch (Max)					
MF timer	A/D activation compare	6 ch	3 units (Max)					
	Input capture	4 ch						
	Free-run timer	3 ch						
	Output compare	6 ch						
	Waveform generator	3 ch						
	PPG	3 ch						
SD card interface			1 unit					
QPRC			4 ch (Max)					
Dual timer			1 unit					
Real-time clock			1 unit					
Watch counter			1 unit					
CRC accelerator			Yes (fixed, programmable)					
Watchdog timer			1 ch (SW) + 1 ch (HW)					
External interrupts			32 pins (Max)+ NMI × 1					
12-bit D/A converter			2 units (Max)					
CSV (clock supervisor)			Yes					
LVD (low-voltage detector)			2 ch					
Built-in CR	High-speed		4 MHz					
	Low-speed		100 kHz					
Debug function			SWJ-DP/ETM/HTM					
Unique ID			Yes					

Notes:

- *Because of package pin limitations, not all functions within the device can be brought out to external pins. You must carefully work out the pin allocation needed for your design.*
  You must use the port relocate function of the I/O port according to your function use.
- *See 12.4.3 Built-In CR Oscillation Characteristics for the accuracy of the built-in CR.*

3. Detailed Device Features

Devices in the S6E2C Series are highly integrated 32-bit microcontrollers with high performance and competitive cost. This series is based on the Arm Cortex-M4F processor with on-chip flash memory and SRAM. The series has peripherals such as motor control timers, A/D converters, and communications interfaces (USB, CAN, UART, CSIO (SPI), I^2C, LIN). The products that are described in this datasheet are placed into TYPE3-M4 product categories "FM4 Family Peripheral Manual Main Part (002-04856)."

32-bit Arm Cortex-M4F Core

- Processor version: r0p1
- Up to 200 MHz frequency operation
- FPU built-in
- Support DSP instructions
- Memory protection unit (MPU): improves the reliability of an embedded system
- Integrated nested vectored interrupt controller (NVIC): 1 NMI (non-maskable interrupt) and 128 peripheral interrupts and 16 priority levels
- 24-bit system timer (Sys Tick): system timer for OS task management

On-chip Memories

- Flash memory

This series is based on two independent on-chip flash memories.

  - Up to 2048 Kbytes
  - Built-in flash accelerator system with 16 Kbytes trace buffer memory
  - Read access to flash memory that can be achieved without wait-cycle up to an operating frequency of 72 MHz. Even at the operating frequency more than 72 MHz, an equivalent single cycle access to flash memory can be obtained by the flash accelerator system.
  - Security function for code protection

- SRAM

This is composed of three independent SRAMs (SRAM0, SRAM1 and SRAM2). SRAM0 is connected to the I-code bus and D-code bus of Cortex-M4F core. SRAM1 and SRAM2 are connected to system bus of Cortex-M4F core.

  - SRAM0: up to 192 Kbytes
  - SRAM1: 32 Kbytes
  - SRAM2: 32 Kbytes

External Bus Interface

- Supports SRAM, NOR, NAND flash and SDRAM device
- Up to 9 chip selects CS0 to CS8 (CS8 is only for SDRAM)
- 8-/16-/32-bit data width
- Up to 25-bit address bus
- Maximum Access size: 256M byte
- Supports address/data multiplexing
- Supports external RDY function

USB Interface (Max two channels)

The USB interface is composed of a device and a host.

- USB device
  - USB 2.0 Full-speed supported
  - Max 6 EndPoint supported
    - EndPoint 0 is control transfer
    - EndPoint 1, 2 can be selected bulk-transfer, interrupt-transfer or isochronous-transfer
    - EndPoint 3 to 5 can select bulk-transfer or interrupt-transfer
    - EndPoint 1 to 5 comprise double buffer
  - The size of each endpoint is as follows.
    - Endpoint 0, 2 to 5: 64 byte
    - EndPoint 1: 256 byte

- USB host
  - USB2.0 Full-Speed/Low-Speed supported
  - Bulk-transfer, interrupt-transfer, and isochronous-transfer support
  - USB Device connected/dis-connected automatically detect
  - IN/OUT token handshake packet automatically
  - Max 256-byte packet length supported
  - Wake-up function supported

CAN Interface (Max two channels)

- Compatible with CAN specification 2.0A/B
- Maximum transfer rate: 1 Mbps
- Built-in 32-message buffer

CAN-FD Interface (One channel)

- Compatible with CAN Specification 2.0A/B
- Maximum transfer rate: 5 Mbps
- Message buffer for receiver: up to 192 messages
- Message buffer for transmitter: up to 32 messages
- CAN with flexible data rate (non-ISO CAN FD)
- Notes:
  - CAN FD cannot communicate between non-ISO CAN FD and ISO CAN FD, because non-ISO CAN FD and ISO CAN FD are different frame format.
  - About the problem of "non-ISO CAN FD", see the White Paper from CiA(CAN in Automation). http://www.can-newsletter.org/engineering/standardization/141222_can-fd-and-crc-issued_white-paper_bosch

Multi-function Serial Interface (Max 16 Channels)

- Separate 64 byte receive and transmit FIFO buffers for channels 0 to 7.
- Operation mode is selectable for each channel from the following:
  - UART
  - CSIO (SPI)
  - LIN
  - I^2C
- UART
  - Full-duplex double buffer
  - Selection with or without parity supported
  - Built-in dedicated baud rate generator
  - External clock available as a serial clock
  - Various error detect functions available (parity errors, framing errors, and overrun errors)
- CSIO (SPI)
  - Full-duplex double buffer
  - Built-in dedicated baud rate generator
  - Overrun error detect function available
  - Serial chip select function (ch 6 and ch 7 only)
  - Supports high-speed SPI (ch 4 and ch 6 only)
  - Data length 5 to 16-bit
- LIN
  - LIN protocol Rev.2.1 supported
  - Full-duplex double buffer
  - Master/slave mode supported
  - LIN break field generation (can change to 13- to 16-bit length)
  - LIN break delimiter generation (can change to 1- to 4-bit length)
  - Various error detect functions available (parity errors, framing errors, and overrun errors)
- I^2C
  - Standard mode (Max 100 kbps)/Fast mode (Max 400 kbps) supported
  - Fast mode Plus (Fm+) (Max 1000 kbps, only for ch 3 = ch A and ch 7 = ch B) supported

DMA Controller (Eight Channels)

DMA controller has an independent bus, so the CPU and DMA controller can process simultaneously.

- Eight independently configured and operated channels
- Transfer can be started by software or request from the built-in peripherals
- Transfer address area: 32-bit (4 GB)
- Transfer mode: Block transfer/Burst transfer/Demand transfer
- Transfer data type: bytes/half-word/word
- Transfer block count: 1 to 16
- Number of transfers: 1 to 65536

DSTC (Descriptor System Data Transfer Controller; 256 channels)

The DSTC can transfer data at high-speed without going via the CPU. The DSTC adopts the descriptor system and, following the specified contents of the descriptor that has already been constructed on the memory, can access directly the memory/peripheral device and perform the data-transfer operation.

It supports the software activation, the hardware activation, and the chain activation functions.

A/D Converter (Max 32 Channels)

- 12-bit A/D Converter
  - Successive approximation type
  - Built-in three units
  - Conversion time: 0.5 µs at 5 V
  - Priority conversion available (priority at two levels)
  - Scanning conversion mode
  - Built-in FIFO for conversion data storage (for SCAN conversion: 16 steps, for priority conversion: 4 steps)

D/A Converter (Max two channels)

- R-2R type
- 12-bit resolution

Base Timer (Max 16 channels)

Operation mode is selected from the following for each channel:

- 16-bit PWM timer
- 16-bit PPG timer
- 16-/32-bit reload timer
- 16-/32-bit PWC timer

General Purpose I/O Port

This series can use its pins as general purpose I/O ports when they are not used for external bus or peripherals; moreover, the port relocate function is built in. It can set the I/O port to which the peripheral function can be allocated.

- Capable of pull-up control per pin
- Capable of reading pin level directly
- Built-in port-relocate function
- Up to 120 high-speed general-purpose I/O ports in 144-pin package
- Some pins 5 V tolerant I/O.
  See "5. Pin Descriptions" and "6. I/O Circuit Type" for the corresponding pins.

Multi-function Timer (Max three units)

The multi-function timer is composed of the following blocks:

Minimum resolution: 5.00 ns

- 16-bit free-run timer × 3 ch/unit
- Input capture × 4 ch/unit
- Output compare × 6 ch/unit
- A/D activation compare × 6 ch/unit
- Waveform generator × 3 ch/unit
- 16-bit PPG timer × 3 ch/unit

The following functions can be used to achieve the motor control:

- PWM signal output function
- DC chopper waveform output function
- Dead time function
- Input capture function
- A/D convertor activate function
- DTIF (motor emergency stop) interrupt function

Real-Time Clock (RTC)

The real-time clock can count year, month, day, hour, minute, second, or day of the week from 00 to 99.

- Interrupt function with specifying date and time (year/month/day/hour/minute) is available. This function is also available by specifying only year, month, day, hour, or minute.
- Timer interrupt function after set time or each set time.
- Capable of rewriting the time with continuing the time count.
- Leap year automatic count is available.

Quadrature Position/Revolution Counter (QPRC; Max four channels)

The Quadrature Position/Revolution Counter (QPRC) is used to measure the position of the position encoder. It is also possible to use up/down counter.

- The detection edge of the three external event input pins AIN, BIN and ZIN is configurable.
- 16-bit position counter
- 16-bit revolution counter
- Two 16-bit compare registers

Dual Timer (32-/16-bit Down Counter)

The dual timer consists of two programmable 32-/16-bit down counters.
Operation mode is selectable from the following for each channel:

- Free-running
- Periodic (= Reload)
- One shot

Watch Counter

The watch counter is used for wake up from low-power consumption mode. It is possible to select the main clock, sub clock, built-in High-speed CR clock, or built-in low-speed CR clock as the clock source.

- Interval timer: up to 64 s (max) with a sub clock of 32.768 kHz

External Interrupt Controller Unit

- External interrupt input pin: Max 32 pins
- Include one non-maskable interrupt (NMI)

Watchdog Timer (Two channels)

A watchdog timer can generate interrupts or a reset when a time-out value is reached.

This series consists of two different watchdogs: a "hardware" watchdog and a "software" watchdog.

The hardware watchdog timer is clocked by low-speed internal CR oscillator. The hardware watchdog is thus active in any power saving mode except RTC mode and Stop mode.

Cyclic Redundancy Check (CRC) Accelerator

The CRC accelerator helps to verify data transmission or storage integrity.

CCITT CRC16 and IEEE-802.3 CRC32 are supported.

- CCITT CRC16 generator polynomial: 0x1021
- IEEE-802.3 CRC32 generator polynomial: 0x04C11DB7

Programmable Cyclic Redundancy Check (PRGCRC) Accelerator

The CRC accelerator helps a verify data transmission or storage integrity.

CCITT CRC16, IEEE-802.3 CRC32 and generating polynomial are supported.

- CCITT CRC16 generator polynomial: 0x1021
- IEEE-802.3 CRC32 generator polynomial: 0x04C11DB7
- Generating polynomial

SD Card Interface

It is possible to use the SD card that conforms to the following standards.

- Part 1 Physical Layer Specification version 3.01
- Part E1 SDIO Specification version 3.00
- Part A2 SD Host Controller Standard Specification version 3.00
- 1-bit or 4-bit data bus

Ethernet-MAC

- Compliant with IEEE802.3 specification
- 10 Mbps/100 Mbps data transfer rates supported
- MII/RMII for external PHY device supported.
- MII: Max one channel
- RMII: Max one channel
- Full-duplex and half-duplex mode supported.
- Wake-ON-LAN supported
- Built-in dedicated descriptor-system DMAC
- Built-in 2 Kbytes transmit FIFO and 2 Kbytes receive FIFO.
- Compliant IEEE1588-2008 (PTP)

I²S (Inter-IC Sound Bus) Interface (TX x one channel, RX x one channel)

- Supports three transfer protocols
  - I²S17
  - Left justified
  - DSP mode
  - Separate clock generation block for flexible system integration options
- Master/slave mode selectable
- RX Only, TX Only or TX and RX simultaneous operation selectable
- Word length is programmable from 7-bits to 32-bits
- RX/TX FIFO integrated (RX: 66 words x 32-bits, TX: 66 words x 32-bits)
- DMA, interrupts, or polling based data transfer supported

High-speed Quad SPI

Up to 66 MHz clock rates for very fast data transfers to and from SPI compatible devices.

Up to 256 Mbytes of memory mapped address space.

- Single data rate (SDR)
- Supports single, dual, and quad data modes
- Built-in direct mode and command sequencer mode
  - Direct mode: Access by use of transmission FIFO/reception FIFO (up to 16 word x 32 bit)
  - Command sequencer mode: Automatic access assigned to external device area.

Clock and Reset

- Clocks

Five clock sources (two external oscillators, two internal CR oscillators, and Main PLL) that are dynamically selectable.

  - Main clock: 4 MHz to 48 MHz
  - Sub clock: 30 kHz to 100 kHz
  - High-speed internal CR clock: 4 MHz
  - Low-speed internal CR clock: 100 kHz
  - Main PLL Clock

- Resets
  - Reset requests from INITX pin
  - Power on reset
  - Software reset
  - Watchdog timer reset
  - Low-voltage detector reset
  - Clock supervisor reset

Clock Supervisor (CSV)

Clocks generated by internal CR oscillators are used to supervise abnormality of the external clocks.

- External OSC clock failure (clock stop) is detected, reset is asserted.
- External OSC frequency anomaly is detected, interrupt or reset is asserted.

Low-Voltage Detector (LVD)

This Series include two-stage monitoring of voltage on the VCC pins. When the voltage falls below the voltage that has been set, the low-voltage detector function generates an interrupt or reset.

- LVD1: error reporting via interrupt
- LVD2: auto-reset operation

Low-power Consumption mode

Six low power consumption modes are supported.

- Sleep
- Timer
- RTC
- Stop
- Deep standby RTC (selectable from with/without RAM retention)
- Deep standby stop (selectable from with/without RAM retention)

Peripheral Clock Gating

The system can reduce the current consumption of the total system with gating the operation clocks of peripheral functions not used.

VBAT

The consumption power during the RTC operation can be reduced by supplying the power supply independent from the RTC (calendar circuit)/32 kHz oscillation circuit. The following circuits can also be used.

- RTC
- 32-kHz oscillation circuit
- Power-on circuit
- Back up register: 32 bytes
- Port circuit

Debug

- Serial wire JTAG debug port (SWJ-DP)
- Embedded trace macrocells (ETM) provide comprehensive debug and trace facilities.
- AHB trace macrocells (HTM)

Unique ID

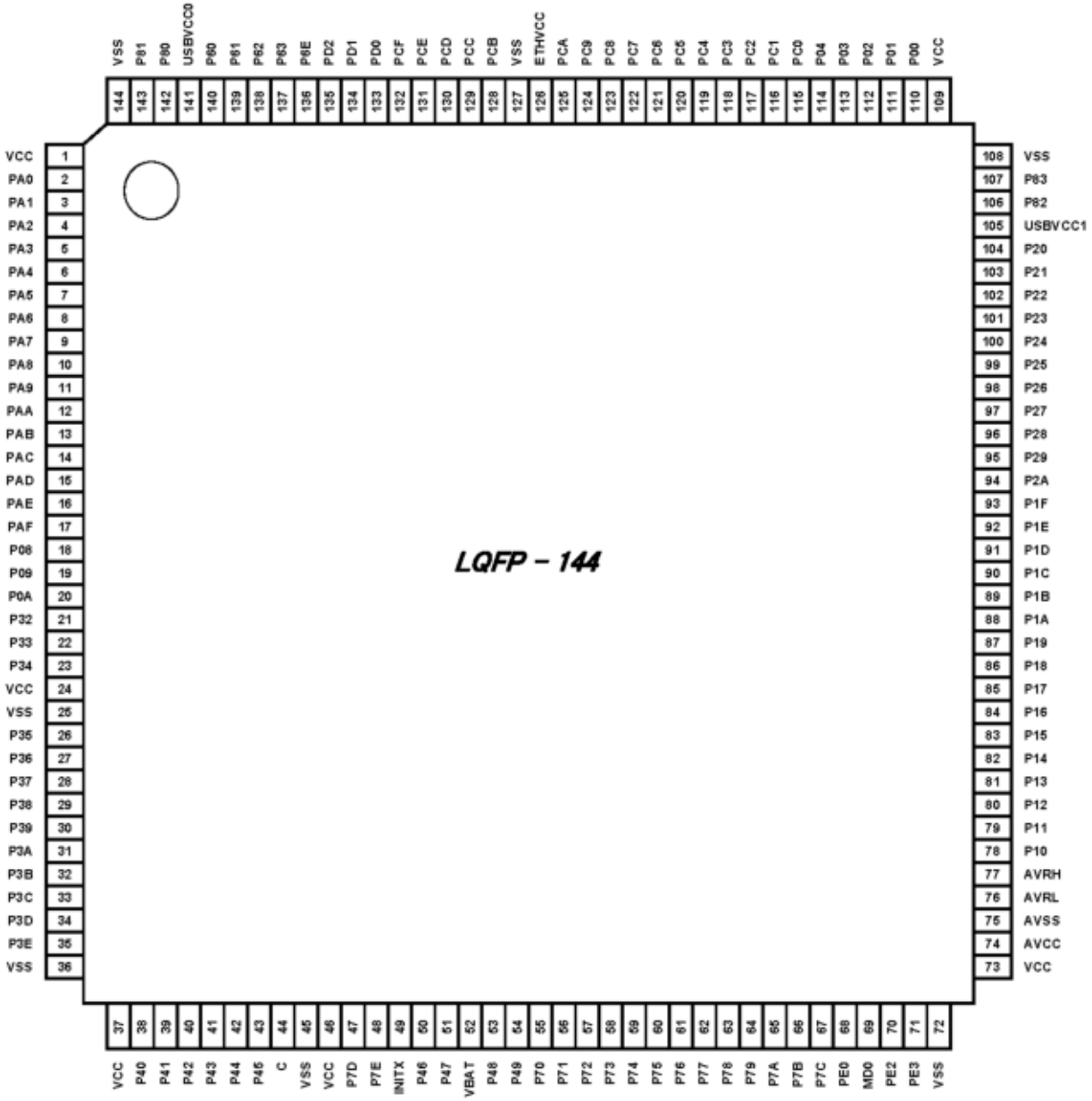
Unique value of the device (41-bit) is set.

Power Supply

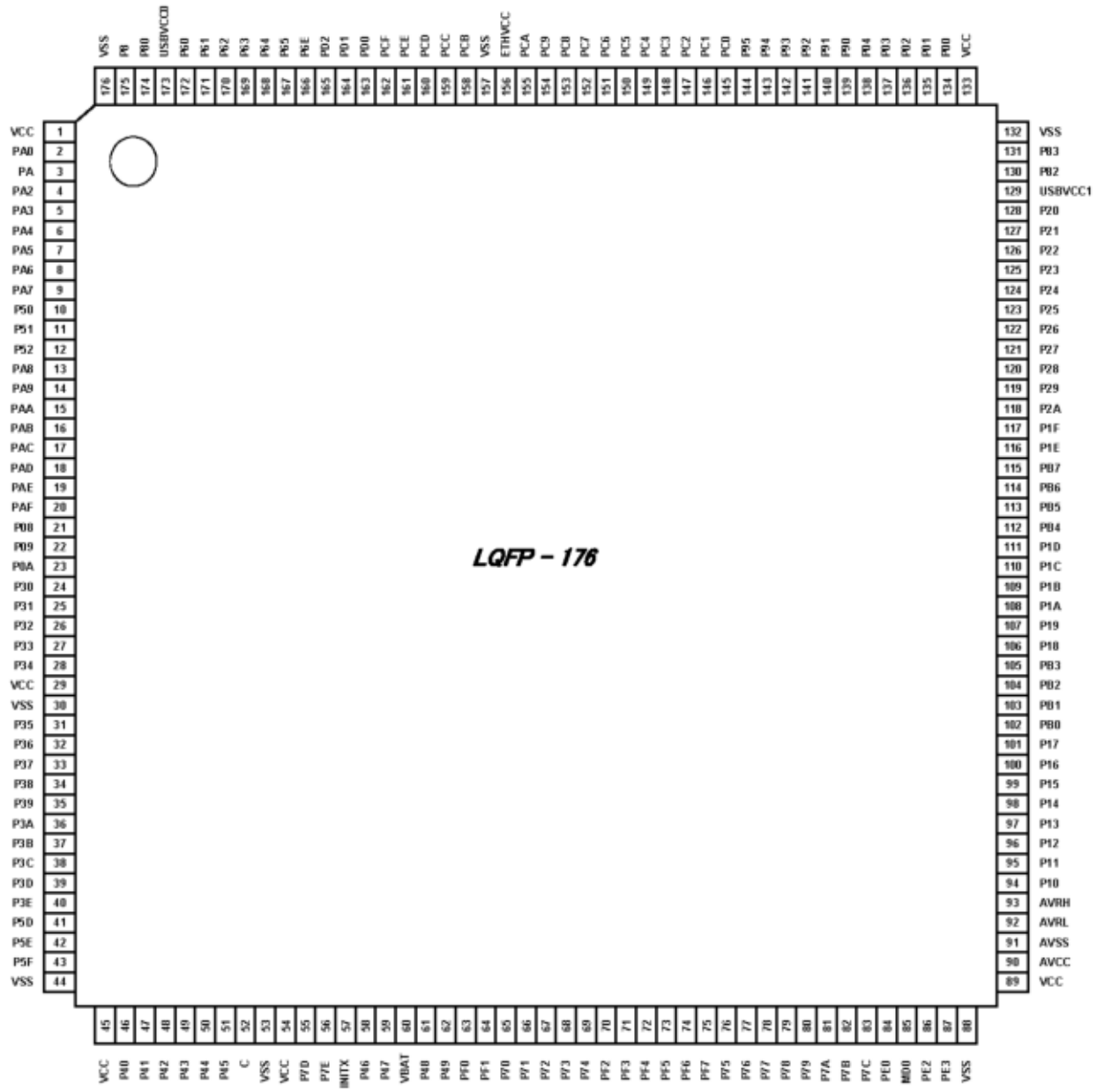
- Five power supplies
  - Wide range voltage:
    VCC = 2.7 V to 5.5 V
  - Power supply for USB ch 0 I/O:
    USBVCC0 = 3.0 V to 3.6 V (when USB is used)
    = 2.7 V to 5.5 V (when GPIO is used)
  - Power supply for USB ch 1 I/O:
    USBVCC1 = 3.0 V to 3.6 V (when USB is used)
    = 2.7 V to 5.5 V (when GPIO is used)
  - Power supply for Ethernet-MAC I/O:
    ETHVCC = 3.0 V to 5.5 V (when Ethernet is used.)
    = 2.7 V to 5.5 V (when GPIO is used)
  - Power supply for VBAT:
    VBAT = 1.65 V to 5.5 V

4. Pin Assignments

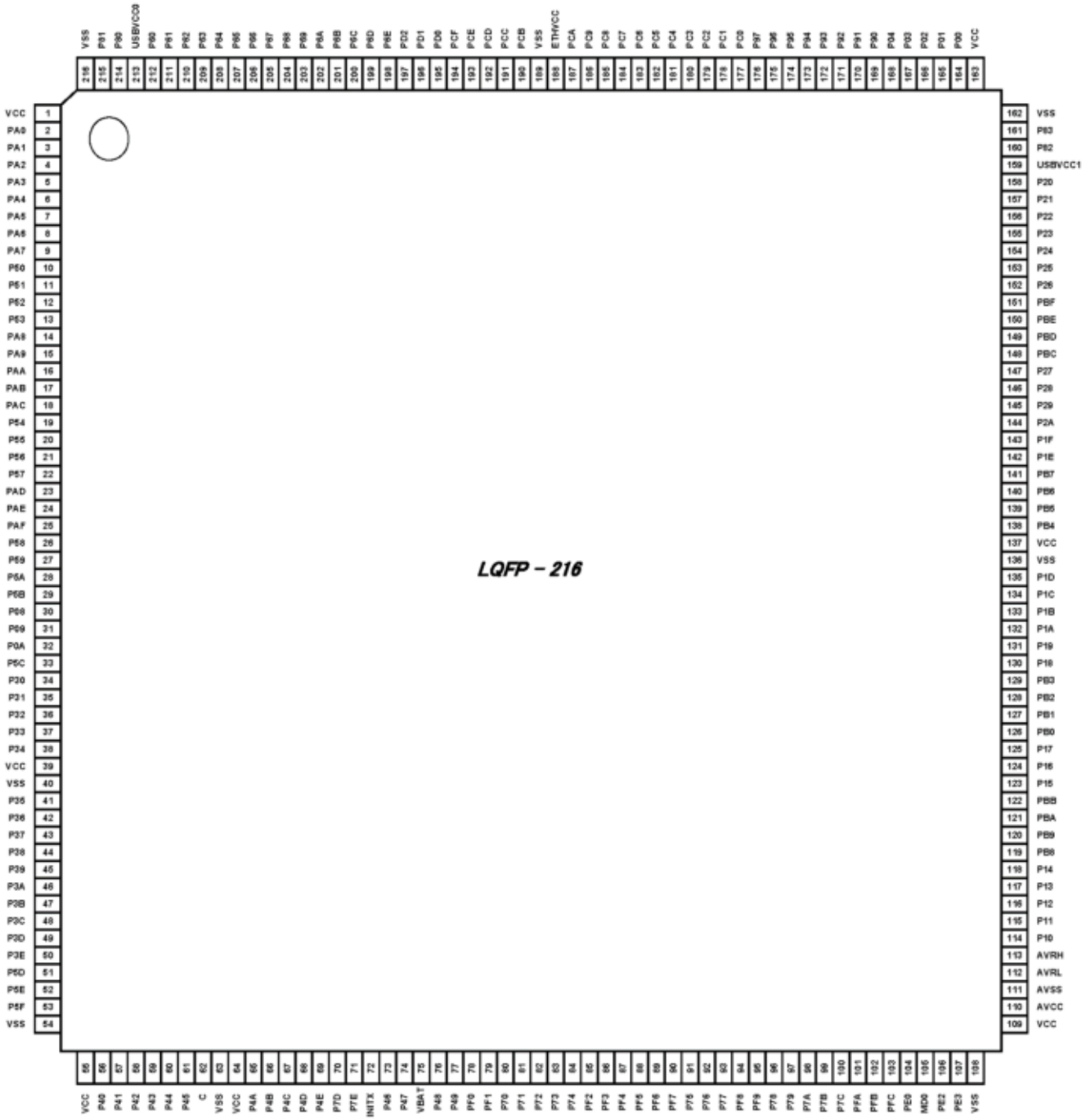
LQS144



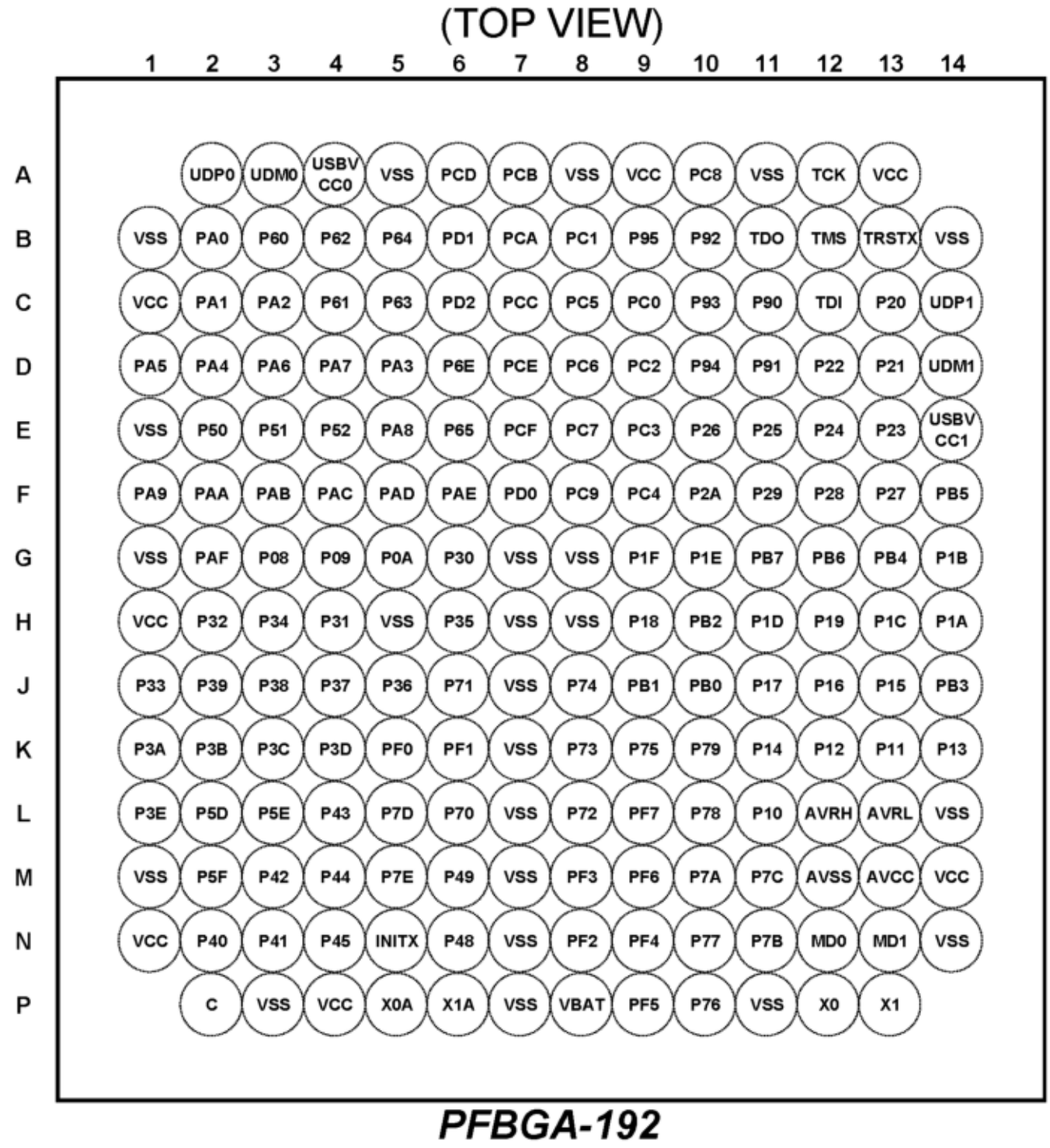
LQP176


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PA3 5
PA4 6
PA5 7
PA6 8
PA7 9
P50 10
P51 11
P52 12
PA8 13
PA9 14
PAA 15
PAB 16
PAC 17
PAD 18
PAE 19
PAF 20
P08 21
P09 22
P0A 23
P30 24
P31 25
P32 26
P33 27
P34 28
VCC 29
VSS 30
P35 31
P36 32
P37 33
P38 34
P39 35
P3A 36
P3B 37
P3C 38
P3D 39
P3E 40
P5D 41
P5E 42
P5F 43
VSS 44
132 VSS
131 PB3
130 PB2
129 USBVCC1
128 P20
127 P21
126 P22
125 P23
124 P24
123 P25
122 P26
121 P27
120 P28
119 P29
118 P2A
117 P1F
116 P1E
115 PB7
114 PB6
113 PB5
112 PB4
111 P1D
110 P1C
109 P1B
108 P1A
107 P19
106 P18
105 PB3
104 PB2
103 PB1
102 PB0
101 P17
100 P16
99 P15
98 P14
97 P13
96 P12
95 P11
94 P10
93 AVRH
92 AVRL
91 AVSS
90 AVCC
89 VCC
45 VCC
46 P40
47 P41
48 P42
49 P43
50 P44
51 P45
52 C
53 VSS
54 VCC
55 P7D
56 P7E
57 INITX
58 P46
59 P47
60 VBAT
61 P48
62 P49
63 P50
64 PF1
65 P70
66 P71
67 P72
68 P73
69 P74
70 PF2
71 PF3
72 PF4
73 P75
74 P76
75 P77
76 P75
77 P76
78 P77
79 P78
80 P79
81 P7A
82 P7B
83 P7C
84 PE0
85 MD0
86 PE2
87 PE3
88 VSS

LQQ216



LBE192



PFBGA-192

5. Pin Descriptions

List of Pin Functions

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel.

Use the extended port function register (EPFR) to select the pin.

Pin Number				Pin Name	Alternate Pin Functions							I/O Circuit Type	Pin State Type
LQQ216	LQP176	LQS144	LBE192										
1	1	1	C1	VCC								-	-
2	2	2	B2	PA0	RTO20_0 (PPG20_0)	TIOA8_0	AIN2_0	INT00_0	MADATA00_0			G	K
3	3	3	C2	PA1	RTO21_0 (PPG20_0)	TIOA9_0	BIN2_0	MADATA01_0				G	I
4	4	4	C3	PA2	RTO22_0 (PPG22_0)	TIOA10_0	ZIN2_0	MADATA02_0				G	I
5	5	5	D5	PA3	RTO23_0 (PPG22_0)	TIOA11_0	MADATA03_0					G	I
6	6	6	D2	PA4	RTO24_0 (PPG24_0)	TIOA12_0	MADATA04_0					G	I
7	7	7	D1	PA5	SIN1_0	RTO25_0 (PPG24_0)	TIOA13_0	INT01_0	MADATA05_0			G	K
8	8	8	D3	PA6	SOT1_0 (SDA1_0))	DTTI2X_0	MADATA06_0					E	I
9	9	9	D4	PA7	SCK1_0 (SCL1_0)	IC20_0	MADATA07_0					E	I
10	10	-	E2	P50	SCS72_0	RTO00_1 (PPG00_1)	TIOA8_2	MADATA16_0				E	I
11	11	-	E3	P51	SCS73_0	RTO01_1 (PPG00_1)	TIOB8_2	MADATA17_0				E	I
12	12	-	E4	P52	RTO02_1 (PPG02_1)	TIOA9_2	MADATA18_0					E	I
13	-	-	-	P53	RTO03_1 (PPG02_1)	TIOB9_2	MADATA19_0					E	I
14	13	10	E5	PA8	SIN7_0	IC21_0	INT02_0	WKUP1	MADATA08_0			I	Q
15	14	11	F1	PA9	SOT7_0 (SDA7_0)	IC22_0	MADATA09_0					N	I
16	15	12	F2	PAA	SCK7_0 (SCL7_0)	IC23_0	IC23_0	MADATA10_0				N	I
17	16	13	F3	PAB	SCS70_0	RX0_0	FRCK2_0	INT03_0	MADATA11_0			E	K
18	17	14	F4	PAC	SCS71_0	TX0_0	TIOB8_0	AIN3_0	MADATA12_0			E	I
19	-	-	-	P54	SIN15_1	RTO04_1 (PPG04_1)	TIOA10_2	INT00_2	MADATA20_0			E	K
20	-	-	-	P55	SOT15_1 (SDA15_1)	RTO05_1 (PPG04_1)	TIOB10_2	MADATA21_0				E	I
21	-	-	-	P56	SCK15_1 (SCL15_1)	DTTI0X_1	TIOB0_1	MADATA22_0				E	I
22	-	-	-	P57	IC00_1	TIOB1_1	MADATA23_0					E	I
23	18	15	F5	PAD	SCK3_0 (SCL3_0)	TIOB9_0	BIN3_0	MADATA13_0				N	I
24	19	16	F6	PAE	ADTG_0	SOT3_0 (SDA3_0)	TIOB10_0	ZIN3_0	MADATA14_0			N	I
25	20	17	G2	PAF	SIN3_0	TIOB11_0	INT16_0	MADATA15_0	-			I	K
26	-	-	-	P58	SIN11_1	IC01_1	TIOB2_1	MADATA24_0	INT02_2			E	K

Pin Number				Pin Name	Alternate Pin Functions							I/O Circuit Type	Pin State Type
LQQ216	LQP176	LQS144	LBE192										
27	-	-	-	P59	SOT11_1 (SDA11_1)	IC02_1	TIOB3_1	MADATA25_0				E	I
28	-	-	-	P5A	SCK11_1 (SCL11_1)	IC03_1	TIOB4_1	MADATA26_0				E	I
29	-	-	-	P5B	FRCK0_1	TIOB5_1	MADATA27_0					E	I
30	21	18	G3	P08	SIN14_0	TIOB12_0	INT17_0	MDQM0_0				E	K
31	22	19	G4	P09	SOT14_0 (SDA14_0)	TIOB13_0	INT18_0	MDQM1_0				E	K
32	23	20	G5	P0A	ADTG_1	SCK14_0 (SCL14_0)	AIN2_1	MCLKOUT_0				L	I
33	-	-	-	P5C	TIOA11_2	MADATA28_0	RTCCO_1	SUBOUT_1				E	I
34	24	-	G6	P30	RX0_1	TIOA13_2	INT03_2	MDQM2_0	I2SDI0_0			E	K
35	25	-	H4	P31	TX0_1	TIOB13_2	MDQM3_0	I2SCK0_0				E	I
36	26	21	H2	P32	BIN2_1	INT19_0	S_DATA1_0					L	K
37	27	22	J1	P33	FRCK0_0	ZIN2_1	S_DATA0_0					L	I
38	28	23	H3	P34	IC03_0	INT00_1	S_CLK_0					L	K
39	29	24	H1	VCC								-	-
40	30	25	H5	VSS								-	-
41	31	26	H6	P35	IC02_0	INT01_1	S_CMD_0					L	K
42	32	27	J5	P36	IC01_0	INT02_1	S_DATA3_0					L	K
43	33	28	J4	P37	IC00_0	INT03_1	S_DATA2_0					L	K
44	34	29	J3	P38	ADTG_2	DTTI0X_0	S_WP_0					E	I
45	35	30	J2	P39	SIN2_1	RTO00_0 (PPG00_0)	TIOA0_1	AIN3_1	INT16_1	S_CD_0	MAD24_0	G	K
46	36	31	K1	P3A	SOT2_1 (SDA2_1)	RTO01_0 (PPG00_0)	TIOA1_1	BIN3_1	INT17_1	MAD23_0		G	K
47	37	32	K2	P3B	SCK2_1 (SCL2_1)	RTO02_0 (PPG02_0)	TIOA2_1	ZIN3_1	INT18_1	MAD22_0	MNALE_0	G	K
48	38	33	K3	P3C	SIN13_0	RTO03_0 (PPG02_0)	TIOA3_1	INT19_1	MAD21_0	MNCLE_0		G	K
49	39	34	K4	P3D	SOT13_0 (SDA13_0)	RTO04_0 (PPG04_0)	TIOA4_1	MAD20_0	MNWEX_0			G	I
50	40	35	L1	P3E	SCK13_0 (SCL13_0)	RTO05_0 (PPG04_0)	TIOA5_1	MAD19_0	MNREX_0			G	I
51	41	-	L2	P5D	SIN10_1	TIOB11_2	INT01_2	MADATA29_0	I2SMCLK0_0			E	K
52	42	-	L3	P5E	SOT10_1 (SDA10_1)	TIOA12_2	MADATA30_0	I2SDO0_0				E	I

Pin Number				Pin Name	Alternate Pin Functions							I/O Circuit Type	Pin State Type
LQQ216	LQP176	LQS144	LBE192										
53	43	-	M2	P5F	SCK10_1 (SCL10_1)	TIOB12_2	MADATA31_0	I2SWS0_0				E	I
54	44	36	M1	VSS								-	-
55	45	37	N1	VCC								-	-
56	46	38	N2	P40	SIN3_1	RTO10_0 (PPG10_0)	TIOA0_0	AIN0_0	INT23_0	MCSX7_0		G	K
57	47	39	N3	P41	SOT3_1 (SDA3_1)	RTO11_0 (PPG10_0)	TIOA1_0	BIN0_0	MCSX6_0			G	I
58	48	40	M3	P42	SCK3_1 (SCL3_1)	RTO12_0 (PPG12_0)	TIOA2_0	ZIN0_0	MCSX5_0			G	I
59	49	41	L4	P43	SIN15_0	RTO13_0 (PPG12_0)	TIOA3_0	INT04_0	MCSX4_0			G	K
60	50	42	M4	P44	SOT15_0 (SDA15_0)	RTO14_0 (PPG14_0)	TIOA4_0	MCSX3_0				G	I
61	51	43	N4	P45	SCK15_0 (SCL15_0)	RTO15_0 (PPG14_0)	TIOA5_0	MCSX2_0				G	I
62	52	44	P2	C								-	-
63	53	45	P3	VSS								-	-
64	54	46	P4	VCC								-	-
65	-	-	-	P4A	SIN12_1	AIN0_1	INT04_2					E	K
66	-	-	-	P4B	SOT12_1 (SDA12_1)	BIN0_1						E	I
67	-	-	-	P4C	SCK12_1 (SCL12_1)	ZIN0_1						E	I
68	-	-	-	P4D	SCS72_1	RX2_2	INT05_2					E	K
69	-	-	-	P4E	SCS73_1	TX2_2						E	I
70	55	47	L5	P7D	SCK1_1 (SCL1_1)	RX2_0	DTTI1X_0	INT05_0	WKUP2	MCSX1_0		L	Q
71	56	48	M5	P7E	ADTG_7	TX2_0	FRCK1_0	MCSX0_0				L	I
72	57	49	N5	INITX								B	C
73	58	50	P5	P46	X0A							P	S
74	59	51	P6	P47	X1A							Q	T
75	60	52	P8	VBAT								-	-
76	61	53	N6	P48	VREGCTL							O	U
77	62	54	M6	P49	VWAKEUP							O	U
78	63	-	K5	PF0	SCS63_0	RX2_1	FRCK1_1	TIOA15_1	INT22_1			E	K
79	64	-	K6	PF1	SCS62_0	TX2_1	TIOB15_1	INT23_1				E	K
80	65	55	L6	P70	ADTG_8	SIN1_1	INT06_0	MRDY_0				I	K
81	66	56	J6	P71	SOT1_1 (SDA1_1)	MAD00_0						E	I
82	67	57	L8	P72	SIN9_0	TIOB0_0	INT07_0	MAD01_0				E	K
83	68	58	K8	P73	SOT9_0 (SDA9_0)	TIOB1_0	MAD02_0					E	I
84	69	59	J8	P74	SCK9_0 (SCL9_0)	TIOB2_0	MAD03_0					E	I
85	70	-	N8	PF2	RTO10_1 (PPG10_1)	TIOA6_1	MRASX_0					L	I

Pin Number				Pin Name	Alternate Pin Functions							I/O Circuit Type	Pin State Type
LQQ216	LQP176	LQS144	LBE192										
86	71	-	M8	PF3	RTO11_1 (PPG10_1)	TIOB6_1	INT05_1	MCASX_0				L	K
87	72	-	N9	PF4	RTO12_1 (PPG12_1)	TIOA7_1	INT06_1	MSDWEX_0				L	K
88	73	-	P9	PF5	RTO13_1 (PPG12_1)	TIOB7_1	INT07_1	MCSX8_0				L	K
89	74	-	M9	PF6	RTO14_1 (PPG14_1)	TIOA14_1	INT20_1	MSDCKE_0				L	K
90	75	-	L9	PF7	RTO15_1 (PPG14_1)	TIOB14_1	INT21_1	MSDCLK_0				L	K
91	76	60	K9	P75	SIN8_0	TIOB3_0	AIN1_0	INT20_0	MAD04_0			E	K
92	77	61	P10	P76	SOT8_0 (SDA8_0)	TIOB4_0	BIN1_0	MAD05_0				E	I
93	78	62	N10	P77	SCK8_0 (SCL8_0)	TIOB5_0	ZIN1_0	MAD06_0				E	I
94	-	-	-	PF8	SCS70_1	DTTI1X_1	AIN1_1					E	I
95	-	-	-	PF9	SCS71_1	IC10_1	BIN1_1					E	I
96	79	63	L10	P78	SIN6_0	IC10_0	INT21_0	MAD07_0				E	K
97	80	64	K10	P79	SOT6_0 (SDA6_0)	IC11_0	MAD08_0					L	I
98	81	65	M10	P7A	SCK6_0 (SCL6_0)	IC12_0	MAD09_0					L	I
99	82	66	N11	P7B	DA1	SCS60_0	IC13_0	INT22_0				R	J
100	83	67	M11	P7C	DA0	SCS61_0	INT04_1					R	J
101	-	-	-	PFA	SCK7_1 (SCL7_1)	IC11_1	ZIN1_1					E	I
102	-	-	-	PFB	SOT7_1 (SDA7_1)	IC12_1	INT07_2					E	K
103	-	-	-	PFC	SIN7_1	IC13_1	INT06_2					E	K
104	84	68	N13	PE0	MD1							C	E
105	85	69	N12	MD0								J	D
106	86	70	P12	PE2	X0							A	A
107	87	71	P13	PE3	X1							A	B
108	88	72	N14	VSS								-	-
109	89	73	M14	VCC								-	-
110	90	74	M13	AVCC								-	-
111	91	75	M12	AVSS								-	-
112	92	76	L13	AVRL								-	-
113	93	77	L12	AVRH								-	-
114	94	78	L11	P10	AN00	SIN10_0	TIOA0_2	AIN0_2	INT08_0			F	M
115	95	79	K13	P11	AN01	SOT10_0 (SDA10_0)	TIOB0_2	BIN0_2				F	L
116	96	80	K12	P12	AN02	SCK10_0 (SCL10_0)	TIOA1_2	ZIN0_2				F	L
117	97	81	K14	P13	AN03	SIN6_1	RX1_1	INT25_1				F	M
118	98	82	K11	P14	AN04	SOT6_1 (SDA6_1)	TX1_1					F	L
119	-	-	-	PB8	ADTG_6	SCS63_1	INT08_2	TRACED8				E	O

Pin Number				Pin Name	Alternate Pin Functions							I/O Circuit Type	Pin State Type
LQQ216	LQP176	LQS144	LBE192										
120	-	-	-	PB9	SIN9_1	AIN2_2	INT09_2	TRACED9				E	O
121	-	-	-	PBA	SOT9_1 (SDA9_1)	BIN2_2	TRACED10					E	N
122	-	-	-	PBB	SCK9_1 (SCL9_1)	ZIN2_2	TRACED11					E	N
123	99	83	J13	P15	AN05	SIN11_0	TIOB1_2	AIN1_2	INT09_0			F	M
124	100	84	J12	P16	AN06	SOT11_0 (SDA11_0)	TIOA2_2	BIN1_2				F	L
125	101	85	J11	P17	AN07	SCK11_0 (SCL11_0)	TIOB2_2	ZIN1_2				F	L
126	102	-	J10	PB0	AN16	SCK6_1 (SCL6_1)	TIOA9_1					F	L
127	103	-	J9	PB1	AN17	SCS60_1	TIOB9_1	INT08_1				F	M
128	104	-	H10	PB2	AN18	SCS61_1	TIOA10_1	INT09_1				F	M
129	105	-	J14	PB3	AN19	SCS62_1	TIOB10_1					F	L
130	106	86	H9	P18	AN08	SIN2_0	TIOA3_2	INT10_0				F	M
131	107	87	H12	P19	AN09	SOT2_0 (SDA2_0)	TIOB3_2	INT24_1	TRACECLK			F	O
132	108	88	H14	P1A	AN10	SCK2_0 (SCL2_0)	TIOA4_2	TRACED0				F	N
133	109	89	G14	P1B	AN11	SIN12_0	TIOB4_2	INT11_0	TRACED1			F	O
134	110	90	H13	P1C	AN12	SOT12_0 (SDA12_0)	TIOA5_2	TRACED2				F	N
135	111	91	H11	P1D	AN13	SCK12_0 (SCL12_0)	TIOB5_2	TRACED3				F	N
136	-	-	-	VSS								-	-
137	-	-	-	VCC								-	-
138	112	-	G13	PB4	AN20	SIN8_1	TIOA11_1	INT10_1	TRACED4			F	O
139	113	-	F14	PB5	AN21	SOT8_1 (SDA8_1)	TIOB11_1	INT11_1	TRACED5			F	O
140	114	-	G12	PB6	AN22	SCK8_1 (SCL8_1)	TIOA12_1	TRACED6				F	N
141	115	-	G11	PB7	AN23	TIOB12_1	TRACED7					F	N
142	116	92	G10	P1E	AN14	TIOA8_1	INT26_1	MAD10_0				F	M
143	117	93	G9	P1F	AN15	RTS5_0	TIOB8_1	INT27_1	MAD11_0			F	M
144	118	94	F10	P2A	AN24	CTS5_0	MAD12_0					F	L
145	119	95	F11	P29	AN25	SCK5_0 (SCL5_0)	MAD13_0					F	L
146	120	96	F12	P28	AN26	SOT5_0 (SDA5_0)	MAD14_0					F	L
147	121	97	F13	P27	AN27	SIN5_0	INT24_0	MAD15_0				F	M
148	-	-	-	PBC	TX1_2	TRACED12						E	N
149	-	-	-	PBD	SCK0_1 (SCL0_1)	RX1_2	AIN3_2	INT10_2	TRACED13			E	O
150	-	-	-	PBE	SOT0_1 (SDA0_1)	BIN3_2	TRACED14					E	N
151	-	-	-	PBF	SIN0_1	ZIN3_2	INT11_2	TRACED15				E	O
152	122	98	E10	P26	TX1_0	MAD16_0						E	I
153	123	99	E11	P25	AN28	RX1_0	INT25_0	MAD17_0				F	M
154	124	100	E12	P24	AN29	TIOA13_1	MAD18_0					F	L

Pin Number				Pin Name	Alternate Pin Functions							I/O Circuit Type	Pin State Type
LQQ216	LQP176	LQS144	LBE192										
155	125	101	E13	P23	UHCONX1	AN30	SCK0_0 (SCL0_0)	TIOB13_1				F	L
156	126	102	D12	P22	AN31	SOT0_0 (SDA0_0)	INT26_0					F	M
157	127	103	D13	P21	ADTG_4	SIN0_0	INT27_0	CROUT_0				I	K
158	128	104	C13	P20	NMIX	WKUP0						I	F
159	129	105	E14	USBV CC1								-	-
160	130	106	D14	P82	UDM1							H	R
161	131	107	C14	P83	UDP1							H	R
162	132	108	B14	VSS								-	-
163	133	109	A13	VCC								-	-
164	134	110	B13	P00	TRSTX							E	G
165	135	111	A12	P01	TCK	SWCLK						E	G
166	136	112	C12	P02	TDI							E	G
167	137	113	B12	P03	TMS	SWDIO						E	G
168	138	114	B11	P04	TDO	SWO						E	G
169	139	-	C11	P90	INT12_1	Q_IO3_0						S	K
170	140	-	D11	P91	SIN5_1	INT13_1	Q_IO2_0					S	K
171	141	-	B10	P92	SOT5_1 (SDA5_1)	INT14_1	Q_IO1_0					S	K
172	142	-	C10	P93	SCK5_1 (SCL5_1)	INT15_1	Q_IO0_0					S	K
173	143	-	D10	P94	CTS5_1	Q_SCK_0						S	I
174	144	-	B9	P95	RTS5_1	Q_CS0_0						S	I
175	-	-	-	P96	RX0_2	INT12_2	Q_CS1_0					S	K
176	-	-	-	P97	TX0_2	INT13_2	Q_CS2_0					S	K
177	145	115	C9	PC0	E_RXER							K	V
178	146	116	B8	PC1	TIOB6_0	E_RX03						K	V
179	147	117	D9	PC2	TIOA6_0	E_RX02						K	V
180	148	118	E9	PC3	TIOB7_0	E_RX01						K	V
181	149	119	F9	PC4	TIOA7_0	E_RX00						K	V
182	150	120	C8	PC5	TIOB14_0	E_RXDV						K	V
183	151	121	D8	PC6	TIOA14_0	E_MDIO						K	V
184	152	122	E8	PC7	INT13_0	E_MDC	CROUT_1					E	W
185	153	123	A10	PC8	E_RXCK_REFCK							K	V
186	154	124	F8	PC9	TIOB15_0	E_COL						K	V
187	155	125	B7	PCA	TIOA15_0	E_CRS						K	V
188	156	126	A9	ETHVCC								-	-
189	157	127	A8	VSS								-	-
190	158	128	A7	PCB	INT28_0	E_COUT						L	W
191	159	129	C7	PCC	E_TCK							K	V
192	160	130	A6	PCD	SOT4_1 (SDA4_1)	INT14_0	E_TXER					L	W
193	161	131	D7	PCE	SIN4_1	INT15_0	E_TX03					L	W
194	162	132	E7	PCF	RTS4_1	INT12_0	E_TX02					L	W
195	163	133	F7	PD0	INT30_1	E_TX01						L	W
196	164	134	B6	PD1	INT31_1	E_TX00						L	W
197	165	135	C6	PD2	CTS4_1	FRCK2_1	E_TXEN					L	V
198	166	136	D6	P6E	ADTG_5	SCK4_1 (SCL4_1)	IC23_1	INT29_0	E_PPS			E	W

Pin Number				Pin Name	Alternate Pin Functions							I/O Circuit Type	Pin State Type
LQQ216	LQP176	LQS144	LBE192										
199	-	-	-	P6D	SCK14_1 (SCL14_1)	IC22_1	TIOB6_2					E	I
200	-	-	-	P6C	SOT14_1 (SDA14_1)	IC21_1	TIOA6_2					E	I
201	-	-	-	P6B	SIN14_1	IC20_1	TIOB7_2	INT14_2				E	K
202	-	-	-	P6A	DTTI2X_1	TIOA7_2						E	I
203	-	-	-	P69	RTO20_1 (PPG20_1)	TIOB14_2						E	I
204	-	-	-	P68	SCK13_1 (SCL13_0)	RTO21_1 (PPG20_1)	TIOA14_2					E	I
205	-	-	-	P67	SOT13_1 (SDA13_1)	RTO22_1 (PPG22_1)	TIOB15_2					E	I
206	-	-	-	P66	SIN13_1	RTO23_1 (PPG22_1)	TIOA15_2	INT15_2				E	K
207	167	-	E6	P65	RTO24_1 (PPG24_1)	INT28_1						E	K
208	168	-	B5	P64	CTS4_0	RTO25_1 (PPG24_1)	INT29_1					I	K
209	169	137	C5	P63	ADTG_3	RTS4_0	INT30_0	MOEX_0				L	K
210	170	138	B4	P62	SCK4_0 (SCL4_0)	MWEX_0						L	I
211	171	139	C4	P61	UHCONX0	SOT4_0 (SDA4_0)	MALE_0	RTCCO_0	SUBOUT_0			L	I
212	172	140	B3	P60	SIN4_0	INT31_0	WKUP3					I	Q
213	173	141	A4	USBVCC0								-	-
214	174	142	A3	P80	UDM0							H	R
215	175	143	A2	P81	UDP0							H	R
216	176	144	B1	VSS								-	-
-	-	-	E1									-	-
-	-	-	G1									-	-
-	-	-	P7									-	-
-	-	-	P11									-	-
-	-	-	L14									-	-
-	-	-	A11									-	-
-	-	-	A5									-	-
-	-	-	N7									-	-
-	-	-	M7									-	-
-	-	-	L7									-	-
-	-	-	K7									-	-
-	-	-	J7									-	-
--	-	-	G7									-	-
-	-	-	H7									-	-
-	-	-	H8									-	-
-	-	-	G8									-	-

Signal Descriptions

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel.

Use the extended port function register (EPFR) to select the pin.

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
A/D converter	ADTG_0	A/D converter external trigger input pin	24	19	16	F6
	ADTG_1		32	23	20	G5
	ADTG_2		44	34	29	J3
	ADTG_3		209	169	137	C5
	ADTG_4		157	127	103	D13
	ADTG_5		198	166	136	D6
	ADTG_6		119	-	-	-
	ADTG_7		71	56	48	M5
	ADTG_8		80	65	55	L6
	AN00	A/D converter analog input pin. ANxx describes A/D converter ch xx.	114	94	78	L11
	AN01		115	95	79	K13
	AN02		116	96	80	K12
	AN03		117	97	81	K14
	AN04		118	98	82	K11
	AN05		123	99	83	J13
	AN06		124	100	84	J12
	AN07		125	101	85	J11
	AN08		130	106	86	H9
	AN09		131	107	87	H12
	AN10		132	108	88	H14
	AN11		133	109	89	G14
	AN12		134	110	90	H13
	AN13		135	111	91	H11
	AN14		142	116	92	G10
	AN15		143	117	93	G9
	AN16		126	102	-	J10
	AN17		127	103	-	J9
	AN18		128	104	-	H10
	AN19		129	105	-	J14
	AN20		138	112	-	G13
	AN21		139	113	-	F14
	AN22		140	114	-	G12
	AN23		141	115	-	G11
	AN24		144	118	94	F10
	AN25		145	119	95	F11
	AN26		146	120	96	F12
	AN27		147	121	97	F13
	AN28		153	123	99	E11
	AN29		154	124	100	E12
	AN30		155	125	101	E13
	AN31		156	126	102	D12

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
Base Timer 0	TIOA0_0	Base Timer ch 0 TIOA pin	56	46	38	N2
	TIOA0_1		45	35	30	J2
	TIOA0_2		114	94	78	L11
	TIOB0_0	Base Timer ch 0 TIOB pin	82	67	57	L8
	TIOB0_1		21	-	-	-
	TIOB0_2		115	95	79	K13
Base Timer 1	TIOA1_0	Base Timer ch 1 TIOA pin	57	47	39	N3
	TIOA1_1		46	36	31	K1
	TIOA1_2		116	96	80	K12
	TIOB1_0	Base Timer ch 1 TIOB pin	83	68	58	K8
	TIOB1_1		22	-	-	-
	TIOB1_2		123	99	83	J13
Base Timer 2	TIOA2_0	Base Timer ch 2 TIOA pin	58	48	40	M3
	TIOA2_1		47	37	32	K2
	TIOA2_2		124	100	84	J12
	TIOB2_0	Base Timer ch 2 TIOB pin	84	69	59	J8
	TIOB2_1		26	-	-	-
	TIOB2_2		125	101	85	J11
Base Timer 3	TIOA3_0	Base Timer ch 3 TIOA pin	59	49	41	L4
	TIOA3_1		48	38	33	K3
	TIOA3_2		130	106	86	H9
	TIOB3_0	Base Timer ch 3 TIOB pin	91	76	60	K9
	TIOB3_1		27	-	-	-
	TIOB3_2		131	107	87	H12
Base Timer 4	TIOA4_0	Base Timer ch 4 TIOA pin	60	50	42	M4
	TIOA4_1		49	39	34	K4
	TIOA4_2		132	108	88	H14
	TIOB4_0	Base Timer ch 4 TIOB pin	92	77	61	P10
	TIOB4_1		28	-	-	-
	TIOB4_2		133	109	89	G14
Base Timer 5	TIOA5_0	Base Timer ch 5 TIOA pin	61	51	43	N4
	TIOA5_1		50	40	35	L1
	TIOA5_2		134	110	90	H13
	TIOB5_0	Base Timer ch 5 TIOB pin	93	78	62	N10
	TIOB5_1		29	-	-	-
	TIOB5_2		135	111	91	H11
Base Timer 6	TIOA6_0	Base Timer ch 6 TIOA pin	179	147	117	D9
	TIOA6_1		85	70	-	N8
	TIOA6_2		200	-	-	-
	TIOB6_0	Base Timer ch 6 TIOB pin	178	146	116	B8
	TIOB6_1		86	71	-	M8
	TIOB6_2		199	-	-	-

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
Base Timer 7	TIOA7_0	Base Timer ch 7 TIOA pin	181	149	119	F9
	TIOA7_1		87	72	-	N9
	TIOA7_2		202	-	-	-
	TIOB7_0	Base Timer ch 7 TIOB pin	180	148	118	E9
	TIOB7_1		88	73	-	P9
	TIOB7_2		201	-	-	-
Base Timer 8	TIOA8_0	Base Timer ch 8 TIOA pin	2	2	2	B2
	TIOA8_1		142	116	92	G10
	TIOA8_2		10	10	-	E2
	TIOB8_0	Base Timer ch 8 TIOB pin	18	17	14	F4
	TIOB8_1		143	117	93	G9
	TIOB8_2		11	11	-	E3
Base Timer 9	TIOA9_0	Base Timer ch 9 TIOA pin	3	3	3	C2
	TIOA9_1		126	102	-	J10
	TIOA9_2		12	12	-	E4
	TIOB9_0	Base Timer ch 9 TIOB pin	23	18	15	F5
	TIOB9_1		127	103	-	J9
	TIOB9_2		13	-	-	-
Base Timer 10	TIOA10_0	Base Timer ch 10 TIOA pin	4	4	4	C3
	TIOA10_1		128	104	-	H10
	TIOA10_2		19	-	-	-
	TIOB10_0	Base Timer ch 10 TIOB pin	24	19	16	F6
	TIOB10_1		129	105	-	J14
	TIOB10_2		20	-	-	-
Base Timer 11	TIOA11_0	Base Timer ch 11 の TIOA pin	5	5	5	D5
	TIOA11_1		138	112	-	G13
	TIOA11_2		33	-	-	-
	TIOB11_0	Base Timer ch 11 TIOB pin	25	20	17	G2
	TIOB11_1		139	113	-	F14
	TIOB11_2		51	41	-	L2
Base Timer 12	TIOA12_0	Base Timer ch 12 TIOA pin	6	6	6	D2
	TIOA12_1		140	114	-	G12
	TIOA12_2		52	42	-	L3
	TIOB12_0	Base Timer ch 12 TIOB pin	30	21	18	G3
	TIOB12_1		141	115	-	G11
	TIOB12_2		53	43	-	M2

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
Base Timer 13	TIOA13_0	Base Timer ch 13 TIOA pin	7	7	7	D1
	TIOA13_1		154	124	100	E12
	TIOA13_2		34	24	-	G6
	TIOB13_0	Base Timer ch 13 TIOB pin	31	22	19	G4
	TIOB13_1		155	125	101	E13
	TIOB13_2		35	25	-	H4
Base Timer 14	TIOA14_0	Base Timer ch 14 TIOA pin	183	151	121	D8
	TIOA14_1		89	74	-	M9
	TIOA14_2		204	-	-	-
	TIOB14_0	Base Timer ch 14 TIOB pin	182	150	120	C8
	TIOB14_1		90	75	-	L9
	TIOB14_2		203	-	-	-
Base Timer 15	TIOA15_0	Base Timer ch 15 TIOA pin	187	155	125	B7
	TIOA15_1		78	63	-	K5
	TIOA15_2		206	-	-	-
	TIOB15_0	Base timer ch 15 TIOB pin	186	154	124	F8
	TIOB15_1		79	64	-	K6
	TIOB15_2		205	-	-	-
CAN 0	TX0_0	CAN interface ch 0 TX output pin	18	17	14	F4
	TX0_1		35	25	-	H4
	TX0_2		176	-	-	-
	RX0_0	CAN interface ch 0 RX output pin	17	16	13	F3
	RX0_1		34	24	-	G6
	RX0_2		175	-	-	-
CAN 1	TX1_0	CAN interface ch 1 TX output pin	152	122	98	E10
	TX1_1		118	98	82	K11
	TX1_2		148	-	-	-
	RX1_0	CAN interface ch 1 RX output pin	153	123	99	E11
	RX1_1		117	97	81	K14
	RX1_2		149	-	-	-
CAN 2 (CAN-FD)	TX2_0	CAN-FD interface ch 2 TX output pin	71	56	48	M5
	TX2_1		79	64	-	K6
	TX2_2		69	-	-	-
	RX2_0	CAN-FD interface ch 2 RX input pin	70	55	47	L5
	RX2_1		78	63	-	K5
	RX2_2		68	-	-	-

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
Debugger	SWCLK	Serial wire debug interface clock input pin	165	135	111	A12
	SWDIO	Serial wire debug interface data input/output pin	167	137	113	B12
	SWO	Serial wire viewer output pin	168	138	114	B11
	TCK	JTAG test clock input pin	165	135	111	A12
	TDI	JTAG test data input pin	166	136	112	C12
	TDO	JTAG debug data output pin	168	138	114	B11
	TMS	JTAG test mode state input/output pin	167	137	113	B12
	TRACECLK	Trace CLK output pin of ETM/HTM	131	107	87	H12
	TRACED0	Trace data output pin of ETM/ Trace data output pin of HTM	132	108	88	H14
	TRACED1		133	109	89	G14
	TRACED2		134	110	90	H13
	TRACED3		135	111	91	H11
	TRACED4	Trace data output pin of HTM	138	112	-	G13
	TRACED5		139	113	-	F14
	TRACED6		140	114	-	G12
	TRACED7		141	115	-	G11
	TRACED8		119	-	-	-
	TRACED9		120	-	-	-
	TRACED10		121	-	-	-
	TRACED11		122	-	-	-
	TRACED12		148	-	-	-
	TRACED13		149	-	-	-
	TRACED14		150	-	-	-
	TRACED15		151	-	-	-
	TRSTX	JTAG test reset Input pin	164	134	110	B13

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
External bus	MAD00_0	External bus interface address bus	81	66	56	J6
	MAD01_0		82	67	57	L8
	MAD02_0		83	68	58	K8
	MAD03_0		84	69	59	J8
	MAD04_0		91	76	60	K9
	MAD05_0		92	77	61	P10
	MAD06_0		93	78	62	N10
	MAD07_0		96	79	63	L10
	MAD08_0		97	80	64	K10
	MAD09_0		98	81	65	M10
	MAD10_0		142	116	92	G10
	MAD11_0		143	117	93	G9
	MAD12_0		144	118	94	F10
	MAD13_0		145	119	95	F11
	MAD14_0		146	120	96	F12
	MAD15_0		147	121	97	F13
	MAD16_0		152	122	98	E10
	MAD17_0		153	123	99	E11
	MAD18_0		154	124	100	E12
	MAD19_0		50	40	35	L1
	MAD20_0		49	39	34	K4
	MAD21_0		48	38	33	K3
	MAD22_0		47	37	32	K2
	MAD23_0		46	36	31	K1
	MAD24_0		45	35	30	J2
	MCSX0_0	External bus interface chip select output pin	71	56	48	M5
	MCSX1_0		70	55	47	L5
	MCSX2_0		61	51	43	N4
	MCSX3_0		60	50	42	M4
	MCSX4_0		59	49	41	L4
	MCSX5_0		58	48	40	M3
	MCSX6_0		57	47	39	N3
	MCSX7_0		56	46	38	N2
	MCSX8_0		88	73	-	P9

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
External bus	MADATA00_0	External bus interface data bus (address/data multiplex bus)	2	2	2	B2
	MADATA01_0		3	3	3	C2
	MADATA02_0		4	4	4	C3
	MADATA03_0		5	5	5	D5
	MADATA04_0		6	6	6	D2
	MADATA05_0		7	7	7	D1
	MADATA06_0		8	8	8	D3
	MADATA07_0		9	9	9	D4
	MADATA08_0		14	13	10	E5
	MADATA09_0		15	14	11	F1
	MADATA10_0		16	15	12	F2
	MADATA11_0		17	16	13	F3
	MADATA12_0		18	17	14	F4
	MADATA13_0		23	18	15	F5
	MADATA14_0		24	19	16	F6
	MADATA15_0		25	20	17	G2
	MADATA16_0		10	-	-	-
	MADATA17_0		11	-	-	-
	MADATA18_0		12	-	-	-
	MADATA19_0		13	-	-	-
	MADATA20_0		19	-	-	-
	MADATA21_0		20	-	-	-
	MADATA22_0		21	-	-	-
	MADATA23_0		22	-	-	-
	MADATA24_0		26	-	-	-
	MADATA25_0		27	-	-	-
	MADATA26_0		28	-	-	-
	MADATA27_0		29	-	-	-
	MADATA28_0		33	-	-	-
	MADATA29_0		51	-	-	-
	MADATA30_0		52	-	-	-
	MADATA31_0		53	-	-	-
	MDQM0_0	External bus interface byte mask signal output pin	30	21	18	G3
	MDQM1_0		31	22	19	G4
	MDQM2_0		34	-	-	-
	MDQM3_0		35	-	-	-
	MALE_0	External bus interface address latch enable output signal for multiplex	211	171	139	C4
	MRDY_0	External bus interface external RDY input signal	80	65	55	L6
	MCLKOUT_0	External bus interface external clock output pin	32	23	20	G5

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
External bus	MNALE_0	External bus interface ALE signal to control NAND flash output pin	47	37	32	K2
	MNCLE_0	External bus interface CLE signal to control NAND flash output pin	48	38	33	K3
	MNREX_0	External bus interface read enable signal to control NAND flash	50	40	35	L1
	MNWEX_0	External bus interface write enable signal to control NAND flash	49	39	34	K4
	MOEX_0	External bus interface read enable signal for SRAM	209	169	137	C5
	MWEX_0	External bus interface write enable signal for SRAM	210	170	138	B4
	MSDCLK_0	SDRAM interface SDRAM clock output pin	90	75	-	L9
	MSDCKE_0	SDRAM interface SDRAM clock enable pin	89	74	-	M9
	MRASX_0	SDRAM interface SDRAM column active strobe pin	85	70	-	N8
	MCASX_0	SDRAM interface SDRAM row active strobe pin	86	71	-	M8
	MSDWEX_0	SDRAM interface SDRAM write enable pin	87	72	-	N9
External interrupt	INT00_0	External interrupt request 00 input pin	2	2	2	B2
	INT00_1		38	28	23	H3
	INT00_2		19	-	-	-
	INT01_0	External interrupt request 01 input pin	7	7	7	D1
	INT01_1		41	31	26	H6
	INT01_2		51	41	-	L2
	INT02_0	External interrupt request 02 input pin	14	13	10	E5
	INT02_1		42	32	27	J5
	INT02_2		26	-	-	-
	INT03_0	External interrupt request 03 input pin	17	16	13	F3
	INT03_1		43	33	28	J4
	INT03_2		34	24	-	G6
	INT04_0	External interrupt request 04 input pin	59	49	41	L4
	INT04_1		100	83	67	M11
	INT04_2		65	-	-	-
	INT05_0	External interrupt request 05 input pin	70	55	47	L5
	INT05_1		86	71	-	M8
	INT05_2		68	-	-	-

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
External interrupt	INT06_0	External interrupt request 06 input pin	80	65	55	L6
	INT06_1		87	72	-	N9
	INT06_2		103	-	-	-
	INT07_0	External interrupt request 07 input pin	82	67	57	L8
	INT07_1		88	73	-	P9
	INT07_2		102	-	-	-
	INT08_0	External interrupt request 08 input pin	114	94	78	L11
	INT08_1		127	103	-	J9
	INT08_2		119	-	-	-
	INT09_0	External interrupt request 09 input pin	123	99	83	J13
	INT09_1		128	104	-	H10
	INT09_2		120	-	-	-
	INT10_0	External interrupt request 10 input pin	130	106	86	H9
	INT10_1		138	112	-	G13
	INT10_2		149	-	-	-
	INT11_0	External interrupt request 11 input pin	133	109	89	G14
	INT11_1		139	113	-	F14
	INT11_2		151	-	-	-
	INT12_0	External interrupt request 12 input pin	194	162	132	E7
	INT12_1		169	139	-	C11
	INT12_2		175	-	-	-
	INT13_0	External interrupt request 13 input pin	184	152	122	E8
	INT13_1		170	140	-	D11
	INT13_2		176	-	-	-
	INT14_0	External interrupt request 14 input pin	192	160	130	A6
	INT14_1		171	141	-	B10
	INT14_2		201	-	-	-
	INT15_0	External interrupt request 15 input pin	193	161	131	D7
	INT15_1		172	142	-	C10
	INT15_2		206	-	-	-
	INT16_0	External interrupt request 16 input pin	25	20	17	G2
	INT16_1		45	35	30	J2
	INT17_0	External interrupt request 17 input pin	30	21	18	G3
	INT17_1		46	36	31	K1
	INT18_0	External interrupt request 18 input pin	31	22	19	G4
	INT18_1		47	37	32	K2
	INT19_0	External interrupt request 19 input pin	36	26	21	H2
	INT19_1		48	38	33	K3
	INT20_0	External interrupt request 20 input pin	91	76	60	K9
	INT20_1		89	74	-	M9

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
External interrupt	INT21_0	External interrupt request 21 input pin	96	79	63	L10
	INT21_1		90	75	-	L9
	INT22_0	External interrupt request 22 input pin	99	82	66	N11
	INT22_1		78	63	-	K5
	INT23_0	External interrupt request 23 input pin	56	46	38	N2
	INT23_1		79	64	-	K6
	INT24_0	External interrupt request 24 input pin	147	121	97	F13
	INT24_1		131	107	87	H12
	INT25_0	External interrupt request 25 input pin	153	123	99	E11
	INT25_1		117	97	81	K14
	INT26_0	External interrupt request 26 input pin	156	126	102	D12
	INT26_1		142	116	92	G10
	INT27_0	External interrupt request 27 input pin	157	127	103	D13
	INT27_1		143	117	93	G9
	INT28_0	External interrupt request 28 input pin	190	158	128	A7
	INT28_1		207	167	-	E6
	INT29_0	External interrupt request 29 input pin	198	166	136	D6
	INT29_1		208	168	-	B5
	INT30_0	External interrupt request 30 input pin	209	169	137	C5
	INT30_1		195	163	133	F7
	INT31_0	External interrupt request 31 input pin	212	172	140	B3
	INT31_1		196	164	134	B6
	NMIX	Non-maskable interrupt input pin	158	128	104	C13

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
GPIO	P00	General-purpose I/O port 0	164	134	110	B13
	P01		165	135	111	A12
	P02		166	136	112	C12
	P03		167	137	113	B12
	P04		168	138	114	B11
	P08		30	21	18	G3
	P09		31	22	19	G4
	P0A		32	23	20	G5
	P10	General-purpose I/O port 1	114	94	78	L11
	P11		115	95	79	K13
	P12		116	96	80	K12
	P13		117	97	81	K14
	P14		118	98	82	K11
	P15		123	99	83	J13
	P16		124	100	84	J12
	P17		125	101	85	J11
	P18		130	106	86	H9
	P19		131	107	87	H12
	P1A		132	108	88	H14
	P1B		133	109	89	G14
	P1C		134	110	90	H13
	P1D		135	111	91	H11
	P1E		142	116	92	G10
	P1F		143	117	93	G9
	P20	General-purpose I/O port 2	158	128	104	C13
	P21		157	127	103	D13
	P22		156	126	102	D12
	P23		155	125	101	E13
	P24		154	124	100	E12
	P25		153	123	99	E11
	P26		152	122	98	E10
	P27		147	121	97	F13
	P28		146	120	96	F12
	P29		145	119	95	F11
	P2A		144	118	94	F10

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
GPIO	P30	General-purpose I/O port 3	34	24	-	G6
	P31		35	25	-	H4
	P32		36	26	21	H2
	P33		37	27	22	J1
	P34		38	28	23	H3
	P35		41	31	26	H6
	P36		42	32	27	J5
	P37		43	33	28	J4
	P38		44	34	29	J3
	P39		45	35	30	J2
	P3A		46	36	31	K1
	P3B		47	37	32	K2
	P3C		48	38	33	K3
	P3D		49	39	34	K4
	P3E		50	40	35	L1
	P40	General-purpose I/O port 4	56	46	38	N2
	P41		57	47	39	N3
	P42		58	48	40	M3
	P43		59	49	41	L4
	P44		60	50	42	M4
	P45		61	51	43	N4
	P46		73	58	50	P5
	P47		74	59	51	P6
	P48		76	61	53	N6
	P49		77	62	54	M6
	P4A		65	-	-	-
	P4B		66	-	-	-
	P4C		67	-	-	-
	P4D		68	-	-	-
	P4E		69	-	-	-

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
GPIO	P50	General-purpose I/O port 5	10	10	-	E2
	P51		11	11	-	E3
	P52		12	12	-	E4
	P53		13	-	-	-
	P54		19	-	-	-
	P55		20	-	-	-
	P56		21	-	-	-
	P57		22	-	-	-
	P58		26	-	-	-
	P59		27	-	-	-
	P5A		28	-	-	-
	P5B		29	-	-	-
	P5C		33	-	-	-
	P5D		51	41	-	L2
	P5E		52	42	-	L3
	P5F		53	43	-	M2
	P60	General-purpose I/O port 6	212	172	140	B3
	P61		211	171	139	C4
	P62		210	170	138	B4
	P63		209	169	137	C5
	P64		208	168	-	B5
	P65		207	167	-	E6
	P66		206	-	-	-
	P67		205	-	-	-
	P68		204	-	-	-
	P69		203	-	-	-
	P6A		202	-	-	-
	P6B		201	-	-	-
	P6C		200	-	-	-
	P6D		199	-	-	-
	P6E		198	166	136	D6

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
GPIO	P70	General-purpose I/O port 7	80	65	55	L6
	P71		81	66	56	J6
	P72		82	67	57	L8
	P73		83	68	58	K8
	P74		84	69	59	J8
	P75		91	76	60	K9
	P76		92	77	61	P10
	P77		93	78	62	N10
	P78		96	79	63	L10
	P79		97	80	64	K10
	P7A		98	81	65	M10
	P7B		99	82	66	N11
	P7C		100	83	67	M11
	P7D		70	55	47	L5
	P7E		71	56	48	M5
	P80	General-purpose I/O port 8	214	174	142	A3
	P81		215	175	143	A2
	P82		160	130	106	D14
	P83		161	131	107	C14
	P90	General-purpose I/O port 9	169	139	-	C11
	P91		170	140	-	D11
	P92		171	141	-	B10
	P93		172	142	-	C10
	P94		173	143	-	D10
	P95		174	144	-	B9
	P96		175	-	-	-
	P97		176	-	-	-

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
GPIO	PA0	General-purpose I/O port A	2	2	2	B2
	PA1		3	3	3	C2
	PA2		4	4	4	C3
	PA3		5	5	5	D5
	PA4		6	6	6	D2
	PA5		7	7	7	D1
	PA6		8	8	8	D3
	PA7		9	9	9	D4
	PA8		14	13	10	E5
	PA9		15	14	11	F1
	PAA		16	15	12	F2
	PAB		17	16	13	F3
	PAC		18	17	14	F4
	PAD		23	18	15	F5
	PAE		24	19	16	F6
	PAF		25	20	17	G2
	PB0	General-purpose I/O port B	126	102	-	J10
	PB1		127	103	-	J9
	PB2		128	104	-	H10
	PB3		129	105	-	J14
	PB4		138	112	-	G13
	PB5		139	113	-	F14
	PB6		140	114	-	G12
	PB7		141	115	-	G11
	PB8		119	-	-	-
	PB9		120	-	-	-
	PBA		121	-	-	-
	PBB		122	-	-	-
	PBC		148	-	-	-
	PBD		149	-	-	-
	PBE		150	-	-	-
	PBF		151	-	-	-

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
GPIO	PC0	General-purpose I/O port C	177	145	115	C9
	PC1		178	146	116	B8
	PC2		179	147	117	D9
	PC3		180	148	118	E9
	PC4		181	149	119	F9
	PC5		182	150	120	C8
	PC6		183	151	121	D8
	PC7		184	152	122	E8
	PC8		185	153	123	A10
	PC9		186	154	124	F8
	PCA		187	155	125	B7
	PCB		190	158	128	A7
	PCC		191	159	129	C7
	PCD		192	160	130	A6
	PCE		193	161	131	D7
	PCF		194	162	132	E7
	PD0	General-purpose I/O port D	195	163	133	F7
	PD1		196	164	134	B6
	PD2		197	165	135	C6
	PE0	General-purpose I/O port E	104	84	68	N13
	PE2		106	86	70	P12
	PE3		107	87	71	P13
	PF0	General-purpose I/O port F	78	63	-	K5
	PF1		79	64	-	K6
	PF2		85	70	-	N8
	PF3		86	71	-	M8
	PF4		87	72	-	N9
	PF5		88	73	-	P9
	PF6		89	74	-	M9
	PF7		90	75	-	L9
	PF8		94	-	-	-
	PF9		95	-	-	-
	PFA		101	-	-	-
	PFB		102	-	-	-
	PFC		103	-	-	-

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
Multi-Function Serial 0	SIN0_0	Multi-function serial interface ch 0 input pin	157	127	103	D13
	SIN0_1		151	-	-	-
	SOT0_0 (SDA0_0)	Multi-function serial interface ch 0 output pin	156	126	102	D12
	SOT0_1 (SDA0_1)	This pin operates as SOT0 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA0 when it is used in an I^2C (operation mode 4).	150	-	-	-
	SCK0_0 (SCL0_0)	Multi-function serial interface ch 0 clock I/O pin	155	125	101	E13
	SCK0_1 (SCL0_1)	This pin operates as SCK0 when it is used in a CSIO (operation mode 2) and as SCL0 when it is used in an I^2C (operation mode 4)	149	-	-	-
Multi-Function Serial 1	SIN1_0	Multi-function serial interface ch 1 input pin	7	7	7	D1
	SIN1_1		80	65	55	L6
	SOT1_0 (SDA1_0)	Multi-function serial interface ch 1 output pin	8	8	8	D3
	SOT1_1 (SDA1_1)	This pin operates as SOT1 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA1 when it is used in an I2C (operation mode 4).	81	66	56	J6
	SCK1_0 (SCL1_0)	Multi-function serial interface ch 1 clock I/O pin	9	9	9	D4
	SCK1_1 (SCL1_1)	This pin operates as SCK1 when it is used in a CSIO (operation mode 2) and as SCL1 when it is used in an I^2C (operation mode 4).	70	55	47	L5
Multi-Function Serial 2	SIN2_0	Multi-function serial interface ch 2 input pin	130	106	86	H9
	SIN2_1		45	35	30	J2
	SOT2_0 (SDA2_0)	Multi-function serial interface ch 2 output pin	131	107	87	H12
	SOT2_1 (SDA2_1)	This pin operates as SOT2 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA2 when it is used in an I^2C (operation mode 4).	46	36	31	K1
	SCK2_0 (SCL2_0)	Multi-function serial interface ch 2 clock I/O pin	132	108	88	H14
	SCK2_1 (SCL2_1)	This pin operates as SCK2 when it is used in a CSIO (operation mode 2) and as SCL2 when it is used in an I^2C (operation mode 4).	47	37	32	K2

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
Multi-Function Serial 3	SIN3_0	Multi-function serial interface ch 3 input pin	25	20	17	G2
	SIN3_1		56	46	38	N2
	SOT3_0 (SDA3_0)	Multi-function serial interface ch 3 output pin	24	19	16	F6
	SOT3_1 (SDA3_1)	This pin operates as SOT3 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA3 when it is used in an I^2C (operation mode 4).	57	47	39	N3
	SCK3_0 (SCL3_0)	Multi-function serial interface ch 3 clock I/O pin	23	18	15	F5
	SCK3_1 (SCL3_1)	This pin operates as SCK3 when it is used in a CSIO (operation modes 2) and as SCL3 when it is used in an I^2C (operation mode 4).	58	48	40	M3
Multi-Function Serial 4	SIN4_0	Multi-function serial interface ch 4 input pin	212	172	140	B3
	SIN4_1		193	161	131	D7
	SOT4_0 (SDA4_0)	Multi-function serial interface ch 4 output pin	211	171	139	C4
	SOT4_1 (SDA4_1)	This pin operates as SOT4 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA4 when it is used in an I^2C (operation mode 4).	192	160	130	A6
	SCK4_0 (SCL4_0)	Multi-function serial interface ch 4 clock I/O pin	210	170	138	B4
	SCK4_1 (SCL4_1)	This pin operates as SCK4 when it is used in a CSIO (operation mode 2) and as SCL4 when it is used in an I^2C (operation mode 4).	198	166	136	D6
	CTS4_0	Multi-function serial interface ch 4 CTS input pin	208	168	-	B5
	CTS4_1		197	165	135	C6
	RTS4_0	Multi-function serial interface ch 4 RTS output pin	209	169	137	C5
	RTS4_1		194	162	132	E7

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
Multi-Function Serial 5	SIN5_0	Multi-function serial interface ch 5 input pin	147	121	97	F13
	SIN5_1		170	140	-	D11
	SOT5_0 (SDA5_0)	Multi-function serial interface ch 5 output pin	146	120	96	F12
	SOT5_1 (SDA5_1)	This pin operates as SOT5 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA5 when it is used in an I²C (operation mode 4).	171	141	-	B10
	SCK5_0 (SCL5_0)	Multi-function serial interface ch 5 clock I/O pin	145	119	95	F11
	SCK5_1 (SCL5_1)	This pin operates as SCK5 when it is used in a CSIO (operation mode 2) and as SCL5 when it is used in an I²C (operation mode 4).	172	142	-	C10
	CTS5_0	Multi-function serial interface ch 5 CTS input pin	144	118	94	F10
	CTS5_1		173	143	-	D10
	RTS5_0	Multi-function serial interface ch 5 RTS output pin	143	117	93	G9
	RTS5_1		174	144	-	B9
Multi-Function Serial 6	SIN6_0	Multi-function serial interface ch 6 input pin	96	79	63	L10
	SIN6_1		117	97	81	K14
	SOT6_0 (SDA6_0)	Multi-function serial interface ch 6 output pin	97	80	64	K10
	SOT6_1 (SDA6_1)	This pin operates as SOT6 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA6 when it is used in an I²C (operation mode 4).	118	98	82	K11
	SCK6_0 (SCL6_0)	Multi-function serial interface ch 6 clock I/O pin	98	81	65	M10
	SCK6_1 (SCL6_1)	This pin operates as SCK6 when it is used in a CSIO (operation mode 2) and as SCL6 when it is used in an I²C (operation mode 4).	126	102	-	J10
	SCS60_0	Multi-function serial interface ch 6 chip select 0 input/output pin	99	82	66	N11
	SCS60_1		127	103	-	J9
	SCS61_0	Multi-function serial interface ch 6 chip select1 input/output pin	100	83	67	M11
	SCS61_1		128	104	-	H10
	SCS62_0	Multi-function serial interface ch 6 chip select2 input/output pin	79	64	-	K6
	SCS62_1		129	105	-	J14
	SCS63_0	Multi-function serial interface ch 6 chip select3 input/output pin	78	63	-	K5
	SCS63_1		119	-	-	-

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
Multi-Function Serial 7	SIN7_0	Multi-function serial interface ch 7 input pin	14	13	10	E5
	SIN7_1		103	-	-	-
	SOT7_0 (SDA7_0)	Multi-function serial interface ch 7 output pin	15	14	11	F1
	SOT7_1 (SDA7_1)	This pin operates as SOT7 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA7 when it is used in an I²C (operation mode 4).	102	-	-	-
	SCK7_0 (SCL7_0)	Multi-function serial interface ch 7 clock I/O pin	16	15	12	F2
	SCK7_1 (SCL7_1)	This pin operates as SCK7 when it is used in a CSIO (operation mode 2) and as SCL7 when it is used in an I²C (operation mode 4).	101	-	-	-
	SCS70_0	Multi-function serial interface ch 7 chip select 0 input/output pin	17	16	13	F3
	SCS70_1		94	-	-	-
	SCS71_0	Multi-function serial interface ch 7 chip select 1 input/output pin	18	17	14	F4
	SCS71_1		95	-	-	-
	SCS72_0	Multi-function serial interface ch 7 chip select 2 input/output pin	10	10	-	E2
	SCS72_1		68	-	-	-
	SCS73_0	Multi-function serial interface ch 7 chip select 3 input/output pin	11	11	-	E3
	SCS73_1		69	-	-	-
Multi-Function Serial 8	SIN8_0	Multi-function serial interface ch 8 input pin	91	76	60	K9
	SIN8_1		138	112	-	G13
	SOT8_0 (SDA8_0)	Multi-function serial interface ch 8 output pin	92	77	61	P10
	SOT8_1 (SDA8_1)	This pin operates as SOT8 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA8 when it is used in an I²C (operation mode 4).	139	113	-	F14
	SCK8_0 (SCL8_0)	Multi-function serial interface ch 8 clock I/O pin	93	78	62	N10
	SCK8_1 (SCL8_1)	This pin operates as SCK8 when it is used in a CSIO (operation mode 2) and as SCL8 when it is used in an I²C (operation mode 4).	140	114	-	G12
Multi-Function Serial 9	SIN9_0	Multi-function serial interface ch 9 input pin	82	67	57	L8
	SIN9_1		120	-	-	-
	SOT9_0 (SDA9_0)	Multi-function serial interface ch 9 output pin	83	68	58	K8
	SOT9_1 (SDA9_1)	This pin operates as SOT9 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA9 when it is used in an I²C (operation mode 4).	121	-	-	-
	SCK9_0 (SCL9_0)	Multi-function serial interface ch 9 clock I/O pin	84	69	59	J8
	SCK9_1 (SCL9_1)	This pin operates as SCK9 when it is used in a CSIO (operation mode 2) and as SCL9 when it is used in an I²C (operation mode 4).	122	-	-	-

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
Multi-Function Serial 10	SIN10_0	Multi-function serial interface ch 10 input pin	114	94	78	L11
	SIN10_1		51	41	-	L2
	SOT10_0 (SDA10_0)	Multi-function serial interface ch 10 output pin	115	95	79	K13
	SOT10_1 (SDA10_1)	This pin operates as SOT10 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA10 when it is used in an I²C (operation mode 4).	52	42	-	L3
	SCK10_0 (SCL10_0)	Multi-function serial interface ch 10 clock I/O pin	116	96	80	K12
	SCK10_1 (SCL10_1)	This pin operates as SCK10 when it is used in a CSIO (operation mode 2) and as SCL10 when it is used in an I²C (operation mode 4).	53	43	-	M2
Multi-Function Serial 11	SIN11_0	Multi-function serial interface ch 11 input pin	123	99	83	J13
	SIN11_1		26	-	-	-
	SOT11_0 (SDA11_0)	Multi-function serial interface ch 11 output pin	124	100	84	J12
	SOT11_1 (SDA11_1)	This pin operates as SOT11 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA11 when it is used in an I²C (operation mode 4).	27	-	-	-
	SCK11_0 (SCL11_0)	Multi-function serial interface ch 11 clock I/O pin	125	101	85	J11
	SCK11_1 (SCL11_1)	This pin operates as SCK11 when it is used in a CSIO (operation mode 2) and as SCL11 when it is used in an I²C (operation mode 4).	28	-	-	-
Multi-Function Serial 12	SIN12_0	Multi-function serial interface ch 12 input pin	133	109	89	G14
	SIN12_1		65	-	-	-
	SOT12_0 (SDA12_0)	Multi-function serial interface ch 12 output pin	134	110	90	H13
	SOT12_1 (SDA12_1)	This pin operates as SOT12 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA12 when it is used in an I²C (operation mode 4).	66	-	-	-
	SCK12_0 (SCL12_0)	Multi-function serial interface ch 12 clock I/O pin	135	111	91	H11
	SCK12_1 (SCL12_1)	This pin operates as SCK12 when it is used in a CSIO (operation mode 2) and as SCL12 when it is used in an I²C (operation mode 4).	67	-	-	-

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
Multi-Function Serial 13	SIN13_0	Multi-function serial interface ch 13 input pin	48	38	33	K3
	SIN13_1		206	-	-	-
	SOT13_0 (SDA13_0)	Multi-function serial interface ch 13 output pin	49	39	34	K4
	SOT13_1 (SDA13_1)	This pin operates as SOT13 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA13 when it is used in an I²C (operation mode 4).	205	-	-	-
	SCK13_0 (SCL13_0)	Multi-function serial interface ch 13 clock I/O pin	50	40	35	L1
	SCK13_1 (SCL13_1)	This pin operates as SCK13 when it is used in a CSIO (operation mode 2) and as SCL13 when it is used in an I²C (operation mode 4).	204	-	-	-
Multi-Function Serial 14	SIN14_0	Multi-function serial interface ch 14 input pin	30	21	18	G3
	SIN14_1		201	-	-	-
	SOT14_0 (SDA14_0)	Multi-function serial interface ch 14 output pin	31	22	19	G4
	SOT14_1 (SDA14_1)	This pin operates as SOT14 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA14 when it is used in an I²C (operation mode 4).	200	-	-	-
	SCK14_0 (SCL14_0)	Multi-function serial interface ch 14 clock I/O pin	32	23	20	G5
	SCK14_1 (SCL14_1)	This pin operates as SCK14 when it is used in a CSIO (operation mode 2) and as SCL14 when it is used in an I²C (operation mode 4).	199	-	-	-
Multi-Function Serial 15	SIN15_0	Multi-function serial interface ch 15 input pin	59	49	41	L4
	SIN15_1		19	-	-	-
	SOT15_0 (SDA15_0)	Multi-function serial interface ch 15 output pin	60	50	42	M4
	SOT15_1 (SDA15_1)	This pin operates as SOT15 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA15 when it is used in an I²C (operation mode 4).	20	-	-	-
	SCK15_0 (SCL15_0)	Multi-function serial interface ch 15 clock I/O pin	61	51	43	N4
	SCK15_1 (SCL15_1)	This pin operates as SCK15 when it is used in a CSIO (operation mode 2) and as SCL15 when it is used in an I²C (operation mode 4).	21	-	-	-

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
Multi-Function Timer 0	DTTI0X_0	Input signal controlling waveform generator outputs RTO00 to RTO05 of Multi-Function Timer 0.	44	34	29	J3
	DTTI0X_1		21	-	-	-
	FRCK0_0	16-bit free-run timer ch 0 external clock input pin	37	27	22	J1
	FRCK0_1		29	-	-	-
	IC00_0	16-bit input capture input pin of Multi-Function Timer 0. ICxx describes channel number.	43	33	28	J4
	IC00_1		22	-	-	-
	IC01_0		42	32	27	J5
	IC01_1		26	-	-	-
	IC02_0		41	31	26	H6
	IC02_1		27	-	-	-
	IC03_0		38	28	23	H3
	IC03_1		28	-	-	-
	RTO00_0 (PPG00_0)	Waveform generator output pin of Multi-Function Timer 0. This pin operates as PPG00 when it is used in PPG0 output modes.	45	35	30	J2
	RTO00_1 (PPG00_1)		10	10	-	E2
	RTO01_0 (PPG00_0)	Waveform generator output pin of Multi-Function Timer 0. This pin operates as PPG00 when it is used in PPG0 output modes.	46	36	31	K1
	RTO01_1 (PPG00_1)		11	11	-	E3
	RTO02_0 (PPG02_0)	Waveform generator output pin of Multi-Function Timer 0. This pin operates as PPG02 when it is used in PPG0 output modes.	47	37	32	K2
	RTO02_1 (PPG02_1)		12	12	-	E4
	RTO03_0 (PPG02_0)	Waveform generator output pin of Multi-Function Timer 0. This pin operates as PPG02 when it is used in PPG0 output modes.	48	38	33	K3
	RTO03_1 (PPG02_1)		13	-	-	-
	RTO04_0 (PPG04_0)	Waveform generator output pin of Multi-Function Timer 0. This pin operates as PPG04 when it is used in PPG0 output modes.	49	39	34	K4
	RTO04_1 (PPG04_1)		19	-	-	-
	RTO05_0 (PPG04_0)	Waveform generator output pin of Multi-Function Timer 0. This pin operates as PPG04 when it is used in PPG0 output modes.	50	40	35	L1
	RTO05_1 (PPG04_1)		20	-	-	-

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
Multi-Function Timer 1	DTTI1X_0	Input signal controlling waveform generator outputs RTO10 to RTO15 of Multi-Function Timer 1.	70	55	47	L5
	DTTI1X_1		94	-	-	-
	FRCK1_0	16-bit free-run timer ch 1 external clock input pin	71	56	48	M5
	FRCK1_1		78	63	-	K5
	IC10_0	16-bit input capture input pin of Multi-Function Timer 1. ICxx describes channel number.	96	79	63	L10
	IC10_1		95	-	-	-
	IC11_0		97	80	64	K10
	IC11_1		101	-	-	-
	IC12_0		98	81	65	M10
	IC12_1		102	-	-	-
	IC13_0		99	82	66	N11
	IC13_1		103	-	-	-
	RTO10_0 (PPG10_0)	Waveform generator output pin of Multi-Function Timer 1. This pin operates as PPG10 when it is used in PPG1 output modes.	56	46	38	N2
	RTO10_1 (PPG10_1)		85	70	-	N8
	RTO11_0 (PPG10_0)	Waveform generator output pin of Multi-Function Timer 1. This pin operates as PPG10 when it is used in PPG1 output modes.	57	47	39	N3
	RTO11_1 (PPG10_1)		86	71	-	M8
	RTO12_0 (PPG12_0)	Waveform generator output pin of Multi-Function Timer 1. This pin operates as PPG12 when it is used in PPG1 output modes.	58	48	40	M3
	RTO12_1 (PPG12_1)		87	72	-	N9
	RTO13_0 (PPG12_0)	Waveform generator output pin of Multi-Function Timer 1. This pin operates as PPG12 when it is used in PPG1 output modes.	59	49	41	L4
	RTO13_1 (PPG12_1)		88	73	-	P9
	RTO14_0 (PPG14_0)	Waveform generator output pin of Multi-Function Timer 1. This pin operates as PPG14 when it is used in PPG1 output modes.	60	50	42	M4
	RTO14_1 (PPG14_1)		89	74	-	M9
	RTO15_0 (PPG14_0)	Waveform generator output pin of Multi-Function Timer 1. This pin operates as PPG14 when it is used in PPG1 output modes.	61	51	43	N4
	RTO15_1 (PPG14_1)		90	75	-	L9

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
Multi-Function Timer 2	DTTI2X_0	Input signal controlling waveform generator outputs RTO20 to RTO25 of Multi-Function Timer 1.	8	8	8	D3
	DTTI2X_1		202	-	-	-
	FRCK2_0	16-bit free-run timer ch 2 external clock input pin	17	16	13	F3
	FRCK2_1		197	165	135	C6
	IC20_0	16-bit input capture input pin of Multi-Function Timer 2. ICxx describes channel number.	9	9	9	D4
	IC20_1		201	-	-	-
	IC21_0		14	13	10	E5
	IC21_1		200	-	-	-
	IC22_0		15	14	11	F1
	IC22_1		199	-	-	-
	IC23_0		16	15	12	F2
	IC23_1		198	166	136	D6
	RTO20_0 (PPG20_0)	Waveform generator output pin of Multi-Function Timer 2. This pin operates as PPG20 when it is used in PPG2 output modes.	2	2	2	B2
	RTO20_1 (PPG20_1)		203	-	-	-
	RTO21_0 (PPG20_0)	Waveform generator output pin of Multi-Function Timer 2. This pin operates as PPG20 when it is used in PPG2 output modes.	3	3	3	C2
	RTO21_1 (PPG20_1)		204	-	-	-
	RTO22_0 (PPG22_0)	Waveform generator output pin of Multi-Function Timer 2. This pin operates as PPG22 when it is used in PPG2 output modes.	4	4	4	C3
	RTO22_1 (PPG22_1)		205	-	-	-
	RTO23_0 (PPG22_0)	Waveform generator output pin of Multi-Function Timer 2. This pin operates as PPG22 when it is used in PPG2 output modes.	5	5	5	D5
	RTO23_1 (PPG22_1)		206	-	-	-
	RTO24_0 (PPG24_0)	Waveform generator output pin of Multi-Function Timer 2. This pin operates as PPG24 when it is used in PPG2 output modes.	6	6	6	D2
	RTO24_1 (PPG24_1)		207	167	-	E6
	RTO25_0 (PPG24_0)	Waveform generator output pin of Multi-Function Timer 2. This pin operates as PPG24 when it is used in PPG2 output modes.	7	7	7	D1
	RTO25_1 (PPG24_1)		208	168	-	B5

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
Quadrature Position/ Revolution Counter 0	AIN0_0	QPRC ch 0 AIN input pin	56	46	38	N2
	AIN0_1		65	-	-	-
	AIN0_2		114	94	78	L11
	BIN0_0	QPRC ch 0 BIN input pin	57	47	39	N3
	BIN0_1		66	-	-	-
	BIN0_2		115	95	79	K13
	ZIN0_0	QPRC ch 0 ZIN input pin	58	48	40	M3
	ZIN0_1		67	-	-	-
	ZIN0_2		116	96	80	K12
Quadrature Position/ Revolution Counter 1	AIN1_0	QPRC ch 1 AIN input pin	91	76	60	K9
	AIN1_1		94	-	-	-
	AIN1_2		123	99	83	J13
	BIN1_0	QPRC ch 1 BIN input pin	92	77	61	P10
	BIN1_1		45	-	-	-
	BIN1_2		124	100	84	J12
	ZIN1_0	QPRC ch 1 ZIN input pin	93	78	62	N10
	ZIN1_1		101	-	-	-
	ZIN1_2		125	101	85	J11
Quadrature Position/ Revolution Counter 2	AIN2_0	QPRC ch 2 AIN input pin	2	2	2	B2
	AIN2_1		32	23	20	G5
	AIN2_2		120	-	-	-
	BIN2_0	QPRC ch 2 BIN input pin	3	3	3	C2
	BIN2_1		36	26	21	H2
	BIN2_2		121	-	-	-
	ZIN2_0	QPRC ch 2 ZIN input pin	4	4	4	C3
	ZIN2_1		37	27	22	J1
	ZIN2_2		122	-	-	-
Quadrature Position/ Revolution Counter 3	AIN3_0	QPRC ch 3 AIN input pin	18	17	14	F4
	AIN3_1		45	35	30	J2
	AIN3_2		149	-	-	-
	BIN3_0	QPRC ch 3 BIN input pin	23	18	15	F5
	BIN3_1		46	36	31	K1
	BIN3_2		150	-	-	-
	ZIN3_0	QPRC ch 3 ZIN input pin	24	19	16	F6
	ZIN3_1		47	37	32	K2
	ZIN3_2		151	-	-	-

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
Real-time clock	RTCCO_0	0.5 seconds pulse output pin of real-time clock	211	171	139	C4
	RTCCO_1		33	-	-	-
	SUBOUT_0	Sub-clock output pin	211	171	139	C4
	SUBOUT_1		33	-	-	-
USB0	UDM0	USB ch 0 device/host D – pin	214	174	142	A3
	UDP0	USB ch 0 device/host D + pin	215	175	143	A2
	UHCONX0	USB ch 0 external pull-up control pin	211	171	139	C4
USB1	UDM1	USB ch 1 device/host D – pin	160	130	106	D14
	UDP1	USB ch 1 device/host D + pin	161	131	107	C14
	UHCONX1	USB ch 1 external pull-up control pin	155	125	101	E13
Low power Consumption mode	WKUP0	Deep Standby mode return signal input pin 0	158	128	104	C13
	WKUP1	Deep Standby mode return signal input pin 1	14	13	10	E5
	WKUP2	Deep Standby mode return signal input pin 2	70	55	47	L5
	WKUP3	Deep Standby mode return signal input pin 3	212	172	140	B3
D/A converter	DA0	D/A converter ch 0 analog output pin	100	83	67	M11
	DA1	D/A converter ch 1 analog output pin	99	82	66	N11
VBAT	VREGCTL	On-board regulator control pin	76	61	53	N6
	VWAKEUP	The return signal input pin from a hibernation state	77	62	54	M6
SD I/F	S_CLK_0	SD memory card interface SD memory card clock output pin	38	28	23	H3
	S_CMD_0	SD memory card interface SD memory card command output	41	31	26	H6
	S_DATA1_0	SD memory card interface SD memory card data bus	36	26	21	H2
	S_DATA0_0		37	27	22	J1
	S_DATA3_0		42	32	27	J5
	S_DATA2_0		43	33	28	J4
	S_CD_0	SD memory card interface SD memory card detection pin	45	35	30	J2
	S_WP_0	SD memory card interface SD memory card write protection	44	34	29	J3

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
Ethernet	E_COL	Collision detection	186	154	124	F8
	E_COUT	Clock output for Ethernet PHY	190	158	128	A7
	E_CRS	Carrier detection	187	155	125	B7
	E_MDC	Management clock	184	152	122	E8
	E_MDIO	Management data I/O	183	151	121	D8
	E_PPS	PTP counter monitor	198	166	136	D6
	E_RX00	Received data0	181	149	119	F9
	E_RX01	Received data1	180	148	118	E9
	E_RX02	Received data2	179	147	117	D9
	E_RX03	Received data3	178	146	116	B8
	E_RXCK_REFCK	Received clock input/ Reference clock	185	153	123	A10
	E_RXDV	Received data enable	182	150	120	C8
	E_RXER	Received data error detection	177	145	115	C9
	E_TCK	Transition clock input	191	159	129	C7
	E_TX00	Transition data0	196	164	134	B6
	E_TX01	Transition data1	195	163	133	F7
	E_TX02	Transition data2	194	162	132	E7
	E_TX03	Transition data3	193	161	131	D7
	E_TXEN	Transition data enable	197	165	135	C6
	E_TXER	Transition data error detection	192	160	130	A6
I^2S	I2SMCLK0_0	I^2S external clock pin	51	41	-	L2
	I2SDO0_0	I^2S serial transition data output pin	52	42	-	L3
	I2SWS0_0	I^2S frame synchronization signal pin	53	43	-	M2
	I2SDI0_0	I^2S serial received data input pin	34	24	-	G6
	I2SCK0_0	I^2S bit clock pin	35	25	-	H4
High-speed quad SPI	Q_SCK_0	SPI clock output pin	173	143	-	D10
	Q_IO0_0	SPI data input/output pin	172	142	-	C10
	Q_IO1_0		171	141	-	B10
	Q_IO2_0		170	140	-	D11
	Q_IO3_0		169	139	-	C11
	Q_CS0_0	SPI chip select output pin	174	144	-	B9
	Q_CS1_0		175	-	-	-
	Q_CS2_0		176	-	-	-

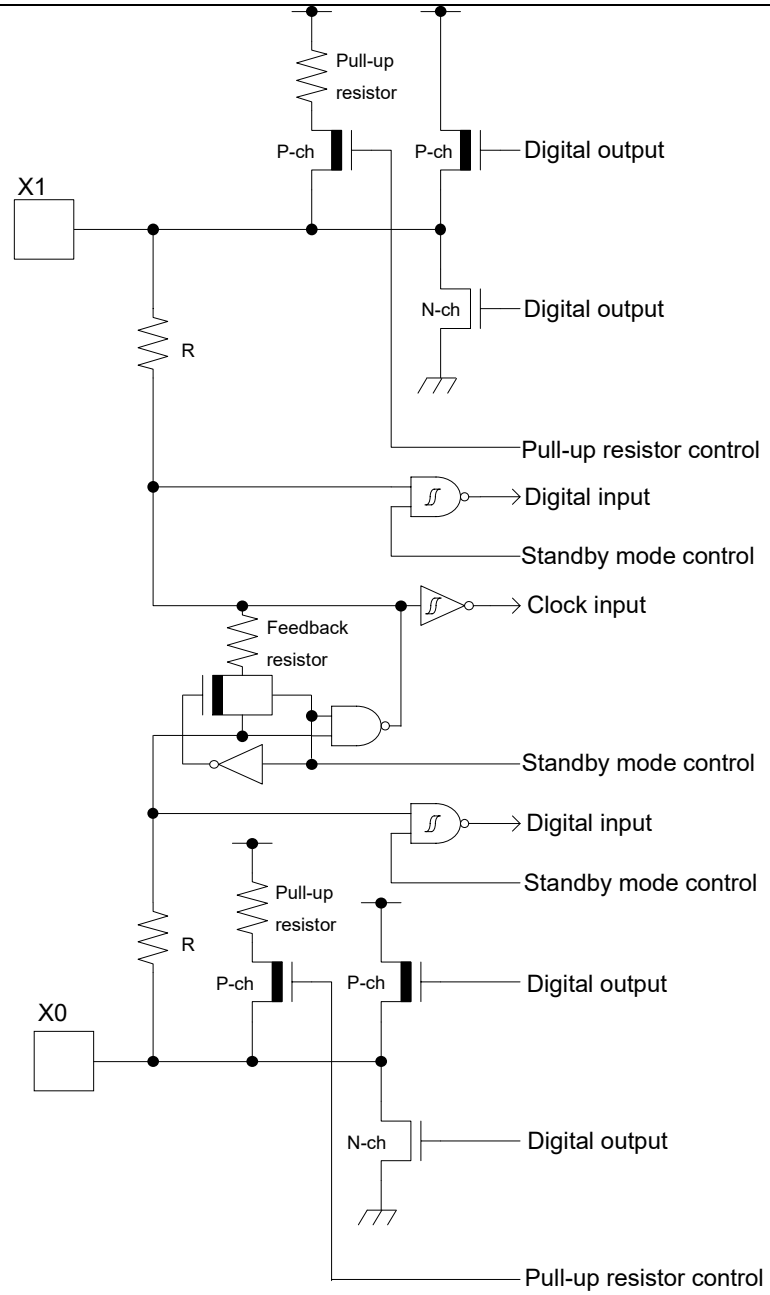
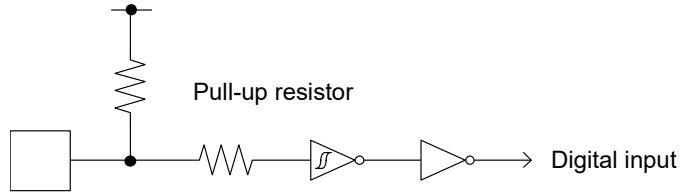
Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
Reset	INITX	External reset Input pin A reset is valid when INITX = L.	72	57	49	N5
Mode	MD1	Mode 1 pin During serial programming to flash memory, MD1 = L must be input.	104	84	68	N13
	MD0	Mode 0 pin During normal operation, MD0 = L must be input. During serial programming to flash memory, MD0 = H must be input.	105	85	69	N12
Power	VCC	Power supply pin	1	1	1	C1
			39	29	24	H1
			55	45	37	N1
			64	54	46	P4
			109	89	73	M14
			137	-	-	-
			163	133	109	A13
	USBVCC0	3.3V power supply port for USB I/O	213	173	141	A4
	USBVCC1		159	129	105	E14
	ETHVCC	Power supply pin for Ethernet I/O	188	156	126	A9
GND	VSS	GND pin	40	30	25	H5
			54	44	36	M1
			63	53	45	P3
			108	88	72	N14
			136	-	-	-
			162	132	108	B14
			189	157	127	A8
			216	176	144	B1
			-	-	-	E1
			-	-	-	G1
			-	-	-	P7
			-	-	-	P11
			-	-	-	L14
			-	-	-	A11
			-	-	-	A5
			-	-	-	N7
			-	-	-	M7
			-	-	-	K7
			-	-	-	J7
			-	-	-	G7
			-	-	-	H7
			-	-	-	H8
			-	-	-	G8

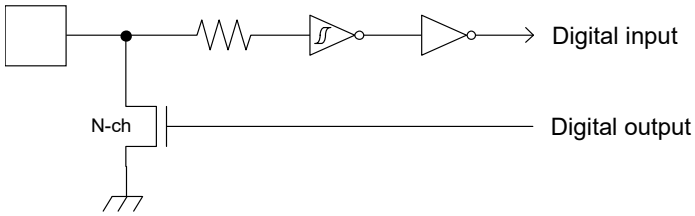
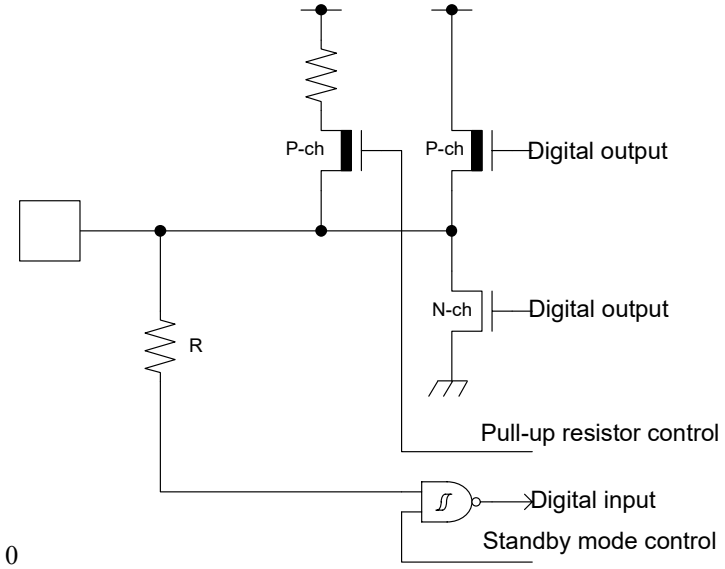
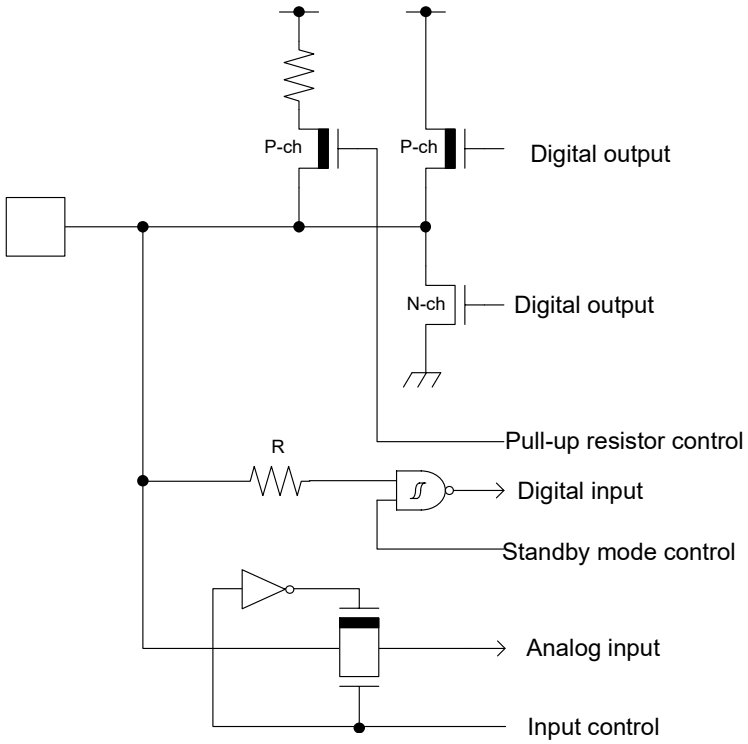
Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
Clock	X0	Main clock (oscillation) input pin	106	86	70	P12
	X1	Main clock (oscillation) I/O pin	107	87	71	P13
	X0A	Sub clock (oscillation) input pin	73	58	50	P5
	X1A	Sub clock (oscillation) I/O pin	74	59	51	P6
	CROUT_0	Built-in High-speed CR-oscillation clock output port	157	127	103	D13
	CROUT_1		184	152	122	E8
Analog power	AVCC	A/D converter and D/A converter analog power-supply pin	110	90	74	M13
	AVRL	A/D converter analog reference voltage input pin	112	92	76	L13
	AVRH	A/D converter analog reference voltage input pin	113	93	77	L12
VBAT power	VBAT	VBAT power supply pin Backup power supply (battery etc.) and system power supply	75	60	52	P8
Analog GND	AVSS	A/D converter and D/A converter GND pin	111	91	75	M12
C pin	C	Power supply stabilization capacity pin	62	52	44	P2

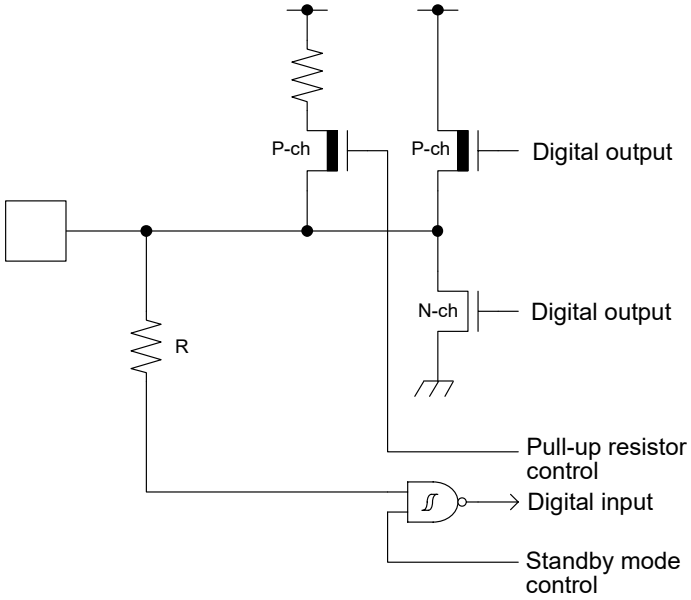
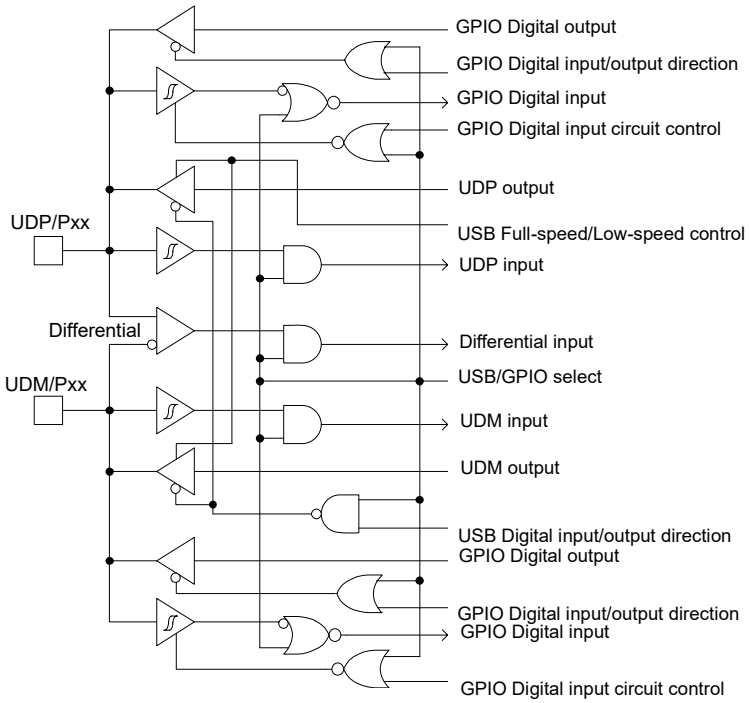
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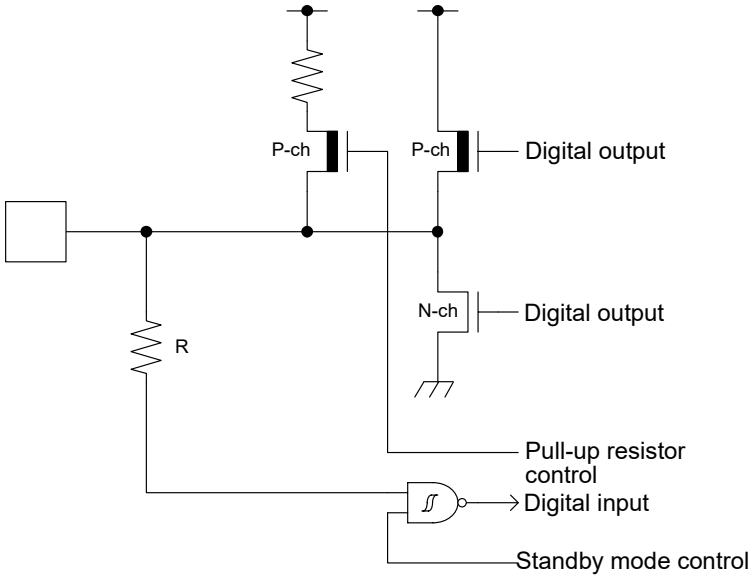
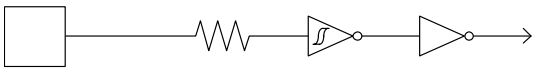
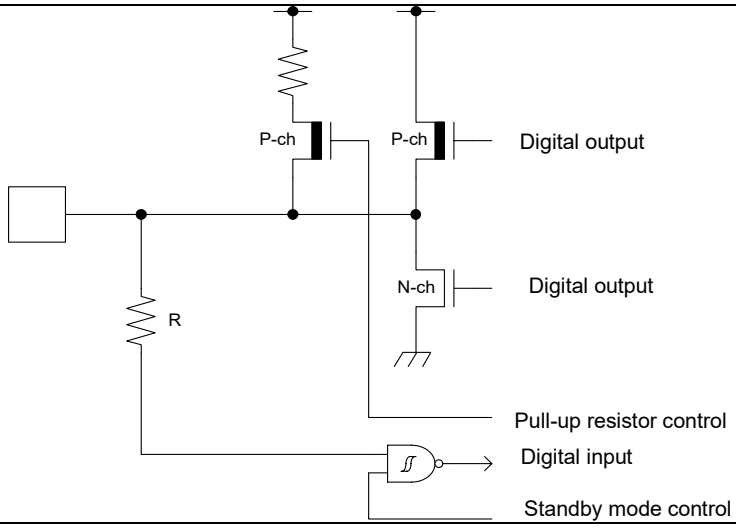
- *While this device contains a Test Access Port (TAP) based on the IEEE 1149.1-2001 JTAG standard, it is not fully compliant to all requirements of that standard. This device may contain a 32-bit device ID that is the same as the 32-bit device ID in other devices with different functionality. The TAP pins may also be configurable for purposes other than access to the TAP controller.*

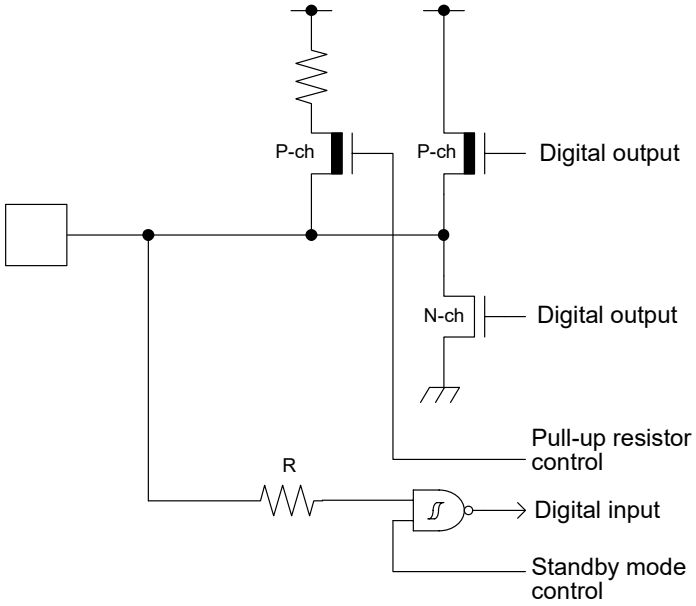
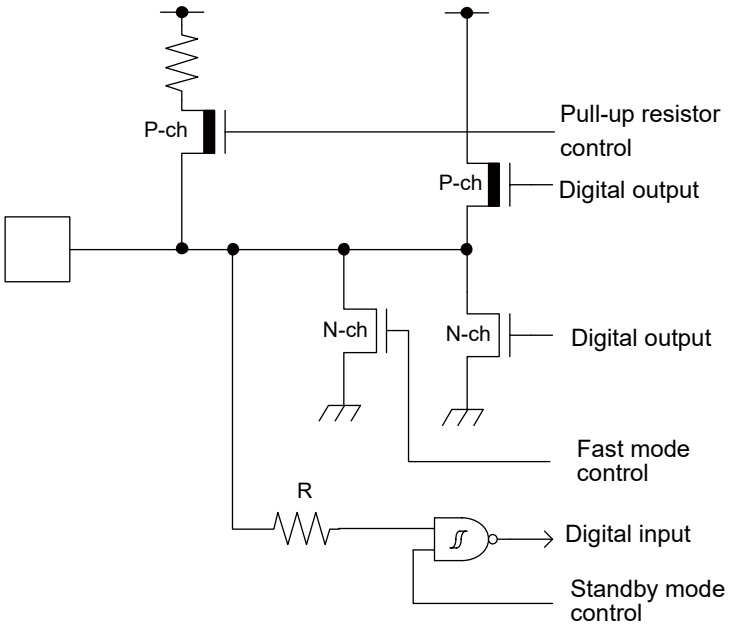
6. I/O Circuit Type

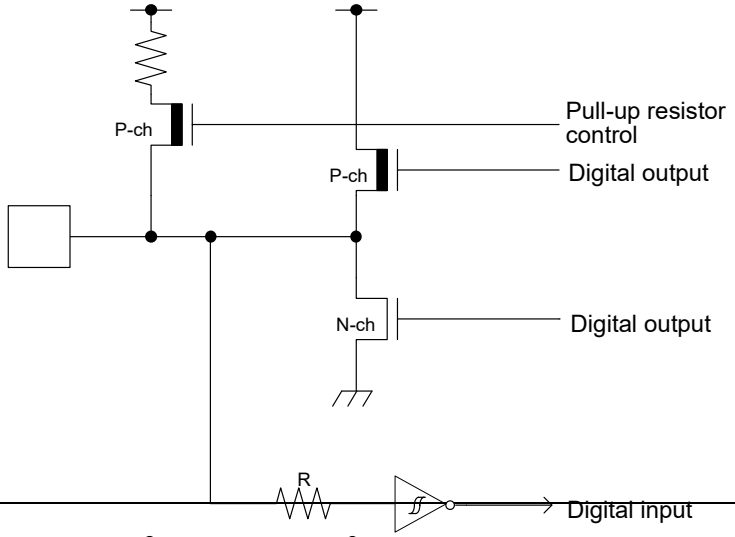
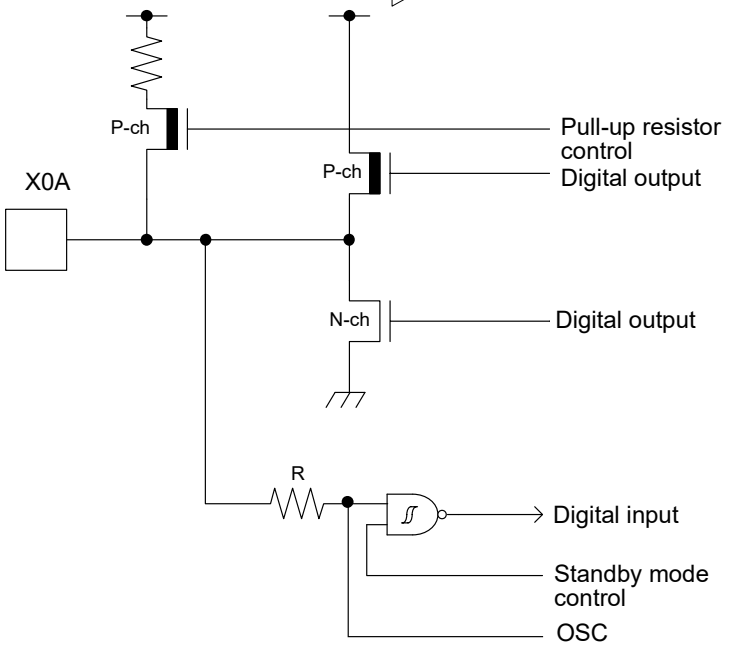
Type	Circuit	Remarks
A		It is possible to select the main oscillation/GPIO function. When the main oscillation is selected: ・ Oscillation feedback resistor: approximately 1 MΩ ・ Standby mode control When the GPIO is selected: ・ CMOS level output. ・ CMOS level hysteresis input ・ Pull-up resistor control ・ Standby mode control ・ Pull-up resistor: approximately 50 kΩ ・ I_{OH} = -4 mA, I_{OL} = 4 mA
B		・ CMOS level hysteresis input ・ Pull-up resistor: approximately 50 kΩ

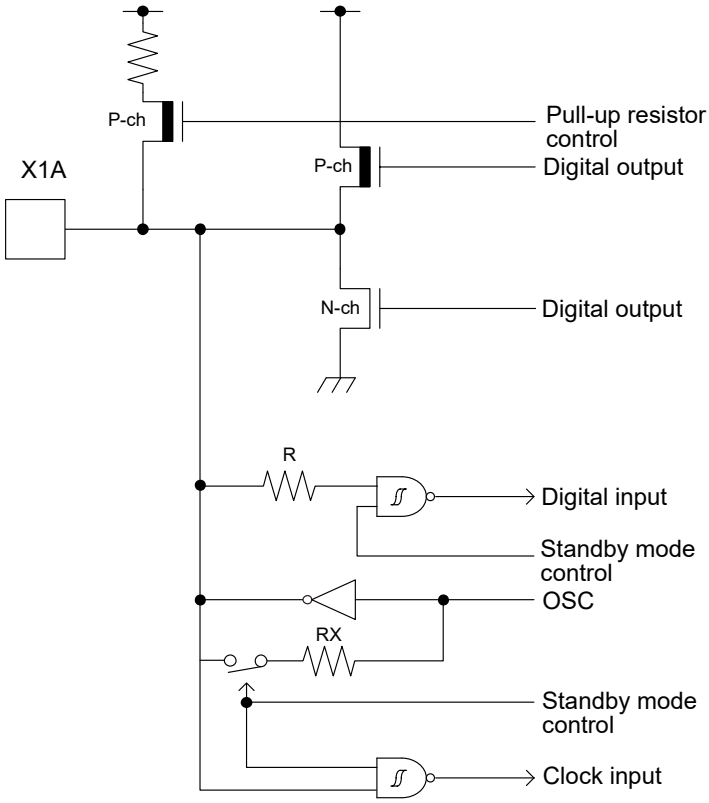
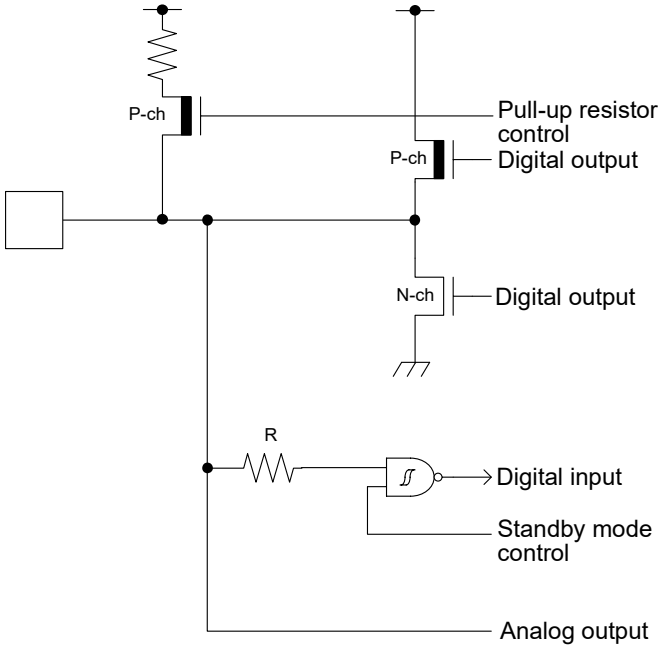
Type	Circuit	Remarks
C		• Open drain output • CMOS level hysteresis input
E		• CMOS level output • CMOS level hysteresis input • Pull-up resistor control • Standby mode control • Pull-up resistor: approximately 50 kΩ • I_{OH} = -4 mA, I_{OL} = 4 mA • When this pin is used as an I^2C pin, the digital output P-ch transistor is always off.
F		• CMOS level output • CMOS level hysteresis input • Input control • Analog input • Pull-up resistor control • Standby mode control • Pull-up resistor: approximately 50 kΩ • I_{OH} = -4 mA, I_{OL} = 4 mA • When this pin is used as an I^2C pin, the digital output P-ch transistor is always off.

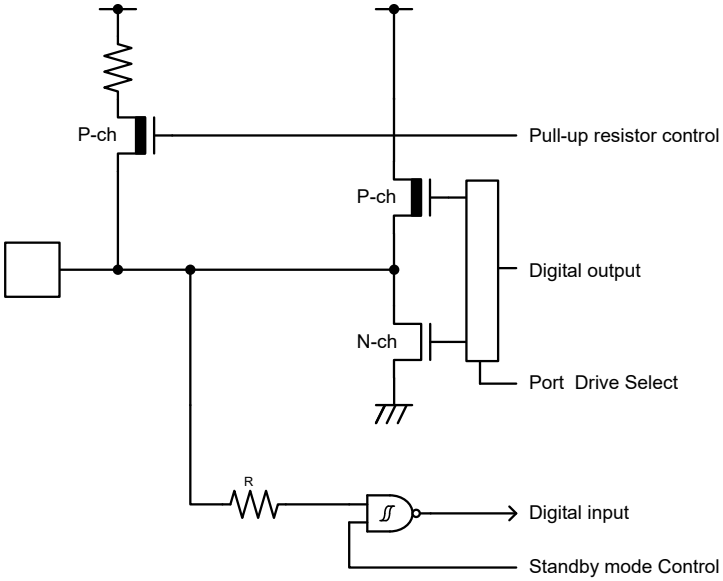
Type	Circuit	Remarks
G		・ CMOS level output ・ CMOS level hysteresis input ・ Pull-up resistor control ・ Standby mode control ・ Pull-up resistor: approximately 50 kΩ ・ I_{OH} = -12 mA, I_{OL} = 12 mA ・ When this pin is used as an I^2C pin, the digital output P-ch transistor is always off.
H		It is possible to select either USB I/O or GPIO function. When the USB I/O is selected: ・ Full-speed, low-speed control When the GPIO is selected: ・ CMOS level output ・ CMOS level hysteresis input ・ Standby mode control ・ I_{OH} = -20.5 mA, I_{OL} = 18.5 mA

Type	Circuit	Remarks
I		・CMOS level output ・CMOS level hysteresis input ・5 V tolerant ・Pull-up resistor control ・Standby mode control ・Pull-up resistor: approximately 50 kΩ ・I_{OH} = -4 mA, I_{OL} = 4 mA ・Available to control of PZR registers (pseudo-open drain control) ・For PZR registers, refer to GPIO in the FM4 Family Peripheral Manual Main Part (002-04856).
J		CMOS level hysteresis input
K		・CMOS level output ・TTL level hysteresis input ・Pull-up resistor control ・Standby mode control ・Pull-up resistor: approximately 50 kΩ ・I_{OH} = -4 mA, I_{OL} = 4 mA

Type	Circuit	Remarks
L		• CMOS level output • CMOS level hysteresis input • Pull-up resistor control • Standby mode control • Pull-up resistor: approximately 50 kΩ • I_{OH} = -8 mA, I_{OL} = 8 mA • When this pin is used as an I^2C pin, the digital output P-ch transistor is always off.
N		• CMOS level output • CMOS level hysteresis input • 5V tolerant • Pull-up resistor control • Standby mode control • Pull-up resistor: approximately 50 kΩ • I_{OH} = -4 mA, I_{OL} = 4 mA (GPIO) • I_{OL} = 20mA (Fast mode Plus) • Available to control of PZR register (pseudo-open drain control) • For PZR registers, refer to GPIO in the FM4 Family Peripheral Manual Main Part (002-04857). • When this pin is used as an I^2C pin, the digital output P-ch transistor is always off.

Type	Circuit	Remarks
O		• CMOS level output • CMOS level hysteresis input • 5 V tolerant • Pull-up resistor control • Pull-up resistor: approximately 50 kΩ • I_{OH} = -4 mA, I_{OL} = 4 mA • Available to control of PZR register (pseudo-open drain control) • For PZR registers, refer to GPIO in the “FM4 Family Peripheral Manual Main Part (MN709-00001)”. • For I/O setting, refer to VBAT Domain in the FM4 Family Peripheral Manual Main Part (002-04856).
P		• CMOS level output • CMOS level hysteresis input • Pull-up resistor control • Pull-up resistor: approximately 50 kΩ • I_{OH} = -4 mA, I_{OL} = 4 mA • For I/O setting, refer to VBAT Domain in the FM4 Family Peripheral Manual Main Part (002-04856).

Type	Circuit	Remarks
Q		It is possible to select the sub oscillation/GPIO function. When the sub oscillation is selected: ・ Oscillation feedback resistor: approximately 10 MΩ When the GPIO is selected: ・ CMOS level output. ・ CMOS level hysteresis input ・ Pull-up resistor control ・ Pull-up resistor: approximately 50 kΩ ・ I_{OH} = -4 mA, I_{OL} = 4 mA ・ For I/O setting, refer to VBAT Domain in the FM4 Family Peripheral Manual Main Part (002-04856).
R		・ CMOS level output ・ CMOS level hysteresis input ・ Analog output ・ Pull-up resistor control ・ Standby mode control ・ Pull-up resistor: approximately 50 kΩ ・ I_{OH} = -4 mA, I_{OL} = 4 mA (4.5 V to 5.5V) ・ I_{OH} = -2 mA, I_{OL} = 2 mA (2.7 V to 4.5 V)

Type	Circuit	Remarks
S		・CMOS level output ・(It is possible to select by port drive capability. Select register [PDSR]) ・CMOS level hysteresis input ・Pull-up resistor control ・Standby mode control ・Pull-up resistor: approximately 50 kΩ ・I_{OH} = -10 mA, I_{OL} = 10 mA (PDSR = 1) ・I_{OH} = -4 mA, I_{OL} = 4 mA (PDSR = 0) ・When this pin is used as an I^2C pin, the digital output P-ch transistor is always off.

7. Handling Precautions

Every semiconductor device has a characteristic, inherent rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your Cypress semiconductor devices.

7.1 Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

Recommended Operating Conditions

Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the datasheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

Processing and Protection of Pins

These precautions must be followed when handling the pins that connect semiconductor devices to power supply and I/O functions.

1. Preventing Over-Voltage and Over-Current Conditions

   Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.

2. Protection of Output Pins

   Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions, if present for extended periods of time, can damage the device; therefore, avoid this type of connection.

3. Handling of Unused Input Pins

   Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power-supply pin or ground pin.

Latch-Up

Semiconductor devices are constructed by the formation of p-type and n-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic pnpn junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred milliamps to flow continuously at the power supply pin. This condition is called latch-up.

CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

1. Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.
2. Be sure that abnormal current flows do not occur during the power-on sequence.

Observance of Safety Regulations and Standards

Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

Fail-Safe Design

As previously mentioned, all semiconductor devices have inherent rates of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

Precautions Related to Usage of Devices

Cypress semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

7.2 Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Cypress's recommended conditions. For detailed information about mount conditions, contact your sales representative.

Lead Insertion Type

Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Cypress recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason, it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

Surface Mount Type

Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. Cypress recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Cypress ranking of recommended conditions.

Lead-Free Packaging

CAUTION: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

Storage of Semiconductor Devices

Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent this, do the following:

1. Avoid exposure to rapid temperature changes, which can cause moisture to condense inside the product. Store products in locations where temperature changes are slight.
2. Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5°C and 30°C.
3. When Dry Packages are opened, it is recommended to have humidity between 40% and 70%.
4. When necessary, Cypress packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in these aluminum laminate bags for storage.
5. Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

Baking

Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Cypress recommended conditions for baking.

Condition: 125°C/24 h

Static Electricity

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

1. Maintain relative humidity in the working environment between 40% and 70%. Use of an apparatus for ion generation may be needed to remove electricity.
2. Electrically ground all conveyors, solder vessels, soldering irons, and peripheral equipment.
3. Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ). Wearing of conductive clothing and shoes, and the use of conductive floor mats and other measures to minimize shock loads is recommended.
4. Ground all fixtures and instruments, or protect with anti-static measures.
5. Avoid the use of Styrofoam or other highly static-prone materials for storage of completed board assemblies.

7.3 Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

1. Humidity

   Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.

2. Discharge of static electricity

   When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.

3. Corrosive gases, dust, or oil

   Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.

4. Radiation, including cosmic radiation

   Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.

5. Smoke, flame

   CAUTION: Plastic molded devices are flammable and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of Cypress products in other special environmental conditions should consult with sales representatives.

8. Handling Devices

Power-Supply Pins

In products with multiple VCC and VSS pins, respective pins at the same potential are interconnected within the device in order to prevent malfunctions such as latch-up. All of these pins should be connected externally to the power supply or ground lines, however, in order to reduce electromagnetic emission levels, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating.

Be sure to connect the current-supply source with the power pins and GND pins of this device at low impedance. It is also advisable that a ceramic capacitor of approximately 0.1 µF be connected as a bypass capacitor between VCC and VSS near this device.

A malfunction may occur when the power-supply voltage fluctuates rapidly even though the fluctuation is within the guaranteed operating range of the VCC power supply voltage. As a rule of voltage stabilization, suppress voltage fluctuation so that the fluctuation in VCC ripple (peak-to-peak value) at the commercial frequency (50 Hz/60 Hz) does not exceed 10% of the standard VCC value, and the transient fluctuation rate does not exceed 0.1V/µs at a momentary fluctuation such as switching the power supply.

Crystal Oscillator Circuit

Noise near the X0/X1 and X0A/X1A pins may cause the device to malfunction. Design the printed circuit board so that X0/X1, X0A/X1A pins, the crystal oscillator (or ceramic oscillator), and the bypass capacitor to ground are located as close to the device as possible.

It is strongly recommended that the PC board artwork be designed such that the X0/X1 and X0A/X1A pins are surrounded by ground plane, as this is expected to produce stable operation.

Evaluate the oscillation introduced by the use of the crystal oscillator by your mount board.

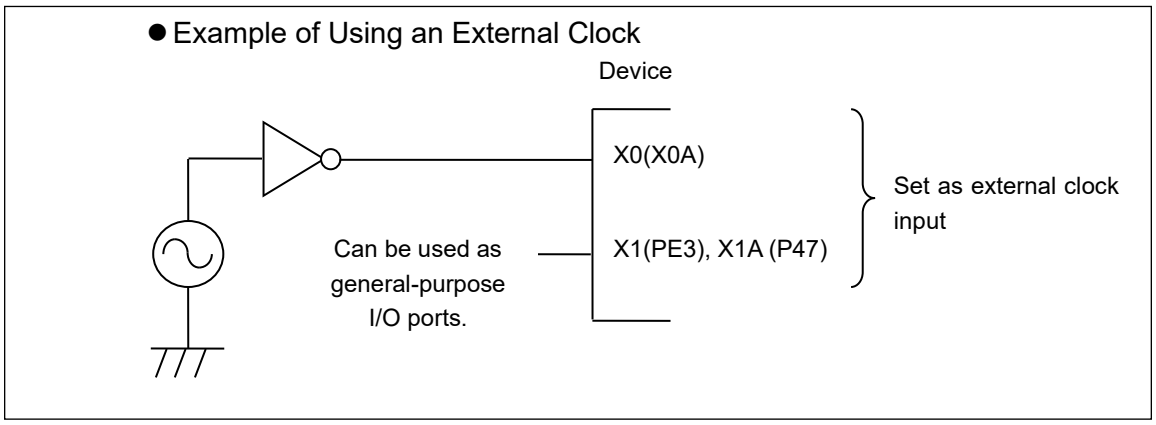
Sub Crystal Oscillator

The sub-oscillator circuit for devices in this family is low gain to keep current consumption low. To stabilize the oscillation, Cypress recommends a crystal oscillator that meets the following conditions:

- Surface mount type
  Size: More than 3.2 mm × 1.5 mm
  Load capacitance: approximately 6 pF to 7 pF
- Lead type
  Load capacitance: approximately 6 pF to 7 pF

Using an External Clock

When using an external clock as an input of the main clock, set X0/X1 to the external clock input, and input the clock to X0. X1(PE3) can be used as a general-purpose I/O port. Similarly, when using an external clock as an input of the sub clock, set X0A/X1A to the external clock input and input the clock to X0A. X1A (P47) can be used as a general-purpose I/O port.

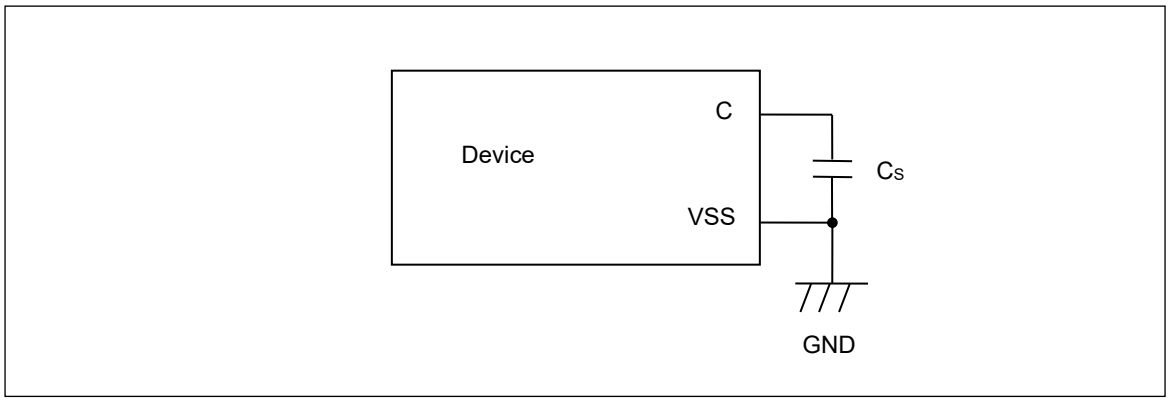


Handling When Using Multi-Function Serial Pin As I²C Pin

If the application uses the multi-function serial pin as an I²C pin, the P-channel transistor of the digital output must be disabled. I²C pins need to conform to electrical limitations like other pins, however, and avoid connecting to live external systems with the MCU power off.

C Pin

Devices in this series contain a regulator. Be sure to connect a smoothing capacitor (C_S) for the regulator between the C pin and the GND pin. Please use a ceramic capacitor or a capacitor of equivalent frequency characteristics as a smoothing capacitor. Some laminated ceramic capacitors have a large capacitance variation due to thermal fluctuation. Please select a capacitor that meets the specifications in the operating conditions to use by evaluating the temperature characteristics of the device. A smoothing capacitor of about 4.7 µF would be recommended for this series.



Mode Pins (MD0)

Connect the MD pin (MD0) directly to VCC or VSS pins. Design the printed circuit board such that the pull-up/down resistance stays low, the distance between the mode pins and VCC pins or VSS pins is as short as possible, and the connection impedance is low when the pins are pulled up/down such as for switching the pin level and rewriting the flash memory data. This is important to prevent the device from erroneously switching to test mode as a result of noise.

Notes on Power-On

Turn power on/off in the following order or at the same time. The device operates normally after all power on.

VBAT only Power-on is possible when VBAT and VCC turn Power-on and Hibernation control is setting and then VCC turns Power-off. About Hibernation control, see Chapter 7-2: VBAT Domain(B) in FM4 Family Peripheral Manual Main Part (002-04856).

Turning on:	VBAT → VCC → USBVCC0
	VBAT → VCC → USBVCC1
	VBAT →VCC →ETHVCC
	VCC → AVCC → AVRH
Turning off:	AVRH → AVCC → VCC
	ETHVCC → VCC → VBAT
	USBVCC1 → VCC → VBAT
	USBVCC0 → VCC → VBAT

Serial Communication

There is a possibility of receiving incorrect data as a result of noise or other issues introduced by the serial communication. Take care to design the printed circuit board to minimize noise.

Consider the case of introducing error as a result of noise, perform error detection such as by applying a checksum of data at the end. If an error is detected, retransmit the data.

Differences in Characteristics within the Product Line

The electric characteristics including power consumption, ESD, latch-up, noise, and oscillation differ among members of the product line because chip layout and memory structures are not the same; for example, different sizes, flash versus ROM, etc. If you are switching to a different product of the same series, please make sure to evaluate the electric characteristics.

Pull-Up Function of 5 V Tolerant I/O

Please do not input the signal more than VCC voltage at the time of Pull-Up function use of 5 V tolerant I/O.

Pin Doubled as Debug Function

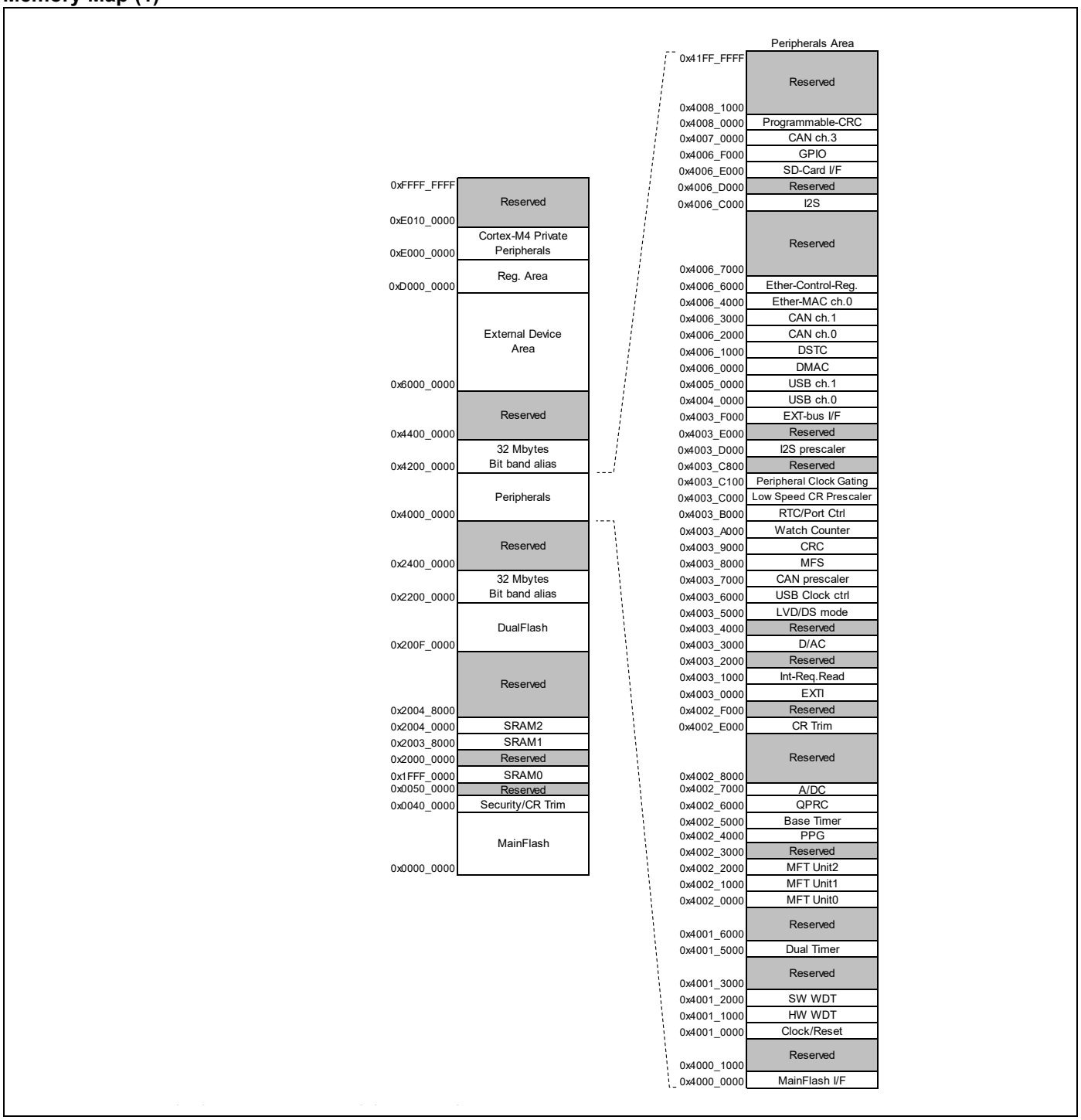
The pin doubled as TDO/TMS/TDI/TCK/TRSTX, SWO/SWDIO/SWCLK should be used as output only. Do not use as input.

9. Memory Size

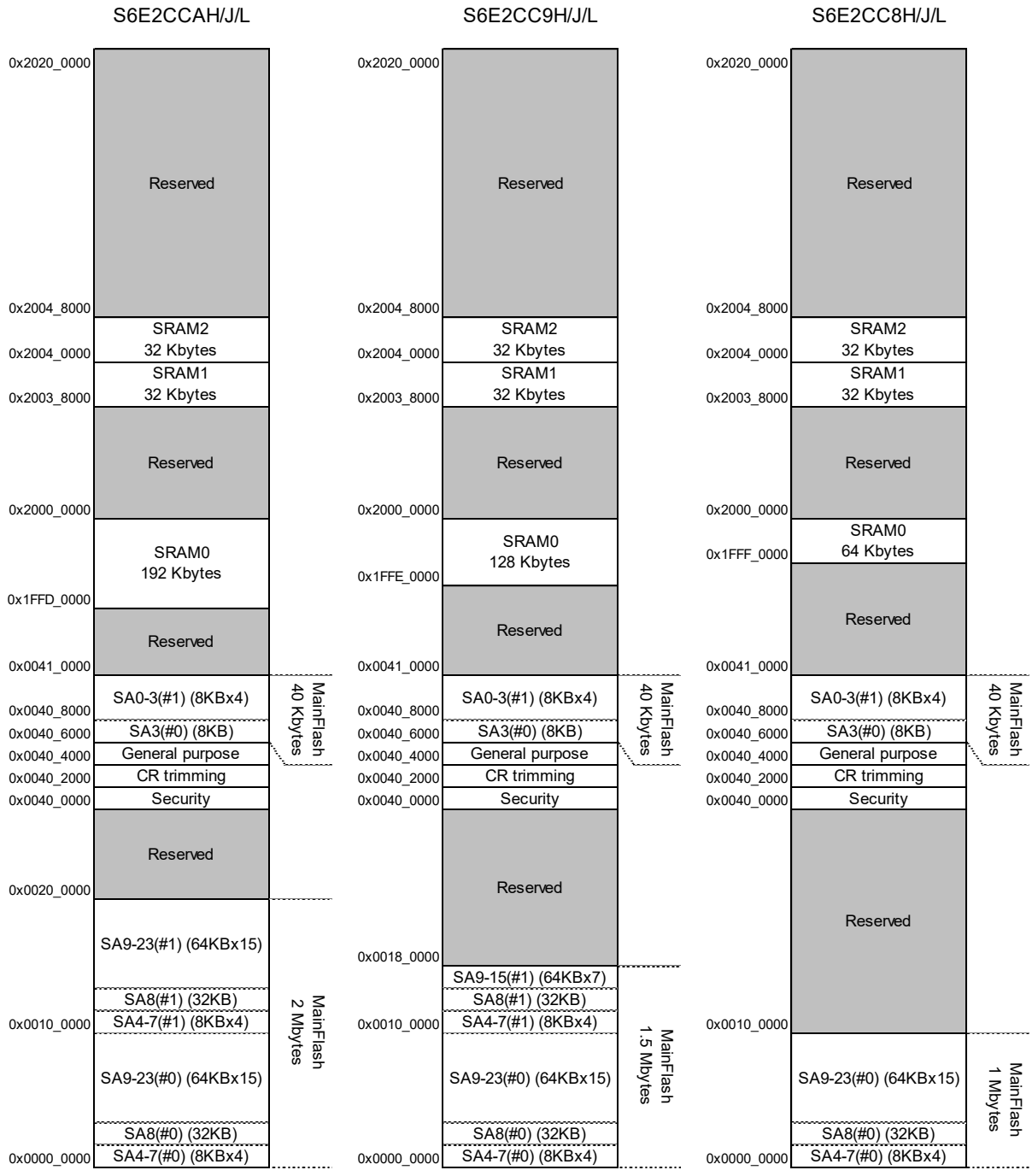
See Memory size in 2. Product Lineup to confirm the memory size.

10. Memory Map

Memory Map (1)

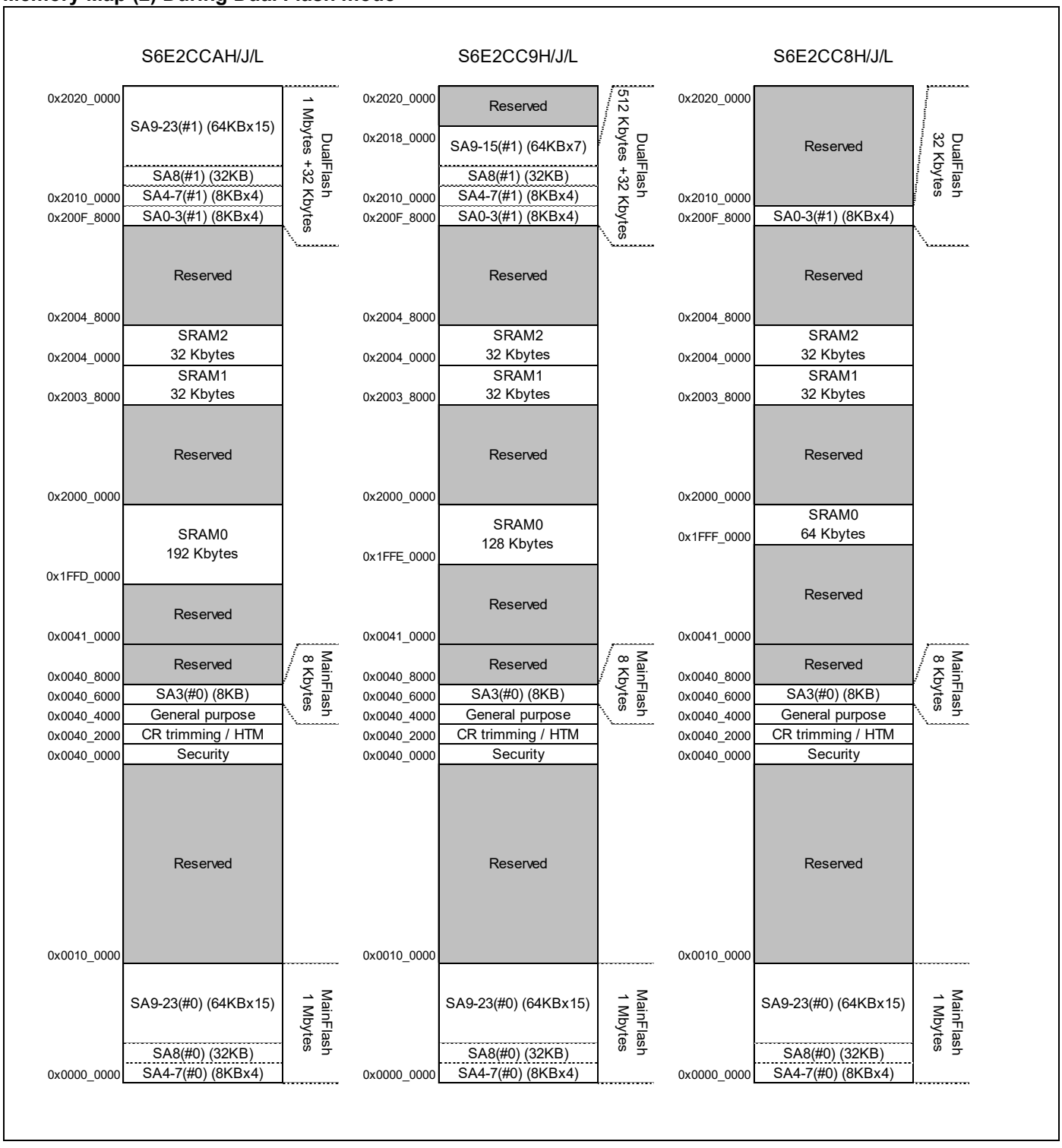


Memory Map (2)

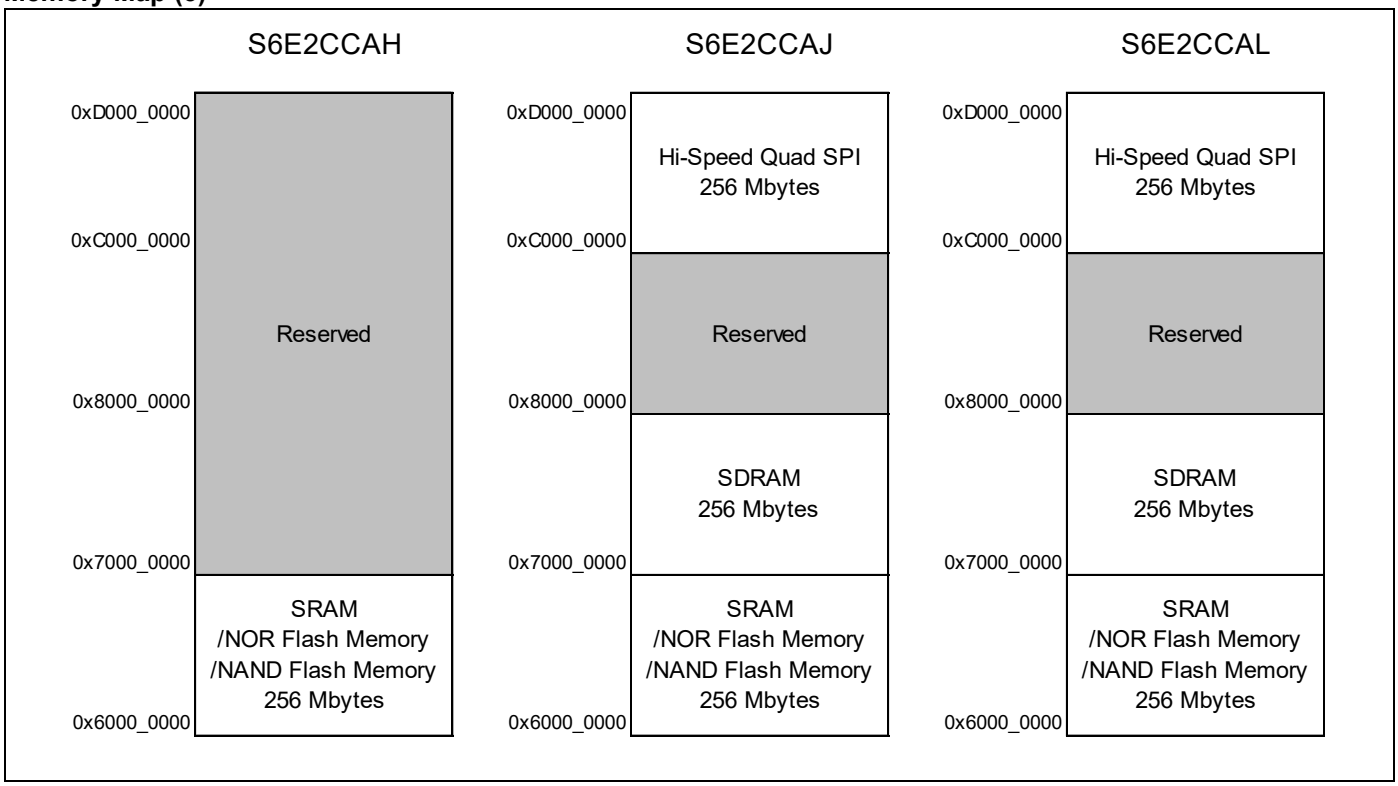


*: See S6E2Cx Series Flash Programming Manual to confirm the details of flash memory.

Memory Map (2) During Dual Flash mode



Memory Map (3)


S6E2CCAH
0xD000_0000
0xC000_0000
Reserved
0x8000_0000
0x7000_0000
SRAM
/NOR Flash Memory
/NAND Flash Memory
256 Mbytes
0x6000_0000
S6E2CCAJ
0xD000_0000
Hi-Speed Quad SPI
256 Mbytes
0xC000_0000
Reserved
0x8000_0000
SDRAM
256 Mbytes
0x7000_0000
SRAM
/NOR Flash Memory
/NAND Flash Memory
256 Mbytes
0x6000_0000
S6E2CCAL
0xD000_0000
Hi-Speed Quad SPI
256 Mbytes
0xC000_0000
Reserved
0x8000_0000
SDRAM
256 Mbytes
0x7000_0000
SRAM
/NOR Flash Memory
/NAND Flash Memory
256 Mbytes
0x6000_0000

Peripheral Address Map

Start Address	End Address	Bus	Peripherals
0x4000_0000	0x4000_0FFF	AHB	MainFlash I/F register
0x4000_1000	0x4000_FFFF		Reserved
0x4001_0000	0x4001_0FFF	APB0	Clock/reset control
0x4001_1000	0x4001_1FFF		Hardware watchdog timer
0x4001_2000	0x4001_2FFF		Software watchdog timer
0x4001_3000	0x4001_4FFF		Reserved
0x4001_5000	0x4001_5FFF		Dual-timer
0x4001_6000	0x4001_FFFF		Reserved
0x4002_0000	0x4002_0FFF	APB1	Multi-Function Timer unit 0
0x4002_1000	0x4002_1FFF		Multi-Function Timer unit 1
0x4002_2000	0x4002_2FFF		Multi-Function Timer unit 1
0x4002_3000	0x4002_3FFF		Reserved
0x4002_4000	0x4002_4FFF		PPG
0x4002_5000	0x4002_5FFF		Base timer
0x4002_6000	0x4002_6FFF		Quadrature position/revolution counter
0x4002_7000	0x4002_7FFF		A/D converter
0x4002_8000	0x4002_DFFF		Reserved
0x4002_E000	0x4002_EFFF		Internal CR trimming
0x4002_F000	0x4002_FFFF		Reserved
0x4003_0000	0x4003_0FFF	APB2	External interrupt controller
0x4003_1000	0x4003_1FFF		Interrupt request batch-read function
0x4003_2000	0x4003_2FFF		Reserved
0x4003_3000	0x4003_3FFF		D/A converter
0x4003_4000	0x4003_4FFF		Reserved
0x4003_5000	0x4003_57FF		Low voltage detector
0x4003_5800	0x4003_5FFF		Deep standby mode Controller
0x4003_6000	0x4003_6FFF		USB clock generator
0x4003_7000	0x4003_7FFF		CAN prescaler
0x4003_8000	0x4003_8FFF		Multi-function serial interface
0x4003_9000	0x4003_9FFF		CRC
0x4003_A000	0x4003_AFFF		Watch counter
0x4003_B000	0x4003_BFFF		RTC/port control
0x4003_C000	0x4003_C0FF		Low-speed CR prescaler
0x4003_C100	0x4003_C7FF		Peripheral clock gating
0x4003_C800	0x4003_CFFF		Reserved
0x4003_D000	0x4003_DFFF		I^2S prescaler
0x4003_E000	0x4003_EFFF		Reserved
0x4003_F000	0x4003_FFFF		External memory interface

Start Address	End Address	Bus	Peripherals
0x4004_0000	0x4004_FFFF	AHB	USB ch 0
0x4005_0000	0x4005_FFFF		USB ch 1
0x4006_0000	0x4006_0FFF		DMAC register
0x4006_1000	0x4006_1FFF		DSTC register
0x4006_2000	0x4006_2FFF		CAN ch 0
0x4006_3000	0x4006_3FFF		CAN ch 1
0x4006_4000	0x4006_5FFF		Ethernet-MAC ch 0
0x4006_6000	0x4006_6FFF		Ethernet-MAC setting register
0x4006_7000	0x4006_BFFF		Reserved
0x4006_C000	0x4006_CFFF		I^2S
0x4006_D000	0x4006_DFFF		Reserved
0x4006_E000	0x4006_EFFF		SD card I/F
0x4006_F000	0x4006_FFFF		GPIO
0x4007_0000	0x4007_FFFF		CAN-FD (CAN ch 2)
0x4008_0000	0x4008_0FFF		Programmable-CRC
0x4008_1000	0x41FF_FFFF		Reserved
0x200E_0000	0x200E_FFFF		Workflash I/F register
0xD000_0000	0xDFFF_FFFF		High-speed quad SPI control register

11. Pin Status in Each CPU State

The terms used for pin status have the following meanings:

- INITX = 0

  This is the period when the INITX pin is at the L level.

- INITX = 1

  This is the period when the INITX pin is at the H level.

- SPL = 0

  This is the status that the standby pin level setting bit (SPL) in the standby mode control register (STB_CTL) is set to 0.

- SPL = 1

  This is the status that the standby pin level setting bit (SPL) in the standby mode control register (STB_CTL) is set to 1.

- Input enabled

  Indicates that the input function can be used.

- Internal input fixed at 0

  This is the status that the input function cannot be used. Internal input is fixed at L.

- Hi-Z

  Indicates that the pin drive transistor is disabled and the pin is put in the Hi-Z state.

- Setting disabled

  Indicates that the setting is disabled.

- Maintain previous state

  Maintains the state that was immediately prior to entering the current mode.
  If a built-in peripheral function is operating, the output follows the peripheral function.
  If the pin is being used as a port, that output is maintained.

- Analog input is enabled

  Indicates that the analog input is enabled.

- Trace output

  Indicates that the trace function can be used.

- GPIO selected

  In Deep standby mode, pins switch to the general-purpose I/O port.

- Setting prohibition

  Prohibition of a setting by specification limitation

List of Pin Behavior by Mode State

Pin Status Type	Function Group	Power-On Reset or Low-Voltage Detection State	INITX Input State	Device Internal Reset State	Run mode or Sleep mode State	Timer mode, RTC mode, or Stop mode State		Deep Standby RTC mode or Deep Standby Stop mode State		Return from Deep Standby mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable				Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1				INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
A	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/internal input fixed at 0	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	Main crystal oscillator input pin/ external main clock input selected	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input Enabled
B	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/internal input fixed at 0	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	External main clock input selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/internal input fixed at 0	Maintain previous state	Hi-Z/internal input fixed at 0	Maintain previous State
	Main crystal oscillator output pin	Hi-Z/ internal input fixed at 0/ or input enable	Hi-Z/ internal input fixed at 0	Hi-Z/ internal input fixed at 0	Maintain previous state while oscillator active/ When oscillation stops[1], it will be Hi-Z/ Internal input fixed at 0					
C	INITX input pin	Pull-up/ input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled
D	Mode input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
E	Mode input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/ input enabled	GPIO selected	Hi-Z/ input enabled	GPIO selected

[1] Oscillation is stopped at Sub Timer mode, sub CR Timer mode, RTC mode, Stop mode, Deep Standby RTC mode, and Deep Standby Stop mode.

Pin Status Type	Function Group	Power-On Reset or Low-Voltage Detection State	INITX Input State	Device Internal Reset State	Run mode or Sleep mode State	Timer mode, RTC mode, or Stop mode State		Deep Standby RTC mode or Deep Standby Stop mode State		Return from Deep Standby mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
F	NMIX selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	WKUP input enabled	Hi-Z/ WKUP input enabled	Maintain previous state
	Resource other than above selected	Hi-Z	Hi-Z/ input enabled	Hi-Z/ input enabled			Hi-Z/ internal input fixed at 0			GPIO selected
	GPIO selected									
G	JTAG selected	Hi-Z	Pull-up/ input enabled	Pull-up/ input enabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state
	GPIO selected	Setting disabled	Setting disabled	Setting disabled			Hi-Z/ internal input fixed at 0	GPIO selected, internal input fixed at 0	Hi-Z/ internal input fixed at 0	GPIO selected
H	JTAG selected	Hi-Z	Pull-up/ input enabled	Pull-up/ input enabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state
	Resource other than above selected	Setting disabled	Setting disabled	Setting disabled			Hi-Z/Internal input fixed at 0	GPIO selected, internal input fixed at 0	Hi-Z/Internal input fixed at 0	GPIO selected
	GPIO selected									
I	Resource selected	Hi-Z	Hi-Z/ input enabled	Hi-Z/ input enabled	Maintain previous state	Maintain previous state	Hi-Z/Internal input fixed at 0	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	GPIO selected									
J	Analog output selected	Hi-Z	Hi-Z/ input enabled	Hi-Z/ input enabled	Maintain previous state	[2]	[3]	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	External interrupt enable selected					Maintain previous state	Maintain previous state			
	Resource other than above selected						Hi-Z/internal input fixed at 0			

[2] Maintain previous state at Timer mode. GPIO selected internal input fixed at 0 at RTC mode, Stop mode.
[3] Maintain previous state at Timer mode. Hi-Z/internal input fixed at 0 at RTC mode, Stop mode..

Pin Status Type	Function Group	Power-On Reset or Low-Voltage Detection State	INITX Input State	Device Internal Reset State	Run mode or Sleep mode State	Timer mode, RTC mode, or Stop mode State		Deep Standby RTC mode or Deep Standby Stop mode State		Return from Deep Standby mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
	GPIO selected									
K	External interrupt enable selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	Resource other than above selected	Hi-Z	Hi-Z/ input enabled	Hi-Z/ input enabled			Hi-Z/internal input fixed at 0			
	GPIO selected									
L	Analog input selected	Hi-Z	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled
	Resource other than above selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/internal input fixed at 0	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	GPIO selected									
M	Analog input selected	Hi-Z	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled
	External interrupt enable selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	Resource other than above selected						Hi-Z/internal input fixed at 0			
	GPIO selected									

Pin Status Type	Function Group	Power-On Reset or Low-Voltage Detection State	INITX Input State	Device Internal Reset State	Run mode or Sleep mode State	Timer mode, RTC mode, or Stop mode State		Deep Standby RTC mode or Deep Standby Stop mode State		Return from Deep Standby mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
N	Analog input selected	Hi-Z	Hi-Z/ internal input fixed at0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled
	Trace selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Trace output	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	Resource other than above selected						Hi-Z/internal input fixed at 0			
	GPIO selected									
O	Analog input selected	Hi-Z	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled
	Trace selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Trace output	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	External interrupt enable selected						Maintain previous state			
	Resource other than above selected						Hi-Z/internal input fixed at 0			
	GPIO selected									

Pin Status Type	Function Group	Power-On Reset or Low-Voltage Detection State	INITX Input State	Device Internal Reset State	Run mode or Sleep mode State	Timer mode, RTC mode, or Stop mode State		Deep Standby RTC mode or Deep Standby Stop mode State		Return from Deep Standby mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
P	Analog input selected	Hi-Z	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled
	WKUP enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	WKUP input enabled	Hi-Z/ WKUP input enabled	GPIO selected
	Resource other than above selected						Hi-Z/internal input fixed at 0	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	
	GPIO selected									
Q	WKUP enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	WKUP input enabled	Hi-Z/ WKUP input enabled	WKUP input enabled
	External interrupt enable selected							GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	Resource other than above selected	Hi-Z	Hi-Z/ input enabled	Hi-Z/ input enabled			Hi-Z/internal input fixed at 0			
	GPIO selected									
R	GPIO selected	Hi-Z	Hi-Z/ input enabled	Hi-Z/ input enabled	Maintain previous state	Maintain previous state	Hi-Z/internal input fixed at 0	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	USB I/O pin	Setting disabled	Setting disabled	Setting disabled	Hi-Z at trans-mission/ input enabled/ internal input fixed at 0 at reception	Hi-Z at trans-mission/ input enabled/ internal input fixed at 0 at reception	Hi-Z at trans-mission/ input enabled/ internal input fixed at 0 at reception	Hi-Z/ input enabled	Hi-Z/ input enabled	Hi-Z/ input enabled

Pin Status Type	Function Group	Power-On Reset or Low-Voltage Detection State	INITX Input State	Device Internal Reset State	Run mode or Sleep mode State	Timer mode, RTC mode, or Stop mode State		Deep Standby RTC mode or Deep Standby Stop mode State		Return from Deep Standby mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
V	Ethernet I/O selected[4]	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at "0	GPIO selected
	Resource other than above selected	Hi-Z	Hi-Z/ input enabled	Hi-Z/ input enabled			Hi-Z/internal input fixed at 0			
	GPIO selected									
W	Ethernet input/output selected[4]	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	External interrupt enable selected									
	Resource other than above selected	Hi-Z	Hi-Z/ input enabled	Hi-Z/ input enabled			Hi-Z/internal input fixed at 0			
	GPIO selected									

[4] It shows the case selected by EPFR14.E_SPLC register

List of VBAT Domain Pin Status

VBAT Pin Status Type	Function Group	Power-on reset[5]	INITX Input State	Device Internal Reset State	Run mode or Sleep mode State	Timer mode, RTC mode, or Stop mode State		Deep Standby RTC mode or Deep Standby Stop mode state		Return from Deep Standby mode State	VBAT RTC mode State	Return from VBAT RTC mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable	Power Supply Stable	Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1	-	-
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-	-	-
S	GPIO selected	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Setting prohibition	-
	Sub crystal oscillator input pin/ external sub clock input selected	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Maintain previous state	Maintain previous state
T	GPIO selected	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Setting prohibition	-
	External sub clock input selected	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state
	Sub crystal oscillator output pin	Hi-Z/ internal input fixed at 0/ or input enable	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state/ When oscillation stops, Hi-Z[6]	Maintain previous state/ When oscillation stops, Hi-Z[6]	Maintain previous state/ When oscillation stops, Hi-Z[6]	Maintain previous state/ When oscillation stops, Hi-Z[6]	Maintain previous state	Maintain previous state	Maintain previous state
U	Resource selected	Hi-Z	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state
	GPIO selected											

[5] When VBAT and VCC power on.
[6] When the SOSCNTL bit in the WTOSCCNT register is 0, the sub crystal oscillator output pin is maintained in the previous state. When the SOSCNTL bit in the WTOSCCNT register is 1, oscillation is stopped at Stop mode and Deep Standby Stop mode.

12. Electrical Characteristics

12.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage[7,8]	V_{CC}	V_{SS} - 0.5	V_{SS} + 6.5	V	
Power supply voltage (for USB)[7,9]	$USBV_{CC}0$	V_{SS} - 0.5	V_{SS} + 6.5	V	
Power supply voltage (for USB) [7, 9]	$USBV_{CC}1$	V_{SS} - 0.5	V_{SS} + 6.5	V	
Power supply voltage (for Ethernet-MAC) [7, 10]	$ETHV_{CC}$	V_{SS} - 0.5	V_{SS} + 6.5	V	
Power supply voltage (VBAT) [7 ,11]	V_{BAT}	V_{SS} - 0.5	V_{SS} + 6.5	V	
Analog power supply voltage [7, 12]	AV_{CC}	V_{SS} - 0.5	V_{SS} + 6.5	V	
Analog reference voltage [7 ,12]	AVRH	V_{SS} - 0.5	V_{SS} + 6.5	V	
Input voltage [7]	V_I	V_{SS} - 0.5	V_{CC} + 0.5 (≤ 6.5V)	V	Except for USB and Ethernet-MAC pin
		V_{SS} - 0.5	$USBV_{CC}0$ + 0.5 (≤ 6.5V)	V	USB ch 0 pin
		V_{SS} - 0.5	$USBV_{CC}1$ + 0.5 (≤ 6.5V)	V	USB ch 1 pin
		V_{SS} - 0.5	$ETHV_{CC}$ + 0.5 (≤ 6.5V)	V	Ethernet-MAC Pin
		V_{SS} - 0.5	V_{SS} + 6.5	V	5V tolerant
Analog pin input voltage [7]	V_{IA}	V_{SS} - 0.5	AV_{CC} + 0.5 (≤ 6.5V)	V	
Output voltage [7]	V_O	V_{SS} - 0.5	V_{CC} + 0.5 (≤ 6.5V)	V	
L level maximum output current[13]	I_{OL}	-	10	mA	4 mA type
			20	mA	8 mA type
			20	mA	10 mA type
			20	mA	12 mA type
			22.4	mA	I^2C Fm+
L level average output current[14]	I_{OLAV}	-	4	mA	4 mA type
			8	mA	8 mA type
			10	mA	10 mA type
			12	mA	12 mA type
			20	mA	I^2C Fm+
L level total maximum output current	$\sum I_{OL}$	-	100	mA	
L level total maximum output current [15]	$\sum I_{OLAV}$	-	50	mA	
H level maximum output current [13]	I_{OH}	-	- 10	mA	4 mA type
			-20	mA	8 mA type
			- 20	mA	10 mA type
			- 20	mA	12 mA type

[7] These parameters are based on the condition that $V_{SS} = AV_{SS} = 0.0V$.
[8] V_{CC} must not drop below V_{SS} - 0.5V.
[9] $USBV_{CC}0$, $USBV_{CC}1$ must not drop below V_{SS} - 0.5V.
[10] $ETHV_{CC}$ must not drop below V_{SS} - 0.5V.
[11] V_{BAT} must not drop below V_{SS} - 0.5V.
[12] Ensure that the voltage does not exceed V_{CC} + 0.5V, for example, when the power is turned on.
[13] The maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.
[14] The average output current is defined as the average current value flowing through any one of the corresponding pins for a 100 ms period.
[15] The total average output current is defined as the average current value flowing through all of corresponding pins for a 100 ms period.

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
H level average output current [14]	I_{OHAV}	-	- 4	mA	4 mA type
			-8	mA	8 mA type
			- 10	mA	10 mA type
			- 12	mA	12 mA type
H level total maximum output current	$\sum I_{OH}$	-	- 100	mA	
H level total average output current [15]	$\sum I_{OHAV}$	-	- 50	mA	
Storage temperature	T_{STG}	- 55	+ 150	°C	

WARNING:

− *Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings. Do not exceed any of these ratings.*

12.2 Recommended Operating Conditions

Parameter	Symbol	Conditions	Value		Unit	Remarks
			Min	Max		
Power supply voltage	V_{CC}	-	2.7 [16]	5.5	V	
Power supply voltage (for USB ch 0)	$USBV_{CC}0$	-	3.0	3.6 ($\leq V_{CC}$)	V	When P81/UDP0 and P80/UDM0 pins are used as USB (UDP0, UDM0)
			2.7	5.5 ($\leq V_{CC}$)		When P81/UDP0 and P80/UDM0 pins are used as GPIO (P81, P80)
Power supply voltage (for USB ch 1)	$USBV_{CC}1$	-	3.0	3.6 ($\leq V_{CC}$)	V	When P83/UDP1 and P82/UDM1 pins are used as USB (UDP1, UDM1)
			2.7	5.5 ($\leq V_{CC}$)		When P83/UDP1 and P82/UDM1 pins are used as GPIO (P83, P82)
Power supply voltage (for Ethernet-MAC)	$ETHV_{CC}$	-	3.0	3.6 ($\leq V_{CC}$)	V	When the pins in Ethernet-MAC Pins, except the P6E/ADTG_5/SCK4_1/IC23_1/INT29_0/E_PPS pin, are used as Ethernet-MAC pins
			4.5	5.5 ($\leq V_{CC}$)		
			2.7	5.5 ($\leq V_{CC}$)		When the pins in Ethernet-MAC Pins, except the P6E/ADTG_5/SCK4_1/IC23_1/INT29_0/E_PPS pin, are used as Ethernet-MAC pins
Power supply voltage (VBAT)	V_{BAT}	-	1.65	5.5	V	
Analog power supply voltage	AV_{CC}	-	2.7	5.5	V	$AV_{CC} = V_{CC}$
Analog reference voltage	AVRH	-	[17]	AV_{CC}	V	
	AVRL	-	AV_{SS}	AV_{SS}	V	
Operating temperature: Junction temperature	T_J	-	- 40	+ 125	°C	
Operating temperature: Ambient temperature	T_A	-	-40	[18]	°C	

[16] For the voltage range between V_{CC}(min) and the low voltage detection reset (V_{DH}), the MCU must be clocked from either the High-speed CR or the low-speed CR.

[17] The minimum value of analog reference voltage depends on the value of compare clock cycle (Tcck). See 12.5 12-bit A/D Converter for the details.

[18] The maximum temperature of the ambient temperature (T_A) can guarantee a range that does not exceed the junction temperature (T_J).
The calculation formula of the ambient temperature (T_A) is:

$$T_A\ (Max) = T_J(Max) - Pd(Max) \times \theta_{JA}$$

Pd: Power dissipation (W)
θ_{JA}: Package thermal resistance (°C/W)

$$Pd\ (Max) = V_{CC} \times I_{CC}\ (Max) + \Sigma\ (I_{OL} \times V_{OL}) + \Sigma\ ((V_{CC} - V_{OH}) \times (-I_{OH}))$$

I_{OL}: L level output current
I_{OH}: H level output current

V_{OL}: L level output voltage
V_{OH}: H level output voltage

Package thermal resistance and maximum permissible power for each package are shown below.
The operation is guaranteed maximum permissible power or less for semiconductor devices.

Table for Package Thermal Resistance and Maximum Permissible Power

Package	Printed Circuit Board	Thermal Resistance θja (°C/W)	Maximum Permissible Power (mW)	
			T_A = +85 °C	T_A = +105 °C
LQS144 (0.5-mm pitch)	Single-layered both sides	48	833	417
	4 layers	33	1212	606
LQP176 (0.5-mm pitch)	Single-layered both sides	45	889	444
	4 layers	31	1290	645
LQQ216 (0.4-mm pitch)	Single-layered both sides	46	870	435
	4 layers	32	1250	625
LBE192 (0.8-mm pitch)	Single-layered both sides	-	-	-
	4 layers	35	1143	571

WARNING:

- *The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges. Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.*
- *No warranty is made with respect to uses, operating conditions, or combinations not represented on the datasheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.*

Ethernet-MAC Pins

Pin Name	Ethernet-MAC Function	Except For Ethernet-MAC Function	Power Supply Type
P6E/ADTG_5/SCK4_1/IC23_1/INT29_0/E_PPS	E_PPS [19]	P6E/ADTG_5/SCK4_1/IC23_1/INT29_0	V_{CC}
PC0/E_RXER	E_RXER	PC0	$ETHV_{CC}$
PC1/TIOB6_0/E_RX03	E_RX03	PC1/TIOB6_0	
PC2/TIOA6_0/E_RX02	E_RX02	PC2/TIOA6_0	
PC3/TIOB7_0/E_RX01	E_RX01	PC3/TIOB7_0	
PC4/TIOA7_0/E_RX00	E_RX00	PC4/TIOA7_0	
PC5/TIOB14_0/E_RXDV	E_RXDV	PC5/TIOB14_0	
PC6/TIOA14_0/E_MDIO	E_MDIO	PC6/TIOA14_0	
PC7/INT13_0/E_MDC/CROUT_1	E_MDC	PC7/INT13_0/CROUT_1	
PC8/E_RXCK_REFCK	E_RXCK_REFCK	PC8	
PC9/TIOB15_0/E_COL	E_COL	PC9/TIOB15_0	
PCA/TIOA15_0/E_CRS	E_CRS	PCA/TIOA15_0	
PCB/INT28_0/E_COUT	E_COUT	PCB/INT28_0	
PCC/E_TCK	E_TCK	PCC	
PCD/SOT4_1/INT14_0/E_TXER	E_TXER	PCD/SOT4_1/INT14_0	
PCE/SIN4_1/INT15_0/E_TX03	E_TX03	PCE/SIN4_1/INT15_0	
PCF/RTS4_1/INT12_0/E_TX02	E_TX02	PCF/RTS4_1/INT12_0	
PD0/INT30_1/E_TX01	E_TX01	PD0/INT30_1	
PD1/INT31_1/E_TX00	E_TX00	PD1/INT31_1	
PD2/CTS4_1/FRCK2_1/E_TXEN	E_TXEN	PD2/CTS4_1/FRCK2_1	

[19] It is used to confirm the PTP counter cycle in Ethernet-MAC by waveforms.

Calculation Method of Power Dissipation (Pd)

The power dissipation is shown in the following formula.

$$Pd = V_{CC} \times I_{CC} + \Sigma (I_{OL} \times V_{OL}) + \Sigma ((V_{CC}-V_{OH}) \times (-I_{OH}))$$

I_{OL}: L level output current
I_{OH}: H level output current
V_{OL}: L level output voltage
V_{OH}: H level output voltage

I_{CC} is the current drawn by the device.
It can be analyzed as follows.

$$I_{CC} = I_{CC}(INT) + \Sigma I_{CC}(IO)$$

I_{CC} (INT): Current drawn by internal logic and memory, etc. through the regulator

ΣI_{CC} (IO): Sum of current (I/O switching current) drawn by the output pin

For I_{CC} (INT), it can be anticipated by "(1) Current Rating" in "12.3. DC Characteristics" (This rating value does not include I_{CC} (IO) for a value at pin fixed).
For I_{CC} (IO), it depends on system used by customers.
The calculation formula is shown below.

$$I_{CC}(IO) = (C_{INT} + C_{EXT}) \times V_{CC} \times f_{SW}$$

C_{INT}: Pin internal load capacitance
C_{EXT}: External load capacitance of output pin
f_{SW}: Pin switching frequency

Parameter	Symbol	Conditions	Capacitance Value
Pin internal load capacitance	C_{INT}	4 mA type	1.93 pF
		8 mA type	3.45 pF
		12 mA type	3.42 pF

Calculate I_{CC} (Max) as follows when the power dissipation can be evaluated by yourself:

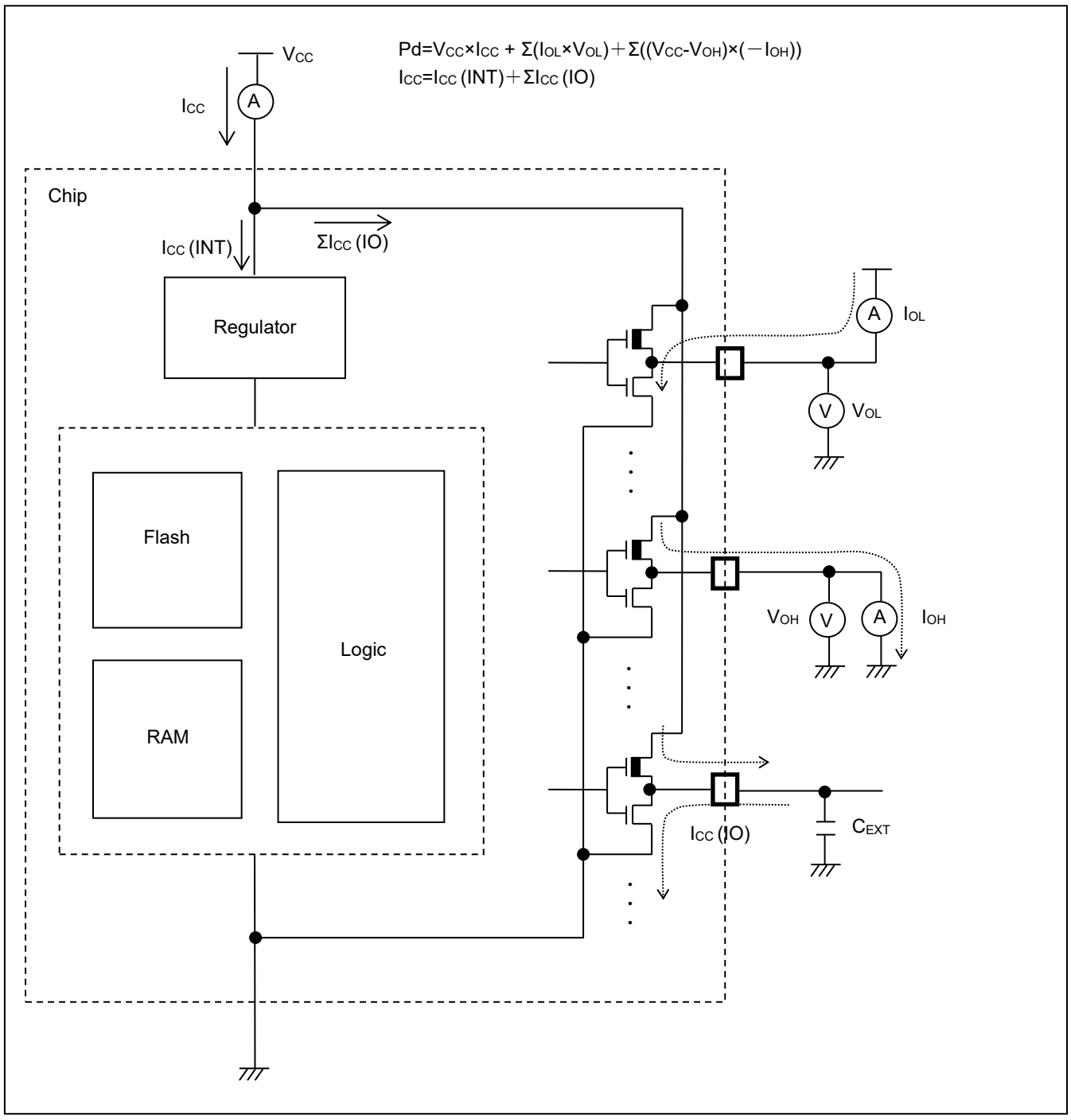
Measure current value I_{CC} (Typ) at normal temperature (+25°C).

Add maximum leakage current value I_{CC} (leak_max) at operating on a value in (1).

$$I_{CC}(Max) = I_{CC}(Typ) + I_{CC}(leak_max)$$

Parameter	Symbol	Conditions	Current Value
Maximum leakage current at operating	I_{CC} (leak_max)	T_J = +125 °C	79.2 mA
		T_J = +105 °C	39.4 mA
		T_J = +85 °C	26.5 mA

Current Explanation Diagram



12.3 DC Characteristics

12.3.1 Current Rating

Table 12-1 Typical and Maximum Current Consumption in Normal Operation (PLL), Code Running from Flash Memory (Flash Accelerator Mode and Trace Buffer Function Enabled)

Parameter	Symbol	Pin Name	Conditions		Frequency[20]	Value		Unit	Remarks
						Typ[21]	Max[22]		
Power supply current	I_{CC}	VCC	Normal operation[23], [24] (PLL)	[25]	200 MHz	117	224	mA	[26] When all peripheral clocks are on
					192 MHz	113	219	mA	
					180 MHz	106	211	mA	
				[27]	160 MHz	95	197	mA	
					144 MHz	86	186	mA	
					120 MHz	73	169	mA	
					100 MHz	61	155	mA	
					80 MHz	50	140	mA	
					60 MHz	39	126	mA	
					40 MHz	27	112	mA	
					20 MHz	16	97	mA	
					8 MHz	8.7	88.9	mA	
					4 MHz	6.4	86.1	mA	
				[25]	200 MHz	71	168	mA	[26] When all peripheral clocks are off
					192 MHz	68	165	mA	
					180 MHz	64	159	mA	
				[27]	160 MHz	58	151	mA	
					144 MHz	52	144	mA	
					120 MHz	44	134	mA	
					100 MHz	38	126	mA	
					80 MHz	31	117	mA	
					60 MHz	24	109	mA	
					40 MHz	17	100	mA	
					20 MHz	10	91	mA	
					8 MHz	6.3	86.1	mA	
					4 MHz	5.0	84.5	mA	

[20] Frequency is a value of HCLK when PCLK0 = PCLK1 = PCLK2 = HCLK/2
[21] T_A = +25 °C, V_{CC} = 3.3V
[22] T_J = +125 °C, V_{CC} = 5.5V
[23] Firmware being executed during data collection for this table is not being accessed from the MainFlash memory.
[24] When using a 4 MHz crystal oscillator (including the current consumption of the oscillation circuit)
[25] When stopping flash accelerator mode and trace buffer function (FRWTR.RWT = 11, FBFCR.BE = 1)
[26] When all ports are fixed
[27] When stopping flash accelerator mode and trace buffer function (FRWTR.RWT = 10, FBFCR.BE = 1)

Table 12-2 Typical and Maximum Current Consumption in Normal Operation (PLL), Code with Data Accessing Running from Flash Memory (Flash Accelerator Mode and Trace Buffer Function Disabled)

Parameter	Symbol	Pin Name	Conditions		Frequency[28]	Value		Unit	Remarks
						Typ[29]	Max[30]		
Power supply current	I_{CC}	VCC	Normal operation[31], [32] (PLL)	[33]	200 MHz	128	236	mA	[34] When all peripheral clocks are on
					192 MHz	123	230	mA	
					180 MHz	116	221	mA	
				[35]	160 MHz	102	205	mA	
					144 MHz	93	193	mA	
					120 MHz	79	175	mA	
					100 MHz	67	161	mA	
					80 MHz	54	145	mA	
					60 MHz	42	130	mA	
					40 MHz	30	115	mA	
					20 MHz	17	99	mA	
					8 MHz	9.2	90.0	mA	
					4 MHz	6.7	86.9	mA	
				[33]	200 MHz	74	170	mA	[34] When all peripheral clocks are off
					192 MHz	71	167	mA	
					180 MHz	67	162	mA	
				[35]	160 MHz	59	152	mA	
					144 MHz	53	145	mA	
					120 MHz	45	135	mA	
					100 MHz	39	127	mA	
					80 MHz	32	118	mA	
					60 MHz	25	110	mA	
					40 MHz	18	101	mA	
					20 MHz	11	92	mA	
					8 MHz	6.5	86.8	mA	
					4 MHz	5.1	85.0	mA	

[28] Frequency is a value of HCLK when PCLK0 = PCLK1 = PCLK2 = HCLK
[29] T_A = +25 °C, V_{CC} = 3.3V
[30] T_J = +125 °C, V_{CC} = 5.5V
[31] With data access to a MainFlash memory.
[32] When using a 4 MHz crystal oscillator (including the current consumption of the oscillation circuit)
[33] When stopping flash accelerator mode and trace buffer function (FRWTR.RWT = 11, FBFCR.BE = 0)
[34] When all ports are fixed
[35] When stopping flash accelerator mode and trace buffer function (FRWTR.RWT = 10, FBFCR.BE = 0)

Table 12-3 Typical and Maximum Current Consumption in Normal Operation (PLL), Code with Data Accessing Running from Flash Memory (Flash 0 Wait-Cycle Mode and Read Access 0 Wait)

Parameter	Symbol	Pin Name	Conditions		Frequency[36]	Value		Unit	Remarks
						Typ[37]	Max[38]		
Power supply current	I_{CC}	VCC	Normal operation [39, 40] (PLL)	[41]	72 MHz	71	161	mA	[42] When all peripheral clocks are on
					60 MHz	62	150	mA	
					48 MHz	51	138	mA	
					36 MHz	40	125	mA	
					24 MHz	29	112	mA	
					12 MHz	17	98	mA	
					8 MHz	13	93	mA	
					4 MHz	8.4	88.5	mA	
				[41]	72 MHz	46	132	mA	[42] When all peripheral clocks are off
					60 MHz	41	125	mA	
					48 MHz	34	118	mA	
					36 MHz	27	110	mA	
					24 MHz	20	102	mA	
					12 MHz	12	93	mA	
					8 MHz	9.4	89.7	mA	
					4 MHz	6.5	86.4	mA	

[36] Frequency is a value of HCLK when PCLK0 = PCLK1 = PCLK2 = HCLK
[37] T_A = +25 °C, V_{CC} = 3.3 V
[38] T_J = +125 °C, V_{CC} = 5.5 V
[39] With data access to a MainFlash memory.
[40] When using a 4 MHz crystal oscillator (including the current consumption of the oscillation circuit)
[41] When operating flash 0 wait-cycle mode and read access 0 wait (FRWTR.RWT = 00, FBFCR.SD = 000)
[42] When all ports are fixed

Table 12-4 Typical and Maximum Current Consumption in Normal Operation (Other than PLL), Code with Data Accessing Running from Flash Memory (Flash 0 Wait-Cycle Mode and Read Access 0 Wait)

Parameter	Symbol	Pin Name	Conditions		Frequency[43]	Value		Unit	Remarks
						Typ[44]	Max[45]		
Power supply current	I_{CC}	VCC	Normal operation[46, 47] (main oscillation)	[48]	4 MHz	4.7	84.9	mA	[49] When all peripheral clocks are on
						3.9	83.8	mA	[49] When all peripheral clocks are off
			Normal operation[46] (built-in High-speed CR)	[48]	4 MHz	3.0	83.2	mA	[49] When all peripheral clocks are on
						2.1	82.0	mA	[49] When all peripheral clocks are off
			Normal operation[46, 50] (sub oscillation)	[48]	32 kHz	0.78	80.37	mA	[49] When all peripheral clocks are on
						0.77	80.36	mA	[49] When all peripheral clocks are off
			Normal operation[46] (built-in low-speed CR)	[48]	100 kHz	0.81	80.39	mA	[49] When all peripheral clocks are on
						0.78	80.38	mA	[49] When all peripheral clocks are off

[43] Frequency is a value of HCLK when PCLK0 = PCLK1 = PCLK2 = HCLK/2
[44] TA = +25 °C, VCC = 3.3V
[45] TJ = +125 °C, VCC = 5.5V
[46] With data access to a MainFlash memory.
[47] When using a 4 MHz crystal oscillator (including the current consumption of the oscillation circuit)
[48] When operating flash 0 wait-cycle mode and read access 0 wait (FRWTR.RWT = 00, FBFCR.SD = 000)
[49] When all ports are fixed
[50] When using a 32 kHz crystal oscillator (including the current consumption of the oscillation circuit)

Table 12-5 Typical and Maximum Current Consumption in Sleep Operation (PLL), when PCLK0 = PCLK1 = PCLK2 = HCLK/2

Parameter	Symbol	Pin Name	Conditions	Frequency[51]	Value		Unit	Remarks
					Typ[52]	Max[53]		
Power supply current	I_{CCS}	VCC	Sleep operation[54] (PLL)	200 MHz	88	188	mA	[55] When all peripheral clocks are on
				192 MHz	85	184	mA	
				180 MHz	80	178	mA	
				160 MHz	72	164	mA	
				144 MHz	65	156	mA	
				120 MHz	55	144	mA	
				100 MHz	47	134	mA	
				80 MHz	38	124	mA	
				60 MHz	30	114	mA	
				40 MHz	21	104	mA	
				20 MHz	12	93	mA	
				8 MHz	7.4	87.2	mA	
				4 MHz	5.8	85.2	mA	
				200 MHz	44	134	mA	[55] When all peripheral clocks are off
				192 MHz	42	132	mA	
				180 MHz	40	129	mA	
				160 MHz	36	123	mA	
				144 MHz	33	119	mA	
				120 MHz	28	113	mA	
				100 MHz	24	108	mA	
				80 MHz	20	103	mA	
				60 MHz	16	98	mA	
				40 MHz	12	93	mA	
				20 MHz	7.6	87.6	mA	
				8 MHz	5.2	84.7	mA	
				4 MHz	4.4	83.7	mA	

[51] Frequency is a value of HCLK when PCLK0 = PCLK1 = PCLK2 = HCLK/2
[52] T_A = +25°C, V_{CC} = 3.3V
[53] T_J = +125°C, V_{CC} = 5.5V
[54] When using a 4 MHz crystal oscillator (including the current consumption of the oscillation circuit)
[55] When all ports are fixed

Table 12-6 Typical and Maximum Current Consumption in Sleep Operation (PLL), when PCLK0 = PCLK1 = PCLK2 = HCLK

Parameter	Symbol	Pin Name	Conditions	Frequency[56]	Value		Unit	Remarks
					Typ[57]	Max[58]		
Power supply current	I_{CCS}	VCC	Sleep operation[59] (PLL)	72 MHz	45	130	mA	[60] When all peripheral clocks are on
				60 MHz	38	122	mA	
				48 MHz	31	114	mA	
				36 MHz	24	106	mA	
				24 MHz	18	99	mA	
				12 MHz	11	91	mA	
				8 MHz	8.6	88.3	mA	
				4 MHz	6.3	85.7	mA	
				72 MHz	20	103	mA	[60] When all peripheral clocks are off
				60 MHz	18	99	mA	
				48 MHz	15	96	mA	
				36 MHz	12	93	mA	
				24 MHz	9.1	89.3	mA	
				12 MHz	6.5	86.1	mA	
				8 MHz	5.5	84.9	mA	
				4 MHz	4.6	83.8	mA	

[56] Frequency is a value of HCLK when PCLK0 = PCLK1 = PCLK2 = HCLK
[57] T_A = +25°C, V_{CC} = 3.3V
[58] T_J = +125°C, V_{CC} = 5.5V
[59] When using a 4 MHz crystal oscillator (including the current consumption of the oscillation circuit)
[60] When all ports are fixed

Table 12-7 Typical and Maximum Current Consumption in Sleep Operation (Other than PLL), when PCLK0 = PCLK1 = PCLK2 = HCLK/2

Parameter	Symbol	Pin Name	Conditions	Frequency[61]	Value		Unit	Remarks
					Typ[62]	Max[63]		
Power supply current	I_{CCS}	VCC	Sleep operation[64] (main oscillation)	4 MHz	3.4	82.6	mA	[65] When all peripheral clocks are on
					2.5	81.7	mA	[65] When all peripheral clocks are off
			Sleep operation (built-in High-speed CR)	4 MHz	2.5	81.7	mA	[65] When all peripheral clocks are on
					1.7	80.9	mA	[65] When all peripheral clocks are off
			Sleep operation[66] (sub oscillation)	32 kHz	0.75	79.97	mA	[65] When all peripheral clocks are on
					0.74	79.96	mA	[65] When all peripheral clocks are off
			Sleep operation (built-in low-speed CR)	100 kHz	0.79	80.01	mA	[65] When all peripheral clocks are on
					0.76	79.98	mA	[65] When all peripheral clocks are off

[61] Frequency is a value of HCLK when PCLK0 = PCLK1 = PCLK2 = HCLK/2
[62] T_A = +25 °C, V_{CC} = 3.3V
[63] T_J = +125 °C, V_{CC} = 5.5V
[64] When using a 4 MHz crystal oscillator (including the current consumption of the oscillation circuit)
[65] When all ports are fixed.
[66] When using a 32 kHz crystal oscillator (including the current consumption of the oscillation circuit)

Table 12-8 Typical and Maximum Current Consumption in Stop Mode, TIMER Mode and RTC Mode

Parameter	Symbol	Pin Name	Conditions	Frequency	Value		Unit	Remarks
					Typ[67]	Max[68]		
Power supply current	I_{CCH}	VCC	Stop mode	-	0.56	3.01	mA	[69], [70] T_A = +25°C
					-	27.03	mA	[69], [70] T_A = +85°C
					-	39.92	mA	[69], [70] T_A = +105°C
	I_{CCT}		Timer mode[71] (main oscillation)	4 MHz	1.40	3.85	mA	[69], [70] T_A = +25°C
					-	27.87	mA	[69], [70] T_A = +85°C
					-	40.76	mA	[69], [70] T_A = +105°C
			Timer mode (built-in High-speed CR)	4 MHz	0.95	3.40	mA	[69], [70] T_A = +25°C
					-	27.42	mA	[69], [70] T_A = +85°C
					-	40.31	mA	[69], [70] T_A = +105°C
			Timer mode[72] (sub oscillation)	32 kHz	0.57	3.02	mA	[69], [70] T_A = +25°C
					-	27.04	mA	[69], [70] T_A = +85°C
					-	39.93	mA	[69], [70] T_A = +105°C
			Timer mode (built-in low-speed CR)	100 kHz	0.58	3.03	mA	[69], [70] T_A = +25°C
					-	27.05	mA	[69], [70] T_A = +85°C
					-	39.94	mA	[69], [70] T_A = +105°C
	I_{CCR}		RTC mode[71] (sub oscillation)	32 kHz	0.57	3.02	mA	[69], [70] T_A = +25°C
					-	27.04	mA	[69], [70] T_A = +85°C
					-	39.93	mA	[69], [70] T_A = +105°C

[67] V_{CC} = 3.3V
[68] V_{CC} = 5.5V
[69] When all ports are fixed
[70] When LVD is off
[71] When using a 4 MHz crystal oscillator (including the current consumption of the oscillation circuit)
[72] When using a 32 kHz crystal oscillator (including the current consumption of the oscillation circuit)

Table 12-9 Typical and Maximum Current Consumption in Deep Standby Stop Mode, Deep Standby RTC Mode and VBAT

Parameter	Symbol	Pin Name	Conditions	Frequency	Value		Unit	Remarks
					Typ[73]	Max[74]		
Power supply current	I_{CCHD}	VCC	Deep standby Stop mode (When RAM is off)	-	96	248	µA	[75], [76] T_A = +25°C
					-	3009	µA	[75], [76] T_A = +85°C
					-	3889	µA	[75], [76] T_A = +105°C
			Deep standby Stop mode (When RAM is on)	-	106	259	µA	[75], [76] T_A = +25°C
					-	3020	µA	[75], [76] T_A = +85°C
					-	3900	µA	[75], [76] T_A = +105°C
	I_{CCRD}		Deep standby RTC mode (When RAM is off)	32 kHz	96	248	µA	[75], [76] T_A = +25°C
					-	3009	µA	[75], [76] T_A = +85°C
					-	3889	µA	[75], [76] T_A = +105°C
			Deep standby RTC mode (When RAM is on)		106	259	µA	[75], [76] T_A = +25°C
					-	3020	µA	[75], [76] T_A = +85°C
					-	3900	µA	[75], [76] T_A = +105°C
	I_{CCVBAT}	VBAT	RTC stop[77]	-	0.0058	0.1	µA	[75], [76], [78] T_A = +25°C
					-	1.4	µA	[75], [76], [78] T_A = +85°C
					-	3.3	µA	[75], [76], [78] T_A = +105°C
			RTC operation[77]		1.0	1.8	µA	[75], [76] T_A = +25°C
					-	3.2	µA	[75], [76] T_A = +85°C
					-	5.1	µA	[75], [76] T_A = +105°C

[73] V_{CC} = 3.3 V
[74] V_{CC} = 5.5 V
[75] When all ports are fixed
[76] When LVD is off
[77] In the case of setting RTC after VCC power on.
[78] When sub oscillation is off

Table 12-10 Typical and Maximum Current Consumption in Low-voltage Detection Circuit, Main Flash Memory Write/Erase

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Low-voltage detection circuit (LVD) power supply current	I_{CCLVD}	VCC	At operation	-	4	7	µA	For occurrence of interrupt
MainFlash memory write/erase current	$I_{CCFLASH}$		At write/erase	-	13.4	15.9	mA	When programming or erase in flash memory, Flash Memory Write/Erase current (ICCFLASH) is added to the Power supply current (I_{CC}).

Peripheral Current Dissipation

Clock System	Peripheral	Unit	Frequency (MHz)			Unit	Remarks
			50	100	200		
HCLK	GPIO	All ports	0.39	0.81	1.56	mA	
	DMAC	-	0.99	1.97	3.82		
	DSTC	-	0.73	1.49	2.86		
	External bus I/F	-	0.25	0.48	0.97		
	SD card I/F	-	0.74	1.47	2.90		
	CAN	1 ch	0.06	0.08	0.16		
	CAN-FD	1 ch	0.77	1.50	2.95		
	USB	1 ch	0.48	0.95	1.89		
	Ethernet-MAC	-	1.85	3.63	7.20		
	I^2S	-	0.51	1.02	1.99		
	High-speed Quad SPI	-	0.48	0.97	1.49		
	Programmable CRC	-	0.05	0.10	0.22		
PCLK1	Base timer	4 ch	0.21	0.42	0.83	mA	
	Multi-functional timer/PPG	1 unit/4 ch	0.83	1.65	3.25		
	Quadrature position/revolution counter	1 unit	0.07	0.13	0.27		
	A/D converter	1 unit	0.31	0.60	1.17		
PCLK2	Multi-function serial	1 ch	0.41	0.81	-	mA	

12.3.2 Pin Characteristics

(V_{CC} = $USBV_{CC}0$ = $USBV_{CC}1$ = $ETHV_{CC}$ = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
H level input voltage (hysteresis input)	V_{IHS}	CMOS hysteresis input pin, MD0, MD1	-	V_{CC}×0.8	-	V_{CC} + 0.3	V	
				$ETHV_{CC}$×0.8	-	$ETHV_{CC}$ + 0.3	V	
		MADATAxx	V_{CC} > 3.0V, V_{CC} ≤ 3.6V,	2.4	-	V_{CC} + 0.3	V	At External Bus
		5V tolerant input pin	-	V_{CC}×0.8	-	V_{SS} + 5.5	V	
		Input pin doubled as I^2C Fm+	-	V_{CC}×0.7	-	V_{SS} + 5.5	V	
		TTL Schmitt input pin	-	2.0	-	$ETHV_{CC}$+0.3	V	
L level input voltage (hysteresis input)	V_{ILS}	CMOS hysteresis input pin, MD0, MD1	-	V_{SS} - 0.3	-	V_{CC}×0.2	V	
				V_{SS} - 0.3	-	$ETHV_{CC}$×0.2	V	
		5V tolerant input pin	-	V_{SS} - 0.3	-	V_{CC}×0.2	V	
		Input pin doubled as I^2C Fm+	-	V_{SS}	-	V_{CC}×0.3	V	
		TTL Schmitt input pin	-	V_{SS} - 0.3	-	0.8	V	
H level output voltage	V_{OH}	4 mA type	V_{CC} ≥ 4.5V, I_{OH} = - 4 mA	V_{CC} - 0.5	-	V_{CC}	V	
			V_{CC} < 4.5V, I_{OH} = - 2 mA					
			$ETHV_{CC}$ ≥ 4.5V, I_{OH} = - 4 mA	V_{CC} - 0.5	-	$ETHV_{CC}$	V	
			$ETHV_{CC}$ < 4.5V, I_{OH} = - 2 mA					
		8 mA type	V_{CC} ≥ 4.5V, I_{OH} = - 8 mA	V_{CC} - 0.5	-	V_{CC}	V	
			V_{CC} < 4.5V, I_{OH} = - 4 mA					
			$ETHV_{CC}$ ≥ 4.5V, I_{OH} = - 8 mA	$ETHV_{CC}$ - 0.5	-	$ETHV_{CC}$	V	
			$ETHV_{CC}$ < 4.5V, I_{OH} = - 4 mA					
		10 mA type	V_{CC} ≥ 4.5V, I_{OH} = - 10 mA	V_{CC} - 0.5	-	V_{CC}	V	
			V_{CC} < 4.5V, I_{OH} = - 8 mA					
		12 mA type	V_{CC} ≥ 4.5V, I_{OH} = - 12 mA	V_{CC} - 0.5	-	V_{CC}	V	
			V_{CC} < 4.5V, I_{OH} = - 8 mA					
		The pin doubled as USB I/O	$USBV_{CC}$ ≥ 4.5V, I_{OH} = - 20.5 mA	$USBV_{CC}$ - 0.4	-	$USBV_{CC}$	V	$USBV_{CC0}$ and $USBV_{CC1}$ are described as $USBV_{CC}$.
			$USBV_{CC}$ < 4.5V, I_{OH} = - 13.0 mA					
		The pin doubled as I^2C Fm+	V_{CC} ≥ 4.5V, I_{OH} = - 4 mA	V_{CC} - 0.5	-	V_{CC}	V	At GPIO
			V_{CC} < 4.5V, I_{OH} = - 3 mA					

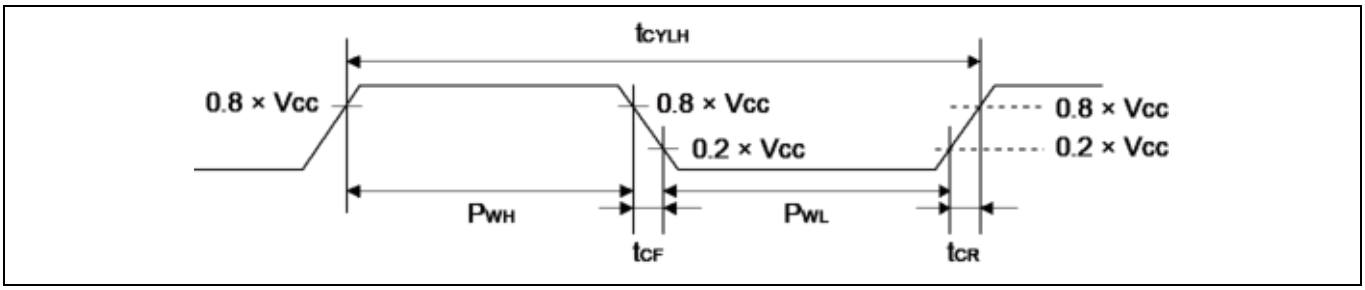
Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
L level output voltage	V_{OL}	4 mA type	$V_{CC} \geq 4.5V$, I_{OL} = 4 mA	V_{SS}	-	0.4	V	
			$V_{CC} < 4.5V$, I_{OL} = 2 mA					
			$ETHV_{CC} \geq 4.5V$, I_{OL} = 4 mA	V_{SS}	-	0.4	V	
			$RTHV_{CC} < 4.5V$, I_{OL} = 2 mA					
		8 mA type	$V_{CC} \geq 4.5V$, I_{OL} = 8 mA	V_{SS}	-	0.4	V	
			$V_{CC} < 4.5V$, I_{OL} = 4 mA					
			$ETHV_{CC} \geq 4.5V$, I_{OL} = 8 mA	V_{SS}	-	0.4	V	
			$RTHV_{CC} < 4.5V$, I_{OL} = 4 mA					
		10 mA type	$V_{CC} \geq 4.5V$, I_{OL} = 10 mA	V_{SS}	-	0.4	V	
			$V_{CC} < 4.5V$, I_{OL} = 8 mA					
		12 mA type	$V_{CC} \geq 4.5V$, I_{OL} = 12 mA	V_{SS}	-	0.4	V	
			$V_{CC} < 4.5V$, I_{OL} = 8 mA					
		The pin doubled as USB I/O	$USBV_{CC} \geq 4.5V$, I_{OL} = 18.5 mA	V_{SS}	-	0.4	V	$USBV_{CC0}$ and $USBV_{CC1}$ are described as $USBV_{CC}$.
			$USBV_{CC} < 4.5V$, I_{OL} = 10.5 mA					
		The pin doubled as I^2C Fm+	$V_{CC} \geq 4.5V$, I_{OL} = 4 mA	V_{SS}	-	0.4	V	At GPIO
			$V_{CC} < 4.5V$, I_{OL} = 3 mA					
			$V_{CC} \leq 4.5V$, I_{OL} = 20 mA					At I2C Fm+
Input leak current	I_{IL}	-	-	- 5	-	+ 5	µA	
Pull-up resistor value	R_{PU}	Pull-up pin	$V_{CC} \geq 4.5V$	25	50	100	kΩ	
			$V_{CC} < 4.5V$	30	80	200		
Input capacitance	C_{IN}	Other than VCC, USBVCC0, USBVCC1, ETHVCC, VBAT, VSS, AVCC, AVSS, AVRH	-	-	5	15	pF	

12.4 AC Characteristics

12.4.1 Main Clock Input Characteristics

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = -40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input frequency	f_{CH}	X0, X1	V_{CC} ≥4.5V	4	48	MHz	When crystal oscillator is connected
			V_{CC} < 4.5V	4	20		
			V_{CC} ≥4.5V	4	48	MHz	When using external clock
			V_{CC} < 4.5V	4	20		
Input clock cycle	t_{CYLH}		V_{CC} ≥4.5V	20.83	250	ns	When using external clock
			V_{CC} < 4.5V	50	250		
Input clock pulse width	-		P_{WH}/t_{CYLH}, P_{WL}/t_{CYLH}	45	55	%	When using external clock
Input clock rise time and fall time	t_{CF}, t_{CR}		-	-	5	ns	When using external clock
Internal operating clock [79] frequency	f_{CC}	-	-	-	200	MHz	Base clock (HCLK/FCLK)
	f_{CP0}	-	-	-	100	MHz	APB0bus clock [80]
	f_{CP1}	-	-	-	200	MHz	APB1bus clock[80]
	f_{CP2}	-	-	-	100	MHz	APB2bus clock [80]
Internal operating clock[79] cycle time	t_{CYCC}	-	-	5	-	ns	Base clock (HCLK/FCLK)
	t_{CYCP0}	-	-	10	-	ns	APB0bus clock [80]
	t_{CYCP1}	-	-	5	-	ns	APB1bus clock [80]
	t_{CYCP2}	-	-	10	-	ns	APB2bus clock[80]

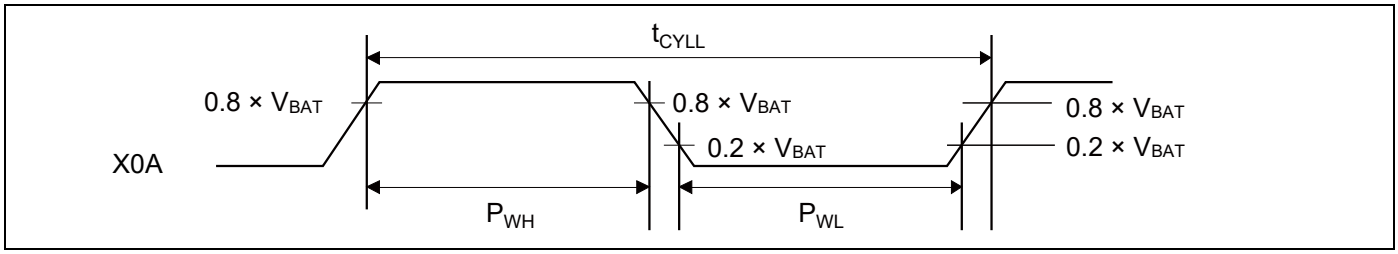


[79] For more information about each internal operating clock, see Chapter 2-1: Clock in FM4 Family Peripheral Manual Main Part (002-04856).
[80] For more about each APB bus to which each peripheral is connected, see 1. Block Diagram in this data sheet.

12.4.2 Sub Clock Input Characteristics

(V_{BAT} = 1.65V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input frequency	$1/t_{CYLL}$	X0A, X1A	-	-	32.768	-	kHz	When crystal oscillator is connected[81]
			-	32	-	100	kHz	When using external clock
Input clock cycle	t_{CYLL}		-	10	-	31.25	µs	When using external clock
Input clock pulse width	-		P_{WH}/t_{CYLL}, P_{WL}/t_{CYLL}	45	-	55	%	When using external clock



12.4.3 Built-In CR Oscillation Characteristics

Built-In High-speed CR

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_{CRH}	T_J = - 20°C to + 105°C	3.92	4	4.08	MHz	When trimming[82]
		T_J = - 40°C to + 125°C	3.88	4	4.12		
		T_J = - 40°C to + 125°C	3	4	5		When not trimming
Frequency stabilization time	t_{CRWT}	-	-	-	30	µs	[83]

Built-In Low-speed CR

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Condition	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_{CRL}	-	50	100	150	kHz	

[81] For more information about crystal oscillator, see Sub crystal oscillator in 8. Handling Devices
[82] In the case of using the values in CR trimming area of flash memory at shipment for frequency/temperature trimming
[83] This is the time to stabilize the frequency of the High-speed CR clock after setting trimming value. During this period, it is able to use the High-speed CR clock as a source clock.

12.4.4 Operating Conditions of Main PLL (in the Case of Using Main Clock for Input Clock of PLL)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time[84] (lock up time)	t_{LOCK}	100	-	-	µs	
PLL input clock frequency	f_{PLLI}	4	-	16	MHz	
PLL multiplication rate	-	13	-	100	multiplier	
PLL macro oscillation clock frequency	f_{PLLO}	200	-	400	MHz	
Main PLL clock frequency[85]	f_{CLKPLL}	-	-	200	MHz	

12.4.5 Operating Conditions of USB/Ethernet PLL・I²S PLL (in the Case of Using Main Clock for Input Clock of PLL)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time[86] (lock up time)	t_{LOCK}	100	-	-	µs	
PLL input clock frequency	f_{PLLI}	4	-	16	MHz	
PLL multiplication rate	-	13	-	100	multiplier	
PLL macro oscillation clock frequency	f_{PLLO}	200	-	400	MHz	USB/Ethernet
				384	MHz	I²S
USB/Ethernet clock frequency[87]	f_{CLKPLL}	-	-	50	MHz	After the M frequency division
I²S clock frequency [88]	f_{CLKPLL}	-	-	12.288	MHz	After the M frequency division

[84] Time from when the PLL starts operating until the oscillation stabilizes
[85] For more information about Main PLL clock (CLKPLL), see Chapter 2-1: Clock in FM4 Family Peripheral Manual Main Part (002-04856).
[86] Time from when the PLL starts operating until the oscillation stabilizes
[87] For more information about USB/Ethernet clock, see Chapter 2-2: USB/Ethernet Clock Generation in FM4 Family Peripheral Manual Communication Macro Part (002-04862).
[88] For more information about I²S clock, see Chapter 7-1: I²S Clock Generation in FM4 Family Peripheral Manual Communication Macro Part (002-04862).

12.4.6 Operating Conditions of Main PLL (in the Case of Using Built-in High-Speed CR Clock for Input Clock of Main PLL)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time[89] (lock up time)	t_{LOCK}	100	-	-	µs	
PLL input clock frequency	f_{PLLI}	3.8	4	4.2	MHz	
PLL multiplication rate	-	50	-	95	multiplier	
PLL macro oscillation clock frequency	f_{PLLO}	190	-	400	MHz	
Main PLL clock frequency [90]	f_{CLKPLL}	-	-	200	MHz	

Note:

- *The High-speed CR clock (CLKHC) should be set with frequency/temperature trimming to act as the source clock of the Main PLL.*

12.4.7 Reset Input Characteristics

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Reset input time	t_{INITX}	INITX	-	500	-	ns	

[89] Time from when the PLL starts operating until the oscillation stabilizes

[90] For more information about Main PLL clock (CLKPLL), see Chapter 2-1: Clock in FM4 Family Peripheral Manual Main Part (002-04856).

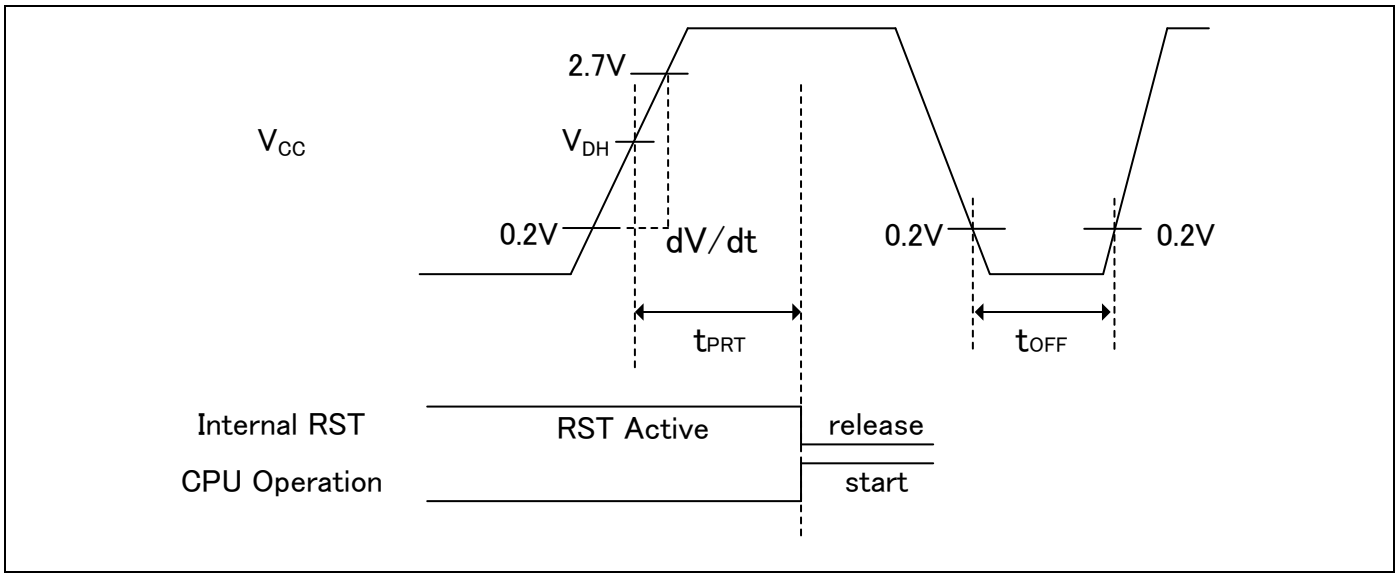
12.4.8 Power-On Reset Timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply shut down time	t_{OFF}	VCC	-	1	-	-	ms	V_{CC} must be held below 0.2V for a minimum period of t_{OFF}. Improper initialization may occur if this condition is not met
Power ramp rate	dV/dt		V_{CC}: 0.2V to 2.70V	0.6	-	1000	mV/µs	This dV/dt characteristic is applied at the power-on of cold start (t_{OFF}>1ms).
Time until releasing Power-on reset	t_{PRT}		-	0.33	-	0.60	ms	

Note:

- *If t_{OFF} cannot be satisfied designs must assert external reset(INITX) at power-up and at any brownout event per 12.4.7 Reset Input Characteristics.*



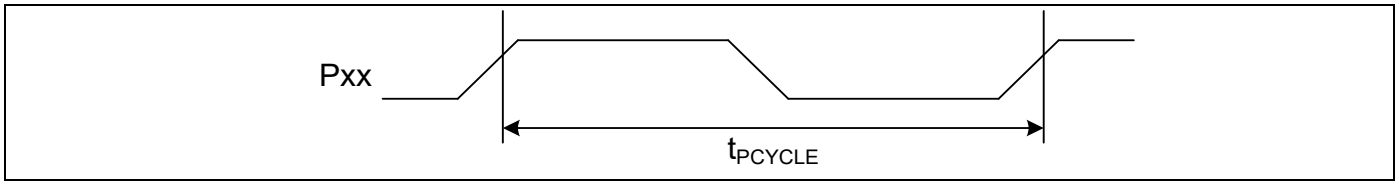
Glossary

- V_{DH}: detection voltage of Low Voltage detection reset. See “12.8. Low-Voltage Detection Characteristics”.

12.4.9 GPIO Output Characteristics

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Output frequency	t_{PCYCLE}	Pxx[91]	$V_{CC} \geq 4.5V$	-	50	MHz	
			$V_{CC} < 4.5V$	-	32	MHz	

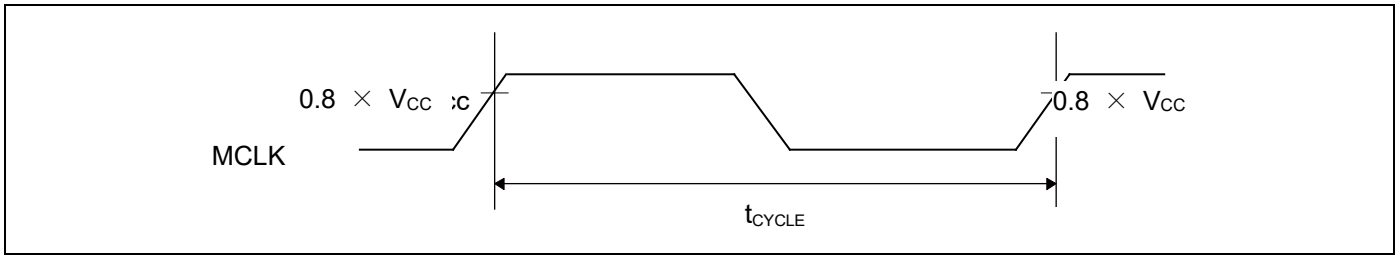


[91] GPIO is a target.

12.4.10 External Bus Timing

External Bus Clock Output Characteristics

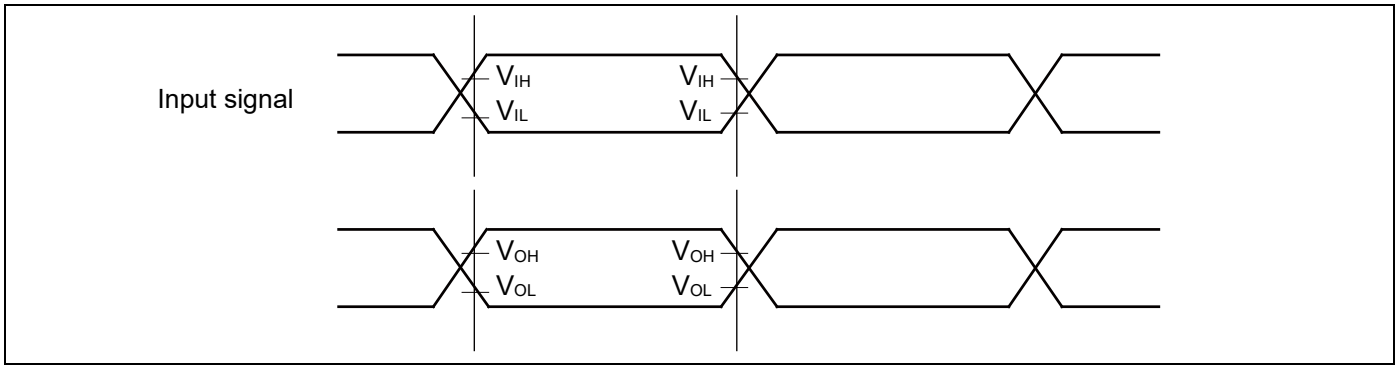
Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Output frequency	t_{CYCLE}	MCLKOUT [92]		-	50[93]	MHz	



External Bus Signal I/O Characteristics

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	Value	Unit	Remarks
Signal input characteristics	V_{IH}	-	0.8 × V_{CC}	V	
	V_{IL}		0.2 × V_{CC}	V	
Signal output characteristics	V_{OH}		0.8 × V_{CC}	V	
	V_{OL}		0.2 × V_{CC}	V	



[92] The external bus clock (MCLKOUT) is a divided clock of HCLK.
For more information about setting of clock divider, see Chapter 14: External Bus Interface in FM4 Family Peripheral Manual Main Part (002-04856).
[93] The Multi-layer AHB clock divided by the (DCLKR:MDIV) divider register, cannot exceed this specification for MCLKOUT or MSDCLK clock.

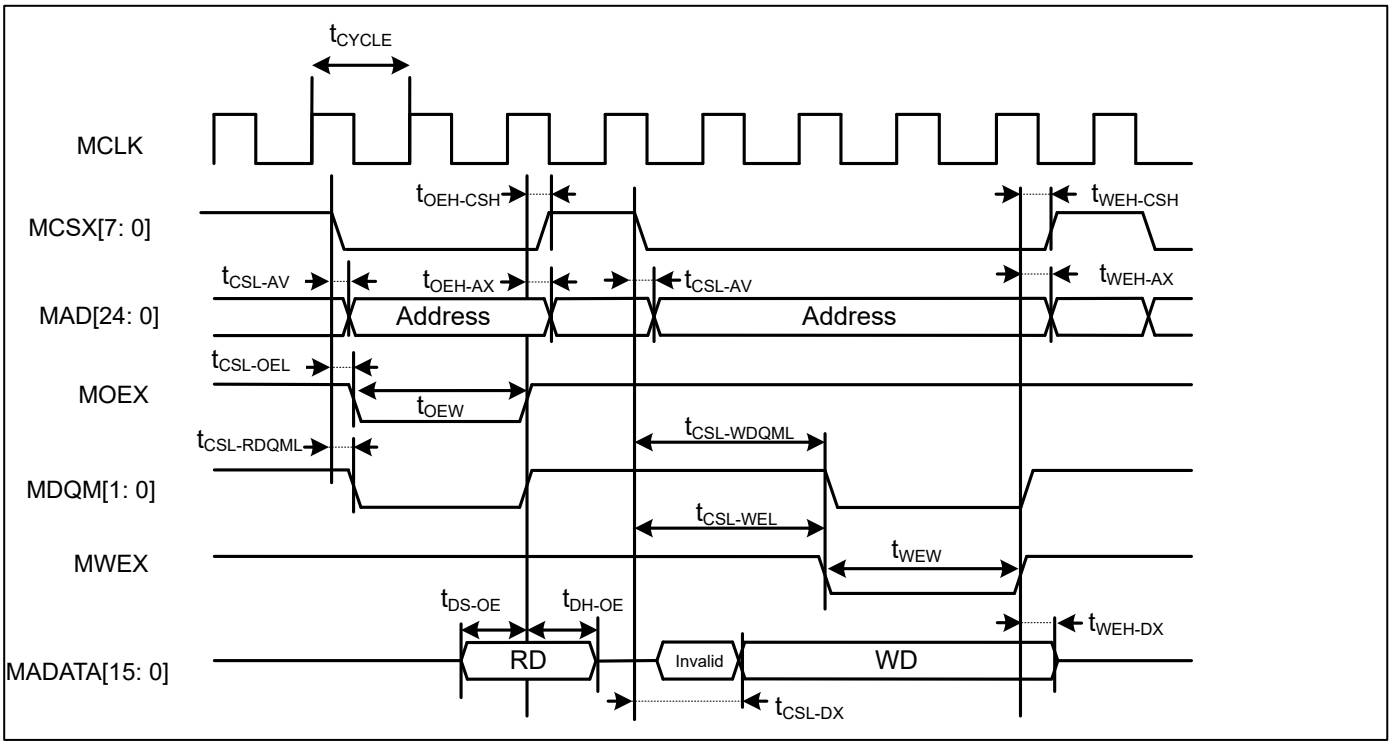
Separate Bus Access Asynchronous SRAM Mode

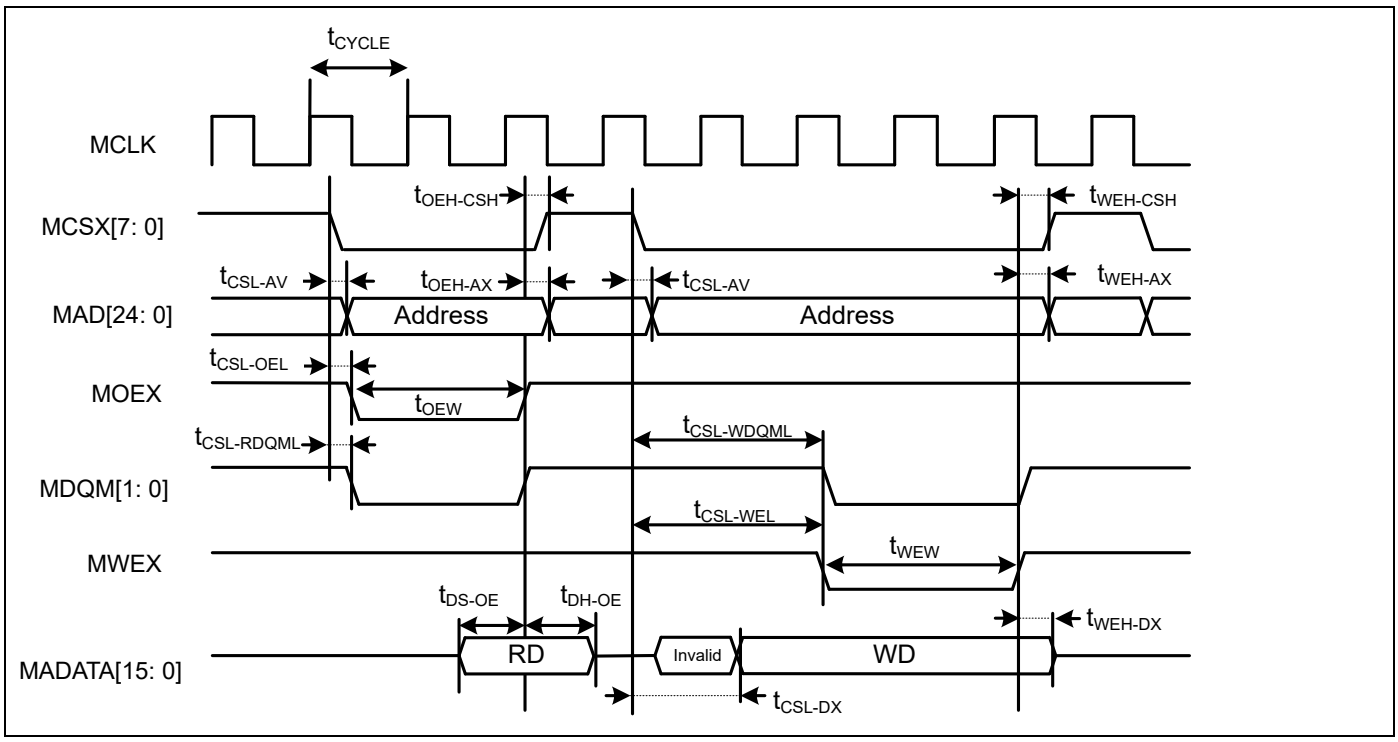
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
MOEX Minimum pulse width	t_{OEW}	MOEX	-	MCLK×n-3	-	ns	
MCSX ↓ →Address output delay time	t_{CSL-AV}	MCSX[7: 0], MAD[24: 0]	-	-9	+9	ns	
MOEX ↑ →Address hold time	t_{OEH-AX}	MOEX, MAD[24: 0]	-	0	MCLK×m+9	ns	
MCSX ↓ → MOEX ↓ delay time	$t_{CSL-OEL}$	MOEX, MCSX[7: 0]	-	MCLK×m-9	MCLK×m+9	ns	
MOEX ↑ → MCSX ↑ time	$t_{OEH-CSH}$		-	0	MCLK×m+9	ns	
MCSX ↓ → MDQM ↓ delay time	$t_{CSL-RDQML}$	MCSX, MDQM[3: 0]	-	MCLK×m-9	MCLK×m+9	ns	
Data set up→MOEX ↑ time	t_{DS-OE}	MOEX, MADATA[31: 0]	-	20	-	ns	
MOEX ↑ → Data hold time	t_{DH-OE}	MOEX, MADATA[31: 0]	-	0	-	ns	
MWEX Minimum pulse width	t_{WEW}	MWEX	-	MCLK×n-3	-	ns	
MWEX ↑ →Address output delay time	t_{WEH-AX}	MWEX, MAD[24: 0]	-	0	MCLK×m+9	ns	
MCSX ↓ → MWEX ↓ delay time	$t_{CSL-WEL}$	MWEX, MCSX[7: 0]	-	MCLK×n-9	MCLK×n+9	ns	
MWEX ↑ → MCSX ↑ delay time	$t_{WEH-CSH}$		-	0	MCLK×m+9	ns	
MCSX ↓ → MDQM ↓ delay time	$t_{CSL-WDQML}$	MCSX, MDQM[3: 0]	-	MCLK×n-9	MCLK×n+9	ns	
MCSX ↓ → Data output time	t_{CSL-DX}	MCSX, MADATA[31: 0]	-	MCLK-9	MCLK+9	ns	
MWEX ↑ → Data hold time	t_{WEH-DX}	MWEX, MADATA[31: 0]	-	0	MCLK×m+9	ns	

Note:

− *When the external load capacitance C_L = 30 pF (m = 0 to 15, n = 1 to 16)*


tCYCLE
MCLK
MCSX[7: 0]
MAD[24: 0]
MOEX
MDQM[1: 0]
MWEX
MADATA[15: 0]
tOEH-CSH
tWEH-CSH
tCSL-AV
tOEH-AX
tCSL-AV
tWEH-AX
Address
Address
tCSL-OEL
tOEW
tCSL-RDQML
tCSL-WDQML
tCSL-WEL
tWEW
tDS-OE
tDH-OE
tWEH-DX
RD
Invalid
WD
tCSL-DX


tCYCLE
MCLK
MCSX[7: 0]
MAD[24: 0]
MOEX
MDQM[1: 0]
MWEX
MADATA[15: 0]
tOEH-CSH
tWEH-CSH
tCSL-AV
tOEH-AX
tCSL-AV
tWEH-AX
Address
Address
tCSL-OEL
tOEW
tCSL-RDQML
tCSL-WDQML
tCSL-WEL
tWEW
tDS-OE
tDH-OE
tWEH-DX
RD
Invalid
WD
tCSL-DX

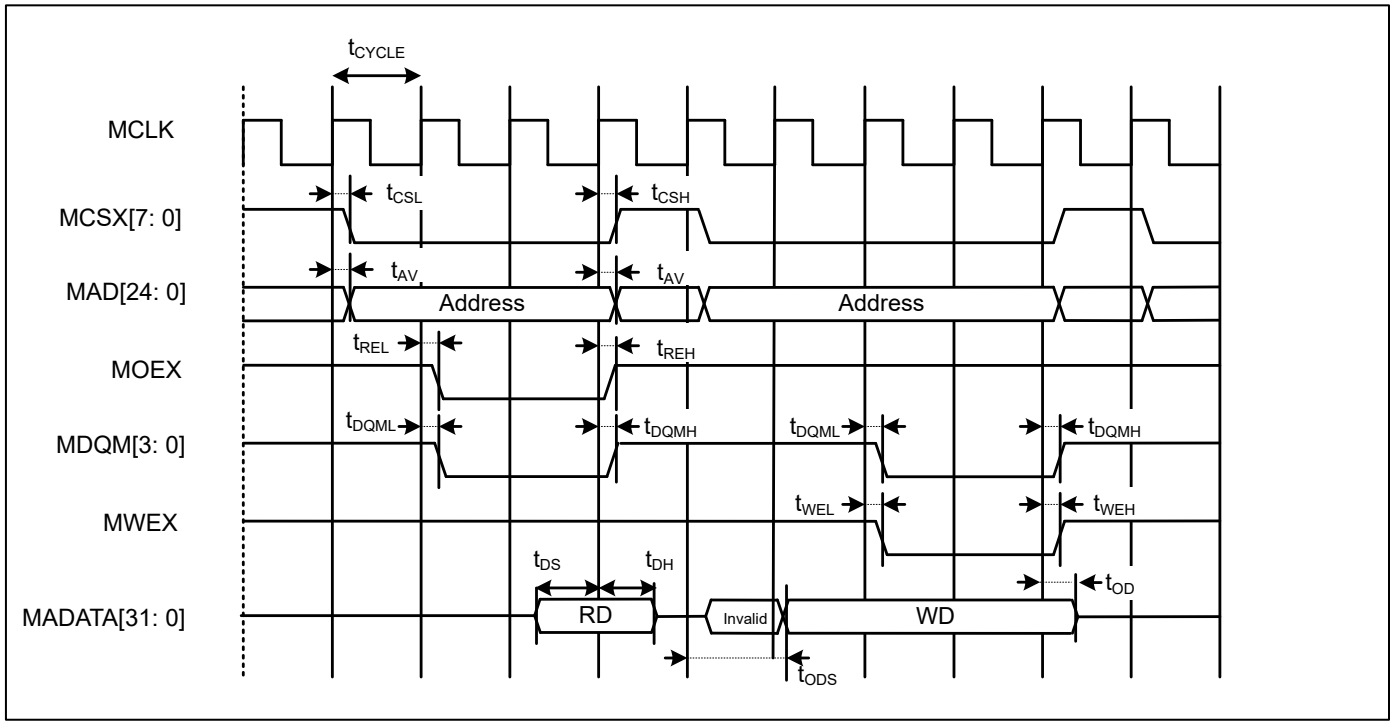
Separate Bus Access Synchronous SRAM Mode

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Address delay time	t_{AV}	MCLK, MAD[24: 0]	-	1	9	ns	
MCSX delay time	t_{CSL}	MCLK, MCSX[7: 0]	-	1	9	ns	
	t_{CSH}		-	1	9	ns	
MOEX delay time	t_{REL}	MCLK, MOEX	-	1	9	ns	
	t_{REH}		-	1	9	ns	
Data set up →MCLK ↑ time	t_{DS}	MCLK, MADATA[31: 0]	-	19	-	ns	
MCLK ↑ → Data hold time	t_{DH}	MCLK, MADATA[31: 0]	-	0	-	ns	
MWEX delay time	t_{WEL}	MCLK, MWEX	-	1	9	ns	
	t_{WEH}		-	1	9	ns	
MDQM[1: 0] delay time	t_{DQML}	MCLK, MDQM[3: 0]	-	1	9	ns	
	t_{DQMH}		-	1	9	ns	
MCLK ↑ → Data output time	t_{ODS}	MCLK, MADATA[31: 0]	-	MCLK+1	MCLK+18	ns	
MCLK ↑ → Data hold time	t_{OD}	MCLK, MADATA[31: 0]	-	1	18	ns	

Note:

− *When the external load capacitance CL = 30 pF*



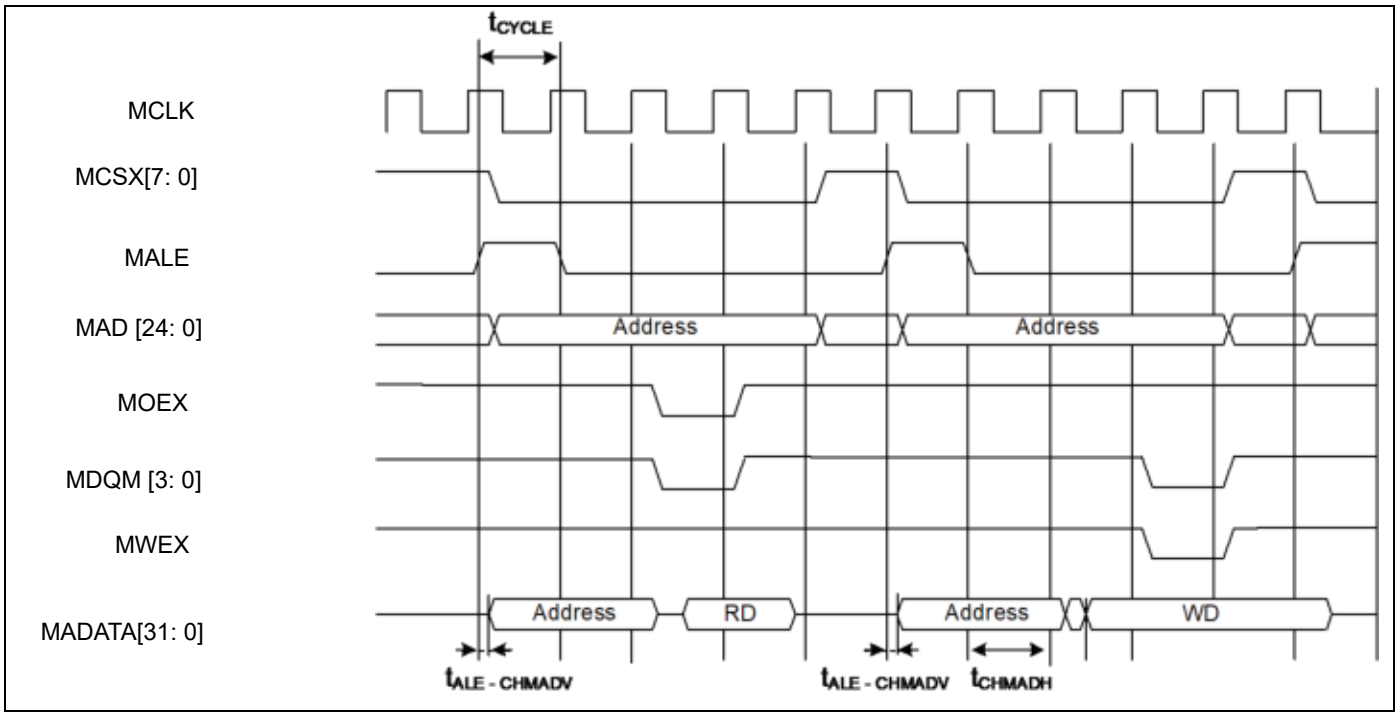
Multiplexed Bus Access Asynchronous SRAM Mode

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Multiplexed address delay time	$t_{ALE-CHMADV}$	MALE, MAD[24: 0]	-	0	10	ns	
Multiplexed address hold time	t_{CHMADH}		-	MCLK×n+0	MCLK×n+10	ns	

Note:

– *When the external load capacitance C_L = 30 pF (m = 0 to 15, n = 1 to 16)*



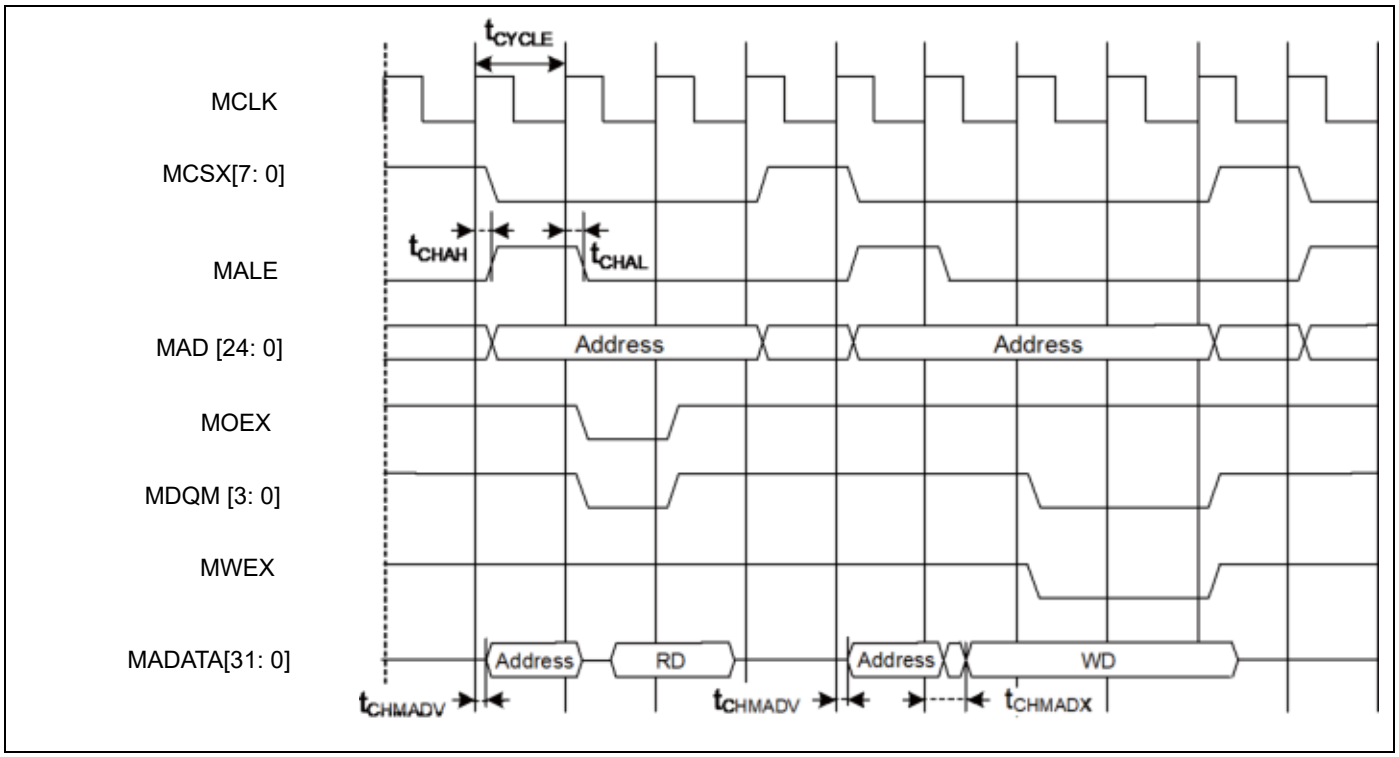
Multiplexed Bus Access Synchronous SRAM Mode

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
MALE delay time	t_{CHAL}	MCLK, MALE	-	1	9		
	t_{CHAH}		-	1	9		
MCLK ↑ →Multiplexed address delay time	t_{CHMADV}	MCLK, MADATA[31: 0]	-	1	t_{OD}	ns	
MCLK ↑ →Multiplexed data output time	t_{CHMADX}		-	1	t_{OD}	ns	

Note:

- *When the external load capacitance C_L = 30 pF*



NAND Flash Mode

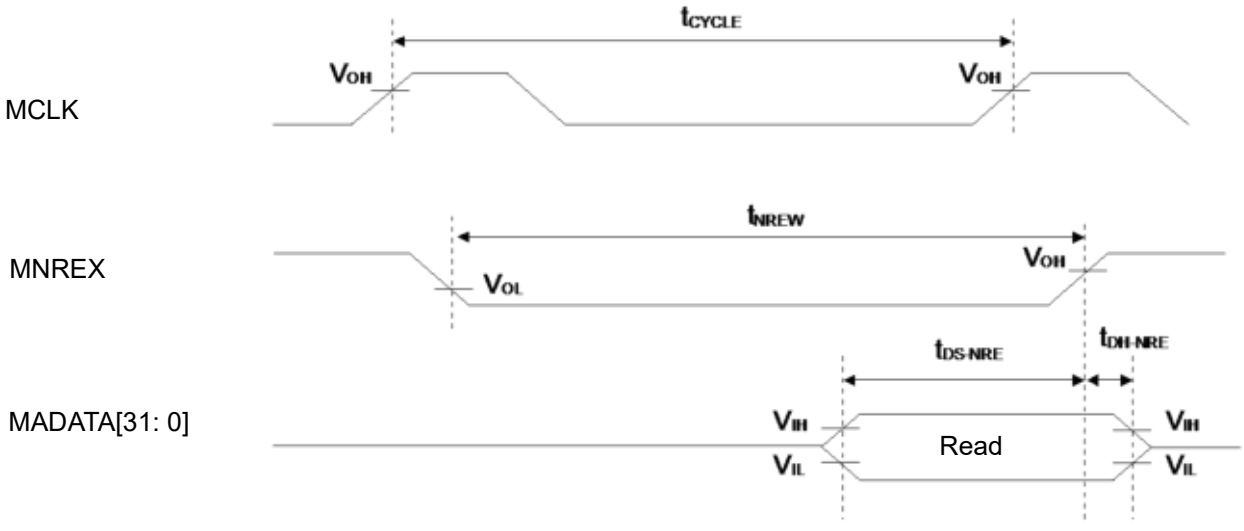
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
MNREX Min pulse width	t_{NREW}	MNREX	-	MCLK×n-3	-	ns	
Data set up →MNREX ↑ time	t_{DS-NRE}	MNREX, MADATA[31: 0]	-	20	-	ns	
MNREX ↑ → Data hold time	t_{DH-NRE}	MNREX, MADATA[31: 0]	-	0	-	ns	
MNALE ↑ → MNWEX delay time	$t_{ALEH-NWEL}$	MNALE, MNWEX	-	MCLK×m-9	MCLK×m+9	ns	
MNALE ↓ → MNWEX delay time	$t_{ALEL-NWEL}$	MNALE, MNWEX	-	MCLK×m-9	MCLK×m+9	ns	
MNCLE ↑ → MNWEX delay time	$t_{CLEH-NWEL}$	MNCLE, MNWEX	-	MCLK×m-9	MCLK×m+9	ns	
MNWEX ↑ → MNCLE delay time	$t_{NWEH-CLEL}$	MNCLE, MNWEX	-	0	MCLK×m+9	ns	
MNWEX Min pulse width	t_{NWEW}	MNWEX	-	MCLK×n-3	-	ns	
MNWEX ↓ → Data output time	$t_{NWEL-DV}$	MNWEX, MADATA[31: 0]	-	-9	9	ns	
MNWEX ↑ → Data hold time	$t_{NWEH-DX}$	MNWEX, MADATA[31: 0]	-	0	MCLK×m+9	ns	

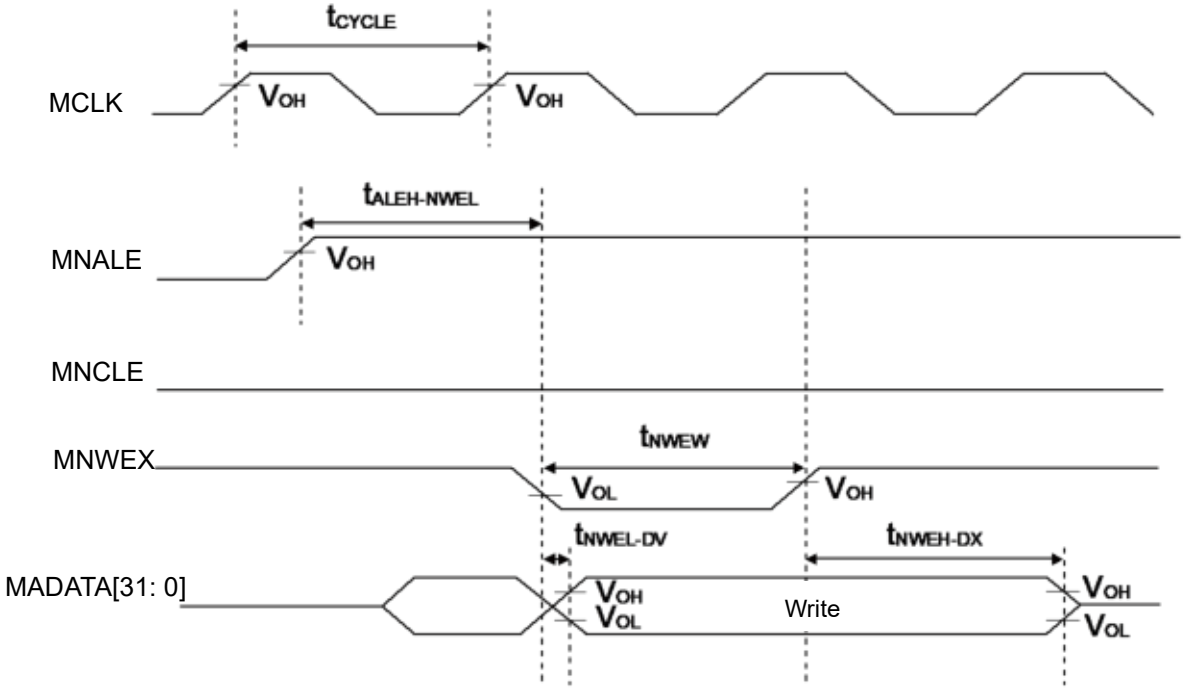
Note:

- *When the external load capacitance C_L = 30 pF (m = 0 to 15, n = 1 to 16)*

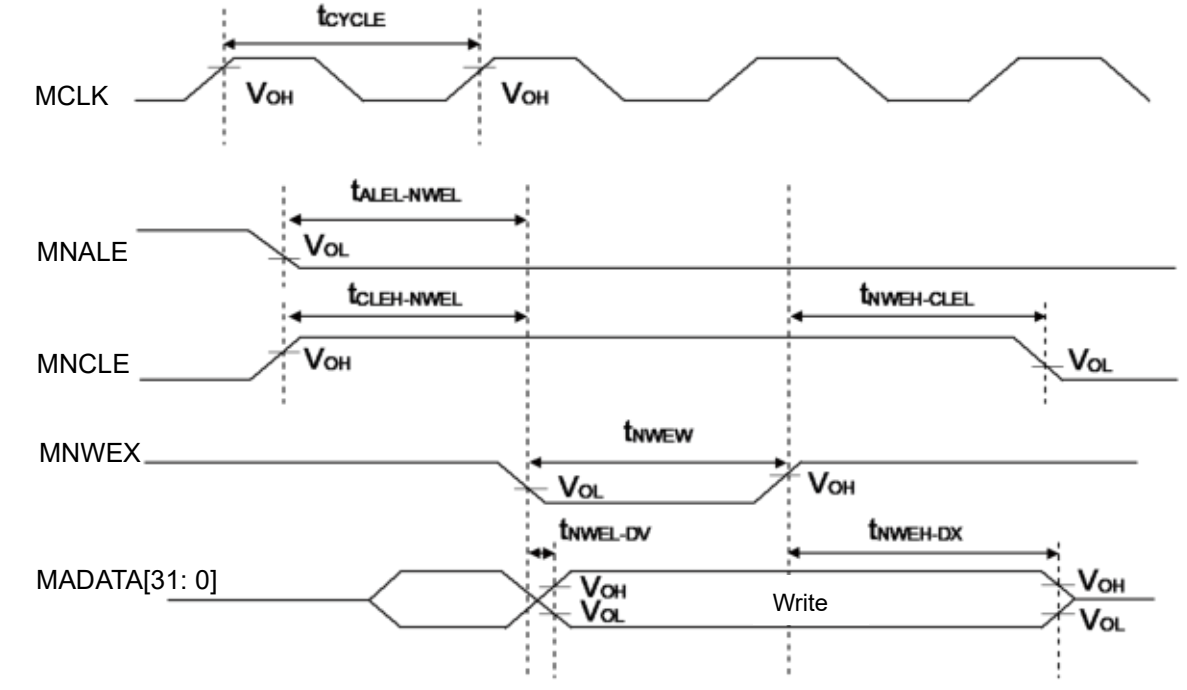
NAND Flash Read



NAND Flash Address Write



NAND Flash Command Write

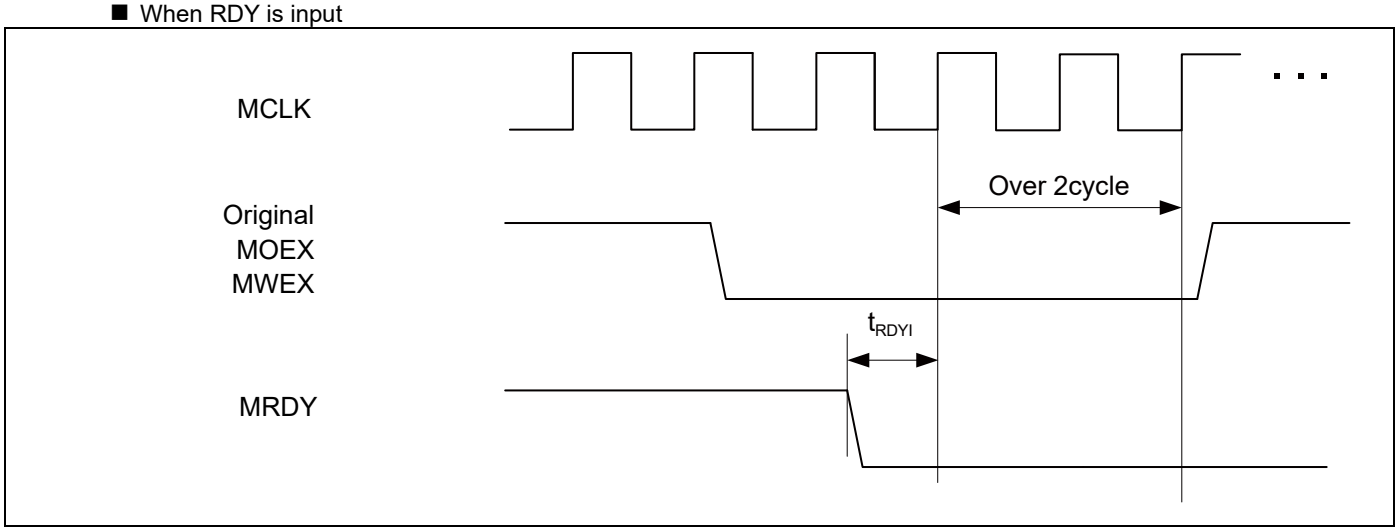


External Ready Input Timing

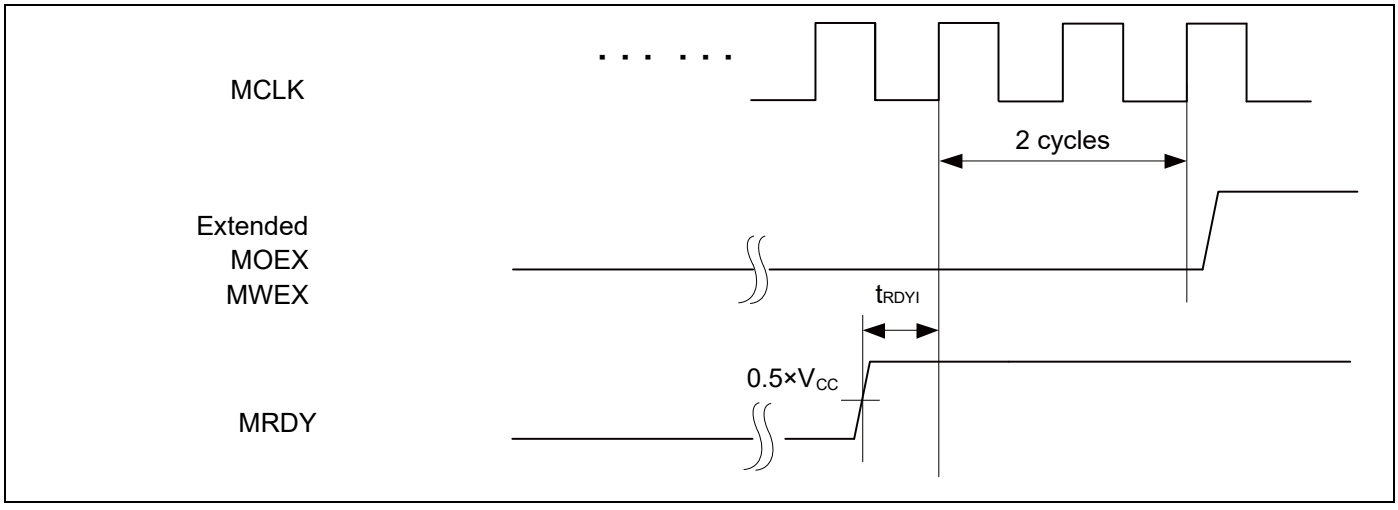
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
MCLK↑ MRDY input setup time	t_{RDYI}	MCLK, MRDY	-	19	-	ns	

■ When RDY is input



■ When RDY is released



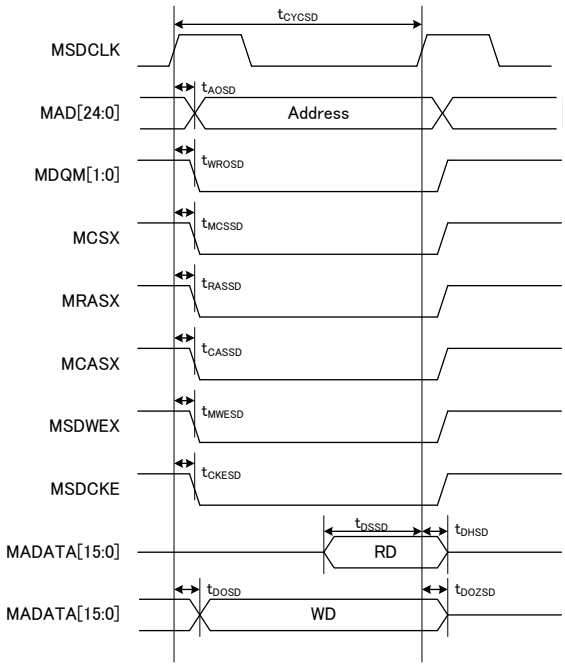
SDRAM Mode

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Value	Unit		Unit	Remarks
				Min	Max		
Output frequency	t_{CYCSD}	MSDCLK	-	-	50	MHz	
Address delay time	t_{AOSD}	MSDCLK, MAD[15: 0]	-	2	12	ns	
MSDCLK ↑ → Data output delay time	t_{DOSD}	MSDCLK, MADATA[31: 0]	-	2	12	ns	
MSDCLK ↑ → Data output Hi-Z time	t_{DOZSD}	MSDCLK, MADATA[31: 0]	-	2	19.5	ns	
MDQM[3: 0] delay time	t_{WROSD}	MSDCLK, MDQM[1: 0]	-	1	12	ns	
MCSX delay time	t_{MCSSD}	MSDCLK, MCSX8	-	2	12	ns	
MRASX delay time	t_{RASSD}	MSDCLK, MRASX	-	2	12	ns	
MCASX delay time	t_{CASSD}	MSDCLK, MCASX	-	2	12	ns	
MSDWEX delay time	t_{MWESD}	MSDCLK, MSDWEX	-	2	12	ns	
MSDCKE delay time	t_{CKESD}	MSDCLK, MSDCKE	-	2	12	ns	
Data set up time	t_{DSSD}	MSDCLK, MADATA[31: 0]	-	19	-	ns	
Data hold time	t_{DHSD}	MSDCLK, MADATA[31: 0]	-	0	-	ns	

Note:

- *When the external load capacitance C_L = 30 pF*

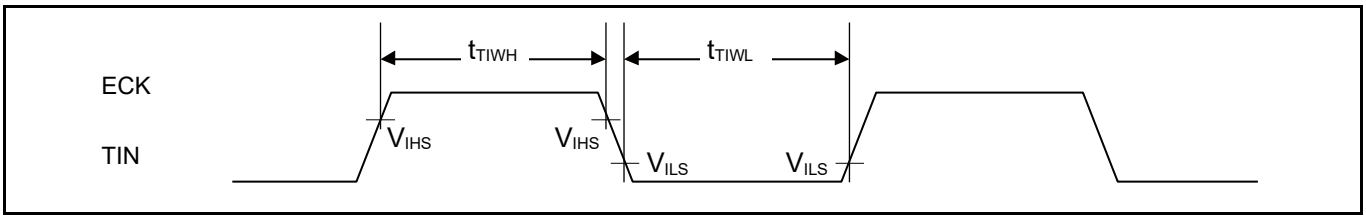


12.4.11 Base Timer Input Timing

Timer Input Timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

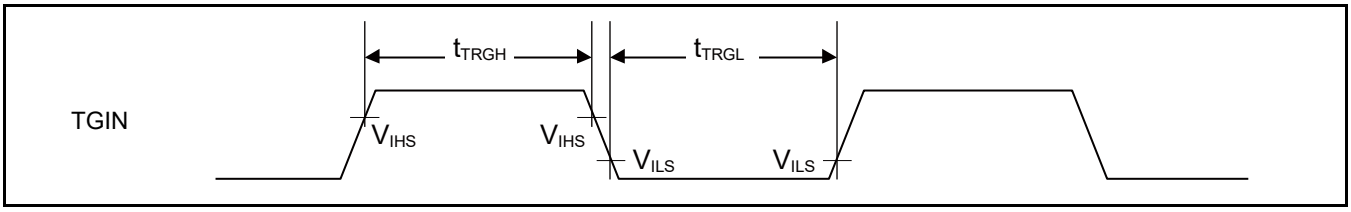
Parameter	Symbol	Pin Name	Value		Unit	Remarks
			Min	Max		
Input pulse width	t_{TIWH}, t_{TIWL}	TIOAn/TIOBn (when using as ECK, TIN)	$2t_{CYCP}$	-	ns	



Trigger Input Timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Value		Unit	Remarks
			Min	Max		
Input pulse width	t_{TRGH}, t_{TRGL}	TIOAn/TIOBn (when using as TGIN)	$2t_{CYCP}$	-	ns	



Note:

- *t_{CYCP} indicates the APB bus clock cycle time. For more information about the APB bus number to which the base timer is connected, see 1. Block Diagram in this datasheet.*

12.4.12 CSIO (SPI) Timing

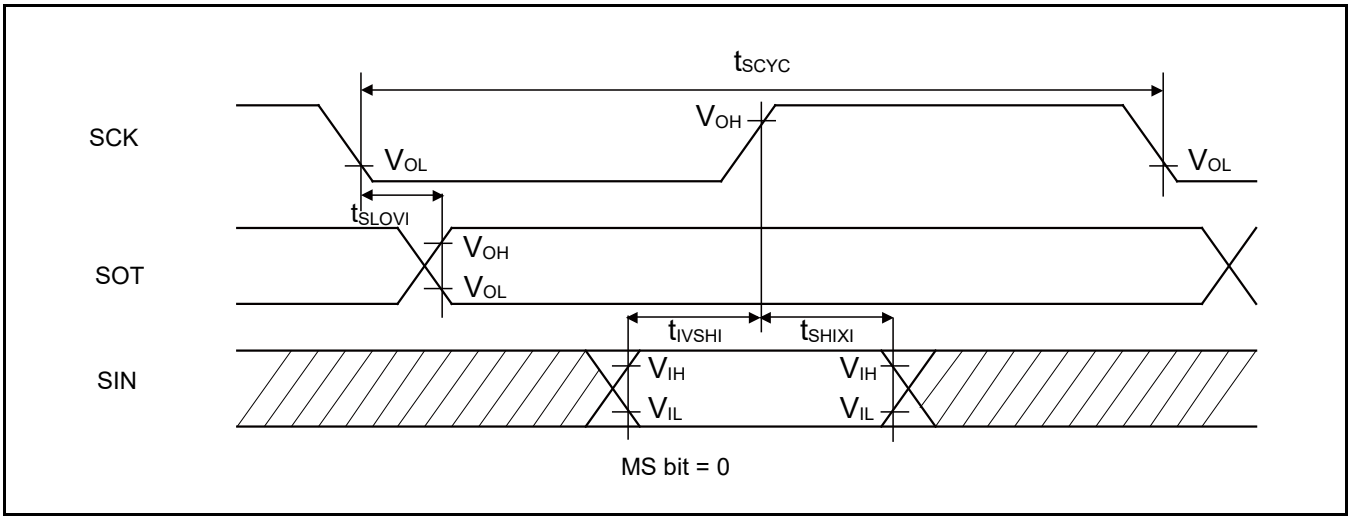
Synchronous Serial (SPI = 0, SCINV = 0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

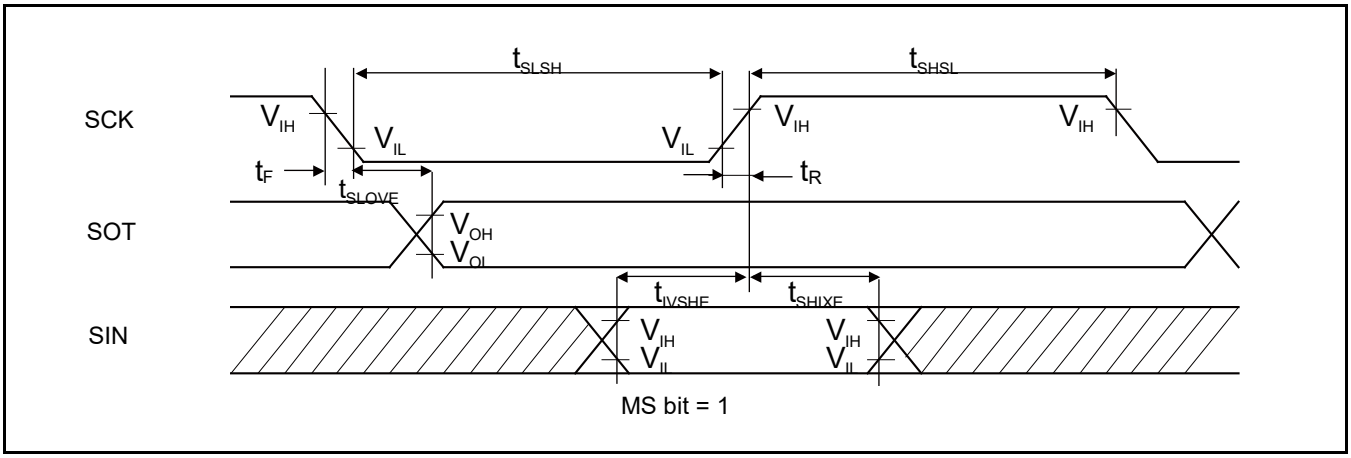
Parameter	Symbol	Pin Name	Conditions	V_{CC} < 4.5V		V_{CC} ≥ 4.5V		Unit
				Min	Max	Min	Max	
Baud rate	-	-		-	8	-	8	Mbps
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK↓→SOT delay time	t_{SLOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN→SCK↑ setup time	t_{IVSHI}	SCKx, SINx		50	-	30	-	ns
SCK↑→SIN hold time	t_{SHIXI}	SCKx, SINx		0	-	0	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK↓→SOT delay time	t_{SLOVE}	SCKx, SOTx		-	50	-	30	ns
SIN→SCK↑ setup time	t_{IVSHE}	SCKx, SINx		10	-	10	-	ns
SCK↑→SIN hold time	t_{SHIXE}	SCKx, SINx		20	-	20	-	ns
SCK fall time	t_F	SCKx		-	5	-	5	ns
SCK rise time	t_R	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 1. Block Diagram in this datasheet.*
- *These characteristics only guarantee the same relocate port number; for example, the combination of SCLKx_0 and SOTx_1 is not guaranteed.*



MS bit = 0



MS bit = 1

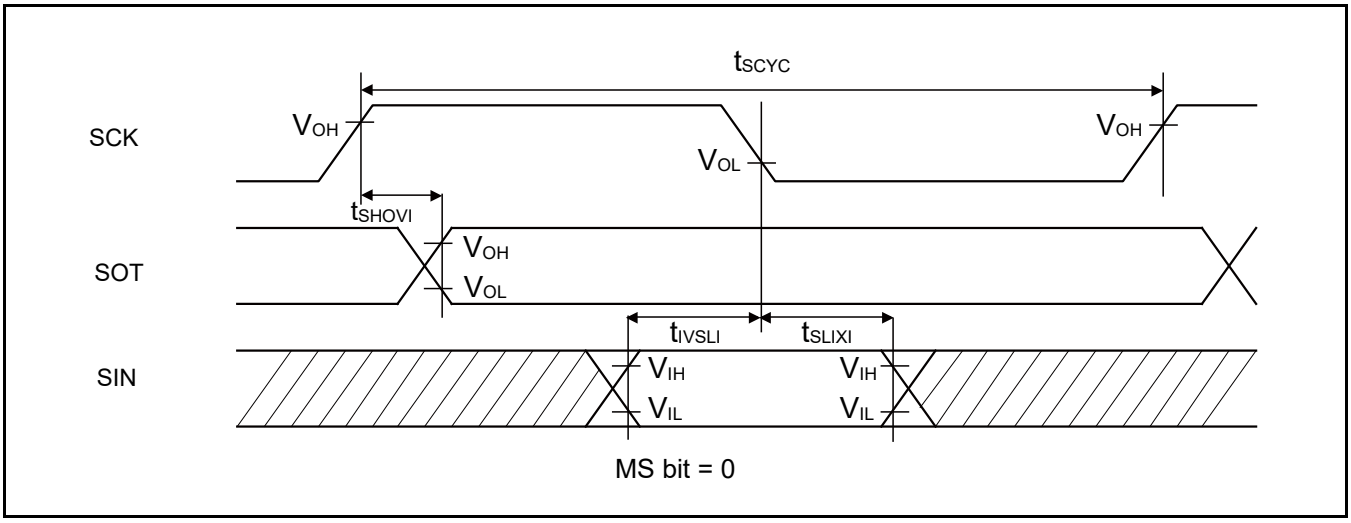
Synchronous Serial (SPI = 0, SCINV = 1)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

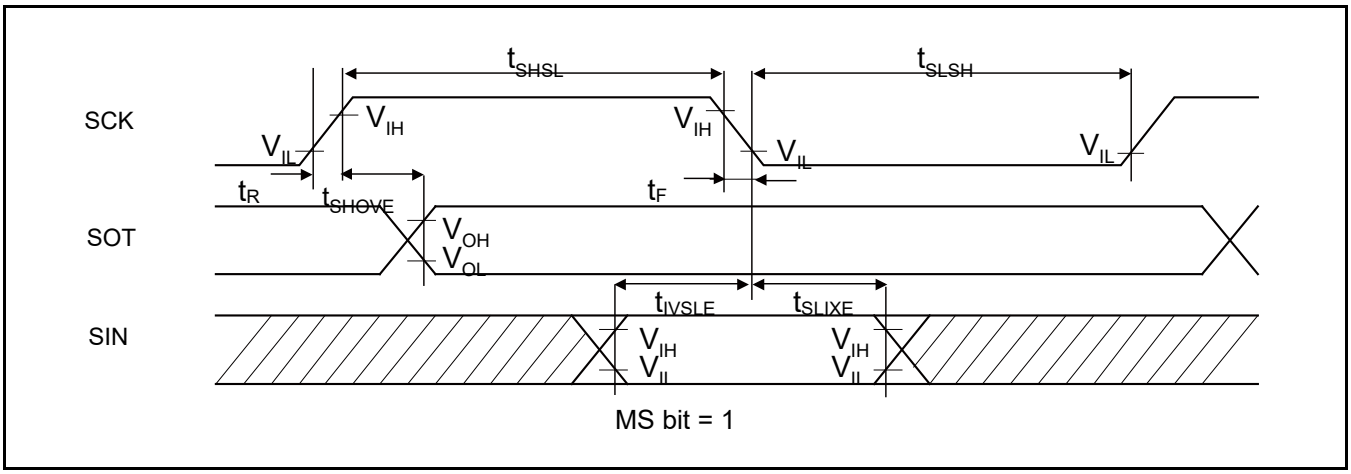
Parameter	Symbol	Pin Name	Conditions	V_{CC} < 4.5V		V_{CC} ≥ 4.5V		Unit
				Min	Max	Min	Max	
Baud rate	-	-	-	-	8	-	8	Mbps
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK↑→SOT delay time	t_{SHOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN→SCK↓ setup time	t_{IVSLI}	SCKx, SINx		50	-	30	-	ns
SCK↓→SIN hold time	t_{SLIXI}	SCKx, SINx		0	-	0	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK↑→SOT delay time	t_{SHOVE}	SCKx, SOTx		-	50	-	30	ns
SIN→SCK↓ setup time	t_{IVSLE}	SCKx, SINx		10	-	10	-	ns
SCK↓→SIN hold time	t_{SLIXE}	SCKx, SINx		20	-	20	-	ns
SCK fall time	t_F	SCKx		-	5	-	5	ns
SCK rise time	t_R	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 1. Block Diagram in this datasheet.*
- *These characteristics only guarantee the same relocate port number; for example, the combination of SCKx_0 and SOTx_1 is not guaranteed.*
- *When the external load capacitance C_L = 30 pF.*



MS bit = 0



MS bit = 1

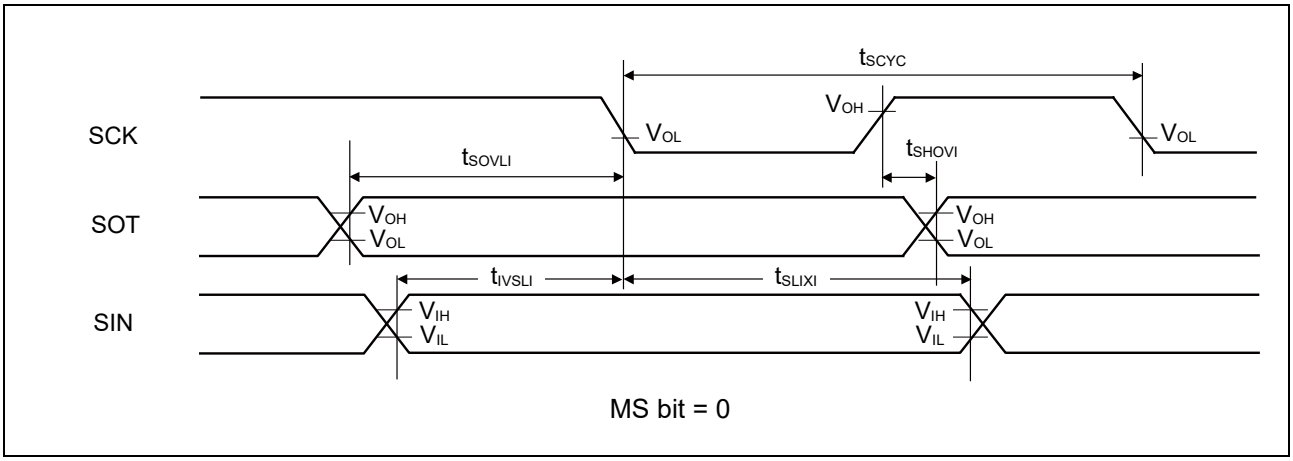
Synchronous Serial (SPI = 1, SCINV = 0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

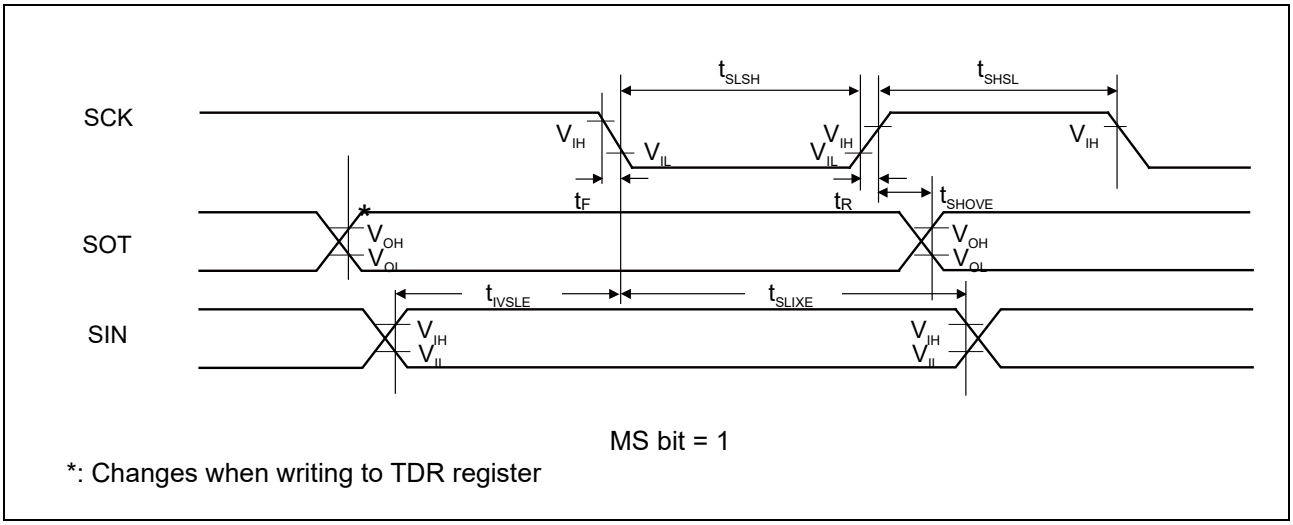
Parameter	Symbol	Pin Name	Conditions	V_{CC} < 4.5V		V_{CC} ≥ 4.5V		Unit
				Min	Max	Min	Max	
Baud rate	-	-	-	-	8	-	8	Mbps
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK↑→SOT delay time	t_{SHOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN→SCK↓ setup time	t_{IVSLI}	SCKx, SINx		50	-	30	-	ns
SCK↓→SIN hold time	t_{SLIXI}	SCKx, SINx		0	-	0	-	ns
SOT→SCK↓ delay time	t_{SOVLI}	SCKx, SOTx		$2t_{CYCP}$ - 30	-	$2t_{CYCP}$ - 30	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK↑→SOT delay time	t_{SHOVE}	SCKx, SOTx		-	50	-	30	ns
SIN→SCK↓ setup time	t_{IVSLE}	SCKx, SINx		10	-	10	-	ns
SCK↓→SIN hold time	t_{SLIXE}	SCKx, SINx		20	-	20	-	ns
SCK fall time	t_F	SCKx		-	5	-	5	ns
SCK rise time	t_R	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 1. Block Diagram in this datasheet.*
- *These characteristics only guarantee the same relocate port number; for example, the combination of SCLKx_0 and SOTx_1 is not guaranteed.*
- *When the external load capacitance C_L = 30 pF.*



MS bit = 0



MS bit = 1

*: Changes when writing to TDR register

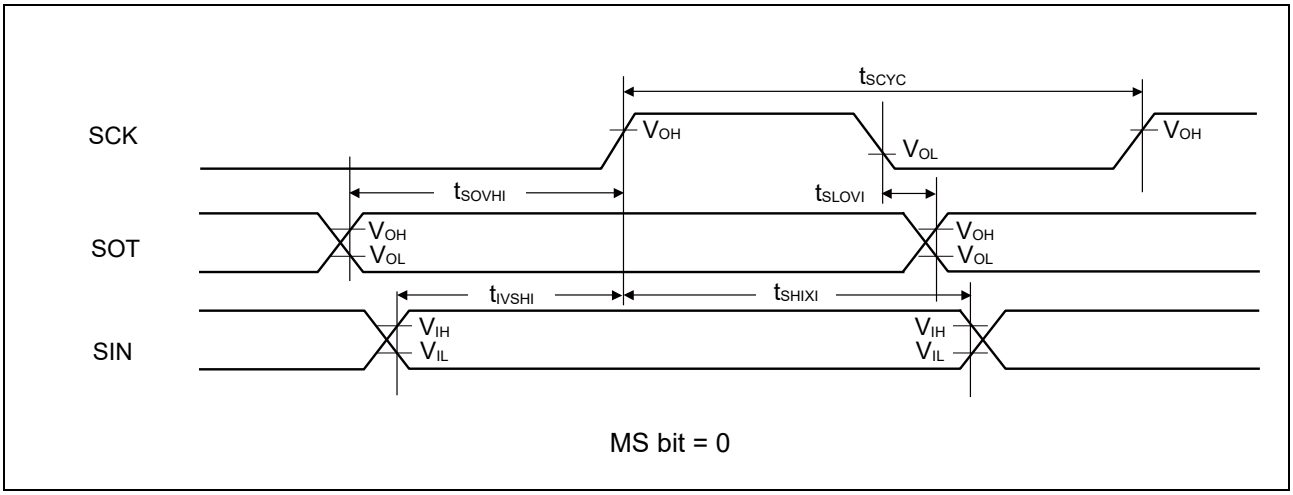
Synchronous Serial (SPI = 1, SCINV = 1)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

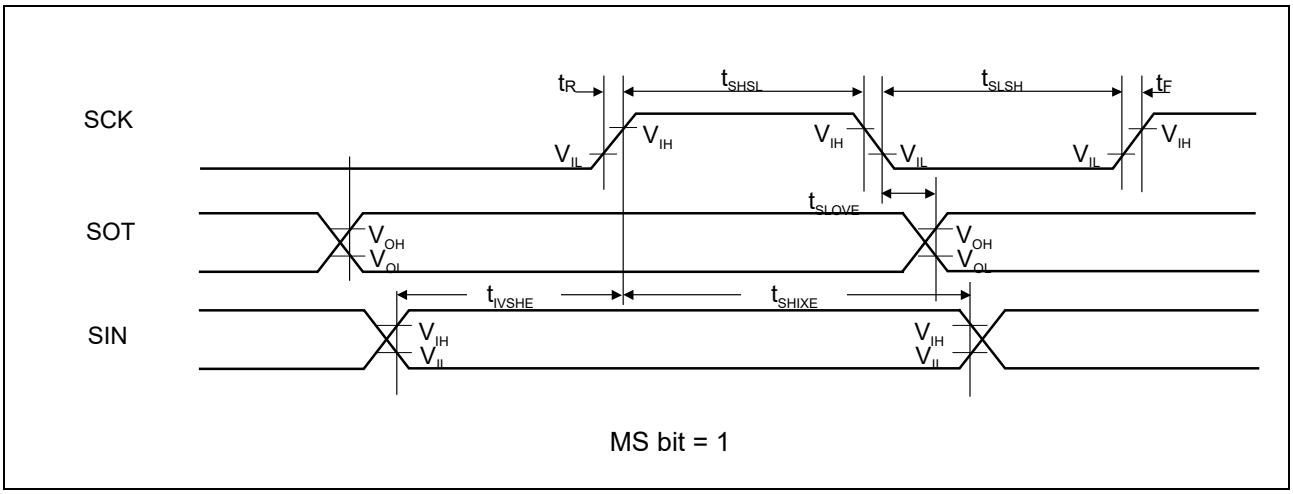
Parameter	Symbol	Pin Name	Conditions	V_{CC} < 4.5V		V_{CC} ≥ 4.5V		Unit
				Min	Max	Min	Max	
Baud rate	-	-	-	-	8	-	8	Mbps
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK↓→SOT delay time	t_{SLOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN→SCK↑ setup time	t_{IVSHI}	SCKx, SINx		50	-	30	-	ns
SCK↑→SIN hold time	t_{SHIXI}	SCKx, SINx		0	-	0	-	ns
SOT→SCK↑ delay time	t_{SOVHI}	SCKx, SOTx		$2t_{CYCP}$ - 30	-	$2t_{CYCP}$ - 30	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK↓→SOT delay time	t_{SLOVE}	SCKx, SOTx		-	50	-	30	ns
SIN→SCK↑ setup time	t_{IVSHE}	SCKx, SINx		10	-	10	-	ns
SCK↑→SIN hold time	t_{SHIXE}	SCKx, SINx		20	-	20	-	ns
SCK fall time	t_F	SCKx		-	5	-	5	ns
SCK rise time	t_R	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 1. Block Diagram in this datasheet.*
- *These characteristics only guarantee the same relocate port number; for example, the combination of SCLKx_0 and SOTx_1 is not guaranteed.*
- *When the external load capacitance C_L = 30 pF.*



MS bit = 0



MS bit = 1

When Using Synchronous Serial Chip Select (SCINV = 0, CSLVL = 1)

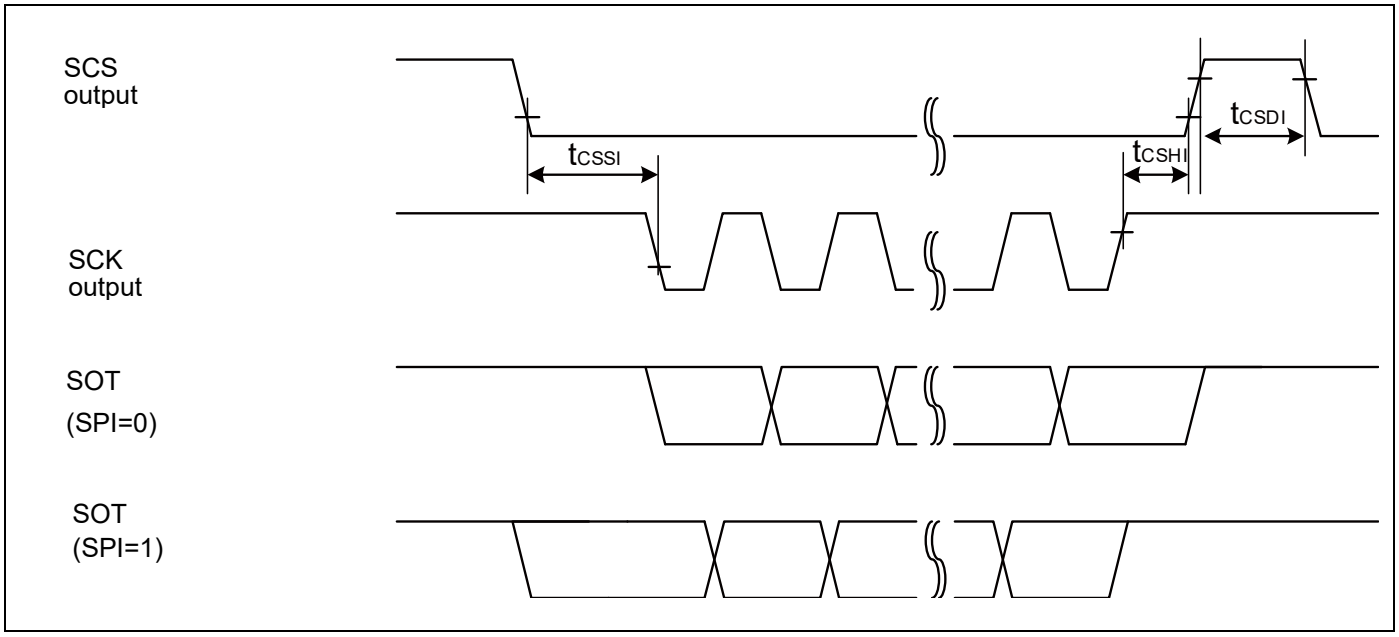
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

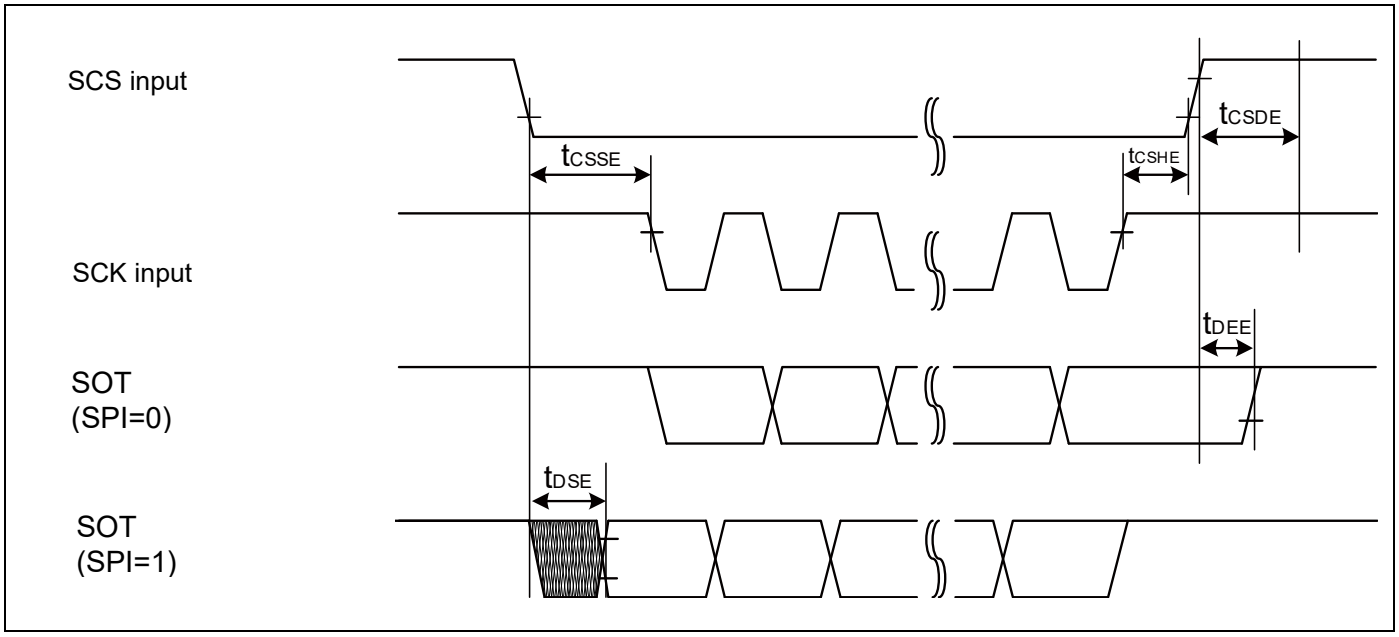
Parameter	Symbol	Conditions	V_{CC} < 4.5V		V_{CC} ≥ 4.5V		Unit
			Min	Max	Min	Max	
SCS↓→SCK↓ setup time	t_{CSSI}	Internal shift clock operation	[94]-50	[94]+0	[94]-50	[94]+0	ns
SCK↑→SCS↑ hold time	t_{CSHI}		[95]+0	[95]+50	[95]+0	[95]+50	ns
SCS deselect time	t_{CSDI}		[96]-50 +5t_{CYCP}	[96]+50 +5t_{CYCP}	[96]-50 +5t_{CYCP}	[96]+50 +5t_{CYCP}	ns
SCS↓→SCK↓ setup time	t_{CSSE}	External shift clock operation	3t_{CYCP}+30	-	3t_{CYCP}+30	-	ns
SCK↑→SCS↑ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		3t_{CYCP}+30	-	3t_{CYCP}+30	-	ns
SCS ↓ →SOT delay time	t_{DSE}		-	40	-	40	ns
SCS ↑ →SOT delay time	t_{DEE}		0	-	0	-	ns

Notes:

- *t_{CYCP} indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 1. Block Diagram in this datasheet.*
- *For more information about CSSU, CSHD, CSDS, and the serial chip select timing operating clock, see FM4 Family Peripheral Manual Main Part (002-04856).*
- *When the external load capacitance C_L = 30 pF.*

[94] CSSU bit value×serial chip select timing operating clock cycle [ns]
[95] CSHD bit value×serial chip select timing operating clock cycle [ns]
[96] CSDS bit value×serial chip select timing operating clock cycle [ns]


SCS
output
SCK
output
SOT
(SPI=0)
SOT
(SPI=1)
tCSSI
tCSDI
tCSHI


SCS input
SCK input
SOT
(SPI=0)
SOT
(SPI=1)
tCSSE
tCSDE
tCSHE
tDEE
tDSE

When Using Synchronous Serial Chip Select (SCINV = 1, CSLVL = 1)

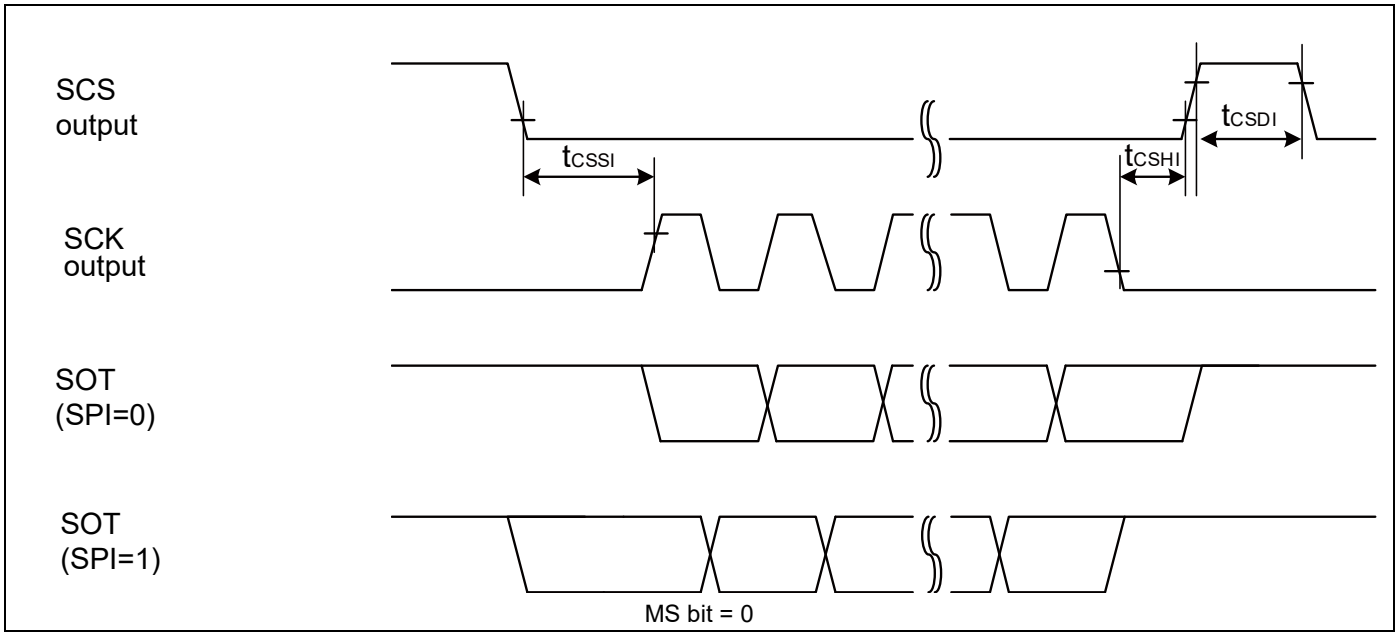
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

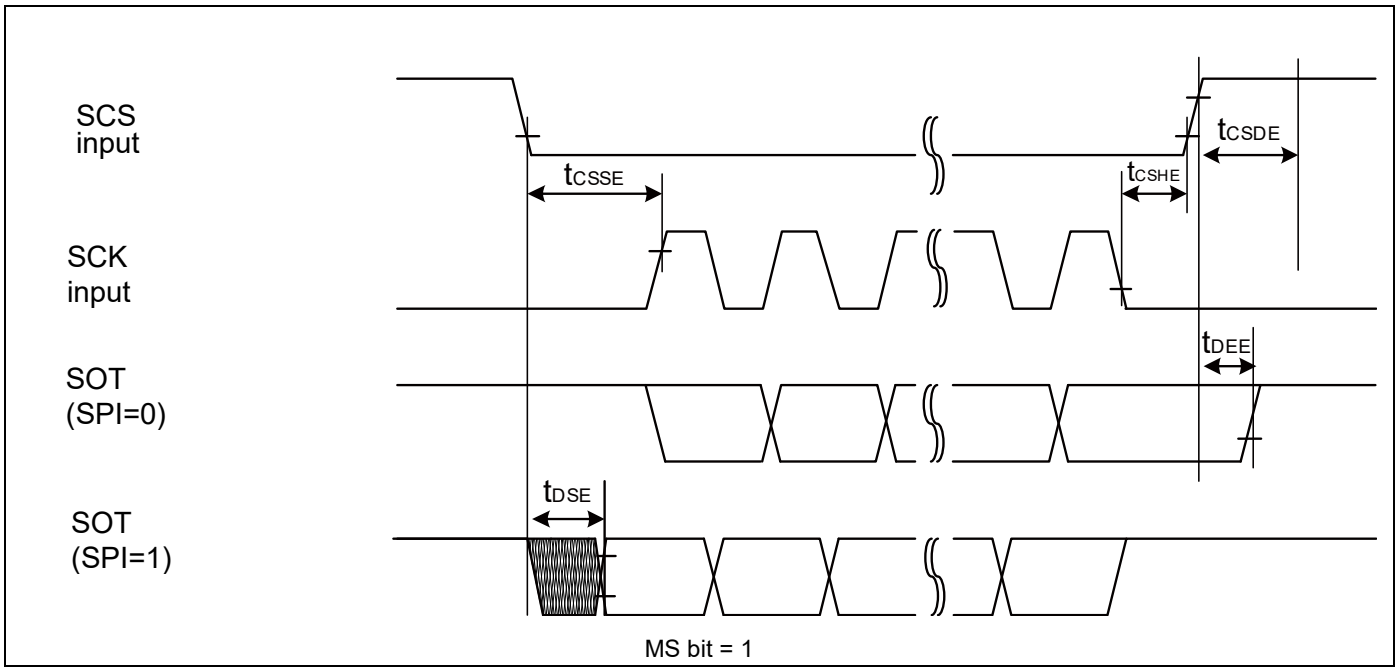
Parameter	Symbol	Conditions	V_{CC} < 4.5V		V_{CC} ≥ 4.5V		Unit
			Min	Max	Min	Max	
SCS↓→SCK↓ setup time	t_{CSSI}	Internal shift clock operation	[97]-50	[97]+0	[97]-50	[97]+0	ns
SCK↑→SCS↑ hold time	t_{CSHI}		[98]+0	[98]+50	[98]+0	[98]+50	ns
SCS deselect time	t_{CSDI}		[99]-50 +5t_{CYCP}	[99]+50 +5t_{CYCP}	[99]-50 +5t_{CYCP}	[99]+50 +5t_{CYCP}	ns
SCS↓→SCK↓ setup time	t_{CSSE}	External shift clock operation	3t_{CYCP}+30	-	3t_{CYCP}+30	-	ns
SCK↑→SCS↑ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		3t_{CYCP}+30	-	3t_{CYCP}+30	-	ns
SCS ↓ →SOT delay time	t_{DSE}		-	40	-	40	ns
SCS ↑ →SOT delay time	t_{DEE}		0	-	0	-	ns

Notes:

- *t_{CYCP} indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 1. Block Diagram in this datasheet.*
- *For more information about CSSU, CSHD, CSDS, and the serial chip select timing operating clock, see FM4 Family Peripheral Manual Main Part (002-04856).*
- *When the external load capacitance C_L = 30 pF.*

[97] CSSU bit value×serial chip select timing operating clock cycle [ns]
[98] CSHD bit value×serial chip select timing operating clock cycle [ns]
[99] CSDS bit value×serial chip select timing operating clock cycle [ns]


SCS
output
SCK
output
SOT
(SPI=0)
SOT
(SPI=1)
tCSSI
tCSDI
tCSHI
MS bit = 0


SCS
input
SCK
input
SOT
(SPI=0)
SOT
(SPI=1)
tCSSE
tCSDE
tCSHE
tDEE
tDSE
MS bit = 1

When Using Synchronous Serial Chip Select (SCINV = 0, CSLVL = 0)

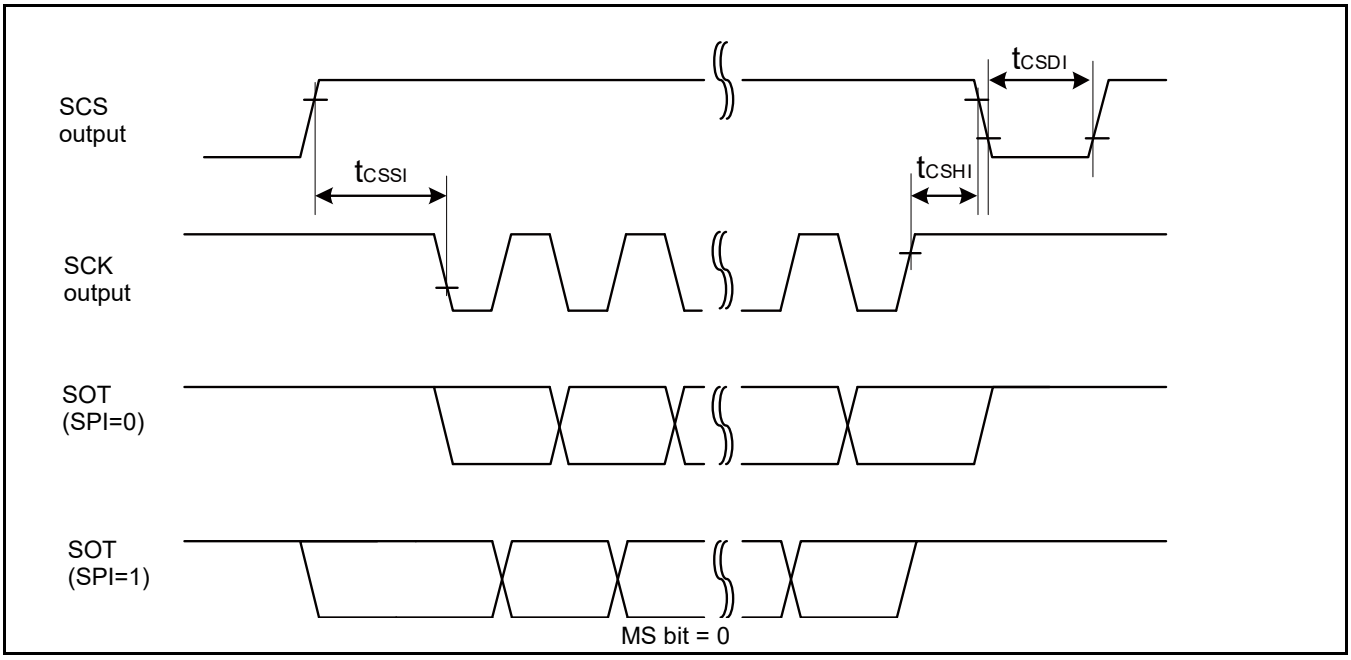
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

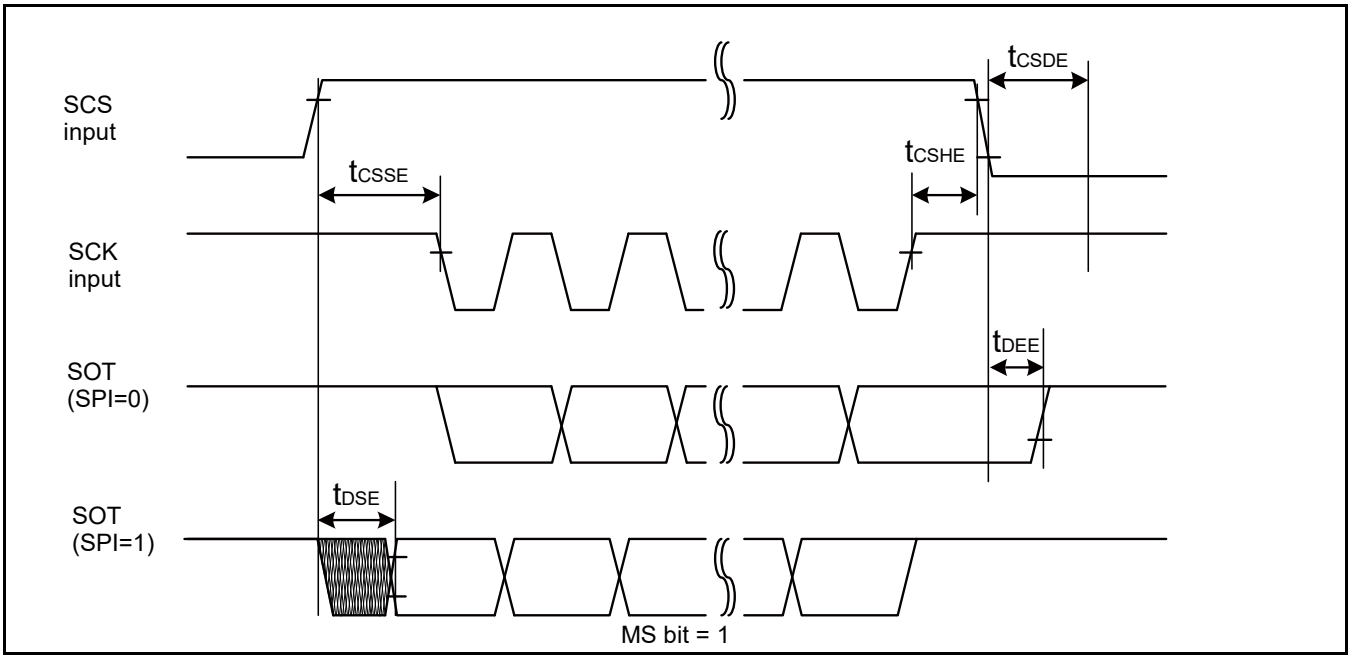
Parameter	Symbol	Conditions	V_{CC} < 4.5V		V_{CC} ≥ 4.5V		Unit
			Min	Max	Min	Max	
SCS↑→SCK↓ setup time	t_{CSSI}	Internal shift clock operation	[100]-50	[100]+0	[100]-50	[100]+0	ns
SCK↑→SCS↓ hold time	t_{CSHI}		[101]+0	[101]+50	[101]+0	[101]+50	ns
SCS deselect time	t_{CSDI}		[102]-50 +5t_{CYCP}	[102]+50 +5t_{CYCP}	[102]-50 +5t_{CYCP}	[102]+50 +5t_{CYCP}	ns
SCS↑→SCK↓ setup time	t_{CSSE}	External shift clock operation	3t_{CYCP}+30	-	3t_{CYCP}+30	-	ns
SCK↑→SCS↓ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		3t_{CYCP}+30	-	3t_{CYCP}+30	-	ns
SCS↑→SOT delay time	t_{DSE}		-	40	-	40	ns
SCS↓→SOT delay time	t_{DEE}		0	-	0	-	ns

Notes:

- *t_{CYCP} indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 1. Block Diagram in this datasheet.*
- *For more information about CSSU, CSHD, CSDS, and the serial chip select timing operating clock, see FM4 Family Peripheral Manual Main Part (002-04856).*
- *When the external load capacitance C_L = 30 pF.*

[100] CSSU bit value×serial chip select timing operating clock cycle [ns]
[101] CSHD bit value×serial chip select timing operating clock cycle [ns]
[102] CSDS bit value×serial chip select timing operating clock cycle [ns]


SCS
output
tCSSI
tCSDI
tCSHI
SCK
output
SOT
(SPI=0)
SOT
(SPI=1)
MS bit = 0


SCS
input
tCSSE
tCSDE
tCSHE
SCK
input
SOT
(SPI=0)
tDEE
tDSE
SOT
(SPI=1)
MS bit = 1

When Using Synchronous Serial Chip Select (SCINV = 1, CSLVL = 0)

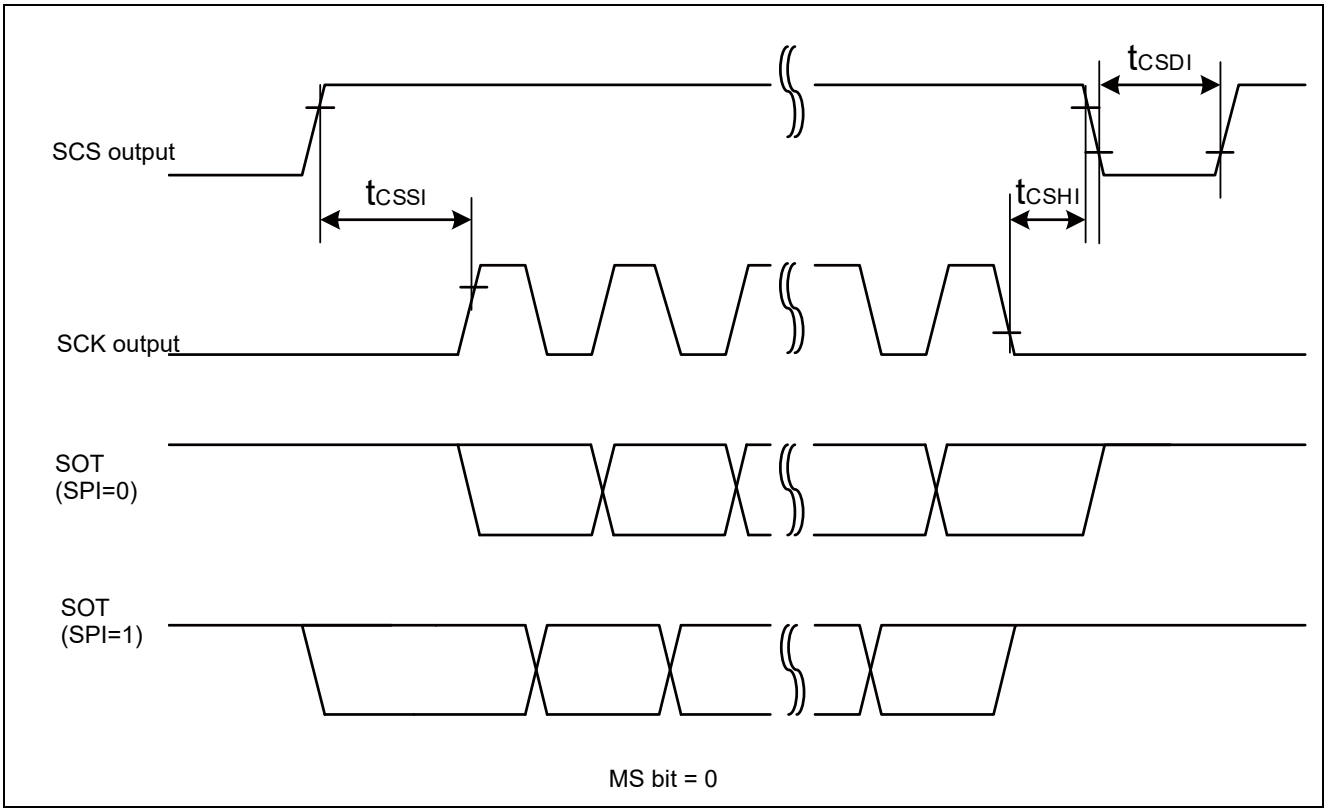
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

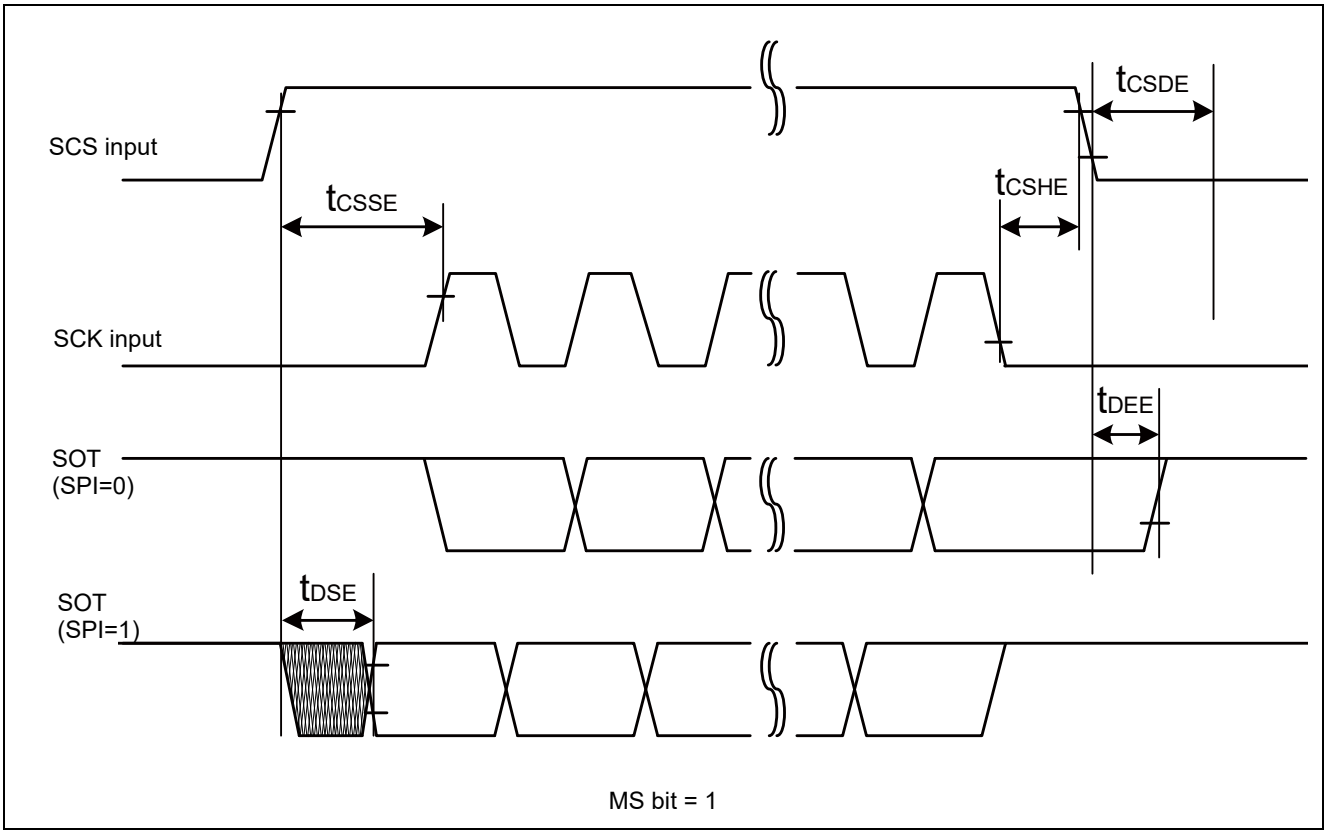
Parameter	Symbol	Conditions	V_{CC} < 4.5V		V_{CC} ≥ 4.5V		Units
			Min	Max	Min	Max	
SCS ↑ →SCK ↑ setup time	t_{CSSI}	Internal shift clock operation	[103]-50	[103]+0	[103]-50	[103]+0	ns
SCK ↓ →SCS ↓ hold time	t_{CSHI}		[104]+0	[104]+50	[104]+0	[104]+50	ns
SCS deselect time	t_{CSDI}		[105]-50 +5t_{CYCP}	[105]+50 +5t_{CYCP}	[105]-50 +5t_{CYCP}	[105]+50 +5t_{CYCP}	ns
SCS ↑ →SCK ↑ setup time	t_{CSSE}	External shift clock operation	3t_{CYCP}+30	-	3t_{CYCP}+30	-	ns
SCK ↓ →SCS ↓ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		3t_{CYCP}+30	-	3t_{CYCP}+30	-	ns
SCS ↑ →SOT delay time	t_{DSE}		-	40	-	40	ns
SCS ↓ →SOT delay time	t_{DEE}		0	-	0	-	ns

Notes:

- *t_{CYCP} indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 1. Block Diagram in this datasheet.*
- *For more information about CSSU, CSHD, CSDS, and the serial chip select timing operating clock, see FM4 Family Peripheral Manual Main Part (002-04856).*
- *When the external load capacitance C_L = 30 pF.*

[103] CSSU bit value×serial chip select timing operating clock cycle [ns]
[104] CSHD bit value×serial chip select timing operating clock cycle [ns]
[105] CSDS bit value×serial chip select timing operating clock cycle [ns]


SCS output
SCK output
SOT
(SPI=0)
SOT
(SPI=1)
tCSSI
tCSHI
tCSDI
MS bit = 0


SCS input
SCK input
SOT
(SPI=0)
SOT
(SPI=1)
tCSSE
tCSHE
tCSDE
tDEE
tDSE
MS bit = 1

High-Speed Synchronous Serial (SPI = 0, SCINV = 0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

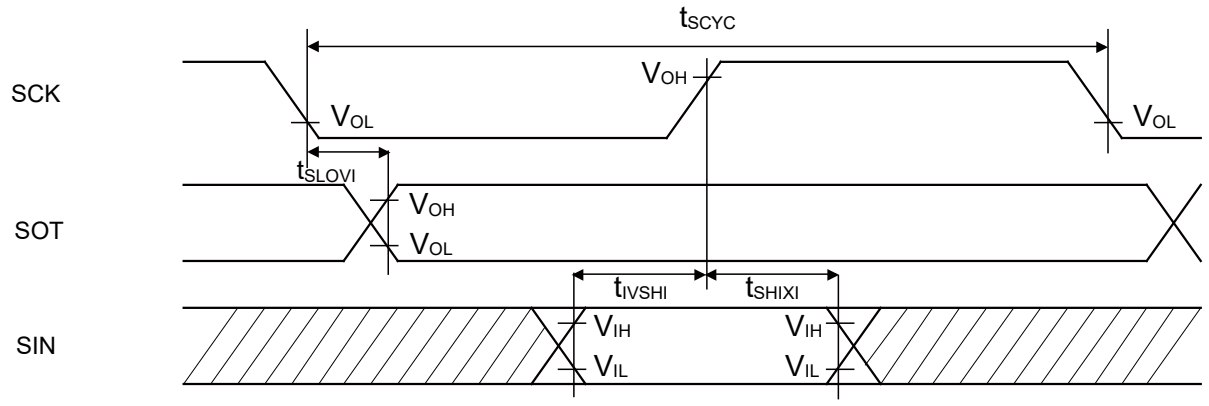
Parameter	Symbol	Pin Name	Conditions	V_{CC} < 4.5V		V_{CC} ≥ 4.5V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK↓→SOT delay time	t_{SLOVI}	SCKx, SOTx		- 10	+ 10	- 10	+ 10	ns
SIN→SCK↑ setup time	t_{IVSHI}	SCKx, SINx		14 12.5*	-	12.5	-	ns
SCK↑→SIN hold time	t_{SHIXI}	SCKx, SINx		5	-	5	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ - 5	-	$2t_{CYCP}$ - 5	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK↓→SOT delay time	t_{SLOVE}	SCKx, SOTx		-	15	-	15	ns
SIN→SCK↑ setup time	t_{IVSHE}	SCKx, SINx		5	-	5	-	ns
SCK↑→SIN hold time	t_{SHIXE}	SCKx, SINx		5	-	5	-	ns
SCK fall time	t_F	SCKx		-	5	-	5	ns
SCK rise time	t_R	SCKx		-	5	-	5	ns

Notes:

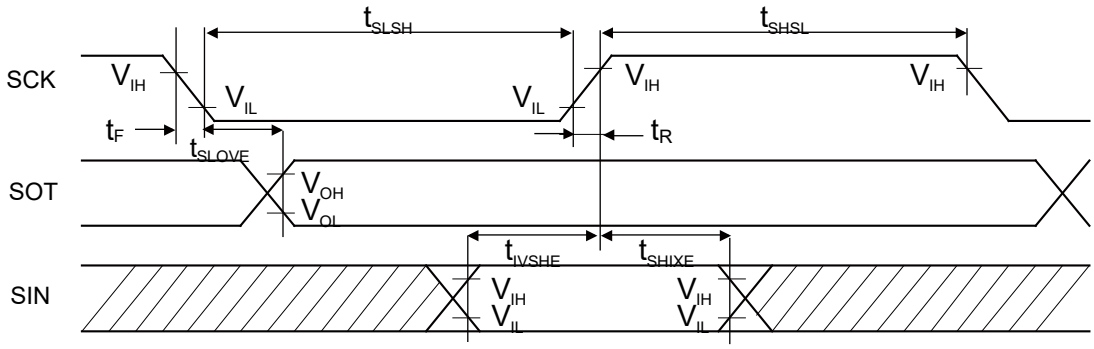
- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 1. Block Diagram in this datasheet.*
- *These characteristics only guarantee the following pins:*

  No chip select: SIN4_0, SOT4_0, SCK4_0

  Chip select: SIN6_0, SOT6_0, SCK6_0, SCS60_0, SCS61_0, SCS62_0, SCS63_0
- *When the external load capacitance C_L = 30 pF. (For *, when C_L = 10 pF)*



MS bit = 0



MS bit = 1

High-Speed Synchronous Serial (SPI = 0, SCINV = 1)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

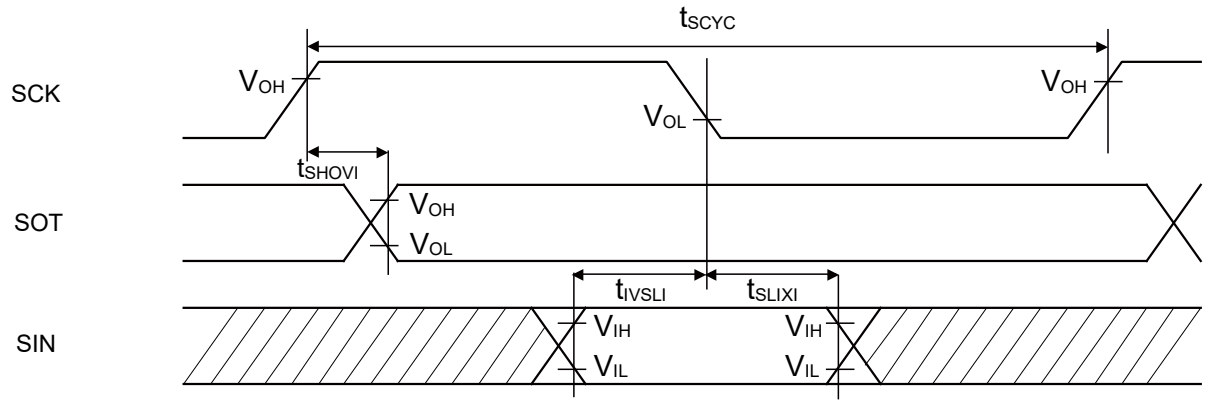
Parameter	Symbol	Pin Name	Conditions	V_{CC} < 4.5V		V_{CC} ≥ 4.5V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK↑→SOT delay time	t_{SHOVI}	SCKx, SOTx		- 10	+ 10	- 10	+ 10	ns
SIN→SCK↓ setup time	t_{IVSLI}	SCKx, SINx		14 12.5*	-	12.5	-	ns
SCK↓→SIN hold time	t_{SLIXI}	SCKx, SINx		5	-	5	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ - 5	-	$2t_{CYCP}$ - 5	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK↑→SOT delay time	t_{SHOVE}	SCKx, SOTx		-	15	-	15	ns
SIN→SCK↓ setup time	t_{IVSLE}	SCKx, SINx		5	-	5	-	ns
SCK↓→SIN hold time	t_{SLIXE}	SCKx, SINx		5	-	5	-	ns
SCK fall time	t_F	SCKx		-	5	-	5	ns
SCK rise time	t_R	SCKx		-	5	-	5	ns

Notes:

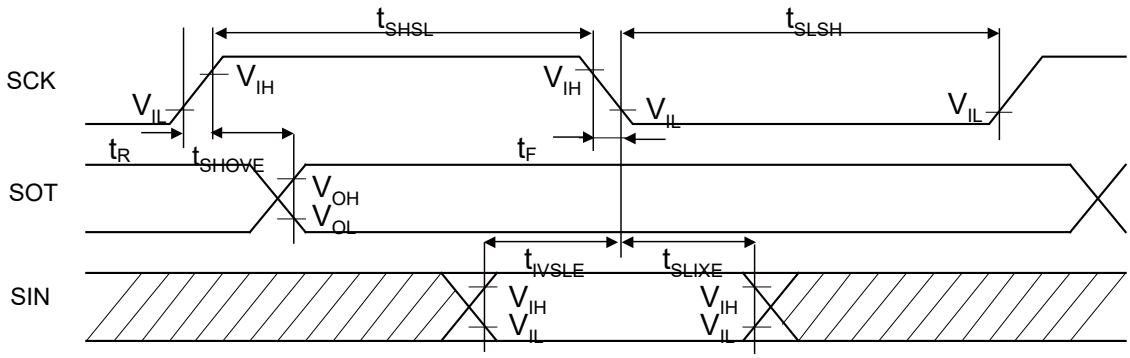
- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 1. Block Diagram in this datasheet.*
- *These characteristics only guarantee the following pins:*

  No chip select: SIN4_0, SOT4_0, SCK4_0

  Chip select: SIN6_0, SOT6_0, SCK6_0, SCS60_0, SCS61_0, SCS62_0, SCS63_0
- *When the external load capacitance C_L = 30 pF. (For *, when C_L = 10 pF)*



MS bit = 0



MS bit = 1

High-Speed Synchronous Serial (SPI = 1, SCINV = 0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

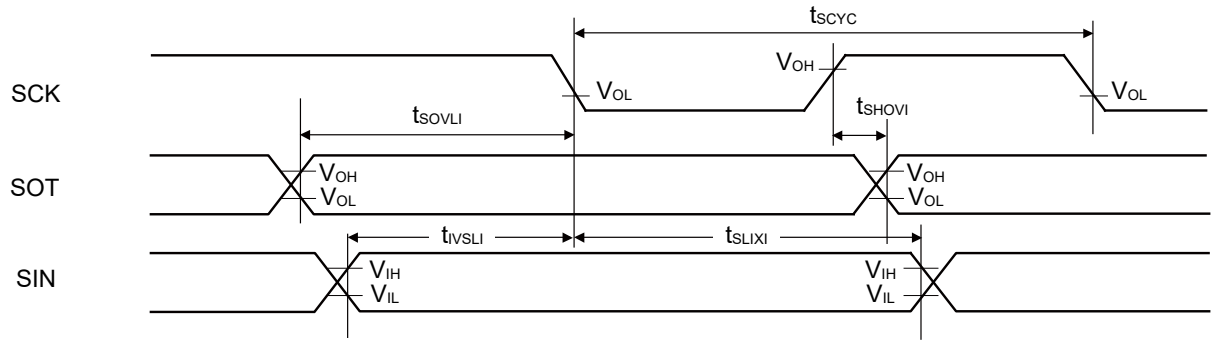
Parameter	Symbol	Pin Name	Conditions	V_{CC} < 4.5V		V_{CC} ≥ 4.5V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK↑→SOT delay time	t_{SHOVI}	SCKx, SOTx		- 10	+ 10	- 10	+ 10	ns
SIN→SCK↓ setup time	t_{IVSLI}	SCKx, SINx		14 12.5*	-	12.5	-	ns
SCK↓→SIN hold time	t_{SLIXI}	SCKx, SINx		5	-	5	-	ns
SOT→SCK↓ delay time	t_{SOVLI}	SCKx, SOTx		$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ - 5	-	$2t_{CYCP}$ - 5	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK↑→SOT delay time	t_{SHOVE}	SCKx, SOTx		-	15	-	15	ns
SIN→SCK↓ setup time	t_{IVSLE}	SCKx, SINx		5	-	5	-	ns
SCK↓→SIN hold time	t_{SLIXE}	SCKx, SINx		5	-	5	-	ns
SCK fall time	t_F	SCKx		-	5	-	5	ns
SCK rise time	t_R	SCKx		-	5	-	5	ns

Notes:

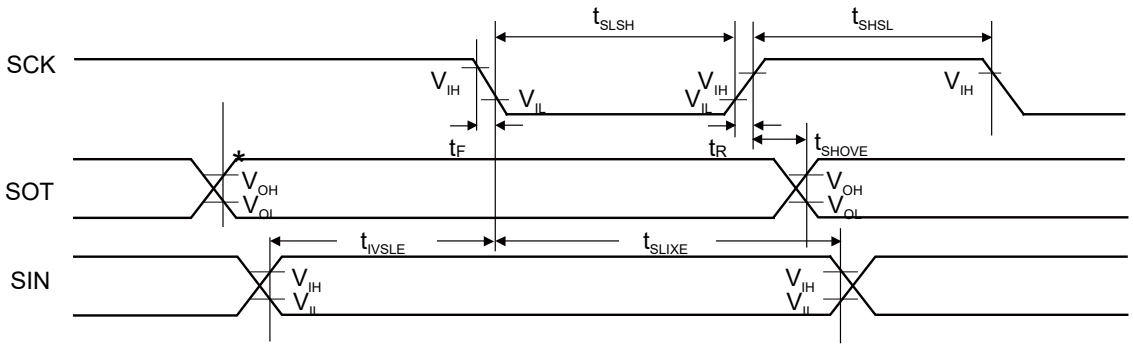
- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 1. Block Diagram in this datasheet.*
- *These characteristics only guarantee the following pins:*

  No chip select: SIN4_0, SOT4_0, SCK4_0

  Chip select: SIN6_0, SOT6_0, SCK6_0, SCS60_0, SCS61_0, SCS62_0, SCS63_0
- *When the external load capacitance C_L = 30 pF. (for *, when C_L = 10 pF)*



MS bit = 0



MS bit = 1

*: Changes when writing to TDR register

High-Speed Synchronous Serial (SPI = 1, SCINV = 1)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

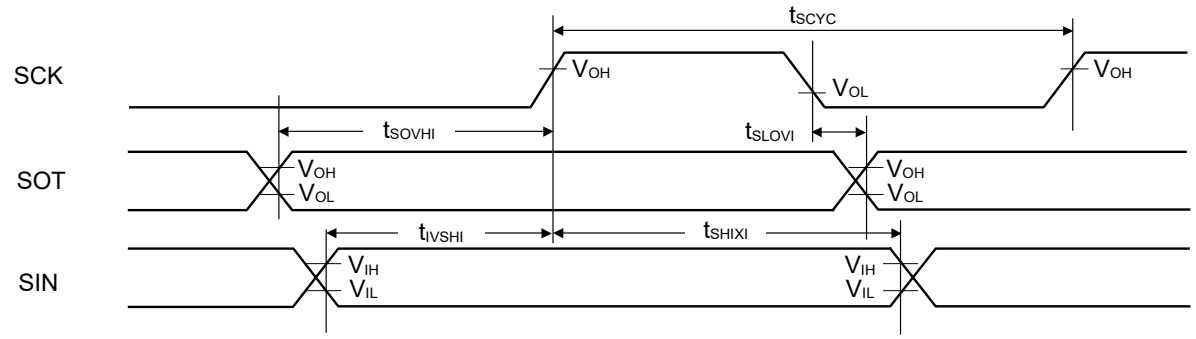
Parameter	Symbol	Pin Name	Conditions	V_{CC} < 4.5V		V_{CC} ≥ 4.5V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK↓→SOT delay time	t_{SLOVI}	SCKx, SOTx		- 10	+ 10	- 10	+ 10	ns
SIN→SCK↑ setup time	t_{IVSHI}	SCKx, SINx		14 12.5*	-	12.5	-	ns
SCK↑→SIN hold time	t_{SHIXI}	SCKx, SINx		5	-	5	-	ns
SOT→SCK↑ delay time	t_{SOVHI}	SCKx, SOTx		$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ - 5	-	$2t_{CYCP}$ - 5	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK↓→SOT delay time	t_{SLOVE}	SCKx, SOTx		-	15	-	15	ns
SIN→SCK↑ setup time	t_{IVSHE}	SCKx, SINx		5	-	5	-	ns
SCK↑→SIN hold time	t_{SHIXE}	SCKx, SINx		5	-	5	-	ns
SCK fall time	t_F	SCKx		-	5	-	5	ns
SCK rise time	t_R	SCKx		-	5	-	5	ns

Notes:

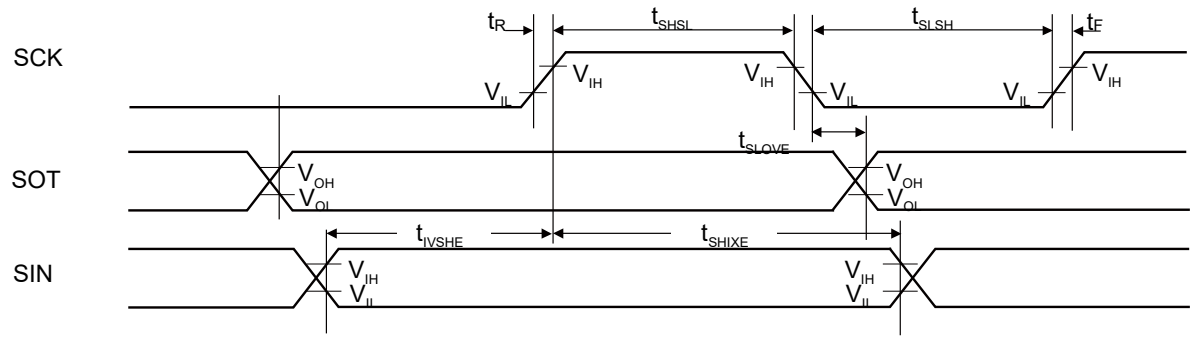
- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 1. Block Diagram in this datasheet.*
- *These characteristics only guarantee the following pins:*

  No chip select: SIN4_0, SOT4_0, SCK4_0

  Chip select: SIN6_0, SOT6_0, SCK6_0, SCS60_0, SCS61_0, SCS62_0, SCS63_0
- *When the external load capacitance C_L = 30 pF. (for *, when C_L = 10 pF)*



MS bit = 0



MS bit = 1

When Using High-Speed Synchronous Serial Chip Select (SCINV = 0, CSLVL = 1)

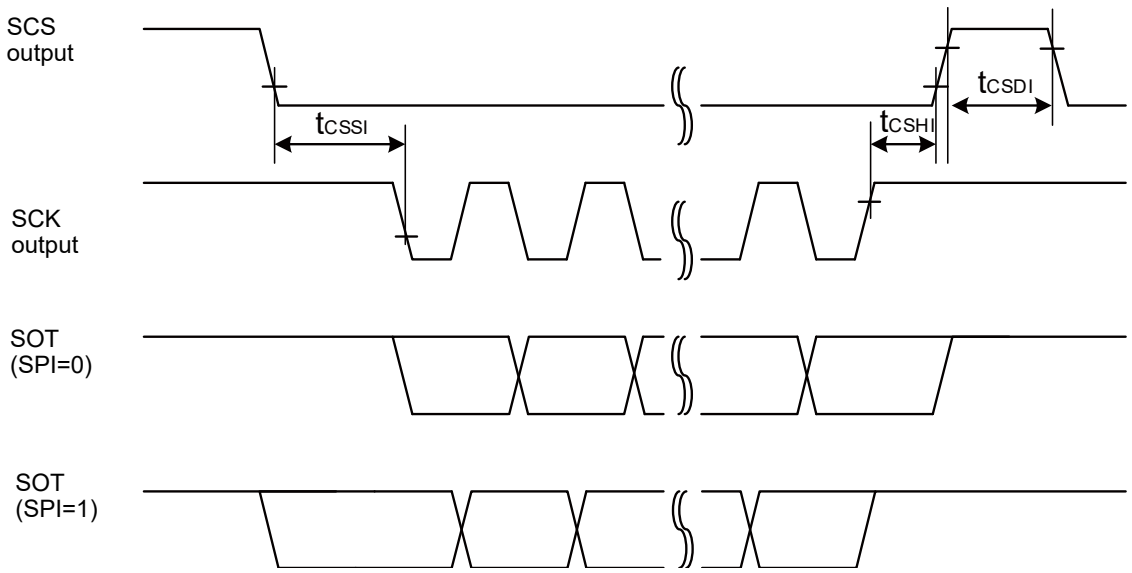
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	V_{CC} < 4.5V		V_{CC} ≥ 4.5V		Unit
			Min	Max	Min	Max	
SCS↓→SCK↓ setup time	t_{CSSI}	Internal shift clock operation	[106]-20	[106]+0	[106]-20	[106]+0	ns
SCK↑→SCS↑ hold time	t_{CSHI}		[107]+0	[107]+20	[107]+0	[107]+20	ns
SCS deselect time	t_{CSDI}		[108]-20 +5t_{CYCP}	[108]+20 +5t_{CYCP}	[108]-20 +5t_{CYCP}	[108]+20 +5t_{CYCP}	ns
SCS↓→SCK↓ setup time	t_{CSSE}	External shift clock operation	3t_{CYCP}+15	-	3t_{CYCP}+15	-	ns
SCK↑→SCS↑ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		3t_{CYCP}+15	-	3t_{CYCP}+15	-	ns
SCS↓→SOT delay time	t_{DSE}		-	25	-	25	ns
SCS↑→SOT delay time	t_{DEE}		0	-	0	-	ns

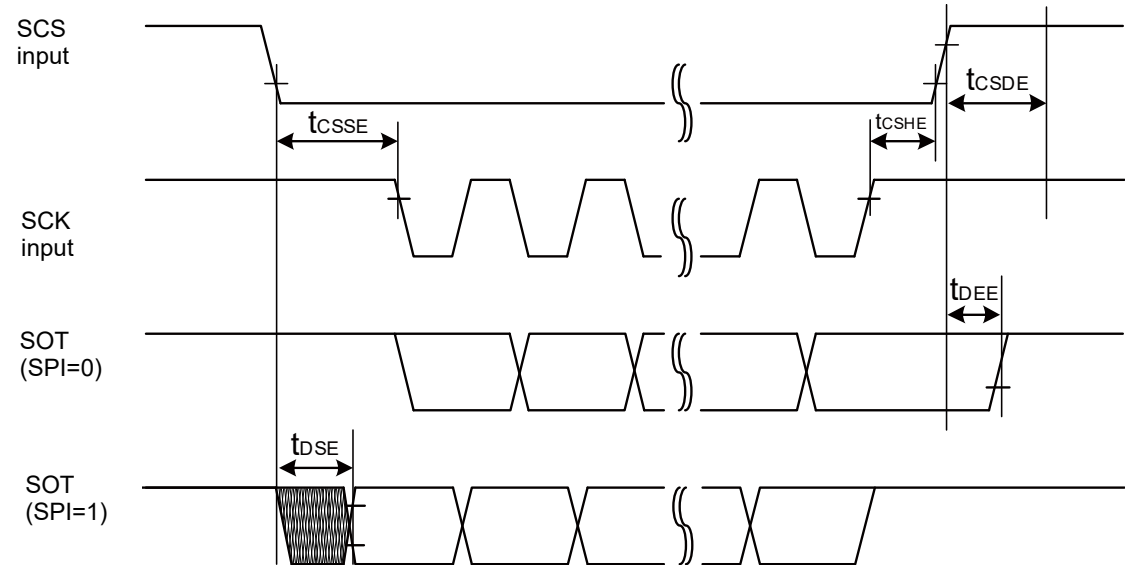
Notes:

- *t_{CYCP} indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 1. Block Diagram in this datasheet.*
- *For more information about CSSU, CSHD, CSDS, and the serial chip select timing operating clock, see FM4 Family Peripheral Manual Main Part (002-04856).*
- *When the external load capacitance C_L = 30 pF.*

[106] CSSU bit value×serial chip select timing operating clock cycle [ns]
[107] CSHD bit value×serial chip select timing operating clock cycle [ns]
[108] CSDS bit value×serial chip select timing operating clock cycle [ns]



MS bit = 0



MS bit = 1

When Using High-Speed Synchronous Serial Chip Select (SCINV = 1, CSLVL = 1)

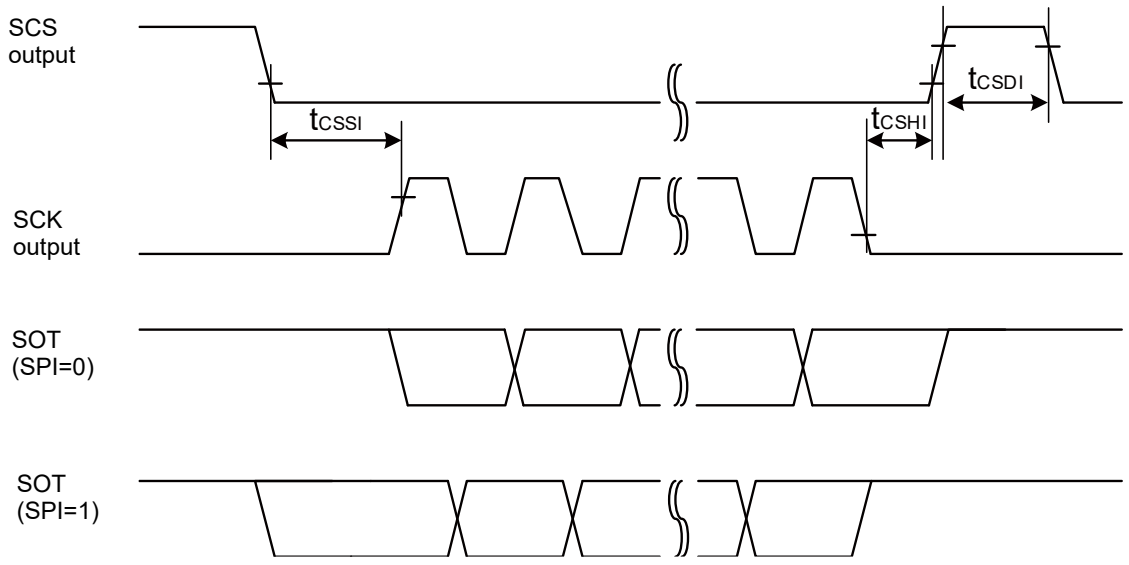
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	V_{CC} < 4.5V		V_{CC} ≥ 4.5V		Unit
			Min	Min	Min	Max	
SCS↓→SCK↓ setup time	t_{CSSI}	Internal shift clock operation	[109]-20	[109]+0	[109]-20	[109]+0	ns
SCK↑→SCS↑ hold time	t_{CSHI}		[110]+0	[110]+20	[110]+0	[110]+20	ns
SCS deselect time	t_{CSDI}		[111]-20 +5t_{CYCP}	[111]+20 +5t_{CYCP}	[111]-20 +5t_{CYCP}	[111]+20 +5t_{CYCP}	ns
SCS↓→SCK↑ setup time	t_{CSSE}	External shift clock operation	3t_{CYCP}+15	-	3t_{CYCP}+15	-	ns
SCK↑→SCS↑ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		3t_{CYCP}+15	-	3t_{CYCP}+15	-	ns
SCS↓→SOT delay time	t_{DSE}		-	25	-	25	ns
SCS↑→SOT delay time	t_{DEE}		0	-	0	-	ns

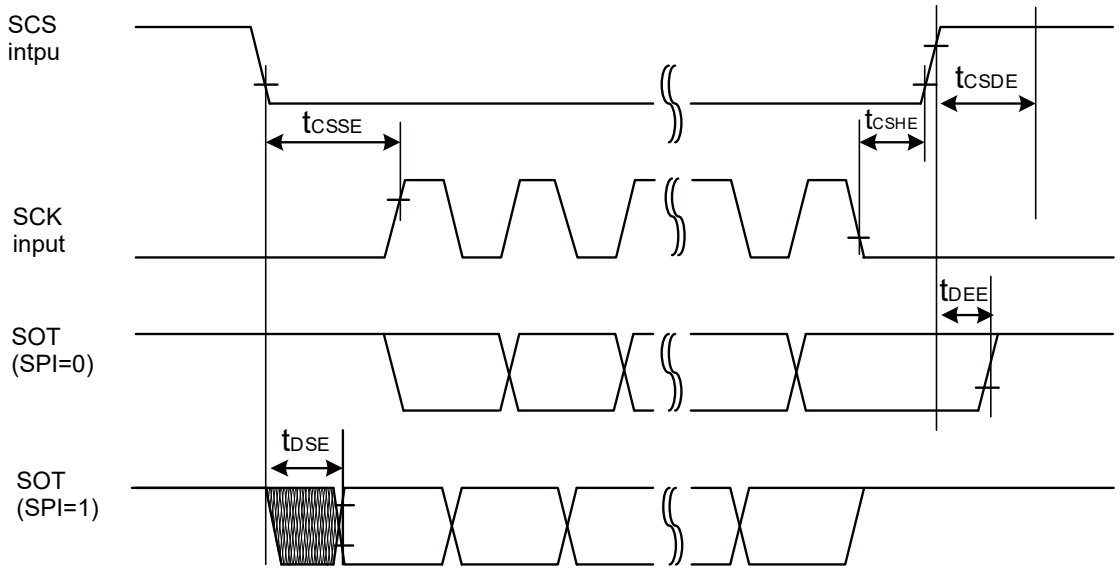
Notes:

- *t_{CYCP} indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 1. Block Diagram in this datasheet.*
- *For more information about CSSU, CSHD, CSDS, and the serial chip select timing operating clock, see FM4 Family Peripheral Manual Main Part (002-04856).*
- *When the external load capacitance C_L = 30 pF.*

[109] CSSU bit value×serial chip select timing operating clock cycle [ns]
[110] CSHD bit value×serial chip select timing operating clock cycle [ns]
[111] CSDS bit value×serial chip select timing operating clock cycle [ns]



MS bit = 0



MS bit = 1

When Using High-Speed Synchronous Serial Chip Select (SCINV = 0, CSLVL = 0)

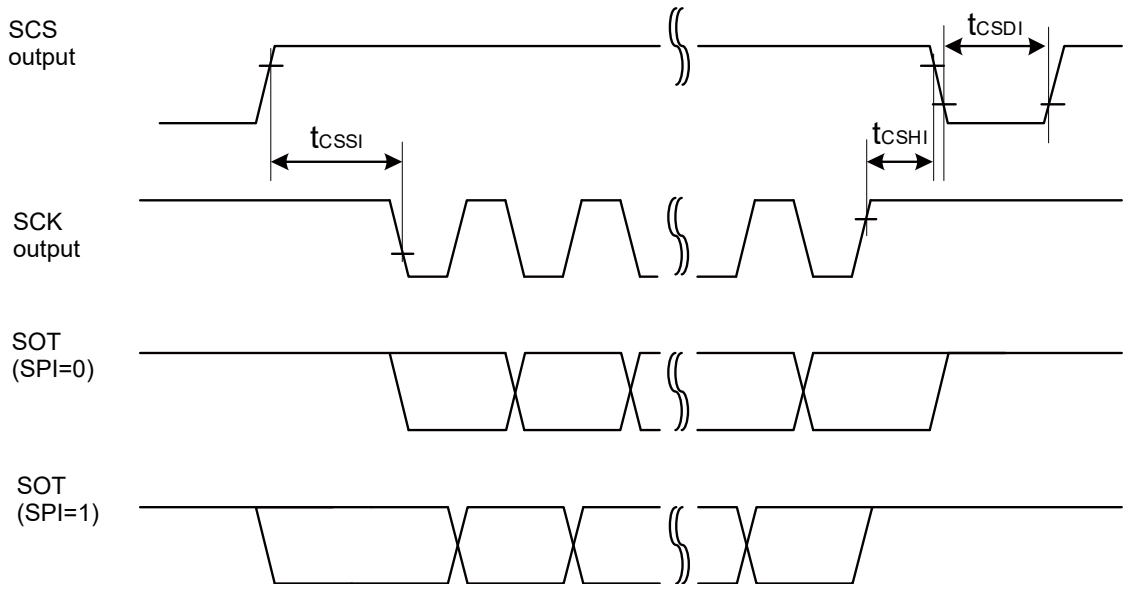
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	V_{CC} < 4.5V		V_{CC} ≥ 4.5V		Unit
			Min	Max	Min	Max	
SCS↑→SCK↓ setup time	t_{CSSI}	Internal shift clock operation	[112]-20	[112]+0	[112]-20	[112]+0	ns
SCK↑→SCS↓ hold time	t_{CSHI}		[113]+0	[113]+20	[113]+0	[113]+20	ns
SCS deselect time	t_{CSDI}		[114]-20 +5t_{CYCP}	[114]+20 +5t_{CYCP}	[114]-20 +5t_{CYCP}	[114]+20 +5t_{CYCP}	ns
SCS↑→SCK↓ setup time	t_{CSSE}	External shift clock operation	3t_{CYCP}+15	-	3t_{CYCP}+15	-	ns
SCK↑→SCS↓ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		3t_{CYCP}+15	-	3t_{CYCP}+15	-	ns
SCS↑→SOT delay time	t_{DSE}		-	25	-	25	ns
SCS↓→SOT delay time	t_{DEE}		0	-	0	-	ns

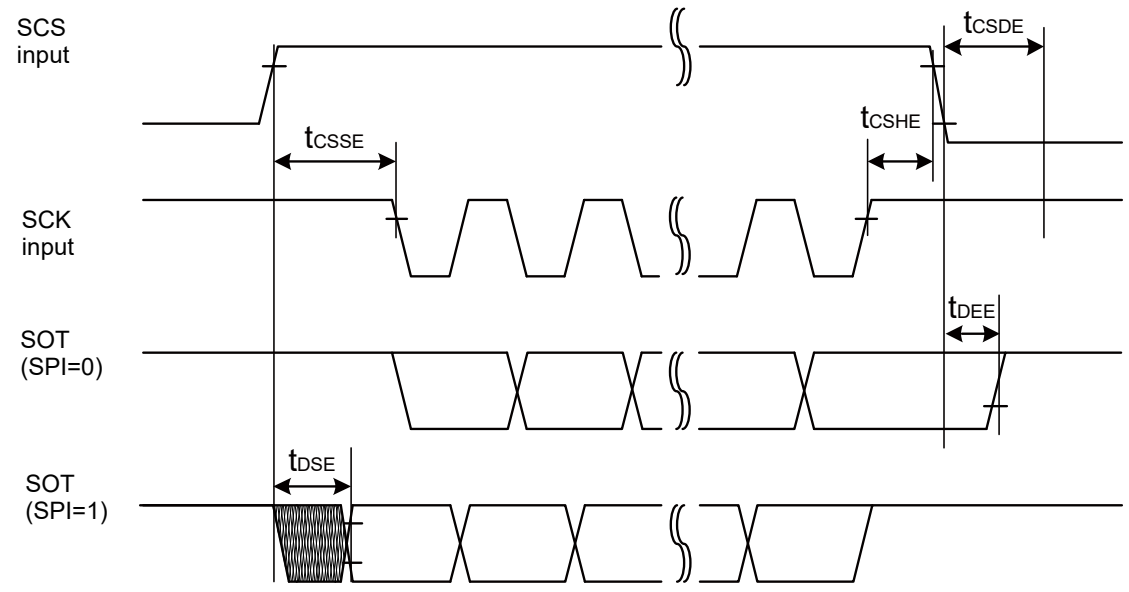
Notes:

- *t_{CYCP} indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 1. Block Diagram in this datasheet.*
- *For more information about CSSU, CSHD, CSDS, and the serial chip select timing operating clock, see FM4 Family Peripheral Manual Main Part (002-04856).*
- *When the external load capacitance C_L = 30 pF.*

[112] CSSU bit value×serial chip select timing operating clock cycle [ns]
[113] CSHD bit value×serial chip select timing operating clock cycle [ns]
[114] CSDS bit value×serial chip select timing operating clock cycle [ns]



MS bit = 0



MS bit = 1

When Using High-Speed Synchronous Serial Chip Select (SCINV = 1, CSLVL = 0)

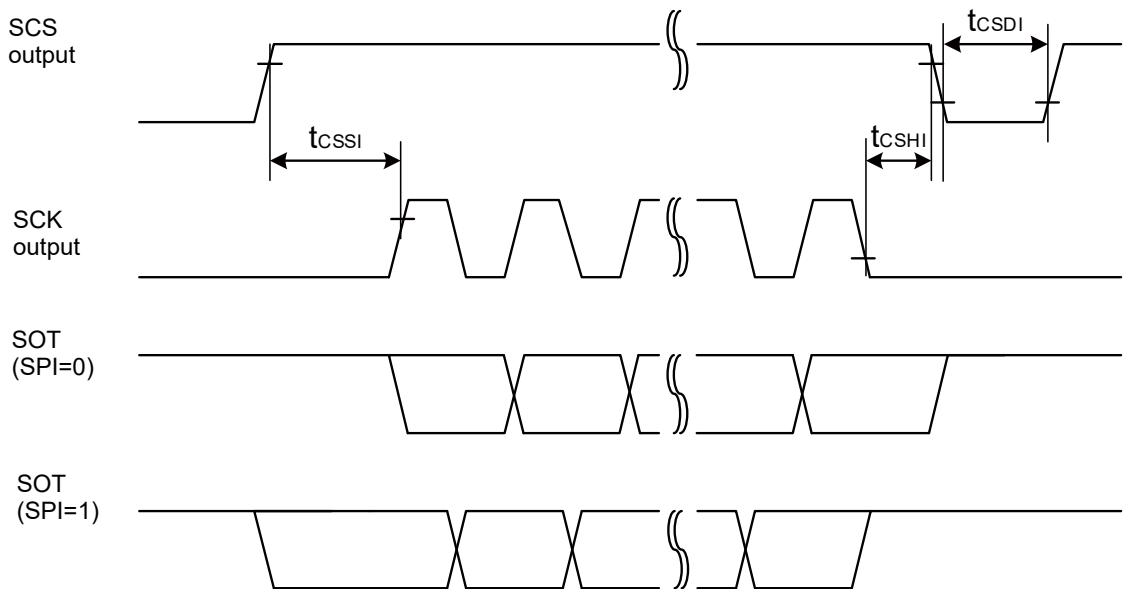
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	V_{CC} < 4.5V		V_{CC} ≥ 4.5V		Unit
			Min	Max	Min	Max	
SCS↓→SCK↓ setup time	t_{CSSI}	Internal shift clock operation	[115]-20	[115]+0	[115]-20	[115]+0	ns
SCK↑→SCS↓ hold time	t_{CSHI}		[116]+0	[116]+20	[116]+0	[116]+20	ns
SCS deselect time	t_{CSDI}		[117]-20 +5t_{CYCP}	[117]+20 +5t_{CYCP}	[117]-20 +5t_{CYCP}	[117]+20 +5t_{CYCP}	ns
SCS↑→SCK↑ setup time	t_{CSSE}	External shift clock operation	3t_{CYCP}+15	-	3t_{CYCP}+15	-	ns
SCK↓→SCS↓ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		3t_{CYCP}+15	-	3t_{CYCP}+15	-	ns
SCS↑→SOT delay time	t_{DSE}		-	40	-	40	ns
SCS↓→SOT delay time	t_{DEE}		0	-	0	-	ns

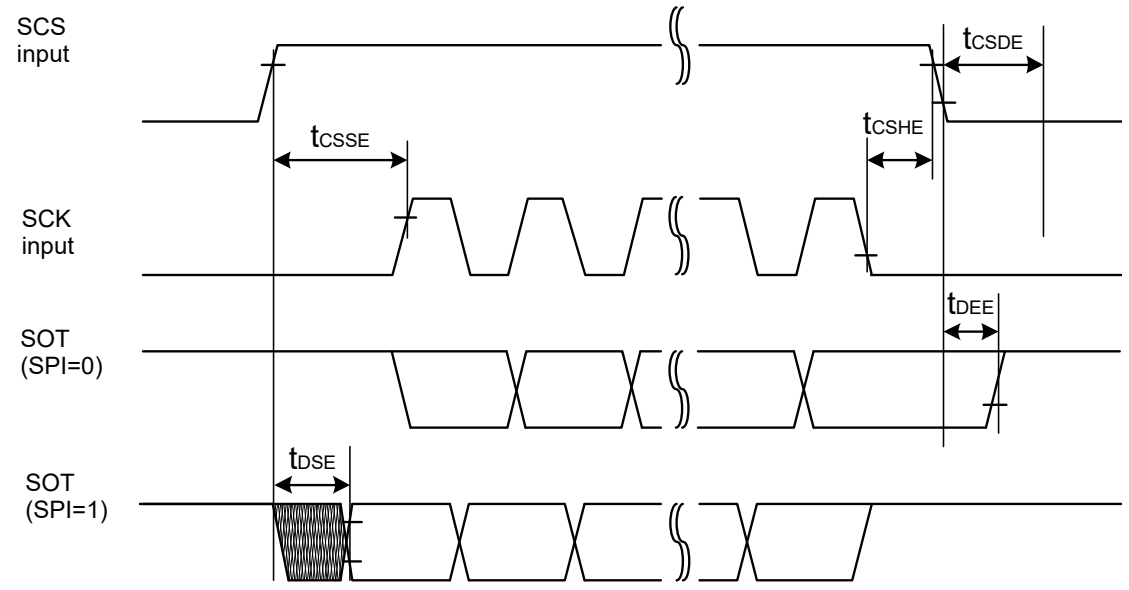
Notes:

- *t_{CYCP} indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 1. Block Diagram in this datasheet.*
- *For more information about CSSU, CSHD, CSDS, and the serial chip select timing operating clock, see FM4 Family Peripheral Manual Main Part (002-04856).*
- *When the external load capacitance C_L = 30 pF.*

[115] CSSU bit value×serial chip select timing operating clock cycle [ns]
[116] CSHD bit value×serial chip select timing operating clock cycle [ns]
[117] CSDS bit value×serial chip select timing operating clock cycle [ns]



MS bit = 0



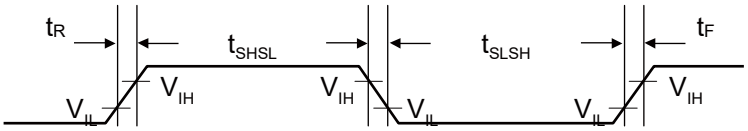
MS bit = 1

External Clock (EXT = 1): When in Asynchronous Mode Only

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min	Max		
Serial clock L pulse width	t_{SLSH}	C_L = 30 pF	t_{CYCP} + 10	-	ns	
Serial clock H pulse width	t_{SHSL}		t_{CYCP} + 10	-	ns	
SCK fall time	t_F		-	5	ns	
SCK rise time	t_R		-	5	ns	

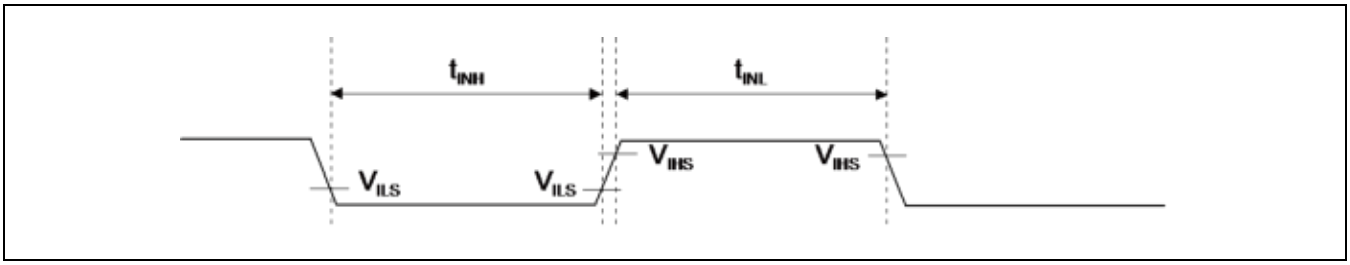
SCK



12.4.13 External Input Timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{INH}, t_{INL}	ADTGx	-	$2t_{CYCP}$[118]	-	ns	A/D converter trigger input
		FRCKx					Free-run timer input clock
		ICxx					Input capture
		DTTIxX	-	$2t_{CYCP}$[118]	-	ns	Waveform generator
		INT00 to INT31, NMIX	-	$2t_{CYCP}$ + 100[118]	-	ns	External interrupt, NMI
				500[119]	-	ns	
		WKUPx	-	500[120]	-	ns	Deep standby wake up

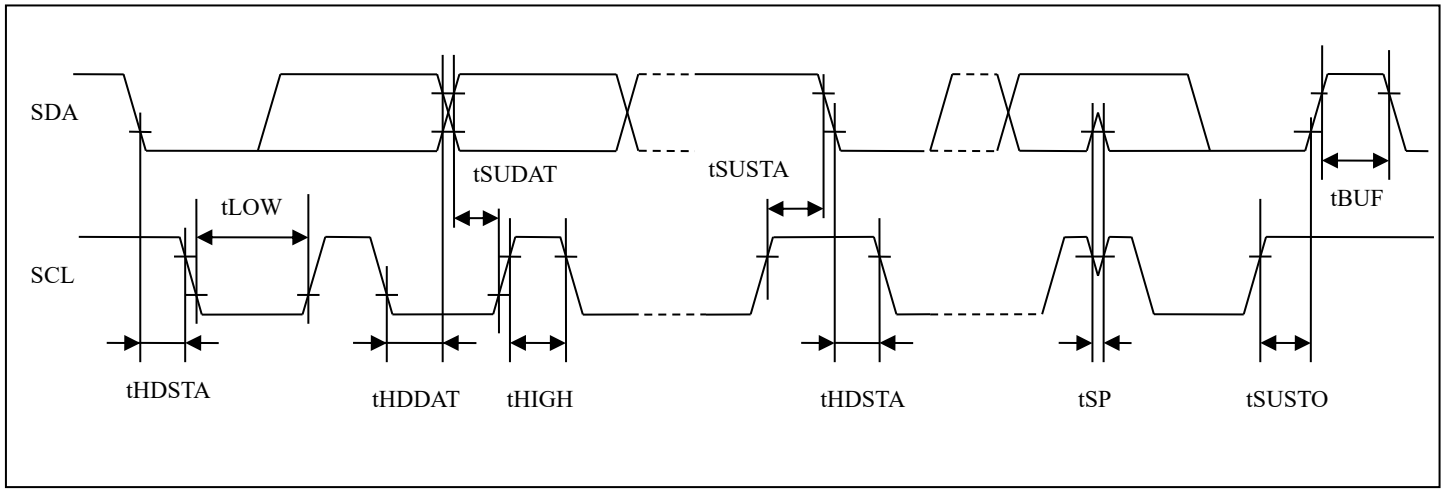


[118] t_{CYCP} indicates the APB bus clock cycle time except stop when in Stop mode, in Timer mode. For more information about the APB bus number to which the A/D converter, multi-function timer, and external interrupt are connected, see 1 Block Diagram in this data sheet.
[119] When in Stop mode, in Timer mode
[120] When in Deep Standby RTC mode, in Deep Standby Stop mode

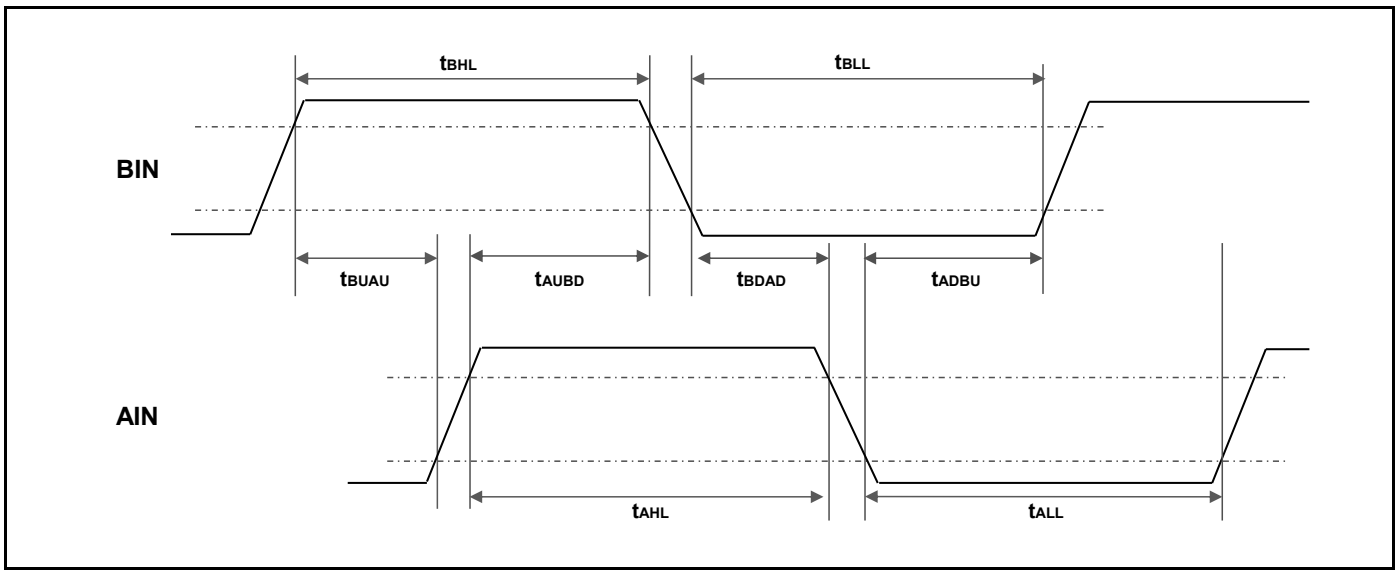
12.4.14 Quadrature Position/Revolution Counter Timing

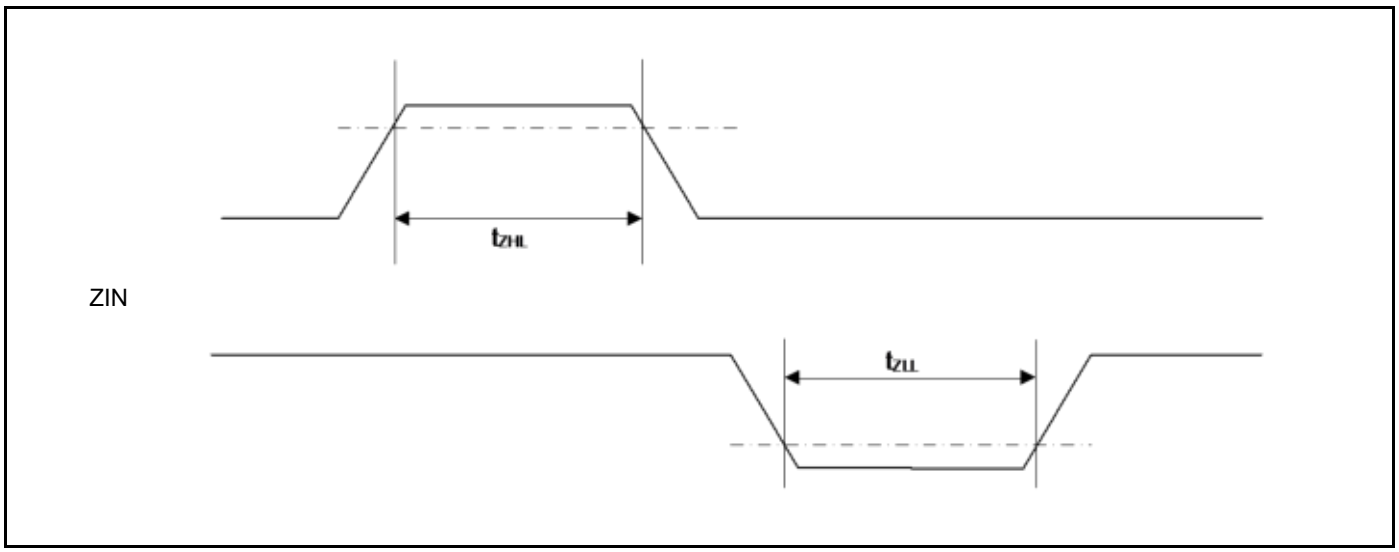
(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = -40°C to +105°C)

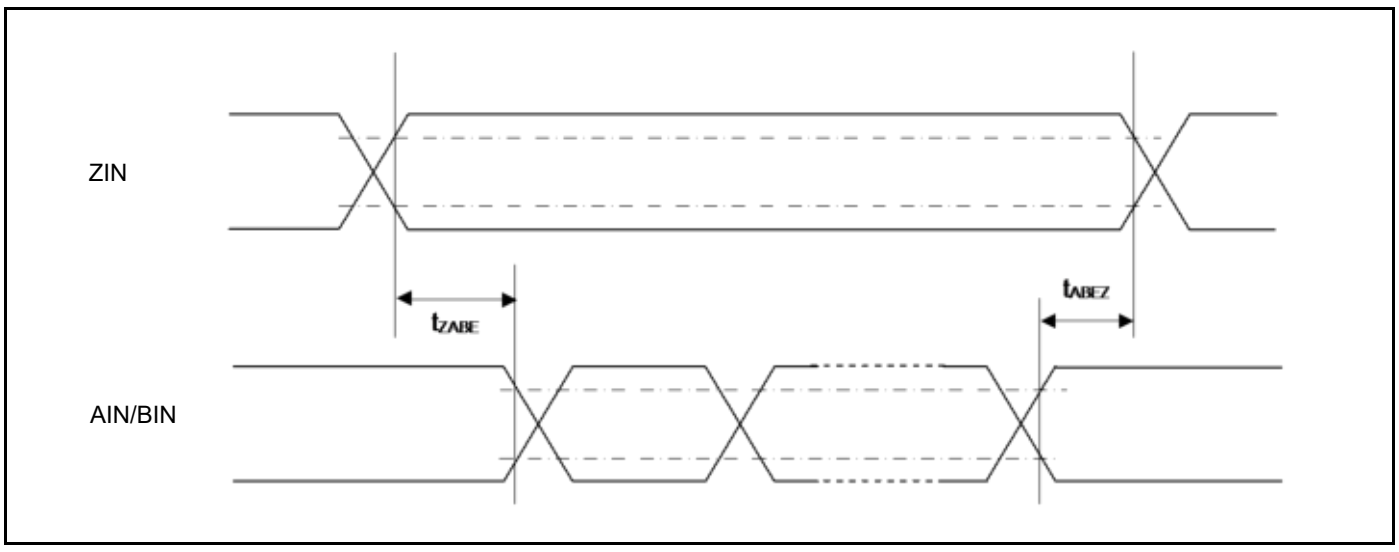
Parameter	Symbol	Conditions	Value		Unit
			Min	Max	
AIN pin H width	t_{AHL}	-	$2t_{CYCP}$[121]	-	ns
AIN pin L width	t_{ALL}	-			
BIN pin H width	t_{BHL}	-			
BIN pin L width	t_{BLL}	-			
BIN rise time from AIN pin H level	t_{AUBU}	PC_Mode2 or PC_Mode3			
AIN fall time from BIN pin H level	t_{BUAD}	PC_Mode2 or PC_Mode3			
BIN fall time from AIN pin L level	t_{ADBD}	PC_Mode2 or PC_Mode3			
AIN rise time from BIN pin L level	t_{BDAU}	PC_Mode2 or PC_Mode3			
AIN rise time from BIN pin H level	t_{BUAU}	PC_Mode2 or PC_Mode3			
BIN fall time from AIN pin H level	t_{AUBD}	PC_Mode2 or PC_Mode3			
AIN fall time from BIN pin L level	t_{BDAD}	PC_Mode2 or PC_Mode3			
BIN rise time from AIN pin L level	t_{ADBU}	PC_Mode2 or PC_Mode3			
ZIN pin H width	t_{ZHL}	QCR: CGSC = 0			
ZIN pin L width	t_{ZLL}	QCR: CGSC = 0			
AIN/BIN rise and fall time from determined ZIN level	t_{ZABE}	QCR: CGSC = 1			
Determined ZIN level from AIN/BIN rise and fall time	t_{ABEZ}	QCR: CGSC = 1			



[121] t_{CYCP} indicates the APB bus clock cycle time except when in Stop mode, in Timer mode. For more information about the APB bus number to which the quadrature position/revolution counter is connected, see 1. Block Diagram in this data sheet.


BIN
AIN
tBHL
tBLL
tBUAU
tAUBD
tBDAD
tADBU
tAHL
tALL


ZIN
tZHL
tZLL


ZIN
AIN/BIN
tZABE
tABEZ

12.4.15 I²C Timing

Standard-Mode, Fast-Mode

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

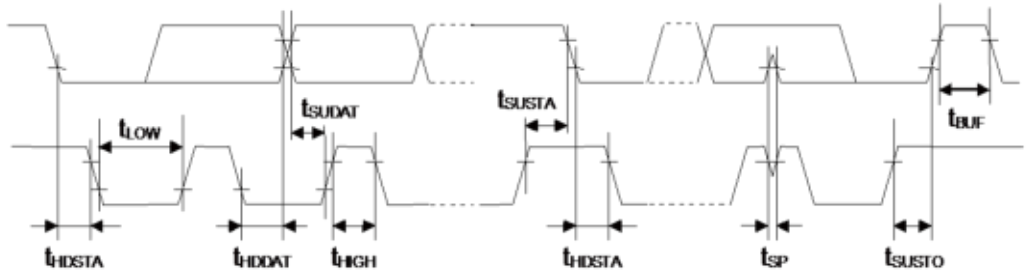
Parameter	Symbol	Conditions	Standard-Mode		Fast-Mode		Unit	Remarks
			Min	Max	Min	Max		
SCL clock frequency	f_{SCL}	C_L = 30 pF, R = (V_p/I_{OL})[122]	0	100	0	400	kHz	
(Repeated) START condition hold time SDA ↓ → SCL ↓	t_{HDSTA}		4.0	-	0.6	-	µs	
SCL clock L width	t_{LOW}		4.7	-	1.3	-	µs	
SCL clock H width	t_{HIGH}		4.0	-	0.6	-	µs	
(Repeated) START condition setup time SCL ↑ → SDA ↓	t_{SUSTA}		4.7	-	0.6	-	µs	
Data hold time SCL ↓ → SDA ↓ ↑	t_{HDDAT}		0	3.45[123]	0	0.9[124]	µs	
Data setup time SDA ↓ ↑ → SCL ↑	t_{SUDAT}		250	-	100	-	ns	
Stop condition setup time SCL ↑ → SDA ↑	t_{SUSTO}		4.0	-	0.6	-	µs	
Bus free time between "Stop condition" and "START condition"	t_{BUF}		4.7	-	1.3	-	µs	
Noise filter	t_{SP}	2 MHz ≤ t_{CYCP} < 40 MHz	2 t_{CYCP}[125]	-	2 t_{CYCP}[125]	-	ns	[126]
		40 MHz ≤ t_{CYCP} < 60 MHz	4 t_{CYCP}[125]	-	4 t_{CYCP}[125]	-	ns	
		60 MHz ≤ t_{CYCP} < 80 MHz	6 t_{CYCP}[125]	-	6 t_{CYCP}[125]	-	ns	
		80 MHz ≤ t_{CYCP} ≤ 100 MHz	8 t_{CYCP}[125]	-	8 t_{CYCP}[125]	-	ns	

[122] R and C_L represent the pull-up resistance and load capacitance of the SCL and SDA lines, respectively. V_p indicates the power supply voltage of the pull-up resistance and I_{OL} indicates V_{OL} guaranteed current.
[123] The maximum t_{HDDT} must not extend beyond the low period (t_{LOW}) of the device's SCL signal.
[124] Fast-mode I²C bus device can be used on a Standard-mode I²C bus system as long as the device satisfies the requirement of "t_{SUDAT} ≥ 250 ns.
[125] t_{CYCP} is the APB bus clock cycle time. For more information about the APB bus number to which the I²C is connected, see 1.Block Diagram in this data sheet.
When using Standard-mode, the peripheral bus clock must be set more than 2 MHz.
When using Fast-mode, the peripheral bus clock must be set more than 8 MHz.
[126] The noise filter time can be changed by register settings. Change the number of the noise filter steps according to the APB bus clock frequency.

Fast mode Plus (Fm+)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	Fast mode Plus (Fm+)[127]		Unit	Remarks
			Min	Max		
SCL clock frequency	f_{SCL}	C_L = 30 pF, R = (V_p/I_{OL})[128]	0	1000	kHz	
(Repeated) START condition hold time SDA ↓ → SCL ↓	t_{HDSTA}		0.26	-	µs	
SCL clock L width	t_{LOW}		0.5	-	µs	
SCL clock H width	t_{HIGH}		0.26	-	µs	
SCL clock frequency	t_{SUSTA}		0.26	-	µs	
(Repeated) START condition hold time SDA ↓ → SCL ↓	t_{HDDAT}		0	0.45[129, 130]	µs	
Data setup time SDA ↓ ↑ → SCL ↑	t_{SUDAT}		50	-	ns	
Stop condition setup time SCL ↑ → SDA ↑	t_{SUSTO}		0.26	-	µs	
Bus free time between "Stop condition" and "START condition"	t_{BUF}		0.5	-	µs	
Noise filter	t_{SP}	60 MHz ≤ t_{CYCP} < 80 MHz	6 t_{CYCP}[131]	-	ns	[132]
		80 MHz ≤ t_{CYCP} ≤ 100 MHz	8 t_{CYCP}[131]	-	ns	



[127] When using fast mode plus (Fm+), set the I/O pin to the mode corresponding to I²C Fm+ in the EPFR register. See Chapter 12: I/O Port in FM4 Family Peripheral Manual Main Part (002-04856) for the details.
[128] R and C_L represent the pull-up resistance and load capacitance of the SCL and SDA lines, respectively. V_p indicates the power supply voltage of the pull-up resistance and I_{OL} indicates V_{OL} guaranteed current.
[129] The maximum t_{HDDT} must not extend beyond the low period (t_{LOW}) of the device's SCL signal.
[130] The Fast mode I²C bus device can be used on a Standard-mode I²C bus system as long as the device satisfies the requirement of "t_{SUDAT} ≥ 250 ns.
[131] t_{CYCP} is the APB bus clock cycle time. For more information about the APB bus number to which the I²C is connected, see 1 Block Diagram in this data sheet. To use fast mode plus (Fm+), set the peripheral bus clock at 64 MHz or more.
[132] The noise filter time can be changed by register settings. Change the number of the noise filter steps according to the APB bus clock frequency.

12.4.16 SD Card Interface Timing

Default-Speed mode

■ Clock CLK (All values are referenced to V_{IH} and V_{IL} transition points)

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

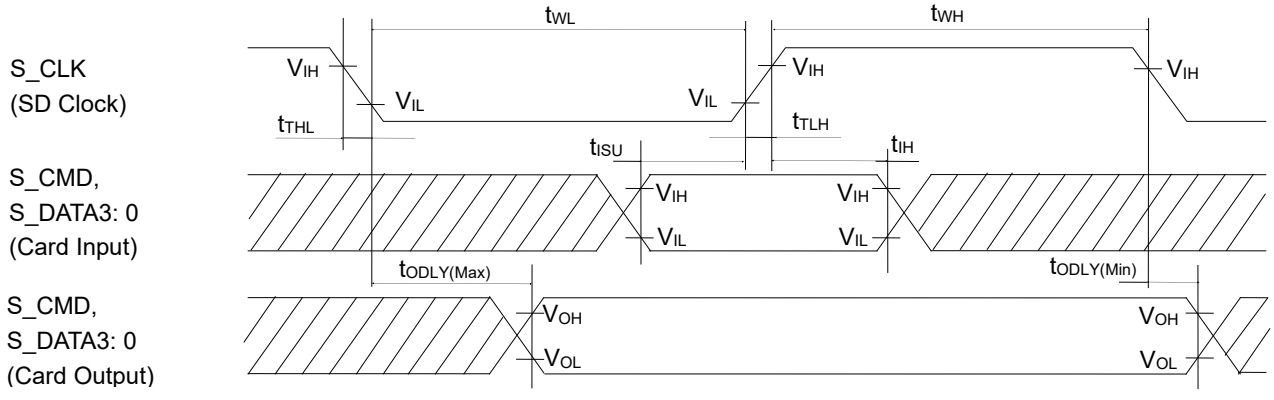
Parameter	Symbol	Pin Name	Conditions	Value		Remarks
				Min	Max	
Clock frequency Data Transfer mode	f_{PP}	S_CLK	C_{CARD} ≤ 10 pF (1card)	0[133]	25	MHz
Clock frequency Identification mode	f_{OD}	S_CLK		0[133]/100	400	kHz
Clock low time	t_{WL}	S_CLK		10	-	ns
Clock high time	t_{WH}	S_CLK		10	-	ns
Clock rise time	t_{TLH}	S_CLK		-	10	ns
Clock fall time	t_{THL}	S_CLK		-	10	ns

■ Card Inputs CMD, DAT (referenced to Clock CLK)

Parameter	Symbol	Pin Name	Conditions	Value		Remarks
				Min	Max	
Input set-up time	t_{ISU}	S_CMD, S_DATA3: 0	C_{CARD} ≤ 10 pF (1card)	5	-	ns
Input hold time	t_{IH}	S_CMD, S_DATA3: 0		5	-	ns

■ Card Outputs CMD, DAT (referenced to Clock CLK)

Parameter	Symbol	Pin Name	Conditions	Value		Remarks
				Min	Max	
Output Delay time during Data Transfer mode	t_{ODLY}	S_CMD, S_DATA3: 0	C_{CARD} ≤ 40 pF (1card)	0	14	ns
Output Delay time during Identification mode	t_{ODLY}	S_CMD, S_DATA3: 0		0	50	ns



Default-Speed mode

Notes:

− *The Card Input corresponds to the Host Output and the Card Output corresponds to the Host Input because this model is the Host.*

[133] 0 Hz means to stop the clock. The given minimum frequency range is for cases where a continuous clock is required.

– *For more information about clock frequency (f_{PP}), see Chapter 15: SD card Interface in FM4 Family Peripheral Manual Main Part (002-04856)*

High-speed mode

■ Clock CLK (All values are referred to V_{IH} and V_{IL})

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

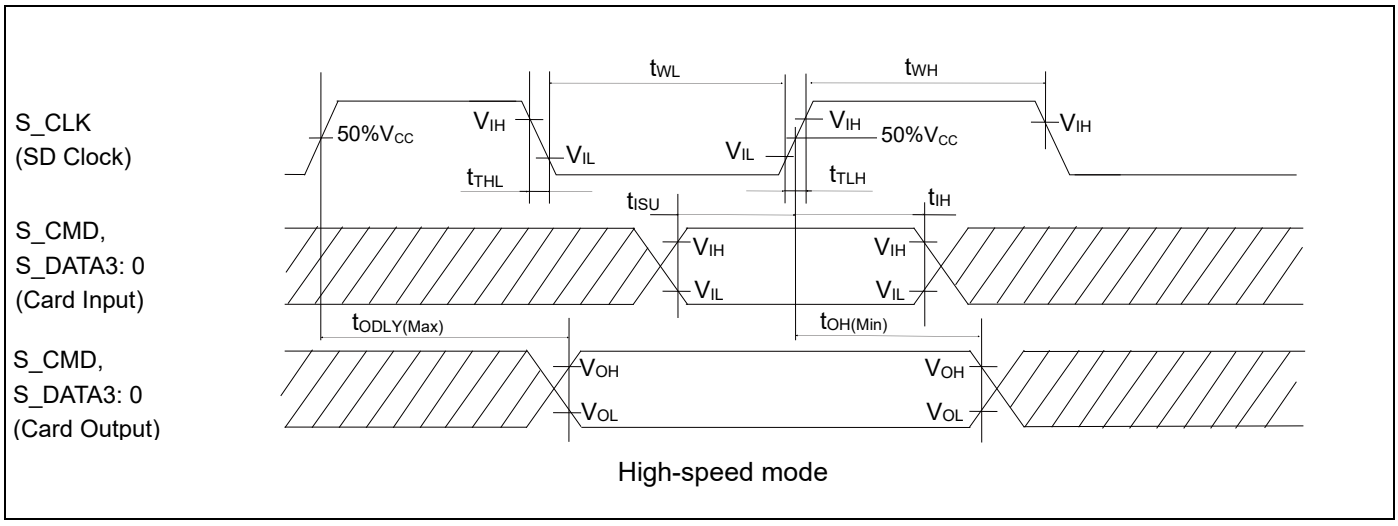
Parameter	Symbol	Pin Name	Conditions	Value		Remarks
				Min	Max	
Clock frequency Data Transfer mode	f_{PP}	S_CLK	C_{CARD} ≤ 10 pF (1card)	0	50	MHz
Clock low time	t_{WL}	S_CLK		7	-	ns
Clock high time	t_{WH}	S_CLK		7	-	ns
Clock rise time	t_{TLH}	S_CLK		-	3	ns
Clock fall time	t_{THL}	S_CLK		-	3	ns

■ Card Inputs CMD, DAT (referenced to Clock CLK)

Parameter	Symbol	Pin Name	Conditions	Value		Remarks
				Min	Max	
Input set-up time	t_{ISU}	S_CMD, S_DATA3: 0	C_{CARD} ≤ 10 pF (1card)	6	-	ns
Input hold time	t_{IH}	S_CMD, S_DATA3: 0		2	-	ns

■ Card Outputs CMD, DAT (referenced to Clock CLK)

Parameter	Symbol	Pin Name	Conditions	Value		Remarks
				Min	Max	
Output delay time during data transfer mode	t_{ODLY}	S_CMD, S_DATA3: 0	C_L ≤ 40 pF (1card)	0	14	ns
Output hold time	t_{OH}	S_CMD, S_DATA3: 0	C_L ≥ 15 pF (1card)	2.5	-	ns
Total system capacitance for each line[134]	C_L	-	1card	-	40	pF



High-speed mode

[134] In order to satisfy severe timing, host shall drive only one card.

Notes:

- *The Card Input corresponds to the Host Output and the Card Output corresponds to the Host Input because this model is the Host.*
- *For more information about clock frequency (f_{PP}), see Chapter 15: SD card Interface in FM4 Family Peripheral Manual Main Part (002-04856).*

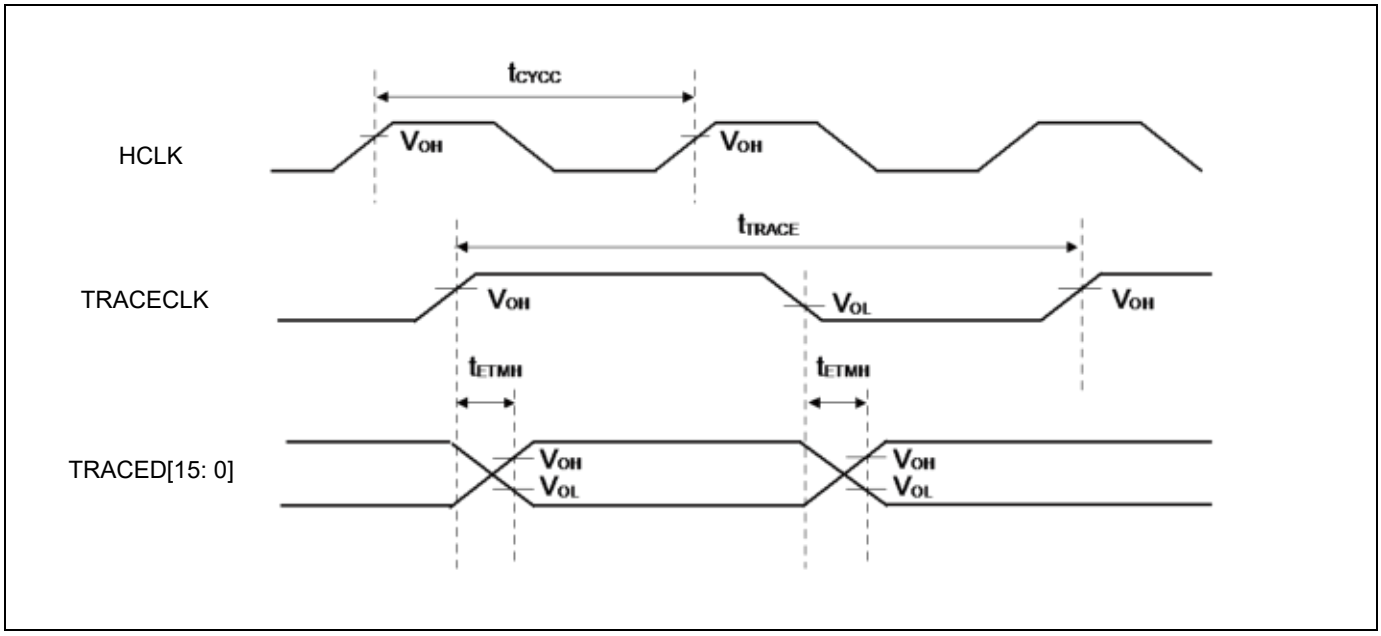
12.4.17 ETM/ HTM Timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Data hold	t_{ETMH}	TRACECLK, TRACED[15: 0]	$V_{CC} \geq 4.5V$	2	9	ns	
			V_{CC} <4.5V	2	15		
TRACECLK frequency	$1/t_{TRACE}$	TRACECLK	$V_{CC} \geq 4.5V$		50	MHz	
			V_{CC} <4.5V		32	MHz	
TRACECLK clock cycle	t_{TRACE}		$V_{CC} \geq 4.5V$	20	-	ns	
			V_{CC} <4.5V	31.25	-	ns	

Note:

- *When the external load capacitance C_L = 30 pF.*



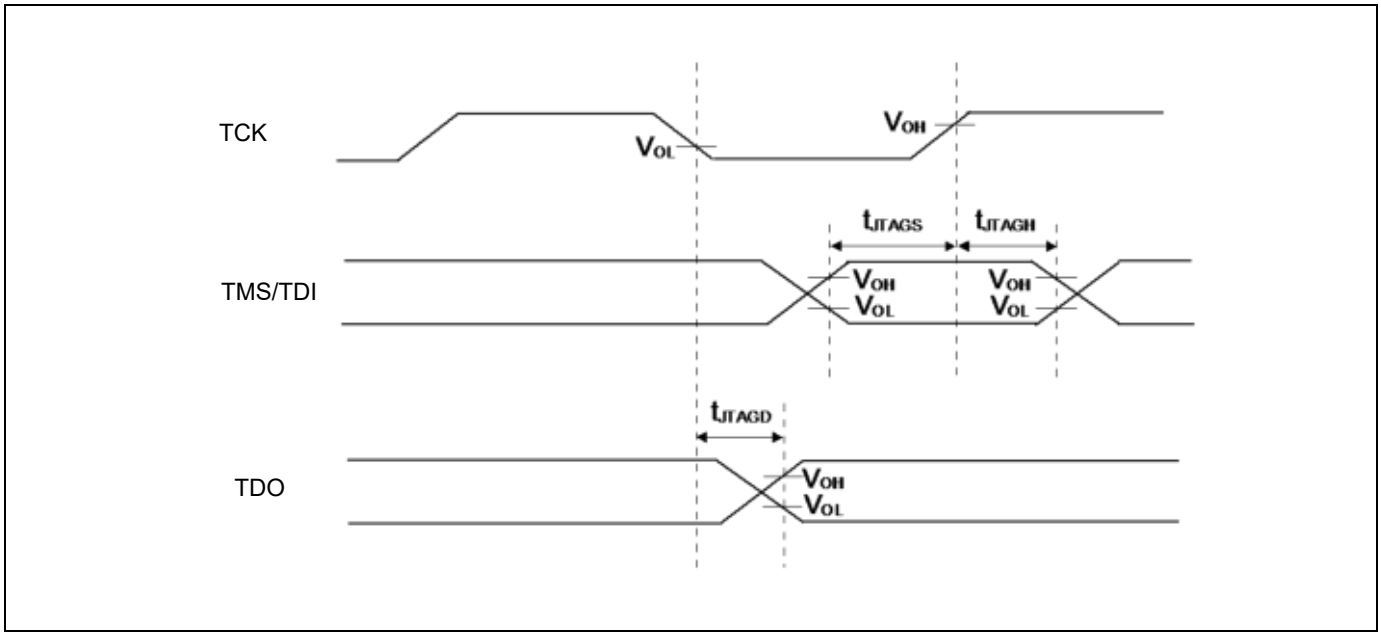
12.4.18 JTAG Timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
TMS, TDI setup time	t_{JTAGS}	TCK, TMS, TDI	$V_{CC} \geq 4.5V$	15	-	ns	
			$V_{CC} < 4.5V$				
TMS, TDI hold time	t_{JTAGH}	TCK, TMS, TDI	$V_{CC} \geq 4.5V$	15	-	ns	
			$V_{CC} < 4.5V$				
TDO delay time	t_{JTAGD}	TCK, TDO	$V_{CC} \geq 4.5V$	-	25	ns	
			$V_{CC} < 4.5V$	-	45		

Note:

- *When the external load capacitance C_L = 30 pF.*

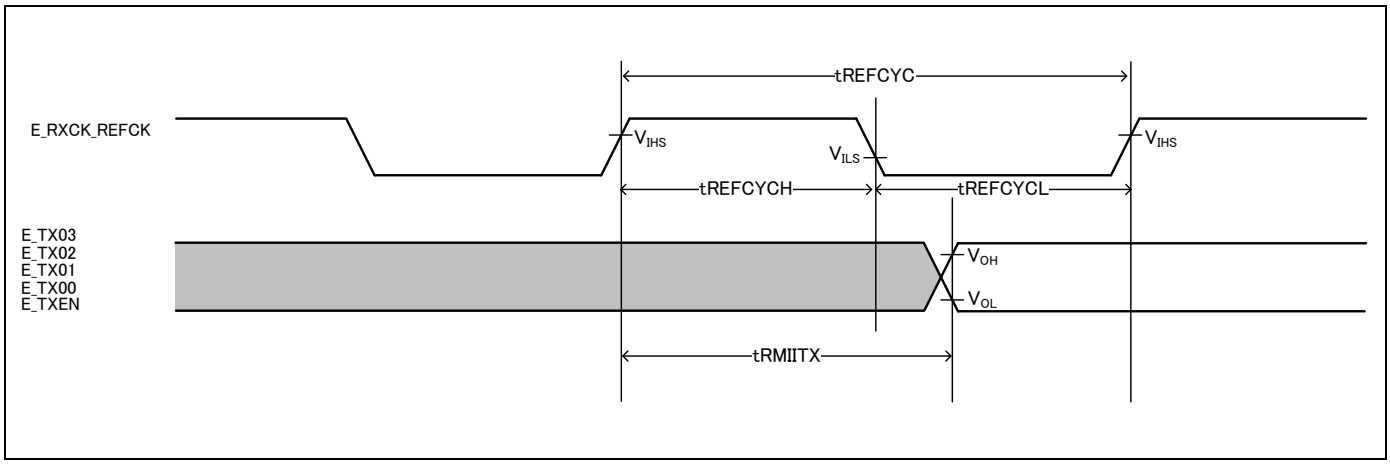


12.4.19 Ethernet-MAC Timing

RMII Transmission (100 Mbps/10 Mbps)

($ETHV_{CC}$ = 3.0V to 3.6V, 4.5V to 5.5V[135], V_{SS} = 0V, C_L = 25 pF)

Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Reference clock cycle time[136]	t_{REFCYC}	E_RXCK_REFCK	20 ns (typical)	-	-	ns
Reference clock High-pulse-width duty cycle	$t_{REFCYCH}$	E_RXCK_REFCK	$t_{REFCYCH}/t_{REFCYC}$	35	65	%
Reference clock Low-pulse-width duty cycle	$t_{REFCYCL}$	E_RXCK_REFCK	$t_{REFCYCL}/t_{REFCYC}$	35	65	%
Transmitted data → REFCK ↑ delay time	t_{RMIITX}	E_TX03, E_TX02, E_TX01, E_TX00, E_TXEN	-	-	12	ns

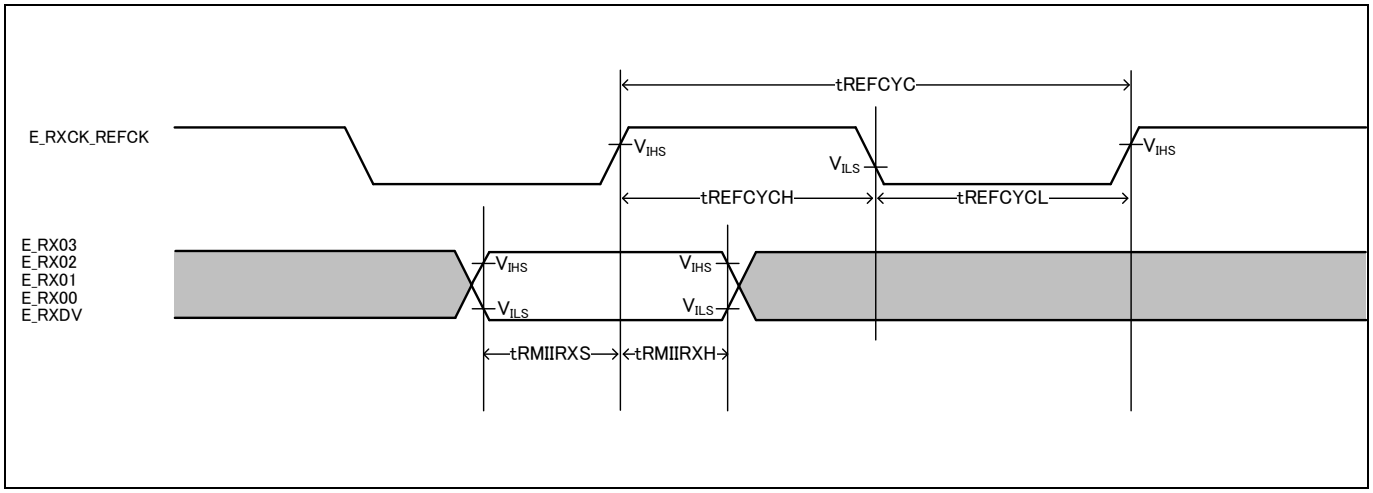


[135] When ETHV = 4.5V to 5.5V, it is recommended to add a series resistor at the output pin to suppress the output current.
[136] The reference clock is fixed to 50 MHz in the RMII specifications. The clock accuracy should meet the PHY-device specifications.

RMII Receiving (100 Mbps/10 Mbps)

($ETHV_{CC}$ = 3.0V to 3.6V, 4.5V to 5.5V, V_{SS} = 0V, C_L = 25 pF)

Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Reference clock cycle time[137]	t_{REFCYC}	E_RXCK_REFCK	20 ns (typical)	-	-	ns
Reference clock High-pulse-width duty cycle	$t_{REFCYCH}$	E_RXCK_REFCK	$t_{REFCYCH}/t_{REFCYC}$	35	65	%
Reference clock Low-pulse-width duty cycle	$t_{REFCYCL}$	E_RXCK_REFCK	$t_{REFCYCL}/t_{REFCYC}$	35	65	%
Received data → REFCK ↑ Setup time	$t_{RMIIRXS}$	E_RX03, E_RX02, E_RX01, E_RX00, E_RXDV	-	4	-	ns
Received data → REFCK ↑ Hold time	$t_{RMIIRXH}$	E_RX03, E_RX02, E_RX01, E_RX00, E_RXDV	-	2	-	ns

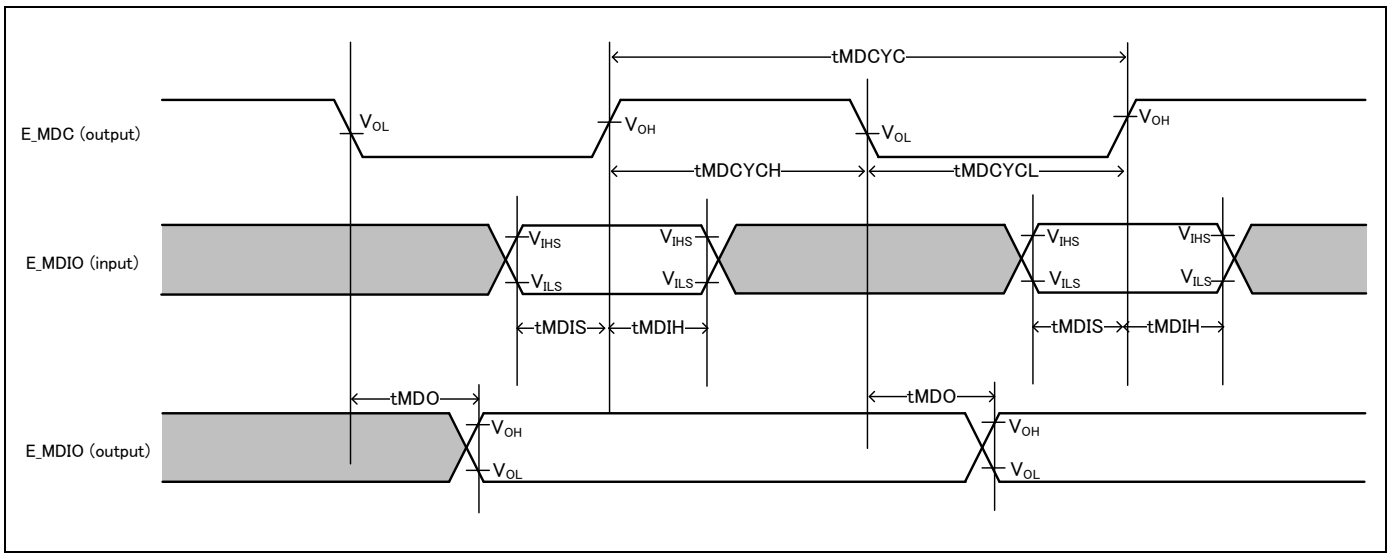


[137] The reference clock is fixed to 50 MHz in the RMII specifications. The clock accuracy should meet the PHY-device specifications.

Management Interface

($ETHV_{CC}$ = 3.0V to 3.6V, 4.5V to 5.5V, V_{SS} = 0V, C_L = 25 pF)

Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Management clock cycle time[138]	t_{MDCYC}	E_MDC	-	400	-	ns
Management clock High pulse width duty cycle	t_{MDCYCH}	E_MDC	t_{MDCYCH}/t_{MDCYC}	35	65	%
Management clock Low pulse width duty cycle	t_{MDCYCL}	E_MDC	t_{MDCYCL}/t_{MDCYC}	35	65	%
MDC ↓ → MDIO Delay time	t_{MDO}	E_MDIO	-	-	60	ns
MDIO → MDC ↑ Setup time	t_{MDIS}	E_MDIO	-	20	-	ns
MDC ↑ → MDIO Hold time	t_{MDIH}	E_MDIO	-	0	-	ns

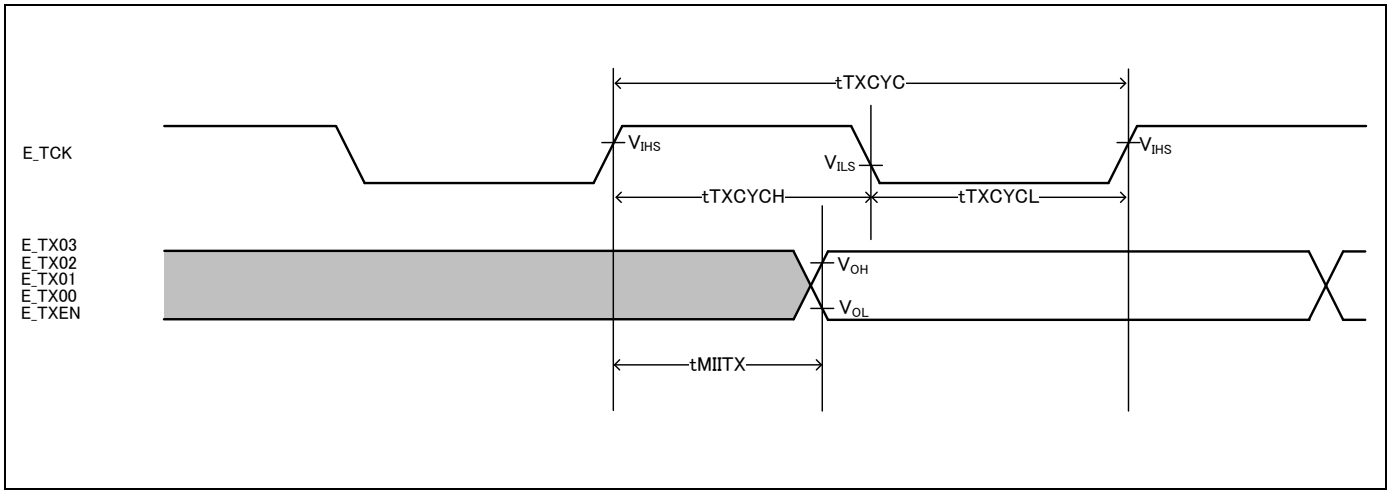


[138] The clock time should be set to a value greater than the minimum value by setting the Ethernet-MAC setting register.

MII Transmission (100 Mbps/10 Mbps)

($ETHV_{CC}$ = 3.0V to 3.6V, 4.5V to 5.5V[139], V_{SS} = 0V, C_L = 25 pF)

Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Transmission clock Cycle time[140]	t_{TXCYC}	E_TCK	100 Mbps 40 ns (typical)	-	-	ns
			100 Mbps 400 ns (typical)	-	-	ns
Transmission clock High-pulse-width duty cycle	t_{TXCYCH}	E_TCK	t_{TXCYCH}/t_{TXCYC}	35	65	%
Transmission clock Low-pulse-width duty cycle	t_{TXCYCL}	E_TCK	t_{TXCYCL}/t_{TXCYC}	35	65	%
TXCK ↑ → Transmitted data delay time	t_{MIITX}	E_TX03, E_TX02, E_TX01, E_TX00, E_TXEN	-	-	24	ns

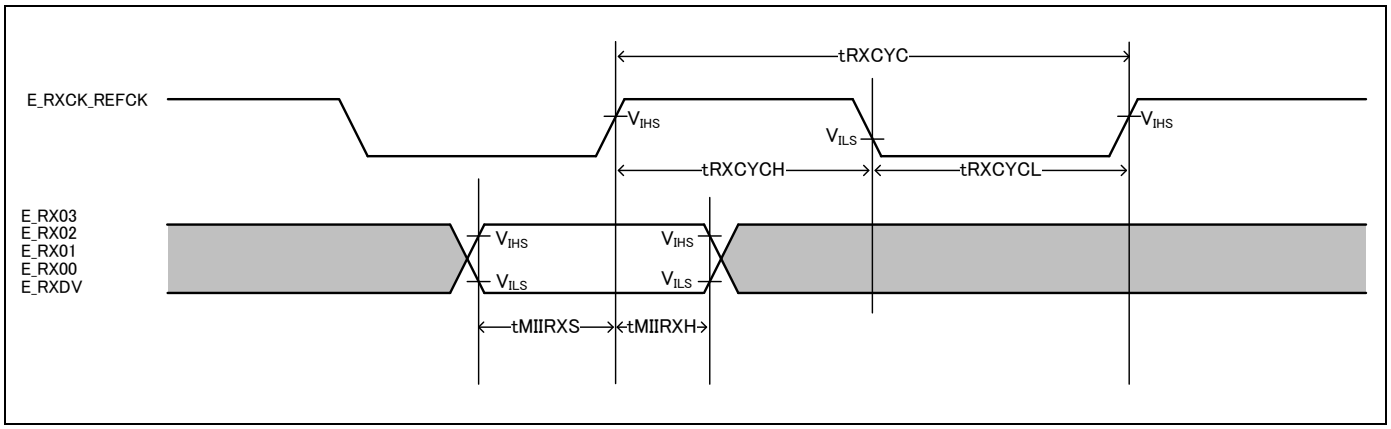


[139] When ETHV = 4.5V to 5.5V, it is recommended to add a series resistor at the output pin to suppress the output current.
[140] The transmission clock is fixed to 25 MHz or 2.5 MHz in the MII specifications. The clock accuracy should meet the PHY-device specifications.

MII Receiving (100 Mbps/10 Mbps)

($ETHV_{CC}$ = 3.0V to 3.6V, 4.5V to 5.5V, V_{SS} = 0V, C_L = 25 pF)

Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Receiving clock cycle time[141]	t_{RXCYC}	E_RXCK_REFCK	100 Mbps 40 ns (typical)	-	-	ns
			100 Mbps 400 ns (typical)	-	-	ns
Receiving clock High pulse width duty cycle	t_{RXCYCH}	E_RXCK_REFCK	t_{RXCYCH}/t_{RXCYC}	35	65	%
Receiving clock Low pulse width duty cycle	t_{RXCYCL}	E_RXCK_REFCK	t_{RXCYCL}/t_{RXCYC}	35	65	%
Received data → REFCK ↑Setup time	t_{MIIRXS}	E_RX03, E_RX02, E_RX01, E_RX00, E_RXDV	-	5	-	ns
REFCK ↑ → Received data Hold time	t_{MIIRXH}	E_RX03, E_RX02, E_RX01, E_RX00, E_RXDV	-	2	-	ns



[141] The reference clock is fixed to 50 MHz in the RMII specifications. The clock accuracy should meet the PHY-device specifications.

12.4.20 I²S Timing

Master Mode Timing

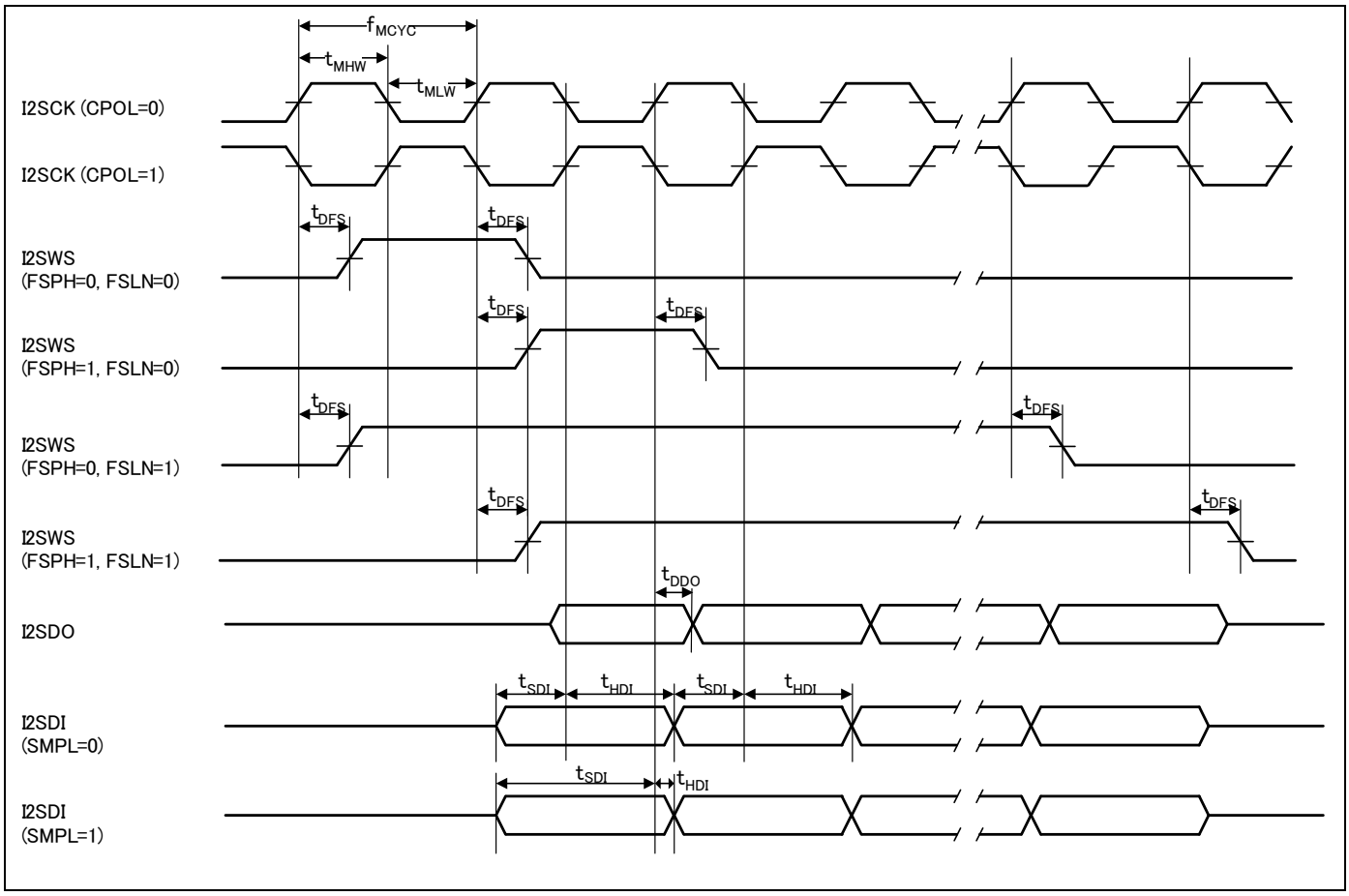
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Output frequency	f_{MCYC}	I2SCK	-	-	12.288	MHz	
Output clock pulse width	t_{MHW}	I2SCK	-	45	55	%	
	t_{MLW}			45	55	%	
I2SCK→I2SWS delay time	t_{DFS}	I2SCK, I2SWS	-	0	24.0	ns	
I2SCK→I2SDO delay time[142]	t_{DDO}	I2SCK, I2SDO	-	0	24.0	ns	
I2SDI→I2SCK setup time	t_{HSDI}	I2SCK, I2SDI	-	25.0	-	ns	
I2SDI→I2SCK hold time	t_{HDJ}		-	0	-	ns	
Input signal rise time	t_{FI}	I2SDI	-	-	5	ns	
Input signal fall time	t_{FI}		-	-	5	ns	

Notes:

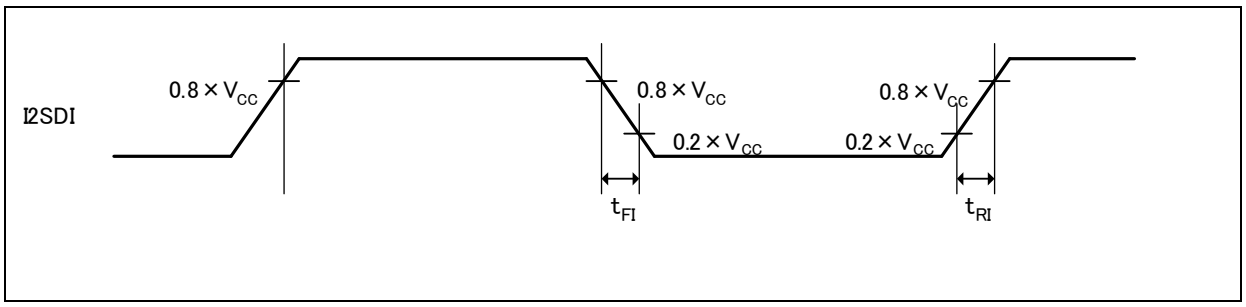
- *When the external load capacitance C_L = 20 pF*
- *When I2SWS = 48 kHz, I2MCLK = 256 × I2SWS*
  Frame synchronization signal (I2SWS) is settable to 48 kHz, 32 kHz, 16 kHz.
  See Chapter 7-2: I²S (Inter-IC Sound bus) Interface in FM4 Family Peripheral Manual Communication Macro Part (002-04862) for the details.

[142] Except for the first bit of transmission frame



Note:

- *See Chapter 7-2: I²S (Inter-IC Sound bus) Interface in FM4 Family Peripheral Manual Communication Macro Part (002-04862) for the details of CPOL, FSPH, FSLIN, and SMPL.*



Slave Mode Timing

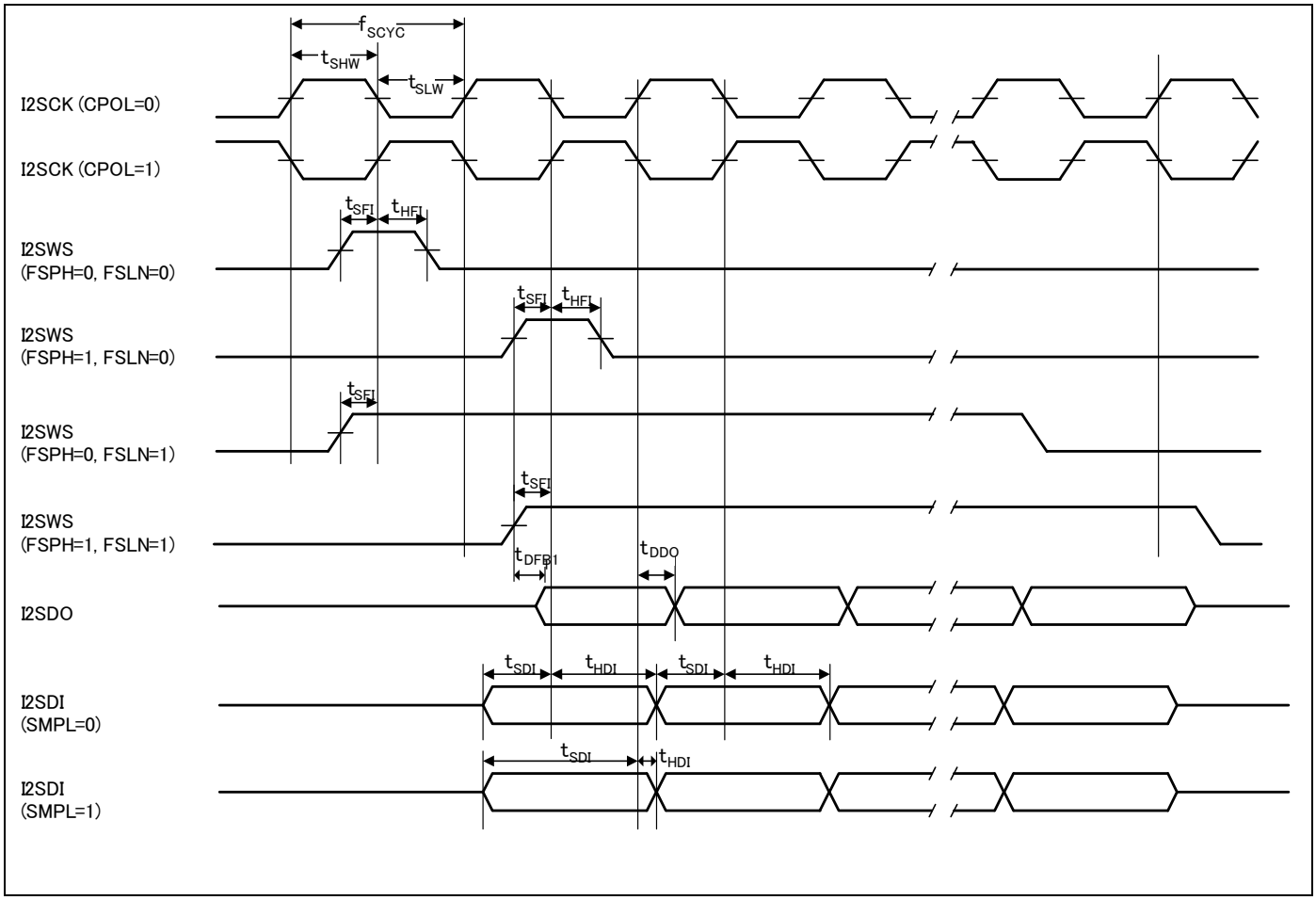
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input frequency	f_{SCYC}	I2SCK	-	-	12.288	MHz	
Input clock pulse width	t_{SHW}	I2SCK	-	45	55	%	
	t_{SLW}			45	55	%	
I2SWS→I2SCK Setup time	t_{SFI}	I2SCK, I2SWS	-	8	-	ns	
I2SWS→I2SCK Hold time	t_{HFI}	I2SCK, I2SWS	-	0	-	ns	
I2SCK ↑ →I2SDO Delay time[143]	t_{DDO}	I2SCK, I2SDO	-	0	32	ns	
I2SCK ↑ →I2SDO Delay Time[144]	t_{DFB1}		-	0	32	ns	
I2SDI→I2SCK ↓ Setup time	t_{SDI}	I2SCK, I2SDI	-	8	-	ns	
I2SDI→I2SCK ↓ Hold time	t_{HDI}		-	0	-	ns	
Input signal rise time	t_{FI}	I2SCK, I2SWS, I2SDI	-	-	5	ns	
Input signal fall time	t_{FI}		-	-	5	ns	

Notes:

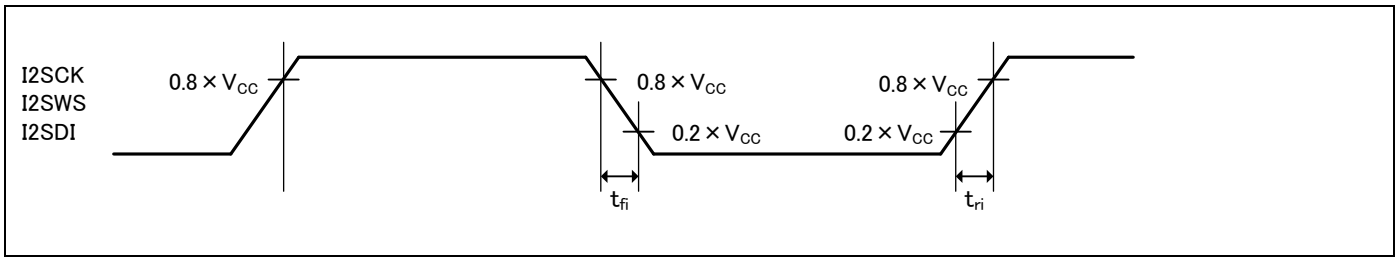
- *When the external load capacitance C_L = 20 pF*
- *When I2SWS = 48 kHz, I2MCLK = 256 × I2SWS*
  Frame synchronization signal (I2SWS) is settable to 48 kHz, 32 kHz, 16 kHz. See Chapter 7-2: I^2S (Inter-IC Sound bus) Interface in FM4 Family Peripheral Manual Communication Macro Part (002-04862) for the details.

[143] Except for the first bit of transmission frame
[144] When FSPH bit = 1.



Notes:

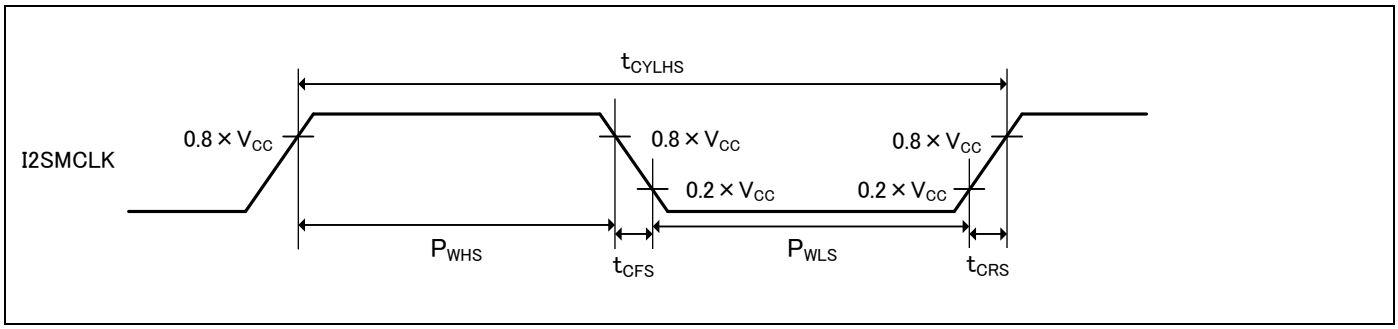
- *See Chapter 7-2: I²S (Inter-IC Sound bus) Interface in FM4 Family Peripheral Manual Communication Macro Part (002-04862) for the details of FSPH, FSLN, SMPL*
- *I2SCK input is selectable polarity by CPOL bit of CNTREG register*



I2SMCLK Input Characteristics

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input frequency	f_{CHS}	I2SMCK	-	-	25	MHz	
Input clock cycle	t_{CYLHS}	-	-	40	-	ns	
Input clock pulse width	-	-	P_{WHS}/t_{CYLHS} P_{WLS}/t_{CYLHS}	45	55	%	When using external clock
Input clock rise time and fall time	t_{CFS} t_{CRS}	-	-	-	5	ns	When using external clock



I2SMCLK Output Characteristics

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Output frequency	f_{CHS}	I2SMCK	-	-	12.288	MHz	

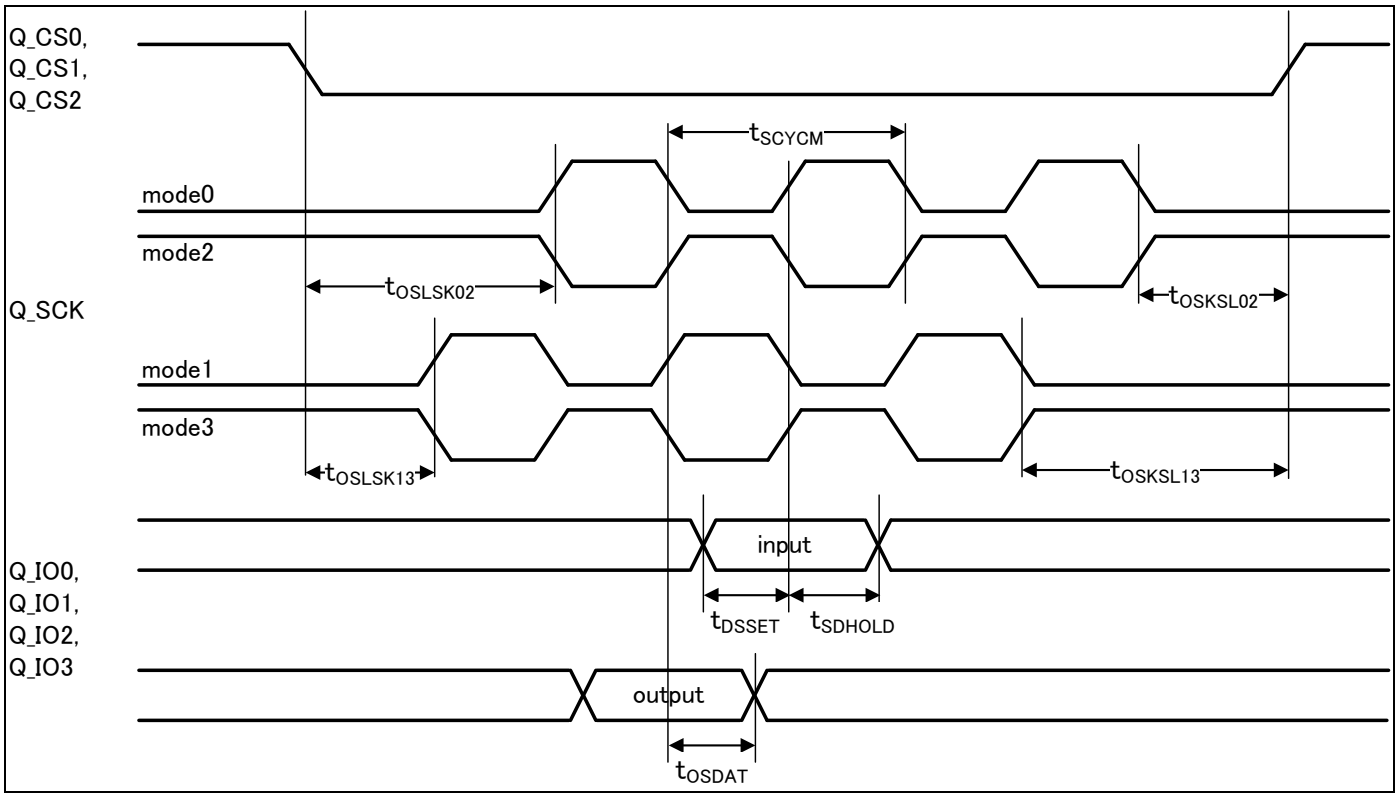
12.4.21 High-Speed Quad SPI Timing

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock frequency	t_{SCYCM}	Q_SCK_0	C_L = 15 pF, V_{CC} = 3.0 to 3.6V	-	66	MHz	When RTM = 1 and mode = 0, 1, 3
			C_L = 30 pF	-	50	MHz	When RTM = 1 and mode = 2 or RTM = 0 and mode = 0, 1, 2, 3
Enabled CS→ CLK Starting Time (mode0/mode2)	$t_{OSLSK02}$	Q_SCK_0, Q_CS0_0, Q_CS1_0, Q_CS2_0	C_L = 30 pF	$1.5 \times t_{SCYCM}$ - 5	-	ns	
Enabled CS→ CLK Starting Time (mode1/mode3)	$t_{OSLSK13}$			t_{SCYCM} - 5	-	ns	
CLK Last→ Disabled CS Time (mode0/mode2)	$t_{OSKSL02}$			t_{SCYCM}	-	ns	
CLK Last→ Disabled CS Time (mode1/mode3)	$t_{OSKSL13}$			$1.5 \times t_{SCYCM}$	-	ns	
SIO Data output time	t_{OSDAT}	Q_SCK_0, Q_IO0_0, Q_IO1_0, Q_IO2_0, Q_IO3_0	C_L = 15 pF, V_{CC} = 3.0 to 3.6V	0	5	ns	
			C_L = 30 pF	0	5		
SIO Setup	t_{DSSET}		C_L = 30 pF	3	-	ns	When RTM = 1 and mode = 0, 1, 3
				10	-		When RTM = 1 and mode = 2 or RTM = 0 and mode = 0, 1, 2, 3
SIO Hold	t_{SDHOLD}		C_L = 30 pF	$0.5 \times t_{SCYCM}$	-	ns	

Notes:

- *See Chapter 8-3: High-Speed Quad SPI controller in FM4 Family Peripheral Manual Communication Macro Part (002-04862) for the detail of RTM mode.*
- *When using High-Speed Quad SPI, please set PDSR register to set the pin drive capability for V_{CC} = 3V. See Chapter 12: I/O Port in FM4 Family Peripheral Manual Main Part (002-04856) for the details.*


Q_CS0,
Q_CS1,
Q_CS2
tSCYCM
mode0
mode2
tOSLSK02
tOSKSL02
Q_SCK
mode1
mode3
tOSLSK13
tOSKSL13
input
Q_IO0,
Q_IO1,
Q_IO2,
Q_IO3
tDSSET
tSDHOLD
output
tOSDAT

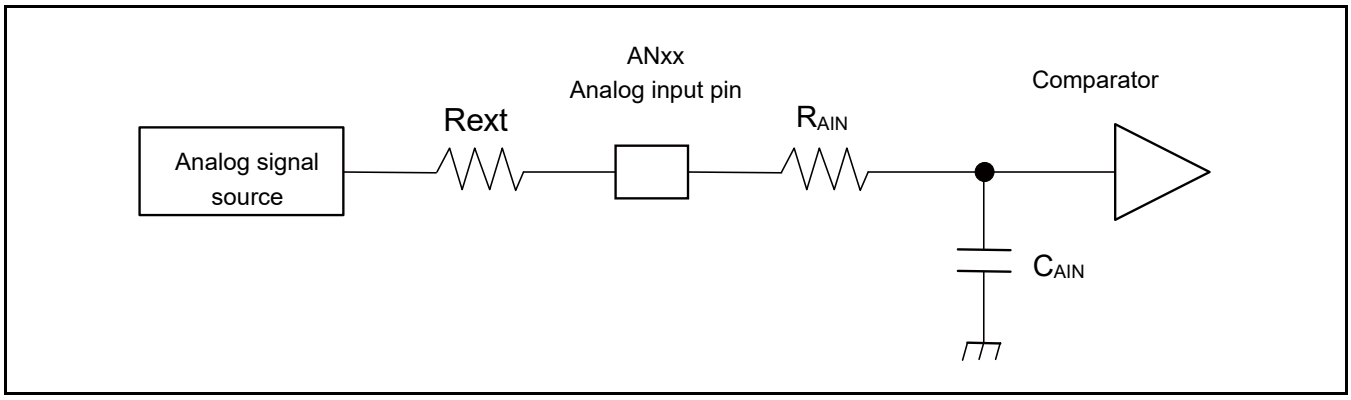
12.5 12-bit A/D Converter

Electrical Characteristics for the A/D Converter

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = AVRL = 0V)

Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	12	bit	
Integral nonlinearity	-	-	- 4.5	-	+ 4.5	LSB	AVRH = 2.7V to 5.5V
Differential nonlinearity	-	-	- 2.5	-	+ 2.5	LSB	
Zero transition voltage	V_{ZT}	ANxx	- 15	-	+ 15	mV	
Full-scale transition voltage	V_{FST}	ANxx	AVRH – 15	-	AVRH + 15	mV	
			AV_{CC} - 15	-	AV_{CC} + 15	mV	
Conversion time	-	-	0.5[145]	-	-	µs	AV_{CC} ≥ 4.5V
Sampling time[146]	t_S	-	0.15	-	10	µs	AV_{CC} ≥ 4.5V
			0.3	-			AV_{CC} < 4.5V
Compare clock cycle[147]	t_{CCK}	-	25	-	1000	ns	AV_{CC} ≥ 4.5V
			50	-	1000		AV_{CC} < 4.5V
State transition time to operation permission	t_{STT}	-	-	-	1.0	µs	
Power supply current (analog + digital)	-	AVCC	-	0.69	0.92	mA	A/D 1 unit operation
			-	1.3	22	µA	When A/D stop
Reference power supply current (AVRH)	-	AVRH	-	1.1	1.97	mA	A/D 1 unit operation AVRH = 5.5V
			-	0.3	6.3	µA	When A/D stop
Analog input capacity	C_{AIN}	-	-	-	12.05	pF	
Analog input resistance	R_{AIN}	-	-	-	1.2	kΩ	AV_{CC} ≥ 4.5V
					1.8		AV_{CC} < 4.5V
Interchannel disparity	-	-	-	-	4	LSB	
Analog port input leak current	-	ANxx	-	-	5	µA	
Analog input voltage	-	ANxx	AV_{SS}	-	AVRH	V	
			AV_{SS}	-	AV_{CC}	V	
Reference voltage	-	AVRH	4.5	-	AV_{CC}	V	Tcck ＜50 ns
			2.7	-	AV_{CC}		Tcck ≥ 50 ns
	-	AVRL	AV_{SS}	-	AV_{SS}	V	

[145] The conversion time is the value of sampling time (t_S) + compare time (t_C).
The condition of the minimum conversion time is when the value of T_s = 150 ns and T_c = 350 ns (AV_{CC} ≥ 4.5V). Ensure that it satisfies the value of sampling time (t_S) and compare clock cycle (t_{CCK}).
For setting of sampling time and compare clock cycle, see Chapter 1-1: A/D Converter in FM4 Family Peripheral Manual Analog Macro Part (002-04860). The register setting of the A/D converter is reflected by the APB bus clock timing. For more information about the APB bus number to which the A/D converter is connected, see 1 Block Diagram in this data sheet.
The sampling clock and compare clock are set at base clock (HCLK).
[146] A necessary sampling time changes by external impedance. Ensure that it sets the sampling time to satisfy (Equation 1).
[147] The compare time (t_C) is the value of (Equation 2).



(Equation 1) $t_S \geq (R_{AIN} + R_{ext}) \times C_{AIN} \times 9$

t_S: Sampling time

R_{AIN}: Input resistance of A/D = 1.2 kΩ at 4.5V ≤ AV_{CC} ≤ 5.5V

Input resistance of A/D = 1.8 kΩ at 2.7V ≤ AV_{CC} < 4.5V

C_{AIN}: Input capacity of A/D = 12.05 pF at 2.7V ≤ AV_{CC} ≤ 5.5V

R_{ext}: Output impedance of external circuit

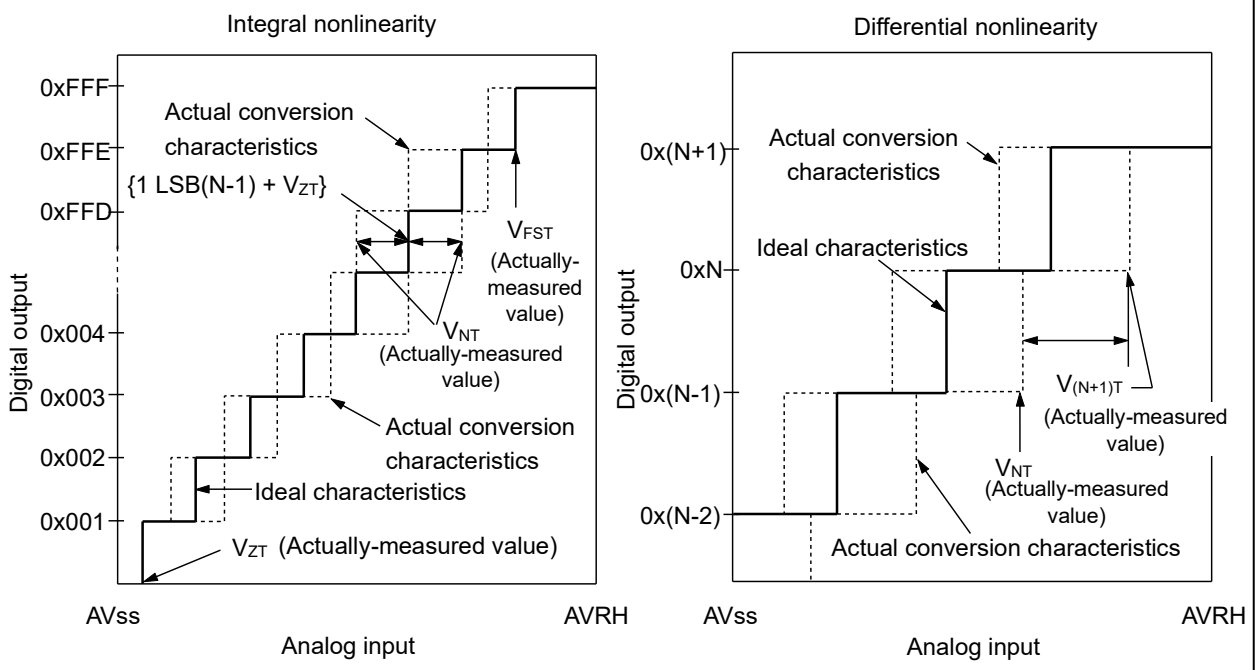
(Equation 2) $t_C = t_{CCK} \times 14$

t_C: Compare time

t_{CCK}: Compare clock cycle

Definition of 12-bit A/D Converter Terms

- Resolution: Analog variation that is recognized by an A/D converter.
- Integral nonlinearity: Deviation of the line between the zero-transition point (0b000000000000 ⟷ 0b000000000001) and the full-scale transition point (0b111111111110 ⟷ 0b111111111111) from the actual conversion characteristics.
- Differential nonlinearity: Deviation from the ideal value of the input voltage that is required to change the output code by 1 LSB.



$$\text{Integral nonlinearity of digital output N} = \frac{V_{NT} - \{1LSB \times (N - 1) + V_{ZT}\}}{1LSB} \text{ [LSB]}$$

$$\text{Differential nonlinearity of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1LSB} - 1 \text{ [LSB]}$$

$$1LSB = \frac{V_{FST} - V_{ZT}}{4094}$$

N: A/D converter digital output value.
V_{ZT}: Voltage at which the digital output changes from 0x000 to 0x001.
V_{FST}: Voltage at which the digital output changes from 0xFFE to 0xFFF.
V_{NT}: Voltage at which the digital output changes from 0x(N − 1) to 0xN.

12.6 12-bit D/A Converter

Electrical Characteristics for the D/A Converter

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	DAx	-	-	12	bit	
Conversion time	t_{C20}		0.56	0.69	0.81	µs	Load 20 pF
	t_{C100}		2.79	3.42	4.06	µs	Load 100 pF
Integral nonlinearity[148]	INL		- 16	-	+ 16	LSB	
Differential nonlinearity[148]	DNL		- 0.98	-	+ 1.5	LSB	
Output voltage offset	V_{OFF}		-	-	+ 10	mV	When setting 0x000
			- 20.0	-	+ 1.4	mV	When setting 0xFFF
Analog output impedance	R_O		3.10	3.80	4.50	kΩ	D/A operation
			2.0	-	-	MΩ	When D/A stop
Power supply current[148]	IDDA	AVCC	260	330	410	µs	D/A 1ch operation AV_{CC} = 3.3V
			400	510	620	µs	D/A 1ch operation AV_{CC} = 5.0V
	IDSA		-	-	14	µs	When D/A stop

[148] During no load

12.7 USB Characteristics

(V_{CC} = AV_{CC} = 2.7V to 5.5V, $USBV_{CC}0$ = $USBV_{CC}1$ = 3.0V to 3.6V, V_{SS} = AV_{SS} = 0V)

Parameter		Symbol	Pin Name	Conditions	Value		Unit	Reference
					Min	Max		
Input characteristics	Input H level voltage	V_{IH}	UDP0/ UDM0, UDP1/ UDM1	-	2.0	$USBV_{CC}$ + 0.3	V	1
	Input L level voltage	V_{IL}		-	V_{SS} - 0.3	0.8	V	1
	Differential input sensitivity	V_{DI}		-	0.2	-	V	2
	Different common mode range	V_{CM}		-	0.8	2.5	V	2
Output characteristics	Output H level voltage	V_{OH}		External pull-down resistance = 15 kΩ	2.8	3.6	V	3
	Output L level voltage	V_{OL}		External pull-up resistance = 1.5 kΩ	0.0	0.3	V	3
	Crossover voltage	V_{CRS}		-	1.3	2.0	V	4
	Rise time	t_{FR}		Full-Speed	4	20	ns	5
	Fall time	t_{FF}		Full-Speed	4	20	ns	5
	Rise/fall time matching	t_{FRFM}		Full-Speed	90	111.11	%	5
	Output impedance	Z_{DRV}		Full-Speed	28	44	Ω	6
	Rise time	t_{LR}		Low-Speed	75	300	ns	7
	Fall time	t_{LF}		Low-Speed	75	300	ns	7
	Rise/fall time matching	t_{LRFM}		Low-Speed	80	125	%	7

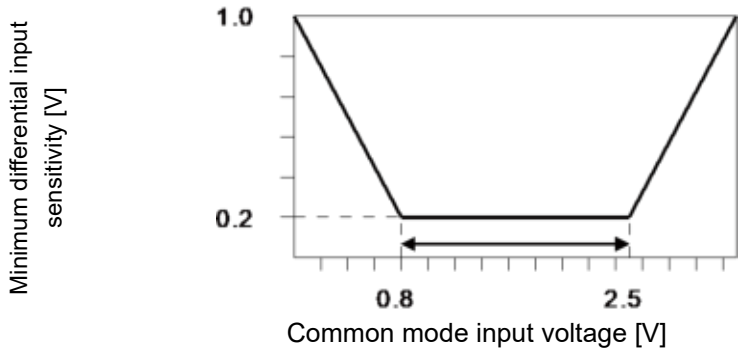
References:

1: The switching threshold voltage of the single-end-receiver of USB I/O buffer is set as within V_{IL} (Max) = 0.8V, V_{IH} (Min) = 2.0V (TTL input standard).

There is some hysteresis applied to lower noise sensitivity.

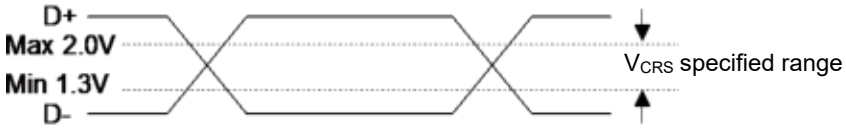
2: Use differential-receiver to receive USB differential data signal. Differential-receiver has 200 mV of differential input sensitivity when the differential data input is within 0.8V to 2.5V to the local ground reference level.

Above voltage range is the common mode input voltage range.

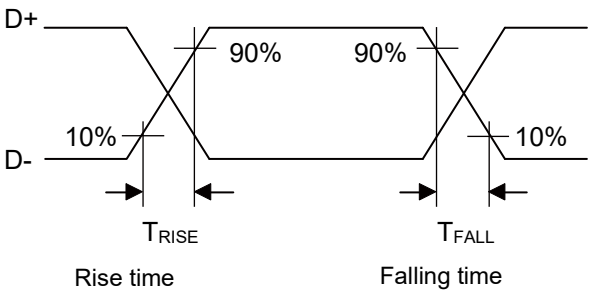


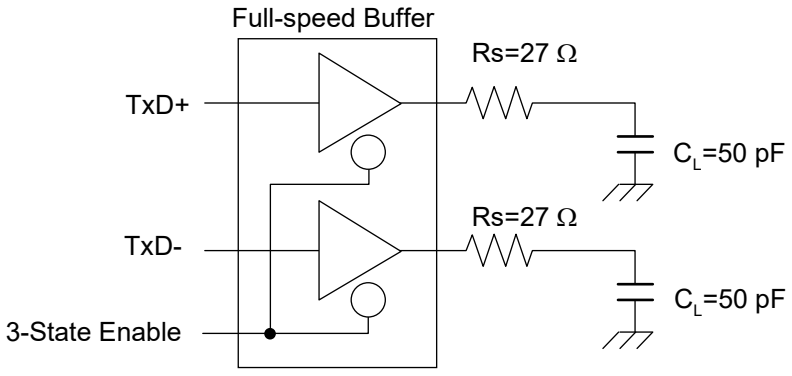
3: The output drive capability of the driver is below 0.3V at low state (V_{OL}) (to 3.6V and 1.5 kΩ load), and 2.8V or above (to the VSS and 1.5 kΩ load) at high state (V_{OH}).

4: The cross voltage of the external differential output signal (D +/D −) of USB I/O buffer is within 1.3V to 2.0V.

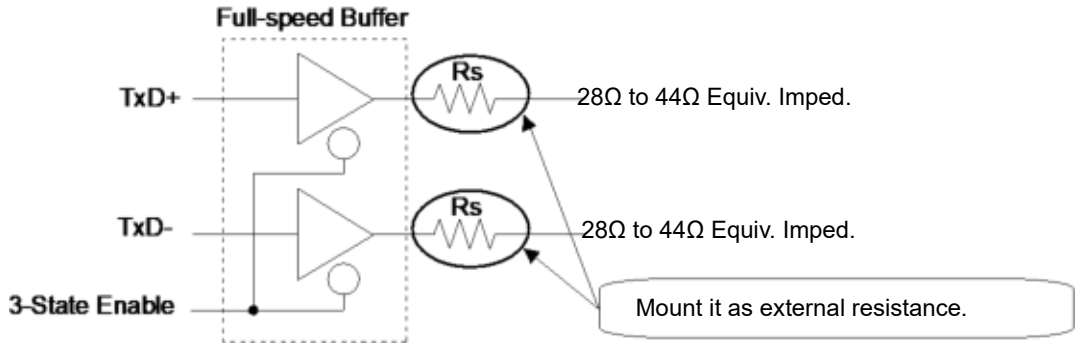


5: They indicate rise time (t_{RISE}) and fall time (t_{FALL}) of the full-speed differential data signal.
They are defined by the time between 10% and 90% of the output signal voltage.
For full-speed buffer, t_R/t_F ratio is regulated as within ± 10% to minimize RFI emission.



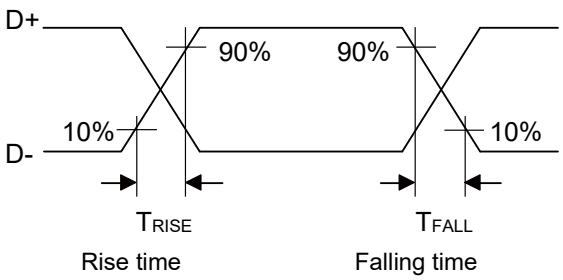


6: USB Full-speed connection is performed via twisted-pair cable shield with 90Ω ± 15% characteristic impedance (differential mode).
USB standard defines that the output impedance of the USB driver must be in the range from 28 Ω to 44 Ω. So, a discrete series resistor (Rs) addition is defined in order to satisfy the above definition and keep balance.
When using this USB I/O, use it with 25 Ω to 30 Ω (recommended value 27 Ω) series resistor Rs.



Rs series resistor 25Ω to 30Ω
Series resistor of 27Ω (recommendation value) must be added.
And, use "resistance with an uncertainty of 5% by E24 sequence."

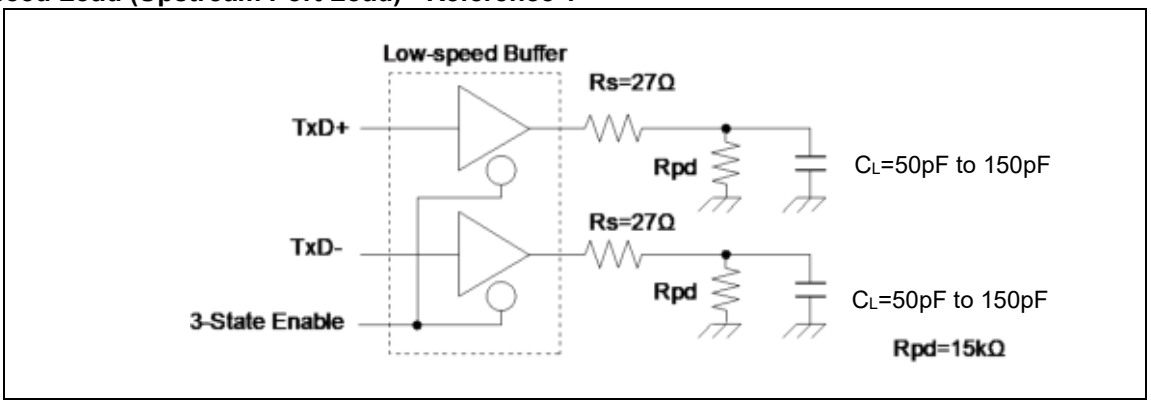
7: They indicate rise time (t_{RISE}) and fall time (t_{FALL}) of the low-speed differential data signal.
They are defined by the time between 10% and 90% of the output signal voltage.



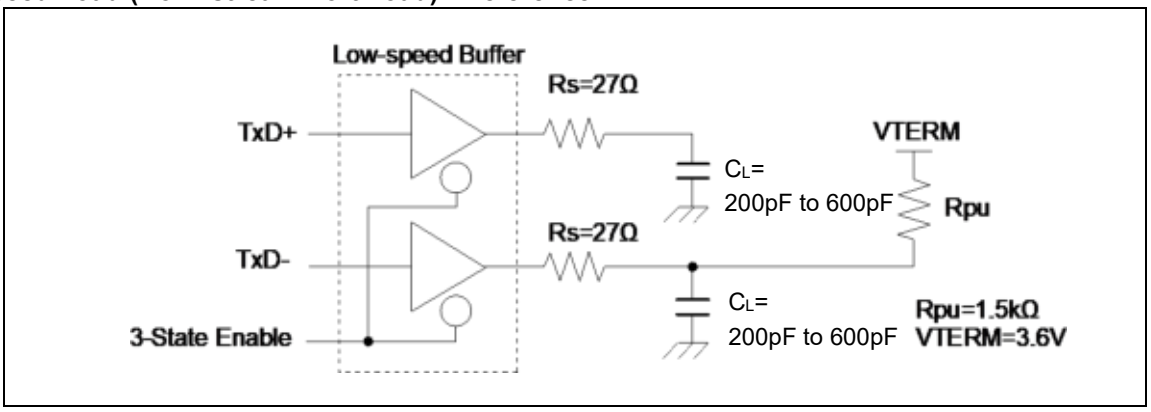
Note:

- *See Low-Speed Load (Compliance Load) for conditions of external load.*

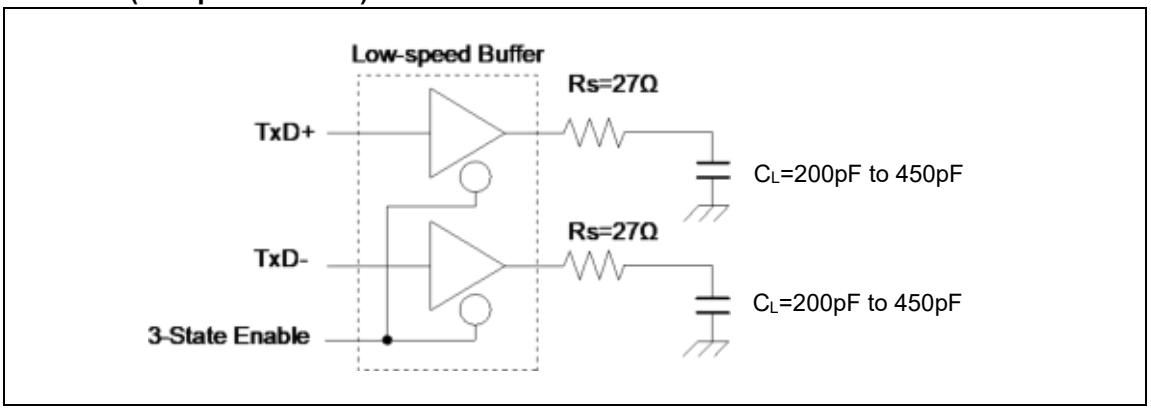
Low-Speed Load (Upstream Port Load) - Reference 1



Low-Speed Load (Downstream Port Load) - Reference 2



Low-Speed Load (Compliance Load)



12.8 Low-Voltage Detection Characteristics

12.8.1 Low-Voltage Detection Reset

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	-	2.46	2.55	2.64	V	When voltage drops
Released voltage	VDH	-	2.51	2.60	2.69	V	When voltage rises

12.8.2 Interrupt of Low-Voltage Detection

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	SVHI = 00111	2.80	2.90	3.00	V	When voltage drops
Released voltage	VDH		2.90	3.00	3.11	V	When voltage rises
Detected voltage	VDL	SVHI = 00100	2.99	3.10	3.21	V	When voltage drops
Released voltage	VDH		3.09	3.20	3.31	V	When voltage rises
Detected voltage	VDL	SVHI = 01100	3.18	3.30	3.42	V	When voltage drops
Released voltage	VDH		3.28	3.40	3.52	V	When voltage rises
Detected voltage	VDL	SVHI = 01111	3.67	3.80	3.93	V	When voltage drops
Released voltage	VDH		3.76	3.90	4.04	V	When voltage rises
Detected voltage	VDL	SVHI = 01110	3.76	3.90	4.04	V	When voltage drops
Released voltage	VDH		3.86	4.00	4.14	V	When voltage rises
Detected voltage	VDL	SVHI = 01001	4.05	4.20	4.35	V	When voltage drops
Released voltage	VDH		4.15	4.30	4.45	V	When voltage rises
Detected voltage	VDL	SVHI = 01000	4.15	4.30	4.45	V	When voltage drops
Released voltage	VDH		4.25	4.40	4.55	V	When voltage rises
Detected voltage	VDL	SVHI = 11000	4.25	4.40	4.55	V	When voltage drops
Released voltage	VDH		4.34	4.50	4.66	V	When voltage rises
LVD stabilization wait time	t_{LVDW}	-	-	-	$6000 \times t_{CYCP}$ [149]	µs	

[149] t_{CYCP} indicates the APB2 bus clock cycle time.

12.9 MainFlash Memory Write/Erase Characteristics

(V_{CC} = 2.7V to 5.5V)

Parameter		Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time	Large Sector	-	0.7	3.7	s	Includes write time prior to internal erase
	Small Sector	-	0.3	1.1	s	
Half word (16-bit) write time	Write cycles ≤ 100 times	-	12	100	µs	Not including system-level overhead time
	Write cycles > 100 times			200		
Chip erase time[150]		-	13.6	68	s	Includes write time prior to internal erase

Write Cycles and Data Retention Time

Erase/Write Cycles (Cycle)	Data Retention Time (Year)
1,000	20[151]
10,000	10[151]
100,000	5[151]

12.10 Dual Flash Memory Write/Erase Characteristics

It is the same write/erase characteristics as the MainFlash memory.

See 3.6 Dual flash mode in this product's Flash Programming Manual for the detail of dual flash mode.

[150] It indicates the chip erase time of 1 MB MainFlash memory
For devices with 1.5 MB or 2 MB of MainFlash memory, two erase cycles are required.
See 3.2.2 Command Operating Explanations and 3.3.3 Flash Erase Operation in this product's Flash Programming Manual for the detail.

[151] This value comes from the technology qualification (using Arrhenius equation to translate high temperature acceleration test result into average temperature value at + 85°C).

12.11 Standby Recovery Time

12.11.1 Recovery Cause: Interrupt/WKUP

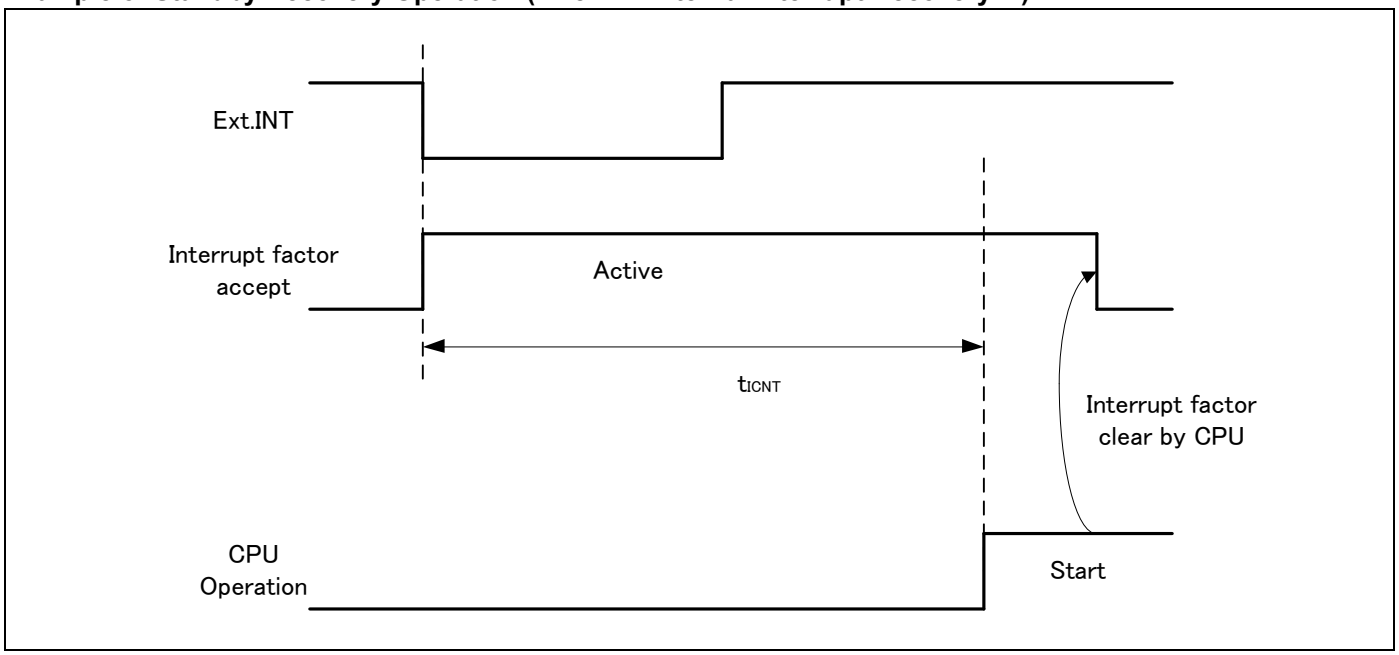
The time from the interrupt occurring to the time of program operation start is shown.

Recovery Count Time

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

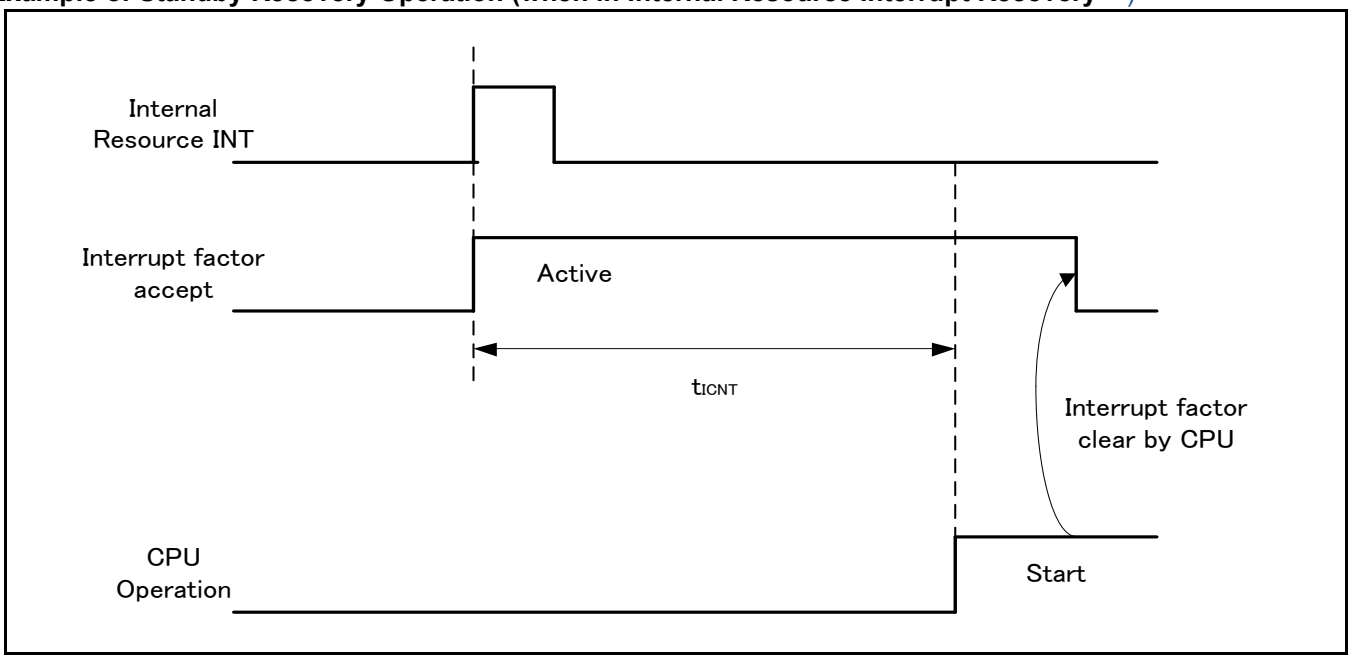
Parameter	Symbol	Value		Unit	Remarks
		Typ	Max[152]		
Sleep mode	t_{ICNT}	HCLK×1		µs	
High-speed CR Timer mode Main Timer mode PLL Timer mode		40	80	µs	
Low-speed CR Timer mode		450	900	µs	
Sub Timer mode		896	1136	µs	
RTC mode Stop mode (High-speed CR/Main/PLL Run mode return)		316	581	µs	
RTC mode Stop mode (Low-speed CR/sub Run mode return)		270	540	µs	
Deep Standby RTC mode with RAM retention		365	667	µs	without RAM retention
Deep Standby Stop mode with RAM retention		365	667	µs	with RAM retention

Example of Standby Recovery Operation (when in External Interrupt Recovery[153])



[152] The maximum value depends on the built-in CR accuracy.
[153] External interrupt is set to detecting fall edge.

Example of Standby Recovery Operation (when in Internal Resource Interrupt Recovery[154])



Notes:

- *The return factor is different in each low-power consumption mode. See Chapter 6: Low Power Consumption mode and Operations of Standby modes in FM4 Family Peripheral Manual Main Part (002-04856).*
- *The recovery process is unique for each operating mode. See Chapter 6: Low Power Consumption mode in FM4 Family Peripheral Manual Main Part (002-04856).*

[154] Depending on the standby mode, interrupt from the internal resource is not included in the recovery cause.

12.11.2 Recovery Cause: Reset

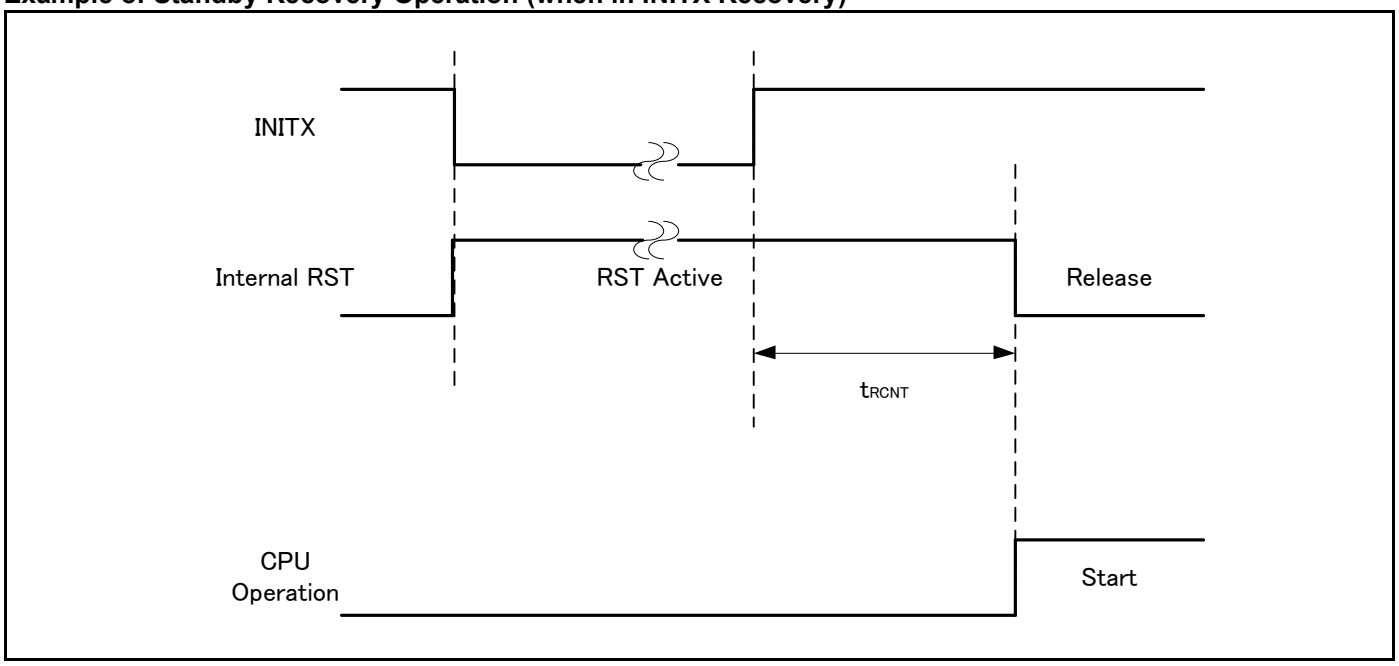
The time from reset release to the program operation start is shown.

Recovery Count Time

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

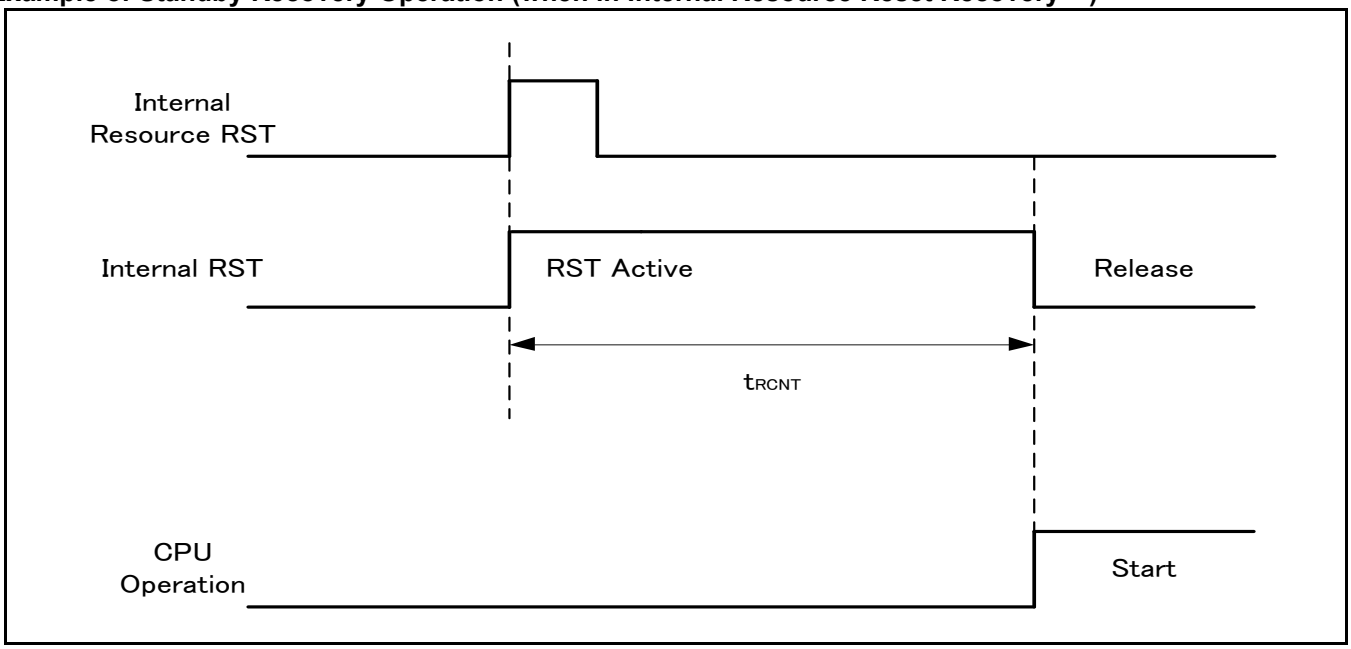
Parameter	Symbol	Value		Unit	Remarks
		Typ	Max[155]		
Sleep mode	t_{RCNT}	155	266	µs	
High-speed CR Timer mode Main Timer mode PLL Timer mode		155	266	µs	
Low-speed CR Timer mode		315	567	µs	
Sub Timer mode		315	567	µs	
RTC mode Stop mode		315	567	µs	
Deep Standby RTC mode with RAM retention		336	667	µs	without RAM retention
Deep Standby Stop mode with RAM retention		336	667	µs	with RAM retention

Example of Standby Recovery Operation (when in INITX Recovery)



[155] The maximum value depends on the built-in CR accuracy.

Example of Standby Recovery Operation (when in Internal Resource Reset Recovery[156])

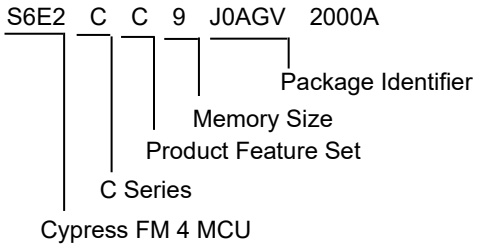


Notes:

- *The return factor is different in each low power consumption mode.*
  See Chapter 6: Low Power Consumption mode and Operations of Standby modes in "FM4 Family Peripheral Manual Main Part (002-04856).
- *The recovery process is unique for each operating mode. See Chapter 6: Low Power Consumption mode in FM4 Family Peripheral Manual Main Part (002-04856).*
- *When the power-on reset/low-voltage detection reset, they are not included in the return factor. See 12.4.8 Power-On Reset Timing.*
- *In recovering from reset, CPU changes to High-speed Run mode. In the case of using the main clock and PLL clock, they need further main clock oscillation stabilization wait time and oscillation stabilization wait time of Main PLL clock.*
- *Internal resource reset indicates Watchdog reset and CSV reset.*

[156] Depending on the low-power consumption mode, the reset issue from the internal resource is not included in the recovery cause.

13. Ordering Information



Part Number	Flash (MB)	RAM (KB)	USB 2.0	CAN/ CAN FD	Ethernet-MAC	Package
S6E2CC8H0AGV2000A	1	128	2ch	2ch/1ch	1ch (max) MII: 1ch RII: 1ch (max)	Plastic LQFP (0.5 mm pitch), 144 pin (LQS144)
S6E2C58H0AGV2000A	1	128	2ch	2ch/1ch	N/A	
S6E2C59H0AGV2000A	1.5	192	2ch	2ch/1ch	N/A	
S6E2C5AH0AGV2000A	2	256	2ch	2ch/1ch	N/A	
S6E2C18H0AGV2000A	1	128	N/A	N/A	N/A	
S6E2C19H0AGV2000A	1.5	192	N/A	N/A	N/A	
S6E2C1AH0AGV2000A	2	256	N/A	N/A	N/A	
S6E2C28H0AGV2000A	1	128	2ch	N/A	1ch (max) MII: 1ch RII: 1ch (max)	
S6E2C29H0AGV2000A	1.5	192	2ch	N/A	1ch (max) MII: 1ch RII: 1ch (max)	
S6E2C2AH0AGV2000A	2	256	2ch	N/A	1ch (max) MII: 1ch RII: 1ch (max)	
S6E2C38H0AGV2000A	1	128	2ch	N/A	N/A	
S6E2C39H0AGV2000A	1.5	192	2ch	N/A	N/A	
S6E2C48H0AGV2000A	1	128	N/A	2ch/1ch	N/A	
S6E2C49H0AGV2000A	1.5	192	N/A	2ch/1ch	N/A	

Part Number	Flash (MB)	RAM (KB)	USB 2.0	CAN/ CAN FD	Ethernet-MAC	Package
S6E2C4AH0AGV2000A	2	256	N/A	2ch/1ch	N/A	
S6E2CC9H0AGV2000A	1.5	192	2ch	2ch/1ch	1ch (max) MII: 1ch RII: 1ch (max)	
S6E2CCAHHAGV2000A	2	256	2ch	N/A	N/A	
S6E2CC8J0AGV2000A	1	128	2ch	2ch/1ch	1ch (max) MII: 1ch RII: 1ch (max)	Plastic LQFP (0.5 mm pitch), 176 pin (LQP176)
S6E2CC9J0AGV2000A	1.5	192	2ch	2ch/1ch	1ch (max) MII: 1ch RII: 1ch (max)	
S6E2C58J0AGV2000A	1	128	2ch	2ch/1ch	N/A	
S6E2C59J0AGV2000A	1.5	192	2ch	2ch/1ch	N/A	
S6E2C5AJ0AGV2000A	2	256	2ch	2ch/1ch	N/A	
S6E2C18J0AGV2000A	1	128	N/A	N/A	N/A	
S6E2C19J0AGV2000A	1.5	192	N/A	N/A	N/A	
S6E2C1AJ0AGV2000A	2	256	N/A	N/A	N/A	
S6E2C28J0AGV2000A	1	128	2ch	N/A	1ch (max) MII: 1ch RII: 1ch (max)	
S6E2C29J0AGV2000A	1.5	192	2ch	N/A	1ch (max) MII: 1ch RII: 1ch (max)	
S6E2C2AJ0AGV2000A	2	256	2ch	N/A	1ch (max) MII: 1ch RII: 1ch (max)	
S6E2C38J0AGV2000A	1	128	2ch	N/A	N/A	
S6E2C39J0AGV2000A	1.5	192	2ch	N/A	N/A	

Part Number	Flash (MB)	RAM (KB)	USB 2.0	CAN/ CAN FD	Ethernet-MAC	Package
S6E2C48J0AGV2000A	1	128	N/A	2ch/1ch	N/A	
S6E2C49J0AGV2000A	1.5	192	N/A	2ch/1ch	N/A	
S6E2C4AJ0AGV2000A	2	256	N/A	2ch/1ch	N/A	
S6E2CCAJHAGV2000A	2	256	2ch	N/A	N/A	
S6E2C18J0AGB1000A	1	128	N/A	N/A	N/A	Plastic FBGA (0.8 mm pitch), 192 pin (LBE192)
S6E2C19J0AGB1000A	1.5	192	N/A	N/A	N/A	
S6E2C1AJ0AGB1000A	2	256	N/A	N/A	N/A	
S6E2C28J0AGB1000A	1	128	2ch	N/A	1ch (max) MII: 1ch RII: 1ch (max)	
S6E2C29J0AGB1000A	1.5	192	2ch	N/A	1ch (max) MII: 1ch RII: 1ch (max)	
S6E2C2AJ0AGB1000G	2	256	2ch	N/A	1ch (max) MII: 1ch RII: 1ch (max)	
S6E2C38J0AGB1000A	1	128	2ch	N/A	N/A	
S6E2C39J0AGB1000A	1.5	192	2ch	N/A	N/A	
S6E2C3AJ0AGB1000A	2	256	2ch	N/A	N/A	
S6E2C48J0AGB1000A	1	128	N/A	2ch/1ch	N/A	
S6E2C49J0AGB1000A	1.5	192	N/A	2ch/1ch	N/A	

Part Number	Flash (MB)	RAM (KB)	USB 2.0	CAN/ CAN FD	Ethernet-MAC	Package
S6E2C4AJ0AGB1000A	2	256	N/A	2ch/1ch	N/A	
S6E2C58J0AGB1000A	1	128	2ch	2ch/1ch	N/A	
S6E2C59J0AGB1000A	1.5	192	2ch	2ch/1ch	N/A	
S6E2C5AJ0AGB1000A	2	256	2ch	2ch/1ch	N/A	
S6E2CC8J0AGB1000A	1	128	2ch	2ch/1ch	1ch (max) MII: 1ch RII: 1ch (max)	
S6E2CC9J0AGB1000A	1.5	192	2ch	2ch/1ch	1ch (max) MII: 1ch RII: 1ch (max)	
S6E2CCAJ0AGB1000A	2	256	2ch	2ch/1ch	1ch (max) MII: 1ch RII: 1ch (max)	
S6E2CCAJHAGB1000A	2	256	2ch	2ch/1ch	1ch (max) MII: 1ch RII: 1ch (max)	
S6E2C18L0AGL2000A	1	128	N/A	N/A	N/A	
S6E2C19L0AGL2000A	1.5	192	N/A	N/A	N/A	
S6E2C1AL0AGL2000A	2	256	N/A	N/A	N/A	
S6E2C28L0AGL2000A	1	128	2ch	N/A	1ch (max) MII: 1ch RII: 1ch (max)	Plastic LQFP (0.4 mm pitch), 216 pin (LQQ216)
S6E2C29L0AGL2000A	1.5	192	2ch	N/A	1ch (max) MII: 1ch RII: 1ch (max)	
S6E2C2AL0AGL2000G	2	256	2ch	N/A	1ch (max) MII: 1ch RII: 1ch (max)	
S6E2C38L0AGL2000A	1	128	2ch	N/A	N/A	

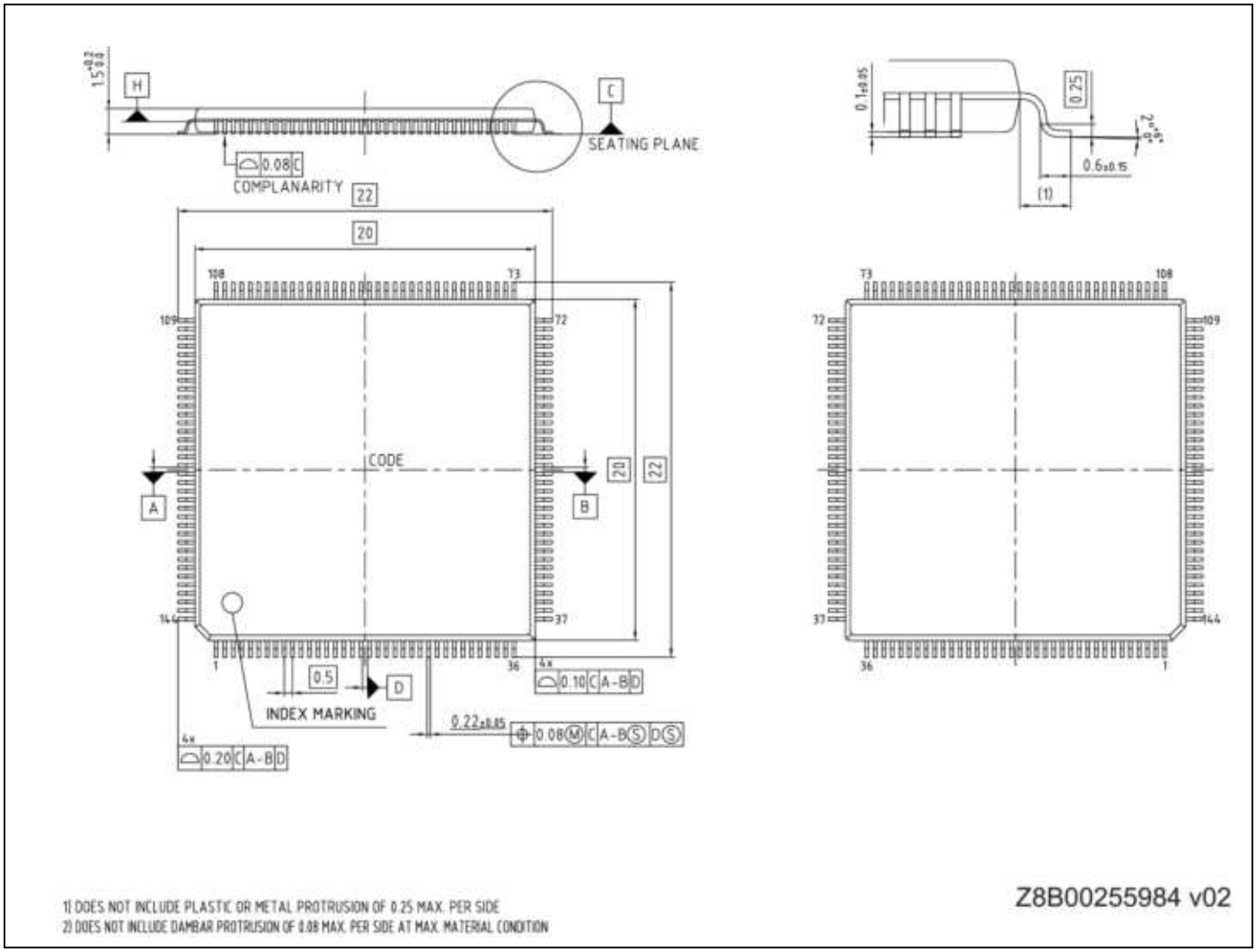
Part Number	Flash (MB)	RAM (KB)	USB 2.0	CAN/ CAN FD	Ethernet-MAC	Package
S6E2C39L0AGL2000A	1.5	192	2ch	N/A	N/A	
S6E2C3AL0AGL2000A	2	256	2ch	N/A	N/A	
S6E2C48L0AGL2000A	1	128	N/A	2ch/1ch	N/A	
S6E2C49L0AGL2000A	1.5	192	N/A	2ch/1ch	N/A	
S6E2C4AL0AGL2000A	2	256	N/A	2ch/1ch	N/A	
S6E2C58L0AGL2000A	1	128	2ch	2ch/1ch	N/A	
S6E2C59L0AGL2000A	1.5	192	2ch	2ch/1ch	N/A	
S6E2C5AL0AGL2000A	2	256	2ch	2ch/1ch	N/A	
S6E2CC8L0AGL2000A	1	128	2ch	2ch/1ch	1ch (max) MII: 1ch RII: 1ch (max)	
S6E2CC9L0AGL2000A	1.5	192	2ch	2ch/1ch	1ch (max) MII: 1ch RII: 1ch (max)	
S6E2CCAL0AGL2000A	2	256	2ch	2ch/1ch	1ch (max) MII: 1ch RII: 1ch (max)	

14. Acronyms

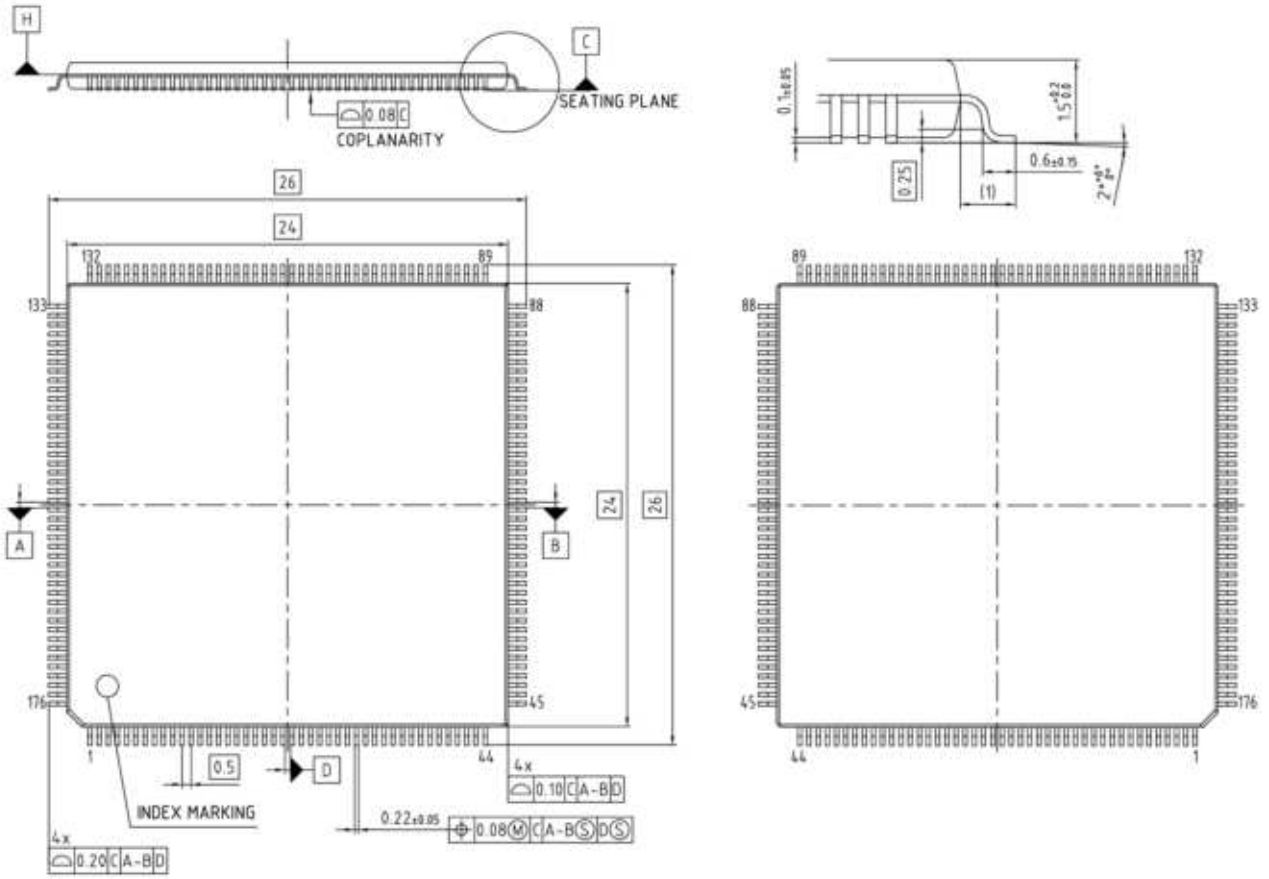
Acronym	Description
ADC	analog-to-digital converter
ACK	acknowledge
AHB	AMBA (advanced microcontroller bus architecture) high-performance bus, an ARM data transfer bus
ARM®	Advanced RISC Machine, a CPU architecture
CEC	Consumer Electronics Control, a command and control interface over HDMI (High Definition Multimedia Interface)
CMOS	complementary metal oxide semiconductor
CPU	central processing unit
CR	clock and reset
CRC	cyclic redundancy check, an error-checking protocol
CSIO	clock synchronous serial interface
CSV	clock supervisor
CTS	clear to send, a flow control signal in some data communication interfaces
DTSC	descriptor system data transfer controller
EOM	end of message
FIFO	first in, first out
GPIO	general-purpose input/output
HDMI	High Definition Multimedia Interface
HDMI-CEC	High Definition Multimedia Interface - Consumer Electronics Control, see CEC
I/F	interface
I^2C, or IIC	Inter-Integrated Circuit, a communications protocol
I^2S, or IIS	Inter-IC (integrated circuit) Sound, a communications protocol
I/O	input/output, see also GPIO
IRQ	interrupt request
LIN	Local Interconnect Network, a communications protocol
LVD	low-voltage detect
MFS	multi-function serial
MSB	most significant byte
MTB	micro trace buffer
NMI	non-maskable interrupt
NVIC	nested vectored interrupt controller
OS	operating system
OSC	oscillator
PLL	phase-locked loop
PPG	programmable pulse generator
PWC	pulse-width counter
PWM	pulse-width modulator
RAM	random access memory
RX	receive
RTS	request to send, a flow control signal in some data communication interfaces
SPI	Serial Peripheral Interface, a communications protocol
SRAM	static random access memory
SW-DP	serial wire debug port
TX	transmit
UART	universal asynchronous receiver transmitter
USB	Universal Serial Bus

15. Package Dimensions

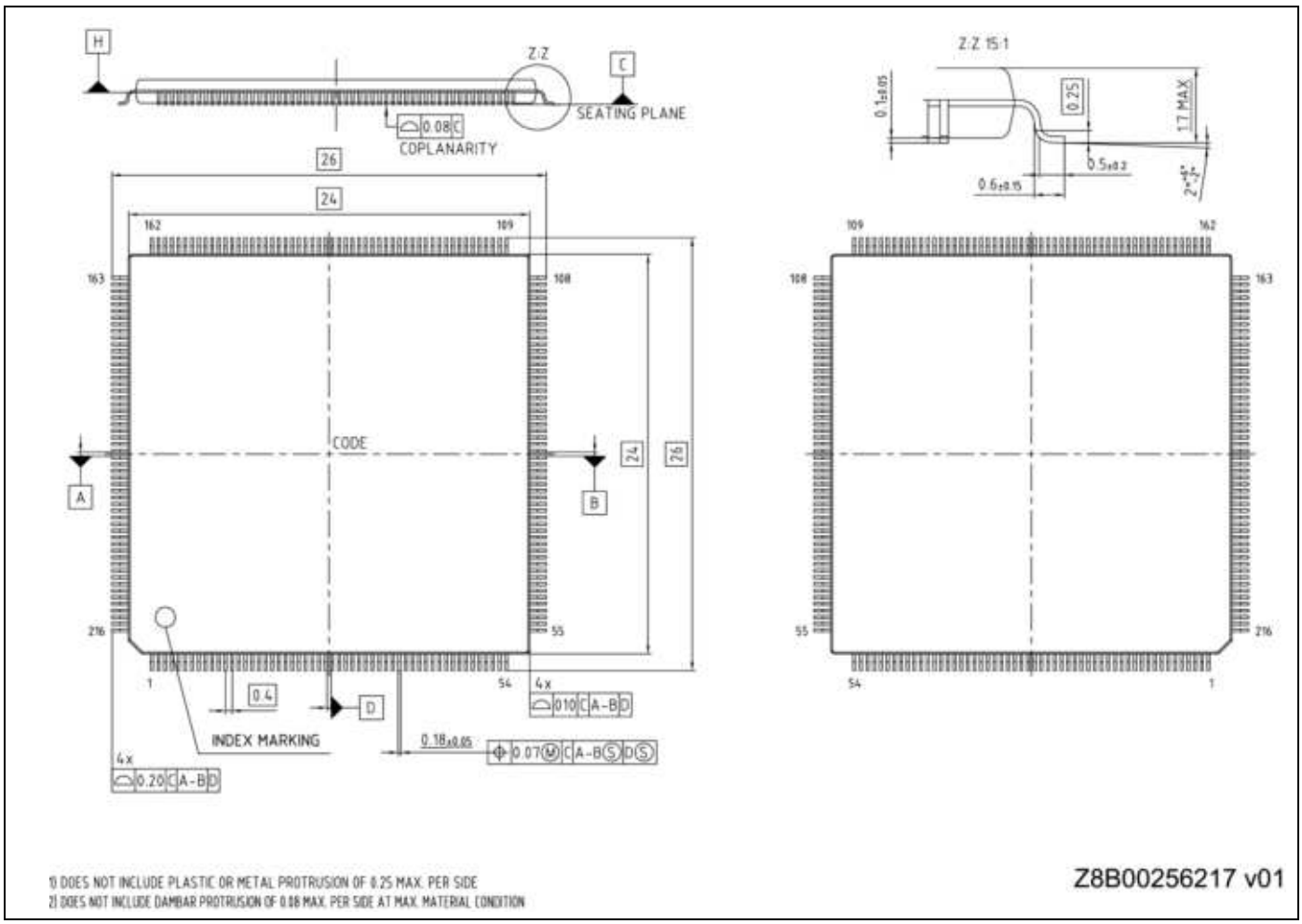
Package Type	Package Code
LQFP 144	LQS 144



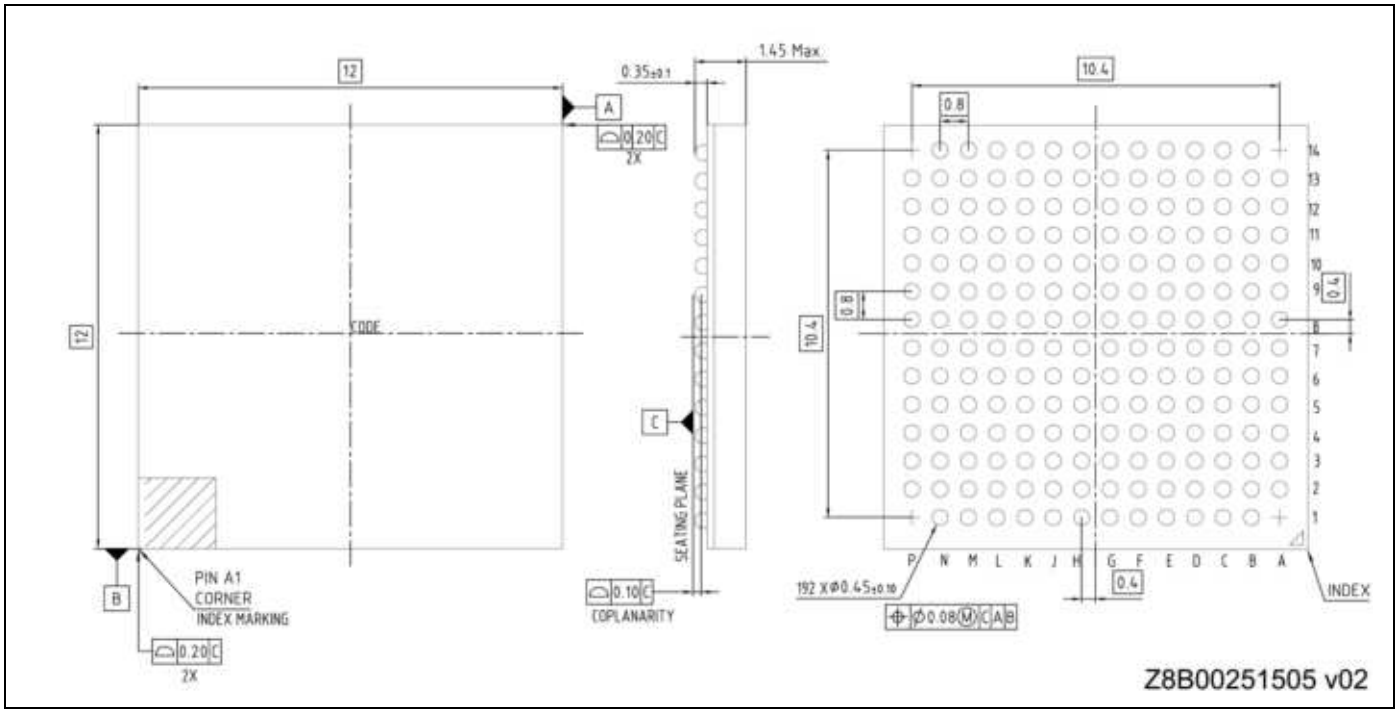
Package Type	Package Code
LQFP 176	LQP 176



Package Type	Package Code
LQFP 216	LQQ 216



Package Type	Package Code
PFBGA 192	LBE 192



16. Major Changes

Spansion Publication Number: DS709-00009

Page	Section	Change Results
Revision 0.1		
-	-	Initial release
Revision 0.2		
1, 3	Title	Added the following products. S6E2CC8HHA/S6E2CC9HHA/S6E2CCAHHA/ S6E2CC8JHA/S6E2CC9JHA/S6E2CCAJHA/ S6E2CC8LHA/S6E2CC9LHA/S6E2CCALHA
14	2.Feature	Added “Crypto Assist Function”
16, 17	3.Product Lineup	Added “Crypto Assist Function”
18	4.Packages	Added the following products. S6E2CC8HHA/S6E2CC9HHA/S6E2CCAHHA/ S6E2CC8JHA/S6E2CC9JHA/S6E2CCAJHA/ S6E2CC8LHA/S6E2CC9LHA/S6E2CCALHA
212	15.ORDERING INFORMATION	Added the following part numbers. S6E2CC8HHAGV20000/S6E2CC9HHAGV20000/S6E2CCAHHAGV2000/ S6E2CC8JHAGV20000/S6E2CC9JHAGV20000/S6E2CCAJHAGV20000/ S6E2CC8JHAGB10000/S6E2CC9JHAGB10000/S6E2CCAJHAGB10000/ S6E2CC8LHAGL20000/S6E2CC9LHAGL20000/S6E2CCALHAGL20000
Revision 0.3		
1, 3	Title	Added the following products. S6E2CCAJGA /S6E2CC8JGA/S6E2CC8JFA/S6E2CCAJFA
14	2.Features	Added Voice Function
15, 16	3.Product Lineup	Added the following products. S6E2CCAJGA /S6E2CC8JGA/S6E2CC8JFA/S6E2CCAJFA
17	4.Packages	Added the following products. S6E2CCAJGA /S6E2CC8JGA/S6E2CC8JFA/S6E2CCAJFA
211	15.Ordering Information	Added the following products. S6E2CCAJGAGV20000/ S6E2CC8JGAGB10000/ S6E2CC8JFAGB10000 S6E2CCAJGAGB10000/ S6E2CCAJFAGB10000
Revision 1.0		
7 15	2. Features 3. Product Lineup	Added that CAN-FD Interface supported non-CAN FD.
12 15 90 91	2. Features 3. Product Lineup 10. Block Diagram 12. Memory Map	Deleted HDM-CEC/Remote Control Receiver.
18-20	5. Pin Assignments	Deleted the pins of HDM-CEC/Remote Control Receiver.(CEC0,CEC1) Modified the pin name of I2S. (MI2S*_0→MI2S*0_0) Deleted the pin of IGTRG0_0.
22-24	6. Pin Descriptions	Deleted the pins of HDM-CEC/Remote Control Receiver.(CEC0,CEC1) Modified the pin name of I2S. (MI2S*_0→MI2S*0_0) Modified the pin number of PF7 in LQFP216.(91→90) Modified the pin number of X1. (73, 58, 50, P5→107, 87, 71, P13) Modified the pin number of X0A. (107, 87, 71, P13→73, 58, 50, P5)
75-82	7. I/O Circuit Type	Modified IOH/IOL of Type S.(IOH=-12mA→-10mA, IOL=12mA→10mA) Added the case of using I2C in Type E, F, G, L, N, S.
97-105	13. Pin Status In Each CPU State	Deleted X and Y in Pin Status Type.
106-107	14.1. Absolute Maximum Ratings	Added 10mA type.
108-112	14.2. Recommended Operating Conditions	Added AVRL in Analog reference voltage. Modified the mistake in Ethernet-MAC Pins. Modified the leakage current in Maximum leakage current at operating
113-122	14.3.1. Current Rating	Modified the maximum current of each category.
123-124	14.3.2. Pin Characteristics	Added the characteristic of external bus in H level input voltage (hysteresis input). Added the characteristic of 10mA type.

Page	Section	Change Results
127	14.4.5. Operating Conditions of USB/Ethernet PLL・I2S PLL (in the case of using main clock for input clock of PLL)	Modified the maximum of I2S PLL macro oscillation clock frequency. (307.2MHz→384MHz)
196	14.5.12-bit A/D Converter	Modified the minimum of Sampling time. Modified the characteristic of State transition time to operation permission Added AVRL in Analog reference voltage.
204	14.8.2. Interrupt of Low-Voltage Detection	Modified the SVHI values in Conditions
5&6	Product Lineup	Deleted the max data
83	Electrical Characteristics	Deleted the power consumption item due to an error in the Absolute Maximum Ratings under the Electrical Characteristics.

NOTE: Please see “Document History” for later revised information.

Document History

Document Title: FM4: S6E2C Series Microcontroller Datasheet 200 MHz Arm® Cortex®-M4F High-Performance MCU
Document Number: 002-04980

Revision	ECN	Submission Date	Description of Change
**	-	03/25/2015	New spec.
*A	5126421	02/05/2016	Company name and layout design change. Added the note of TAP pin. Updated Package Code and Dimensions (LQFP-144, LQFP-176, LQFP-216).
*B	5634625	02/20/2017	Updated "12.4.8 Power-On Reset Timing" to change parameter from "Power Supply rise time(t_{VCCR})[ms]" to "Power ramp rate(dV/dt)[mV/us]" and added some comments. Modified typos in "12.4.12 CSIO (SPI) Timing". Deleted "SPI=1, MS=0" in the titles and added MS=0,1 in the schematic Modified Real-Time Clock(RTC) in "Features" Changed starting count value from 01 to 00. Deleted "second, or day of the week" in the Interrupt function. Modifications related to the VBAT in the following chapter. "8 Handling Devices" Notes on Power-on "11. Pin Status in Each CPU State" List of VBAT Domain Pin Status "12.3.1 Current Rating" Deleted descriptions about Voice function Deleted MPNs below from "13. Ordering Information" S6E2CCAJGAGV20000, S6E2CC8JGAGB10000, S6E2CC8JFAGB10000, S6E2CCAJGAGB10000, S6E2CCAJFAGB10000 S6E2CC8H0AGV20000, S6E2CC9H0AGV20000, S6E2CCAH0AGV20000, S6E2CC8HHAGV20000, S6E2CC9HHAGV20000, S6E2CCAHHAGV20000, S6E2CC8J0AGV20000, S6E2CC9J0AGV20000, S6E2CCAJ0AGV20000, S6E2CC8JHAGV20000, S6E2CC9JHAGV20000, S6E2CCAJHAGV20000, S6E2CC8J0AGB10000, S6E2CC9J0AGB10000, S6E2CCAJ0AGB10000, S6E2CC8JHAGB10000, S6E2CC9JHAGB10000, S6E2CCAJHAGB10000, S6E2CC8L0AGL20000, S6E2CC9L0AGL20000, S6E2CCAL0AGL20000, S6E2CC8LHAGL20000, S6E2CC9LHAGL20000, S6E2CCALHAGL20000 Added MPNs below to "13. Ordering Information" S6E2CC8H0AGV2000A, S6E2CC9H0AGV2000A, S6E2CCAH0AGV2000A, S6E2CC8HHAGV2000A, S6E2CC9HHAGV2000A, S6E2CCAHHAGV2000A, S6E2CC8J0AGV2000A, S6E2CC9J0AGV2000A, S6E2CCAJ0AGV2000A, S6E2CC8JHAGV2000A, S6E2CC9JHAGV2000A, S6E2CCAJHAGV2000A, S6E2CC8J0AGB1000A, S6E2CC9J0AGB1000A, S6E2CCAJ0AGB1000A, S6E2CC8JHAGB1000A, S6E2CC9JHAGB1000A, S6E2CCAJHAGB1000A, S6E2CC8L0AGL2000A, S6E2CC9L0AGL2000A, S6E2CCAL0AGL2000A, S6E2CC8LHAGL2000A, S6E2CC9LHAGL2000A, S6E2CCALHAGL2000A Deleted Baud rate spec for High-Speed Synchronous Serial in "12.4.12 CSIO (SPI) Timing"

Revision	ECN	Submission Date	Description of Change
			Modified the expression of the “Built-in CR” and add Note in the “2. Product Lineup” Modified typo(SCLKx_0 -> SCKx_0) Change the name from “USB Function” to “USB Device” Added Maximum Access size in “Features” Updated IO circuit (type A) Completing Sunset Review.
*C	6110443	03/26/2018	Updated Document Title to read as “FM4: S6E2C Series Microcontroller Datasheet 200 MHz ARM Cortex-M4F High-Performance MCU”. Merged S6E2CC, S6E2C5, S6E2C4, S6E2C3, S6E2C2, and S6E2C1 datasheets. Recreated Pin Assignments drawings using only the pin names and added a pin multiplexing table that shows alternative functions. Added navigation aids to tables with hyperlinks to circuit types and pin behavior. Added part differentiation tables at the beginning of the document and reorganized the front of the datasheet to match Cypress specifications. Replaced table footnotes with continuous footnote numbering (throughout). Added and expanded Ordering Information table. Added the Acronyms table. Updated Package Outlines in 15 Package Dimensions to latest. Changed Typ to Max in 12.4.7 Reset Input Characteristics, 12.4.8 Power-On Reset Timing, and 12.4.9 GPIO Output Characteristics. Removed Crypo function and part numbers that supported Crypto. Completing Sunset Review.
*D	6579097	05/22/2019	Updated to new template.
*E	7901049	05/10/2023	Updated Block diagram. Updated Pin Description: Updated pin description of pin 25 and 26 corresponding to LQQ216 package. Updated Package Dimensions: Spec 002-13015 – Changed revision from *A to *B. Spec 002-15150 – Changed revision from ** to *A. Updated some format issues across the document. Updated links across the document. Completing Sunset Review.
*F	8101392	01/24/2025	Updated Memory Map, Ordering Information and Package Dimensions. Replaced package diagram spec 002-15150 by Z8B00252086, 002-13015 by Z8B00255984, 002-13493 by Z8B00251505, 002-15153 by Z8B00256217. Completing ECN Sunset Review.
*G	8185906	07/23/2026	Deleted the power consumption item &related max data due to an error in the Product lineup & Absolute Maximum Ratings under the Electrical Characteristics.

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