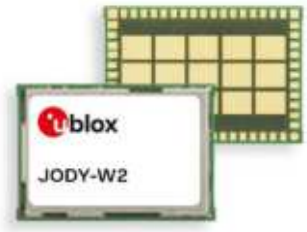
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JODY-W2 series

Host-based multiradio modules with Wi-Fi 5 and Bluetooth 5.2

Data sheet



Abstract

This technical data sheet describes the JODY-W2 series modules with 1x1 802.11n/ac and dual-mode Bluetooth 5.2. JODY-W2 is ideal for in-vehicle infotainment and telematics applications with simultaneous use cases requiring high data rates, such as in-car hotspots, Wi-Fi display applications such as Apple CarPlay, or video streaming across multiple clients. Connection to a host processor is through SDIO, or High-Speed UART interfaces (Bluetooth only).

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Functional Sample	Draft	For functional testing. Revised and supplementary data will be published later.
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Initial Production	Early production information	Data from product verification. Revised and supplementary data may be published later.
Mass Production / End of Life	Production information	Document contains the final product specification.

This document applies to the following products:

Product name	Type number	Chipset	PCN reference	Product status
JODY-W263-A	JODY-W263-00A-00	88W8987A	N/A	Mass production
JODY-W263-A	JODY-W263-01A-00	88W8987S	N/A	Mass production
JODY-W263	JODY-W263-00B-00	88W8987	N/A	Mass production
JODY-W263	JODY-W263-10B-00	88W8987	N/A	Mass production
JODY-W263-A	JODY-W263-10A-00	88W8987A	N/A	Initial production
JODY-W263	JODY-W263-01B-00	88W8987	N/A	Initial production
JODY-W263	JODY-W263-11B-00	88W8987	N/A	Initial production

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1 Functional description

1.1 Overview

The JODY-W2 series comprises compact modules based on the NXP 88W8987 chipset family. The chipsets used in the automotive grade JODY-W2 modules are AEC-Q100 compliant. The modules enable Wi-Fi 5, Bluetooth® Classic (BR/EDR), and Bluetooth® Low Energy (LE) communication, and are ideal for automotive and industrial applications.

JODY-W2 modules can be operated in the following modes:

- Wi-Fi 1x1 802.11a/b/g/n/ac in 2.4 GHz or 5 GHz
- Dual-mode Bluetooth® Core 5.2, including audio, can be operated fully simultaneously with Wi-Fi

JODY-W2 modules undergo extended automotive qualification in accordance with ISO 16750-4 and are manufactured in line with ISO/TS 16949. Connection to a host processor is through SDIO, or High-Speed UART interfaces.

1.2 Applications

Automotive applications

- In-car Access Point for internet access
- In the car applications such as Apple Car-Play, Miracast, and so on.
- Rear-seat display
- Rapid sync-n-go applications and fast content download to the vehicle.
- Hands-free equipment (Bluetooth)

Industrial applications

- Manufacturing floor automation, wireless control terminals and point-to-point backhaul
- Machine control
- Medical in-hospital applications
- Security and surveillance
- Outdoor content distribution
- Robust wireless connectivity in a broad range of industrial applications

1.3 Block diagram

Figure 1 shows the various components and interfaces supported in JODY-W2 series modules.

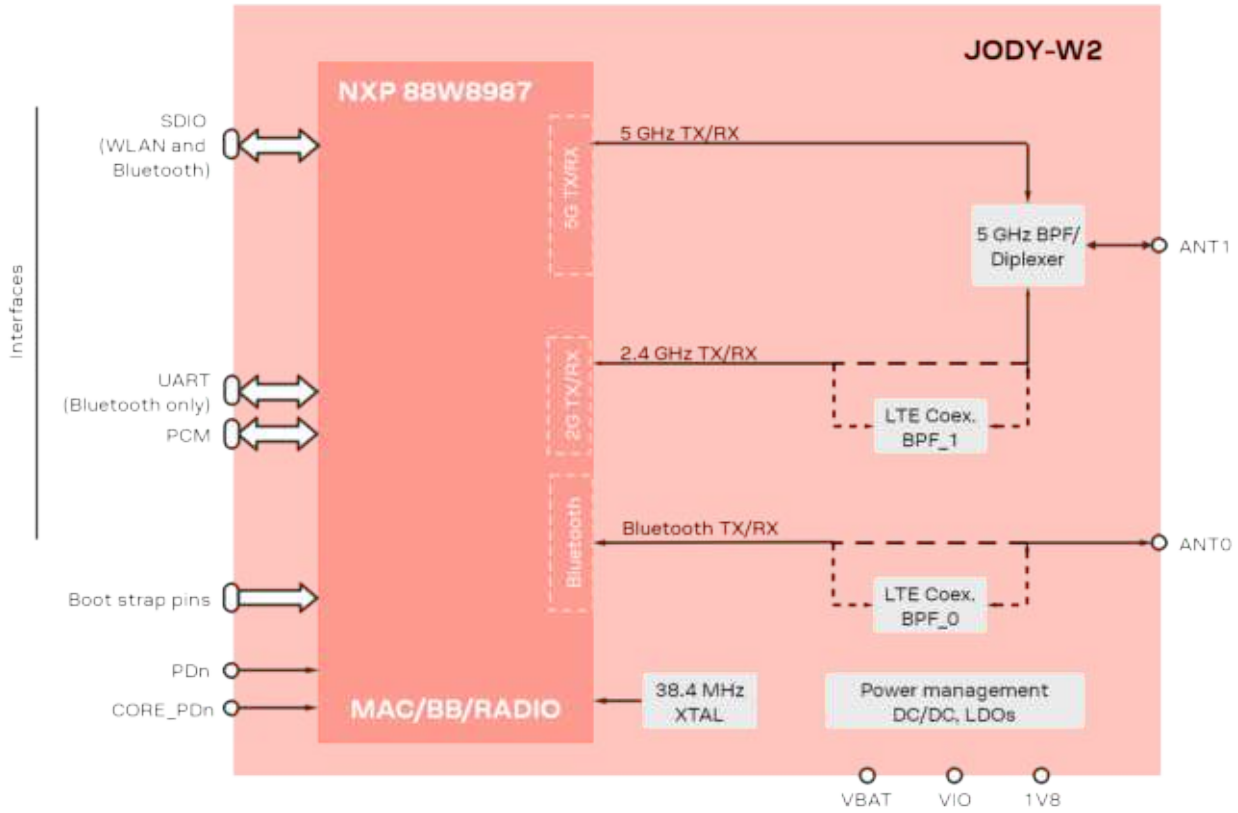


Figure 1: JODY-W263-A block diagram

JODY-W2 variants equipped with an LTE coexistence filter (2.4 GHz BPF), as shown in Table 1, are recommended when co-located with LTE devices operating in LTE bands 7, 38, 40, or 41.

Ordering code	Antenna configuration		LTE Coexistance BPF	
	ANT0	ANT1	BPF_0	BPF_1
JODY-W263-00A JODY-W263-01A JODY-W263-00B JODY-W263-10B	Bluetooth	2.4 and 5 GHz Wi-Fi	No	No
JODY-W263-10A JODY-W263-01B JODY-W263-11B	Bluetooth	2.4 and 5 GHz Wi-Fi	Yes	Yes

Table 1: Supported JODY-W2 configurations

1.4 Product features

Item	Description	
Grade	JODY-W263 JODY-W263-A	Professional Automotive
Chipset	JODY-W263 JODY-W263-A	NXP 88W8987 NXP 88W8987(S/A)
Antenna type	Two antenna pins for Wi-Fi and Bluetooth	
Supported Wi-Fi radio modes	IEEE 802.11 a/b/g/n/ac	
Supported Wi-Fi bands	2.5 / 5 GHz	
Max. Wi-Fi output power	19 dBm (at antenna pin)	
Bluetooth Core version	5.2	
Bluetooth profiles	HCI	
Supported Bluetooth radio modes	Bluetooth BR/EDR Bluetooth Low Energy	
Supported Bluetooth LE data rates	1 Mbps 2 Mbps	
LTE coexistence filter	See Table 1	
OS support	Linux / Android	
Interfaces	SDIO 3.0 (Wi-Fi/Bluetooth) UART (Bluetooth) PCM (Bluetooth digital audio)	
Features	Micro access point with max. 8 connected clients	
	Simultaneous client and access point mode	
	WPA3	
	RF parameters/MAC addresses in OTP	
Max. ambient operating temperature	85 °C (JODY-W263-01A: 105 °C)	
Module size	19.8 x 13.8 mm	

Table 2: JODY-W2 series product features

1.4.1 Wi-Fi features

- Standards: IEEE 802.11a/b/g/n/ac/d/e/h/i/k/r/u/v/w[1]
- IEEE 802.11ac PHY data rates up to 433 Mbit/s (80 MHz)
- 20/40/80 MHz bandwidth
- Simultaneous client and access point operation
- Support of Wi-Fi direct/P2P mode
- 128-bit AES hardware crypto engine. TKIP/WEP, AES/CCMP, AES/CMAC, AES/GCMP
- WPA/WPA2 and WAPI encryption is supported by hardware
- SDIO 3.0 host interface for Wi-Fi (and optionally Bluetooth)
- WPA3-SAE is supported in station and AP mode

1.4.1.1 Wi-Fi Simultaneous operation modes

- AP Simultaneous operation
  - AP + AP - Multi-BSS support (MAX_UAP_BSS = 2)
  - AP + AP + STA
  - AP + STA
- P2P Simultaneous operation
  - P2P + STA
  - P2P + AP
  - P2P + STA + AP

☞ Note that two or more Wi-Fi interfaces should operate in the same channel.

1.4.2 Bluetooth features

- Bluetooth Core 5.2 with Bluetooth Low Energy
- BR and EDR packet types – 1 Mbit/s, 2 Mbit/s, and 3 Mbit/s
- LE 2 Mbit/s PHY
- LE Data Length Extension
- LE Advertising Extension
- Bluetooth Class 1 and 2
- Standard SDIO and UART HCI transport layer
- PCM interface for voice applications

1.4.3 General product features

- Driver support for Linux, Android, FreeRTOS (NXP MCUXpresso)
- Coexistence with cellular and other on-chip radios
- Small footprint (19.8 mm x 13.8 mm), LGA package
- Automotive qualification tests (climatic, mechanical, and operating life tests) in accordance with ISO 16750-4 planned

[1] 802.11k/r/u/v in STA mode only

1.4.4 Reserved MAC addresses

JODY-W2 series modules have four consecutive MAC addresses that are unique for each module variant. The first two of these four addresses are configured during production.

The first address is used for the Bluetooth communication, while the second address is configured for Wi-Fi communication. The Data Matrix Code shown on the product label includes the Bluetooth MAC address, as described in the Labeling and ordering information. The remaining two MAC addresses are not used in the manufacturing configuration but are reserved for module usage.

MAC address	Assignment	Last two bits of MAC address	Example
Module1, address 1	Bluetooth	0b00	*D4:CA:6E:44:00:04*
Module1, address 2	Wi-Fi	0b01	D4:CA:6E:44:00:05
Module1, address 3	(free for use)	0b10	D4:CA:6E:44:00:06
Module1, address 4	(free for use)	0b11	D4:CA:6E:44:00:07
Module2, address 1	Bluetooth	0b00	*D4:CA:6E:44:00:08*
Module2, address 2	Wi-Fi	0b01	D4:CA:6E:44:00:09
Module2, address 3	(free for use)	0b10	D4:CA:6E:44:00:0A
Module2, address 4	(free for use)	0b11	D4:CA:6E:44:00:0B

Table 3: MAC address assignment

For further information about using the MAC address for secondary Wi-Fi interfaces, see also “Using reserved MAC addresses” in the JODY-W2 system integration manual [2].

2 Interfaces

2.1 Host interface configuration

The JODY-W2 series provides two configuration pins, **CONFIG[0]** and **CONFIG[1]**, for selecting the host interface configuration. Additional configuration pins are used to set parameters following a reset. To set a configuration bit to 0, attach a 100 kΩ resistor to GND. No external pull-up resistor is required to set a configuration bit to 1. Table 4 and Table 5 show all strapping options.

CONFIG[1]	CONFIG[0]	Wi-Fi	Bluetooth	Firmware download	Number of SDIO functions
1	0	SDIO	UART	SDIO+UART(parallel/Serial)	1 (Wi-Fi)
1	1	SDIO	SDIO	SDIO+SDIO(parallel/Serial)	2 (Wi-Fi, Bluetooth)

Table 4: Host interface configuration options

Additional configuration pins are listed in Table 5.

Name	Pin	Description
PCM_OUT	17	Set high during reset
BT_UART_RTS	38	Set high during reset
LTE_COEX_TX	13	Set high during reset
BT_UART_TX	36	Set low during reset. A 51 kΩ pull down resistor is implemented on the module.

Table 5: Additional configuration pins

2.2 SDIO interface

The SDIO device interface conforms to the industry standard SDIO 3.0 specification (UHS-I, up to 104 MByte/s). The interface allows host controllers to access the Wi-Fi, and optionally Bluetooth, functions of JODY-W2 series modules using the SDIO bus protocol. The interface supports 4-bit SDIO transfer mode at the full clock range up to 208 MHz. For SDIO 2.0 running at 25 MHz and 50 MHz clock frequencies. Only a signal voltage of 1.8 V is supported for all bus speed modes.

Bus speed mode	Max clock frequency [MHz]	Signal voltage [V]	Max. bus speed [MB/s]
DS: Default Speed	25	1.8	12.5
HS: High Speed	50	1.8	25
SDR12	25	1.8	12.5
SDR25	50	1.8	25
SDR50	100	1.8	50
SDR104	208	1.8	104
DDR50	50	1.8	50

Table 6: Supported SDIO bus speed modes

2.2.1 Default speed and high-speed modes (1.8 V)

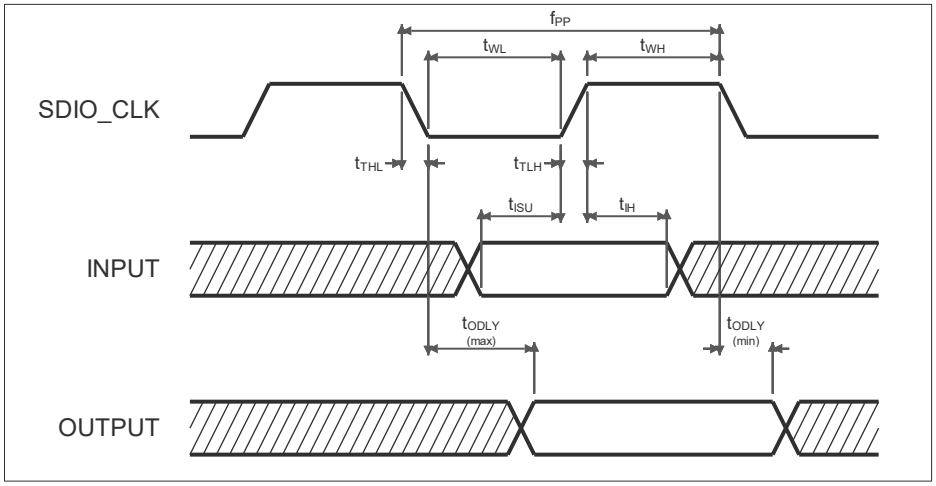


Figure 2: SDIO Protocol timing diagram - default speed mode (1.8 V)

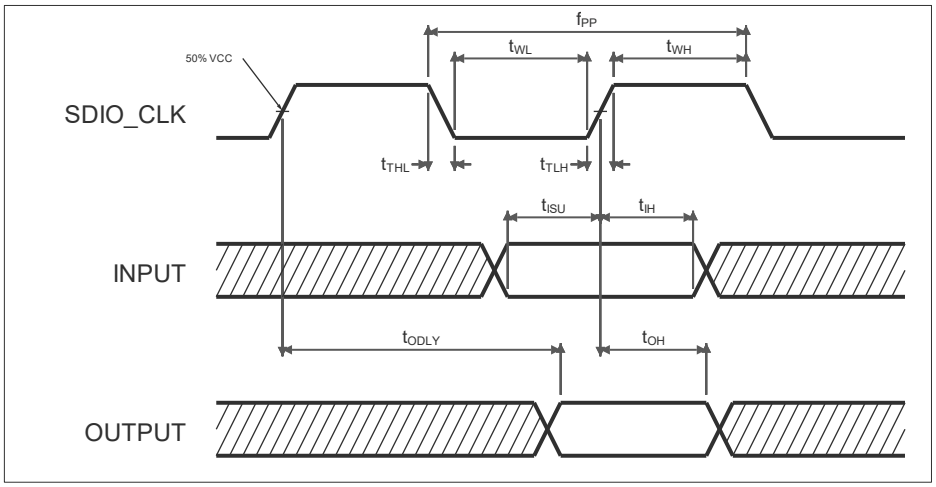


Figure 3: SDIO Protocol timing diagram – high speed mode (1.8 V)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
f_{PP}	Clock frequency – Data Transfer Mode	Normal	0	-	25	MHz
		High speed	0	-	50	MHz
f_{OD}	Clock frequency – Identification Mode	Normal	0		400	kHz
		High speed	0	-	400	kHz
t_{WL}	Clock low time	Normal	10	-	-	ns
		High speed	7	-	-	ns
t_{WH}	Clock high time	Normal	10	-	-	ns
		High speed	7	-	-	ns
t_{TLH}	Clock rise time	Normal	-	-	10	ns
		High speed	-	-	3	ns
t_{THL}	Clock low time	Normal	-	-	10	ns
		High speed	-	-	3	ns
t_{ISU}	Input setup time	Normal	5	-	-	ns
		High speed	6	-	-	ns

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
t_{IH}	Input hold time	Normal	5	-	-	ns
		High speed	2	-	-	ns
t_{ODLY}	Output delay time	Normal	-	-	14	ns
t_{ODLY}	Output delay time CL ≤ 40 pF (1 card)	High speed	-	-	14	ns
t_{OH}	Output hold time	High speed	2.5	-	-	ns

Table 7: SDIO timing data – Default speed, High speed modes (1.8 V)

2.2.2 SDR12, SDR25, SDR50 modes (up to 100 MHz, 1.8 V)

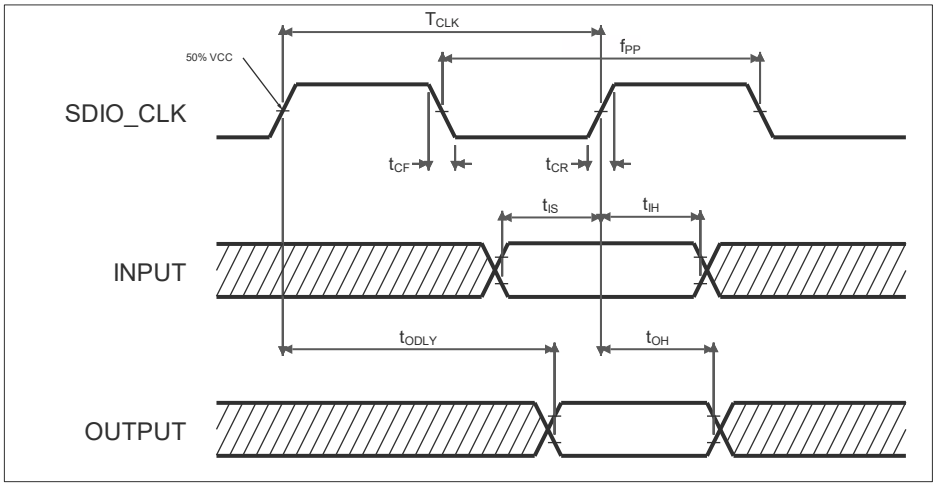


Figure 4: SDIO protocol timing diagram – SDR12, SDR25, SDR50 modes (up to 100 MHz, 1.8 V)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
f_{PP}	Clock frequency	SDR12	0	-	25	MHz
		SDR25	0	-	50	MHz
		SDR50	0	-	100	MHz
t_{IS}	Input setup time	SDR12/25/50	3	-	-	ns
t_{IH}	Input hold time	SDR12/25/50	0.8	-	-	ns
t_{CLK}	Clock time	SDR12/25/50	10	-	40	ns
t_{CR}, t_{CF},	Rise time, fall time T_{CR}, T_{CF} < 2 ns (max) at 100 MHz C_{CARD} = 10 pF	SDR12/25/50		-	0.2*T_{CLK}	ns
t_{ODLY}	Output delay time $C_L \leq 30$ pF	SDR12/25	-	-	14	ns
		SDR50	-		7.5	
t_{OH}	Output hold time C_L = 15 pF	SDR12/25/50	1.5	-	-	ns

Table 8: SDIO timing data – SDR12, SDR25, SDR50 modes (up to 100 MHz, 1.8 V)

2.2.3 SDR104 mode (208 MHz, 1.8 V)

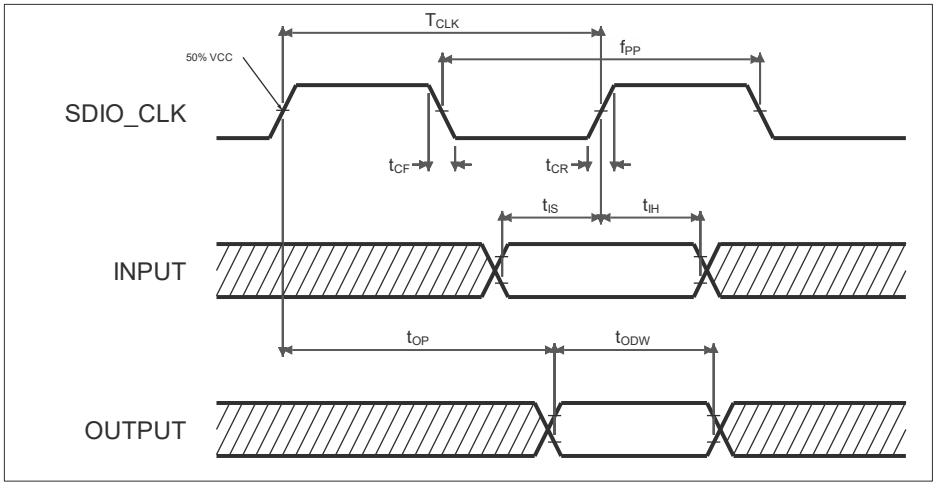


Figure 5: SDIO protocol timing diagram – SDR104 mode (208 MHz, 1.8 V)

Symbol	Parameter	Condition	Min.	Typ	Max.	Units
f_{PP}	Clock frequency	SDR104	0	-	208	MHz
T_{IS}	Input setup time	SDR104	1.4	-	-	ns
T_{IH}	Input hold time	SDR104	0.8	-	-	ns
T_{CLK}	Clock time	SDR104	4.8	-	-	ns
t_{CR}, t_{CF},	Rise time, fall time T_{CR}, T_{CF} < 0.96 ns (max) at 208 MHz C_{CARD} = 10 pF	SDR104		-	0.2*T_{CLK}	ns
T_{OP}	Card output phase	SDR104	0	-	10	ns
T_{ODW}	Output timing of variable data window	SDR104	2.88	-	-	ns

Table 9: SDIO timing data – SDR104 mode (208 MHz) (1.8 V)

2.2.4 DDR50 Mode (50 MHz, 1.8 V)

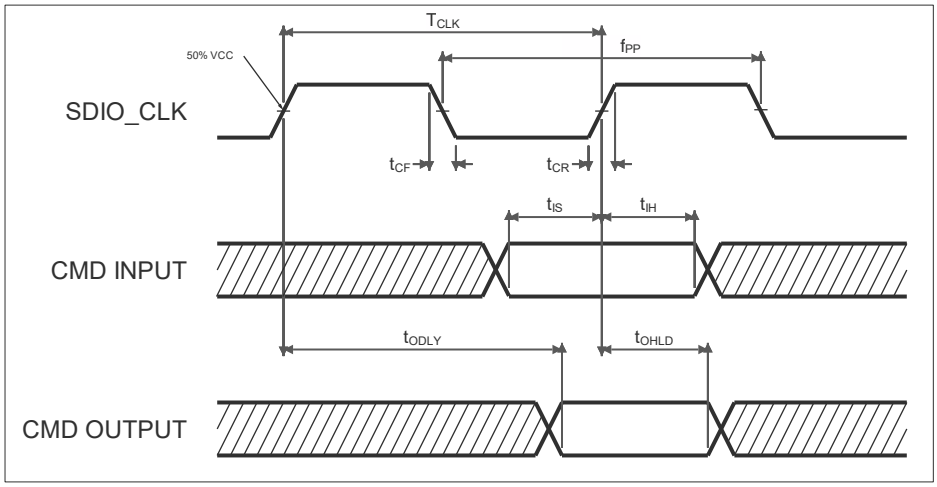


Figure 6: SDIO CMD timing diagram – DDR50 mode (50 MHz, 1.8 V)

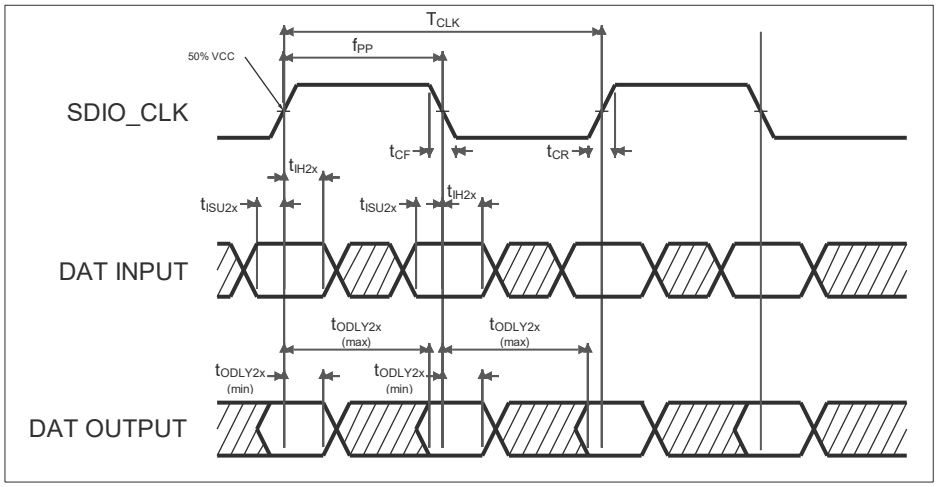


Figure 7: SDIO DAT [3:0] timing diagram – DDR50 mode (50 MHz, 1.8 V)

Symbol	Parameter	Condition	Min.	Typ	Max.	Units
Clock						
TCLK	Clock time 50 MHz (max) between rising edges	DDR50	20	-	-	ns
tCR, tCF,	Rise time, fall time TCR, TCF < 4.00 ns (max) at 50 MHz CCARD = 10 pF	DDR50	-	-	0.2*TCLK	ns
Clock Duty		DDR50	45	-	55	%
CMD Input (referenced to clock rising edge)						
tIS	Input setup time CCARD ≤ 10 pF (1 card)	DDR50	6	-	-	ns
tIH	Input hold time CCARD ≤ 10 pF (1 card)	DDR50	0.8	-	-	ns
CMD Output (referenced to clock rising edge)						
tODLY	Output delay time during data transfer mode CL ≤ 30 pF (1 card)	DDR50	-	-	13.7	ns
tOHLD	Output hold time CL ≥ 15 pF (1 card)	DDR50	1.5	-	-	ns
DAT[3:0] Input (referenced to clock rising and falling edges)						
tIS2x	Input setup time CCARD ≤ 10 pF (1 card)	DDR50	3			ns
tIH2x	Input hold time CCARD ≤ 10 pF (1 card)	DDR50	0.8			ns
DAT[3:0] Output (referenced to clock rising and falling edges)						
tODLY2x (max)	Output delay time during data transfer mode CL ≤ 25 pF (1 card)	DDR50			7.0	ns
tODLY2x (min)	Output hold time CL ≥ 15 pF (1 card)	DDR50	1.5			ns

Table 10: SDIO timing data – DDR50 mode (50 MHz, 1.8 V)

2.3 High Speed UART interface

JODY-W2 series modules support a high-speed Universal Asynchronous Receiver/Transmitter (UART) interface in compliance with the industry standard 16550 specification.

The main features of the UART interface are:

- FIFO mode permanently selected for transmit and receive operations
- Automatic baud rate detection
- Two pins for transmit and receive operations
- Two flow control pins
- Interrupt triggers for low-power, high throughput operation
- High throughput (4 Mbps)

Baud rate				
1200	38400	460800	1500000	3000000 (default)
2400	57600	500000	1843200	3250000
4800	76800	921600	2000000	3692300
9600	115200	1000000	2100000	4000000
19200	230400	1382400	2764800	

Table 11: Supported UART baud rates

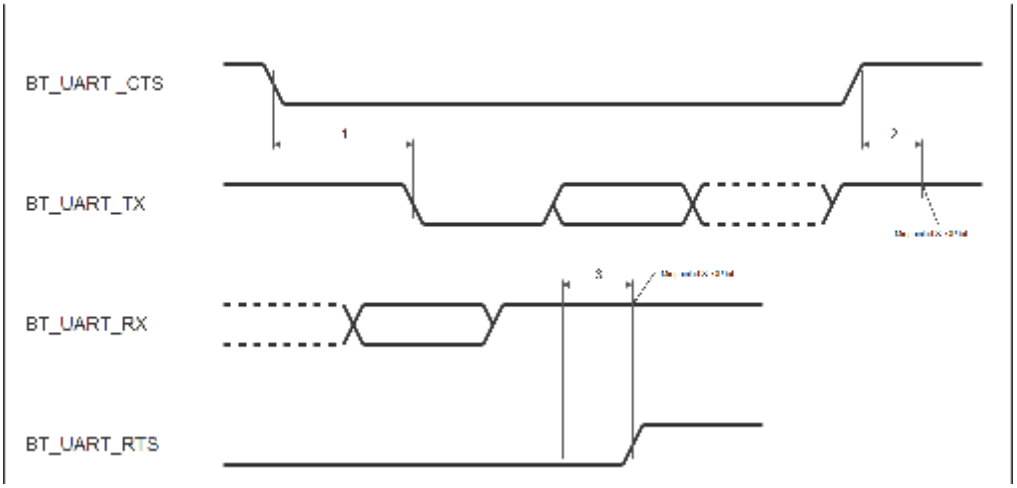


Figure 8: UART timing characteristics

Reference	Characteristic	Min.	Typ.	Max.	Units
1	Delay time, BT_UART_CTS low to BT_UART_TX valid	-	-	1.5	Bit period
2	Setup time, BT_UART_CTS high before midpoint of stop bit	-	-	0.5	Bit period
3	Delay time, midpoint of stop bit to BT_UART_RTS high	-	-	0.5	Bit period

Table 12: UART timing specification

2.4 PCM interface

JODY-W2 series modules include a Pulse Code Modulation (PCM) interface that supports:

- Central or Peripheral mode
- PCM bit width size of 8 bits or 16 bits
- Up to 4 slots with configurable bit width and start positions
- Short frame and long frame synchronization
- Burst PCM mode

In PCM Central mode, the interface generates a 2 MHz or a 2.048 MHz **PCM_CLK** and 8 kHz **PCM_SYNC** signal.

In Peripheral mode, the interface has both **PCM_CLK** and **PCM_SYNC** inputs to allow another unit on the PCM bus generate the signals.

2.4.1 PCM interface specifications

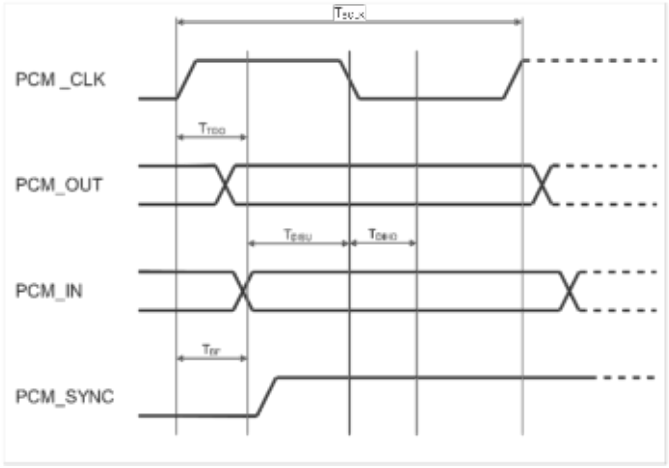


Figure 9: PCM timing specification – Central mode

Symbol	Parameter	Condition	Min.	Typ	Max.	Units
FBCLK	PCM clock frequency	-	-	2/2.048	-	MHz
Duty Cycle$_{BCLK}$	-		0.4	0.5	0.6	-
$T_{BCLK\ rise/fall}$	-	-	-	3	-	ns
T_{DO}	-	-	-	-	15	ns
T_{DISU}	-	-	20	-	-	ns
T_{DIHO}	-	-	15	-	-	ns
T_{BF}	-	-	-	-	15	ns

Table 13: PCM timing specification – Central mode

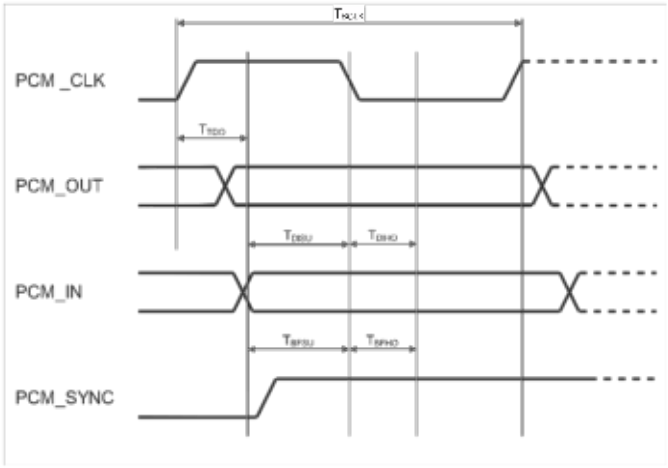


Figure 10: PCM timing specification – Peripheral mode

Symbol	Parameter	Condition	Min.	Typ	Max.	Units
FBCLK	PCM clock frequency	-	-	2/2.048	-	MHz
Duty Cycle$_{BCLK}$	-		0.4	0.5	0.6	-
$T_{BCLK\ rise/fall}$	-	-	-	3	-	ns
T_{DO}	-	-	-	-	30	ns
T_{DISU}	-	-	20	-	-	ns
T_{DIHO}	-	-	15	-	-	ns
T_{BF}	-	-	-	-	15	ns

Table 14: PCM timing specification – Peripheral mode

3 Pin definition

3.1 Pin description

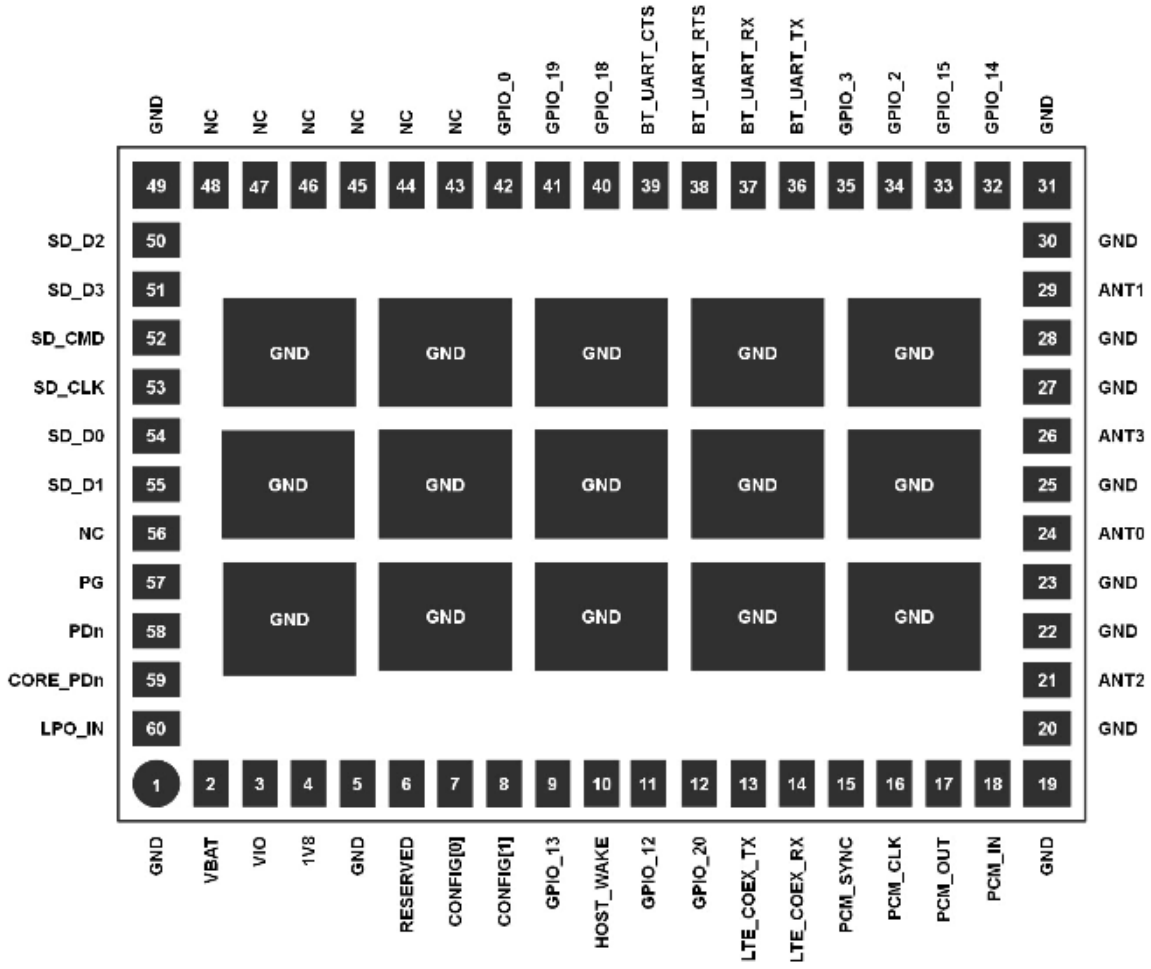


Figure 11: JODY-W2 pin assignment (top view)

No.	Name	Chip pin	I/O[2]	Description	Domain
1	GND		GND	Ground	GND
2	VBAT		PWR	Module supply input (2.8 V – 5.5 V)	VBAT
3	VIO		PWR	VIO supply (1.8 V or 3.3 V)	VIO
4	1V8		PWR	VIO supply for SDIO, Supply for analog part (1.8 V)	1V8
5	GND		GND	Ground	GND
6	CONFIG[2]		NC	Reserved. A “DNI” pull-up resistor should be added at this pin to respond to future chipset changes.	1V8
7	CONFIG[0]	CONFIG_HOST[0]	I	Configuration pin. See also Table 4: Host interface configuration options.	1V8
8	CONFIG[1]	CONFIG_HOST[1]	I	Configuration pin. See also Table 4: Host interface configuration options.	1V8

[2] I/O notations: I=Input, O=Output, I/O=Input or Output, OD=Open Drain, NC=Not Connected, PWR=Power, GND=Ground, RF=Radio i/f

No.	Name	Chip pin	I/O[2]	Description	Domain
9	GPIO_13	GPIO[13]	I/O	Optional host to Wi-Fi out-of-band wake-up signal (input)	VIO
10	HOST_WAKE	GPIO[1]	I/O	Wi-Fi to host out-of-band wake-up signal (output)	VIO
11	GPIO_12	GPIO[12]	I/O	Optional host to Bluetooth out-of-band wake-up signal (input)	VIO
12	GPIO_20	GPIO[20]	I/O	Bluetooth to host out-of-band wake-up signal (output) GPIO_1 or GPIO_4 can be used as alternative signals.	VIO
13	LTE_COEX_TX	GPIO[17] / JTAG_TDO	I/O	Configuration pin, see also Table 5: Additional configuration pins.	VIO
14	LTE_COEX_RX	GPIO[16] / JTAG_TDI	I/O		VIO
15	PCM_SYNC	PCM_SYNC / GPIO[7]	I/O	PCM frame sync, can be output (Central) or input (Peripheral)	VIO
16	PCM_CLK	PCM_CLK / GPIO[6]	I/O	PCM clock, can be output (Central) or input (Peripheral)	VIO
17	PCM_OUT	PCM_DOUT / GPIO[5]	O	PCM data output. Configuration pin, see also Table 5: Additional configuration pins.	VIO
18	PCM_IN	PCM_DIN / GPIO[4]	I	PCM data input	VIO
19	GND		GND	Ground	GND
20	GND		GND	Ground	GND
21	ANT2		NC	Reserved (Do not connect)	-
22	GND		GND	Ground	GND
23	GND		GND	Ground	GND
24	ANT0		RF	Bluetooth antenna signal. Do not connect to DC	VBAT
25	GND		GND	Ground	GND
26	ANT3		NC	Reserved (Do not connect)	-
27	GND		GND	Ground	GND
28	GND		GND	Ground	GND
29	ANT1		RF	Wi-Fi dual-band antenna signal. Do not connect to DC	VBAT
30	GND		GND	Ground	GND
31	GND		GND	Ground	GND
32	GPIO_14	GPIO[14] / JTAG_TCK	I/O	Can be used as Wi-Fi independent reset signal (input)	VIO
33	GPIO_15	GPIO[15] / JTAG_TMS	I/O	Can be used as Bluetooth independent reset signal (input)	VIO
34	GPIO_2	GPIO[2]	I/O		VIO
35	GPIO_3	GPIO[3]	I/O		VIO
36	BT_UART_TX	UART_SOUT / GPIO[8]	O	Bluetooth UART serial data output. Configuration pin, see also Table 5: Additional configuration pins.	VIO
37	BT_UART_RX	UART_SIN / GPIO[9]	I	Bluetooth UART serial data input	VIO
38	BT_UART_RTS	UART_RTSn / GPIO[11]	O	Bluetooth UART active-low request-to-send signal (output). Configuration pin, see also Table 5: Additional configuration pins.	VIO
39	BT_UART_CTS	UART_CTSn / GPIO[10]	I	Bluetooth UART active-low clear-to-send signal (input)	VIO
40	GPIO_18	GPIO[18]	I/O		VIO
41	GPIO_19	GPIO[19]	I/O		VIO

No.	Name	Chip pin	I/O[2]	Description	Domain
42	GPIO_0	GPIO[0]	I/O		VIO
43-48	NC		NC	Reserved (Do not connect)	-
49	GND		GND	Ground	GND
50	SD_D2	SD_DAT[2]	I/O	SDIO data line bit [2]	1V8
51	SD_D3	SD_DAT[3]	I/O	SDIO data line bit [3]	1V8
52	SD_CMD	SD_CMD	I/O	SDIO Command line	1V8
53	SD_CLK	SD_CLK	I	SDIO Clock input	1V8
54	SD_D0	SD_DAT[0]	I/O	SDIO data line bit [0]	1V8
55	SD_D1	SD_DAT[1]	I/O	SDIO data line bit [1]	1V8
56	NC		NC	Reserved (Do not connect)	-
57	PG		OD	Open-drain output from the internal DC/DC converter, which indicates the power quality of the 2.2 V rail. High impedance indicates power good. Low level indicates 2.2 V is not in power good. A (100 kΩ) pull-up resistor must be connected to this pin to detect the power good state.	-
58	PDn	PDn	I	Power-down interface of the chipset: 0 = power-down mode 1 = normal mode Can accept an input of 1.8 V to 4.5 V. No Internal pull-up on this pin.	1V8
59	CORE_PDn		I	Enable pin of the core voltage regulator: 0 = power supply off Connect with PDn	1V8
60	LPO_IN	SPL_CLK_IN	I	Sleep clock input (optional) 32.768 kHz clock input used for lower power operation in sleep mode. Only supported on professional grade variants: JODY-W263-xxB	VIO
-	Exposed Pins		GND	15 Ground/Thermal exposed pins Connect to ground. For more information, see the JODY-W2 system integration manual [2].	GND

Table 15: JODY-W2 series pin description

4 Electrical specifications

⚠ Stressing the device above one or more of the Absolute maximum ratings can cause permanent damage. These are stress ratings only. Operating the module at these or at any conditions other than those specified in the Operating conditions should be avoided. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

☞ All given application information is only advisory and does not form part of the specification.

4.1 Absolute maximum ratings

Symbol	Description	Min.	Max.	Units
VBAT	Power supply voltage	-0.3	6.0	V
VIO	I/O supply voltage 1.8 V / 3.3 V	-	4.0	V
1V8	Analog power supply voltage 1.8 V	-	1.98	V
$T_{STORAGE}$	Storage temperature	-40	+85	°C
	Storage temperature JODY-W263-01A	-40	+105	°C

Table 16: Absolute maximum ratings

⚠ The product is not protected against overvoltage or reversed voltages. Voltage spikes exceeding the power supply voltage specification described in Table 16 must be limited to values within the specified boundaries by using appropriate protection devices.

4.2 Maximum ESD ratings

Applicability	Min.	Max.	Units
Human Body Model (HBM), according to ANSI/ESDA/JEDEC JS-001	-1500	+1500	V
Charged Device Model (CDM), according to ANSI/ESDA/JEDEC JS-002	-500	+500	V

Table 17: Maximum ESD ratings

4.3 Operating conditions

Symbol	Parameter	Min.	Typ.	Max.	Units
VBAT	Power supply voltage	2.8	-	5.5	V
VIO	I/O supply voltage 1.8 V	1.67	-	1.92	V
	I/O supply voltage 3.3 V	3.07	-	3.53	V
1V8	Analog power supply voltage 1.8 V	1.71	1.8	1.89	V
T_A	Ambient operating temperature				
	JODY-W263-00A/-10A/-00B/-01B	-40	-	+85	°C
	JODY-W263-01A	-40	-	+105	°C
	JODY-W263-10B/-11B	-30	-	+85	°C
Ripple Noise	Peak-to-peak voltage ripple on all supply lines.	-	-	10	mV

Table 18: Operating conditions

4.4 Wi-Fi power consumption

Peak current condition	Temperature	VBAT (3.3 V) [A]	1V8 (1.8 V) [A]
Active transmission	Room temperature	0.5	0.18
	T_max (105 °C)	0.8	0.2
Firmware Initialization	Room temperature	0.7	0.2
	T_max (105 °C)	0.7	0.2

Table 19: Peak current consumption

Wi-Fi operation modes	VBAT (3.3 V) [mA]	1V8 (1.8 V) [mA]	VIO (1.8 V) [mA]
Power – save modes			
Power down	1.02	0.2	0.04
Wi-Fi alone enabled	1.41	0.12	0.21
Wi-Fi and Bluetooth in deep-sleep	1.49	0.12	0.27
IEEE Power Save DTIM 10 and BT deep-sleep	1.61	0.18	0.27
IEEE Power Save DTIM 5 and BT deep-sleep	1.76	0.37	0.27
IEEE Power Save DTIM 3 and BT deep-sleep	1.85	0.43	0.26
IEEE Power Save DTIM 1 and BT deep-sleep	2.61	1.07	0.26
Active transmit modes			
CCK 1Mbps, BW20, Ch7, 18 dBm	345	75	0.07
CCK 11Mbps, BW20, Ch7, 18 dBm	353	75	0.07
MCS0, HT20, Ch7, 18 dBm	344	75	0.07
MCS7, HT20, Ch7, 15 dBm	255	70	0.07
MCS0, VHT20, Ch100, 18 dBm	325	135	0.07
MCS7, VHT20, Ch100, 15 dBm	245	125	0.07
MCS9, VHT40, Ch102, 15 dBm	232	123	0.07
MCS9, VHT80, Ch106, 15 dBm	242	123	0.07
Receive modes			
CCK 1 Mbps, BW20, Ch7, -50 dBm	56	41	0.07
MCS2, HT20, Ch7, -50 dBm	63	41	0.07
MCS2, VHT20, Ch100, -50 dBm	66	61	0.07
MCS3, VHT40, Ch102, -50 dBm	73	71	0.07
MCS9, VHT80, Ch106, -40 dBm	87	75	0.07

Table 20: Wi-Fi radio typical current consumption with different modes of operation

4.5 Bluetooth power consumption

Bluetooth operation modes	VBAT (3.3 V) [mA]	1V8 (1.8 V) [mA]	VIO (1.8 V) [mA]
Operating modes			
Bluetooth alone (SDIO not connected)	0.95	0.13	0.26
Bluetooth classic inquiry scan	1.64	0.25	0.27
Bluetooth classic page scan	7.95	1.54	0.25
Bluetooth LE advertisement	1.95	1.42	0.27
Bluetooth LE scanning	12.51	16.11	0.27
Active transmit mode			
Bluetooth classic DH5, 10 dBm, Ch39	55	83	0.07
Bluetooth classic 2-DH5, 10 dBm, Ch39	56	74	0.07
Bluetooth classic 3-DH5, 10 dBm, Ch39	60	73	0.07
Bluetooth LE, PN9, Ch19	58	77	0.07
Active receive mode			
Bluetooth classic DH1, 1 Mbps, -60 dBm, Ch39	56	48	0.07
Bluetooth classic DH5, 1 Mbps, -60 dBm, Ch39	57	53	0.07
Bluetooth classic DH5, 2 Mbps, -60 dBm, Ch39	57	52	0.07
Bluetooth classic DH5, 3 Mbps, -60 dBm, Ch39	56	53	0.07
Bluetooth LE, -60 dBm, Ch19	57	52	0.07

Table 21: Bluetooth radio typical current consumption with different operating modes

4.6 Digital pad ratings

Symbol	Parameter	VIO	Min.	Max.	Units
V_{IH}	Input high voltage	1.8 V - 3.3 V	0.7*VIO	VIO+0.4	V
V_{IL}	Input low voltage	1.8 V - 3.3 V	-0.4	0.3*VIO	V
V_{HYS}	Input hysteresis	1.8 V - 3.3 V	100	-	mV
V_{OH}	Output high voltage	1.8 V - 3.3V	VIO-0.4	-	V
V_{OH}	Output low voltage	1.8 V - 3.3 V	-	0.4	V

Table 22: DC characteristics VIO

4.7 Radio specifications

4.7.1 Bluetooth

Parameter	Specification
RF Frequency Range	2.4 – 2.5 GHz
Supported Modes	Bluetooth Core 5.2
Number of channels	79 (BR/EDR)
	40 (LE)
Modulation	1 Mbps: GFSK (BR) 2 Mbps: π/4 DQPSK (EDR) 3 Mbps: 8DQPSK (EDR)
Transmit Power	Class 1 BR +10 dBm
	Class 1 EDR +9 dBm
	LE +8 dBm
Receiver sensitivity (typical values)	BR -87 dBm ± 1.5 dB
	EDR -86 dBm ± 1.5 dB
	LE -99 dBm ± 1.5 dB

Table 23: Bluetooth radio parameters

4.7.2 Wi-Fi

Parameter	Operation mode	Specification
RF Frequency range	802.11b/g/n	2.400 – 2.500 GHz
	802.11a/n/ac	4.900 – 5.925 GHz
Modulation	802.11b	CCK and DSSS
	802.11a/g/n/ac	OFDM
Supported data rates	802.11b	1, 2, 5.5, 11 Mbps
	802.11a/g	6, 9, 12, 18, 24, 36, 48, 54 Mbps
	802.11n SISO	MCS0 - MCS7 (150 Mbps)
	802.11ac SISO	MCS0 – MCS9 (433 Mbps)
Supported channel bandwidth	802.11n	20, 40 MHz
	802.11ac	20, 40, 80 MHz
Supported guard interval (GI)	802.11n	400, 800 ns
	802.11ac	Short guard interval supported

Table 24: Wi-Fi radio features and specifications

Parameter	Frequency	Operation mode	802.11 EVM limit	Specification (typ. output power tolerance ±2 dB)
Maximum transmit power	2.4 GHz	DSSS/CCK	-9 dB	19 dBm[3]
		OFDM, BPSK	-8 dB	19 dBm
		OFDM, QPSK	-13 dB	18 dBm
		OFDM, 16-QAM	-19 dB	18 dBm
		OFDM, 64-QAM, 3/4	-25 dB	17 dBm
		OFDM, 64-QAM, 5/6	-28 dB	17 dBm

[3] FCC output power limit 12 dBm

Parameter	Frequency	Operation mode	802.11 EVM limit	Specification (typ. output power tolerance ±2 dB)
	5 GHz	OFDM, BPSK	-5 dB	16 dBm
		OFDM, QPSK	-13 dB	15 dBm
		OFDM, 16-QAM	-19 dB	15 dBm
		OFDM, 64-QAM, 3/4	-25 dB	15 dBm
		OFDM, 64-QAM, 5/6	-28 dB	15 dBm
		OFDM, 256-QAM, 3/4	-30 dB	15 dBm
		OFDM, 256-QAM, 5/6	-32 dB	14 dBm

Table 25: Wi-Fi Radio maximum transmit power parameter

Band	Operating mode	Bandwidth	Data rate	Specification
2.4 GHz	802.11b	20 MHz	1 Mbps/2 Mbps	-97 dBm/-94 dBm
			5.5 Mbps/11 Mbps	-92 dBm/-88 dBm
	802.11g	20 MHz	6Mbps/9Mbps	-89 dBm/-88 dBm
			12 Mbps/18 Mbps	-86 dBm/-84 dBm
			24 Mbps/36 Mbps	-81 dBm/-79 dBm
			48 Mbps/54 Mbps	-75dBm/-73dBm
	802.11n	20 MHz	MCS0/MCS1	-89 dBm/-88 dBm
			MCS2/MCS3	-86 dBm/-84 dBm
			MCS4/MCS5	-81 dBm/-79 dBm
			MCS6/MCS7	-75 dBm/-73 dBm
5 GHz	802.11a	20 MHz	6 Mbps/9 Mbps	-88 dBm/-87 dBm
			12 Mbps/18 Mbps	-88 dBm/-86 dBm
			24 Mbps/36 Mbps	-83 dBm/-80 dBm
			48 Mbps/54 Mbps	-75 dBm/-74 dBm
	802.11ac	20 MHz	MCS0/MCS1	-88 dBm/-87 dBm
			MCS2/MCS3	-85 dBm/-82 dBm
			MCS4/MCS5	-80 dBm/-76 dBm
			MCS6/MCS7	-75 dBm/-73 dBm
			MCS8	-69 dBm
		40 MHz	MCS0/MCS1	-85 dBm/-84 dBm
			MCS2/MCS3	-82 dBm/-79 dBm
			MCS4/MCS5	-77 dBm/-73 dBm
			MCS6/MCS7	-72 dBm/-71 dBm
			MCS8/MCS9	-67 dBm/-65 dBm
		80 MHz	MCS0/MCS1	-81 dBm/-81 dBm
			MCS2/MCS3	-79 dBm/-76 dBm
			MCS4/MCS5	-74 dBm/-70 dBm
			MCS6/MCS7	-69 dBm/-68 dBm
			MCS8/MCS9	-63 dBm/-61 dBm

Table 26: Wi-Fi radio sensitivity

5 Software

JODY-W2 series modules are based on the NXP 88W8987 chipset family and the drivers and firmware required to operate JODY-W2 series modules are developed by NXP. A firmware binary is downloaded by the host operating system driver at start-up.

The following software options are available for the JODY-W2 module:

- Open-source Linux/Android driver (`mxm_mwifiex`) for mainstream use is available free of charge and already integrated into the Linux BSP for NXP i.MX application processors
- Proprietary Linux/Android drivers providing different feature packs
- MCUXpresso Wi-Fi/Bluetooth support for supported NXP MCUs

The proprietary drivers are distributed by u-blox to customers that have signed a limited use license agreement (LULA-M) with u-blox. The license can be signed electronically. Contact your local support team for more information. The driver package is also available directly from NXP.

The software packages typically include:

- Dedicated kernel driver that binds the Wi-Fi device to the kernel. Driver sources are provided.
- Dedicated Wi-Fi firmware image that is uploaded during initialization of the Wi-Fi device.
- Dedicated Bluetooth firmware image that is uploaded during initialization of the Bluetooth device.
- Laboratory and manufacturing tools.

6 Mechanical specifications

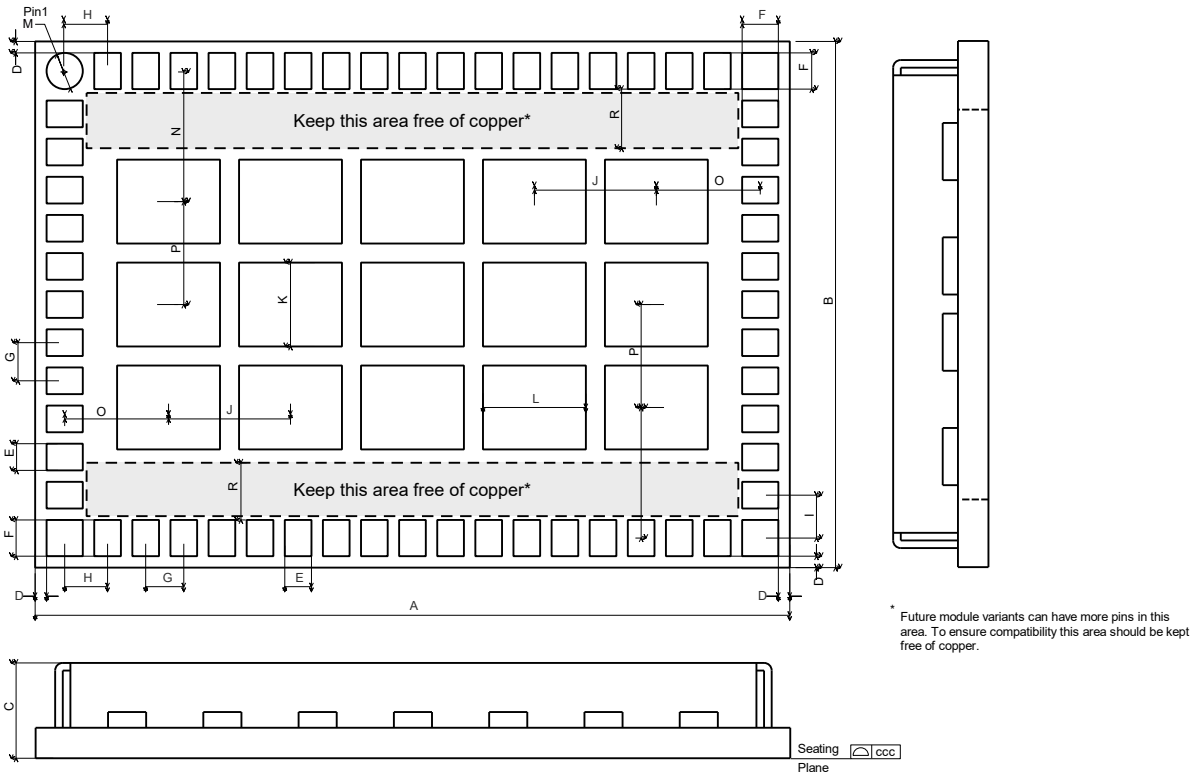


Figure 12: JODY-W2 series dimensions (bottom view)

Parameter	Description	Typical		Tolerance	
A	Module length [mm]	19.8	(779.5 mil)	+0.35/-0.1	(+13.8/-3.9 mil)
B	Module width [mm]	13.8	(543.3 mil)	+0.1/-0.1	(+3.9/-3.9 mil)
C	Module thickness [mm]	2.5	(98.4 mil)	+0.2/-0.2	(+7.9/-7.9 mil)
ccc	Seating plane coplanarity [mm]	<0.1	(3.94 mil)		
D	PCB edge-to-pin Edge [mm]	0.3	(11.8 mil)	+0.20/-0.20	(+7.9/-7.9 mil)
E	Pin width [mm]	0.7	(27.6 mil)	+0.05/-0.05	(+2.0/-2.0 mil)
F	Pin length [mm]	0.95	(37.4 mil)	+0.05/-0.05	(+2.0/-2.0 mil)
G	Pin to pin pitch [mm]	1.0	(39.4 mil)	+0.02/-0.02	(+0.8/-0.8 mil)
H	Horizontal corner pin-to-pin pitch [mm]	1.125	(44.3 mil)	+0.02/-0.02	(+0.8/-0.8 mil)
I	Lateral corner pin-to-pin pitch [mm]	1.125	(44.3 mil)	+0.02/-0.02	(+0.8/-0.8 mil)
J	Horizontal thermal pads pitch [mm]	3.2	(126.0 mil)	+0.02/-0.02	(+0.8/-0.8 mil)
K	Thermal pad height [mm]	2.2	(86 6 mil)	+0.1/-0.1	(+3.9/-3.9 mil)
L	Thermal pad length [mm]	2.7	(106.3 mil)	+0.1/-0.1	(+3.9/-3.9 mil)
M	Pin 1 diameter [mm]	0.95	(37.4 mil)	+0.05/-0.05	(+2.0/-2.0 mil)
N	Horizontal pin-to-thermal pad pitch [mm]	3.425	(134.8 mil)	+0.02/-0.02	(+0.8/-0.8 mil)
O	Lateral pin-to-thermal pad distance [mm]	2.725	(107.3 mil)	+0.02/-0.02	(+0.8/-0.8 mil)
P	Lateral thermal pads pitch [mm]	2.7	(106.3 mil)	+0.02/-0.02	(+0.8/-0.8 mil)
R	Reserved area for future module variants	1.55	(61.0 mil)	+0.05/-0.05	(+2.0/-2.0 mil)

Table 27: Description of parameters

7 Qualification and approvals

7.1 Country approvals

Table 28 describes the status of JODY-W2 module certification in each country/region.

Country/region	JODY-W263 / JODY-W263-A
Europe	Approved
Great Britain	Approved
USA	Approved
Canada	Approved
Taiwan	Approved
Japan	Approved
South Korea	Approved
Australia and New Zealand	Approved

Table 28: Country approval status

Additional country certifications can be progressed upon request. Contact your local support team for further information.

☞ For detailed information about the regulatory requirements that must be met when using JODY-W2 modules in an end product, see the system integration manual [2].

7.2 Approved antennas

JODY-W2 has been tested and approved for Bluetooth and Wi-Fi operation in the 2.4 GHz band and Wi-Fi operation in the 5 GHz band using the approved antennas described in the JODY-W2 system integration manual [2].

For information about the specifications that must be fulfilled in an end product utilizing the JODY-W2 radio type approval, see the JODY-W2 antenna reference design application note [3]. The application note provides PCB layout details and electrical specifications.

1.1 Bluetooth qualification

JODY-W2 is qualified for Bluetooth® Core 5.2 "Controller Subsystem" operation and is listed as a qualified design (QD ID: 166205) with the Bluetooth Special Interest Group (SIG). This means that there is no need to do any further qualification if the module is combined with a host stack that is qualified for Bluetooth as a "Host Subsystem".

8 Product handling

8.1 Packaging

JODY-W2 series modules are delivered as hermetically sealed, reeled tapes that enable efficient production, production lot set-up, and tear-down. For more information about the packaging, shipment, storage, and handling of JODY-W2 modules, see the Packaging reference guide [1].

8.1.1 Reels

JODY-W2 series modules are deliverable in quantities of 500 pieces on a reel. The modules are shipped on reel Type A, as described in the Packaging reference guide [1].

8.1.2 Tapes

Figure 13 shows the position, dimensions, and orientation of the JODY-W2 modules as they are delivered on tape.

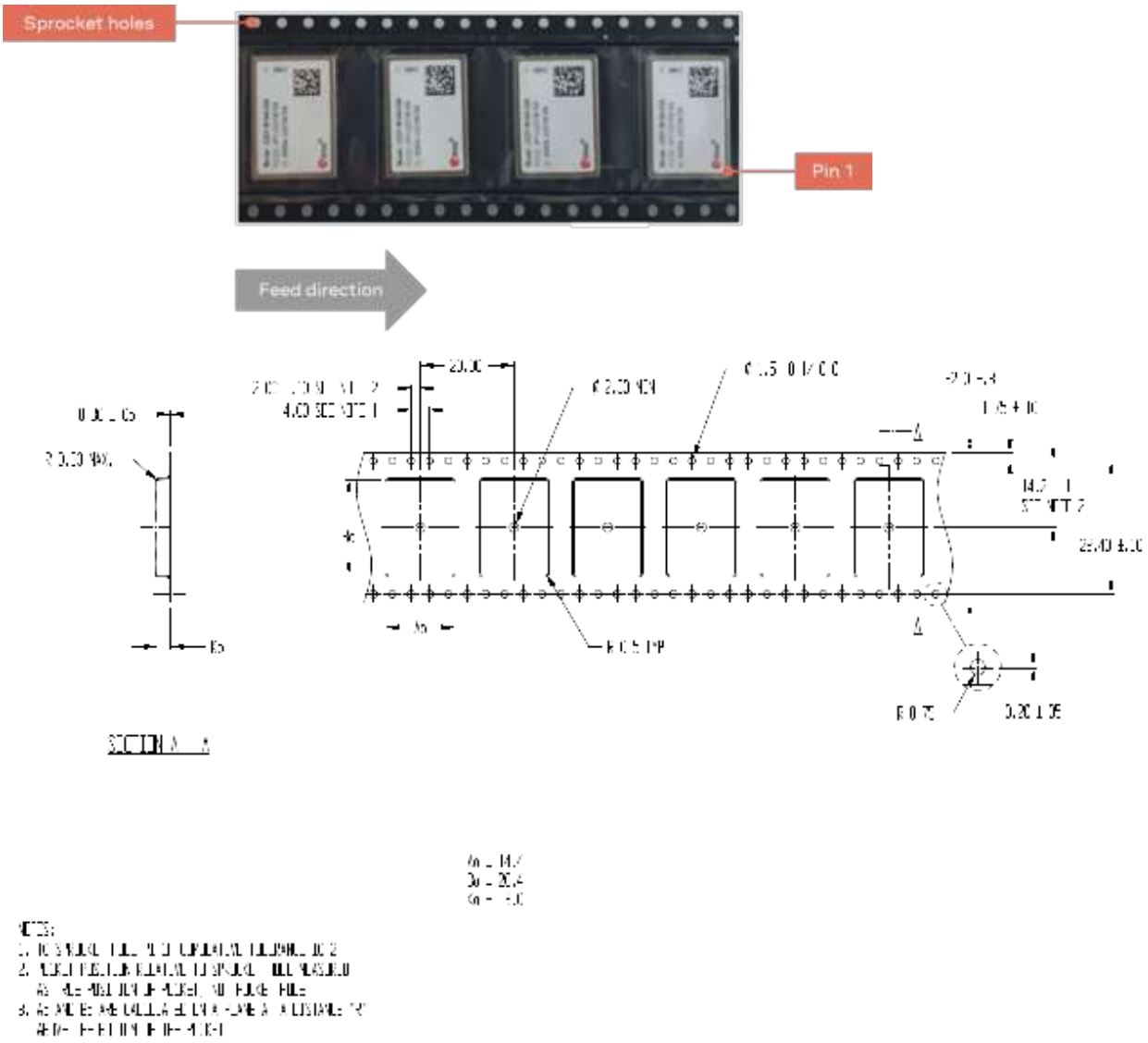


Figure 13: JODY-W2 tape orientation and dimensions

8.2 Moisture sensitivity levels

⚠ JODY-W2 series automotive-grade modules are rated at moisture sensitivity level 3. JODY-W2 series professional-grade modules are rated at moisture sensitivity level 4. A warning to highlight the moisture and static sensitivity risk is carried on each Moisture Barrier Bag (MBB) that protects the modules during shipping.

⚠ In factory conditions with maximum temperature and relative humidity of 30 °C/60%RH, modules rated at MSL3 must be mounted within 168 hours after opening the dry pack. Otherwise, the modules must be stored at less than 10%RH. In the same conditions, MSL4 modules must be mounted within 72 hours after opening the dry pack. Modules require baking if the humidity indicator card shows more than 10% when read at 23±5°C, or if any of the conditions cannot be met. Refer to J-STD-033B standards for further information about the bake procedure.

For more information about MSL (Moisture Sensitivity Level), labeling, and storage, see also the Product packaging reference guide [1].

8.3 Reflow soldering

JODY-W2 series modules are approved for a single reflow cycle only.

⚠ Reflow soldering profiles must be selected in accordance with u-blox soldering recommendations described in the system integration manual [2]. Failure to observe these recommendations can result in severe damage to the product.

8.4 ESD handling precautions

⚠ JODY-W2 series modules are electrostatic sensitive devices (ESD) that demand adherence to special ESD precautions. Failure to observe these precautions can result in severe damage to the product.

Proper ESD handling and packaging procedures must be applied throughout the processing, handling, and operation of any application that incorporates JODY-W2 series modules. ESD precautions should be implemented on the application board where the module is mounted.

For further information about the handling of JODY-W2 series modules, see also the JODY-W2 system integration manual [2].

9 Labeling and ordering information

9.1 Product labeling

The labels on both automotive and professional grade JODY-W2 series modules include important product information. Figure 14 shows the label applied to JODY-W2 series modules. Each of the given label references are described in Table 29.



Figure 14: JODY-W2 series sample label

Reference	Description
1	Product (model) name: Type number with the product version.
2	Minor product version
3	Date of production encoded YY/WW (year/week)
4	FCC/ISED ID with which the module has been listed
5	Data Matrix with unique serial number comprising 19 alphanumeric symbols: - The first 3 symbols are used for production tracking and are an abbreviated representation of the Type number that is unique to each module variant. - The following 12 symbols represent the unique hexadecimal Bluetooth address of the module AABBCCDDEEFF, and - The last 4 symbols represent the hardware and firmware version encoded HHFF.
6	u-blox logo. The red dot above the logo represents the physical location of pin 1.

Table 29: JODY-W2 series label references

9.2 Product identifiers

Table 30 describes the three product identifiers, namely the Type number, Model name and Ordering code.

Format	Description	Nomenclature
Model name	Describes the form factor, platform technology and platform variant. Used mostly in product documentation like this data sheet, the model name represents the most common identity for all u-blox products	PPPP-TGVV
Ordering code	Comprises the model name – with additional identifiers to describe the major product version and quality grade	PPPP-TGVV-TTQ
Type number	Comprises the model name and ordering code – with additional identifiers to describe minor product versions.	PPPP -TGVV-TTQ-XX

Table 30: Product code formats

Table 31 describes the identification codes associated with each module variant.

Code	Description	Example
PPPP	Form factor	JODY
TG	Platform T – Dominant technology, For example, W: Wi-Fi, B: Bluetooth G - Generation	W2
VV	Variant based on the same platform; range [00...99]	63
TT	Major product version	00
Q	Quality grade A: Automotive B: Professional C: Standard	A
XX	Minor product version (not relevant for certification)	00

Table 31: Part identification codes

9.3 Ordering codes

Ordering code	Product name	Product
JODY-W263-00A	JODY-W263-A	Automotive grade module based on NXP 88W8987(A) transceiver. Equipped with a single Wi-Fi antenna and one Bluetooth antenna, the module has an operational temperature of -40 °C to +85 °C.
JODY-W263-01A	JODY-W263-A	Automotive grade module based on NXP 88W8987S(A) transceiver. Equipped with a single Wi-Fi antenna and single Bluetooth antenna, the module has an operational temperature of -40 °C to +105 °C.
JODY-W263-00B	JODY-W263	Professional grade module based on NXP 88W8987(I) transceiver. Equipped with a single Wi-Fi antenna and single Bluetooth antenna, the module has an operational temperature of -40 °C to +85 °C.
JODY-W263-10B	JODY-W263	Professional grade module based on NXP 88W8987(E) transceiver. Equipped with a single Wi-Fi antenna and single Bluetooth antenna, the module has an operational temperature of -30 °C to +85 °C.
JODY-W263-01B	JODY-W263	Professional grade module based on NXP 88W8987(I) transceiver. Equipped with a single Wi-Fi antenna and single Bluetooth antenna, the module has an operational temperature of -40 °C to +85 °C. LTE filter for 2.4 GHz Wi-Fi and Bluetooth.
JODY-W263-10A	JODY-W263-A	Automotive grade module based on NXP 88W8987(A) transceiver. Equipped with a single Wi-Fi antenna and one Bluetooth antenna, the module has an operational temperature of -40 °C to +85 °C. LTE filter for 2.4 GHz Wi-Fi and Bluetooth.

Ordering code	Product name	Product
JODY-W263-11B	JODY-W263	Professional grade module based on NXP 88W8987(E) transceiver. Equipped with a single Wi-Fi antenna and single Bluetooth antenna, the module has an operational temperature of -30 °C to +85 °C. LTE filter for 2.4 GHz Wi-Fi and Bluetooth.

Table 32: Product ordering codes

Appendix

A Glossary

Abbreviation	Definition
AC	Alternating Current
CMD	Command
DC	Direct Current
DDR	Double Data Rate
ESD	Electrostatic Sensitive Devices
FCC	Federal Communications Commission
FIFO	First In, First Out
GI	Guard interval
GND	Ground
GPIO	General-purpose input/output
HD	High Definition
HCI	Host Controller Interface
ISED	Innovation, Science and Economic Development Canada
ISM	Industrial, scientific, and medical
LE	Bluetooth Low Energy
LTE	Long Term Evolution
LULA	Limited Use License Agreement
MAC	Medium Access Control
MIMO	Multiple Input Multiple Output
MWS	Mobile Wireless Standards
MSL	Moisture sensitivity level
NFC	Near-Field Communication
OEM	Original equipment manufacturer
P2P	Peer-to-peer
P2P (GC)	P2P Client
P2P (GO)	P2P Group Owner
PCB	Printed Circuit Board
PCI	Peripheral Component Interconnect
PCIe	PCI Express
PCN	Product Change Notification
PCM	Pulse-code modulation
POR	Power-on reset
RED	Radio Equipment Directive
RF	Radio Frequency
RSDB	Real Simultaneous Dual Band
RSS	Radio Standards Specification
RH	Relative humidity
RoHS	Restriction of Hazardous Substances

Abbreviation	Definition
SAR	Specific Absorption Rate
SCO	Synchronous Connection-Oriented
SDIO	Secure Digital Input Output
SDR	Single Data Rate
SISO	Single-input single-output
SMD	Surface-mount Device
STA	Station
TBD	To be defined
USB	Universal Serial Bus
UART	Universal Asynchronous Receiver/Transmitter
VSDB	Virtual Simultaneous Dual Band
WAPI	WLAN Authentication and Privacy Infrastructure
WLAN	Wireless Local Area Network

Table 33: Explanation of the abbreviations and terms used

Related documents

[1] Packaging information reference guide, UBX-14001652
[2] JODY-W2 series system integration manual, UBX-18068879
[3] JODY-W2 antenna reference design application note, UBX-20053581

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Revision history

Revision	Date	Name	Comments
R01	20-Nov-2018	shoe, mhei, kgom	Initial release.
R02	09-Apr-2019	vbak	Updated (Pin name “BT_DEV_WAKE”). Changed the power domain for SDIO lines (Table 15).
R03	02-May-2019	kgom	Changed product status for JODY-W263-01A-00 to Prototype.
R04	25-Apr-2020	vbak, aheg	Corrected pin 59 description and Wi-Fi/Bluetooth output power (). Added current consumption values (section 4.4 and 4.5). Updated pin list. Updated the mechanical specifications (Figure 12).
R05	7-Dec-2020	lber, aheg	Updated the regulatory compliance section with the details about on-going certifications. Approvals are pending. A further update of this data sheet will be distributed once certification reports are available.
R06	11-Dec-2020	mzes	Corrected product name and chipset references in document information and section 1.4.
R07	28-Jan-2021	vbak	Corrected Wi-Fi simultaneous operation modes in section 1.4.1.1.
R08	18-May-2021	aheg, vbak	Updated section 7 to reflect completion of certifications and availability of test reports. Updated power consumption data against the latest design using new DC-DC converter in Table 21.
R09	28-Jan-2022	mzes	Updated Bluetooth to version 5.2 and added Bluetooth qualification section. Updated Software section to include open-source and MCUXpresso software options. Added Australia and New Zealand regulatory compliance section. Removed ambiguous description of operating condition ranges in Electrical specifications and information describing ESD handling precautions duplicated in the system integration manual [2]. Updated information describing Moisture sensitivity levels, Reflow soldering, and ESD handling precautions.
R10	29-Sep-2022	frca, lfar, mzes, fkru, vbak	Added new variant JODY-W263-10B in all relevant sections. Added chipset pin descriptions and alternative functions in Table 15. Removed LTE coexistence interface. Added Taiwan, Japan, and South Korea regulatory compliance information to Approvals chapter. Added Maximum ESD ratings.
R11	07-Jun-2023	mzes	Updated product status to Mass production for JODY-W263-10B variant. Removed regulatory requirements (now described in the SIM) with summary Qualification and approvals information.
R12	16-Aug-2023	vbak	Updated table data for Absolute maximum ratings. Updated ordering codes to include the JODY-W263-01B in Document information.
R13	13-May-2026	lfar, mzes	Updated ordering codes to include JODY-W263-10A/-11B and added missing variants in Table 16: Absolute maximum ratings and Table 18: Operating conditions. Updated Moisture sensitivity levels to add information about MSL4 for professional grade modules.

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