# MPQ4423A

## 3A, 36V, High-Efficiency, Synchronous, Step-Down Converter AEC-Q100 Qualified

The Future of Analog IC Technology

## DESCRIPTION

The MPQ4423A is a high-efficiency, synchronous, rectified, step-down, switch-mode converter with built-in power MOSFETs. It offers a very compact solution that achieves 3A of continuous output current with excellent load and line regulation over a wide input supply range.

The MPQ4423A uses synchronous mode operation to achieve higher efficiency over the output current load range. Current-mode operation provides fast transient response and eases loop stabilization.

Full protection features include over-current protection (OCP) and thermal shutdown.

The MPQ4423A requires a minimal number of readily available, standard, external components and is available in a compact QFN-8 (3mmx3mm) package.

## FEATURES

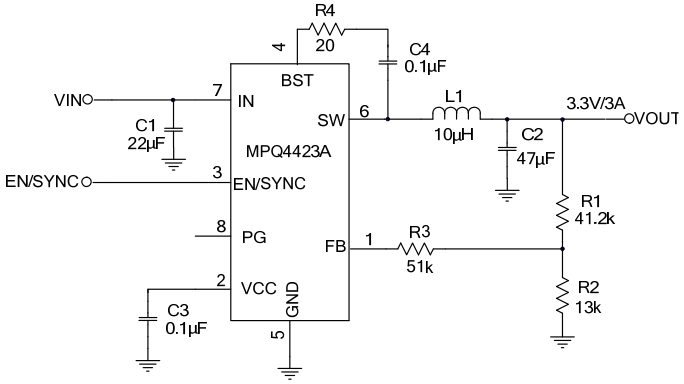
- Wide 4V to 36V Continuous Operating Input Range
- 85mΩ/55mΩ Low $R_{DS(ON)}$ Internal Power MOSFETs
- High-Efficiency Synchronous Mode Operation
- Default 410kHz Switching Frequency
- Synchronizes to a 200kHz to 2.2MHz External Clock
- High Duty Cycle for Automotive Cold Crank
- Forced CCM Mode
- Internal Soft Start
- Power Good
- Over-Current Protection (OCP) and Hiccup
- Thermal Shutdown
- Output Adjustable from 0.8V
- Available in a QFN-8 (3mmx3mm) Package
- Available in AEC-Q100 Grade 1

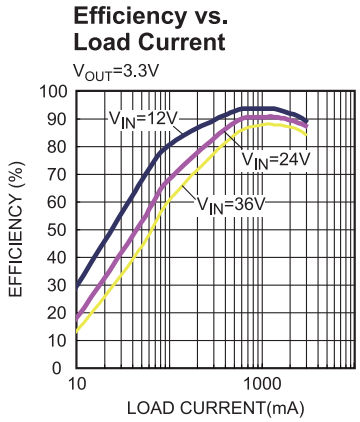
## APPLICATIONS

- Automotive
- Industrial Control System
- Distributed Power Systems

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## TYPICAL APPLICATION





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## ORDERING INFORMATION

| Part Number* | Package | Top Marking |
|---|---|---|
| MPQ4423AGQ | QFN-8 (3mmx3mm) | *See Below* |
| MPQ4423AGQ-AEC1 | QFN-8 (3mmx3mm) | |

* For Tape & Reel, add suffix –Z (e.g. MPQ4423AGQ–Z)

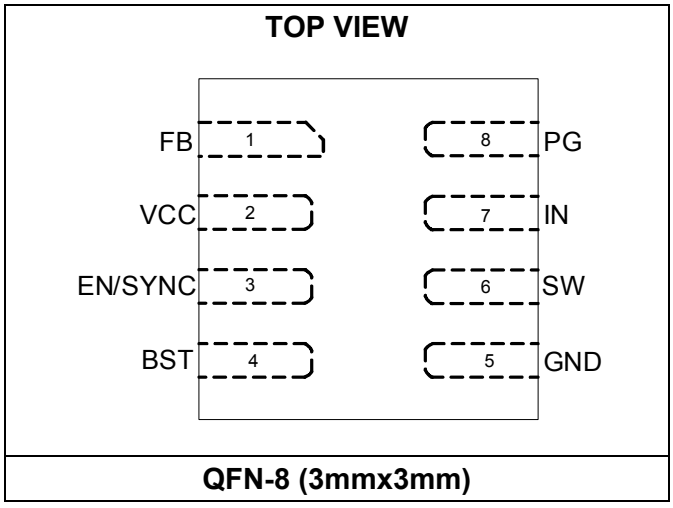
## TOP MARKING

APPY

LLL

APP: Product code of MPQ4423AGQ and MPQ4423AGQ-AEC1
Y: Year code
LLL: Lot number

## PACKAGE REFERENCE





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## ABSOLUTE MAXIMUM RATINGS (1)

$V_{IN}$ .....-0.3V to 40V
$V_{SW}$.....-0.3V to 41V
$V_{BS}$ ..... $V_{SW}$ + 6V
All other pins ..... -0.3V to 6V (2)
Continuous power dissipation ($T_A$ = +25°C) (3)
QFN-8 (3mmx3mm)..... 2.27W
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature..... -65°C to 150°C

### *Recommended Operating Conditions*

Continuous supply voltage ($V_{IN}$).....4V to 36V
Output voltage ($V_{OUT}$).....0.8V to 0.9 x $V_{IN}$
Operating junction temp. ($T_J$)… -40°C to +125°C

### *Thermal Resistance* (4) $\theta_{JA}$ $\theta_{JC}$

| | | |
|---|---|---|
| QFN-8 (3mmx3mm) | 55 | 13 °C/W |

**NOTES:**

1) Absolute maximum ratings are rated under room temperature unless otherwise noted. Exceeding these ratings may damage the device.
2) For details on EN's ABS MAX rating, please refer to the Enable/SYNC Control section on page 14.
3) The maximum allowable power dissipation is a function of the maximum junction temperature $T_J$ (MAX), the junction-to-ambient thermal resistance $\theta_{JA}$, and the ambient temperature $T_A$. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_D$ (MAX) = ($T_J$ (MAX)-$T_A$)/$\theta_{JA}$. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) Measured on JESD51-7, 4-layer PCB.


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## ELECTRICAL CHARACTERISTICS

**$V_{IN}$ = 12V, $T_J$ = -40°C to +125°C, unless otherwise noted. Typical values are at $T_J$ = +25°C.**

| Parameter | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Supply current (shutdown) | $I_{SHDN}$ | $V_{EN}$ = 0V | | | 8 | μA |
| Supply current (quiescent) | $I_Q$ | $V_{EN}$ = 2V, $V_{FB}$ = 1V, no switching | | 0.6 | 0.8 | mA |
| HS switch on resistance | $R_{ON_HS}$ | $V_{BST-SW}$ = 5V | | 85 | 150 | mΩ |
| LS switch on resistance | $R_{ON_LS}$ | $V_{CC}$ = 5V | | 55 | 105 | mΩ |
| Switch leakage | $I_{LKG_SW}$ | $V_{EN}$ = 0V, $V_{SW}$ = 12V | | | 1 | μA |
| Current limit | $I_{LIMIT}$ | Under 40% duty cycle | 3.6 | 5.7 | 7.8 | A |
| Oscillator frequency | $f_{SW}$ | $V_{FB}$ = 750mV | 320 | 410 | 500 | kHz |
| Foldback frequency | $f_{FB}$ | $V_{FB}$ < 400mV | 70 | 100 | 130 | kHz |
| Maximum duty cycle | $D_{MAX}$ | $V_{FB}$ = 750mV, 410kHz | 92 | 95 | | % |
| Minimum on time[5] | $t_{ON_MIN}$ | | | 70 | | ns |
| Sync frequency range | $f_{SYNC}$ | | 0.2 | | 2.4 | MHz |
| Feedback voltage | $V_{FB}$ | $T_J$ = 25°C | 780 | 792 | 804 | mV |
| | | | 776 | | 808 | |
| Feedback current | $I_{FB}$ | $V_{FB}$ = 820mV | | 10 | 100 | nA |
| EN rising threshold | $V_{EN_RISING}$ | | 1.15 | 1.4 | 1.65 | V |
| EN falling threshold | $V_{EN_FALLING}$ | | 1.05 | 1.25 | 1.45 | V |
| EN threshold hysteresis | $V_{EN_HYS}$ | | | 150 | | mV |
| EN input current | $I_{EN}$ | $V_{EN}$ = 2V | | 4 | 8 | μA |
| | | $V_{EN}$ = 0 | | 0 | 0.2 | μA |
| $V_{IN}$ under-voltage lockout threshold rising | $INUV_{RISING}$ | | 3.3 | 3.5 | 3.7 | V |
| $V_{IN}$ under-voltage lockout threshold falling | $INUV_{FALLING}$ | | 3.1 | 3.3 | 3.5 | V |
| $V_{IN}$ under-voltage lockout threshold hysteresis | $INUV_{HYS}$ | | | 200 | | mV |
| VCC regulator | $V_{CC}$ | $I_{CC}$ = 0mA | 4.6 | 4.9 | 5.2 | V |
| VCC load regulation | | $I_{CC}$ = 5mA | | 1.5 | 4 | % |
| Soft-start period | $t_{SS}$ | $V_{OUT}$ from 10% to 90% | 0.45 | 1. 5 | 2.55 | ms |
| Thermal shutdown [5] | | | 150 | 170 | | °C |
| Thermal hysteresis [5] | | | | 30 | | °C |
| PG rising threshold | $PG_{Vth_RISING}$ | as a percentage of $V_{FB}$ | 86 | 90 | 94 | % |
| PG falling threshold | $PG_{Vth_FALLING}$ | as a percentage of $V_{FB}$ | 80 | 84 | 88 | % |


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## ELECTRICAL CHARACTERISTICS *(continued)*

**$V_{IN}$ = 12V, $T_J$ = -40°C to +125°C, unless otherwise noted. Typical values are at $T_J$ = +25°C.**

| Parameter | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| PG threshold hysteresis | $PG_{Vth_HYS}$ | as a percentage of $V_{FB}$ | | 6 | | % |
| PG rising delay | $PG_{Td_RISING}$ | | 40 | 90 | 160 | µs |
| PG falling delay | $PG_{Td_FALLING}$ | | 30 | 55 | 95 | µs |
| PG sink current capability | $V_{PG}$ | Sink 4mA | | 0.1 | 0.3 | V |
| PG leakage current | $I_{LKG_PG}$ | | | 10 | 100 | nA |

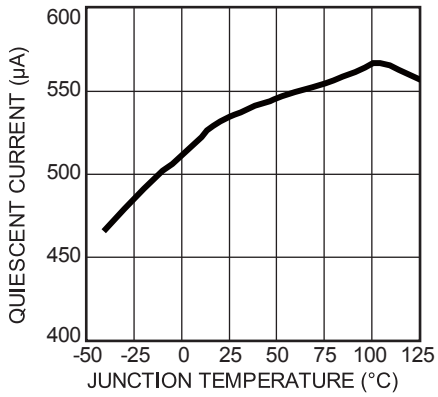
**NOTE:**

5) Derived from bench characterization. Not tested in production

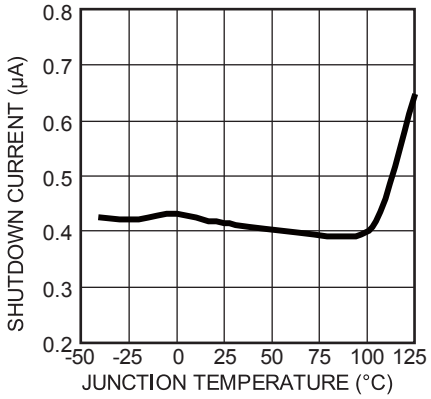

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## TYPICAL CHARACTERISTICS

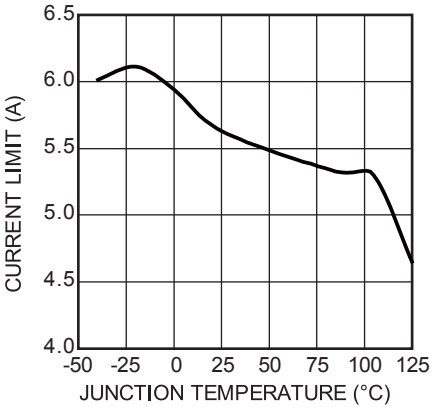
**Quiescent Current vs. Junction Temperature**
$V_{IN}$=12V



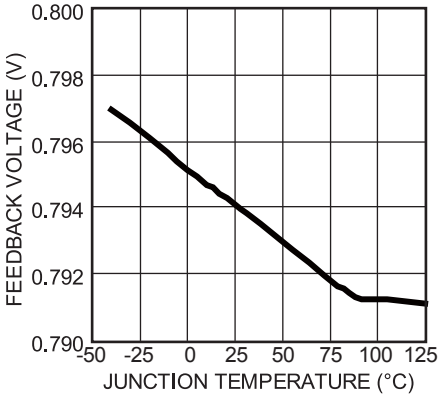

**Shutdown Current vs. Junction Temperature**
$V_{IN}$=12V



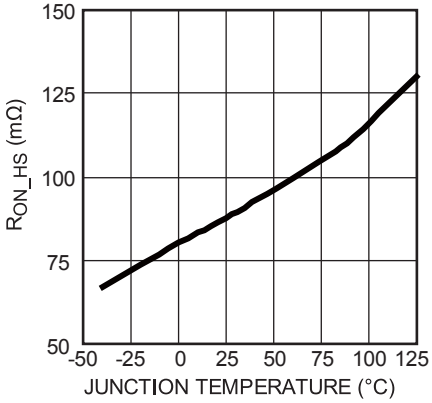

**Current Limit vs. Junction Temperature**
Duty Cycle=40%



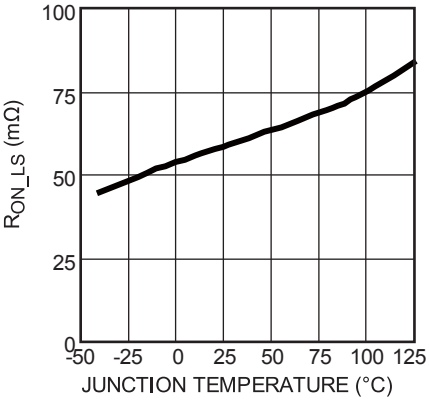

**Feedback Voltage vs. Junction Temperature**
$V_{IN}$=12V



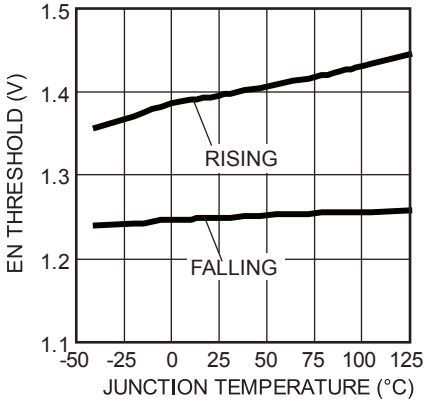

**$R_{ON_HS}$ vs. Junction Temperature**
$V_{IN}$=12V, BST-SW=5V



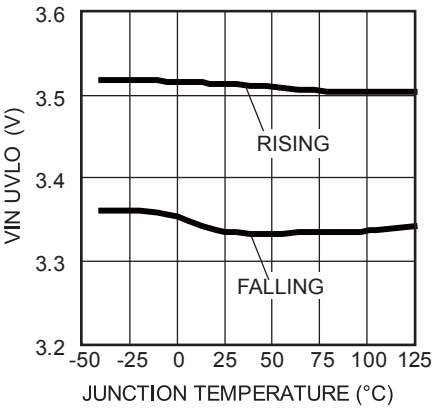

**$R_{ON_LS}$ vs. Junction Temperature**
$V_{IN}$=12V, $V_{CC}$=5V



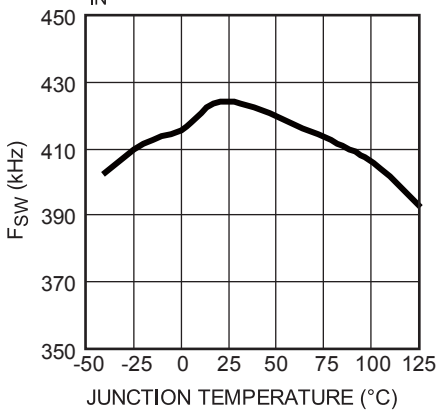

**EN Threshold vs. Junction Temperature**
$V_{IN}$=12V




**$V_{IN}$ UVLO vs. Junction Temperature**




**$F_{SW}$ vs. Junction Temperature**
$V_{IN}$=12V

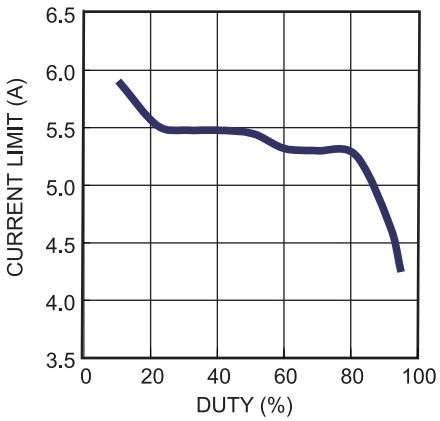




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## TYPICAL CHARACTERISTICS *(continued)*

**Current Limit vs. Duty**



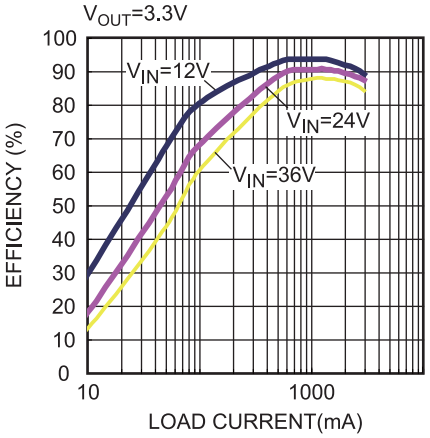


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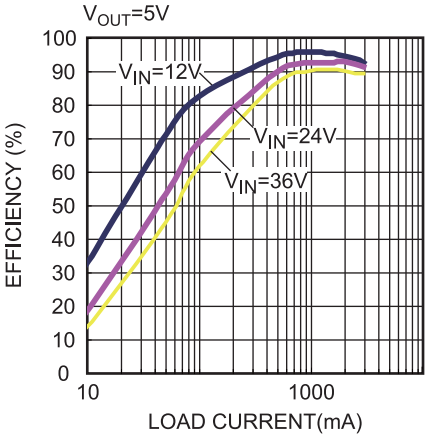
## TYPICAL PERFORMANCE CHARACTERISTICS

**$V_{IN}$ = 12V, $V_{OUT}$ = 3.3V, L = 10µH, $R_{BST}$ = 20Ω, $T_A$ = +25°C, unless otherwise noted.**

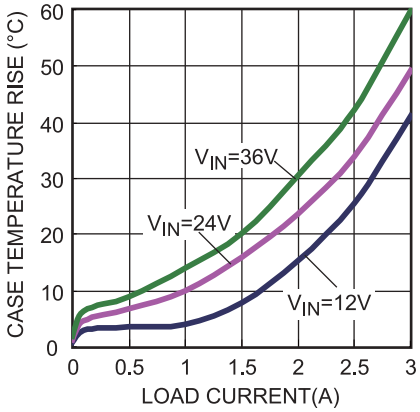
### Efficiency vs. Load Current



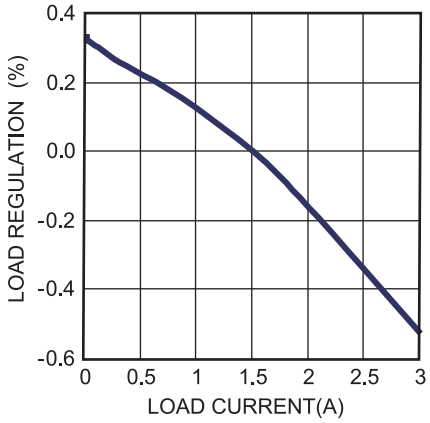

### Efficiency vs. Load Current



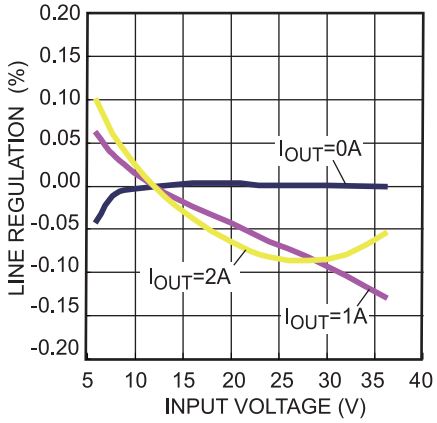

### Thermal Rise




### Load Regulation




### Line Regulation



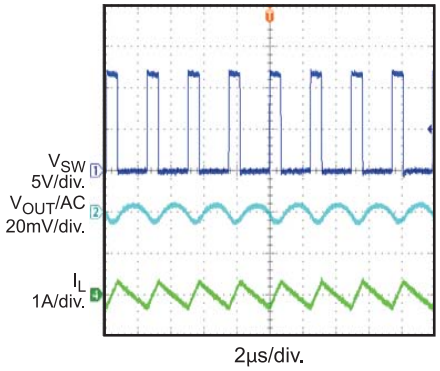


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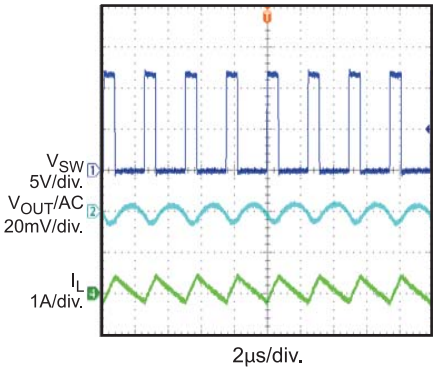
## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**$V_{IN}$ = 12V, $V_{OUT}$ = 3.3V, L = 10µH, $R_{BST}$ = 20Ω, $T_A$ = +25°C, unless otherwise noted.**

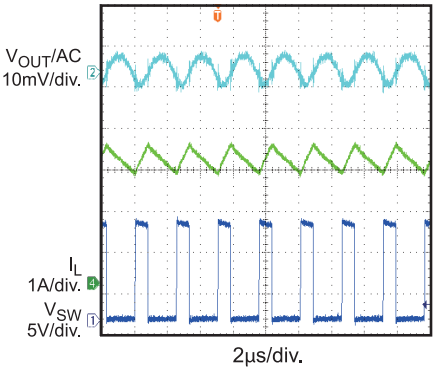
### Steady State
$I_{OUT}$=0A



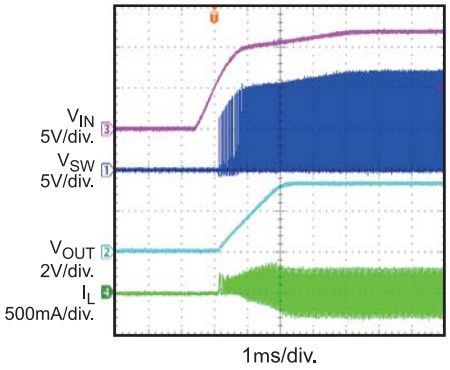

### Steady State
$I_{OUT}$ = 0.1A



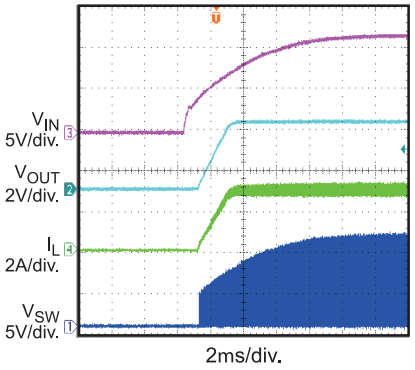

### Steady State
$I_{OUT}$=3A



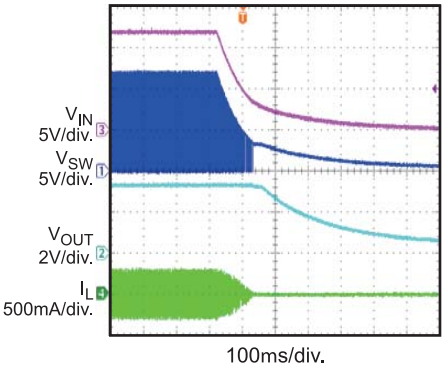

### Start-Up through $V_{IN}$
$I_{OUT}$=0A



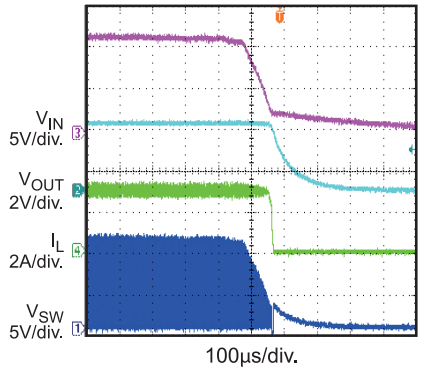

### Start-Up through $V_{IN}$
$I_{OUT}$=3A



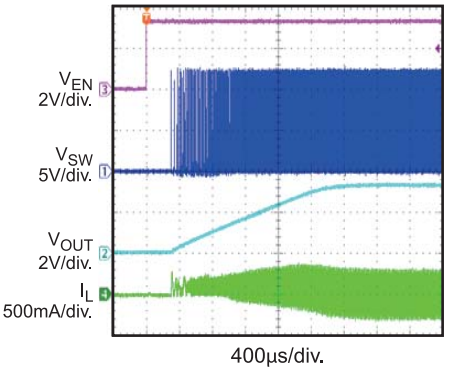

### Shutdown through $V_{IN}$
$I_{OUT}$=0A



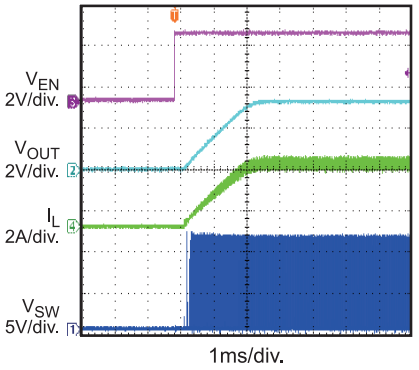

### Shutdown through $V_{IN}$
$I_{OUT}$=3A




### Start-Up through EN
$I_{OUT}$=0A




### Start-Up through EN
$I_{OUT}$=3A



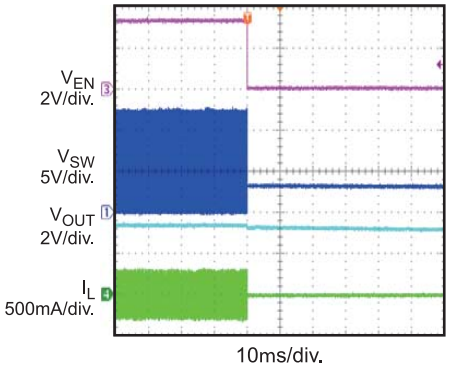


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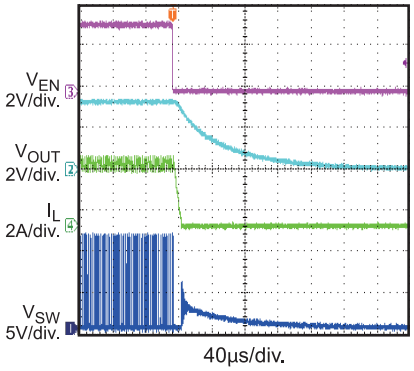
## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**$V_{IN}$ = 12V, $V_{OUT}$ = 3.3V, L = 10µH, $R_{BST}$ = 20Ω, $T_A$ = +25°C, unless otherwise noted.**

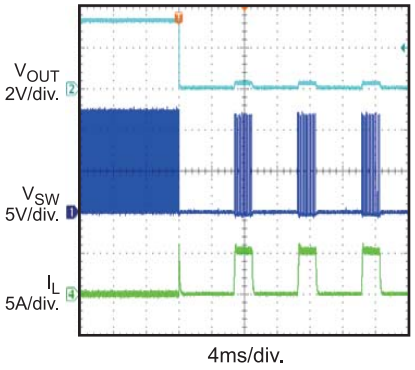
### Shutdown through EN
$I_{OUT}$=0A



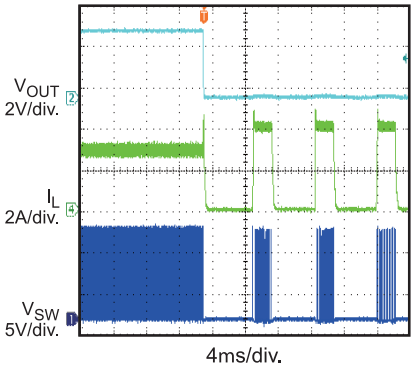

### Shutdown through EN
$I_{OUT}$=3A



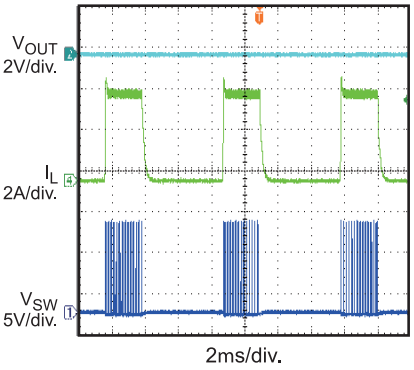

### SCP Entry
$I_{OUT}$=0A to Short Circuit



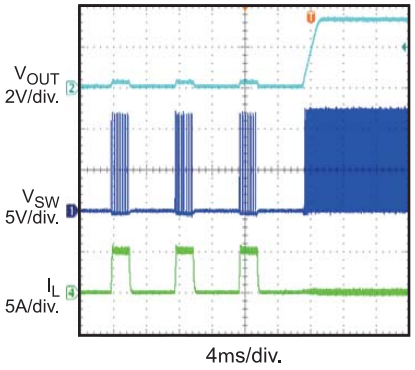

### SCP Entry
$I_{OUT}$=3A to Short Circuit



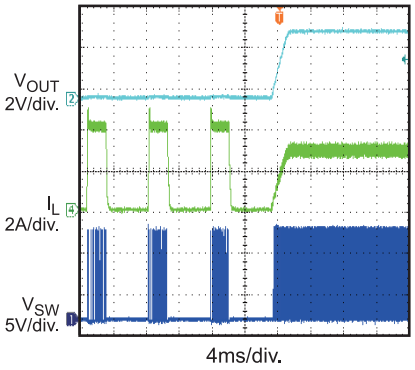

### SCP Steady State



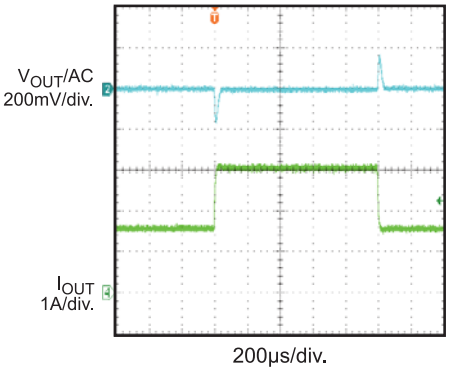

### SCP Recovery
Short Circuit to $I_{OUT}$=0A



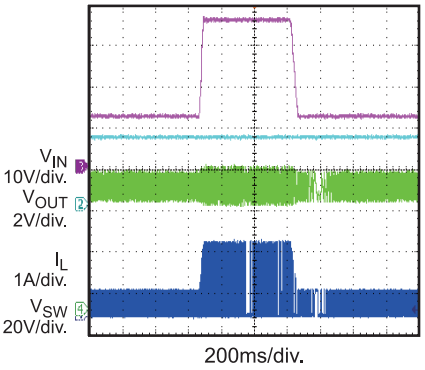

### SCP Recovery
Short Circuit to $I_{OUT}$=3A




### Load Transient
$I_{OUT}$=1.5A<->3A, 1.6A/µs




### Load Dump
$V_{IN}$=12V<->36V, $I_{OUT}$=3A





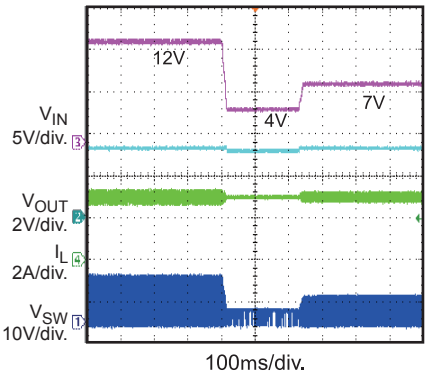
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## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**$V_{IN}$ = 12V, $V_{OUT}$ = 3.3V, L = 10µH, $R_{BST}$ = 20Ω, $T_A$ = +25°C, unless otherwise noted.**

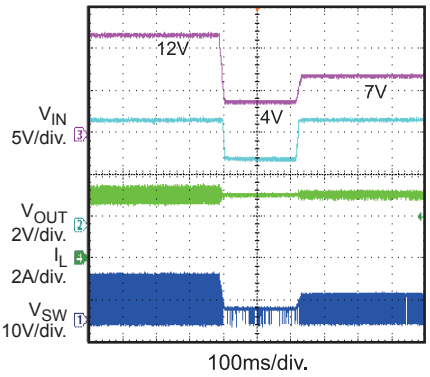
**Cold Crank**

$V_{OUT}$=3.3V, $I_{OUT}$=3A




**Cold Crank**

$V_{OUT}$=5V, $I_{OUT}$=3A





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## PIN FUNCTIONS

| Pin # | Name | Description |
|---|---|---|
| 1 | FB | **Feedback.** Connect FB to the tap of an external resistor divider from the output to GND to set the output voltage. When the FB voltage is below 660mV, the frequency foldback comparator lowers the oscillator frequency to prevent current limit runaway during a short-circuit fault condition. |
| 2 | VCC | **Bias supply.** Decouple VCC with a 0.1μF to 0.22μF capacitor. Select a capacitor that does not exceed 0.22μF. |
| 3 | EN/SYNC | **Enable/synchronize.** Drive EN/SYNC high to enable the MPQ4423A. Apply an external clock to EN/SYNC to change the switching frequency. |
| 4 | BST | **Bootstrap.** A capacitor connected between SW and BST is required to form a floating supply across the high-side switch driver. A 20Ω resistor placed between the SW and BST cap is strongly recommended to reduce SW voltage spikes. |
| 5 | GND | **System ground.** GND is the reference ground of the regulated output voltage. GND requires special consideration during PCB layout. For best results, connect GND with copper traces and vias. |
| 6 | SW | **Switch output.** Connect using a wide PCB trace. |
| 7 | IN | **Supply voltage.** The MPQ4423A operates from a 4V to 36V input rail. C1 is required to decouple the input rail. Connect using a wide PCB trace. |
| 8 | PG | **Power good.** The output of PG is an open drain and goes high if the output voltage exceeds 90% of the nominal voltage. |


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## BLOCK DIAGRAM

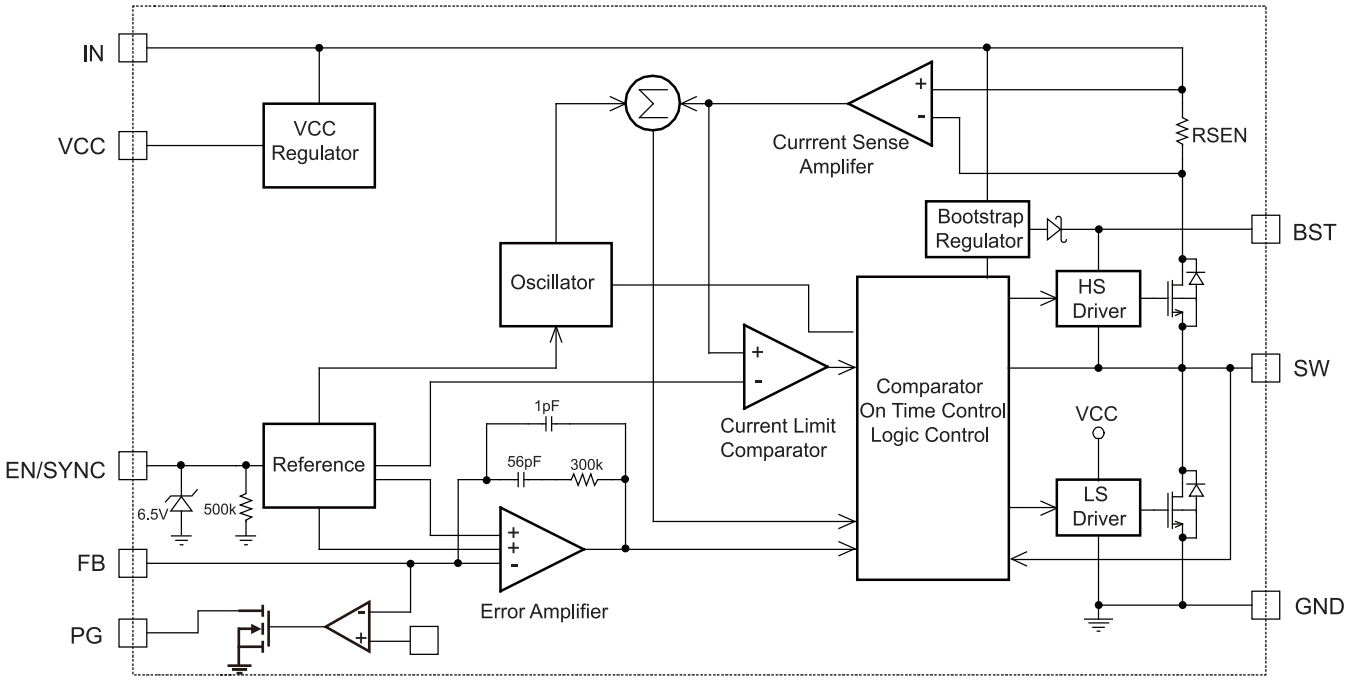



**Figure 1: Functional Block Diagram**


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## OPERATION

The MPQ4423A is a high-efficiency, synchronous, rectified, step-down, switch-mode converter with built-in power MOSFETs. It offers a very compact solution that achieves 3A of continuous output current with excellent load and line regulation over a wide input supply range.

The MPQ4423A operates in a fixed-frequency, peak-current-control mode to regulate the output voltage. An internal clock initiates a PWM cycle. The integrated high-side power MOSFET (HS-FET) turns on and remains on until its current reaches the value set by the COMP voltage ($V_{COMP}$). When the power switch is off, it remains off until the next clock cycle begins. If the current in the power MOSFET does not reach the current value set by COMP within 95% of one PWM period, the power MOSFET is forced off.

### Internal Regulator

The 5V internal regulator powers most of the internal circuitries. This regulator takes the $V_{IN}$ input and operates in the full $V_{IN}$ range. When $V_{IN}$ exceeds 5.0V, the output of the regulator is in full regulation; when $V_{IN}$ falls below 5.0V, the output of the regulator decreases following $V_{IN}$. A 0.1μF decoupling ceramic capacitor is needed at VCC.

### Error Amplifier (EA)

The error amplifier compares the FB voltage against the internal 0.8V reference (REF) and outputs a COMP voltage that controls the power MOSFET current. The optimized internal compensation network minimizes the external component count and simplifies the control loop design.

### Enable/SYNC Control

EN/SYNC is a digital control that turns the regulator on and off. Drive EN/SYNC high to turn on the regulator; drive EN/SYNC low to turn off the regulator. An internal 500kΩ resistor from EN/SYNC to GND allows EN/SYNC to be floated to shut down the chip.

EN/SYNC is clamped internally using a 6.5V series Zener diode (see Figure 2). Connect the EN/SYNC input through a pull-up resistor to any voltage connected to $V_{IN}$. The pull-up resistor limits the EN/SYNC input current below 150μA.

For example, with 12V connected to $V_{IN}$, $R_{PULLUP}$ ≥ (12V - 6.5V) ÷ 150μA = 36.7kΩ.

Connecting EN/SYNC directly to a voltage source without a pull-up resistor requires limiting the voltage amplitude below or equal to 6V to prevent damage to the Zener diode.

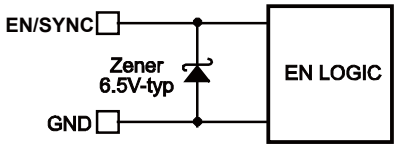



**Figure 2: 6.5V-Type Zener Diode**

To use the synchronous function, connect an external clock in the range of 200kHz to 2.2MHz to EN/SYNC. The external clock should be connected at least 2ms after the output voltage is set. The internal clock rising edge is synchronized to the external clock rising edge when the external clock is connected. The pulse width of the external clock signal should be below 1.7μs.

### Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The MPQ4423A UVLO comparator monitors the output voltage of the internal regulator (VCC). The UVLO rising threshold is about 3.5V, while its falling threshold is 3.3V.

### Internal Soft Start (SS)

The soft start (SS) prevents the converter output voltage from overshooting during start-up. When the chip starts up, the internal circuitry generates a soft-start voltage that ramps up from 0V to 1.2V. When SS is lower than REF, SS overrides REF so the error amplifier uses SS as the reference. When SS exceeds REF, the error amplifier uses REF as the reference. The SS time is internally set to 1.5ms.

### Over-Current Protection (OCP) and Hiccup

The MPQ4423A uses a cycle-by-cycle over-current limit when the inductor current peak value exceeds the set current-limit threshold. If the output voltage drops until FB is below the under-voltage (UV) threshold (typically 84% below the reference), the MPQ4423A enters hiccup mode to restart the part periodically. This protection mode is especially useful when the output is dead-shorted to ground.


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The average short-circuit current is reduced greatly to alleviate the thermal issue and to protect the regulator. The MPQ4423A exits hiccup mode once the over-current condition is removed.

### Thermal Shutdown

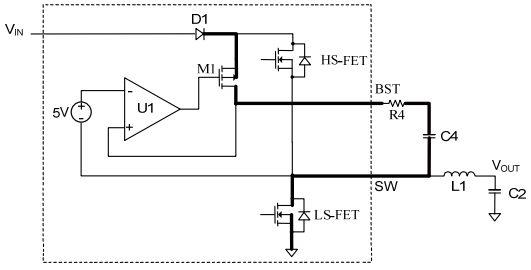
Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 170°C, the entire chip shuts down. When the temperature drops below its lower threshold (typically 140°C), the chip is enabled again.

### Floating Driver and Bootstrap Charging

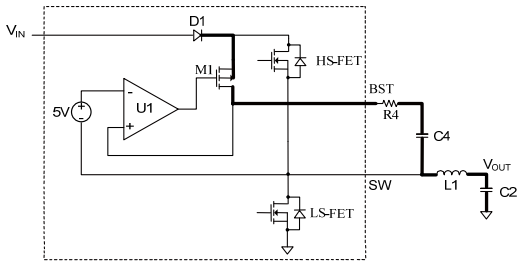
An external bootstrap capacitor powers the floating power MOSFET driver. A dedicated internal regulator charges and regulates the bootstrap capacitor voltage to about 5V (see Figure 3).

When the voltage between the BST and SW nodes drops below regulation, a PMOS pass transistor connected from $V_{IN}$ to BST turns on. The charging current path is from $V_{IN}$ to BST and then to SW. The external circuit should provide enough voltage headroom to facilitate charging. As long as $V_{IN}$ is higher than SW significantly, the bootstrap capacitor remains charged. When the HS-FET is on, $V_{IN}$ is approximately equal to $V_{SW}$, so the bootstrap capacitor cannot charge. When the LS-FET is on, $V_{IN}$ - $V_{SW}$ reaches its maximum for fast charging (the charging path is shown in Figure 3a). When the HS-FET and LS-FET are both off, $V_{SW}$ is equal to $V_{OUT}$, so the difference between $V_{IN}$ and $V_{OUT}$ can charge the bootstrap capacitor (the charging path is shown in Figure 3b).

The floating driver has its own UVLO protection, with a rising threshold of 2.2V and hysteresis of 150mV. A 20Ω resistor placed between the SW and BST cap is strongly recommended to reduce SW voltage spikes.




**3a: BST Charging Path when LS-FET is On**




**3b: BST Charging Path when HS-FET and LS-FET are Both Off**

**Figure 3: Internal Bootstrap Charging Circuit**

### Start-Up and Shutdown

If both $V_{IN}$ and EN exceed their appropriate thresholds, the chip starts up. The reference block starts first, generating a stable reference voltage and current, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

Three events can shut down the chip: EN low, $V_{IN}$ low and thermal shutdown. In the shutdown procedure, the signaling path is blocked first to avoid any fault triggering. $V_{COMP}$ and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command.

### Power Good (PG)

The MPQ4423A has a power good (PG) output. PG is the open drain of the MOSFET. It should be connected to VCC or another voltage source through a resistor (e.g.: 100kΩ). In the presence of an input voltage, the MOSFET turns on so that PG is pulled low before SS is ready. When $V_{FB}$ reaches 90%xREF, PG is pulled high after a delay (typically 90μs). When $V_{FB}$ drops to 84%xREF, PG is pulled low. PG is also pulled low if thermal shutdown occurs or if EN is pulled low.


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# APPLICATION INFORMATION

### Setting the Output Voltage

The external resistor divider sets the output voltage (see Typical Application on page 1). The feedback resistor (R1) sets the feedback loop bandwidth with the internal compensation capacitor. Choose R1 to be around 40kΩ. R2 can then be calculated with Equation (1):

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.792V} - 1} \quad (1)$$

The T-type network is highly recommended when $V_{OUT}$ is low (see Figure 4).

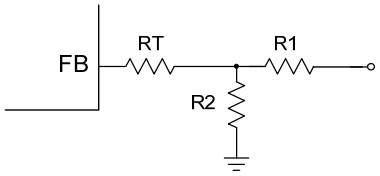



**Figure 4: T-Type Network**

RT + R1 is used to set the loop bandwidth. The higher RT + R1 is, the lower the bandwidth is. To ensure loop stability, it is strongly recommended to limit the bandwidth below 40kHz based on the 410kHz default $f_{sw}$. Table 1 lists the recommended T-type resistor values for common output voltages.

**Table 1: Resistor Selection for Common Output Voltages**

| $V_{OUT}$ (V) | R1 (kΩ) | R2 (kΩ) | RT (kΩ) |
|---|---|---|---|
| 3.3 | 41.2 (1%) | 13 (1%) | 51 (1%) |
| 5 | 41.2 (1%) | 7.68 (1%) | 51 (1%) |

### Selecting the Inductor

Use a 1μH to 10μH inductor with a DC current rating at least 25% higher than the maximum load current for most applications. For the highest efficiency, an inductor with a small DC resistance is recommended. For most designs, the inductance value can be derived from Equation (2):

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}} \quad (2)$$

Where $\Delta I_L$ is the inductor ripple current.

Choose the inductor ripple current to be approximately 30% of the maximum load current. The maximum inductor peak current can be calculated with Equation (3):

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (3)$$

Use a larger inductor for improved efficiency below 100mA under light-load conditions.

### $V_{IN}$ Under-Voltage Lockout (UVLO) Setting

The MPQ4423A has an internal, fixed, under-voltage lockout (UVLO) threshold. The rising threshold is 3.5V, while its falling threshold is about 3.3V. The application needs a higher UVLO point, so the external resistor divider between EN/SYNC and IN can be used to achieve a higher equivalent UVLO threshold (see Figure 5).

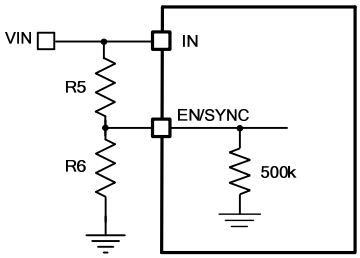



**Figure 5: Adjustable UVLO using EN/SYNC Divider**

The UVLO threshold can be calculated with Equation (4) and Equation (5):

$$INUV_{RISING} = (1 + \frac{R5}{500k//R6}) \times V_{EN_RISING} \quad (4)$$

$$INUV_{FALLING} = (1 + \frac{R5}{500k//R6}) \times V_{EN_FALLING} \quad (5)$$

Where $V_{EN_RISING}$ is 1.4V and $V_{EN_FALLING}$ is 1.25V.

When selecting R5, ensure that it is large enough to limit the current flows into EN/SYNC below 150μA.

### Selecting the Input Capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply AC current to the step-down converter while maintaining the DC input voltage. For best performance, use low ESR capacitors. Ceramic capacitors with X5R or X7R dielectrics are recommended because of their low ESR and small temperature coefficients.


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For most applications, a 22µF ceramic capacitor is sufficient to maintain the DC input voltage. It is strongly recommended to use another lower value capacitor (e.g.: 1µF) with a small package size (0603) to absorb high-frequency switching noise. Place the smaller capacitor as close to IN and GND as possible (see PCB Layout Guidelines on page 18).

Since C1 absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated with Equation (6):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (6)$$

The worse case condition occurs at $V_{IN} = 2V_{OUT}$, shown in Equation (7):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (7)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality ceramic capacitor (e.g.: 1µF) placed as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent an excessive voltage ripple at input. The input voltage ripple caused by capacitance can be estimated with Equation (8):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (8)$$

### Selecting the Output Capacitor

The output capacitor (C2) maintains the DC output voltage. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For best results, use low ESR capacitors to keep the output voltage ripple low. The output voltage ripple can be estimated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C2}\right) \quad (9)$$

Where $L_1$ is the inductor value and $R_{ESR}$ is the equivalent series resistance (ESR) value of the output capacitor.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes the majority of the output voltage ripple. For simplification, the output voltage ripple can be estimated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^2 \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (10)$$

With tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (11)$$

The characteristics of the output capacitor also affect the stability of the regulation system. The MPQ4423A can be optimized for a wide range of capacitance and ESR values.

### BST Resistor and External BST Diode

A 20Ω resistor in series with a BST capacitor is recommended to reduce SW voltage spikes. A higher resistance is better for SW spike reduction but compromises efficiency.

An external BST diode can enhance the efficiency of the regulator when the duty cycle is high (>65%). A power supply between 2.5V and 5V can be used to power the external bootstrap diode. Either VCC or VOUT can be used as the power supply in this circuit (see Figure 6).

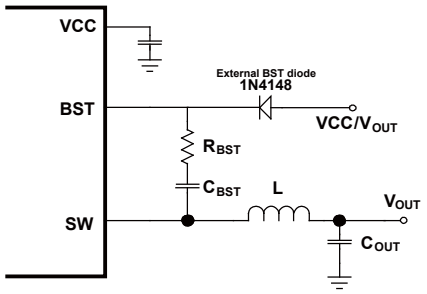



**Figure 6: Optional External Bootstrap Diode to Enhance Efficiency**

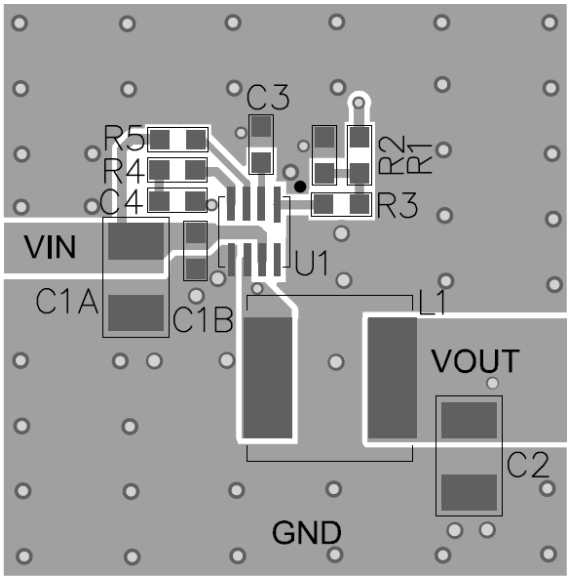
The recommended external BST diode is IN4148, and the recommended BST capacitor value is 0.1µF to 1µF.


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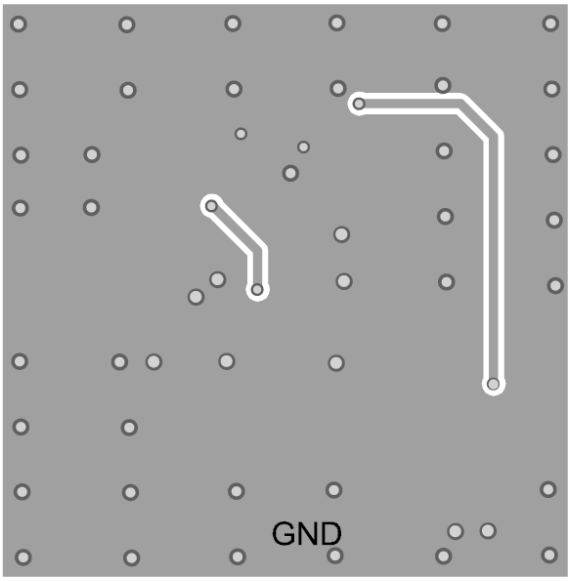
## PCB Layout Guidelines

Efficient PCB layout, especially the input capacitor and VCC capacitor placement, is critical for stable operation. For best results, refer to Figure 7 and follow the guidelines below.

1. Place the ceramics input capacitor as close to IN and GND as possible, especially the small package size (0603) input bypass capacitor.
2. Keep the connection of the input capacitor and IN as short and wide as possible.
3. Place the VCC capacitor to VCC and GND as close as possible.
4. Make the trace length of VCC to the capacitor to GND as short as possible.
5. Use a large ground plane connected directly to GND.
6. Add vias near GND if the bottom layer is the ground plane.
7. Route SW and BST away from sensitive analog areas such as FB.
8. Place the T-type feedback resistor close to the chip to ensure that the trace connecting to FB is as short as possible.




**Top Layer**




**Bottom Layer**

**Figure 7: Recommended PCB Layout**


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## TYPICAL APPLICATION CIRCUITS

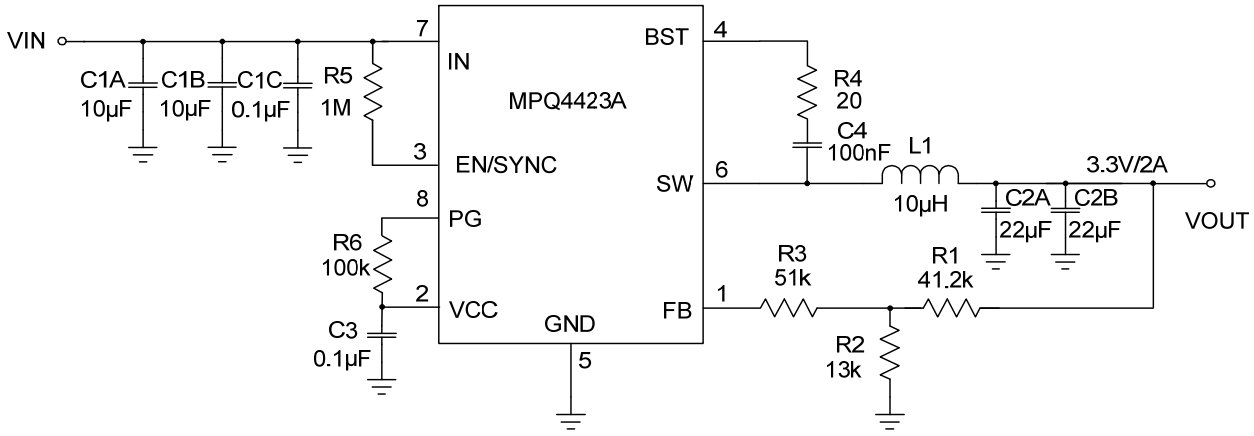
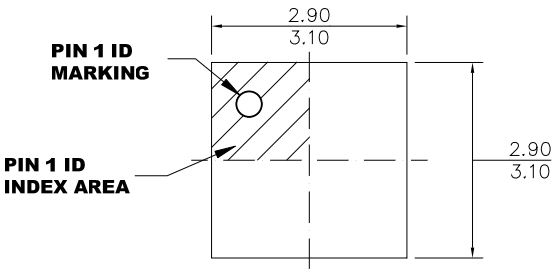


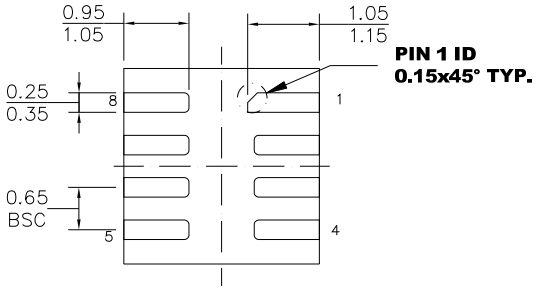

**Figure 8: 3.3V Output Typical Application Circuit**


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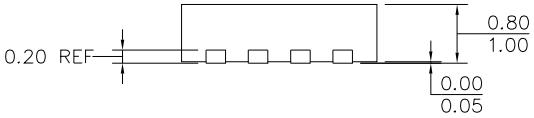
# PACKAGE INFORMATION

**QFN-8 (3mmx3mm)**

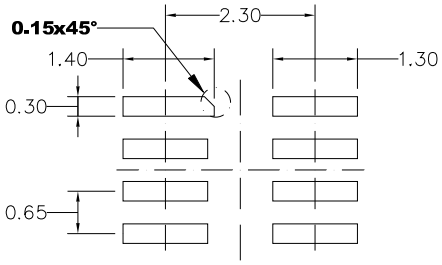



**TOP VIEW** **BOTTOM VIEW**




**SIDE VIEW**




**RECOMMENDED LAND PATTERN**

**NOTE:**

**1) ALL DIMENSIONS ARE IN MILLIMETERS.**
**2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.**
**3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.**
**4) JEDEC REFERENCE IS MO-220.**
**5) DRAWING IS NOT TO SCALE.**

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