A4413

Adjustable Frequency Buck or Buck-Boost Pre-Regulator with Synchronous Buck, 5 V Protected LDO, Pulse-Width Window Watchdog, and NPOR

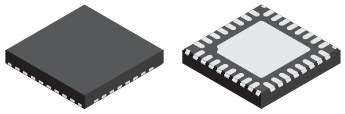
FEATURES AND BENEFITS

- Automotive AEC-Q100 qualified
- 3.5 to 36 V_{IN} operating range, 40 V_{IN} maximum
- Buck or buck-boost pre-regulator (VREG)
- Adjustable PWM switching frequency: 250 kHz to 2.4 MHz
- PWM frequency can be synchronized to external clock
- Synchronous buck regulator (ADJ) delivers 0.8 to 3.3 V
- 5 V internal LDO for remote sensors with foldback short-circuit and short-to-battery protections (V5P)
- Programmable pulse-width window watchdog (PWWD) with scalable activation delay and selectable tolerance
- Internal watchdog clock with ±5% accuracy
- Accepts external WD clock for extreme accuracy
- Active-low Watchdog Enable pin (WD_{ENn})
- Dual bandgaps for increased reliability: BG_{VREF}, BG_{FAULT}
- Power-on reset (NPOR) with rising delay of 2 ms monitors the synchronous buck output
- PowerOK output monitors the 5 V LDO (POK5V)
- Logic-enable input for microprocessor control (ENB)
- High-voltage ignition enable input (ENBAT)
- ENBAT status indicator output (ENBATS)
- SLEW rate control helps reduce EMI/EMC
- Frequency dithering helps reduce EMI/EMC
- OV and UV protection for both output supply rails
- Pin-to-pin and pin-to-ground tolerant at every pin
- −40°C to 150°C junction temperature range
- Thermal shutdown protection

APPLICATIONS

- □ Electronic power steering (EPS) modules
- □ Automotive power trains
- □ CAN power supplies
- □ High-temperature applications

PACKAGE: 32-Pin QFN (suffix ET)



Not to scale

DESCRIPTION

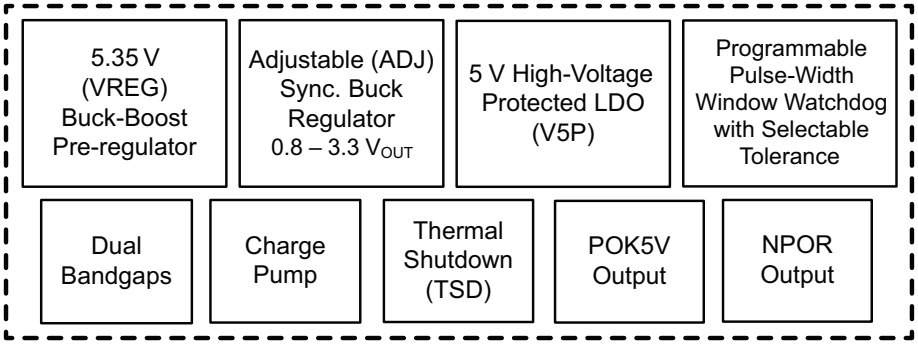
The A4413 is a power management IC that can be configured as a buck or buck-boost pre-regulator to efficiently convert automotive battery voltages into a tightly regulated intermediate voltage complete with control, diagnostics, and protections. The output of the pre-regulator supplies both a 5 V, 75 mA_{MAX} high-voltage protected LDO for remote sensors (V5P), and a 0.8 to 3.3 V, 800 mA_{MAX} adjustable synchronous buck regulator (ADJ). Designed to supply microprocessor power supplies in high-temperature environments, the A4413 is ideal for under hood and other automotive applications.

The A4413 can be enabled by its logic-level (ENB) or high-voltage (ENBAT) input. Diagnostic outputs from the A4413 include a power-on-reset output (NPOR) with a 2 ms rising delay to monitor the synchronous buck, a PowerOK output to monitor the 5 V LDO (POK5V), and an ENBAT status output (ENBATS). Dual bandgaps—one for regulation and one for fault detection—improve long-term reliability of the A4413.

The A4413 contains a pulse-width window watchdog (PWWD) timer that can be programmed to detect pulse widths from 1 to 2 ms (WD_{ADJ}). The watchdog timer has an activation delay that scales with the pulse-width setting to accommodate processor startup. The tolerance of the watchdog's window can be set to ±8%, ±13%, or ±18% using the WD_{TOL} pin. The watchdog timer has an active-low enable pin (WD_{ENn}) to facilitate initial factory programming or field reflash programming.

Protection features include under- and overvoltage lockout on both output supply rails. In case of a shorted output, the V5P LDO features foldback overcurrent protection. In addition, the V5P output is protected from a short-to-battery event. Both switching regulators include pulse-by-pulse current limit, hiccup mode short-circuit protection, LX short-circuit protection, missing asynchronous diode protection (VREG only), and thermal shutdown (TSD).

The A4413 is supplied in a low-profile 32-lead, 5 mm × 5 mm, 0.5 mm pitch QFN package (suffix "ET") with exposed thermal pad.



A4413 Simplified Block Diagram

SELECTION GUIDE

Part Number	Temperature Range	Package	Packing[1]	Lead Frame
A4413KETTR-J	–40°C to 135°C	32-pin QFN with thermal pad	1500 pieces per 7-inch reel	100% matte tin

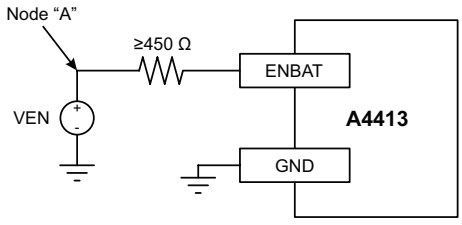
[1] Contact Allegro for additional packing options.

ABSOLUTE MAXIMUM RATINGS[2]

Characteristic	Symbol	Notes	Rating	Unit
VIN	V_{VIN}		−0.3 to 40	V
ENBAT	V_{ENBAT}	With current limiting resistor[3]	−13 to 40	V
			−0.3 to 8	V
	I_{ENBAT}		±75	mA
LX1	V_{LX1}		−0.3 to V_{VIN} + 0.3	V
		t < 250 ns	−1.5	V
		t < 50 ns	V_{VIN} + 3 V	V
SLEW	V_{SLEW}		−0.3 to 18	V
VCP, CP1, CP2	V_{VCP}, V_{CP1}, V_{CP2}		−0.3 to 50	V
V5P	V_{V5P}	Independent of V_{VIN}	−1 to 40	V
All other pins			−0.3 to 7	V
Ambient Temperature	T_A	Range K for automotive	−40 to 135	°C
Junction Temperature	T_J		−40 to 150	°C
Storage Temperature Range	T_{stg}		−40 to 150	°C

[2] Stresses beyond those listed in this table may cause permanent damage to the device. The absolute maximum ratings are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the Electrical Characteristics table is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability

[3] The higher ENBAT ratings (–13 V and 40 V) are measured at node “A” in the following circuit configuration:



THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

Characteristic	Symbol	Test Conditions[4]	Value	Unit
Junction-to-Pad Thermal Resistance	$R_{\theta JC}$	4-layer PCB based on JEDEC standard footprint	30	°C/W

[4] Additional thermal information available on the Allegro website.

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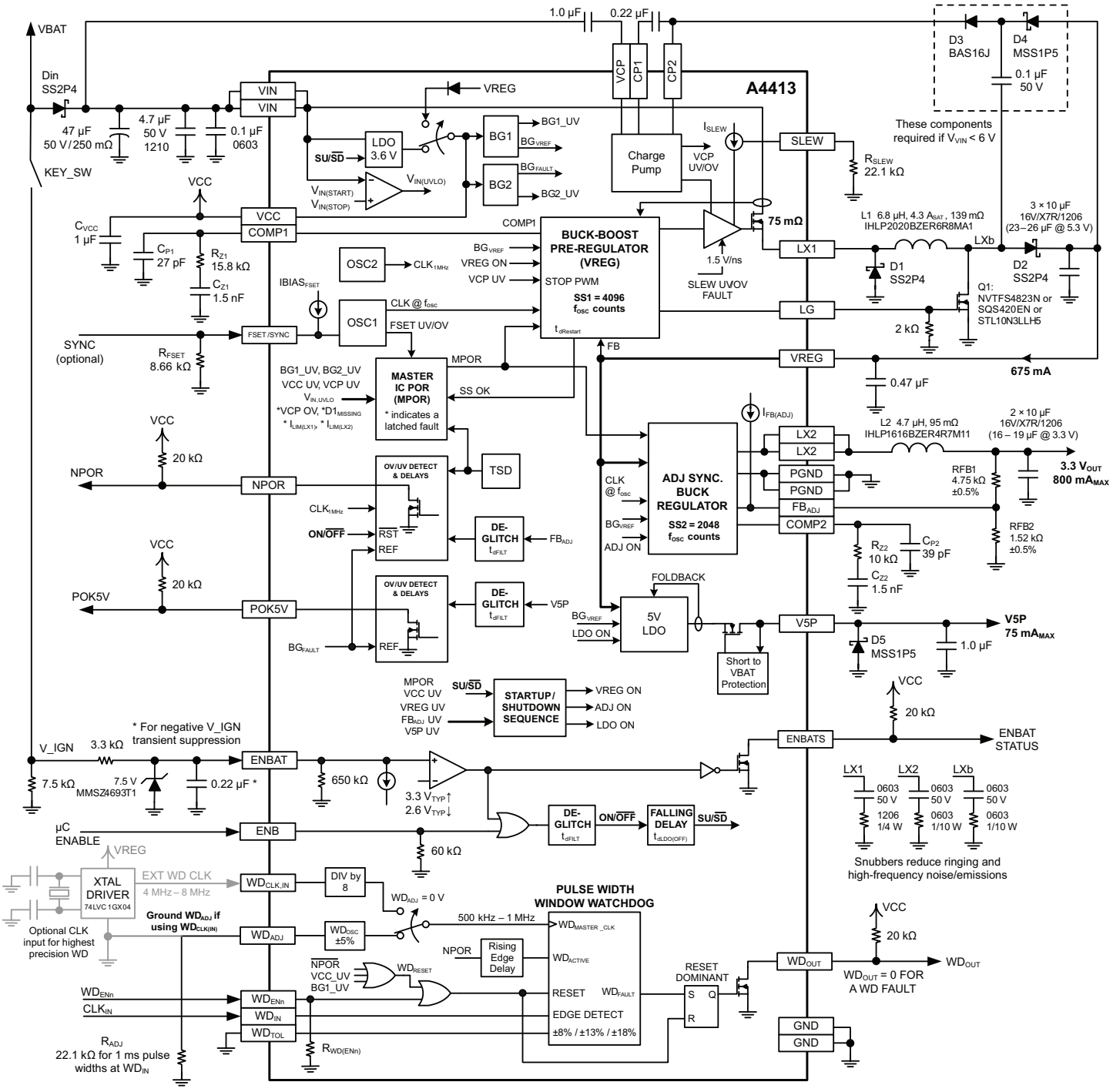
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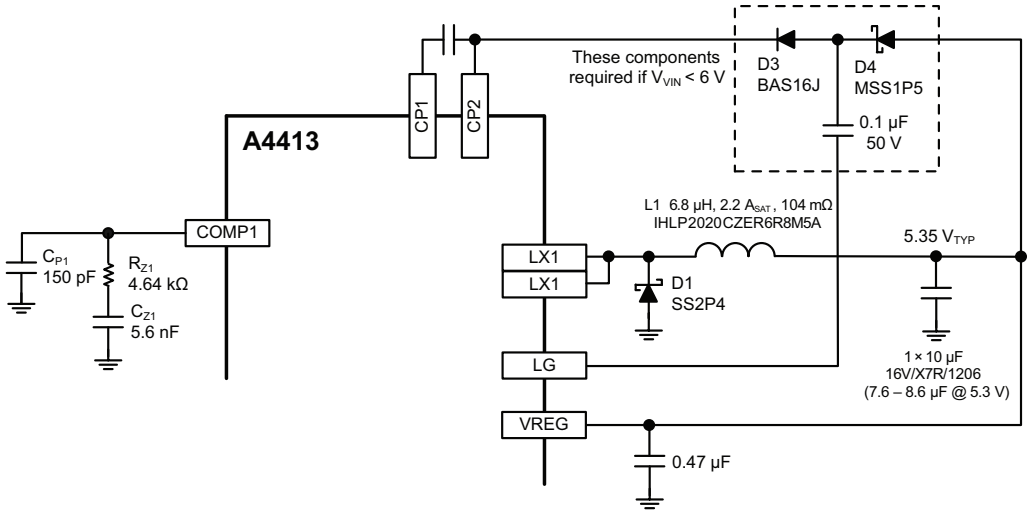
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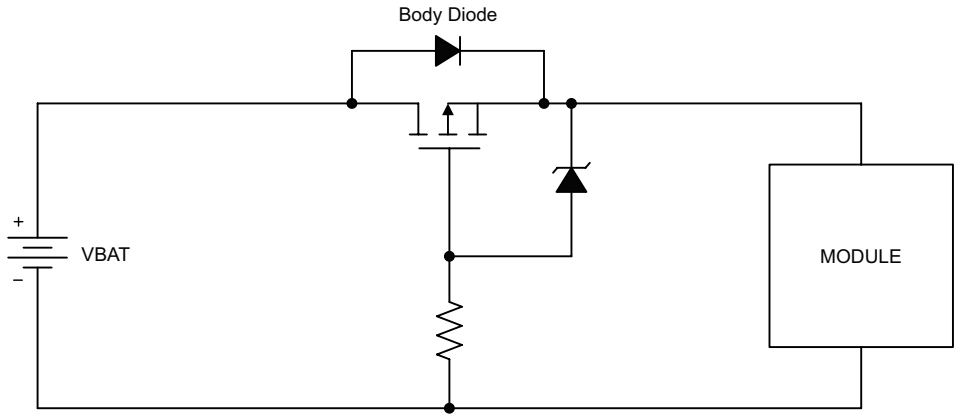
Functional Block Diagram/Typical Schematic

Buck-Boost Mode (f_{OSC} = 2 MHz), Using a Series Diode for Reverse-Battery Protection (D_{IN})

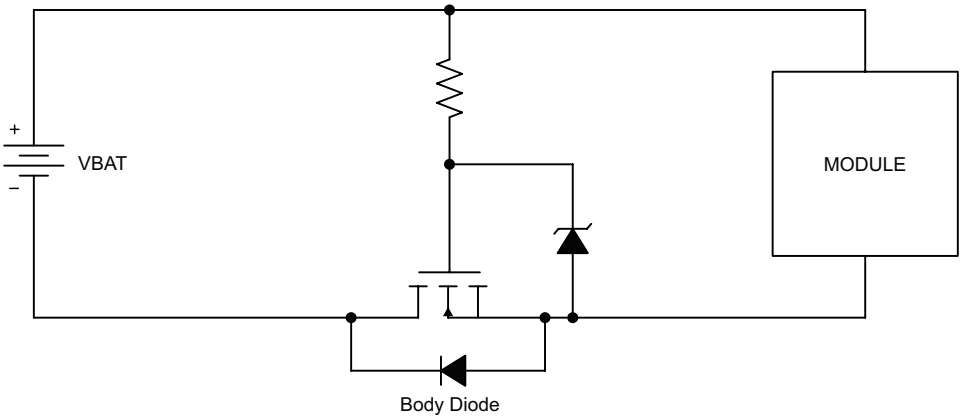
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Functional Block Diagram Modifications for Buck-Only Mode (f_{OSC} = 2 MHz)

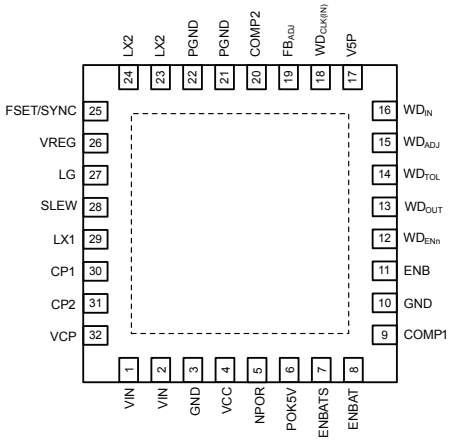


Functional Block Diagram Using a PMOS FET for Reverse-Battery Protection Instead of a Series Schottky Diode (D_{IN})



Functional Block Diagram Using an NMOS FET for Reverse-Battery Protection Instead of a Series Schottky Diode (D_{IN})

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Package ET, 32-Pin QFN
Pinout Diagram

Terminal List Table

Number	Name	Function
1, 2	VIN	Input voltage pins
3, 10	GND	Ground pin
4	VCC	Internal voltage regulator bypass capacitor pin
5	NPOR	Active-low, open-drain output indicating when the synchronous buck is out of regulation
6	POK5V	Open-drain output indicating when the V5P rail is out of regulation
7	ENBATS	Open-drain output indicating the status of the ENBAT (IGN) signal
8	ENBAT	Ignition enable input from the key/switch via a series resistor
9	COMP1	Error amplifier compensation network pin for the buck-boost pre-regulator
11	ENB	Logic compatible enable input from a microcontroller or DSP
12	WD_{ENn}	Active-low watchdog enable input from a microcontroller or DSP; open/low = WD is enabled, high = WD is disabled
13	WD_{OUT}	Open-drain watchdog output; normally high impedance; latched low if a watchdog fault occurs
14	WD_{TOL}	Selectable watchdog tolerance: low = ±8%, float = ±13%, high (to VCC) = ±18%
15	WD_{ADJ}	The watchdog window time is set by connecting R_{ADJ} from this pin to ground
16	WD_{IN}	Watchdog pulse train input from a microcontroller or DSP
17	V5P	5 V protected regulator output
18	$WD_{CLK(IN)}$	WD clock input for highest WD accuracy; if this pin is used, the WD_{ADJ} pin must be grounded. If this pin is unused it should be left floating.
19	FB_{ADJ}	Feedback pin for the adjustable synchronous buck regulator
20	COMP2	Error amplifier compensation network pin for the adjustable synchronous buck regulator
21, 22	PGND	Power ground for the adjustable synchronous regulator and its gate driver
23, 24	LX2	Switching node for the adjustable synchronous buck regulator
25	FSET/SYNC	Frequency setting and synchronization input
26	VREG	Output of the pre-regulator and input to the LDO and adjustable synchronous buck
27	LG	Boost gate drive output for the buck-boost pre-regulator
28	SLEW	Slew rate adjustment for the rise time of LX1
29	LX1	Switching node for the buck-boost pre-regulator
30	CP1	Charge pump capacitor connection
31	CP2	Charge pump capacitor connection
32	VCP	Charge pump reservoir capacitor

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ELECTRICAL CHARACTERISTICS – BUCK AND BUCK-BOOST PRE-REGULATOR SPECIFICATIONS[1]:

Valid at 3.5 V [(4)] < V_{VIN} < 36 V, –40°C < T_A = T_J < 150°C, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
GENERAL SPECIFICATIONS						
Operating Input Voltage	V_{VIN}	Buck-Boost mode, after V_{VIN} > $V_{VIN(START)}$, and V_{ENB} > 2 V, NPOR = 1, POK5V = 1	3.5	13.5	36	V
		Buck Only mode, after V_{VIN} > $V_{VIN(START)}$, and V_{ENB} > 2 V, NPOR = 1, POK5V = 1	5.7	13.5	36	V
VIN UVLO Start Voltage	$V_{VIN(START)}$	V_{VIN} rising, Buck or Boost mode	5.10	5.40	5.70	V
VIN UVLO Stop Voltage	$V_{VIN(STOP)}$	V_{VIN} falling, Buck or Boost mode	2.88	3.04	3.20	V
VIN UVLO Hysteresis	$V_{VIN(HYS)}$	$V_{VIN(START)}$ – $V_{VIN(STOP)}$	–	2.36	–	V
VIN Dropout Voltages, Buck Mode, V_{VIN} Falling	$V_{VIN(STOP1,BUCK)}$	NPOR = 1, POK5V ↓	–	5.0	5.3	V
	$V_{VIN(STOP2,BUCK)}$	V_{VCP} < $V_{CPUV(L)}$ and NPOR ↓, POK5V = 0	–	4.0	4.4	V
Supply Quiescent Current [1]	I_Q	V_{VIN} = 13.5 V, V_{IGN} ≥ 3.6 V or V_{ENB} ≥ 2 V, V_{VREG} = 5.6 V (no PWM)	–	10	–	mA
	$I_{Q(SLEEP)}$	V_{VIN} = 13.5 V, V_{IGN} ≤ 2.2 V and V_{ENB} ≤ 0.8 V	–	–	10	µA
PWM SWITCHING FREQUENCY AND DITHERING						
Switching Frequency	f_{OSC}	R_{FSET} = 8.66 kΩ	1.8	2.0	2.2	MHz
		R_{FSET} = 19.6 kΩ [(2)]	–	1.0	–	MHz
		R_{FSET} = 52.3 kΩ [(2)]	343	400	457	kHz
Frequency Dithering	Δf_{OSC}	As a percent of f_{OSC}	–	±12	–	%
Dither/Slew Start Threshold 1	$V_{VIN(DS,ON1)}$	V_{VIN} rising	16.9	18.0	19.1	V
Dither/Slew Stop Threshold 1	$V_{VIN(DS,OFF1)}$	V_{VIN} falling	–	16.6	–	V
Dither/Slew Start Threshold 2	$V_{VIN(DS,ON2)}$	V_{VIN} rising	–	9.0	–	V
Dither/Slew Stop Threshold 2	$V_{VIN(DS,OFF2)}$	V_{VIN} falling	7.8	8.3	8.8	V
CHARGE PUMP (VCP)						
Output Voltage	V_{VCP}	V_{VCP} – V_{VIN}, V_{VIN} = 13.5 V, V_{VREG} = 5.50 V, I_{VCP} = 5.0 mA, V_{COMP1} = V_{COMP2} = 0 V, V_{ENB} = 3.3 V	4.1	6.6	–	V
		V_{VCP} – V_{VIN}, V_{VIN} = 4.0 V, V_{VREG} = 5.25 V, I_{VCP} = 5.0 mA, V_{COMP1} = V_{COMP2} = 0 V, V_{ENB} = 3.3 V	3.3	–	–	V
Switching Frequency	$f_{SW(CP)}$		–	65	–	kHz
VCC PIN VOLTAGE						
Output Voltage	V_{VCC}	V_{VREG} = 5.35 V	–	4.65	–	V
Thermal Protection						
Thermal Shutdown Threshold [2]	T_{TSD}	T_J rising	155	170	185	°C
Thermal Shutdown Hysteresis [2]	T_{HYS}		–	20	–	°C

[1] For input and output current specifications, negative current is defined as coming out of the node or pin (sourcing), positive current is defined as going into the node or pin (sinking).
[2] Ensured by design and characterization, not production tested.
[3] Specifications at 25°C or 85°C are guaranteed by design and characterization, not production tested.
[4] The lowest operating voltage is only valid if the conditions V_{VIN} > $V_{VIN(START)}$ and V_{VCP} – V_{VIN} > $V_{VCP(UV,H)}$ and V_{VREG} > $V_{VREG(UV,H)}$ are satisfied before V_{VIN} is reduced.

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ELECTRICAL CHARACTERISTICS – BUCK AND BUCK-BOOST PRE-REGULATOR SPECIFICATIONS[1] (continued):

Valid at 3.5 V [(4)] < V_{VIN} < 36 V, –40°C < T_A = T_J < 150°C, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
OUTPUT VOLTAGE SPECIFICATIONS						
Buck Output Voltage – Regulating	V_{VREG}	V_{VIN} = 13.5 V, ENB = 1, 0.1 A < I_{VREG} < 1 A	5.25	5.35	5.45	V
PULSE-WIDTH MODULATION (PWM)						
PWM Ramp Offset	$V_{PWM1OFFS}$	V_{COMP1} for 0% duty cycle	–	400	–	mV
LX1 Rising Slew Rate Control [2]	$LX1_{RISE}$	V_{VIN} = 13.5 V, 10% to 90%, I_{VREG} = 1 A, R_{SLEW} = 22.1 kΩ	–	0.90	–	V/ns
		V_{VIN} = 13.5 V, 10% to 90%, I_{VREG} = 1 A, R_{SLEW} = 150 kΩ	–	0.23	–	V/ns
LX1 Falling Slew Rate [2]	$LX1_{FALL}$	V_{VIN} = 13.5 V, 90% to 10%, I_{VREG} = 1 A	–	1.0	–	V/ns
Buck Minimum On-Time	$t_{ON(BUCK,MIN)}$		–	85	150	ns
Buck Maximum Duty Cycle	$D_{MAX(BUCK)}$	$t_{OFF(BUCK)}$ < 50 ns	–	100	–	%
Boost Duty Cycle [2]	$D_{MIN(BST)}$	After V_{VIN} > $V_{VIN(START)}$, V_{VIN} = 6.5 V	–	20	–	%
	$D_{MAX(BST)}$	After V_{VIN} > $V_{VIN(START)}$, V_{VIN} = 3.5 V	57	62	67	%
COMP1 to LX1 Current Gain	gm_{POWER1}		–	3.6	–	A/V
Slope Compensation [2]	S_{E1}	f_{OSC} = 2.0 MHz	0.73	1.04	1.34	A/µs
		f_{OSC} = 400 kHz	0.15	0.23	0.31	A/µs
INTERNAL MOSFET						
MOSFET On-Resistance	R_{DSon}	V_{VIN} = 13.5 V, T_J = –40°C [(2)], I_{DS} = 0.1 A	–	75	95	mΩ
		V_{VIN} = 13.5 V, T_J = 25°C [(3)], I_{DS} = 0.1 A	–	110	135	mΩ
		V_{VIN} = 13.5 V, T_J = 150°C, I_{DS} = 0.1 A	–	220	265	mΩ
MOSFET Leakage	$I_{FET(LKG)}$	IC disabled, V_{LX1} = 0 V, V_{VIN} = 16 V, −40°C < T_J < 85°C [(3)]	–	–	10	µA
		IC disabled, V_{LX1} = 0 V, V_{VIN} = 16 V, −40°C < T_J < 150°C	–	50	150	µA
ERROR AMPLIFIER						
Open-Loop Voltage Gain	A_{VOL1}		–	60	–	dB
Transconductance	gm_{EA1}	V_{VREG} > 2.7 V	550	750	950	µA/V
		V_{VREG} < 2.7 V	275	375	475	µA/V
Output Current	I_{EA1}		–	±75	–	µA
Maximum Output Voltage	$V_{EA1(out,max)}$	V_{VIN} = 12 V	1.0	1.3	1.6	V
		V_{VIN} = 8 V	1.3	1.7	2.1	V
Minimum Output Voltage	$V_{EA1(out,min)}$		–	–	300	mV
COMP1 Pull-Down Resistance	R_{COMP1}	HICCUP1 = 1 or FAULT1 = 1 or IC disabled, latched until V_{SS1} < $V_{SS1(RST)}$	–	1	–	kΩ

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ELECTRICAL CHARACTERISTICS – BUCK AND BUCK-BOOST PRE-REGULATOR SPECIFICATIONS [1] (continued):

Valid at 3.5 V [(4)] < V_{VIN} < 36 V, –40°C < T_A = T_J < 150°C, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
BOOST MOSFET (LG) GATE DRIVER						
LG High Output Voltage	$V_{LG(ON)}$	V_{VIN} = 6 V, V_{VREG} = 5.35 V	4.6	–	5.5	V
LG Low Output Voltage	$V_{LG(OFF)}$	V_{VIN} = 13.5 V, V_{VREG} = 5.35 V	–	0.2	0.4	V
LG Source Current [1]	$I_{LG(ON)}$	V_{VIN} = 6 V, V_{VREG} = 5.35 V, V_{LG} = 1 V	–	−300	–	mA
LG Sink Current [1]	$I_{LG(OFF)}$	V_{VIN} = 13.5 V, V_{VREG} = 5.35 V, V_{LG} = 1 V	–	150	–	mA
SOFT-START						
SS1 Ramp Time	t_{SS1}		–	4096	–	f_{OSC} cycles
SS1 PWM Frequency Foldback	$f_{SW1(SS)}$	V_{VREG} < 0.65 V_{TYP}	–	f_{OSC}/8	–	–
		0.65 V < V_{VREG} < 1.3 V_{TYP}	–	f_{OSC}/4	–	–
		1.3 V < V_{VREG} < 2.7 V_{TYP}	–	f_{OSC}/2	–	–
		V_{VREG} > 2.7 V_{TYP}	–	f_{OSC}	–	–
HICCUP MODE						
Hiccup1 Enable Delay	$t_{HIC1(EN)}$		–	512	–	f_{OSC} cycles
Hiccup1 Recovery Time	$t_{HIC1(REC)}$	HICCUP1 = 1	–	4096	–	f_{OSC} cycles
Hiccup1 OCP Counts	$t_{HIC1(OCP)}$	V_{VREG} < 1.3 V_{TYP}, V_{COMP} = $V_{EA1(out,max)}$	–	30	–	–
		V_{VREG} > 1.3 V_{TYP}, V_{COMP} = $V_{EA1(out,max)}$	–	120	–	–
CURRENT PROTECTIONS						
Pulse-by-Pulse Current Limit	$I_{LIM1(ton,min)}$	V_{VIN} < 9 V, t_{ON} = $t_{ON(MIN)}$	2.6	2.8	3.3	A
		V_{VIN} > 9 V, t_{ON} = $t_{ON(MIN)}$	1.8	2.0	2.2	A
LX1 Short-Circuit Current Limit	$I_{LIM(LX1)}$	Hiccup mode after 1 × $I_{LIM(LX1)}$ detection	5	7	–	A
MISSING ASYNCHRONOUS DIODE (D1) PROTECTION						
Detection Level	$V_{D(OPEN)}$		−1.8	−1.6	−1.2	V
Time Filtering [2]	$t_{D(OPEN)}$		50	–	250	ns

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[3] Specifications at 25°C or 85°C are guaranteed by design and characterization, not production tested.
[4] The lowest operating voltage is only valid if the conditions V_{VIN} > $V_{VIN(START)}$ and V_{VCP} – V_{VIN} > $V_{VCP(UV,H)}$ and V_{VREG} > $V_{VREG(UV,H)}$ are satisfied before V_{VIN} is reduced.

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ELECTRICAL CHARACTERISTICS – ADJUSTABLE SYNCHRONOUS BUCK REGULATOR[1]:

Valid at 3.5 V [(4)] < V_{VIN} < 36 V, –40°C < T_A = T_J < 150°C, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
FEEDBACK REFERENCE VOLTAGE						
Reference Voltage	$V_{FB(ADJ)}$		787	800	813	mV
PULSE-WIDTH MODULATION (PWM)						
PWM Ramp Offset	$V_{PWM2OFFS}$	V_{COMP2} for 0% duty cycle	–	350	–	mV
High-Side MOSFET Minimum On-Time	$t_{ON(MIN)}$		–	65	105	ns
High-Side MOSFET Minimum Off-Time	$t_{OFF(MIN)}$	Does not include total gate driver non-overlap time, t_{NO}	–	80	110	ns
Gate Driver Non-Overlap Time [2]	t_{NO}		–	15	–	ns
COMP2 to LX2 Current Gain	gm_{POWER2}		–	2.5	–	A/V
Slope Compensation [2]	S_{E2}	f_{OSC} = 2.0 MHz	0.45	0.63	0.81	A/µs
		f_{OSC} = 400 kHz	0.12	0.14	0.19	A/µs
INTERNAL MOSFETS						
High-Side MOSFET On-Resistance	$R_{DSon(HS)}$	T_A = 25°C [(3)], I_{DS} = 100 mA	–	120	150	mΩ
		I_{DS} = 100 mA	–	150	200	mΩ
LX2 Node Rise/Fall Time [2]	$t_{R/F(LX2)}$	V_{VREG} = 5.5 V	–	12	–	ns
High-Side MOSFET Leakage [1]	$I_{DSS(HS)}$	IC disabled, V_{LX2} = 0 V, V_{VREG} = 5.5 V, –40°C < T_J < 85°C [(3)]	–	–	2	µA
		IC disabled, V_{LX2} = 0 V, V_{VREG} = 5.5 V, −40°C < T_J < 150°C	–	3	15	µA
Low-Side MOSFET On-Resistance	$R_{DSon(LS)}$	T_A = 25°C [(3)], I_{DS} = 100 mA	–	65	75	mΩ
		I_{DS} = 100 mA	–	80	110	mΩ
Low-Side MOSFET Leakage [1]	$I_{DSS(LS)}$	IC disabled, V_{LX2} = 5.5 V, –40°C < T_J < 85°C [(3)]	–	–	1	µA
		IC disabled, V_{LX2} = 5.5 V, −40°C < T_J < 150°C	–	4	10	µA
ERROR AMPLIFIER						
Feedback Input Bias Current [1]	$I_{FB(ADJ)}$	V_{COMP2} = 0.8 V, $V_{FB(ADJ)}$ regulated so that I_{COMP2} = 0 A	–	–150	−350	nA
Open-Loop Voltage Gain [2]	A_{VOL2}		–	60	–	dB
Transconductance	gm_{EA2}	I_{COMP2} = 0 µA, $V_{FB(ADJ)}$ > 500 mV	550	750	950	µA/V
		0 V < $V_{FB(ADJ)}$ < 500 mV	–	250	–	µA/V
Source and Sink Current	I_{EA2}	V_{COMP2} = 1.5 V	–	±50	–	µA
Maximum Output Voltage	$V_{EA2(out,max)}$		1.00	1.25	1.50	V
Minimum Output Voltage	$V_{EA2(out,min)}$		–	–	150	mV
COMP2 Pull-Down Resistance	R_{COMP2}	HICCUP2 = 1 or FAULT2 = 1 or IC disabled, latched until SS2 resets	–	1.5	–	kΩ

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ELECTRICAL CHARACTERISTICS – ADJUSTABLE SYNCHRONOUS BUCK REGULATOR[1] (continued):

Valid at 3.5 V [(4)] < V_{VIN} < 36 V, –40°C < T_A = T_J < 150°C, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
SOFT-START						
$V_{FB(ADJ)}$ Soft-Start Ramp Time	t_{SS2}		–	2048	–	f_{OSC} cycles
SS2 PWM Frequency Foldback	$f_{SW2(SS)}$	$V_{FB(ADJ)}$ < 200 mV_{TYP}	–	f_{OSC}/4	–	–
		200 mV_{TYP} < $V_{FB(ADJ)}$ < 500 mV_{TYP}	–	f_{OSC}/2	–	–
		$V_{FB(ADJ)}$ > 500 mV_{TYP}	–	f_{OSC}	–	–
HICCUP MODE						
Hiccup2 Enable Delay	$t_{HIC2(EN)}$		–	512	–	f_{OSC} cycles
Hiccup2 Recovery Time	$t_{HIC2(REC)}$	HICCUP2 = 1	–	2048	–	f_{OSC} cycles
Hiccup2 OCP Counts	$t_{HIC2(OCP)}$	t > $t_{HIC2(EN)}$, $V_{FB(ADJ)}$ < 200 mV_{TYP}	–	32	–	f_{OSC} cycles
		t > $t_{HIC2(EN)}$, $V_{FB(ADJ)}$ > 200 mV_{TYP}	–	120	–	f_{OSC} cycles
CURRENT PROTECTIONS						
Pulse-by-Pulse Current Limit	$I_{LIM2(5\%)}$	Duty cycle = 5%	1.8	2.1	2.4	A
	$I_{LIM2(90\%)}$	Duty cycle = 90%	1.2	1.6	2.0	A
LX2 Short-Circuit Protection	$V_{LIM(LX2)}$	V_{LX2} stuck low for more than 60 ns, Hiccup mode after 1× detection	–	V_{VREG} –1.2 V	–	V
V5P LINEAR REGULATORS						
V5P Accuracy and Load Regulation	V_{V5P}	10 mA < I_{V5P} < 80 mA, V_{VREG} = 5.25 V	4.9	5.0	5.1	V
V5P Output Capacitance [2]	$C_{OUT(V5P)}$		0.7	1.0	1.9	µF
V5P Minimum Output Voltage [2]	$V_{V5P(MIN)}$	V_{VIN} = 4.0 V, V_{VREG} = 5.25 V, V_{VCP} = 7.3 V, I_{V5P} = 75 mA, I_{3V3} = 800 mA (510 mA to VREG)	4.86	4.95	–	V
V5P OVERCURRENT PROTECTION						
V5P Current Limit [1]	$I_{LIM(V5P)}$	V_{V5P} = 5 V	−90	−130	–	mA
V5P Foldback Current [1]	$I_{FBK(V5P)}$	V_{V5P} = 0 V	−20	−45	−70	mA
V5P STARTUP TIMING						
V5P Startup Time [2]	$t_{SS(V5P)}$	C_{V5P} ≤ 1.0 µF, Load = 66 Ω ±5% (75 mA)	–	0.21	1.1	ms

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ELECTRICAL CHARACTERISTICS – CONTROL INPUTS [1]:

Valid at 3.5 V [4] < V_{VIN} < 36 V, –40°C < T_A = T_J < 150°C, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
IGNITION ENABLE (ENBAT) INPUTS						
ENBAT Thresholds	$V_{ENBAT(H)}$	V_{ENBAT} rising	2.9	3.1	3.5	V
	$V_{ENBAT(L)}$	V_{ENBAT} falling	2.2	2.6	2.9	V
ENBAT Hysteresis	$V_{ENBAT(HYS)}$	$V_{ENBAT(H)} – V_{ENBAT(L)}$	–	500	–	mV
ENBAT Bias Current [1]	$I_{ENBAT(BIAS)}$	T_J = 25°C [3], V_{ENBAT} = 3.51 V	–	40	65	µA
		T_J = 150°C, V_{ENBAT} = 3.51 V	–	50	80	µA
ENBAT Pull-Down Resistance	R_{ENBAT}	V_{ENBAT} < 1.2 V	–	650	–	kΩ
LOGIC ENABLE (ENB) INPUT						
ENB Thresholds	$V_{ENB(H)}$	V_{ENB} rising	–	–	2.0	V
	$V_{ENB(L)}$	V_{ENB} falling	0.8	–	–	V
ENB Bias Current [1]	$I_{ENB(IN)}$	V_{ENB} = 3.3 V	–	–	175	µA
ENB Resistance	R_{ENB}	V_{ENB} = 0.8 V	–	60	–	kΩ
ENB/ENBAT FILTER/DEGLITCH						
Enable Filter/Deglitch Time	t_{dFILT}		10	15	20	µs
ENB/ENBAT RESTART DELAY						
Enable Restart Delay Time	$t_{dRestart}$	Measured from the time when ENBAT = ENB = 0 and V_{VREG} < $V_{VREG(UV,L)}$	460	512	565	µs
ENB/ENBAT SHUTDOWN DELAY						
LDO Shutdown Delay	$t_{dLDO(OFF)}$	Measure $t_{dLDO(OFF)}$ from the falling edge of ENB and ENBAT to the time when all LDOs begin to decay	15	50	100	µs
FSET/SYNC INPUTS						
FSET/SYNC Pin Voltage	$V_{FSET/SYNC}$	No external SYNC signal	–	800	–	mV
FSET/SYNC Bias Current	$I_{BIAS(FSET)}$		–	−100	–	nA
FSET/SYNC Open-Circuit (Undercurrent) Detection Time	$t_{FSET/SYNC(UC)}$	1 MHz PWM operation if open	–	3	–	µs
FSET/SYNC Short-Circuit (Overcurrent) Detection Time	$t_{FSET/SYNC(OC)}$	1 MHz PWM operation if shorted	–	3	–	µs
Sync. High Threshold	$V_{SYNC(HI)}$	V_{SYNC} rising	–	–	2.0	V
Sync. Low Threshold	$V_{SYNC(LO)}$	V_{SYNC} falling	0.5	–	–	V
Sync. Input Duty Cycle	DC_{SYNC}		–	–	80	%
Sync. Input Pulse Width	t_{WSYNC}		200	–	–	ns
Sync. Input Transition Times [2]	t_{TSYNC}		–	10	15	ns
SLEW Inputs						
SLEW Pin Operating Voltage	V_{SLEW}		–	800	–	mV
SLEW Pin Open-Circuit (Undercurrent) Detection Time	$V_{SLEW(UC)}$	LX1 defaults to 1.5 V/ns if fault	–	3	–	µs
SLEW Pin Short-Circuit (Overcurrent) Detection Time	$V_{SLEW(OC)}$	LX1 defaults to 1.5 V/ns if fault	–	3	–	µs
SLEW Bias Current [1]	I_{SLEW}		–	−100	–	nA

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ELECTRICAL CHARACTERISTICS – DIAGNOSTIC OUTPUTS [1]:

Valid at 3.5 V [(4)] < V_{VIN} < 36 V, –40°C < T_A = T_J < 150°C, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
NPOR OV/UV PROTECTION THRESHOLDS						
FB_{ADJ} OV Thresholds	$V_{FB(ADJ,OV,H)}$	$V_{FB(ADJ)}$ rising	835	855	875	mV
	$V_{FB(ADJ,OV,L)}$	$V_{FB(ADJ)}$ falling	–	848	–	mV
FB_{ADJ} OV Hysteresis	$V_{FB(ADJ,OV,HYS)}$	$V_{FB(ADJ,OV,H)} – V_{FB(ADJ,OV,L)}$	3	7	14	mV
FB_{ADJ} UV Thresholds	$V_{FB(ADJ,UV,H)}$	$V_{FB(ADJ)}$ rising, triggers turn on of LDOs	–	752	–	mV
	$V_{FB(ADJ,UV,L)}$	$V_{FB(ADJ)}$ falling	725	745	765	mV
FB_{ADJ} UV Hysteresis	$V_{FB(ADJ,UV,HYS)}$	$V_{FB(ADJ,UV,H)} – V_{FB(ADJ,UV,L)}$	3	7	14	mV
NPOR TURN-ON AND TURN-OFF DELAYS						
NPOR Turn-On Delay	$t_{dNPOR(ON)}$	$V_{FB(ADJ)} > V_{FB(ADJ,UV,H)}$, see Figure 12 for timing details	1.6	2	2.4	ms
NPOR Turn-Off Delay	$t_{dNPOR(OFF)}$	ENB and ENBAT low for t > t_{dFILT}, see Figure 12 for timing details	–	–	3	µs
NPOR OUTPUT VOLTAGES						
NPOR Output Low Voltage	$V_{NPOR(L)}$	ENB or ENBAT high, V_{VIN} ≥ 2.5 V, I_{NPOR} = 4 mA	–	150	400	mV
		ENB or ENBAT high, V_{VIN} = 1.5 V, I_{NPOR} = 2 mA	–	–	800	mV
NPOR Leakage Current [1]	$I_{NPOR(LKG)}$	V_{NPOR} = 3.3 V	–	–	2	µA
NPOR AND POK5V OV DELAY TIME						
Overvoltage Detection Delay	t_{dOV}	V5P or FB_{ADJ} overvoltage detection delay time (two independent timers, NPOR and POK5V)	3.2	4.0	4.8	ms
NPOR AND POK5V UV FILTERING/DEGLITCH						
UV Filter/Deglitch Times	t_{dFILT}	Applies to undervoltage of the FB_{ADJ} and V5P voltages	10	15	20	µs
POK5V OV/UV PROTECTION THRESHOLDS						
V5P OV Thresholds	$V_{V5P(OV,H)}$	V_{V5P} rising	5.15	5.33	5.50	V
	$V_{V5P(OV,L)}$	V_{V5P} falling	–	5.30	–	V
V5P OV Hysteresis	$V_{V5P(OV,HYS)}$	$V_{V5P(OV,H)} – V_{V5P(OV,L)}$	15	30	50	mV
V5P UV Thresholds	$V_{V5P(UV,H)}$	V_{V5P} rising	–	4.71	–	V
	$V_{VP5(UV,L)}$	V_{V5P} falling	4.50	4.68	4.85	V
V5P UV Hysteresis	$V_{V5P(UV,HYS)}$	$V_{V5P(UV,H)} – V_{V5P(UV,L)}$	15	30	50	mV

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ELECTRICAL CHARACTERISTICS – DIAGNOSTIC OUTPUTS [1] (continued):

Valid at 3.5 V [(4)] < V_{VVIN} < 36 V, –40°C < T_A = T_J < 150°C, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
POK5V OUTPUT VOLTAGES						
POK5V Output Voltage	$V_{POK5V(L)}$	ENB = 1 or ENBAT = 1, V_{VIN} ≥ 2.5 V, I_{POK5V} = 4 mA	–	150	400	mV
		ENB = 1 or ENBAT= 1, V_{VIN} = 2.2 V, I_{POK5V} = 2 mA	–	–	800	mV
POK5V Leakage Current	$I_{POK5V(LKG)}$	V_{POK5V} = 3.3 V	–	–	2	µA
VREG, VCP, AND BG THRESHOLDS						
VREG OV Thresholds	$V_{VREG(OV,H)}$	V_{VREG} rising, LX1 PWM disabled	5.70	5.95	6.20	V
	$V_{VREG(OV,L)}$	V_{VREG} falling, LX1 PWM enabled	–	5.85	–	V
VREG OV Hysteresis	$V_{VREG(OV,HYS)}$	$V_{VREG(OV,H)}$ – $V_{VREG(OV,L)}$	–	100	–	mV
VREG UV Thresholds	$V_{VREG(UV,H)}$	V_{VREG} rising, triggers rise of SS2	4.14	4.38	4.62	V
	$V_{VREG(UV,L)}$	V_{VREG} falling	–	4.28	–	V
VREG UV Hysteresis	$V_{VREG(UV,HYS)}$	$V_{VREG(UV,H)}$ – $V_{VREG(UV,L)}$	–	100	–	mV
VCP OV Thresholds	$V_{VCP(OV,H)}$	V_{VCP} rising, latches all regulators off	11.0	12.5	14.0	V
VCP UV Thresholds	$V_{VCP(UV,H)}$	V_{VCP} rising, PWM enabled	2.8	3.0	3.2	V
	$V_{VCP(UV,L)}$	V_{VCP} falling, PWM disabled	–	2.6	–	V
VCP UV Hysteresis	$V_{VCP(UV,HYS)}$	$V_{VCP(UV,H)}$ – $V_{VCP(UV,L)}$	–	400	–	mV
BG_{VREF} and BG_{FAULT} UV Thresholds [2]	$V_{x(BG,UV)}$	$V_{VREF(BG)}$ or $V_{FAULT(BG)}$ rising	1.00	1.05	1.10	V
IGNITION STATUS (ENBATS) SPECIFICATIONS						
ENBATS Thresholds	$V_{ENBATS(H)}$	V_{ENBAT} rising	2.9	3.3	3.5	V
	$V_{ENBATS(L)}$	V_{ENBAT} falling	2.2	2.6	2.9	V
ENBATS Output Voltage	$V_{ENBATS(LO)}$	I_{ENBATS} = 4 mA	–	–	400	mV
ENBATS Leakage Current [1]	I_{ENBATS}	V_{ENBATS} = 3.3 V	–	–	2	µA

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ELECTRICAL CHARACTERISTICS – PULSE-WIDTH WINDOW WATCHDOG (PWWD) [1]:

Valid at 3.5 V [4] < V_{VVIN} < 36 V, –40°C < T_A = T_J < 150°C, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
WD ENABLE INPUT (WD_{ENn})						
WD_{ENn} Voltage Thresholds	$V_{WD(ENn,LO)}$	$V_{WD(ENn)}$ falling, WDT enabled	0.8	–	–	V
	$V_{WD(ENn,HI)}$	$V_{WD(ENn)}$ rising, WDT disabled	–	–	2.0	V
WD_{ENn} Input Resistance	$R_{WD(ENn)}$		–	60	–	kΩ
WD_{IN} VOLTAGE THRESHOLDS AND CURRENT						
WD_{IN} Input Voltage Thresholds	$V_{WD(IN,LO)}$	$V_{WD(IN)}$ falling, WD_{ADJ} pulled low by R_{ADJ}	0.8	–	–	V
	$V_{WD(IN,HI)}$	$V_{WD(IN)}$ rising, WD_{ADJ} charging	–	–	2.0	V
WD_{IN} Input Current [1]	$I_{WD(IN)}$	$V_{WD(IN)}$ = 5 V	−10	±1	10	µA
WD_{OUT} SPECIFICATIONS						
WD_{OUT} Output Voltage	$V_{WD(OUT,LO)}$	$I_{WD(OUT)}$ = 4 mA	–	–	400	mV
WD_{OUT} Leakage Current [1]	$I_{WD(OUT)}$	$V_{WD(OUT)}$ = 3.3 V	–	–	2	µA
WATCHDOG (WD) OSCILLATOR, PULSE-WIDTH SELECTION, AND START DELAY						
WD Oscillator Tolerance	$WD_{OSC(TOL)}$	Typical value is at 25°C [2]	−5	±2.5	+5	%
WD Startup Delay	$t_{dWD(START)}$	Gated by WD_{ENn} = 0 × NPOR↥	1.6	2.0	2.4	ms
WD_{IN} Pulse-Width Programming	$t_{WD(IN,PW)}$	R_{ADJ} = 22.1 kΩ ($f_{OSC(WD)}$ = 1 MHz)	0.95	1.0	1.05	ms
		R_{ADJ} = 44.2 kΩ ($f_{OSC(WD)}$ = 500 kHz)	1.9	2.0	2.1	ms
WD First Edge Timeout Delay	$t_{WD(EDGE,TO)}$	R_{ADJ} = 22.1 kΩ ($f_{OSC(WD)}$ = 1 MHz)	4.7	5	5.3	ms
		R_{ADJ} = 44.2 kΩ ($f_{OSC(WD)}$ = 500 kHz)	9.4	10	10.6	ms
WD CLK_{IN} Non-Activity Timeout	$t_{WD(ACT,TO)}$	R_{ADJ} = 22.1 kΩ ($f_{OSC(WD)}$ = 1 MHz)	15.2	16	16.8	ms
		R_{ADJ} = 44.2 kΩ ($f_{OSC(WD)}$ = 500 kHz)	30.4	32	33.6	ms
WATCHDOG CLOCK INPUT ($WD_{CLK(IN)}$)						
Input Clock Divider	$WD_{CLK(DIV)}$		–	8	–	–
$WD_{CLK(IN)}$ Voltage Thresholds	$V_{WD(CLK,IN,LO)}$	$V_{WD(CLK,IN)}$ falling	0.8	–	–	V
	$V_{WD(CLK,IN,HI)}$	$V_{WD(CLK,IN)}$ rising	–	–	2.0	V
WATCHDOG WINDOW TOLERANCE SELECTION ($WD_{WIN(TOL)}$)						
WD Window Tolerance Settings	$WD_{WIN(TOL)}$	WD_{TOL} pin connected to GND	−8	–	+8	%
		WD_{TOL} pin floating	−13	–	+13	%
		WD_{TOL} pin connected to VCC	−18	–	+18	%
WATCHDOG PULSE-WIDTH (PW) ERROR COUNTING						
Counter Increment if PW Fault	WD_{INC}		–	+10	–	counts
Counter Decrement if PW is OK	WD_{DEC}		–	–2	–	counts
Counts to Latch WD_{FAULT} Low	WD_{COUNT}		–	160	–	counts

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FUNCTIONAL DESCRIPTION

Overview

The A4413 is a power management IC designed for automotive applications. It contains a pre-regulator plus two DC post-regulators to create the voltages necessary for typical automotive applications, such as electrical power steering and automatic transmission control.

The pre-regulator can be configured as a buck or buck-boost regulator. Buck-boost is required for applications that need to work at extremely low battery voltages. The pre-regulator generates a fixed 5.35 V and can deliver up to 1 A to power the internal (or external) post-regulators. These post-regulators generate the various voltage levels for the end system.

The A4413 includes two internal post-regulators, a low-dropout linear regulator (LDO), and an adjustable output synchronous buck regulator.

Buck-Boost Pre-Regulator (VREG)

The pre-regulator incorporates an internal high-side buck switch and a boost switch gate driver. An external freewheeling Schottky diode and an LC filter are required to complete the buck converter. By adding a MOSFET and a Schottky diode, the boost configuration can maintain all outputs with input voltages as low as 3.5 V. The buck-boost pre-regulator includes a compensation pin (COMP1). Typical buck-boost performance is shown in Figure 1 and Figure 2.

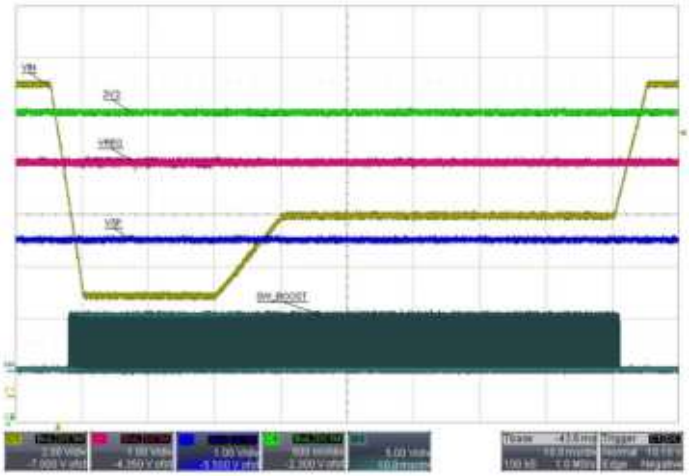


Figure 1: A4413 buck-boost operation at full load with V_{VIN} slew rates ranging from 0.3 V/ms to 1.6 V/ms, representative of an automotive start/stop waveform. $V_{VIN(TYP)}$ = 12 V, $V_{VIN(MIN)}$ = 4 V.

CH1 = VIN, CH2 = VREG, CH3 = V5P, CH4 = 3V3, 10 ms/DIV

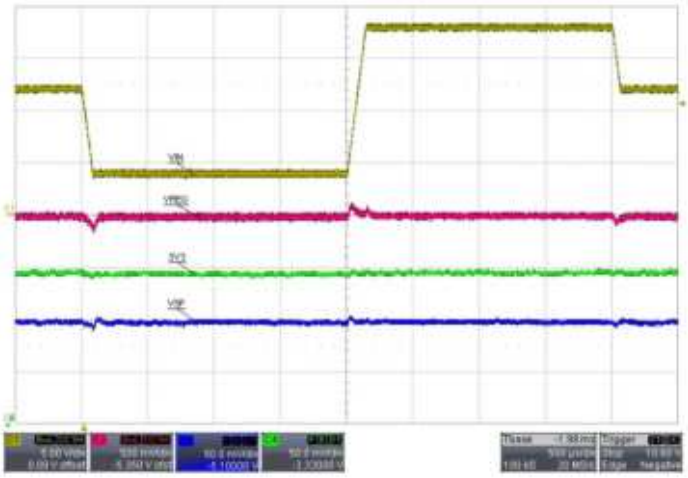


Figure 2: A4413 buck-boost operation at full load with V_{VIN} slew rates of 100 V/ms; V5P deviates only ±0.14% (±7 mV). $V_{VIN(TYP)}$ = 12 V, $V_{VIN(MIN)}$ = 4 V, $V_{VIN(MAX)}$ = 18 V.

CH1 = VIN, CH2 = VREG, CH3 = V5P, CH4 = 3V3, 500 µs/DIV

In general, as PWM frequency decreases, a regulator's output capacitance must increase to maintain low voltage ripple and good load transient response. If the soft-start time is too fast, with higher output capacitance, the combination of capacitor charging plus load current could exceed the regulator's pulse-by-pulse current limit, as shown in Figure 3. The A4413 avoids this potential issue by directly scaling the soft-start time with the oscillator frequency. The soft-start time of the pre-regulator is internally fixed at t_{SS1} f_{OSC} cycles (4096). If f_{OSC} = 2 MHz, the pre-regulator soft-start time will be 2.048 ms. Similarly, if f_{OSC} = 400 kHz, the soft-start time will be 10.24 ms.

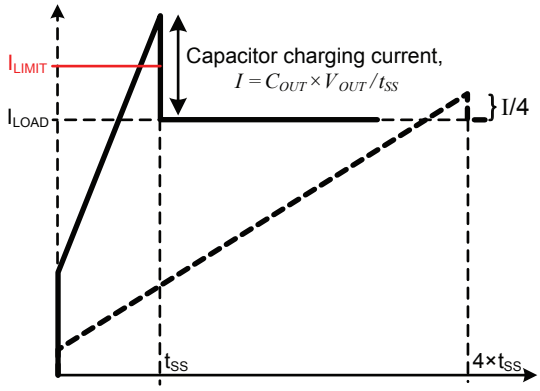


Figure 3: Capacitor charging currents versus soft-start time (t_{SS1}) when f_{OSC} and C_{OUT} are unchanged.

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When the output of the pre-regulator is shorted to ground, it will protect itself by entering hiccup mode. The recovery time between restart attempts, $t_{HIC1(REC)}$, is internally fixed at 4096 f_{OSC} cycles. Protection and safety functions provided by the buck-boost pre-regulator are:

1. High voltage rating for load dump
2. Overvoltage protection
3. Switch node to ground short-circuit protection
4. Open freewheeling diode protection
5. Pulse-by-pulse current limit
6. Hiccup short-circuit protection, shown in Figure 4

For the pre-regulator, hiccup mode is enabled during soft-start after $t_{HIC1(EN)}$ f_{OSC} cycles (512). If V_{VREG} is less than 1.3 V, the number of overcurrent pulses (OCP) is limited to only 30. If V_{VREG} is greater than 1.3 V, the number of OCP pulses is increased to 120 to accommodate the possibility of starting into a relatively high output capacitance. The time between restart attempts or the hiccup recovery time is $t_{HIC1(REC)}$ (4096) f_{OSC} cycles, as indicated by the vertical cursors in Figure 4.

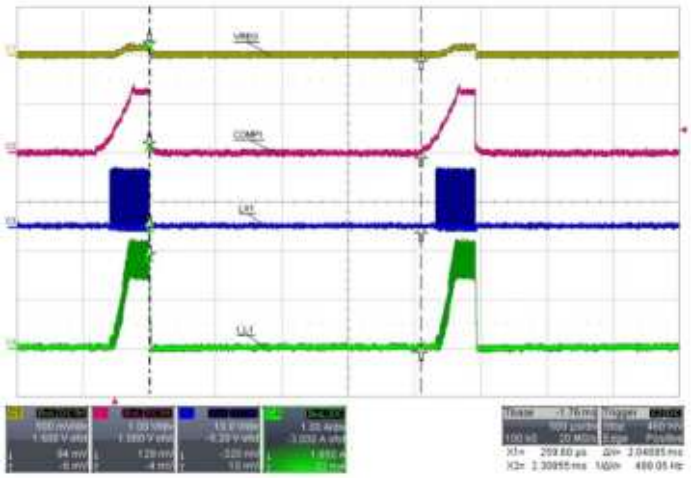


Figure 4: Pre-regulator hiccup mode operation when VREG is shorted to GND, f_{OSC} = 2 MHz.

CH1 = VREG, CH2 = COMP1, CH3 = LX1, CH4 = I_{L1}, 1 ms/DIV

Adjustable Synchronous Buck Regulator (ADJ)

The A4413 integrates the high-side and low-side MOSFETs necessary for implementing an adjustable output 800 mA_{DC} (1 A_{PEAK}) synchronous buck regulator. The synchronous buck is powered by the 5.35 V pre-regulator output. An external LC filter is required to complete the synchronous buck regulator. The synchronous buck output voltage is adjusted by a connecting a resistor divider from the buck output to the feedback pin (FB_{ADJ}). The synchronous buck regulator includes a compensation pin (COMP2).

Similar to the pre-regulator, the soft-start time of the synchronous buck is internally fixed at t_{SS1} f_{OSC} cycles (2048). If f_{OSC} = 2 MHz, the synchronous buck soft-start time will be 1.024 ms. Likewise, if f_{OSC} = 400 kHz, the soft-start time will be 5.12 ms.

Protection and safety functions provided by the synchronous buck are:

1. Undervoltage detection
2. Overvoltage protection
3. Switch node to ground short-circuit protection
4. Pulse-by-pulse current limit
5. Hiccup short-circuit protection, shown in Figure 5

For the synchronous buck, hiccup mode is enabled during soft-start after $t_{HIC2(EN)}$ f_{OSC} cycles (512). If $V_{FB(ADJ)}$ is less than 200 mV_{TYP}, the number of overcurrent pulses (OCP) is limited to only 32. If $V_{FB(ADJ)}$ is greater than 200 mV_{TYP}, the number of OCP pulses is increased to 120 to accommodate the possibility of starting into a relatively high output capacitance. The time between restart attempts or the hiccup recovery time is $t_{HIC2(REC)}$ (2048) f_{OSC} cycles, as indicated by the cursors in Figure 5.

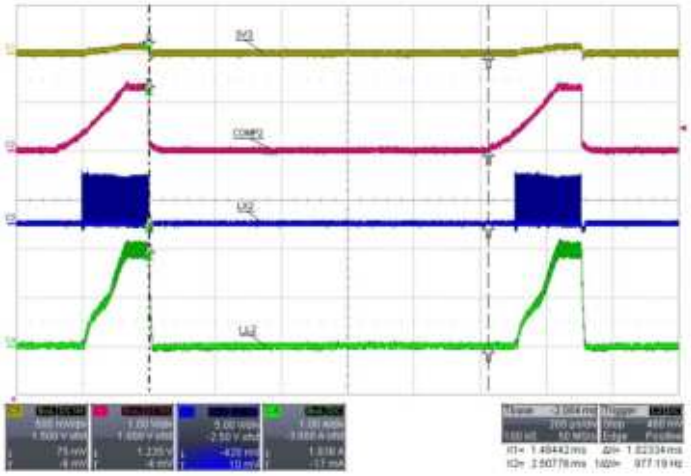


Figure 5: Synchronous buck hiccup mode operation when VOUT is shorted to GND, f_{OSC} = 2 MHz.

CH1 = 3V3, CH2 = COMP2, CH3 = LX2, CH4 = I_{L2}, 200 µs/DIV

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Low-Dropout Linear Regulator (LDO)

The A4413 has a high-voltage protected 5 V / 75 mA_{MAX} low-dropout regulator (V5P). The switching pre-regulator efficiently regulates the battery voltage to an intermediate value to power the LDO. The pre-regulator topology reduces LDO power dissipation and junction temperature.

The V5P regulator includes protection against accidental short circuit to the battery voltage. This makes the V5P output suitable for powering remote sensors or circuitry via a wiring harness where a short to battery is possible.

The V5P linear regulator provides the following protection features:

1. Undervoltage and overvoltage detection
2. Current limit with foldback short-circuit protection; see Figure 6

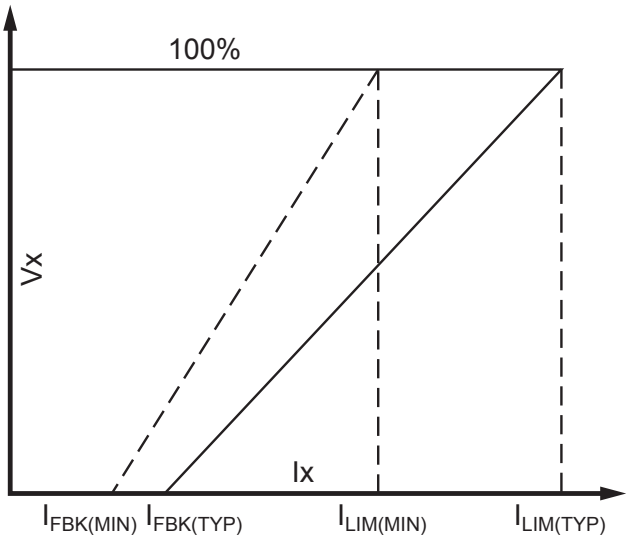


Figure 6: Typical LDO foldback characteristics

Pulse-Width Window Watchdog (PWWD)

The A4413 pulse-width window watchdog circuit monitors an external clock applied to the WD_{IN} pin. This clock should be generated by the primary microcontroller or DSP. The A4413 watchdog measures the time between two clock edges, either rising or falling. So the watchdog effectively measures both the "high" and "low" pulse widths, as shown in Figure 16.

If an incorrect pulse width is detected, the watchdog increments its fault counter by 10. If a correct pulse width is detected, the watchdog decrements its fault counter by 2. If the watchdog's fault counter exceeds 160, then the WD fault latch will be set and the WD_{OUT} pin will transition low. This fault condition is labelled WD_{FAULT} in Figure 16.

The watchdog and its fault latch will be reset if:

1. The WD_{ENn} pin is set high (i.e. WD is disabled), or
2. NPOR goes low (i.e. ENB and ENBAT are low), or
3. The internal rail, VCC, is low (VIN is removed), or
4. The bandgap, BG1, transitions low.

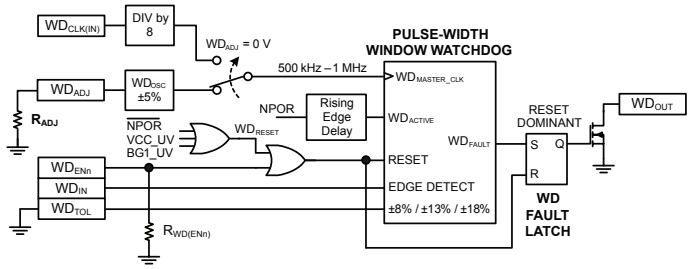


Figure 7: Pulse-Width Window Watchdog

The expected pulse width (PW) is programmed by connecting a resistor (R_{ADJ}) from the WD_{ADJ} pin to ground. The relationship between R_{ADJ} and PW is:

$$R_{ADJ} = 22.1 \times PW$$

where PW is in ms and R_{ADJ} is the required external resistor value in kΩ. The typical range for PW is 1 to 2 ms.

The watchdog will be enabled if the following two conditions are satisfied:

1. The WD_{ENn} pin is a logic low, and
2. NPOR transitions high and remains high for at least $t_{dWD(START)}$ (2 ms_{TYP}). This requires all regulators to be above their undervoltage thresholds.

The watchdog startup delay allows the microcontroller or DSP to complete its initialization routines before delivering a clock to the WD_{IN} pin. The $t_{dWD(START)}$ time is shown in both Figure 16 and Figure 17.

After startup, if no clock edges are detected at WD_{IN} for at least $t_{dWD(START)} + t_{WD(EDGE,TO)}$, the A4413 will set the WD latch and WD_{OUT} will transition low. $t_{WD(EDGE,TO)}$ varies with the value of R_{ADJ} as shown in the Electrical Characteristics table. The "no clock edge timeout" condition is shown as (1) in Figure 17.

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During normal operation, if clock activity is no longer detected at WD_{IN} for at least $t_{WD(ACT,TO)}$, the A4413 will set the WD latch, and WD_{OUT} will transition low. $t_{WD(ACT,TO)}$ varies with the value of R_{ADJ} as shown in the Electrical Characteristics table. The "loss of clock activity" condition is shown as (2) in Figure 17.

The nominal WD_{IN} pulse width is set by the value of R_{ADJ}. However, the pulse widths generated by a microcontroller or DSP depend on many factors and will have some pulse-to-pulse variation. The A4413 accommodates pulse-width variations by allowing the designer to select a "window" of allowable variations. The size of the window is chosen based on the voltage at the WD_{TOL} pin, as shown in Table 1.

Table 1: The WD_{TOL} pin voltage determines the WD_{IN} pulse-width tolerance or "window"

WD_{TOL} (V)	Allowed WD_{IN} Pulse-Width Tolerance
Low (0 V)	±8%
Float (Open)	±13%
High (VCC)	±18%

The watchdog performs its calculations based on an internally generated clock. The internal clock typically has an accuracy of ±2.5%, but may vary as much as ±5% due to IC process shifts and temperature variations. Variations in this clock result in a shift of the "OK Region" (i.e. the expected pulse width) at WD_{IN}, shown as a green area in Figure 18.

If the internal clock does not provide enough pulse-width measurement accuracy, the A4413 allows the designer to accept a high-precision clock at the $WD_{CLK(IN)}$ pin. If the $WD_{CLK(IN)}$ pin is used, then the WD_{ADJ} pin must be grounded. Figure 8 shows an example where a crystal and a tiny 6-pin driver (74LVC1GX04 by TI or NXP) are used to generate an external clock. The external clock should be in the 4 to 8 MHz frequency range for corresponding WD_{IN} pulse widths of 1 to 2 ms.

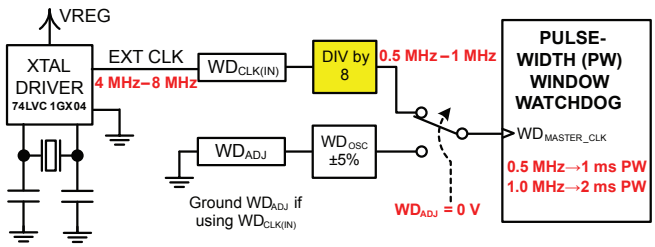


Figure 8: Applying an external clock to the $WD_{CLK(IN)}$ pin allows extremely accurate pulse-width measurements

Dual Bandgaps (BG_{VREF}, BG_{FAULT})

Dual bandgaps, or references, are implemented within the A4413. One bandgap (BG_{VREF}) is dedicated solely to closed-loop control of the output voltages. The second bandgap (BG_{FAULT}) is employed for fault detection functions. Having redundant bandgaps improves reliability of the A4413.

If the reference bandgap is out of specification (BG_{VREF}), then the output voltages will be out of specification and the monitoring bandgap will report a fault condition by setting NPOR and/or POK5V low.

If the monitoring bandgap is out of specification (BG_{FAULT}), then the outputs will remain in regulation, but the monitoring circuits will report a fault condition by setting NPOR and/or POK5V low.

The reference and fault detection bandgap circuits include two smaller secondary bandgaps that are used to detect undervoltage of the main bandgaps during power-up.

Adjustable Frequency, Synchronization (FSET/SYNC)

The PWM switching frequency of the A4413 is adjustable from 250 kHz to 2.4 MHz. Connecting a resistor from the FSET/SYNC pin to ground sets the "base" switching frequency. An FSET resistor with ±1% tolerance is recommended. The FSET resistor can be calculated using the following equation:

$$R_{FSET} = (21{,}956 / f_{OSC}) - 2.315$$

where f_{OSC} is the desired "base" oscillator frequency (PWM switching frequency) in kHz, and the resulting R_{FSET} value is in kΩ.

A graph of oscillator frequency (f_{OSC}) versus FSET resistor values is shown in Figure 9.

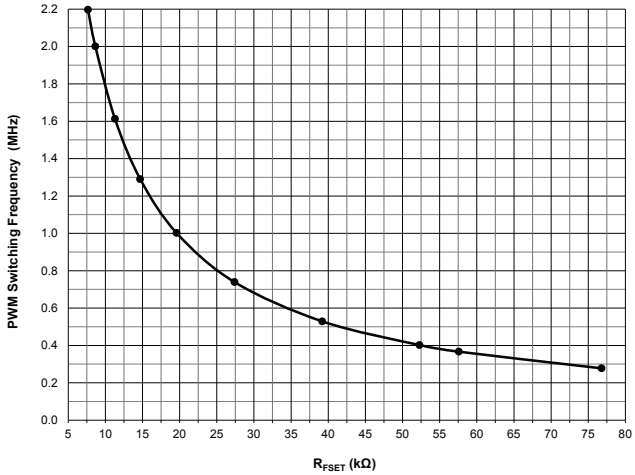


Figure 9: Oscillator Frequency (f_{OSC}) versus R_{FSET}

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The PWM frequency of the A4413 may be increased or decreased by applying a clock to the FSET/SYNC pin. The clock must satisfy the voltage thresholds and timing requirements shown in the Electrical Characteristics table.

Frequency Dithering and LX1 Slew Rate Control

The A4413 includes two innovative techniques to help reduce EMI/EMC for demanding automotive applications.

First, the A4413 performs pseudo-random dithering of the PWM frequency. Dithering the PWM frequency spreads the energy above and below the base frequency set by R_{FSET}. A typical fixed-frequency PWM regulator will create distinct "spikes" of energy at f_{OSC}, and at higher frequency multiples of f_{OSC}. Conversely, the A4413 spreads the spectrum around f_{OSC}, thus creating a lower magnitude at any comparative frequency. Frequency dithering is disabled if SYNC is used or V_{VIN} drops below approximately 8.3 V or above 18 V.

Second, the A4413 includes a pin to adjust the rising slew rate of the LX1 node by simply changing the value of a resistor from the SLEW pin to ground. Slower rise times of LX1 reduce ringing and high-frequency harmonics of the regulator. The rise time may be adjusted to be relatively long and will increase thermal dissipation of the pre-regulator if set too high. Typical LX1 slew rates are shown in Table 2.

Table 2: Typical LX1 Rising Slew Rate versus R_{SLEW}; LX1 Snubber: 8.66 Ω + 330 pF

R_{SLEW} (kΩ)	LX1 Rising Slew Rate (V/ns)	LX1 10%-90% Transition Time at 12 V_{VIN} (ns)
8.66	1.31	7.3
22.1	0.90	10.7
46.4	0.69	13.9
71.5	0.52	18.5
100	0.33	29.1
121	0.27	35.6
150	0.23	41.7

Enable Inputs (ENB, ENBAT)

Two enable pins are available on the A4413. A logic high on either of these pins enables the A4413. Both ENB and ENBAT must be low to disable the A4413.

One enable (ENB) is logic-level compatible for a microcontroller or DSP control. The other input (ENBAT) may be connected to a high-voltage ignition (IGN) or accessory (ACC) switch through a relatively low-value series resistance, 2 to 3.6 kΩ. For transient suppression, it is strongly recommended that a 0.10 to 0.47 µF capacitor be placed after the series resistance to form a low-pass filter to the ENBAT pin as shown in the Applications Schematic.

Bias Supply (VCC)

The bias supply (VCC) is generated by an internal linear regulator. This supply is the first rail to start up. Most of the internal control circuitry is powered by this supply. The bias supply includes some unique features to ensure reliable operation of the A4413. These features include:

1. Input voltage (VIN) undervoltage lockout
2. Undervoltage detection
3. Short-to-ground protection
4. Operation from VIN or VREG, whichever is higher

Charge Pump (VCP, CP1, CP2)

A charge pump provides the voltage necessary to drive the high-side n-channel MOSFETs in the pre-regulator and the linear regulator.

Two external capacitors are required for typical charge pump operation. During the first half of the charge pump cycle, the "flying" capacitor—between pins CP1 and CP2—is charged from either VIN or VREG, whichever is highest. During the second half of the charge pump cycle, the voltage on the flying capacitor charges the VCP capacitor. For most conditions, the VCP minus VIN voltage is regulated to approximately 6.6 V.

The charge pump will provide enough current to operate the pre-regulator and the LDO at 2.2 MHz, full load, and 125°C ambient, provided V_{VIN} is greater than 6 V. Optional components D3, D4, and CP3 (see Figure 10) must be included if V_{VIN} drops below 6 V. Diode D3 should be a silicon diode rated for at least 200 mA/50 V with less than 50 µA of leakage current when V_R = 13 V and T_A = 125°C. Diode D4 should be a 1 A Schottky diode with a very low forward voltage (V_F) rated to withstand at least 30 V.

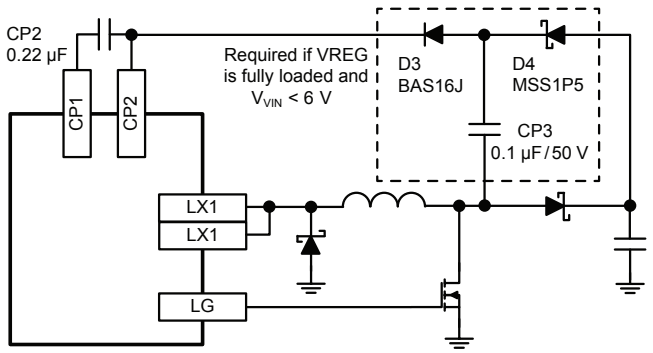


Figure 10: Charge pump enhancement components D3, D4, and CP3 are required if V_{VIN} < 6 V.

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The charge pump incorporates some protection features:

1. Undervoltage lockout of PWM switching
2. Overvoltage "latched" shutdown of the A4413

Startup and Shutdown Sequences

The startup and shutdown sequences of the A4413 are fixed. If no faults exist and ENBAT or ENB transition high, the A4413 will perform its startup routine. If ENBAT and ENB are low for at least $t_{dFILT(EN)} + t_{dLDO(OFF)}$ (typically 65 µs), the A4413 will begin its shutdown sequence. The startup and shutdown sequences are summarized in Table 3 and shown as a timing diagram in Figure 12.

Fault Reporting (NPOR, POK5V)

The A4413 includes two open-drain outputs for fault reporting, as shown in Figure 11. The NPOR comparator monitors TSD and the feedback pin of the synchronous buck ($V_{FB(ADJ)}$) for under- and overvoltage, as shown in Figure 12, Figure 13, and Figure 14. The POK5V comparators monitor the V5P pin for under- and overvoltage, as shown in Figure 12, Figure 13, and Figure 15.

The NPOR circuit includes a 2 ms delay after the synchronous buck's output has risen above its undervoltage threshold. This delay allows the microcontroller or DSP plenty of time to power-up and complete its initialization routines. There is minimal NPOR delay if the synchronous buck's output falls below its undervoltage threshold. The NPOR pin incorporates a 4 ms delay if the synchronous bucks output exceeds its overvoltage threshold.

There are no significant delays on the POK5V output if V5P rises above or falls below its undervoltage thresholds. Similar to the NPOR pin, the POK5V pin incorporates a 4 ms delay if the V5P outputs exceed its overvoltage threshold.

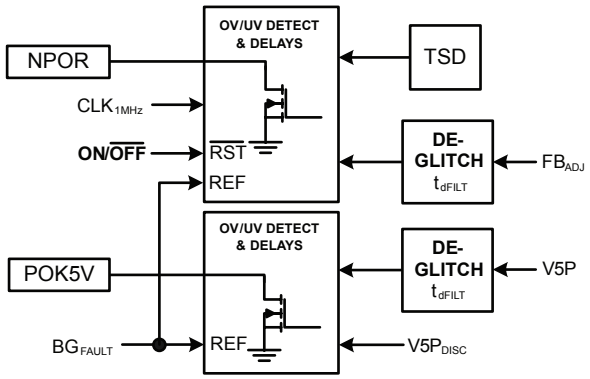


Figure 11: NPOR and POK5V Fault Outputs

The V5P "short-to-battery" monitor is unique: if V5P is accidently connected to the battery voltage, then POK5V will bypass the normal 4 ms overvoltage delay and set itself low immediately.

Fault modes and their effects on NPOR and POK5V are covered in detail in Table 4.

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Table 3: Startup and Shutdown Logic (signal names consistent with Functional Block Diagram)

A4413 Status Signals							Regulator Control Bits (0 = OFF, 1 = ON)			A4413 MODE
ON/$\overline{\text{OFF}}$	MPOR	VREG UV	SS1 LOW	ADJ UV	SS2 LOW	V5P UV	VREG ON	ADJ ON	LDO ON	
X	1	1	1	1	1	1	0	0	0	RESET
0	0	1	1	1	1	1	0	0	0	OFF
1	0	1	1	1	1	1	1	0	0	STARTUP
1	0	0	0	1	1	1	1	1	0	↓
1	0	0	0	0	0	1	1	1	1	↓
1	0	0	0	0	0	0	1	1	1	RUN
0	0	0	0	0	0	0	1	1	1	DEGLITCH + DELAY
0	0	0	0	0	0	0	1	1	0	SHUTTING DOWN
0	0	0	0	0	X	1	1	0	0	↓
0	0	0	X	1	X	1	0	0	0	↓
0	0	1	1	1	1	1	0	0	0	OFF

X = DON'T CARE

ON/$\overline{\text{OFF}}$ = ENBAT + ENB

MPOR = VIN_UV + VCC_UV + VCP_UV + BG1_UV + BG2_UV + SLEW_UV/OV + FSET_UV/OV + TSD + VCP_OV (latched) + $D1_{MISSING}$ (latched) + $I_{LIM(LX1)}$ (latched) + $I_{LIM(LX2)}$ (latched)

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Table 4: Summary of Fault Mode Operation

FAULT TYPE and CONDITION	A4413 RESPONSE TO FAULT	NPOR $V_{FB(ADJ)}$	POK5V V5P	LATCHED FAULT?	RESET METHOD
V5P short to VBAT	POK5V goes low when a V5P disconnect occurs.	Not affected	Low when V5P disconnect occurs	NO	Check for short circuits on V5P
V5P overvoltage (OV)	If OV condition persists for more than t_{dOV}, then set POK5V low.	Not affected	Low if $t > t_{dOV}$	NO	Check for short circuits on V5P
FB_{ADJ} overvoltage (OV)	If OV condition persists for more than t_{dOV}, then set NPOR low. The V5P LDO must remain active.	Low if $t > t_{dOV}$	Not affected	NO	Check for short circuits on FB_{ADJ}
V5P undervoltage (UV)	Closed-loop control will try to raise the LDOs voltage but may be constrained by the foldback current limit. Note: the LDO may be soft-starting.	Not affected	Low	NO	Decrease the load or wait for SS to finish
FB_{ADJ} undervoltage (UV)	Closed-loop control will try to raise the voltage but may be constrained by the pulse-by-pulse current limit. The ADJ regulator may need to enter hiccup mode. Also, the ADJ regulator may be simply soft-starting.	Low	Not affected	NO	Decrease the load or wait for SS to finish
V5P overcurrent (OC)	Foldback current limit will reduce the output voltage of the LDO.	Not affected	Low if the V5P output voltage droops	NO	Decrease the load
FB_{ADJ} pin open circuit	A small internal current sink pulls the voltage at the FB_{ADJ} pin high and mimics an ADJ regulator overvoltage condition.	Low because $V_{FB(ADJ)} > V_{FB(ADJ,OV,H)}$	Not affected	NO	Connect the FB_{ADJ} pin
FB_{ADJ} regulator overcurrent (i.e. hard short to ground) $t < t_{HIC2(EN)}$, $V_{FB(ADJ)} < 200$ mV	Continue to PWM but turn off LX2 when the high side MOSFET current exceeds I_{LIM2}.	Low	Not affected	NO	Remove the short circuit
FB_{ADJ} regulator overcurrent (i.e. hard short to ground) $t > t_{HIC2(EN)}$, $V_{FB(ADJ)} < 200$ mV	Enters hiccup mode after 30 OCP faults.	Low	Not affected	NO	Decrease the load
FB_{ADJ} regulator overcurrent (i.e. soft short to ground) $t > t_{HIC2(EN)}$, $V_{FB(ADJ)} > 200$ mV	Enters hiccup mode after 120 OCP faults.	Low if $V_{FB(ADJ)} < V_{FB(ADJ,UV,L)}$	Not affected	NO	Decrease the load
VREG pin open circuit	V_{VREG} will decay to 0 V and LX1 will switch at maximum duty cycle. The voltage on the VREG output capacitors will be very close to VIN/VBAT.	Low when the output voltage droops	Low if the V5P output voltage droops	NO	Connect the VREG pin
VREG overcurrent (i.e. hard short to ground) $t < t_{HIC1(EN)}$, $V_{VREG} < 1.3$ V, $V_{COMP1} \neq V_{EA1(VO,MAX)}$	Continue to PWM but turn off LX1 when the high side MOSFET current exceeds I_{LIM1}.	Low	Low	NO	Remove the short circuit
VREG overcurrent (i.e. hard short to ground) $t > t_{HIC1(EN)}$, $V_{VREG} < 1.3$ V, $V_{COMP1} = V_{EA1(VO,MAX)}$	Enters hiccup mode after 30 OCP faults.	Low	Low	NO	Decrease the load

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Table 4: Summary of Fault Mode Operation (continued)

FAULT TYPE and CONDITION	A4413 RESPONSE TO FAULT	NPOR $V_{FB(ADJ)}$	POK5V V5P	LATCHED FAULT?	RESET METHOD
VREG overcurrent (i.e. soft short to ground) $t > t_{HIC1(EN)}$, $V_{VREG} > 1.3$ V, $V_{COMP1} = V_{EA1(VO,MAX)}$	Enters hiccup mode after 120 OCP faults.	Low if the output voltage droops	Low if the V5P output voltage droops	NO	Decrease the load
VREG overvoltage (OV) $V_{VREG} > V_{VREG(OV,HI)}$	Control loop will temporarily stop PWM switching of LX1. LX1 will resume switching when V_{VREG} returns to its normal range.	High, but depends on $V_{FB(ADJ)}$	High, but depends on the V5P output	NO	None
VREG asynchronous diode (D1) missing	Results in a Master Power-On Reset (MPOR) after 1 detection. All regulators are shut off.	Low when the output voltage droops	Low if the V5P output voltage droops	YES	Place D1 then cycle EN or VIN
Asynchronous diode (D1) short-circuited or LX1 shorted to ground	Results in an MPOR after 1 detection of the high-side MOSFET current exceeding $I_{LIM(LX1)}$, so all regulators are shut off.	Low when the output voltage droops	Low if the V5P output voltage droops	YES	Remove the short then cycle EN or VIN
LX2 shorted to ground	If LX2 is less than V_{VREG} – 1.2 V after the internal blanking time (~60 ns), the high-side FET will be shut off.	Transitions low when the output voltage droops	Not affected	NO	Remove the short
Slew pin open circuit (SLEW_OV)	Results in a “default” slew rate of 1.5 V/ns for LX1.	Operates normally	Operates normally	NO	Place the Slew Rate Resistor
Slew pin shorted to ground (SLEW_UV)	Results in a “default” slew rate of 1.5 V/ns for for LX1.	Operates normally	Operates normally	NO	Place the Slew Rate Resistor
FSET/SYNC pin open circuit (FSET/SYNC_OV)	Results in “default” PWM frequency of 1 MHz	Operates normally	Operates normally	NO	Connect the FSET/SYNC pin
FSET/SYNC pin shorted to ground (FSET/SYNC_UV)	Results in “default” PWM frequency of 1 MHz.	Operates normally	Operates normally	NO	Remove the short circuit
Charge pump (VCP) overvoltage (OV)	Results in an MPOR, so all regulators are off.	Low	Low	YES	Check VCP/CP1/CP2, then cycle EN or VIN
Charge pump (VCP) undervoltage (UV)	Results in an MPOR, so all regulators are off.	Low	Low	NO	Check VCP/CP1/CP2 components
CP1 or CP2 pin open circuit	Results in VCP_UV and an MPOR, so all regulators are off.	Low	Low	NO	Connect the CP1 or CP2 pins
CP1 pin shorted to ground	Results in VCP_UV and an MPOR, so all regulators are off.	Low	Low	NO	Remove the short circuit
CP2 pin shorted to ground	Results in high current from the charge pump and (intentional) fusing of an internal trace. Also results in MPOR, so all regulators are off.	Low	Low	N/A	Remove the short circuit and replace the A4413

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Table 4: Summary of Fault Mode Operation (continued)

FAULT TYPE and CONDITION	A4413 RESPONSE TO FAULT	NPOR $V_{FB(ADJ)}$	POK5V V5P	LATCHED FAULT?	RESET METHOD
BG_{VREF} or BG_{FAULT} undervoltage (UV)	Results in an MPOR, so all regulators are off.	Low	Low	NO	Raise VIN or wait for BGs to power up
BG_{VREF} or BG_{FAULT} overvoltage (OV)	If BG_{VREF} is too high, all regulators will appear to be OV (because BG_{FAULT} is good) If BG_{FAULT} is too high, all regulators will appear to be UV (because BG_{VREF} is good)	Low	Low	N/A	Replace the A4413
VCC undervoltage or pin shorted to ground	Results in an MPOR, so all regulators are off.	Low	Low	NO	Raise VIN or remove short from at VCC pin
Thermal shutdown (TSD)	Results in an MPOR, so all regulators are off.	Low	Low	NO	Let the A4413 cool down

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TIMING DIAGRAMS
(Not to Scale)

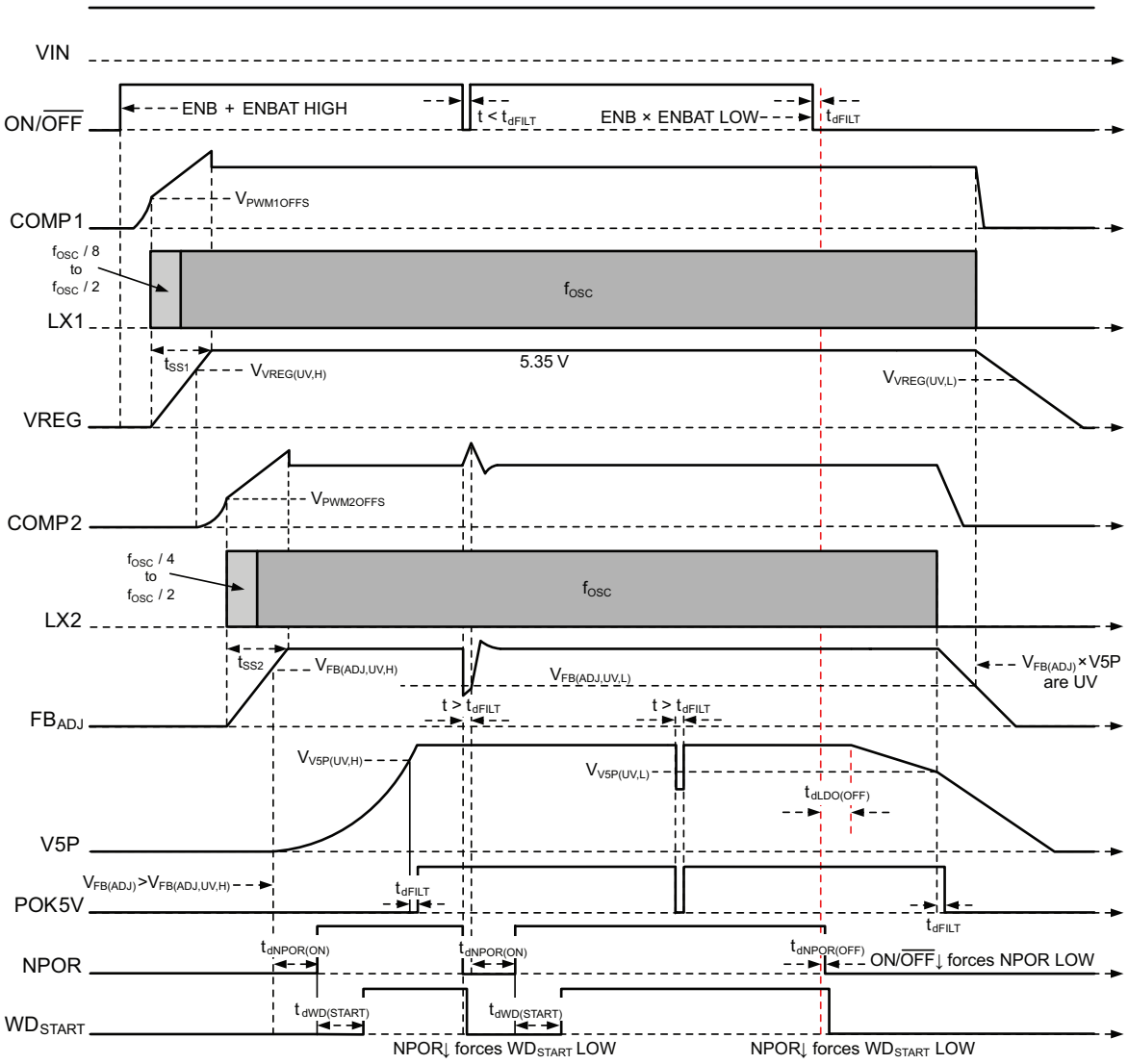


Figure 12: Startup and Shutdown by ENBAT or ENB with V_{VIN} = 12 V_{DC}. Also shows reactions to glitches on V5P or FB_{ADJ}.

× is for "and", + is for "or"

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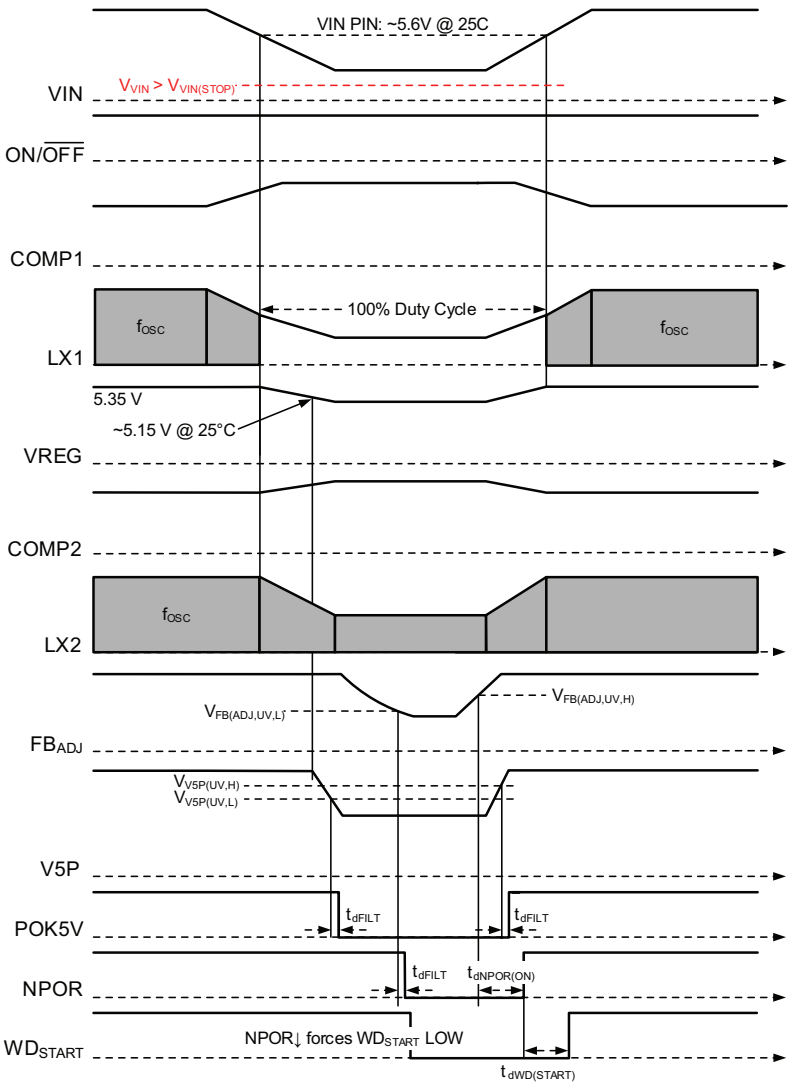


Figure 13: Buck Only Mode, Input Voltage (VIN) Undervoltage, $V_{VIN} > V_{VIN(STOP)}$

× is for "and", + is for "or"

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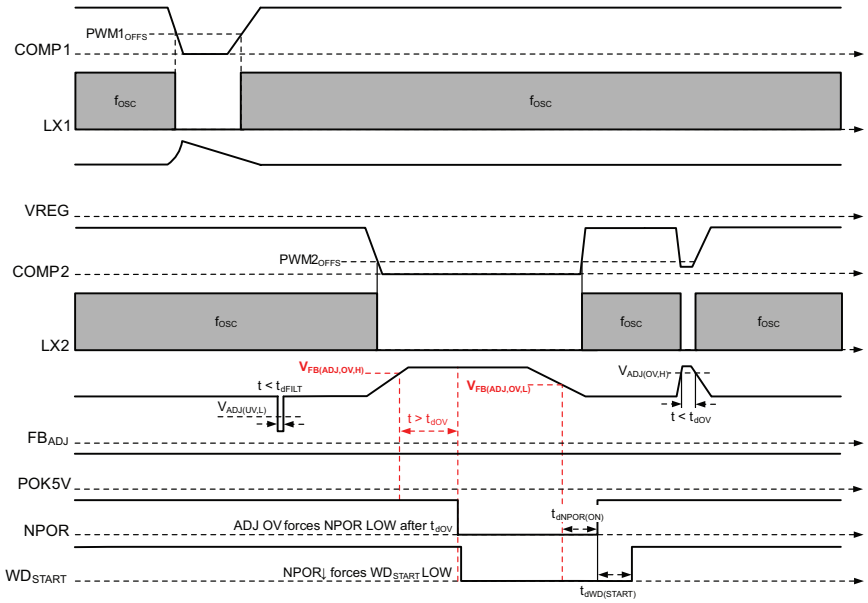
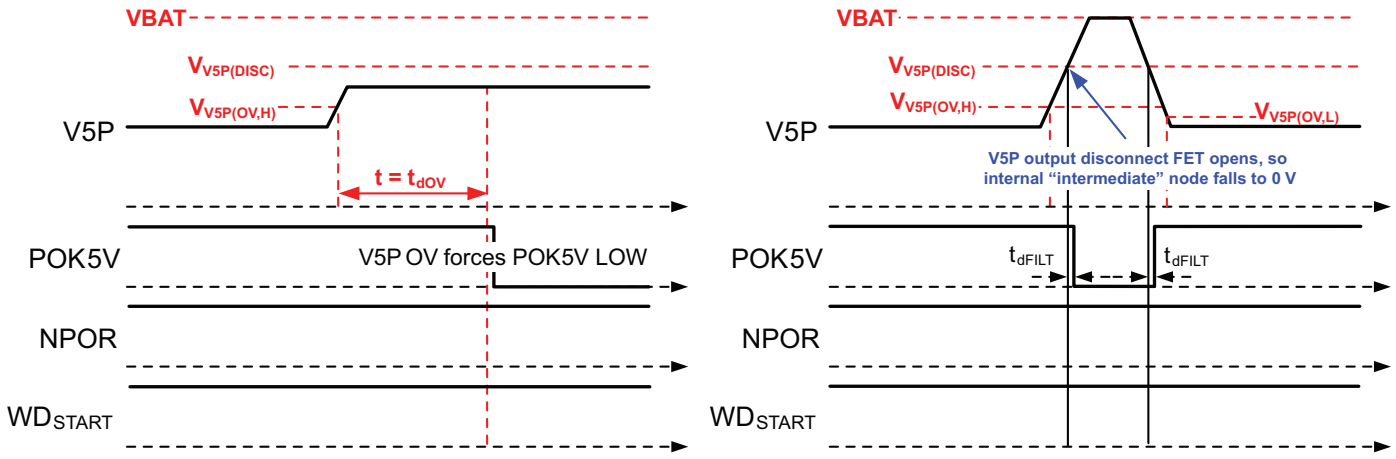


Figure 14: VREG and ADJ Overvoltage Operation

× is for "and", + is for "or"



CASE 1: $V_{V5P(DISC)} > V_{V5P} > V_{V5P(OV,H)}$

CASE 2: $V_{V5P} > V_{V5P(DISC)}$

Figure 15: Overvoltage Cases for V5P

× is for "and", + is for "or"

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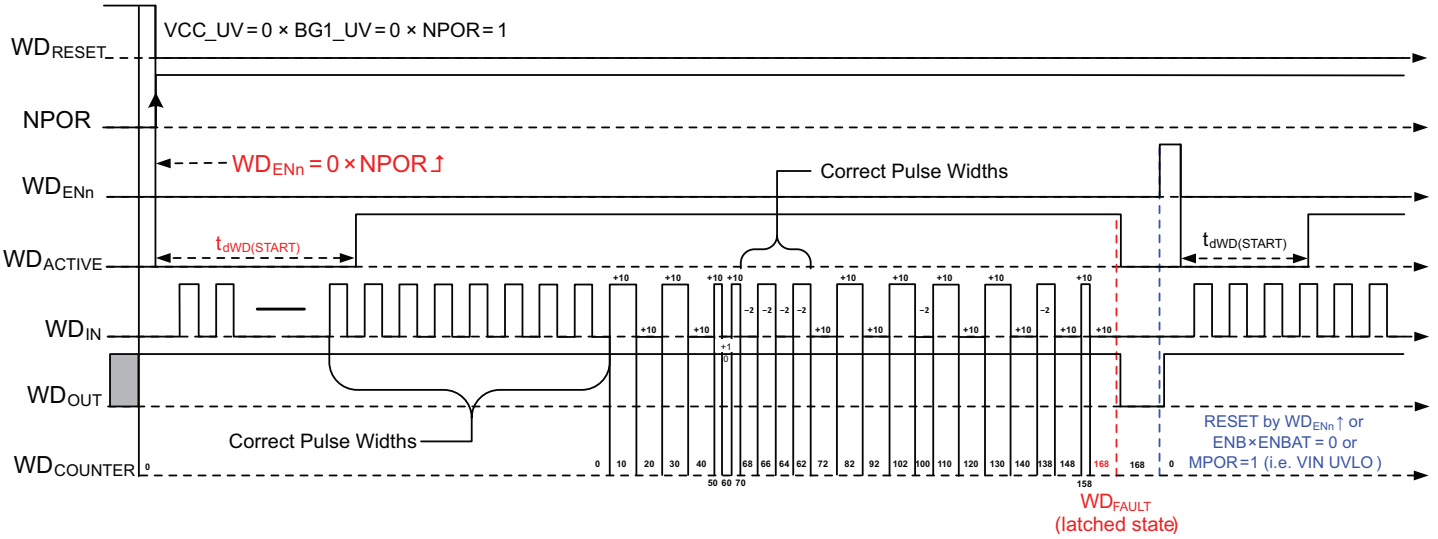


Figure 16: Watchdog operation with correct pulse widths, initially, but a WD fault occurs because too many incorrect pulse widths occur and WD_{COUNT} > 160.

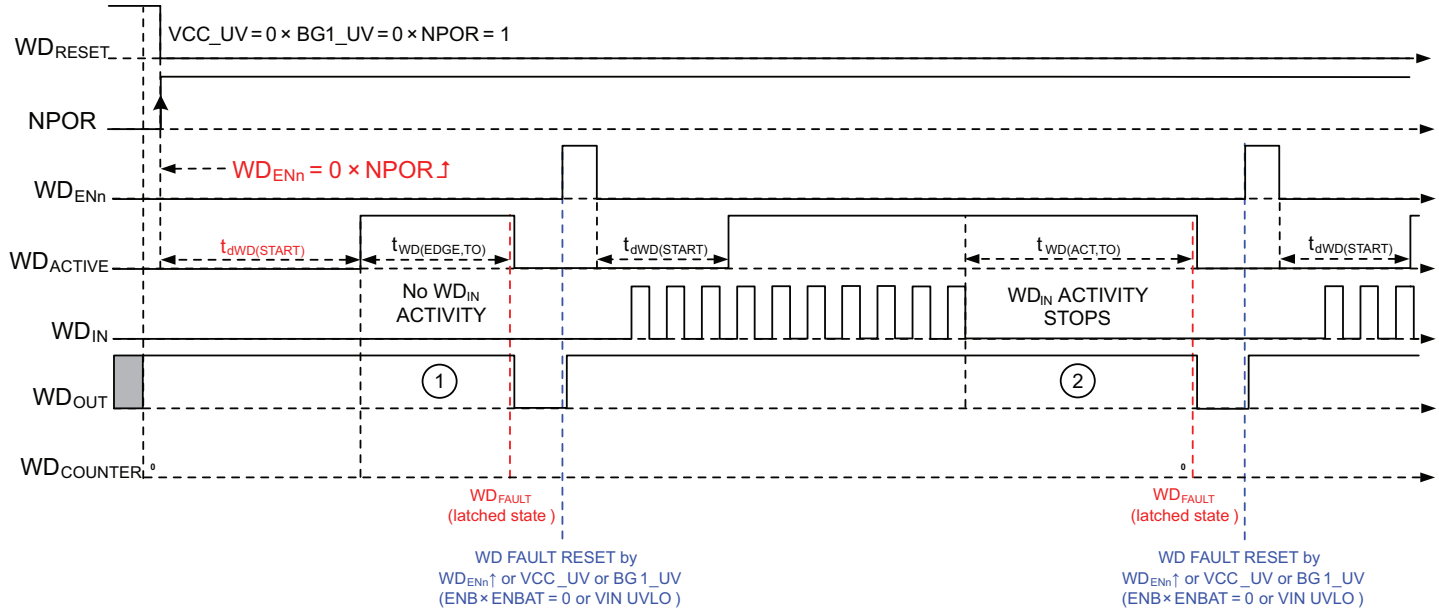


Figure 17: Watchdog operation with faults from:

1. After $t_{dWD(START)}$, there is no WD_{IN} activity for t > $t_{WD(EDGE,TO)}$
2. WD_{IN} activity stops

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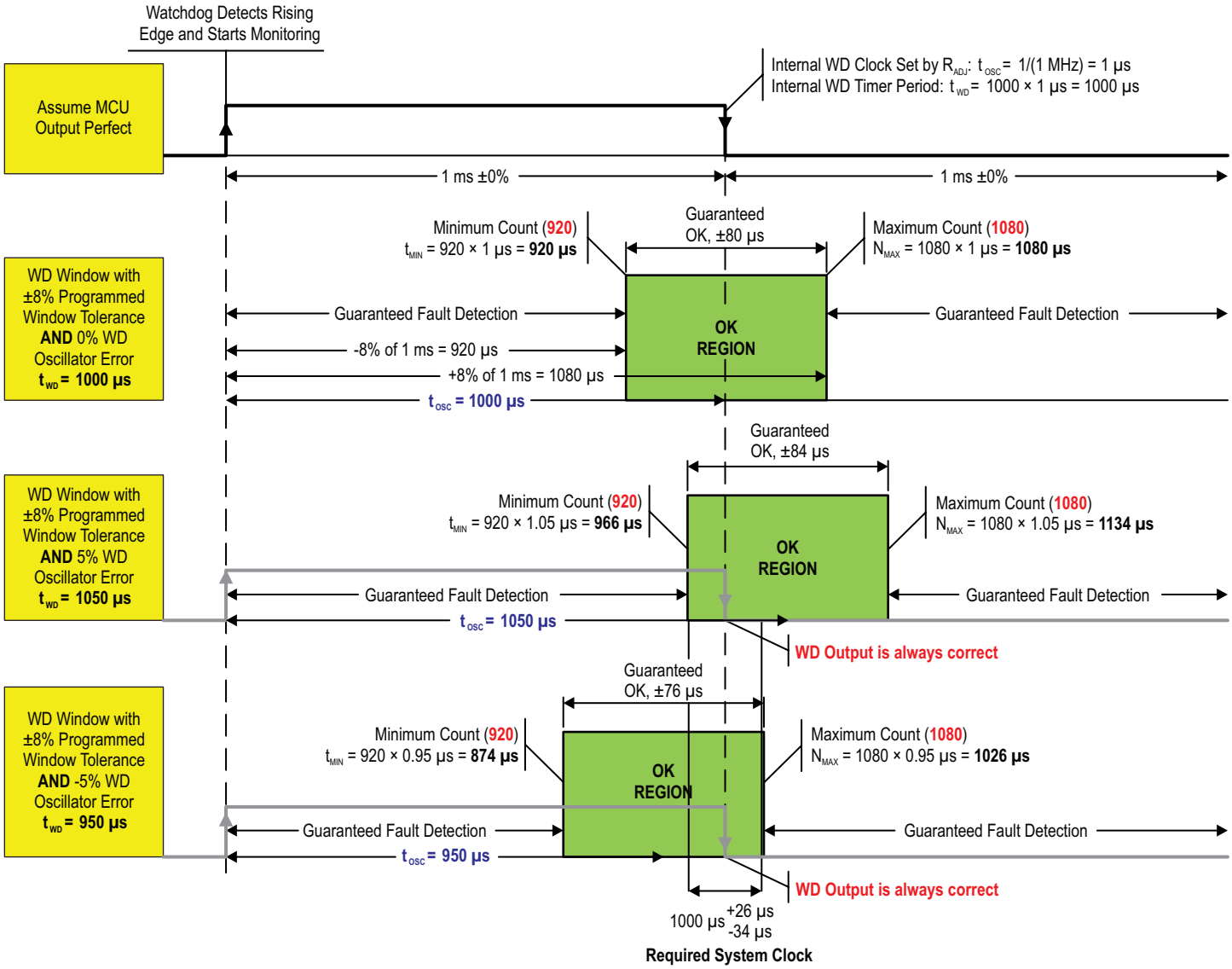


Figure 18: Typical Watchdog Timer System Level Functionality (times are not to scale)

A4413 and System Operating Parameters:
1 ms pulse widths coming from the microcontroller
±8% WD Window Tolerance Selected (WD_{ADJ} = GND)
±5% WD Oscillator Tolerance (worst case maximum)

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DESIGN AND COMPONENT SELECTION

PWM Switching Frequency (R_{FSET})

When the PWM switching frequency is chosen, the designer should be aware of the minimum controllable on-time, $t_{ON(MIN)}$, of the A4413. If the system's required on-time is less than the A4413 minimum controllable on-time, then switch node jitter will occur and the output voltage will have increased ripple or oscillations.

The PWM switching frequency should be calculated using equation 1, where $t_{ON(MIN)}$ is the minimum controllable on-time of the A4413 (85 ns_{TYP}) and $V_{VIN(MAX)}$ is the maximum required operational input voltage (not the peak surge voltage).

$$f_{OSC} < \frac{5.35\ V}{t_{ON(MIN)} \times V_{VIN(MAX)}} \quad (1)$$

If the A4413's synchronization function is used, then the base oscillator frequency should be chosen such that jitter will not result at the maximum synchronized switching frequency according to equation 1.

Charge Pump Capacitors

The charge pump requires two capacitors: a 1 µF connected from pin VCP to VIN, and a 0.22 µF connected between pins CP1 and CP2. These capacitors should be high-quality ceramic capacitors, such as X5R or X7R, with voltage ratings of at least 16 V.

Pre-Regulator Output Inductor (L1)

For peak current-mode control, it is well known that the system will become unstable when the duty cycle is above 50% without adequate slope compensation (S_{E1}). However, the slope compensation in the A4413 is a fixed value based on the oscillator frequency (f_{OSC}). Therefore, it's important to calculate an inductor value so the falling slope of the inductor current (S_{F1}) will work well with the A4413's fixed slope compensation.

Equation 2 can be used to calculate a range of values for the output inductor for the pre-regulator. In equation 2, slope compensation (S_{E1}) is a function of the switching frequency (f_{OSC}) according to equation 3, and V_F is the asynchronous diodes forward voltage.

$$\frac{(5.25\ V + V_F)}{S_{E1}} \le L1 \le \frac{(5.45\ V + V_F)}{\frac{S_{E1}}{2}} \quad (2)$$

$$S_{E1} = 0.00051 \times f_{OSC} + 0.0275 \quad (3)$$

When using equations 2 and 3, f_{OSC} is in kHz, S_{E1} is in A/µs, and L1 will be in µH.

If equation 2 yields an inductor value that is not a standard value, then the next highest standard value should be used. The final inductor value should allow for 10%-20% of initial tolerance and 20%-30% of inductor saturation.

The inductor should not saturate given the peak operating current according to equation 4. In equation 4, $V_{VIN(MAX)}$ is the maximum continuous input voltage, such as 18 V, and V_F is the asynchronous diodes forward voltage.

$$I_{PEAK1} = 3.3\ A - \frac{S_{E1} \times (5.25\ V + V_F)}{1.1 \times f_{OSC} \times (V_{VIN(MAX)} + V_F)} \quad (4)$$

After an inductor is chosen, it should be tested during output short-circuit conditions. The inductor current should be monitored using a current probe. A good design should ensure the inductor or the regulator are not damaged when the output is shorted to ground at maximum continuous input voltage and the highest expected ambient temperature.

The inductor ripple current can be calculated using equation 5.

$$\Delta I_{L1} = \frac{(V_{VIN(TYP)} - 5.35\ V) \times 5.35\ V}{f_{OSC} \times L_1 \times V_{VIN(TYP)}} \quad (5)$$

Pre-Regulator Output Capacitance

The output capacitors filter the output voltage to provide an acceptable level of ripple voltage, and they store energy to help maintain voltage regulation during a load transient. The voltage rating of the output capacitors must support the output voltage with sufficient design margin.

Within the first few PWM cycles after a load transient, the deviation of V_{VREG} will depend mainly on the magnitude of the load step (ΔI_{LOAD1}), the value of the output inductor (L1), the output capacitance (C_{OUT}), and the maximum duty cycle of the pre-regulator (D_{MAX1}). Equations 6 and 7 can be used to calculate a minimum output capacitance to maintain V_{VREG} within 0.5% of its target for a 500 mA load step at only 7 V_{IN}.

$$C_{OUT} \ge \frac{L1 \times (500\ mA)^2}{2 \times (7.0\ V - 5.25\ V) \times (0.005 \times 5.25\ V) \times D_{MAX1}} \quad (6)$$

$$D_{MAX1} = \left(\frac{1}{f_{OSC}} - 80\ ns\right) \times f_{OSC} \quad (7)$$

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After the load transient occurs, the output voltage will deviate from its nominal value until the error amplifier can bring the output voltage back to its nominal value. The speed at which the error amplifier will bring the output voltage back to its setpoint will depend mainly on the closed-loop bandwidth of the system. Selection of the compensation components (R_{Z1}, C_{Z1}, C_{P1}) are discussed in more detail in the Pre-Regulator Compensation section of this datasheet.

The output voltage ripple (ΔV_{VREG}) is a function of the output capacitors parameters: C_{OUT}, ESR_{Co}, and ESL_{Co} according to equation 8.

$$\Delta V_{VREG} = \Delta I_L \times ESR_{Co} + \frac{V_{VIN} - V_{VREG}}{L_O} \times ESL_{Co} + \frac{\Delta I_L}{8 \times f_{OSC} \times C_{OUT}} \quad (8)$$

The type of output capacitors will determine which terms of equation 8 are dominant. For the A4413 and automotive environments, only ceramic capacitors are recommended. The ESR_{CO} and ESL_{CO} of ceramic capacitors are virtually zero, so the peak-to-peak output voltage ripple of V_{VREG} will be dominated by the third term of equation 8.

$$\Delta V_{VREG(PP)} = \frac{\Delta I_L}{8 \times f_{OSC} \times C_{OUT}} \quad (9)$$

Pre-Regulator Ceramic Input Capacitance

The ceramic input capacitors must limit the voltage ripple at the VIN pin to a relatively low voltage during maximum load. Equation 10 can be used to calculate the minimum input capacitance,

$$C_{IN} \geq \frac{I_{VREG(MAX)} \times 0.25}{0.90 \times f_{OSC} \times 50\ mV_{PP}} \quad (10)$$

where $I_{VREG(MAX)}$ is the maximum current from the pre-regulator,

$$I_{VREG(MAX)} = I_{V5P} + \frac{V_{OUT(ADJ)} \times I_{OUT(ADJ)}}{5.35\ V \times 85\%} + 10\ mA \quad (11)$$

A good design should consider the DC bias effect on a ceramic capacitor: as the applied voltage approaches the rated value, the capacitance value decreases. The X5R- and X7R-type capacitors should be the primary choices due to their stability versus both DC bias and temperature. For all ceramic capacitors, the DC bias effect is even more pronounced on smaller case sizes, so a good design will use the largest affordable case size (i.e. 1206/16 V or 1210/50 V).

Also, for improved EMI/EMC performance, it is recommended that two small capacitors be placed as close as physically possible to the VIN pins to address frequencies above 10 MHz. For example, a 0.1 µF/X7R/0603 and a 220 pF/COG/0402 capacitor will address frequencies up to 20 MHz and 200 MHz, respectively.

Pre-Regulator Asynchronous Diode (D1)

The highest peak current in the asynchronous diode (D1) occurs during overload and is limited by the A4413. Equation 4 can be used to calculate this current.

The highest average current in the asynchronous diode occurs when V_{VIN} is at its maximum, D_{BOOST} = 0%, and D_{BUCK} = minimum (10%),

$$I_{AVG} = (1 - D_{BUCK}) \times I_{VREG(MAX)} = 0.9 \times I_{VREG(MAX)} \quad (12)$$

where $I_{VREG(MAX)}$ is calculated using equation 11.

Pre-Regulator Boost MOSFET (Q1)

The maximum RMS current in the boost MOSFET (Q1) occurs when V_{VIN} is very low and the boost operates at its maximum duty cycle,

$$I_{Q1(RMS)} = \sqrt{D_{MAX(BST)} \times \left[\left(I_{PEAK1} - \frac{\Delta I_{L1}}{2}\right)^2 + \frac{\Delta I_{L1}}{12}\right]} \quad (13)$$

where I_{PEAK1} and ΔI_{L1} are derived using equations 4 and 5, respectively, and $D_{MAX(BST)}$ is identified in the Electrical Characteristics table.

The boost MOSFET should have a total gate charge of less than 14 nC at a V_{GS} of 5 V. The V_{DS} rating of the boost MOSFET should be at least 20 V. Several recommended part numbers are shown in the Functional Block Diagram / Typical Schematic.

Pre-Regulator Boost Diode (D2)

The maximum average current in the pre-regulator's boost diode is simply the output current, calculated with equation 11. However, depending on the minimum input voltage, the A4413 will force relatively high peak currents when the boost (LG) becomes active. The A4413 will limit the boost current to the value calculated by equation 4. A diode that is capable of supporting both the average and peak current must be selected.

Pre-Regulator Compensation (R_{Z1}, C_{Z1}, C_{P1})

Although the A4413 can operate in buck-boost mode at low input voltages, it still can be considered a buck converter when examining the control loop. The following equations can be used to calculate the compensation components.

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First, select the target crossover frequency for the final system. While switching at over 2 MHz, the crossover is governed by the required phase margin. Since a type II compensation scheme is used, the system is limited to the amount of phase that can be added. Hence, a relatively safe crossover frequency (f_{C1})—in the region of 40 kHz—is selected. The total system phase and stability will drop at higher crossover frequencies. The R_{Z1} calculation is based on the gain required to set the crossover frequency and can be calculated by equation 14.

$$R_{Z1} = \frac{13.38 \times \pi \times f_{C1} \times C_{OUT}}{gm_{POWER1} \times gm_{EA1}} \quad (14)$$

The series capacitor (C_{Z1}) along with the resistor (R_{Z1}) set the location of the compensation zero. This zero should be placed no lower than ¼ of the crossover frequency but should be kept to a minimum to provide a fast integral response time. Equation 15 can be used to estimate this capacitor value.

$$C_{Z1} > \frac{4}{2\pi \times R_{Z1} \times f_{C1}} \quad (15)$$

Allegro recommends adding a small capacitor (C_{P1}) in parallel with the series combination of R_{Z1}/C_{Z1} to roll off the error amplifier gain at high frequency. This capacitor usually helps reduce LX1 pulse-width jitter, but if too large, it will also decrease the loop phase margin.

Allegro recommends using this capacitor to set a pole at approximately 8× the loop crossover frequency (f_{C1}), as shown in equation 16. If a non-standard capacitor value results, the next higher available value should be used.

$$C_{P1} \approx \frac{1}{2\pi \times R_{Z1} \times 8 \times f_{C1}} \quad (16)$$

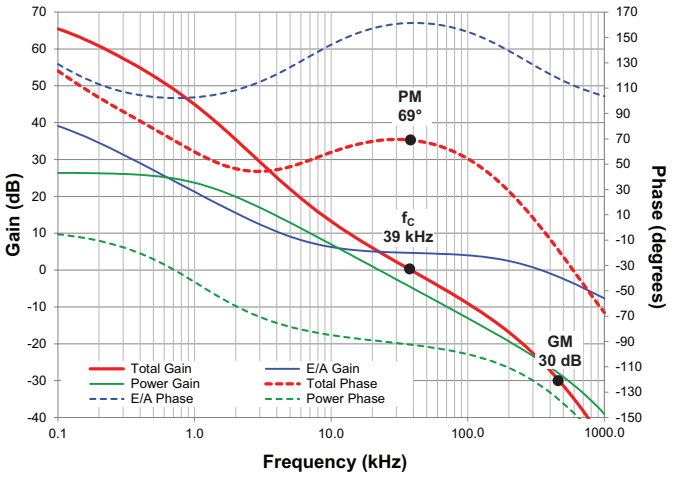


Figure 19: Bode Plot for the Pre-Regulator

R_{Z1} = 15.8 kΩ, C_{Z1} = 1.5 nF, C_{P1} = 27 pF
Lo = 6.8 µH, Co = 3 × 10 µF / 16 V / 1206

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Synchronous Buck Component Selection

Setting the Output Voltage (R_{FB1} and R_{FB2})

The A4413 allows the user to program the output voltage of the synchronous buck from 0.8 to 3.3 V. This is achieved by adding a resistor divider from its output to ground and connecting the center point to the FB_{ADJ} pin; see Figure 20 below.

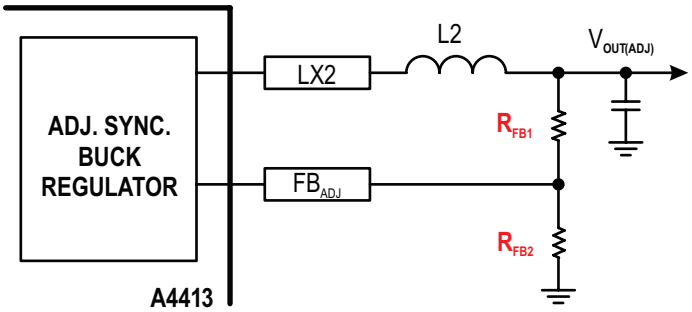


Figure 20: Setting the Synchronous Buck Output

The ratio of the feedback resistors can be calculated based on equation 17.

$$\frac{R_{FB1}}{R_{FB2}} = \left(\frac{V_{OUT(ADJ)}}{800\ mV} - 1\right) \quad (17)$$

Synchronous Buck Output Inductor (L2)

Equation 18 can be used to calculate a range of values for the output inductor for the synchronous buck regulator. Slope compensation (S_{E2}) can be calculated using equation 19.

$$\frac{V_{OUT(ADJ)}}{2 \times S_{E2}} \leq L2 \leq \frac{V_{OUT(ADJ)}}{S_{E2}} \quad (18)$$

$$S_{E2} = 0.000306 \times f_{OSC} + 0.0175 \quad (19)$$

When working with equations 18 and 19, f_{OSC} is in kHz, S_{E2} is in A/µs, and L2 will be in µH.

If equation 18 yields an inductor value that is not a standard value, then the next closest available value should be used. The final inductor value should allow for 10%-20% of initial tolerance and 20%-30% for inductor saturation.

The inductor should not saturate given the peak current at overload according to equation 20.

$$I_{PEAK2} = 2.4\ A - \frac{S_{E2} \times V_{OUT(ADJ)}}{1.1 \times f_{OSC} \times 5.45\ V} \quad (20)$$

After an inductor is chosen, it should be tested during output short-circuit conditions. The inductor current should be monitored using a current probe. A good design should ensure the inductor or the regulator are not damaged when the output is shorted to ground at maximum input voltage and the highest expected ambient temperature.

Once the inductor value is known the inductor ripple current can be calculated using equation 21. The inductor ripple current is used when calculating the output voltage ripple, as shown in equation 24.

$$\Delta I_{L2} = \frac{(5.35\ V \times V_{OUT(ADJ)}) \times V_{OUT(ADJ)}}{f_{OSC} \times L2 \times 5.35\ V} \quad (21)$$

Synchronous Buck Output Capacitance

Within the first few PWM cycles after a load transient, the deviation of $V_{OUT(ADJ)}$ will depend mainly on the magnitude of the load step (ΔI_{LOAD2}), the value of the output inductor (L2), the output capacitance ($C_{OUT(ADJ)}$), and the maximum duty cycle of the synchronous converter (D_{MAX2}). Equations 22 and 23 can be used to calculate a minimum output capacitance to maintain $V_{OUT(ADJ)}$ within 0.5% of its target for a 400 mA (50%) load step.

$$C_{OUT(ADJ)} \geq \frac{L2 \times (400\ mA)^2}{2 \times (5.25\ V - V_{OUT(ADJ)}) \times (0.005 \times V_{OUT(ADJ)}) \times D_{MAX2}} \quad (22)$$

$$D_{MAX2} = \left(\frac{1}{f_{OSC}} - 110\ ns\right) \times f_{OSC} \quad (23)$$

After the load transient occurs, the output voltage will deviate from its nominal value until the error amplifier can bring the output voltage back to its nominal value. The speed at which the error amplifier will bring the output voltage back to its setpoint will depend mainly on the closed-loop bandwidth of the system. Selection of the compensation components (R_{Z1}, C_{Z1}, C_{P1}) are discussed in more detail in the Synchronous Buck Compensation section of this datasheet.

Allegro recommends the use of ceramic capacitors for the synchronoous buck. The peak-to-peak voltage ripple of the synchronous buck ($\Delta V_{OUT(ADJ,PP)}$) can be calculated with equation 24.

$$\Delta V_{OUT(ADJ,PP)} = \frac{\Delta I_{L2}}{8 \times f_{OSC} \times C_{OUT(ADJ)}} \quad (24)$$

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Synchronous Buck Compensation (R_{Z2}, C_{Z2}, C_{P2})

Again, similar techniques as used with the pre-regulator can be used to compensate the synchronous buck.

For the synchronous buck, select 45 kHz for the crossover frequency (f_{C2}) of the synchronous buck. Then, equation 25 can be used to calculate R_{Z2}.

$$R_{Z2} = \frac{V_{OUT(ADJ)} \times 2\pi \times f_{C2} \times C_{OUT(ADJ)}}{800\ mV \times gm_{POWER2} \times gm_{EA2}} \quad (25)$$

The series capacitor (C_{Z2}) along with the resistor (R_{Z2}) set the location of the compensation zero. This zero should be placed no lower than ¼ the crossover frequency and should be kept to a minimum to provide a fast integral response time. Equation 26 can be used to estimate this capacitor value.

$$C_{Z2} > \frac{4}{2\pi \times R_{Z2} \times f_{C2}} \quad (26)$$

Allegro recommends adding a small capacitor (C_{P2}) in parallel with the series combination of R_{Z2}/C_{Z2} to roll off the error amplifier gain at high frequency. This capacitor usually helps reduce LX2 pulse-width jitter, but if too large, it will also decrease the loop's phase margin.

Allegro recommends using this capacitor to set a pole at approximately 8× the loop's crossover frequency (f_{C2}), as shown in equation 27. If a non-standard capacitor value results, use the next higher available value.

$$C_{P2} \approx \frac{1}{2\pi \times R_{Z2} \times 8 \times f_{C2}} \quad (27)$$

Finally, look at the combined bode plot of both the power stage and the compensated error amplifier—the red curves shown in Figure 21. The bandwidth of this system (f_{C2}) is 43 kHz, the phase margin is 68°, and the gain margin is 28 dB.

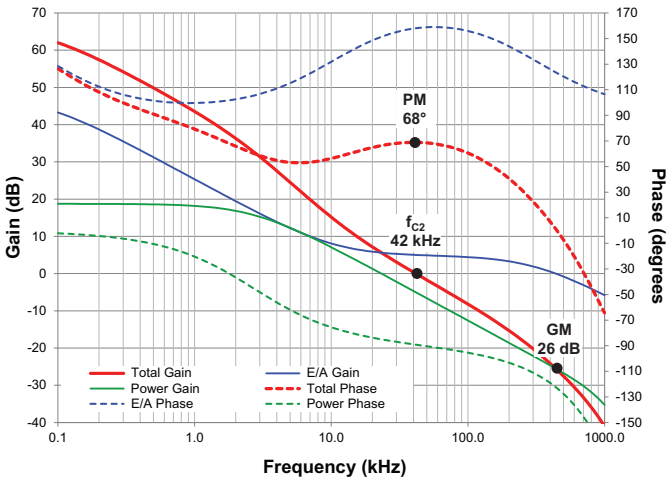


Figure 21: Bode Plot for the Synchronous Buck at 3.3 V_{OUT}

R_{Z2} = 10 kΩ, C_{Z2} = 1.5 nF, C_{P2} = 15 pF
L2 = 4.7 µH, $C_{OUT(ADJ)}$ = 2 × 10 µF / 16 V / 1206

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Linear Regulator (V5P)

The linear regulator only requires a single ceramic capacitor located near the A4413 to ensure stable operation. The range of acceptable values is shown in the Electrical Characteristics table. A 2.2 µF capacitor is a good starting point.

If the V5P output is routed throughout the PCB, it is recommended that a 0.1 µF/0603 ceramic capacitor be placed as close as possible to each load point for local filtering and high-frequency noise reduction.

Also, since the V5P output may be used to power remote circuitry, its load may include external wiring. The inductance of this wiring will cause LC-type ringing and negative spikes at the V5P pin if a "fast" short-to-ground occurs. A small Schottky diode must be placed close to the V5P pin to limit the negative voltages, as shown in the Applications Schematic. The MSS1P5 (or equivalent) is a good choice.

If the V5P regulator is not used, the output capacitance may be reduced to 0.1 µF to save cost.

Internal Bias (VCC)

The internal bias voltage should be decoupled at the VCC pin using a 1 µF, 10 to 16 V ceramic capacitor. It is not recommended to use this pin as a source for external ICs. However, for convenience, this pin may be used as a voltage source for the pull-up resistors to NPOR, POK5V, WD_{OUT}, and ENBATS, provided the maximum total current is limited to less than 2 mA (i.e. when all 4 diagnostic outputs are low).

Signal Pins (NPOR, POK5V, WD_{OUT}, ENBATS)

The A4413 has many signal level pins. The NPOR, POK5V, WD_{OUT}, and ENBATS are open-drain outputs and require external pull-up resistors. Allegro recommends sizing the external pull-up resistors so each pin will sink less than 0.25 to 1 mA when it is a logic low.

RC Snubber Calculations (R_{SNUBx}, C_{SNUBx})

Allegro strongly recommends including provisions for RC snubbers from LX1, LX2, and LXb to ground, as shown in the Applications Schematic. The LX1 and LX2 snubbers are required to meet automotive EMC requirements. The LXb snubber may be needed to reduce system noise when V_{VIN} is less than 7 V and the boost MOSFET (LG pin) starts switching. If the A4413 is used in buck-only mode, the LXb snubber is not necessary.

A simple method to calculate the RC snubber component values is presented here.

Use the tip-and-barrel technique on a scope probe to measure the frequency of the turn-on ringing of the LX node without an RC snubber. The scope's bandwidth must be set to its maximum, at least 200 MHz. The tip-and-barrel scope probe technique is shown in Figure 22. Typical LX ringing and frequency measurement are shown in Figure 23.

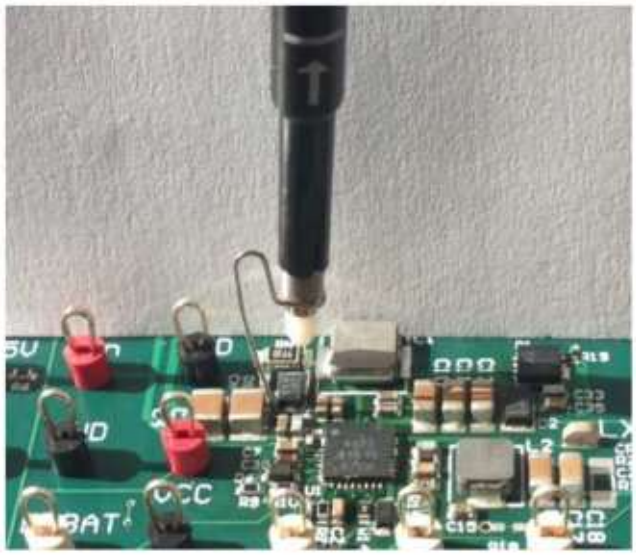


Figure 22: Measure LX ringing with tip-and-barrel

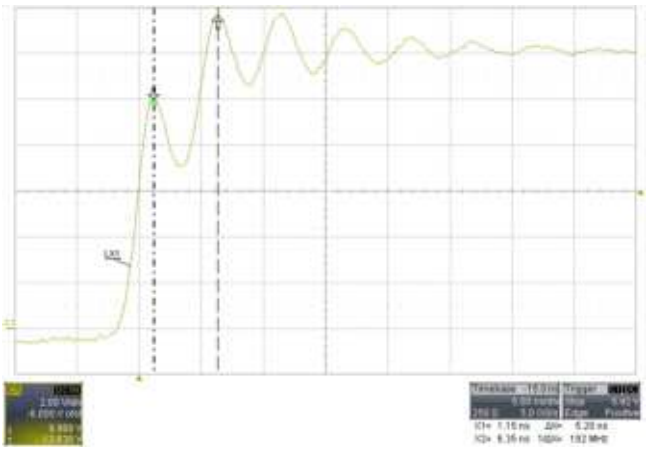


Figure 23: Typical LX ring frequency at turn-on without a snubber and V_{VIN} = 12 V: f_{RING} = 192 MHz

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After the ring frequency has been measured, the total capacitance at the LX node must be estimated. For the buck-boost pre-regulator, the LX1 pin (5 to 10 pF), the PCB (10 to 30 pF), and the asynchronous diode will all contribute to the capacitance. The asynchronous diode junction capacitance (~70 pF at 12 V_R) is usually shown in the datasheet, as shown in Figure 24.

For the synchronous buck, there is no external diode, so the total capacitance will consist of the LX2 pin, the internal synchronous MOSFET (10 to 20 pF), and the PCB.

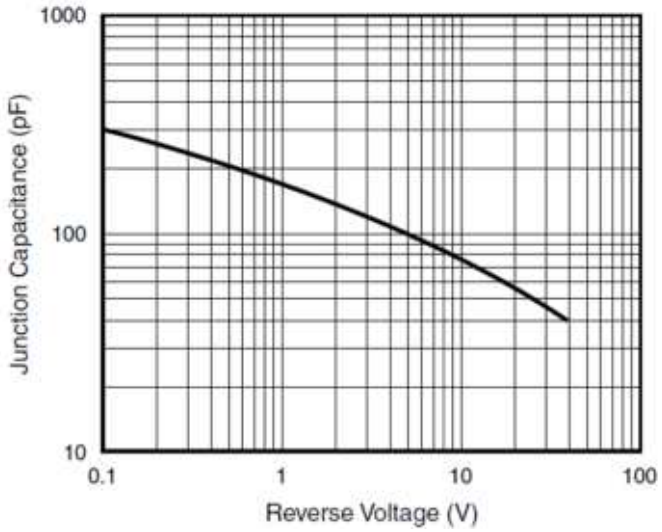


Figure 24: Typical diode junction capacitance

The total capacitance is calculated using equation 28,

$$C_{TOT} = C_{DIODE} + C_{LX1_PIN} + C_{PCB} \quad (28)$$

$$= 70\text{ pF} + 7.5\text{ pF} + 20\text{ pF} = 97.5\text{ pF}$$

Knowing the ring frequency and the total capacitance, the inductive component of the ringing can be calculated using equation 29.

$$L_{RING} = \frac{1}{4 \times \pi^2 \times f_{RING}^2 \times C_{TOT}} \quad (29)$$

$$L_{RING} = \frac{1}{4 \times \pi^2 \times 192^2\ MHz \times 97.5\ pF}$$

$$= 7.05\ nH$$

The snubber resistor is calculated using equation 30.

$$R_{SNUB} = \sqrt{\frac{L_{RING}}{C_{TOT}}} \quad (30)$$

$$R_{SNUB} = \sqrt{\frac{7.05\text{ nH}}{97.5\text{ pF}}} = 8.66\ \Omega \text{ (standard value)}$$

Finally, the snubber capacitor can be calculated using equation 31. If equation 31 results in a non-standard value, use the next higher standard value.

$$C_{SNUB} = \frac{1}{2.5 \times f_{RING} \times R_{SNUB}} \quad (31)$$

$$C_{SNUB} = \frac{1}{2.5 \times 192\text{ MHz} \times 8.66\ \Omega}$$

$$= 270\text{ pF (standard)}$$

It is very important to calculate the power dissipated by the resistor at the maximum steady-state (DC) input operating voltage, using equation 32. Once the maximum power dissipation is known, an adequate component considering power derating at the maximum ambient temperature can be chosen. In this example, $V_{VIN(MAX,DC)}$ = 18 V and f_{OSC} = 2.2 MHz is used.

$$P_{SNUB} = 0.5 \times C_{SNUB} \times V_{VIN}^2 \times f_{SW} \quad (32)$$

$$P_{SNUB} = 0.5 \times 270\text{ pF} \times 18^2\text{ V} \times 2.2\text{ MHz}$$

$$= 96\text{ mW}$$

To support 100 mW at high ambient temperature, a 1206 size resistor would be needed. A 1206 size resistor can dissipate 250 mW up to 100°C and 100 mW (40%) up to almost 135°C, as shown in Figure 25.

Figure 26 shows the LX waveform with the RC snubber components, 8.66 Ω + 270 pF—the high frequency ringing has been eliminated.

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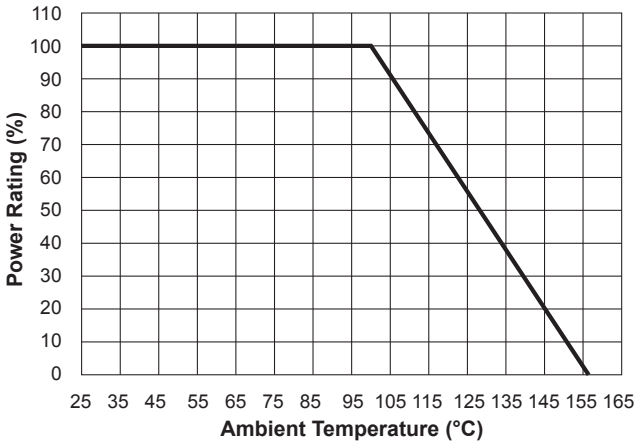


Figure 25: Resistor power derating versus ambient temperature

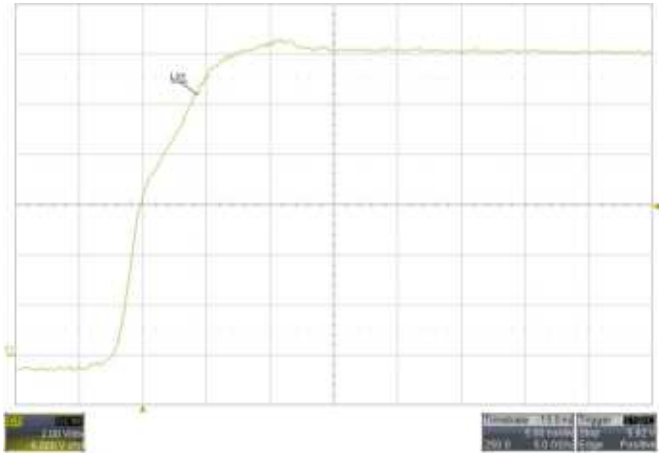


Figure 26: LX waveform including an RC snubber consisting of 8.66 Ω + 270 pF

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PCB LAYOUT RECOMMENDATIONS

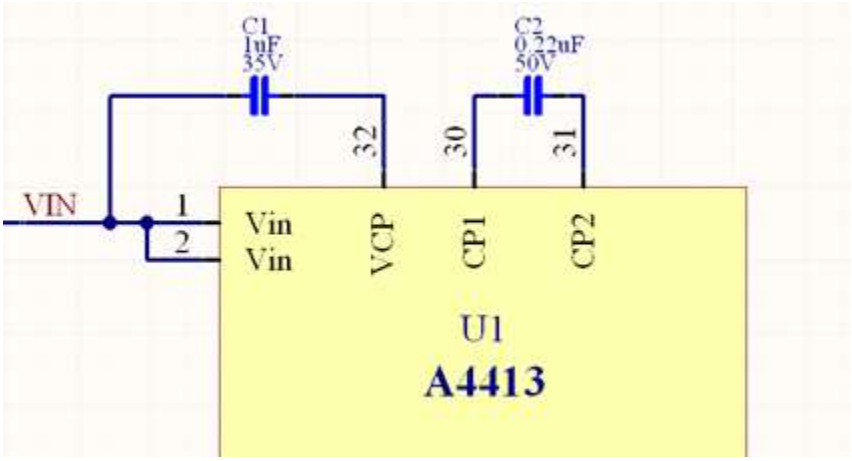


Figure 27a: Charge Pump capacitor C1 and C2. Place these components near pins 30, 31, and 32.

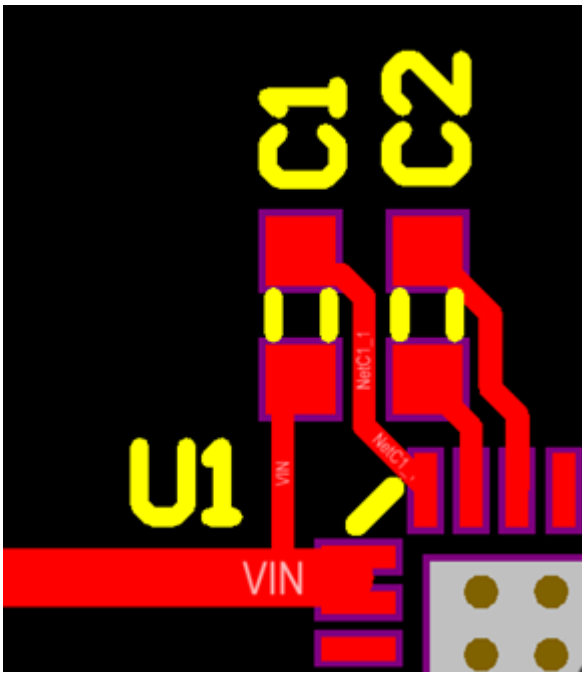


Figure 27b: Recommended placement and connection of the two charge pump capacitors.

1. Start the layout by placing these components near pins 30, 31, and 32 as shown here.

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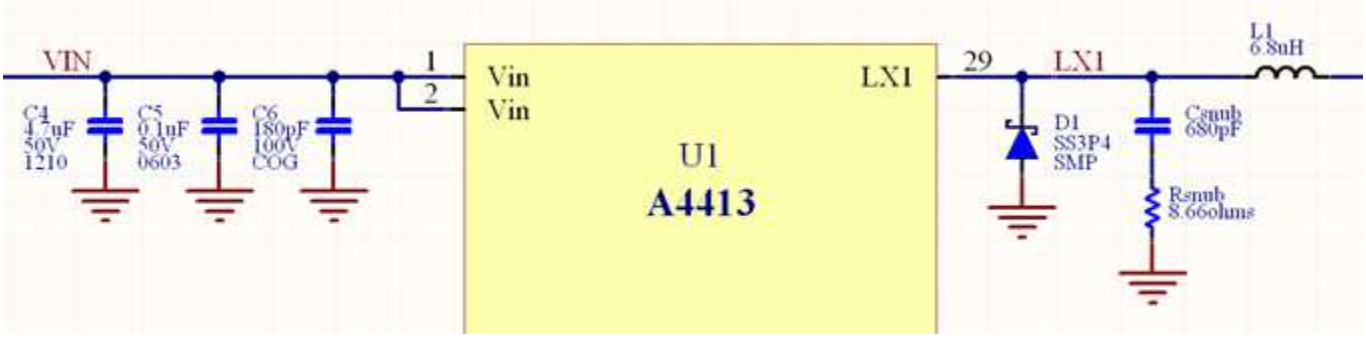


Figure 28a: The most critical power component connections for the pre-regulator. Place these components onto the PCB layout after the charge pump capacitors.

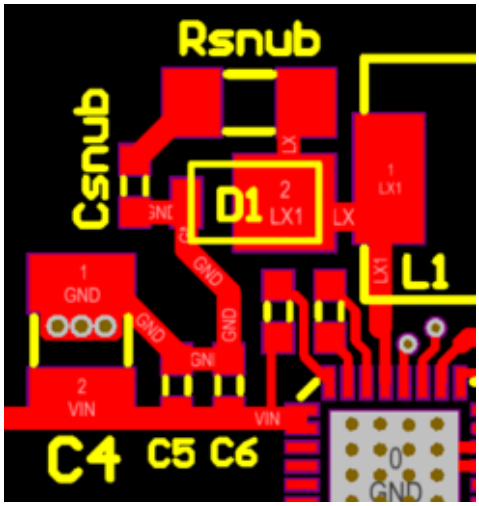


Figure 28b: Recommended placement and connection of the most critical power components.

1. All these components must be on the same layer as the A4413 (U1).
2. Routing between these components must not be interrupted by other traces.
3. Input capacitors (C4, C5, and C6) are located very close to the VIN pins.
4. Minimize the total loop area from C4/C5/C6 through U1 + L1 + D1.
5. The three vias to ground under C4 are placed so they only conduct DC current.
6. The switch node trace (LX1) is very short and just wide enough to carry about 3 A.
7. High-frequency currents passing through D1 are directly routed to C6, C5, and C4.
8. The snubber components connect directly from the LX1 node to ground.

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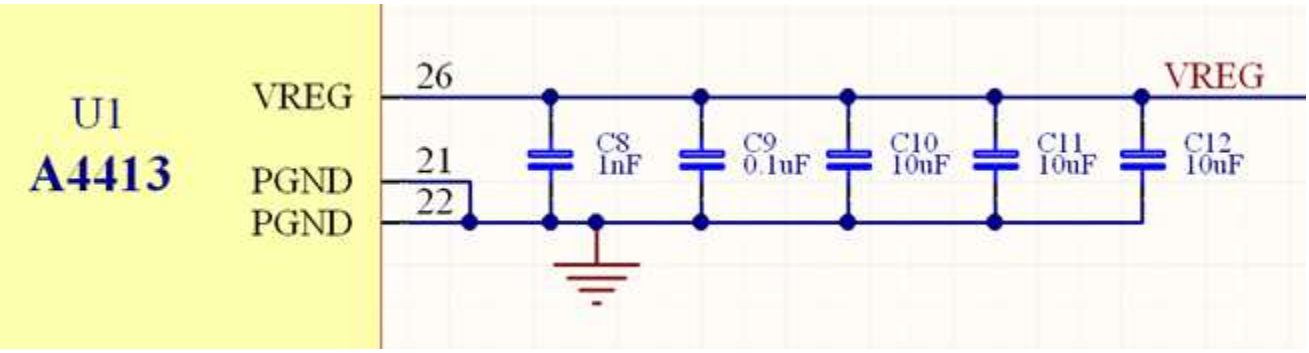


Figure 29a: VREG capacitors (C8 – C12) and PGND connections.
The VREG capacitors are the input bypass capacitors for the synchronous buck.
Place these capacitors so the loop from the VREG to PGND is short and uninterrupted.

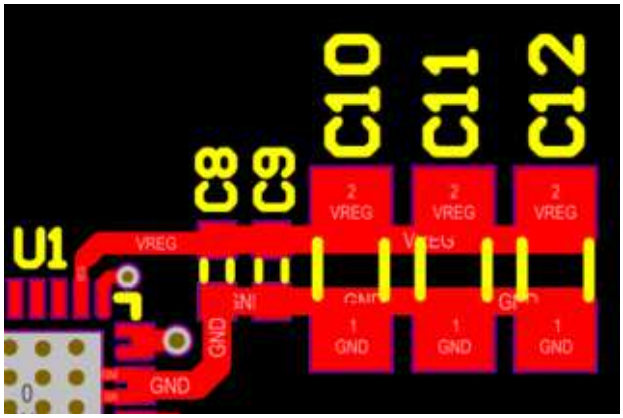


Figure 29b: Recommended placement of the VREG capacitors and their PGND connection.

1. Place these components on the same layer as the A4413 (U1).
2. Minimize the loop from capacitors C8 – C12 to the VREG pin and PGND pin.
3. The ground connection from the capacitors to the PGND pins is uninterrupted.
4. Connect the two PGND pins to the thermal pad (i.e. ground) under the A4413.
5. Note, the LX2 trace (pins 23 and 24) uses a via to avoid interrupting the PGND trace.

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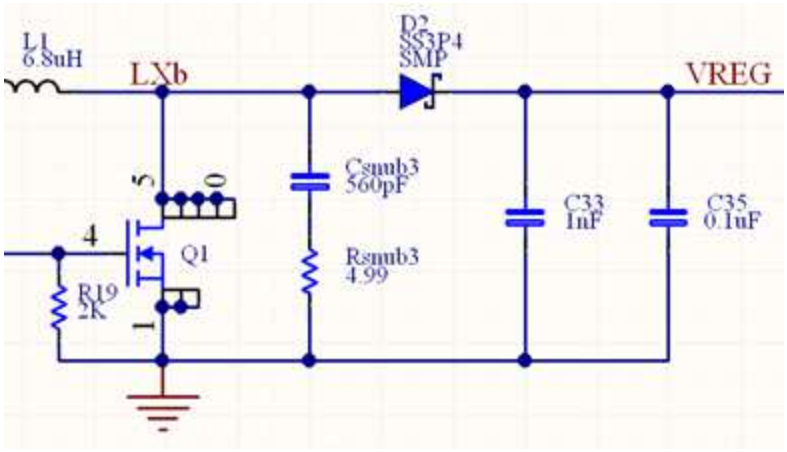


Figure 30a: Boost MOSFET and diode (Q1, D2), local bypass capacitors (C33, C35), and snubber.

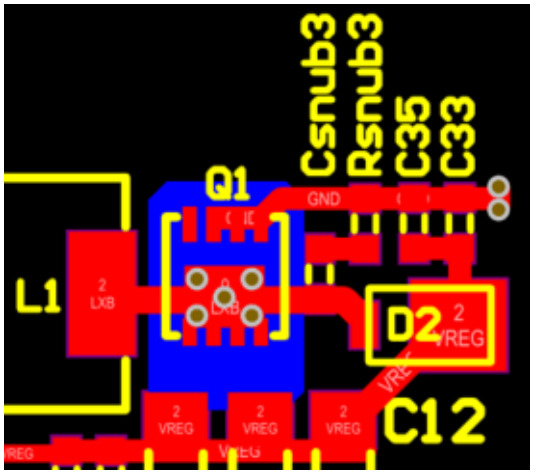


Figure 30b: Recommended placement and routing of the boost MOSFET and diode (Q1, D2), local bypass capacitors (C33, C35), and snubber components (Rsnub3, Csnub3)

1. Minimize the loop from C33/C35 to Q1 to D2.
2. Place a connection to the ground plane outside the hot loop.
3. Include a thermal area on the bottom of the PCB as thermal relief for Q1.

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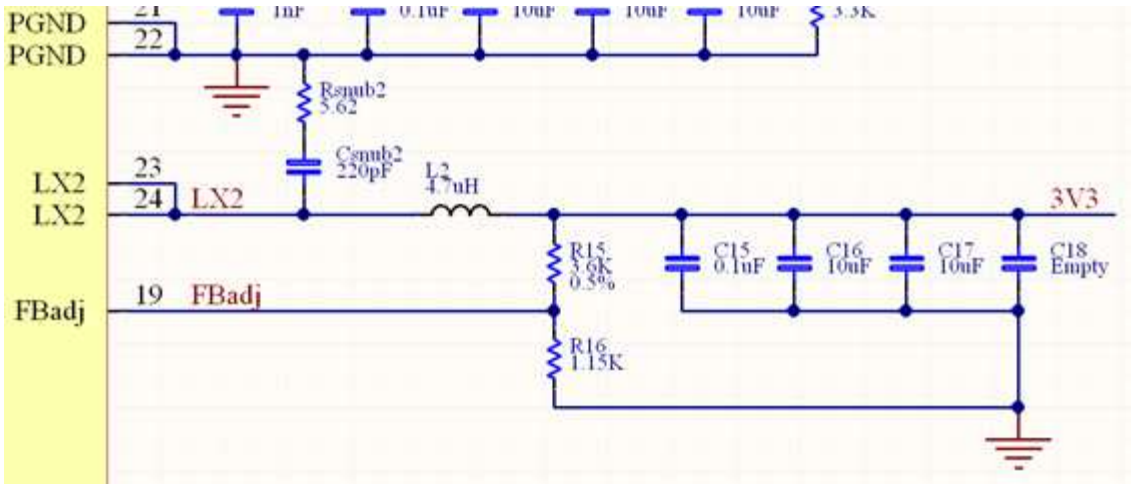


Figure 31a: Synchronous buck output capacitors (C15 – C18), snubber (Rsnub2, Csnubs), and feedback resistor divider (R15, R16).

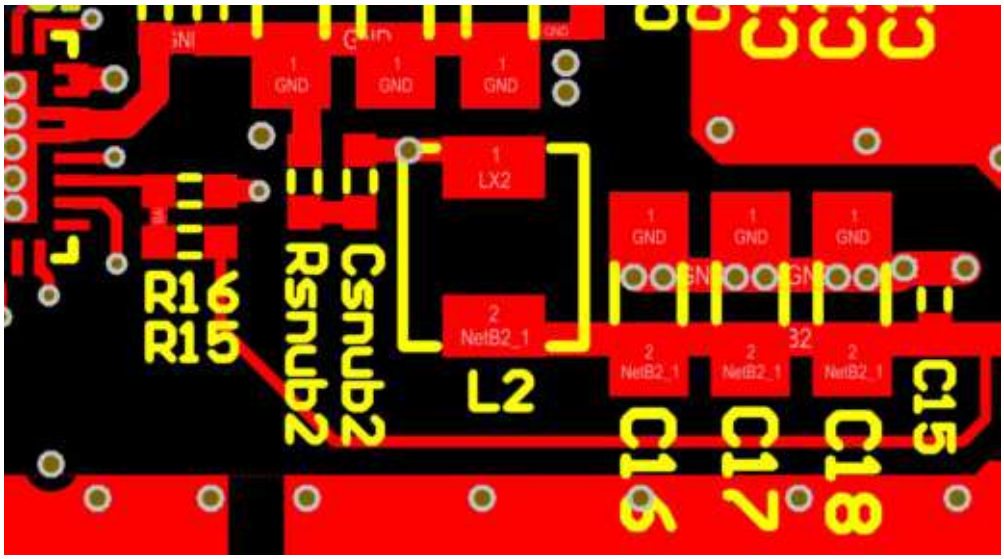


Figure 31b: Recommended placement and routing of the synchronous buck inductor (L2), snubber (Rsnub2, Csnub2), output capacitors (C15 – C18), and feedback resistor divider (R15, R16).

1. Minimize the length and width of the LX2 trace. The width should accommodate 2.4 A_{MAX}.
2. The LX2 trace is on the bottom layer so the VREG capacitors can connect directly to PGND.
3. The output capacitors are grounded at the output of the adjustable buck.
4. The snubber is on the same layer as the inductor and is grounded at the VREG capacitors.
5. The feedback resistor divider (R15, R16) must be located near the FB_{ADJ} pin.
6. The feedback divider is differentially routed to sense the output voltage at the load.

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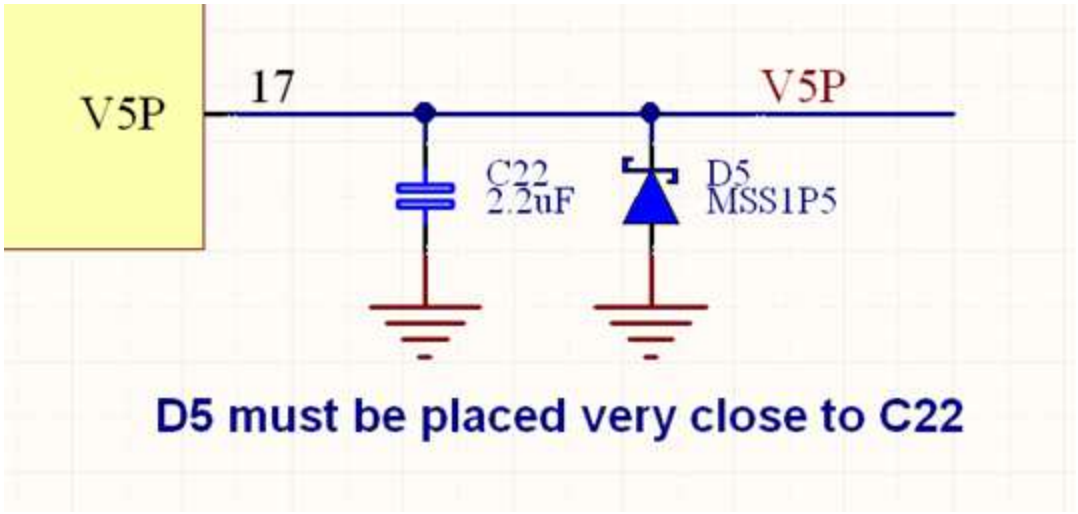


Figure 32a: LDO (V5P) output capacitor and negative clamp diode (C22, D5).

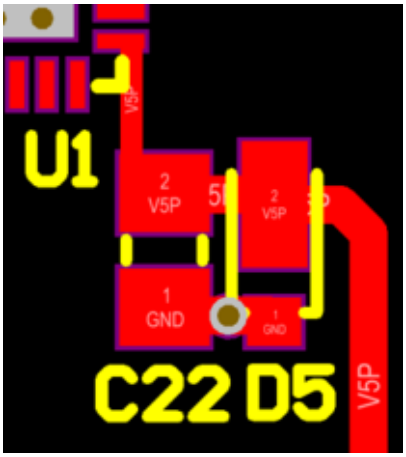


Figure 32b: Recommended placement and routing of the LDO (V5P), output capacitor (C22), and negative clamp diode (D5).

1. Place the output capacitor and negative clamp diode close to the V5P output pin.
2. Connect these two components to the ground plane near the A4413.

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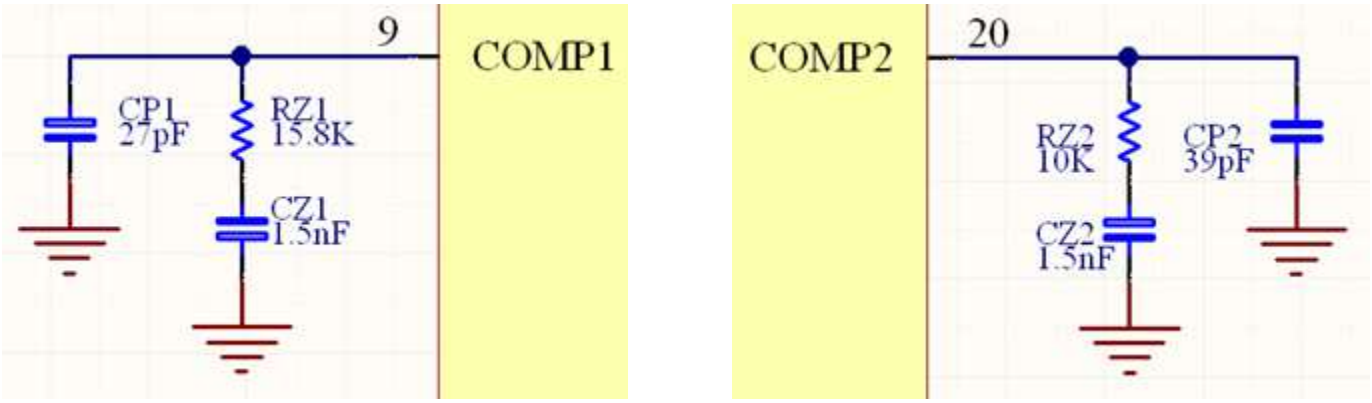


Figure 33a: The COMP1 (RZ1, CZ1, CP1) and COMP2 (RZ2, CZ2, CP2) components.

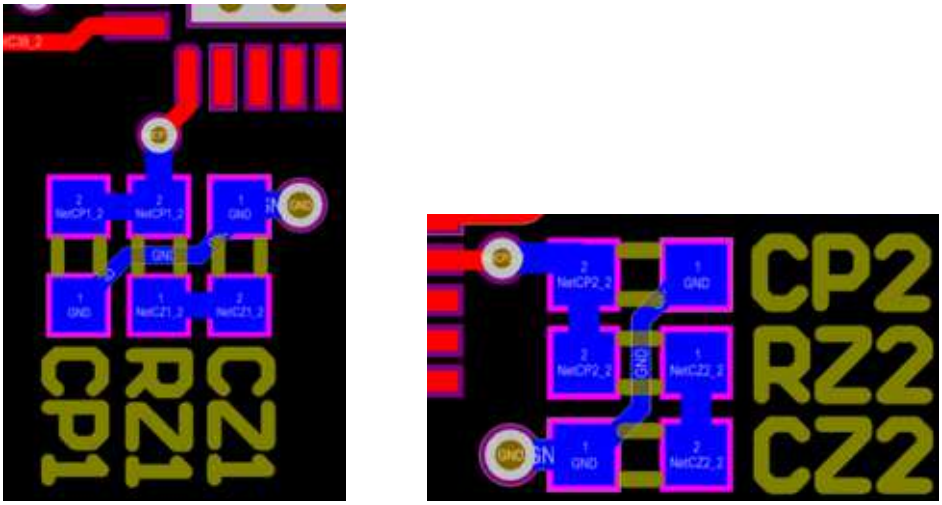


Figure 33b: Recommended placement and routing of COMP1 and COMP2 components.

1. These components can by placed on the bottom of the PCB, near pins 9 and 20.
2. Place a via very close to pins 9 and 20.
3. Keep noisey traces, like LX1 and LX2, as far as possible from these components.

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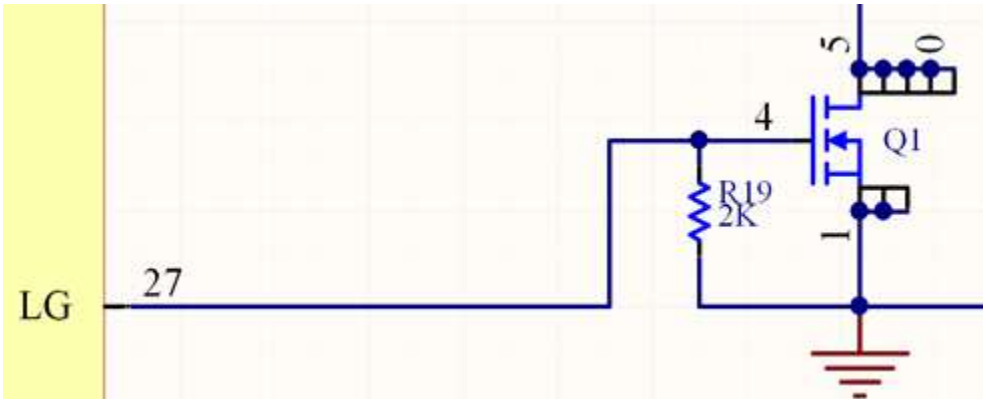


Figure 34a: The gate drive from LG (pin 27) to the boost MOSFET.

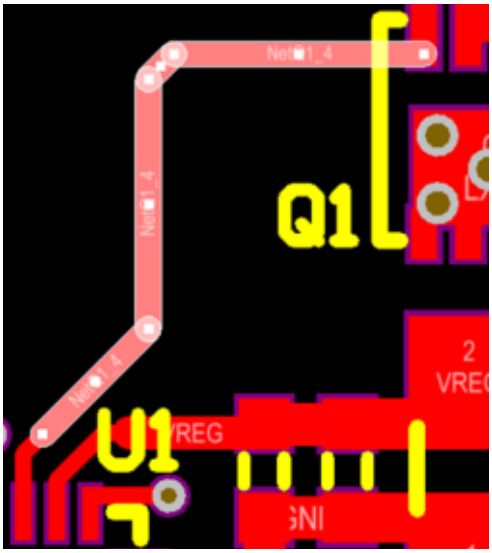


Figure 34b: Recommended routing of the gate driver to the boost MOSFET.

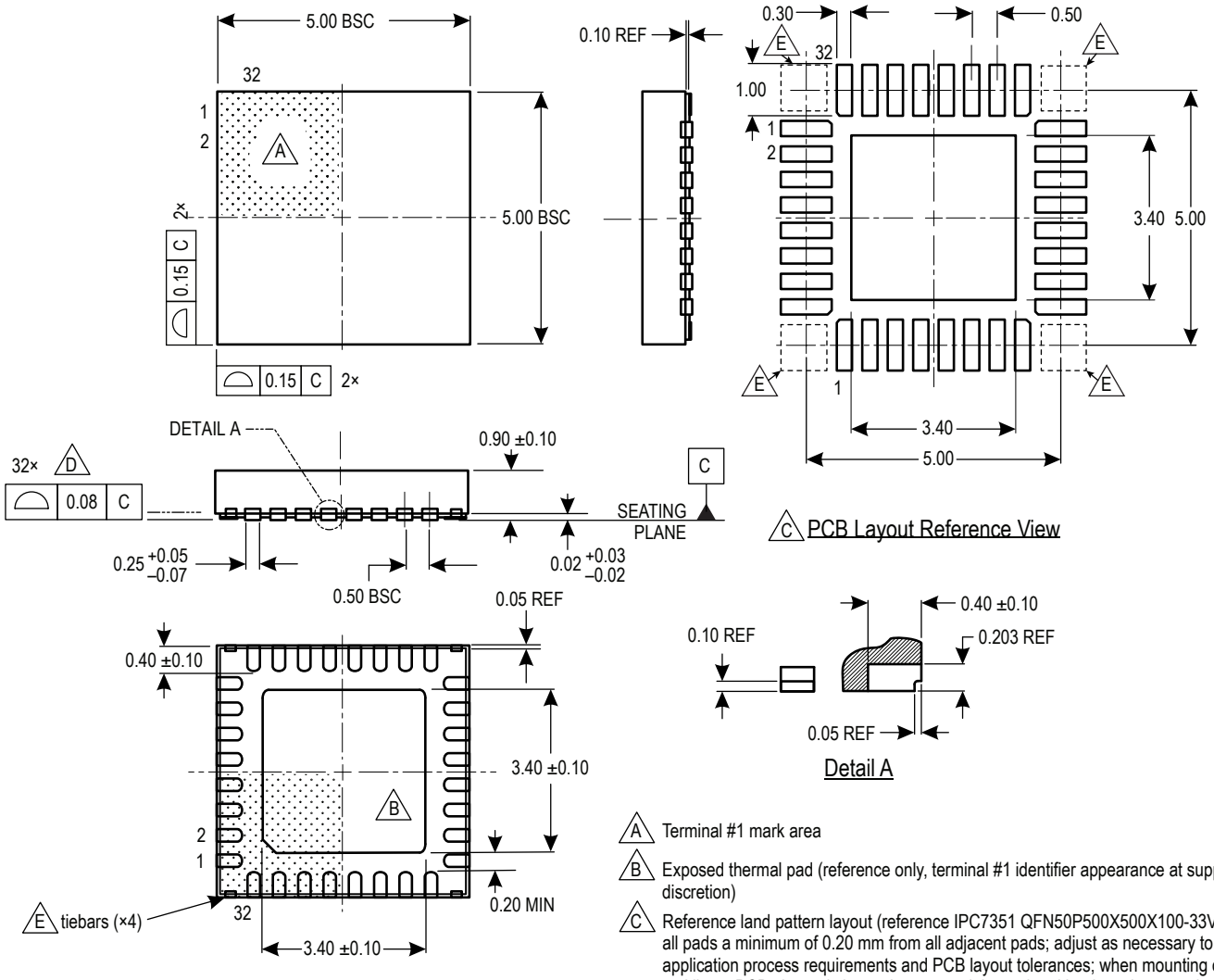
1. It is best to keep the gate drive trace (LG) short and on the same layer as U1 and Q1 (i.e. no vias).
2. Here, the trace routes on the top layer and makes a short vertical run under L1.
3. The return path for the gate driver is layer #2, which is a ground plane.

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PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use

(Reference Allegro DWG-0000378, Rev. 3 and JEDEC MO-220VHHD-5)
Dimensions in millimeters – NOT TO SCALE
Exact case and lead configuration at supplier discretion within limits shown



A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 QFN50P500X500X100-33V6M); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed thermal pad and terminals

E Tiebars (×4) are electrically connected to thermal pad. Avoid active traces in this area to avoid shorts. Ground plane in this area is acceptable when appropriate.

Figure 35: Package ET, 32-Pin QFN with Exposed Pad and Wettable Flank

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Revision History

Number	Date	Description
–	June 29, 2016	Initial release
1	December 20, 2019	Minor editorial updates
2	December 13, 2021	Updated package drawing (page 47)

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