X60003

Precision SOT-23 FGA™ Voltage References

FN8137
Rev 5.00
September 1, 2015

The X60003 FGA™ voltage references is a very high precision analog voltage reference fabricated in Intersil's proprietary Floating Gate Analog technology, which achieves superior levels of performance when compared to conventional band gap, buried zener, or X_{FET}™ technologies.

FGA™ voltage references feature very high initial accuracy, very low temperature coefficient, excellent long term stability, low noise and excellent line and load regulation, at the lowest power consumption currently available. These voltage references enable advanced applications for precision industrial and portable systems operating at significantly higher accuracy and lower power levels than can be achieved with conventional technologies.

Applications

- High resolution A/Ds and D/As
- Digital meters
- Calibration systems
- V-F converters
- Precision current sources
- Precision regulators
- Precision oscillators
- Smart sensors
- Strain gage bridges
- Threshold detectors
- Battery management systems
- Servo systems

Features

- Reference output voltage 4.096V, 5.000V
- Initial accuracy . . . . . ±1.0mV (B grade)
- Ultra low power supply current 500nA
- Low temperature coefficient (B grade) . . . . . 10ppm/°C
- 10mA source and sink current capability
- Very low dropout voltage . . . . . 100mV at No Load
- Input voltage range
  - X60003-41 . . . . . 4.5V to 9.0V
  - X60003-50 . . . . . 5.1V to 9.0V
- 5kV ESD (human body model)
- Standard package . . . . . 3 Ld SOT-23
- Temp range . . . . . -40°C to +85°C

Related Literature

- See AN1494, "Reflow and PC Board Assembly Effects on Intersil FGA References"
- See AN1533, "X-Ray Effects on Intersil FGA References"

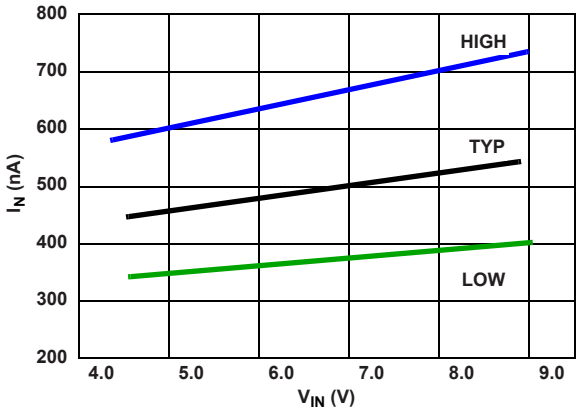


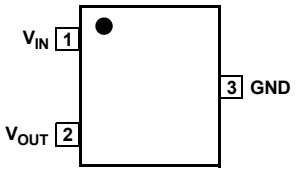
FIGURE 1. I_{IN} vs V_{IN} (3 UNITS)

Available Options

PART NUMBER	V_{OUT} OPTION (V)	INITIAL ACCURACY (mV)	TEMPCO. (ppm/°C)
X60003BIG3Z-41T1	4.096	±1.0	10
X60003CIG3Z-41T1	4.096	±2.5	20
X60003DIG3Z-41T1 (No longer available or supported)	4.096	±5.0	20
X60003BIG3Z-50T1	5.000	±1.0	10
X60003CIG3Z-50T1	5.000	±2.5	20
X60003DIG3Z-50T1	5.000	±5.0	20

Pin Configuration

X60003
(3 LD SOT-23)
TOP VIEW



Pin Descriptions

PIN NUMBER	PIN NAME	DESCRIPTION
1	V_{IN}	Power Supply Input Connection
2	V_{OUT}	Voltage Reference Output Connection
3	GND	Ground Connection

Typical Application Circuit

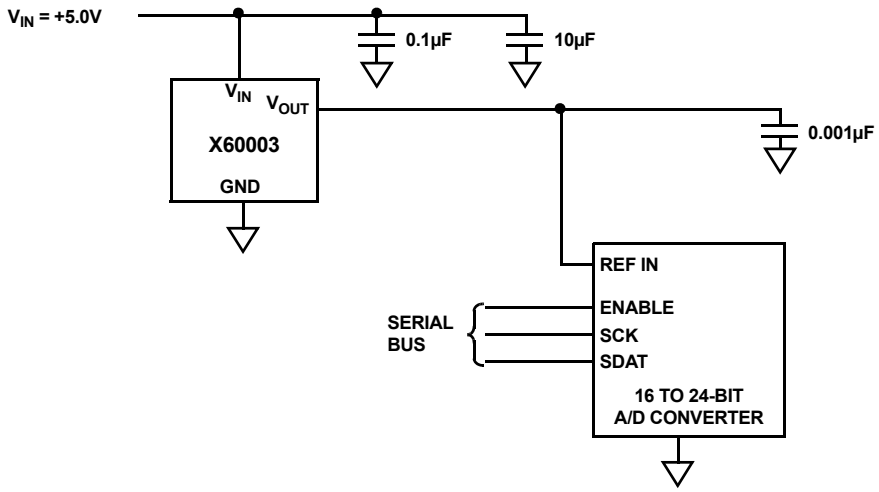


FIGURE 2. TYPICAL APPLICATION PRECISION 16 TO 24-BIT A/D CONVERTER

Ordering Information

PART NUMBER (Notes 2, 3)	PART MARKING (Note 4)	V_{OUT} (V)	GRADE (°C)	TEMP. RANGE (°C)	PACKAGE (RoHS Compliant)	PKG. DWG #
X60003BIG3Z-41T1 (Note 1)	APF	4.096	±1.0mV, 10ppm	-40 to +85	3 Ld SOT-23	P3.064
X60003CIG3Z-41T1 (Note 1)	APH		±2.5mV, 20ppm	-40 to +85	3 Ld SOT-23	P3.064
X60003DIG3Z-41 **(No longer available, recommended replacement: X60003BIG3Z-41T1)**	APJ		±5.0mV, 20ppm	-40 to +85	3 Ld SOT-23	P3.064
X60003DIG3Z-41T1 (Note 1) **(No longer available, recommended replacement: X60003BIG3Z-41T1)**	APJ		±5.0mV, 20ppm	-40 to +85	3 Ld SOT-23	P3.064
X60003BIG3Z-50T1 (Note 1)	APG	5.00	±1.0mV, 10ppm	-40 to +85	3 Ld SOT-23	P3.064
X60003CIG3Z-50T1 (Note 1)	API		±2.5mV, 20ppm	-40 to +85	3 Ld SOT-23	P3.064
X60003DIG3Z-50T1 (Note 1)	APK		±5.0mV, 20ppm	-40 to +85	3 Ld SOT-23	P3.064
X60003-EVALZ	Evaluation Board					

NOTES:

1. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for X60003. For more information on MSL please see techbrief TB363.
4. The part marking is located on the bottom of the part

Absolute Voltage Ratings

Max Voltage Applied
- V_{IN} to GND . . . . . -0.5V to +10V
- V_{OUT} to GND (10s) . . . . . -0.5V to +5.1V

ESD Ratings
- Human Body Model (Tested to JESD22-A114) 5kV
- Machine Model (Tested to JESD22-A115) 500V

Latch Up (Tested per JESD-78B; Class 2, Level A) 100mA

Environmental Operating Conditions

X-Ray Exposure (Note 5) 10mRem

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
3 Lead SOT-23 (Notes 6, 7)	275	110

Maximum Junction Temperature . . . . . +107°C
Storage Temperature Range . . . . . -65°C to +125°C
Pb-Free Reflow Profile . . . . . see TB493

Recommended Operating Conditions

Temperature Range (Industrial) . . . . . -40°C to +85°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

NOTES:

5. Measured with no filtering, distance of 10" from source, intensity set to 55kV and 70mA current, 30s duration. Other exposure levels should be analyzed for Output Voltage drift effects. See "Applications Information" on page 12.
6. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
7. For θ_{JC}, the "case temp" location is taken at the package top center.
8. Post-reflow drift for the X60003 devices will range from 100µV to 1.0mV based on experimental results with devices on FR4 double sided boards. The design engineer must take this into account when considering the reference voltage after assembly.

Electrical Specifications Operating Conditions: I_{OUT} = 0mA, C_{OUT} = 0.001µF, T_A = -40 to +85°C. Boldface limits apply over the operating temperature range, -40°C to +85°C.

SYMBOL	PARAMETER	CONDITIONS	MIN (Note 12)	TYP	MAX (Note 12)	UNITS
V_{OA}	V_{OUT} Accuracy @ T_A = +25°C	X60003B	**-1.0**		**+1.0**	mV
		X60003C	**-2.5**		**+2.5**	mV
		X60003D	**-5.0**		**+5.0**	mV
I_{IN}	Supply Current			500	**900**	nA
TC V_{OUT}	Output Voltage Temperature Coefficient (Note 9)	X60003B			**10**	ppm/°C
		X60003C			**20**	ppm/°C
		X60003D			**20**	ppm/°C
V_N	Output Voltage Noise	0.1Hz to 10Hz		30		μV_{P-P}
I_{SC}	Short Circuit Current	T_A = +25°C		50	80	mA

Electrical Specifications (X60003-41) V_{IN} = 5.0, T_A = -40°C to +85°C, unless otherwise specified. Boldface limits apply over the operating temperature range, -40°C to +85°C.

SYMBOL	PARAMETER	CONDITIONS	MIN (Note 12)	TYP	MAX (Note 12)	UNITS
V_{IN}	Input Voltage Range		**4.5**		**9.0**	V
V_{OUT}	Output Voltage			4.096		V
$\Delta V_{OUT}/\Delta V_{IN}$	Line Regulation	+4.5V ≤ V_{IN} ≤ +8.0V			**150**	µV/V
$\Delta V_{OUT}/\Delta I_{OUT}$	Load Regulation	Sourcing: 0mA ≤ I_{SOURCE} ≤ 10mA		10	**50**	µV/mA
		Sinking: -10mA ≤ I_{SINK} ≤ 0mA		20	**100**	µV/mA
$\Delta V_{OUT}/\Delta T_A$	Thermal Hysteresis (Note 10)	ΔT = -40°C to +85°C		150		ppm
$\Delta V_{OUT}/\Delta t$	Long Term Stability (Note 11)	T_A = +25°C		50		ppm

Electrical Specifications (X60003-50)

V_{IN} = 6.5V, T_A = -40°C to +85°C, unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +85°C.**

SYMBOL	PARAMETER	CONDITIONS	MIN (Note 12)	TYP	MAX (Note 12)	UNITS
V_{IN}	Input Voltage Range		**5.1**		**9.0**	V
V_{OUT}	Output Voltage			5.000		V
$\Delta V_{OUT}/\Delta V_{IN}$	Line Regulation	+5.5V ≤ V_{IN} ≤ +8.0V			**150**	µV/V
$\Delta V_{OUT}/\Delta I_{OUT}$	Load Regulation	Sourcing: 0mA≤ I_{SOURCE} ≤ 10mA		10	**50**	µV/mA
		Sinking: -10mA ≤ I_{SINK} ≤ 0mA		20	**100**	µV/mA
V_{DO}	Dropout Voltage	I_{OUT} = 5mA, ΔV_{OUT} = -0.01%		150	**300**	mV
$\Delta V_{OUT}/\Delta T_A$	Thermal Hysteresis (Note 10)	ΔT = -40°C to +85°C		100		ppm
$\Delta V_{OUT}/\Delta t$	Long Term Stability (Note 11)	T_A = +25°C		45		ppm

NOTES:

9. Over the specified temperature range. Temperature coefficient is measured by the box method whereby the change in V_{OUT} is divided by the temperature range; in this case, -40°C to +85°C = +125°C.
10. Thermal Hysteresis is the change of V_{OUT} measured at T_A = +25°C after temperature cycling over a specified range, ΔT_A. V_{OUT} is read initially at T_A = +25°C for the device under test. The device is temperature cycled and a second V_{OUT} measurement is taken at +25°C. The difference between the initial V_{OUT} reading and the second V_{OUT} reading is then expressed in ppm. For ΔT_A = +125°C, the device under test is cycled from +25°C to +85°C to -40°C to +85°C.
11. Long term drift is logarithmic in nature and diminishes over time. Drift after the first 1000 hours will be approximately 10ppm/sqrt(1kHrs).
12. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Typical Performance Curves (X60003-41)

VIN = 5.0V, IOUT = 0mA, TA = +25°C unless otherwise specified.

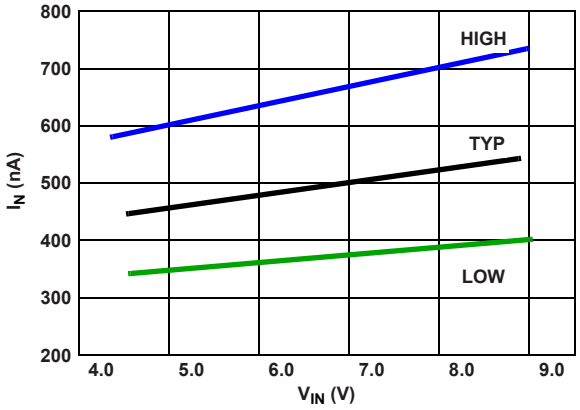


FIGURE 3. I_{IN} vs V_{IN} (3 UNITS)

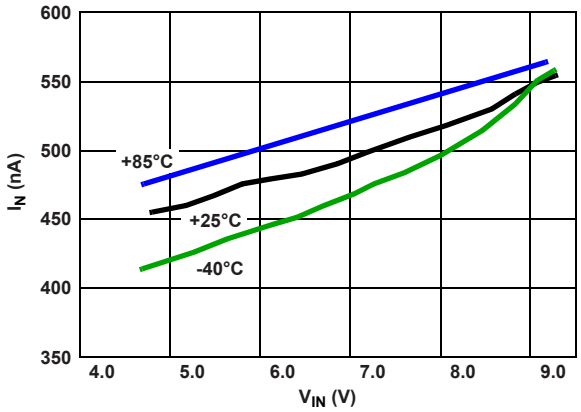


FIGURE 4. I_{IN} vs V_{IN}

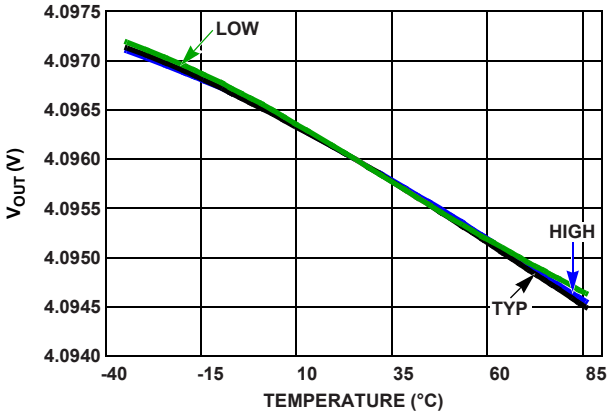


FIGURE 5. VOUT vs TEMPERATURE NORMALIZED TO +25°C (3 UNITS)

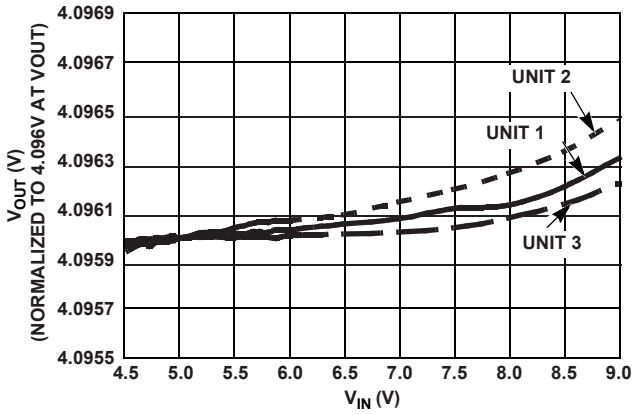


FIGURE 6. LINE REGULATION (3 UNITS)

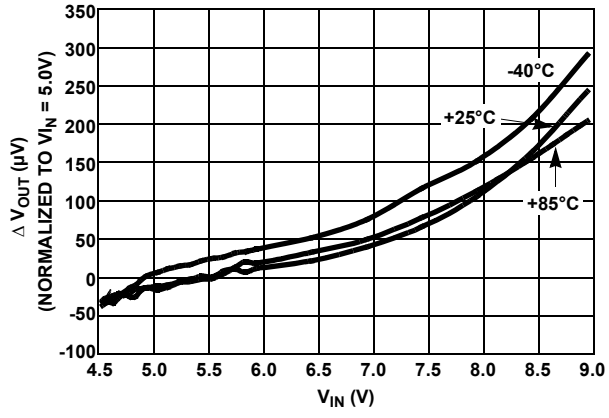


FIGURE 7. LINE REGULATION OVER-TEMPERATURE

Typical Performance Curves (X60003-41)

VIN = 5.0V, IOUT = 0mA, TA = +25°C unless otherwise specified. **(Continued)**

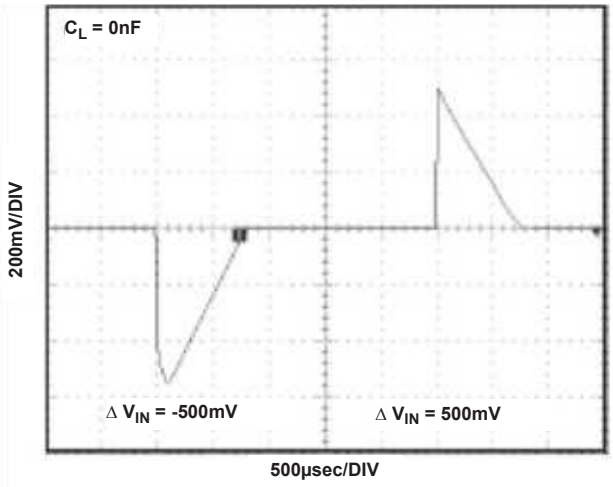


FIGURE 8. LINE TRANSIENT RESPONSE, NO CAPACITIVE LOAD

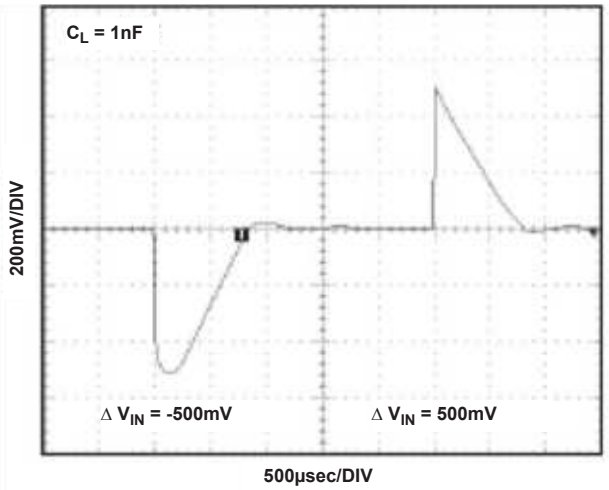


FIGURE 9. LINE TRANSIENT RESPONSE, 0.001µF LOAD CAPACITANCE

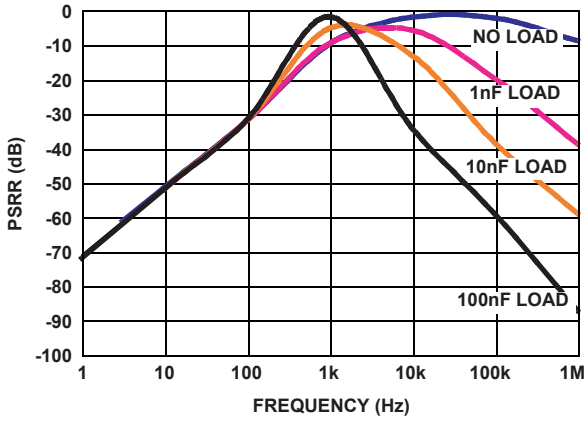


FIGURE 10. PSRR vs CAP LOAD

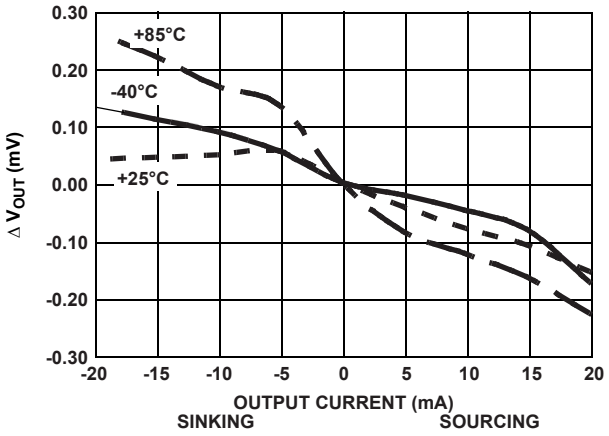


FIGURE 11. LOAD REGULATION

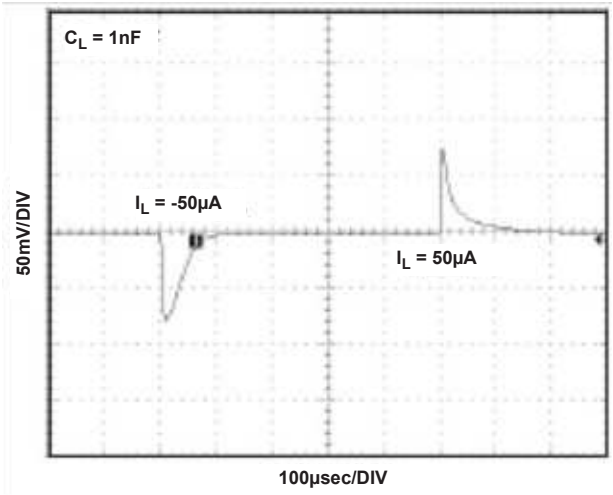


FIGURE 12. LOAD TRANSIENT RESPONSE

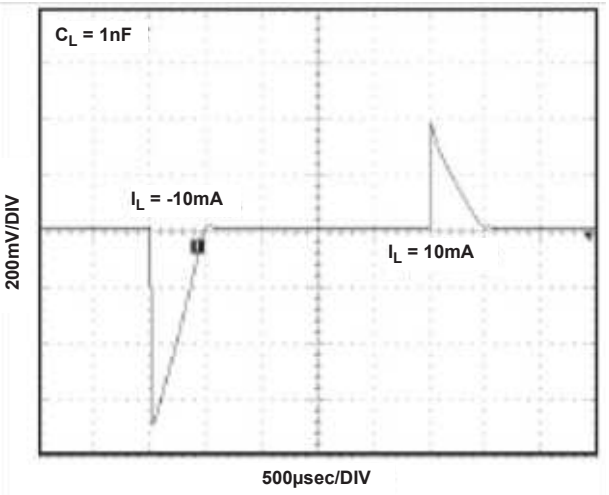


FIGURE 13. LOAD TRANSIENT RESPONSE

Typical Performance Curves (X60003-41)

VIN = 5.0V, IOUT = 0mA, TA = +25°C unless otherwise specified. **(Continued)**

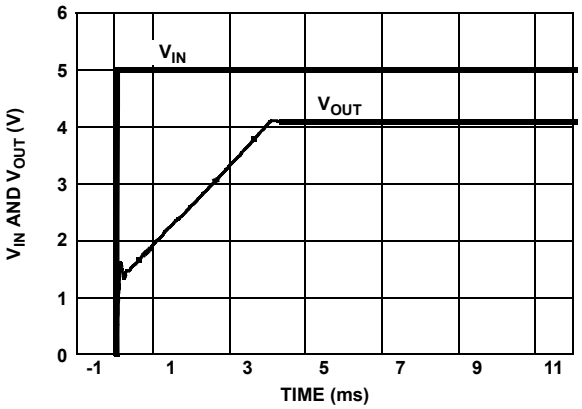


FIGURE 14. TURN-ON TIME (+25°C)

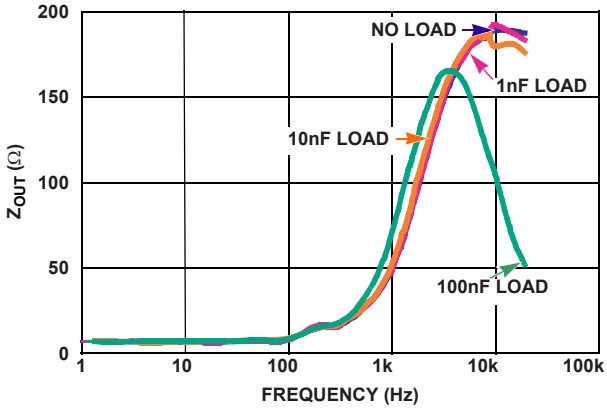


FIGURE 15. Z_{OUT} vs FREQUENCY

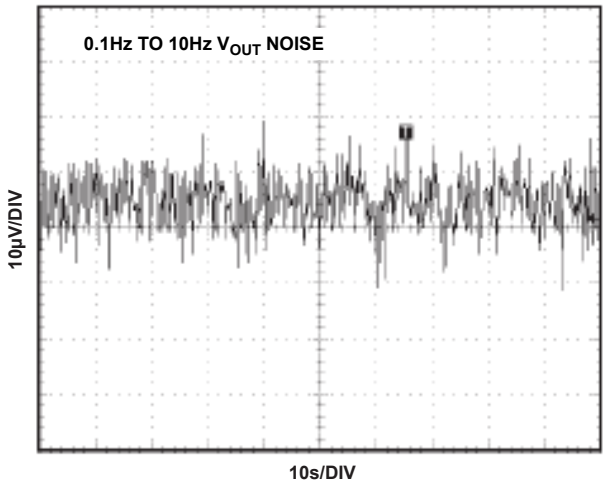


FIGURE 16. BAND PASS FILTER WITH ZERO AT 0.1Hz AND 2 POLES AT 10Hz

Typical Performance Curves (X60003-50)

(V_{IN} = 6.5V, I_{OUT} = 0mA, T_A = +25°C unless otherwise specified)

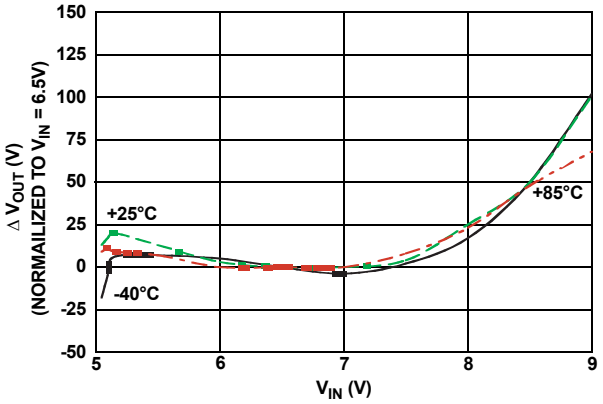


FIGURE 17. LINE REGULATION

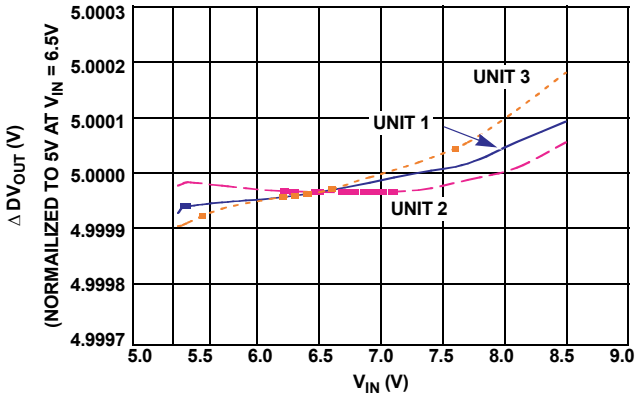


FIGURE 18. LINE REGULATION (3 UNITS)

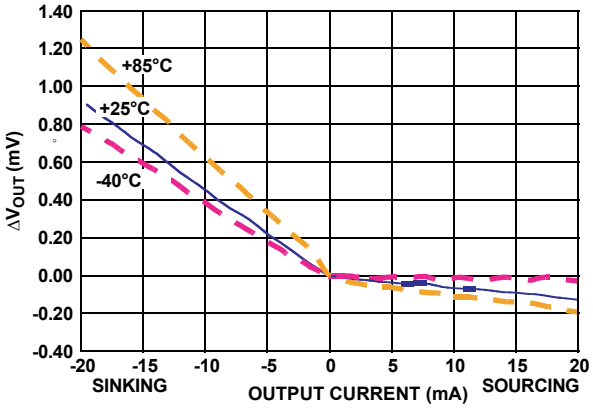


FIGURE 19. LOAD REGULATION OVER TEMPERATURE

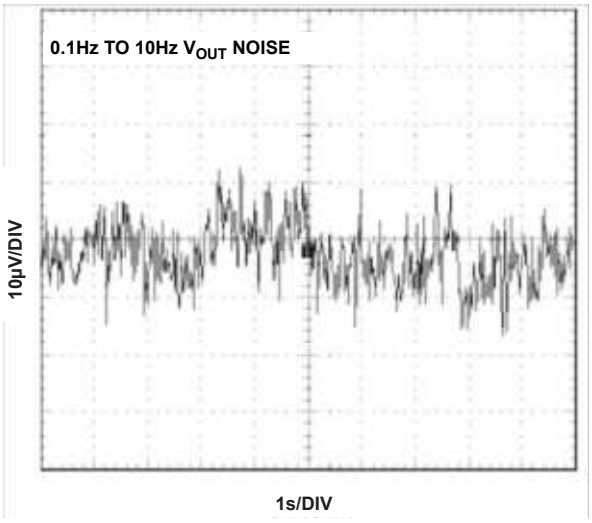


FIGURE 20. BAND PASS FILTER WITH ZERO AT 0.1Hz AND 2 POLES AT 10Hz

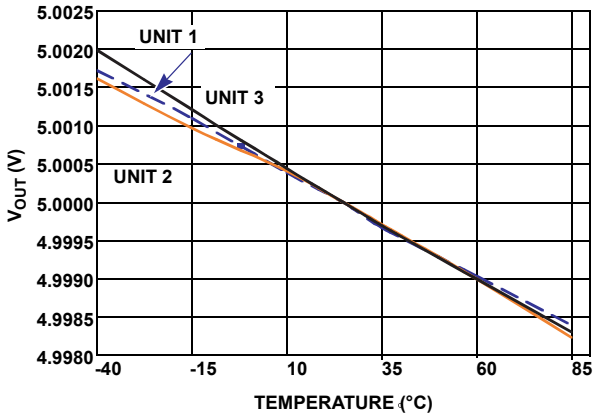


FIGURE 21. V_{OUT} vs TEMPERATURE (3 UNITS)

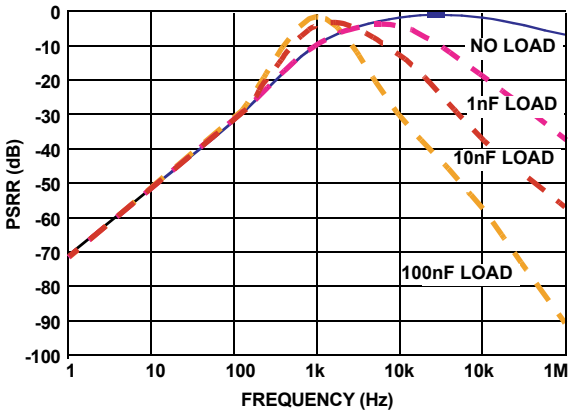


FIGURE 22. PSSR vs CAP LOAD

Typical Performance Curves (X60003-50)

(V_{IN} = 6.5V, I_{OUT} = 0mA, T_A = +25°C unless otherwise specified) **(Continued)**

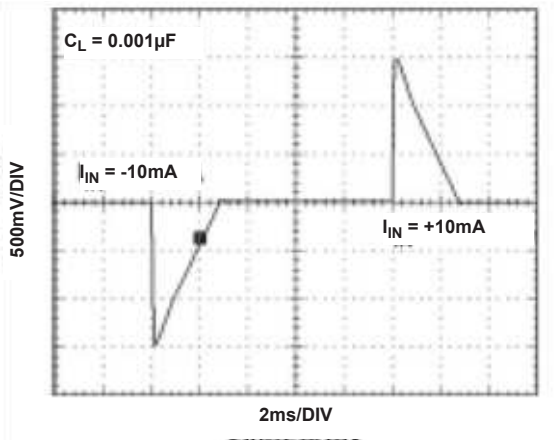


FIGURE 23. 10mA LOAD TRANSIENT RESPONSE

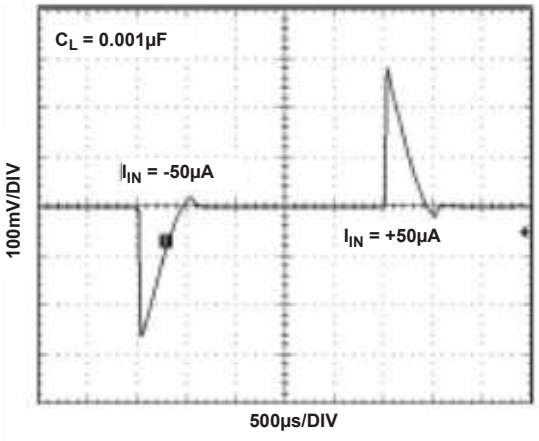


FIGURE 24. 50µA LOAD TRANSIENT RESPONSE

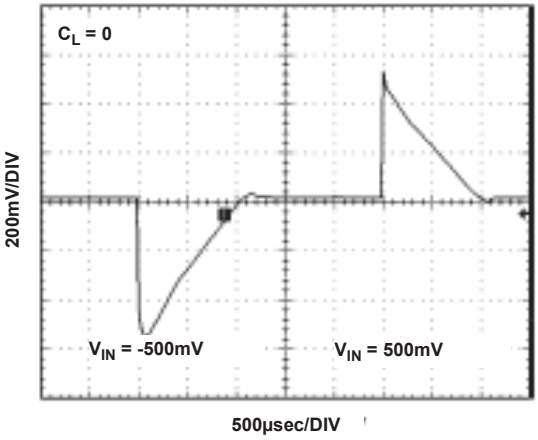


FIGURE 25. LINE TRANSIENT RESPONSE

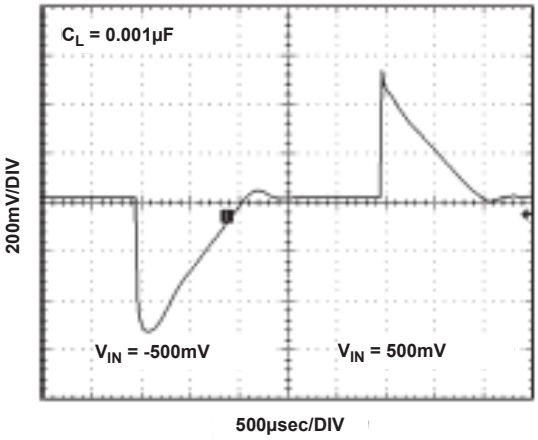


FIGURE 26. LINE TRANSIENT RESPONSE

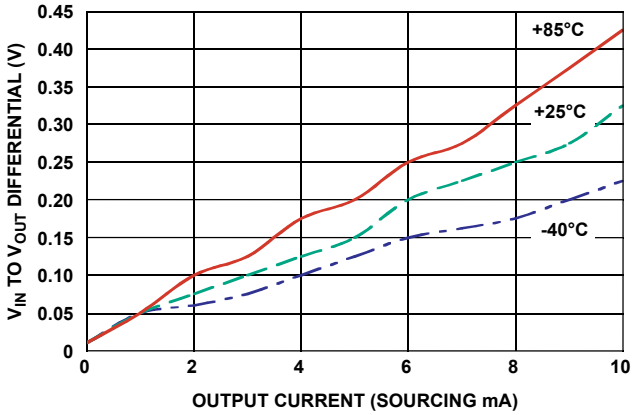


FIGURE 27. MINIMUM V_{IN} TO V_{OUT} DIFFERENTIAL vs OUTPUT CURRENT

Typical Performance Curves (X60003-50)

(V_{IN} = 6.5V, I_{OUT} = 0mA, T_A = +25°C unless otherwise specified) **(Continued)**

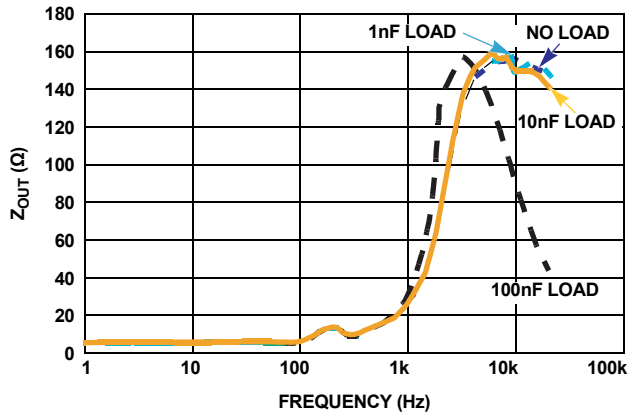


FIGURE 28. Z_{OUT} vs FREQUENCY

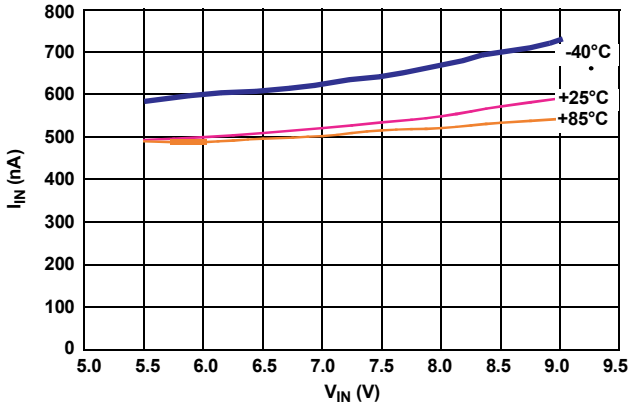


FIGURE 29. I_{IN} vs V_{IN}

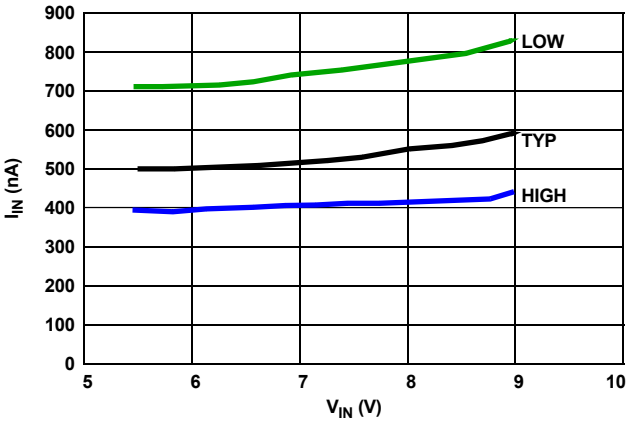


FIGURE 30. I_{IN} vs V_{IN} (3 UNITS)

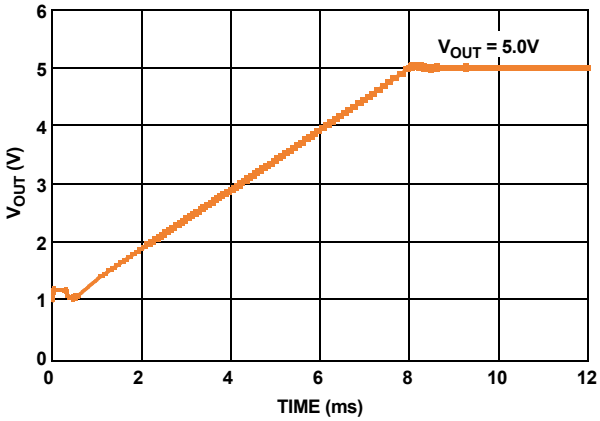


FIGURE 31. TURN-ON TIME

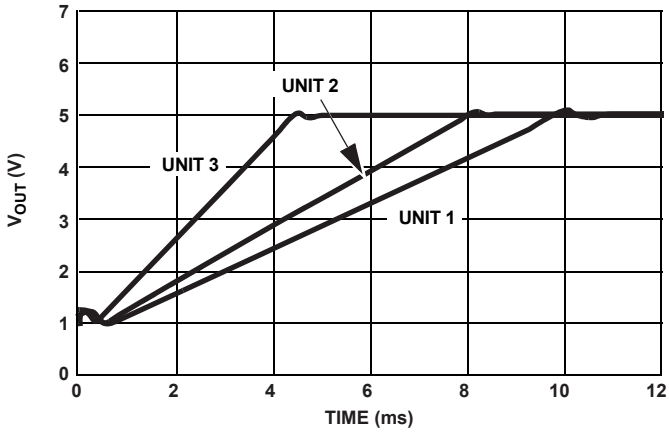


FIGURE 32. X60003 TURN-ON TIME (+25°C), 3 UNITS

Applications Information

FGA Technology

The X60003 voltage references use the floating gate technology to create references with very low drift and supply current. Essentially the charge stored on a floating gate cell is set precisely in manufacturing. The reference voltage output itself is a buffered version of the floating gate voltage. The resulting reference device has excellent characteristics which are unique in the industry: very low temperature drift, high initial accuracy, and almost zero supply current. Also, the reference voltage itself is not limited by voltage bandgaps or zener settings, so a wide range of reference voltages can be programmed (standard voltage settings are provided, but customer-specific voltages are available).

The process used for these reference devices is a floating gate CMOS process, and the amplifier circuitry uses CMOS transistors for amplifier and output transistor circuitry. While providing excellent accuracy, there are limitations in output noise level and load regulation due to the MOS device characteristics. These limitations are addressed with circuit techniques discussed in other sections.

Handling and Board Mounting

FGA references provide excellent initial accuracy and low temperature drift at the expense of very little power drain. There are some precautions to take to insure this accuracy is not compromised. Excessive heat during solder reflow can cause excessive initial accuracy drift, so the recommended +260°C max temperature profile should not be exceeded. Expect up to 1mV drift from the solder reflow process.

FGA references are susceptible to excessive X-radiation like that used in PC board manufacturing. Initial accuracy can change 10mV or more under extreme radiation. If an assembled board needs to be X-rayed, care should be taken to shield the FGA reference device.

Nanopower Operation

Reference devices achieve their highest accuracy when powered up continuously, and after initial stabilization has taken place.

The X60003 is the first high precision voltage reference with ultra low power consumption that makes it practical to leave power-on continuously in battery operated circuits. The X60003 consume extremely low supply current due to the proprietary FGA technology. Supply current at room temperature is typically 500nA which is 1 to 2 orders of magnitude lower than competitive devices. Application circuits using battery power will benefit greatly from having an accurate, stable reference which essentially presents no load to the battery.

In particular, battery-powered data converter circuits that would normally require the entire circuit to be disabled when not in use can remain powered-up between conversions as shown in Figure 33. Data acquisition circuits providing 12 to 24-bits of accuracy can operate with the reference device continuously biased with no power penalty, providing the highest accuracy and lowest possible long term drift.

Other reference devices consuming higher supply currents will need to be disabled in between conversions to conserve battery capacity. Absolute accuracy will suffer as the device is biased and requires time to settle to its final value, or, may not actually settle to a final value as power-on time may be short.

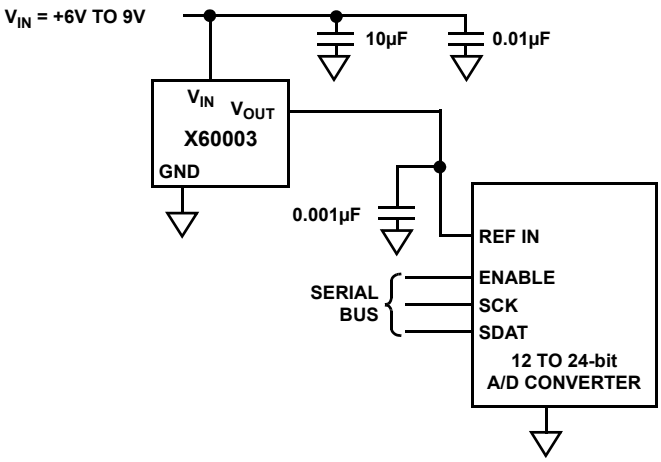


FIGURE 33. BATTERY-POWERED DATA CONVERTER CIRCUITS

Board Mounting Considerations

For applications requiring the highest accuracy, board mounting location should be reviewed. Placing the device in areas subject to slight twisting can cause degradation of the accuracy of the reference voltage due to die stresses. It is normally best to place the device near the edge of a board, or the shortest side, as the axis of bending is most limited at that location. Obviously mounting the device on flexprint or extremely thin PC material will likewise cause loss of reference accuracy.

Board Assembly Considerations

FGA references provide high accuracy and low temperature drift but some PC board assembly precautions are necessary. Normal Output voltage shifts of 100µV to 1mV can be expected with Pb-free reflow profiles or wave solder on multi-layer FR4 PC boards. Precautions should be taken to avoid excessive heat or extended exposure to high reflow or wave solder temperatures, this may reduce device initial accuracy.

Post-assembly x-ray inspection may also lead to permanent changes in device output voltage and should be minimized or avoided. If x-ray inspection is required, it is advisable to monitor the reference output voltage to verify excessive shift has not occurred. If large amounts of shift are observed, it is best to add an X-ray shield consisting of thin zinc (300µm) sheeting to allow clear imaging, yet block x-ray energy that affects the FGA reference.

Special Applications Considerations

In addition to post-assembly examination, there are also other X-ray sources that may affect the FGA reference long term accuracy. Airport screening machines contain X-rays and will have a cumulative effect on the voltage reference output accuracy. Carry-on luggage screening uses low level X-rays and is not a major source of output voltage shift, although if a product is expected to pass through that type of screening over 100 times it may need to consider shielding with copper or aluminum. Checked luggage X-rays are higher intensity and can cause output voltage shift in much fewer passes, so devices expected to go through those machines should definitely consider shielding. Note that just two layers of 1/2 ounce copper planes will reduce the received dose by over 90%. The leadframe for the device which is on the bottom also provides similar shielding.

If a device is expected to pass through luggage X-ray machines numerous times, it is advised to mount a 2-layer (minimum) PC board on the top, and along with a ground plane underneath will effectively shield it from 50 to 100 passes through the machine. Since these machines vary in X-ray dose delivered, it is difficult to produce an accurate maximum pass recommendation.

Noise Performance and Reduction

The output noise voltage in a 0.1Hz to 10Hz bandwidth is typically 30µV_{P-P}. This is shown in the plot in the "Typical Performance Curves" on page 8 and 9. The noise measurement is made with a bandpass filter made of a 1-pole high-pass filter with a corner frequency at 0.1Hz and a 2-pole low-pass filter with a corner frequency at 12.6Hz to create a filter with a 9.9Hz bandwidth. Noise in the 10kHz to 1MHz bandwidth is approximately 400µV_{P-P} with no capacitance on the output, as shown in Figure 34. These noise measurements are made with a 2 decade bandpass filter made of a 1-pole high-pass filter with a corner frequency at 1/10 of the center frequency and 1-pole low-pass filter with a corner frequency at 10x the center frequency. Figure 34 also shows the noise in the 10kHz to 1MHz band can be reduced to about 50µV_{P-P} using a 0.001µF capacitor on the output. Noise in the 1kHz to 100kHz band can be further reduced using a 0.1µF capacitor on the output, but noise in the 1Hz to 100Hz band increases due to instability of the very low power amplifier with a 0.1µF capacitance load. For load capacitances above 0.001µF, the noise reduction network shown in Figure 35 is recommended. This network reduces noise significantly over the full bandwidth. Figure 35 shows that noise is reduced to less than 40µV_{P-P} from 1Hz to 1MHz using this network with a 0.01µF capacitor and a 2kΩ resistor in series with a 10µF capacitor.

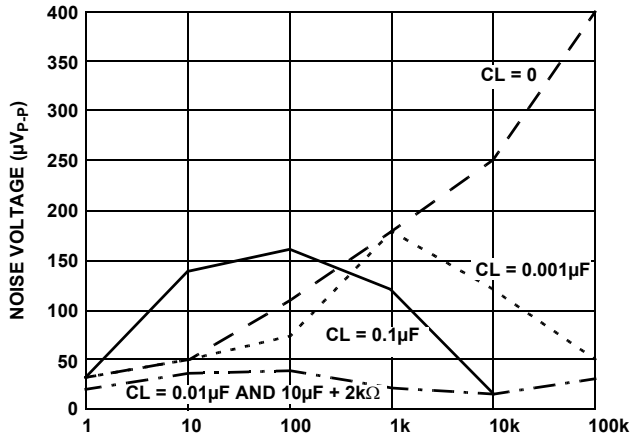


FIGURE 34. X60003 NOISE REDUCTION

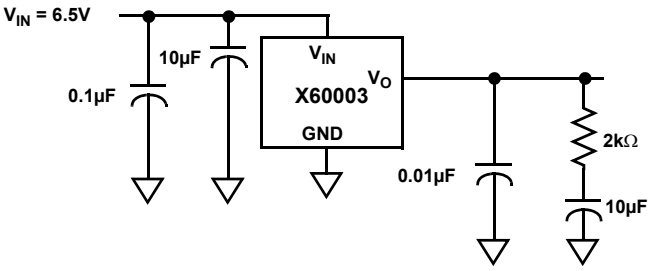


FIGURE 35. NOISE REDUCTION NETWORK

Turn-On Time

The X60003 device has ultra-low supply current and thus the time to bias-up internal circuitry to final values will be longer than with higher power references. Normal turn-on time is typically 7ms. This is shown in the graph, Figure 32. Since devices can vary in supply current down to 300nA, turn-on time can last up to about 12ms. Care should be taken in system design to include this delay before measurements or conversions are started.

Temperature Coefficient

The limits stated for temperature coefficient (tempco) are governed by the method of measurement. The overwhelming standard for specifying the temperature drift of a reference is to measure the reference voltage at two temperatures, take the total variation (V_{HIGH}- V_{LOW}), and divide by the temperature extremes of measurement (T_{HIGH} - T_{LOW}). The result is divided by the nominal reference voltage (at T = +25°C) and multiplied by 10^6 to yield ppm/°C. This is the "Box" method for determining temperature coefficient.

Typical Application Circuits

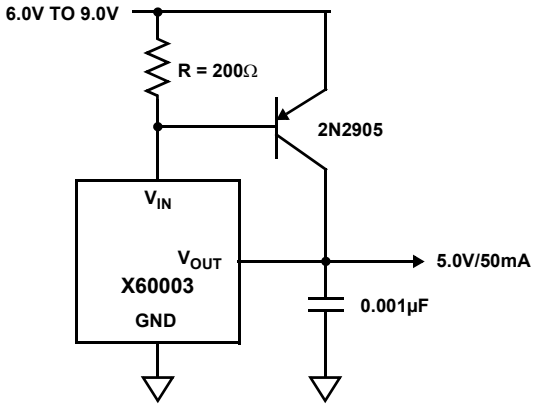


FIGURE 36. PRECISION 5V, 50mA REFERENCE

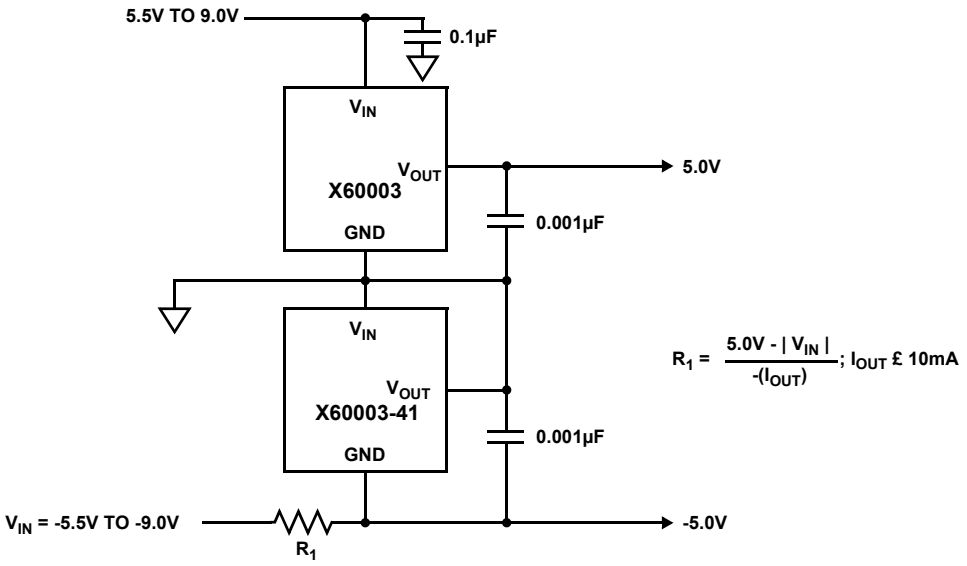


FIGURE 37. ±5.0V DUAL OUTPUT, HIGH ACCURACY REFERENCE

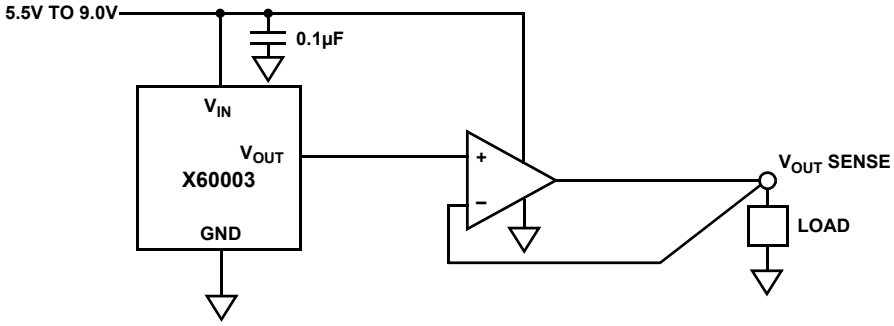


FIGURE 38. KELVIN SENSED LOAD

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
September 1, 2015	FN8137.5	Updated Ordering Information table on page 3.
June 23, 2014	FN8137.4	Updated POD with following changes: In Detail A, changed lead width dimension from 0.13+/-0.05 to 0.085-0.19 Changed dimension of foot of lead from 0.31+/-0.10 to 0.38+/-0.10 In Land Pattern, added 0.4 Rad Typ dimension In Side View, changed height of package from 0.91+/-0.03 to 0.95+/-0.07
March 31, 2010	FN8137.3	Throughout- Converted to new format. Changes made as follows: Moved “Available Options”, “Pin Configuration” and “Pin Descriptions” to page 2 Added “Related Literature” on page 1 Added key selling feature graphic Figure 1 to page 1 Added MSL note to “Ordering Information” table on page 3 Added "Boldface limits apply..." note to common conditions of Electrical Specifications tables on page 4 and page 5. Bolded applicable specs. Added Note 12 to MIN MAX columns of all Electrical Specifications tables. Added Latch Up to “Absolute Voltage Ratings” on page 4 Added Junction Temperature to “Thermal Information” on page 4 Added JEDEC standards used at the time of testing for “ESD Ratings” on page 4 Added “Revision History” on page 15 and “About Intersil” on page 16 Updated package outline drawing on page 17 to new format by adding land pattern and moving dimensions from table onto drawing Removed retired devices from “Ordering Information” table on page 3 and “Available Options” on page 2 as follows: X60003BIG3-41T1 X60003CIG3-41T1 X60003DIG3-41T1 X60003BIG3-50T1 X60003CIG3-50T1 X60003DIG3-50T1 Added the following to page 4: "Environmental Operating Conditions X-Ray Exposure (Note 4).....10mRem Note 4. Measured with no filtering, distance of 10” from source, intensity set to 55kV and 70mA current, 30s duration. Other exposure levels should be analyzed for Output Voltage drift effects. See “Applications Information” on page 10. “Thermal Information” on page 4: Changed Theta JA from 202.70 to 375. Added Theta JC of 110 and applicable note (measured at top of package). In Figures 1, 3, 5 and 30, changed the color to Dark Blue (Unit 3), Black (Unit 2), and Dark Green (Unit 1). Changed name of Unit 3 to High, Unit 2 to Typ and Unit 1 to Low. Figure 4. Changed the colors to Dark Blue (85), Black (25), and Dark Green (-40). Figure 29. Increased the Y-axis to 800nA. Added “Handling and Board Mounting” on page 12

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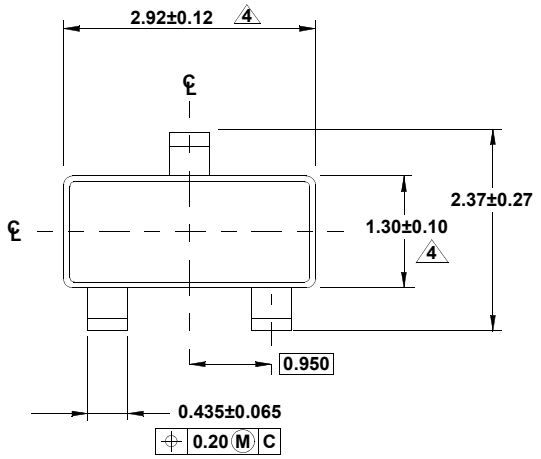
For information regarding Intersil Corporation and its products, see www.intersil.com

Package Outline Drawing

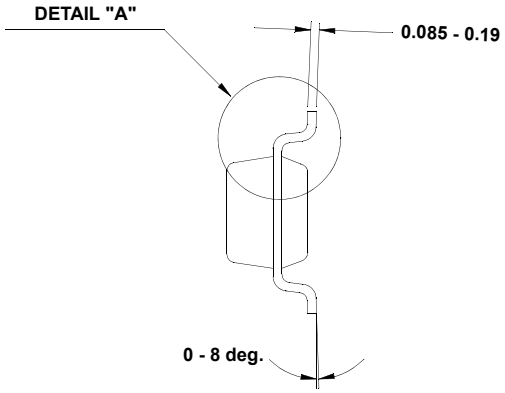
P3.064

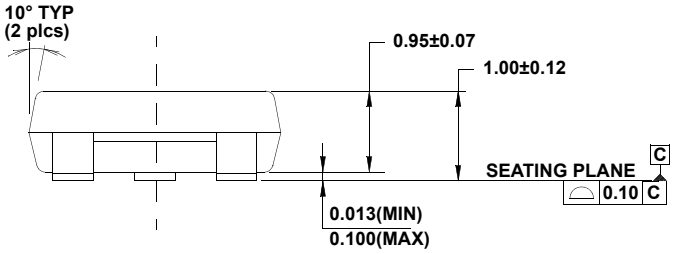
3 LEAD SMALL OUTLINE TRANSISTOR PLASTIC PACKAGE (SOT23-3)

Rev 3, 3/12

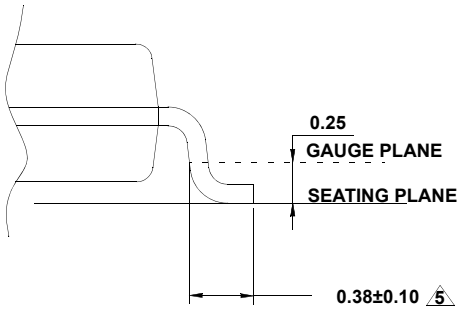


TOP VIEW

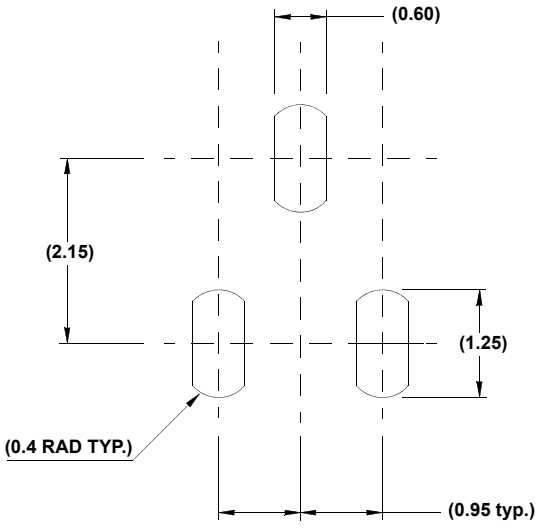




SIDE VIEW



DETAIL "A"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSEY14.5m-1994.
3. Reference JEDEC TO-236.
4. Dimension does not include interlead flash or protrusions.
   Interlead flash or protrusions shall not exceed 0.25mm per side.
5. Footlength is measured at reference to gauge plane.