RA6T2 Group
Renesas Microcontrollers

R01DS0400EJ0150
Rev.1.50
Jul 2, 2025

High-performance 240 MHz Arm Cortex-M33 core, up to 512 KB code flash memory with background operation, 16 KB Data flash memory, and 64 KB SRAM with ECC. Integrated A/D converter with channel-dedicated sample-and-hold circuit for simultaneous sampling and single-end/pseudo-differential input supportive amplifier. Integrated General PWM Timer with 200 MHz operation and high resolution. Integrated Secure Cryptographic Engine with cryptography accelerators and key management support in concert with Arm TrustZone for integrated secure element functionality.

Features

Arm® Cortex®-M33 Core

- Armv8-M architecture with the main extension
- Maximum operating frequency: 240 MHz
- Arm Memory Protection Unit (Arm MPU)
  - Protected Memory System Architecture (PMSAv8)
  - Secure MPU (MPU_S): 8 regions
  - Non-secure MPU (MPU_NS): 8 regions
- SysTick timer
  - Embeds two SysTick timers: Secure and Non-secure instance
  - Driven by LOCO or system clock
- CoreSight™ ETM-M33

Memory

- Up to 512-KB code flash memory
- 16-KB data flash memory (125,000 program/erase (P/E) cycles)
- 64-KB SRAM

Connectivity

- Serial Communications Interface (SCI) × 6
  - Asynchronous interfaces
  - 8-bit clock synchronous interface
  - Smart card interface
  - Simple IIC
  - Simple SPI
  - Simple LIN
  - Manchester coding
- I^2C bus interface (IIC) × 2
  - Transfer at up to 3.2 Mbps (high speed mode)
- Serial Peripheral Interface (SPI) × 2
- CAN with Flexible Data-rate (CANFD)

Analog

- A/D Converter (ADC) × 2
  - Up to 16-bit resolution
  - Up to 6.25 Msps
  - Channel-dedicated sample-and-hold circuit × 6
  - Programmable Gain Amplifier (PGA) × 4
- High-Speed Analog Comparator (ACMPHS) × 4
- 12-bit D/A Converter (DAC12) × 4
- Temperature Sensor (TSN)

Timers

- General PWM Timer 32-bit (GPT32) with High Resolution × 4
  - 156 ps resolution in 200 MHz
- General PWM Timer 32-bit (GPT32) × 6
- Low Power Asynchronous General Purpose Timer (AGT) × 2

Security and Encryption

- Secure Cryptographic Engine (SCE5)
  - Symmetric algorithms: AES
  - Hash-value generation: GHASH
  - 128-bit unique ID
- Arm® TrustZone®
  - Up to three regions for the code flash
  - Up to two regions for the data flash
  - Up to three regions for the SRAM
  - Individual secure or non-secure security attribution for each peripheral
- Device lifecycle management

System and Power Management

- Low power modes
- Event Link Controller (ELC)
- Data Transfer Controller (DTC)
- DMA Controller (DMAC) × 8
- Power-on reset
- Low Voltage Detection (LVD) with voltage settings
- Watchdog Timer (WDT)
- Independent Watchdog Timer (IWDT)
- Key Interrupt Function (KINT)

Data Processing Accelerator

- Trigonometric Function Unit (TFU)
- IIR Filter Accelerator (IIRFA)

Multiple Clock Sources

- Main clock oscillator (MOSC) (8 to 24 MHz)
- High-speed on-chip oscillator (HOCO) (16/18/20 MHz)
- Middle-speed on-chip oscillator (MOCO) (8 MHz)
- Low-speed on-chip oscillator (LOCO) (32.768 kHz)
- IWDT-dedicated on-chip oscillator (15 kHz)
- Clock trim function for HOCO/MOCO/LOCO
- PLL/PLL2
- Clock out support

General-Purpose I/O Ports

- 5-V tolerance, open drain, input pull-up, switchable driving ability

Operating Voltage

- VCC: 2.7 to 3.6 V

Operating Temperature and Packages

- Ta = -40°C to +105°C
  - 100-pin LQFP (14 mm × 14 mm, 0.5 mm pitch)
  - 64-pin LQFP (10 mm × 10 mm, 0.5 mm pitch)
  - 48-pin LQFP (7 mm × 7 mm, 0.5 mm pitch)
  - 64-pin QFN (8 mm × 8 mm, 0.4 mm pitch)
  - 48-pin QFN (7 mm × 7 mm, 0.5 mm pitch)

1. Overview

The MCU integrates multiple series of software-compatible Arm®-based 32-bit cores that share a common set of Renesas peripherals to facilitate design scalability and efficient platform-based product development.

The MCU in this series incorporates a high-performance Arm Cortex®-M33 core running up to 240 MHz with the following features:

- Up to 512 KB code flash memory
- 64 KB SRAM
- General PWM Timer (GPT) - Enhanced High Resolution
- Analog peripherals
- Security and safety features

1.1 Function Outline

Table 1.1 Arm core

Feature	Functional description
Arm Cortex-M33 core	• Maximum operating frequency: up to 240 MHz • Arm Cortex-M33 core: – Armv8-M architecture with security extension – Revision: r0p4-00rel0 • Arm Memory Protection Unit (Arm MPU) – Protected Memory System Architecture (PMSAv8) – Secure MPU (MPU_S): 8 regions – Non-secure MPU (MPU_NS): 8 regions • SysTick timer – Embeds two SysTick timers: Secure and Non-secure instance – Driven by SysTick timer clock (SYSTICCLK) or system clock (ICLK) • CoreSight™ ETM-M33

Table 1.2 Memory

Feature	Functional description
Code flash memory	Maximum 512 KB of code flash memory.
Data flash memory	16 KB of data flash memory.
Option-setting memory	The option-setting memory determines the state of the MCU after a reset.
SRAM	On-chip high-speed SRAM with Error Correction Code (ECC).

Table 1.3 System (1 of 2)

Feature	Functional description
Operating modes	Two operating modes: • Single-chip mode • SCI boot mode
Resets	The MCU provides 14 resets.
Low Voltage Detection (LVD)	The Low Voltage Detection (LVD) module monitors the voltage level input to the VCC pin. The detection level can be selected by register settings. The LVD module consists of three separate voltage level detectors (LVD0, LVD1, LVD2). LVD0, LVD1, and LVD2 measure the voltage level input to the VCC pin. LVD registers allow your application to configure detection of VCC changes at various voltage thresholds.
Clocks	• Main clock oscillator (MOSC) • High-speed on-chip oscillator (HOCO) • Middle-speed on-chip oscillator (MOCO) • Low-speed on-chip oscillator (LOCO) • IWDT-dedicated on-chip oscillator • PLL/PLL2 • Clock out support

Table 1.3 System (2 of 2)

Feature	Functional description
Clock Frequency Accuracy Measurement Circuit (CAC)	The Clock Frequency Accuracy Measurement Circuit (CAC) counts pulses of the clock to be measured (measurement target clock) within the time generated by the clock selected as the measurement reference (measurement reference clock), and determines the accuracy depending on whether the number of pulses is within the allowable range. When measurement is complete or the number of pulses within the time generated by the measurement reference clock is not within the allowable range, an interrupt request is generated.
Interrupt Controller Unit (ICU)	The Interrupt Controller Unit (ICU) controls which event signals are linked to the Nested Vector Interrupt Controller (NVIC), the DMA Controller (DMAC), and the Data Transfer Controller (DTC) modules. The ICU also controls non-maskable interrupts.
Key Interrupt Function (KINT)	The key interrupt function (KINT) generates the key interrupt by detecting rising or falling edge on the key interrupt input pins.
Low power modes	Power consumption can be reduced in multiple ways, including setting clock dividers, stopping modules, selecting power control mode in normal operation, and transitioning to low power modes.
Register write protection	The register write protection function protects important registers from being overwritten due to software errors. The registers to be protected are set with the Protect Register (PRCR).
Memory Protection Unit (MPU)	The MCU has one Memory Protection Unit (MPU).

Table 1.4 Event link

Feature	Functional description
Event Link Controller (ELC)	The Event Link Controller (ELC) uses the event requests generated by various peripheral modules as source signals to connect them to different modules, allowing direct link between the modules without CPU intervention.

Table 1.5 Direct memory access

Feature	Functional description
Data Transfer Controller (DTC)	A Data Transfer Controller (DTC) module is provided for transferring data when activated by an interrupt request.
DMA Controller (DMAC)	The MCU includes an 8-channel direct memory access controller (DMAC) that can transfer data without intervention from the CPU. When a DMA transfer request is generated, the DMAC transfers data stored at the transfer source address to the transfer destination address.

Table 1.6 Timers (1 of 2)

Feature	Functional description
General PWM Timer (GPT)	The General PWM Timer (GPT) is a 32-bit timer with GPT32 × 10 channels. PWM waveforms can be generated by controlling the up-counter, down-counter, or the up- and down-counter. In addition, PWM waveforms can be generated for controlling brushless DC motors. The GPT can also be used as a general-purpose timer.
PWM Delay Generation Circuit (PDG)	The PWM Delay Generation circuit (PDG) has 4 channels delay circuits that can connect to the GPT. The PDG can control the rise and fall edge timing with which the PWM output for the GPT320 through the GPT323.
Port Output Enable for GPT (POEG)	The POEG issues requests to stop output from output pins of the general PWM timer (GPT). Select the method of detection for stopping the output from the list below.
Low power Asynchronous General Purpose Timer (AGT)	The low power Asynchronous General Purpose Timer (AGT) is a 32-bit timer that can be used for pulse output, external pulse width or period measurement, and counting external events. This timer consists of a reload register and a down counter. The reload register and the down counter are allocated to the same address, and can be accessed with the AGT register.
Watchdog Timer (WDT)	The Watchdog Timer (WDT) is a 14-bit down counter that can be used to reset the MCU when the counter underflows because the system has run out of control and is unable to refresh the WDT. In addition, the WDT can be used to generate a non-maskable interrupt or an underflow interrupt.

Table 1.6 Timers (2 of 2)

Feature	Functional description
Independent Watchdog Timer (IWDT)	The Independent Watchdog Timer (IWDT) consists of a 14-bit down counter that must be serviced periodically to prevent counter underflow. The IWDT provides functionality to reset the MCU or to generate a non-maskable interrupt or an underflow interrupt. Because the timer operates with an independent, dedicated clock source, it is particularly useful in returning the MCU to a known state as a fail-safe mechanism when the system runs out of control. The IWDT can be triggered automatically by a reset, underflow, refresh error, or a refresh of the count value in the registers.

Table 1.7 Communication interfaces

Feature	Functional description
Serial Communications Interface (SCI)	The Serial Communications Interface (SCI) × 6 channels have asynchronous and synchronous serial interfaces: ● Asynchronous interfaces (UART and Asynchronous Communications Interface Adapter (ACIA)) ● 8-bit clock synchronous interface ● Simple IIC (master-only) ● Simple SPI ● Simple LIN ● Smart card interface ● Manchester interface The smart card interface complies with the ISO/IEC 7816-3 standard for electronic signals and transmission protocol. SCIn (n = 0 to 4, 9) has FIFO buffers to enable continuous and full-duplex communication, and the data transfer speed can be configured independently using an on-chip baud rate generator.
I^2C bus interface (IIC)	The I^2C bus interface (IIC) has 2 channels. The IIC module conform with and provide a subset of the NXP I^2C (Inter-Integrated Circuit) bus interface functions.
Serial Peripheral Interface (SPI)	The Serial Peripheral Interface (SPI) has 2 channels. The SPI provides high-speed full-duplex synchronous serial communications with multiple processors and peripheral devices.
CAN with Flexible Data-rate (CANFD)	The CAN with Flexible Data-rate (CANFD) module can handle classical CAN frames and CAN-FD frames complied with ISO 11898-1 standard. The module supports 4 transmit buffers and 32 receive buffer.

Table 1.8 Analog

Feature	Functional description
A/D Converter (ADC)	The A/D Converter (ADC) has two units of noise-shaping SAR-type A/D converter. ● Hybrid architecture that combines the features of the successive approximation register-type and the delta-sigma modulation-type. ● Up to 16-bit resolution ● Up to 6.25 Msps ● Up to 29 analog input channels ● Support single-ended input or differential inputs ● Built-in channel-dedicated sample-and-hold circuit (SH) ● Built-in Programmable Gain Amplifier (PGA) ● Temperature sensor output and internal reference voltage, and D/A converters output are selectable for conversion.
12-bit D/A Converter (DAC12)	A 12-bit D/A converter (DAC12) is provided.
High-Speed Analog Comparator (ACMPHS)	The High-Speed Analog Comparator (ACMPHS) compares a test voltage with a reference voltage and provides a digital output based on the conversion result. Both the test and reference voltages can be provided to the comparator from internal sources such as the DAC12 output and an internal PGA output, and an external source. Such flexibility is useful in applications that require go/no-go comparisons to be performed between analog signals without necessarily requiring A/D conversion.
Temperature Sensor (TSN)	The on-chip Temperature Sensor (TSN) determines and monitors the die temperature for reliable operation of the device. The sensor outputs a voltage directly proportional to the die temperature, and the relationship between the die temperature and the output voltage is fairly linear. The output voltage is provided to the ADC for conversion and can be further used by the end application.

Table 1.9 Data processing

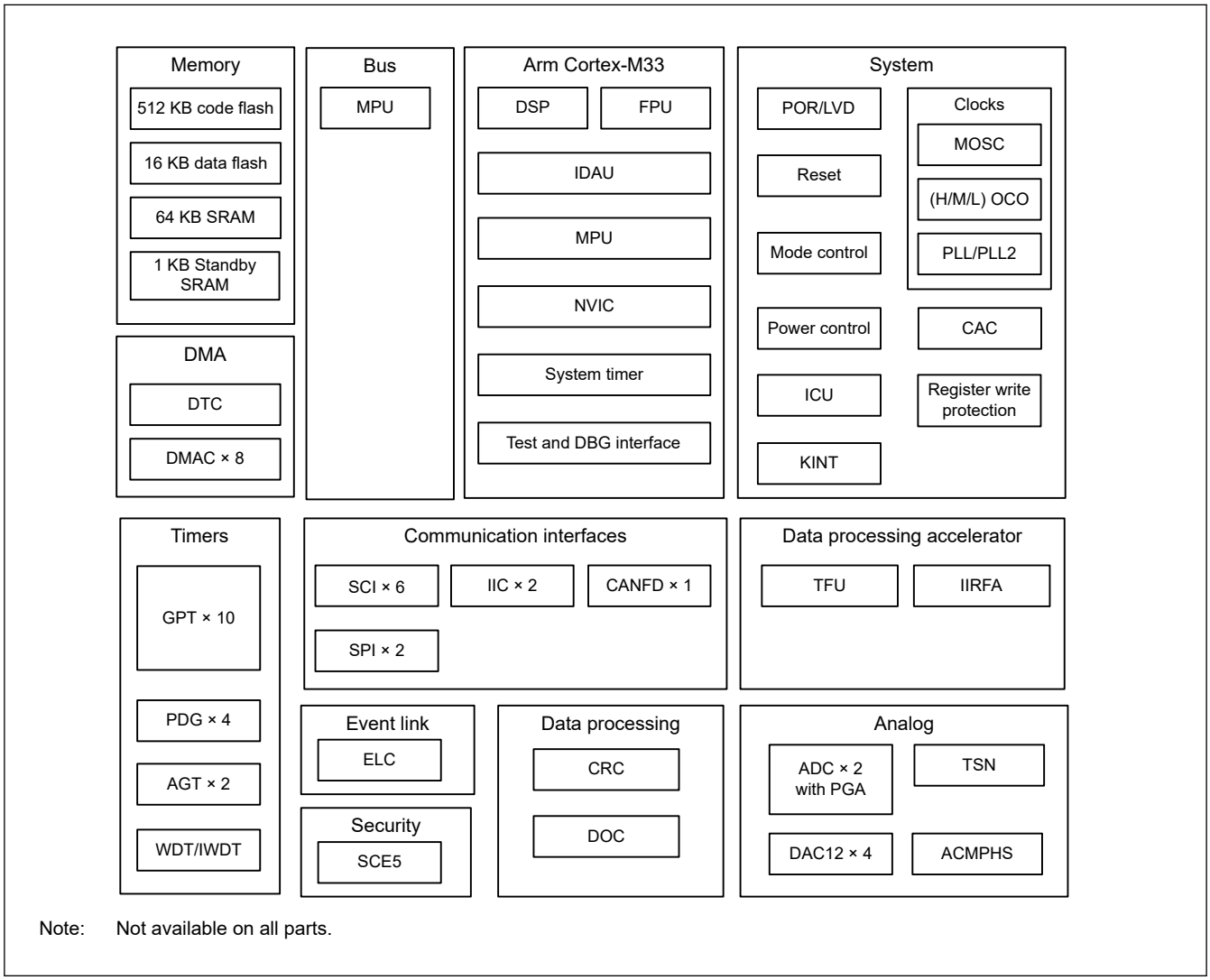
Feature	Functional description
Cyclic Redundancy Check (CRC)	The Cyclic Redundancy Check (CRC) generates CRC codes to detect errors in the data. The bit order of CRC calculation results can be switched for LSB-first or MSB-first communication. Additionally, various CRC-generation polynomials are available. The snoop function allows to monitor the access to specific addresses. This function is useful in applications that require CRC code to be generated automatically in certain events, such as monitoring writes to the serial transmit buffer and reads from the serial receive buffer.
Data Operation Circuit (DOC)	The data operation circuit (DOC) is used to compare, add, and subtract 16 or 32-bit data. An interrupt can be generated when the following conditions apply. ● When the 16 or 32-bit compared values match the detection condition ● When the result of 16 or 32-bit data addition overflows ● When the result of 16 or 32-bit data subtraction underflows

Table 1.10 Data processing accelerator

Feature	Functional description
Trigonometric function unit (TFU)	Calculation of sine, cosine, arctangent, and hypot_k ($\sqrt{x^2+y^2}/k$) ● A sine and cosine can be simultaneously calculated. ● An arctangent and hypot_k can be simultaneously calculated.
IIR Filter Accelerator (IIRFA)	● 16 channels of biquad IIR filter ● Cascaded biquad filter (max.32 stages) ● Operations using single-precision floating-point numbers

1.2 Block Diagram

Figure 1.1 shows a block diagram of the MCU superset. Some individual devices within the group have a subset of the features.

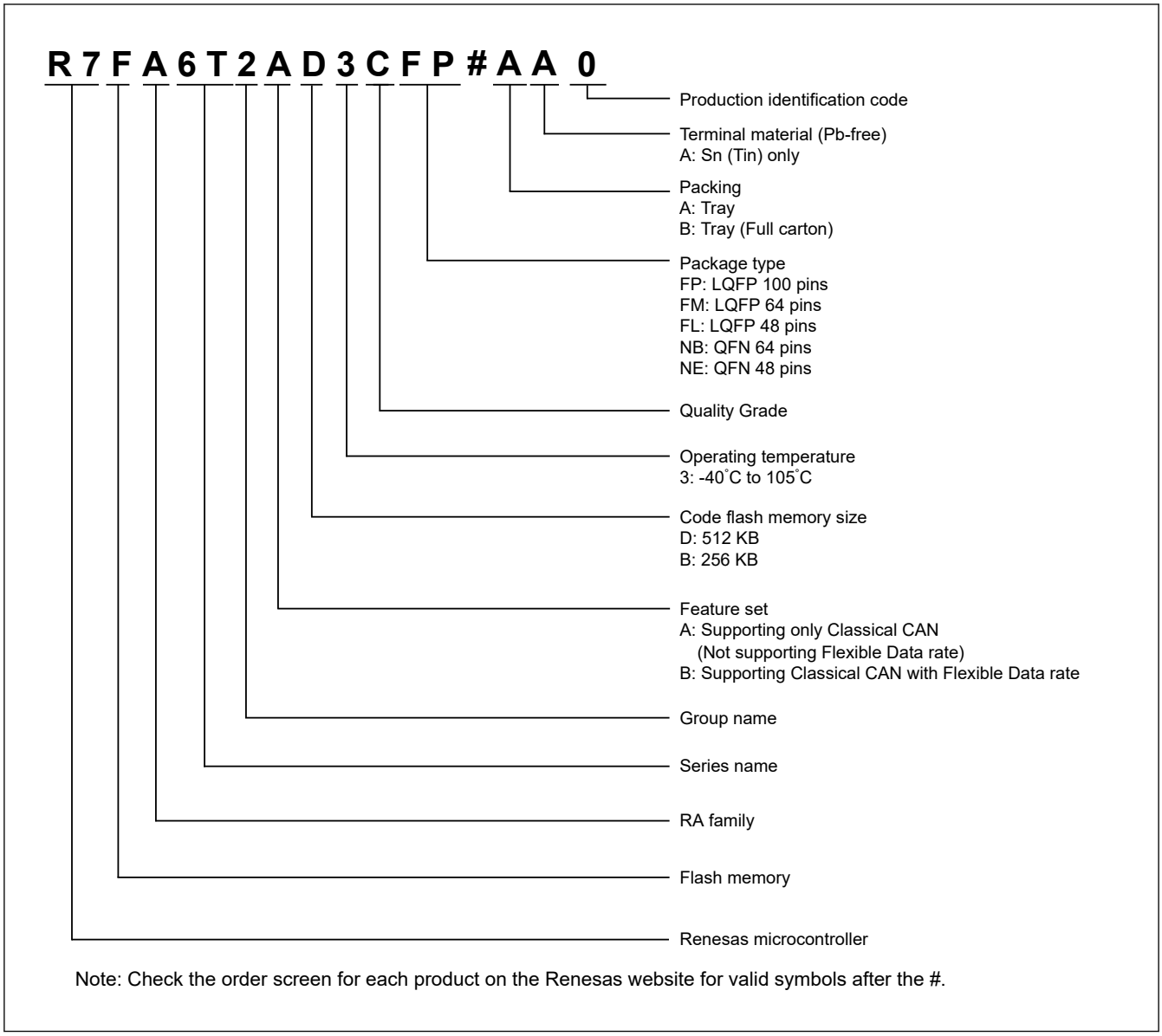


Note: Not available on all parts.

Figure 1.1 Block diagram

1.3 Part Numbering

Figure 1.2 shows the product part number information, including memory capacity and package type. Table 1.11 shows a list of products.



Note: Check the order screen for each product on the Renesas website for valid symbols after the #.

Figure 1.2 Part numbering scheme

Table 1.11 Product list (1 of 2)

Product part number	Package code	Code flash	Data flash	SRAM	CAN-FD	Operating temperature
R7FA6T2AD3CFP	PLQP0100KB-B	512 KB	16 KB	64 KB	Not support	-40 to +105°C
R7FA6T2AD3CFM	PLQP0064KB-C					
R7FA6T2AD3CFL	PLQP0048KB-B					
R7FA6T2AD3CNB	PWQN0064LB-A					
R7FA6T2AD3CNE	PWQN0048KC-A					
R7FA6T2AB3CFP	PLQP0100KB-B	256 KB				
R7FA6T2AB3CFM	PLQP0064KB-C					
R7FA6T2AB3CFL	PLQP0048KB-B					
R7FA6T2AB3CNB	PWQN0064LB-A					
R7FA6T2AB3CNE	PWQN0048KC-A					

Table 1.11 Product list (2 of 2)

Product part number	Package code	Code flash	Data flash	SRAM	CAN-FD	Operating temperature
R7FA6T2BD3CFP	PLQP0100KB-B	512 KB	16 KB	64 KB	Support	-40 to +105°C
R7FA6T2BD3CFM	PLQP0064KB-C					
R7FA6T2BD3CFL	PLQP0048KB-B					
R7FA6T2BD3CNB	PWQN0064LB-A					
R7FA6T2BD3CNE	PWQN0048KC-A					
R7FA6T2BB3CFP	PLQP0100KB-B	256 KB				
R7FA6T2BB3CFM	PLQP0064KB-C					
R7FA6T2BB3CFL	PLQP0048KB-B					
R7FA6T2BB3CNB	PWQN0064LB-A					
R7FA6T2BB3CNE	PWQN0048KC-A					

1.4 Function Comparison

Table 1.12 Function Comparison

Parts number		R7FA6T2XX3CFP	R7FA6T2XX3CFM	R7FA6T2XX3CFL	R7FA6T2XX3CNB	R7FA6T2XX3CNE
Pin count		100	64	48	64	48
Package		LQFP			QFN	
Code flash memory		512 KB, 256KB				
Data flash memory		16 KB				
SRAM	ECC	64 KB				
Standby SRAM	Parity	1 KB				
DMA	DTC	Yes				
	DMAC	8				
System	CPU clock	240 MHz (max.)				
	CPU clock sources	MOSC, HOCO, MOCO, LOCO, PLL				
	CAC	Yes				
	WDT/IWDT	Yes				
	KINT	Yes				
Communication	SCI	6				
	IIC	2*2				
	SPI	2				
	CANFD	1				
Timers	GPT*1	10				
	AGT*1	2				
Analog	ADC	Unit 0: 12 + 9*3, Unit 1: 8 + 9*3	Unit 0: 10, Unit 1: 8	Unit 0: 6, Unit 1: 4	Unit 0: 10, Unit 1: 8	Unit 0: 6, Unit 1: 4
	DAC12	4		2	4	2
	ACMPHS	4		3	4	3
	PGA	4		3	4	3
	TSN	Yes				
Data processing	CRC	Yes				
	DOC	Yes				
Event control	ELC	Yes				
Accelerator	TFU	Yes				
	IIRFA	Yes				
Security		SCE5, TrustZone and Lifecycle management				

Note: The product name differs depending on the memory size and whether CAN-FD is supported. See section 1.3. Part Numbering.
Note 1. Available pins depend on the Pin count. For details, see section 1.7. Pin Lists.
Note 2. Fm+ and Hs-mode are only available for IIC channel IIC0.
Note 3. Shared terminal for UNIT0 and UNIT1.

1.5 Pin Functions

Table 1.13 Pin functions (1 of 3)

Function	Signal	I/O	Description
Power supply	VCC	Input	Power supply pin. Connect it to the system power supply. Connect this pin to VSS by a 0.1-μF capacitor. The capacitor should be placed close to the pin.
	VCL	I/O	Connect this pin to the VSS pin by the smoothing capacitor used to stabilize the internal power supply. Place the capacitor close to the pin.
	VSS	Input	Ground pin. Connect it to the system power supply (0 V).
Clock	EXTAL	Input	Pins for a crystal resonator. An external clock signal can be input through the EXTAL pin.
	XTAL	Output	
	CLKOUT	Output	Clock output pin
Operating mode control	MD	Input	Pin for setting the operating mode. The signal level on this pin must not be changed during operation mode transition on release from the reset state.
System control	RES	Input	Reset signal input pin. The MCU enters the reset state when this signal goes low.
CAC	CACREF	Input	Measurement reference clock input pin
On-chip emulator	TMS	Input	On-chip emulator or boundary scan pins
	TDI	Input	
	TCK	Input	
	TDO	Output	
	TCLK	Output	Output clock for synchronization with the trace data
	TDATA0 to TDATA3	Output	Trace data output
	SWO	Output	Serial wire trace output pin
	SWDIO	I/O	Serial wire debug data input/output pin
	SWCLK	Input	Serial wire clock pin
Interrupt	NMI	Input	Non-maskable interrupt request pin
	IRQn	Input	Maskable interrupt request pins
	IRQn-DS	Input	Maskable interrupt request pins that can also be used in Deep Software Standby mode
KINT	KR00 to KR07	Input	Key interrupt input pins

Table 1.13 Pin functions (2 of 3)

Function	Signal	I/O	Description
GPT	GTETRGA, GTETRGB, GTETRGC, GTETRGD	Input	External trigger input pins
	GTIOCnA, GTIOCnB	I/O	Input capture, output compare, or PWM output pins
	GTADSM0, GTADSM1	Output	A/D conversion start request monitoring output pins
	GTCPPO0 to GTCPPO4, GTCPPO7	Output	Toggle output synchronized with PWM period
	GTIU	Input	Hall sensor input pin U
	GTIV	Input	Hall sensor input pin V
	GTIW	Input	Hall sensor input pin W
	GTOUUP	Output	3-phase PWM output for BLDC motor control (positive U phase)
	GTOULO	Output	3-phase PWM output for BLDC motor control (negative U phase)
	GTOVUP	Output	3-phase PWM output for BLDC motor control (positive V phase)
	GTOVLO	Output	3-phase PWM output for BLDC motor control (negative V phase)
	GTOWUP	Output	3-phase PWM output for BLDC motor control (positive W phase)
	GTOWLO	Output	3-phase PWM output for BLDC motor control (negative W phase)
AGT	AGTEEn	Input	External event input enable signals
	AGTIOn	I/O	External event input and pulse output pins
	AGTOn	Output	Pulse output pins
	AGTOAn	Output	Output compare match A output pins
	AGTOBn	Output	Output compare match B output pins
SCI	SCKn	I/O	Input/output pins for the clock (clock synchronous mode)
	RXDn	Input	Input pins for received data (asynchronous mode/clock synchronous mode)
	TXDn	Output	Output pins for transmitted data (asynchronous mode/clock synchronous mode)
	CTSn_RTSn	I/O	Input/output pins for controlling the start of transmission and reception (asynchronous mode/clock synchronous mode), active-low.
	CTSn	Input	Input for the start of transmission.
	DEn	Output	Output pins for Driver Enable signal
	SCLn	I/O	Input/output pins for the IIC clock (simple IIC mode)
	SDAn	I/O	Input/output pins for the IIC data (simple IIC mode)
	SCKn	I/O	Input/output pins for the clock (simple SPI mode)
	MISOn	I/O	Input/output pins for slave transmission of data (simple SPI mode)
	MOSIn	I/O	Input/output pins for master transmission of data (simple SPI mode)
	SSn	Input	Chip-select input pins (simple SPI mode), active-low
IIC	SCLn	I/O	Input/output pins for the clock
	SDAn	I/O	Input/output pins for data
SPI	RSPCKA, RSPCKB	I/O	Clock input/output pin
	MOSIA, MOSIB	I/O	Input or output pins for data output from the master
	MISOA, MISOB	I/O	Input or output pins for data output from the slave
	SSLA0, SSLB0	I/O	Input or output pin for slave selection
	SSLA1 to SSLA3, SSLB1 to SSLB3	Output	Output pins for slave selection

Table 1.13 Pin functions (3 of 3)

Function	Signal	I/O	Description
CANFD	CRX0	Input	Receive data
	CTX0	Output	Transmit data
Analog power supply	AVCC0	Input	Analog voltage supply pin. This is used as the analog power supply for the respective modules. Supply this pin with the same voltage as the VCC pin.
	AVSS0	Input	Analog ground pin. This is used as the analog ground for the respective modules. Supply this pin with the same voltage as the VSS pin.
	VREFH0	Input	Analog reference voltage supply pin for the ADC. Connect this pin to AVCC0 when not using the ADC.
	VREFL0	Input	Analog reference ground pin for the ADC. Connect this pin to AVSS0 when not using the ADC.
ADC	AN000 to AN028	Input	Input pins for the analog signals to be processed by the A/D converter.
	PGAIN0 to PGAIN3	Input	Pseudo-differential input pins of programmable gain amplifier (Signal source side)
	PGAVSS0 to PGAVSS3	Input	Pseudo-differential input pins of programmable gain amplifier (reference ground side)
	PGAOUT0 to PGAOUT3	Output	Monitor output pins of programmable gain amplifier
	ADTRGm	Input	Input pins for the external trigger signals that start the A/D conversion, active-low.
DAC12	DAn	Output	Output pins for the analog signals processed by the D/A converter.
ACMPHS	VCOUT	Output	Comparator output pin (OR output of all units)
	CMPOUTm	Output	Comparator output pin (m:unit number)
	CMPOUT012	Output	Comparator output pin (OR output of units 0, 1 and 2)
	IVREF0, IVREF1	Input	Reference voltage input pins for comparator
	IVCMPm0, IVCMPm2, IVCMPm3	Input	Analog voltage input pins for comparator (m:unit number)
I/O ports	P201, P212, P213, PA08 to PA15, PB03 to PB10, PB12 to PB15, PC06 to PC12, PC14, PC15, PD00 to PD15, PE00 to PE06, PE08 to PE15	I/O	General-purpose input/output pins
	P000, P001, P002, PA00 to PA07, PB00 to PB02, PC00 to PC05, PC13	Input	General-purpose input pins

1.6 Pin Assignments

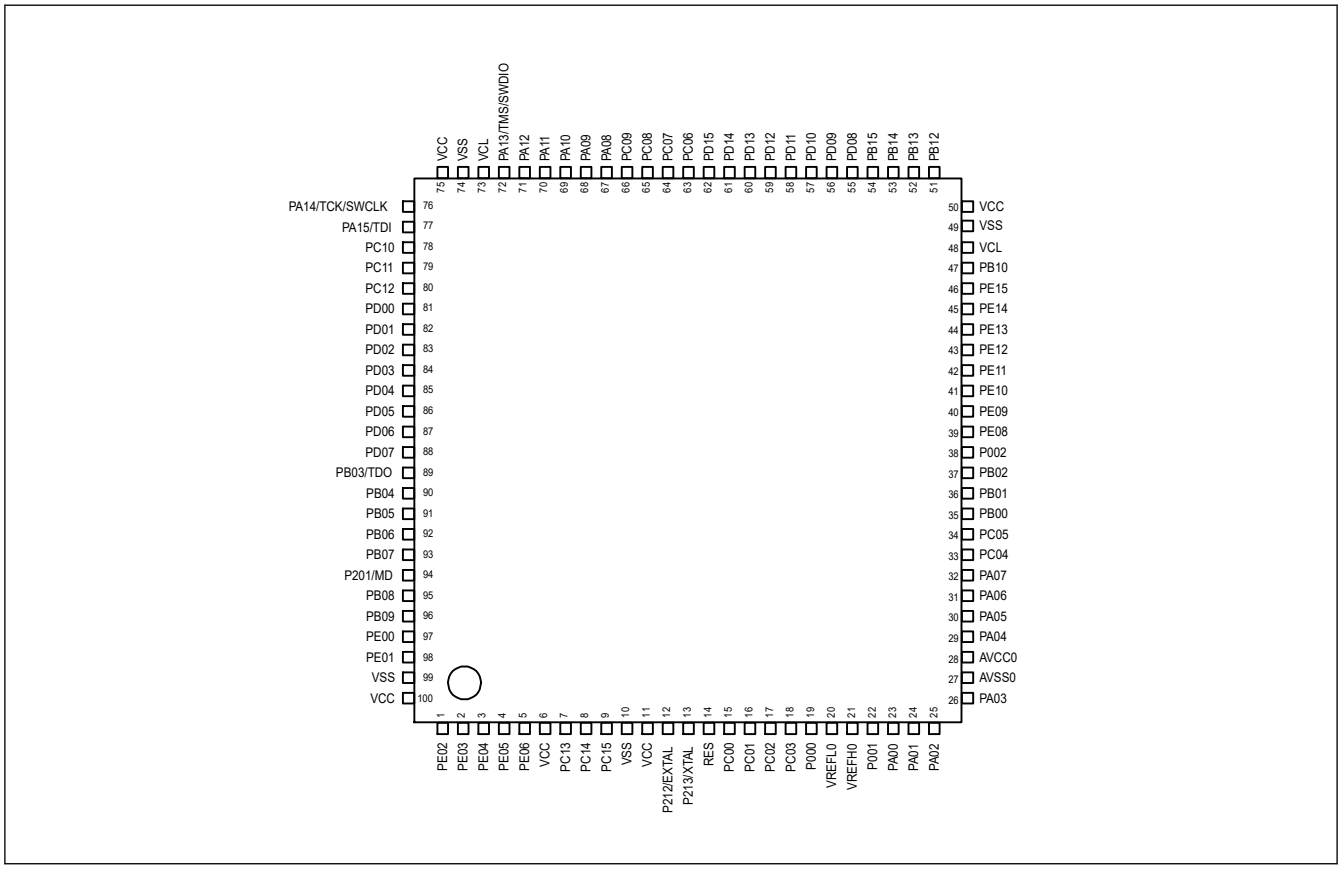


Figure 1.3 Pin assignment for LQFP 100-pin

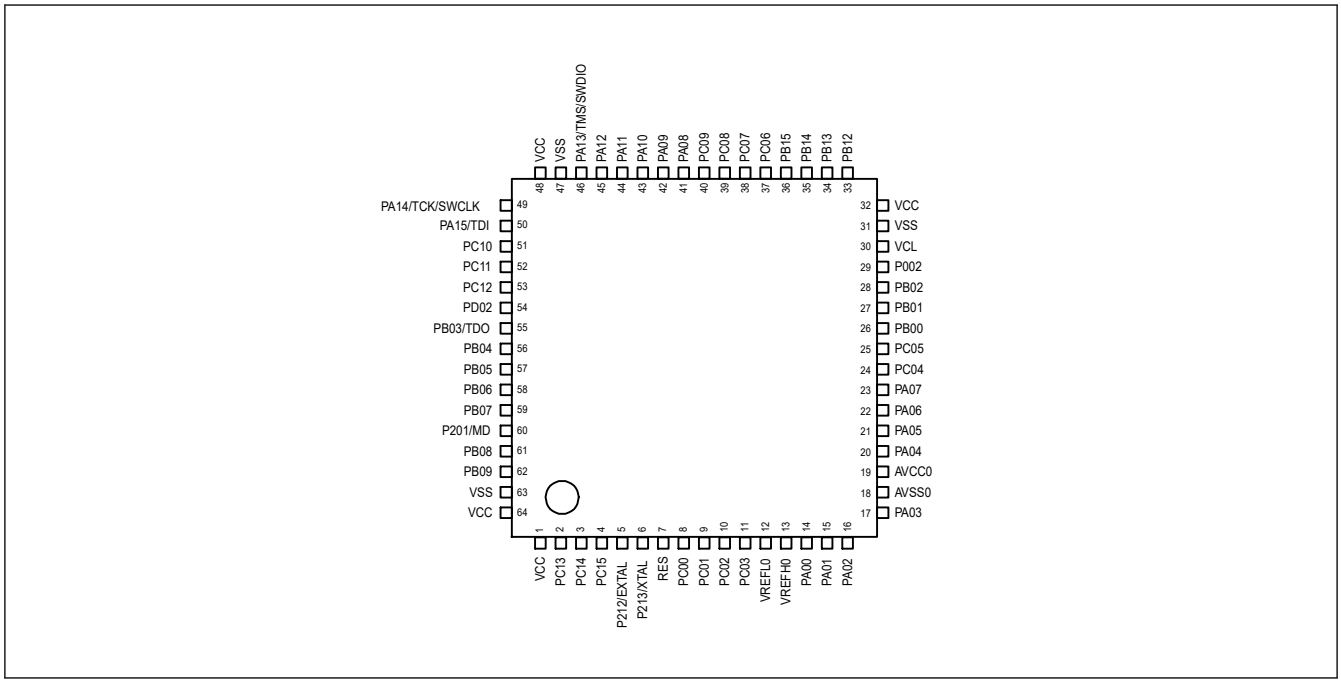


Figure 1.4 Pin assignment for LQFP 64-pin

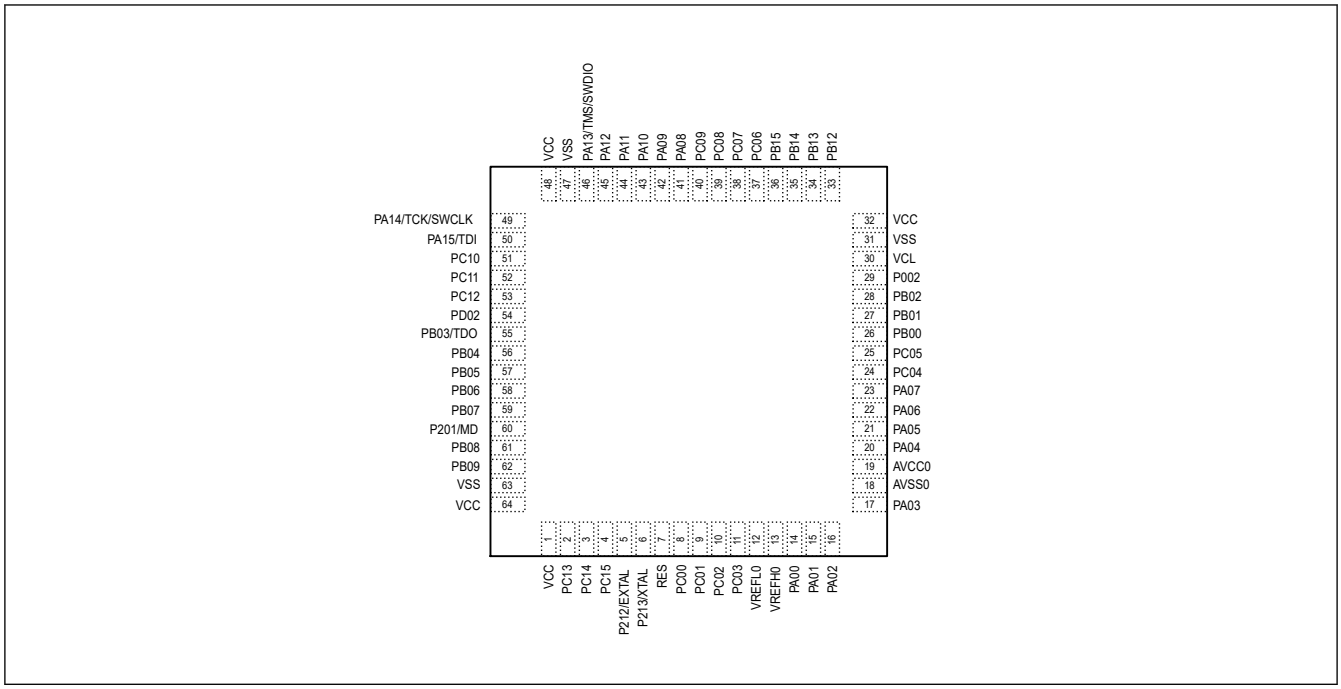


Figure 1.5 Pin assignment for QFN 64-pin

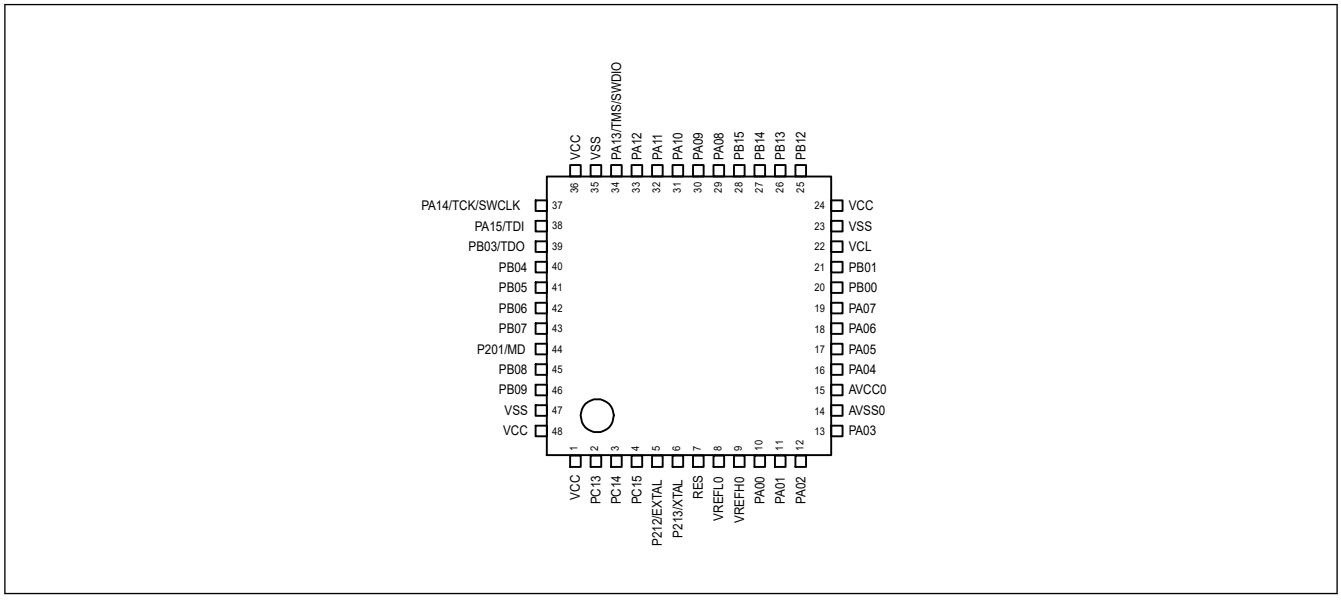


Figure 1.6 Pin assignment for LQFP 48-pin

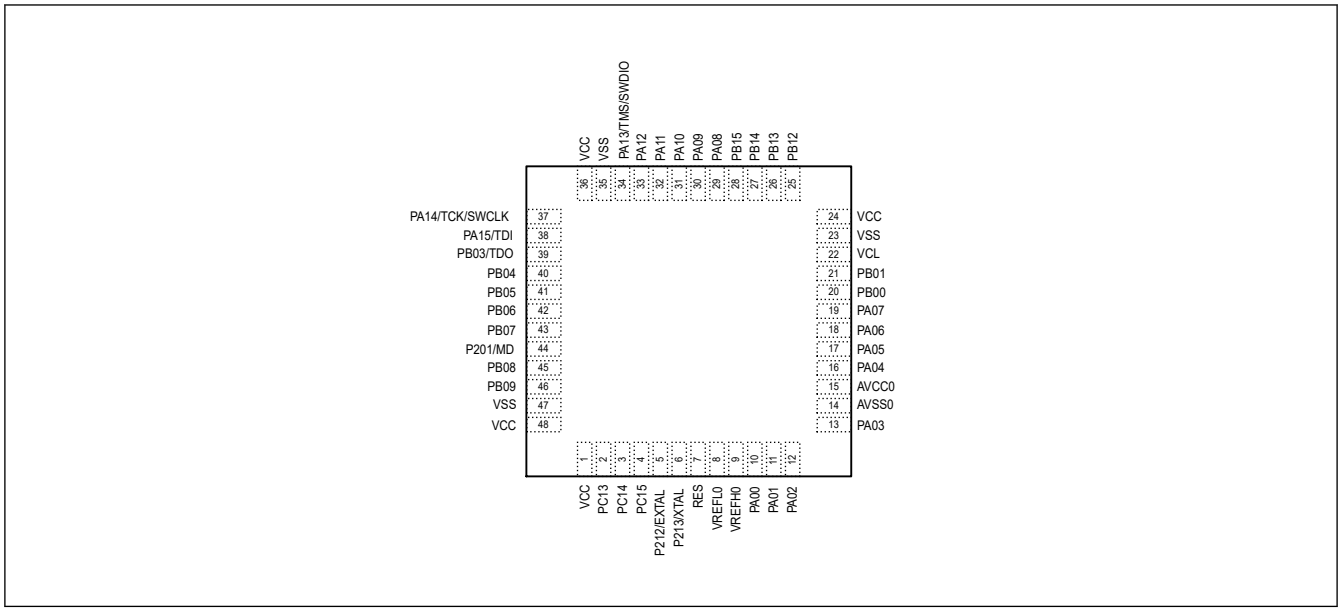


Figure 1.7 Pin assignment for QFN 48-pin

1.7 Pin Lists

Table 1.14 Pin list (1 of 3)

LQFP100	LQFP64, QFN64	LQFP48, QFN48	Power, System, Clock, Debug, CAC	I/O ports	Ex. Interrupt/KINT	SCI/IIC/SPI/CANFD	GPT/AGT	ADC/DAC12/ACMPHS
1	—	—	CLKOUT/TCLK	PE02	—	SCK0_B/DE0/SCK3_A/DE3/RSPCKB_C	GTOVLO/GTIOC7B/GTIOC8A	CMPOUT0
2	—	—	TDATA0	PE03	—	RXD0_B/MISO0_B/SCL0/CTS3_A/SSLB0_C	GTOWLO/GTIOC8A/GTIOC9A	CMPOUT1
3	—	—	TDATA1	PE04	—	TXD0_B/MOSI0_B/SDA0/CTS3_RTS3/SS3_A/DE3/ SSLB1_C	GTOUUP/GTIOC8B/GTIOC7B	CMPOUT2
4	—	—	TDATA2	PE05	—	CTS0_RTS0/SS0_B/DE0/RXD3_A/MISO3_A/SCL3/ MISOB_C	GTOVUP/GTIOC9A/GTIOC8B/ GTCPPO2	CMPOUT3
5	—	—	TDATA3	PE06	—	CTS0_B/TXD3_A/MOSI3_A/SDA3/MOSIB_C	GTOWUP/GTIOC9B/GTCPPO3	—
6	1	1	VCC	—	—	—	—	—
7	2	2	—	PC13	NMI	—	GTETRGD	—
8	3	3	—	PC14	IRQ14	—	GTETRGA/GTIOC3A/GTCPPO0/ GTADSM0/GTCPPO4/AGTIO0	ADTRG0/CMPOUT012
9	4	4	—	PC15	IRQ15	—	GTETRGB/GTIOC3B/GTCPPO1/ GTADSM1/GTCPPO7/AGTIO1	ADTRG1/CMPOUT3
10	—	—	VSS	—	—	—	—	—
11	—	—	VCC	—	—	—	—	—
12	5	5	EXTAL	P212	—	—	—	—
13	6	6	XTAL	P213	IRQ0	—	—	—
14	7	7	RES	—	—	—	—	—
15	8	—	—	PC00	IRQ11-DS	—	—	AN012/PGAOUT0/IVCMP00
16	9	—	—	PC01	IRQ12-DS	—	—	AN013/PGAOUT1/IVCMP10
17	10	—	—	PC02	IRQ13-DS	—	—	AN014/PGAOUT2/IVCMP20
18	11	—	—	PC03	IRQ14-DS	—	—	AN015/PGAOUT3/IVCMP30
19	—	—	—	P000	IRQ0	—	—	AN016/IVREF0
20	12	8	VREFL0	—	—	—	—	—
21	13	9	VREFH0	—	—	—	—	—
22	—	—	—	P001	IRQ2	—	—	AN017/IVREF1
23	14	10	—	PA00	IRQ0-DS	—	—	AN000/PGAIN0/IVCMP02/ IVCMP03
24	15	11	—	PA01	IRQ1	—	—	AN001/PGAVSS0
25	16	12	—	PA02	IRQ2	—	—	AN002/PGAIN1/IVCMP12/ IVCMP13
26	17	13	—	PA03	IRQ3	—	—	AN003/PGAVSS1
27	18	14	AVSS0	—	—	—	—	—
28	19	15	AVCC0	—	—	—	—	—
29	20	16	—	PA04	IRQ4	—	—	AN004/PGAIN2/IVCMP22/ IVCMP23
30	21	17	—	PA05	IRQ5	—	—	AN005/PGAVSS2
31	22	18	—	PA06	IRQ6	—	—	AN006/DA0
32	23	19	—	PA07	IRQ7	—	—	AN007/DA1
33	24	—	—	PC04	IRQ10	—	—	AN010/DA2
34	25	—	—	PC05	IRQ11	—	—	AN011/DA3
35	26	20	—	PB00	IRQ0	—	—	AN008/PGAOUT0/PGAOUT2
36	27	21	—	PB01	IRQ1	—	—	AN009/PGAOUT1/PGAOUT3
37	28	—	—	PB02	IRQ15-DS	—	—	AN018/PGAIN3/IVCMP32/ IVCMP33
38	29	—	—	P002	—	—	—	AN019/PGAVSS3
39	—	—	—	PE08	KR00	SSLA3_C	GTIV/GTIOC3A/GTETRGC/ GTADSM0	AN020/ADTRG0/ CMPOUT012
40	—	—	CACREF	PE09	KR01	SSLA2_C	GTIW/GTIOC3B/GTETRGD/ GTADSM1	AN021/ADTRG1/CMPOUT3
41	—	—	—	PE10	KR02	SSLA1_C	GTOULO/GTIOC2A/GTIOC4A/ GTIOC7A	AN022

Table 1.14 Pin list (2 of 3)

LQFP100	LQFP64, QFN64	LQFP48, QFN48	Power, System, Clock, Debug, CAC	I/O ports	Ex. Interrupt/KINT	SCI/IIC/SPI/CANFD	GPT/AGT	ADC/DAC12/ACMPHS
42	—	—	—	PE11	KR03	SSLA0_C	GTOUUP/GTIOC2B/GTIOC5A/ GTIOC8A	AN023
43	—	—	—	PE12	KR04	RSPCKA_C	GTOVLO/GTIOC1A/GTIOC6A/ GTIOC9A	AN024
44	—	—	—	PE13	KR05	MISOA_C	GTOVUP/GTIOC1B/GTIOC4B/ GTIOC7B	AN025
45	—	—	—	PE14	KR06	MOSIA_C	GTOWLO/GTIOC0A/GTIOC5B/ GTIOC8B	AN026
46	—	—	—	PE15	KR07	RXD4_A/MISO4_A/SCL4	GTOWUP/GTIOC0B/GTIOC6B/ GTIOC9B	AN027
47	—	—	CACREF/VCOUT	PB10	IRQ10-DS	TXD4_A/MOSI4_A/SDA4/CTS3_B	GTIU/GTETRGA/GTETRGB/ GTCPPO4/GTCPPO7	AN028
48	30	22	VCL	—	—	—	—	—
49	31	23	VSS	—	—	—	—	—
50	32	24	VCC	—	—	—	—	—
51	33	25	—	PB12	IRQ2	SCK4_A/DE4/RXD3_B/MISO3_B/SCL3/SSLB0_A/ CRX0	GTETRGA/GTIOC0A/GTIOC4A	ADTRG0
52	34	26	—	PB13	IRQ3	CTS4_A/TXD3_B/MOSI3_B/SDA3/RSPCKB_A/CTX0	GTOULO/GTIOC0B/GTIOC7A/ GTIOC5A	—
53	35	27	—	PB14	IRQ4	CTS4_RTS4/SS4_A/DE4/SCK3_B/DE3/SDA0_C/ MISOB_A	GTOVLO/GTIOC1A/GTIOC8A/ GTIOC6A	—
54	36	28	—	PB15	IRQ5	RXD4_A/MISO4_A/SCL4/CTS3_RTS3/SS3_B/DE3/ SCL0_C/MOSIB_A	GTOWLO/GTIOC1B/GTIOC9A/ GTIOC4B	—
55	—	—	—	PD08	KR00	CTS2_B/TXD1_A/MOSI1_A/SDA1/SSLB1_A	GTIOC2A	—
56	—	—	—	PD09	KR01	CTS2_RTS2/SS2_B/DE2/RXD1_A/MISO1_A/SCL1/ SSLB2_A	GTIOC2B	—
57	—	—	—	PD10	KR02	SCK2_C/DE2/SCK1_A/DE1/SSLB3_A	GTETRGC/GTIOC3A	—
58	—	—	—	PD11	KR03	RXD2_C/MISO2_C/SCL2/CTS1_A	GTIOC3B	—
59	—	—	—	PD12	IRQ12/KR04	TXD2_C/MOSI2_C/SDA2/CTS1_RTS1/SS1_A/DE1/ SCL1_D	GTIOC4A	—
60	—	—	—	PD13	IRQ13/KR05	SCK4_C/DE4/SCK9_C/DE9/SDA1_D	GTIOC4B	—
61	—	—	—	PD14	IRQ14/KR06	RXD4_C/MISO4_C/SCL4/RXD9_C/MISO9_C/SCL9/ SCL0_F	GTIOC5A	—
62	—	—	—	PD15	IRQ15/KR07	TXD4_C/MOSI4_C/SDA4/TXD9_C/MOSI9_C/ SDA9/DE9/SDA0_F	GTIOC5B	—
63	37	—	—	PC06	IRQ6	TXD2_B/MOSI2_B/SDA2/CTS9_RTS9/SS9_C/DE9/ SCL1_E	GTETRGD/GTIOC6A/GTIOC5B/ AGTO0	—
64	38	—	—	PC07	IRQ7	RXD2_B/MISO2_B/SCL2/CTS9_C/SDA1_E	GTETRGA/GTIOC6B/AGTEE0	—
65	39	—	CACREF	PC08	IRQ8	SCK2_B/DE2/CTS3_RTS3/SS3_C/DE3/SCL0_E/ SSLA3_B	GTIV/GTIOC7A/AGTOA0	—
66	40	—	CLKOUT	PC09	IRQ9	CTS2_RTS2/SS2_B/DE2/CTS3_C/SDA0_D/SDA0_E/ SSLA2_B	GTIW/GTIOC7B/GTIOC8A/AGTOB0	—
67	41	29	CLKOUT	PA08	IRQ8/KR00	SCK0_A/DE0/SCK1_C/DE1/SCL0_D/SSLA1_B	GTOUUP/GTIOC8A/GTIOC7B/ GTIOC2A/GTIOC9A/AGTIO0	CMPOUT2
68	42	30	—	PA09	IRQ9/KR01	TXD0_A/MOSI0_A/SDA0/SCL1_C/SSLA0_B	GTOVUP/GTIOC8B/GTIOC8B/ GTIOC2B/GTIOC7B	CMPOUT3
69	43	31	—	PA10	IRQ10/KR02	RXD0_A/MISO0_A/SCL0/SDA1_C/RSPCKA_B	GTOWUP/GTIOC9A/GTIOC9B/ GTIOC3A/GTIOC8B	CMPOUT0
70	44	32	—	PA11	IRQ11/KR03	CTS0_A/RXD1_C/MISO1_C/SCL1/MOSIA_B/CTX0	GTETRGD/GTIOC9B/GTETRGC/ GTIOC3B	CMPOUT1
71	45	33	CACREF	PA12	IRQ12/KR04	CTS0_RTS0/SS0_A/DE0/TXD1_C/MOSI1_C/SDA1/ MISOA_B/CRX0	GTETRGB/GTCPPO0/GTCPPO2/ GTADSM0/GTCPPO7	ADTRG1
72	46	34	TMS/SWDIO	PA13	—	SCK0_C/DE0/CTS1_RTS1/SS1_C/DE1	AGTO0	—
73	—	—	VCL	—	—	—	—	—
74	47	35	VSS	—	—	—	—	—
75	48	36	VCC	—	—	—	—	—
76	49	37	TCK/SWCLK	PA14	—	TXD0_C/MOSI0_C/SDA0/SCK9_B/DE9	AGTO1	—
77	50	38	TDI	PA15	IRQ1/KR02	RXD0_C/MISO0_C/SCL0/RXD9_B/MISO9_B/SCL9/ SSLA0_A	GTETRGB/GTADSM1/GTCPPO4	ADTRG0/CMPOUT012
78	51	—	—	PC10	IRQ6-DS/KR05	TXD1_B/MOSI1_B/SDA1/SCL0_B/RSPCKB_B	AGTIO1	CMPOUT0

Table 1.14 Pin list (3 of 3)

LQFP100	LQFP64, QFN64	LQFP48, QFN48	Power, System, Clock, Debug, CAC	I/O ports	Ex. Interrupt/KINT	SCI/IIC/SPI/CANFD	GPT/AGT	ADC/DAC12/ACMPHS
79	52	—	—	PC11	IRQ7-DS/KR06	RXD1_B/MISO1_B/SCL1/SDA0_B/MISOB_B	AGTOA1	CMPOUT1
80	53	—	—	PC12	IRQ8-DS/KR07	TXD4_B/MOSI4_B/SDA4/SCK1_B/DE1/MOSIB_B	AGTOB1	CMPOUT2
81	—	—	—	PD00	KR00	CTS2_A/RXD3_C/MISO3_C/SCL3/SSLB0_B/CRX0	GTADSM0/GTCPPO4	—
82	—	—	—	PD01	KR01	CTS2_RTS2/SS2_A/DE2/TXD3_C/MOSI3_C/SDA3/ SSLB1_B/CTX0	GTADSM1/GTCPPO7	—
83	54	—	CLKOUT	PD02	IRQ9-DS/KR02	RXD4_B/MISO4_B/SCL4/SCK3_C/DE3	GTCPPO0/GTCPPO2/AGTEE1	CMPOUT3
84	—	—	—	PD03	KR03	SCK4_B/DE4/CTS9_A/SSLB2_B	GTCPPO0	CMPOUT0
85	—	—	—	PD04	KR04	CTS4_RTS4/SS4_B/DE4/CTS9_RTS9/SS9_A/DE9/ SSLB3_B	GTCPPO1	CMPOUT1
86	—	—	—	PD05	KR05	TXD9_A/MOSI9_A/SDA9/SDA1_B/SSLA3_A	GTADSM0/GTCPPO3	—
87	—	—	—	PD06	KR06	RXD9_A/MISO9_A/SCL9/SCL1_B/SSLA2_A	GTCPPO4	—
88	—	—	—	PD07	KR07	SCK9_A/DE9/SSLA1_A	GTADSM1/GTCPPO7	—
89	55	39	TDO/SWO	PB03	IRQ0/KR03	TXD2_A/MOSI2_A/SDA2/TXD9_B/MOSI9_B/SDA9/ RSPCKA_A/CRX0	GTIOC4A/GTCPPO1/GTCPPO3/ AGTO1	ADTRG1/CMPOUT3
90	56	40	CACREF/VCOUT	PB04	IRQ13/KR04	RXD2_A/MISO2_A/SCL2/RXD3_D/MISO3_D/SCL3/ MISOA_A/CTX0	GTIOC4A/GTIOC5A/GTIOC0A/ AGTOA0	—
91	57	41	—	PB05	IRQ3-DS/KR05	SCK2_A/DE2/TXD3_D/MOSI3_D/SDA3/MOSIA_A/ CRX0	GTIU/GTIOC4B/GTIOC6A/GTIOC0B/ AGTOB0	—
92	58	42	—	PB06	IRQ4-DS/KR06	TXD0_D/MOSI0_D/SDA0/CTS3_RTS3/SS3_D/DE3/ SCL0_A/CTX0	GTIV/GTIOC5A/GTIOC4B/GTIOC1A/ AGTOA1	—
93	59	43	—	PB07	IRQ5-DS/KR07	RXD0_D/MISO0_D/SCL0/CTS1_RTS1/SS1_D/DE1/ SDA0_A	GTIW/GTIOC5B/GTETRGC/ GTIOC1B/AGTOB1	—
94	60	44	MD	P201	—	—	—	—
95	61	45	—	PB08	IRQ1-DS/KR00	RXD4/MISO4_C/SCL4/RXD1_D/MISO1_D/SCL1/ SCL1_A/CRX0	GTIOC6A/GTIOC5B/GTIOC2A/ AGTIO0	—
96	62	46	—	PB09	IRQ2-DS/KR01	TXD4/MOSI4_C/SDA4/TXD1_D/MOSI1_D/SDA1/ SDA1_A/CTX0	GTIOC6B/GTIOC2B/AGTIO1	—
97	—	—	CACREF	PE00	—	TXD0_E/MOSI0_E/SDA0/TXD9_D/MOSI9_D/SDA9/ SSLB3_C	GTETRGA/GTIOC4A/GTADSM0/ AGTEE0	ADTRG0
98	—	—	—	PE01	—	RXD0_E/MISO0_E/SCL0/RXD9_D/MISO9_D/SCL9/ SSLB2_C	GTOULO/GTIOC7A/GTIOC4B/ GTADSM1/AGTEE1	ADTRG1
99	63	47	VSS	—	—	—	—	—
100	64	48	VCC	—	—	—	—	—

Note: Several pin names have the added suffix of _A, _B, _C, _D, _E and _F. The suffix can be ignored when assigning functionality.

2. Electrical Characteristics

Unless otherwise specified, minimum and maximum values are guaranteed by either design simulation, characterization results or test in production.

Supported peripheral functions and pins differ from one product name to another.

Unless otherwise specified, the electrical characteristics of the MCU are defined under the following conditions:

- VCC = AVCC0 = 2.7 to 3.6 V
- 2.7 V ≤ VREFH0 ≤ AVCC0
- VSS = AVSS0 = VREFL0 = 0 V
- $T_a = T_{opr}$

Figure 2.1 shows the timing conditions.

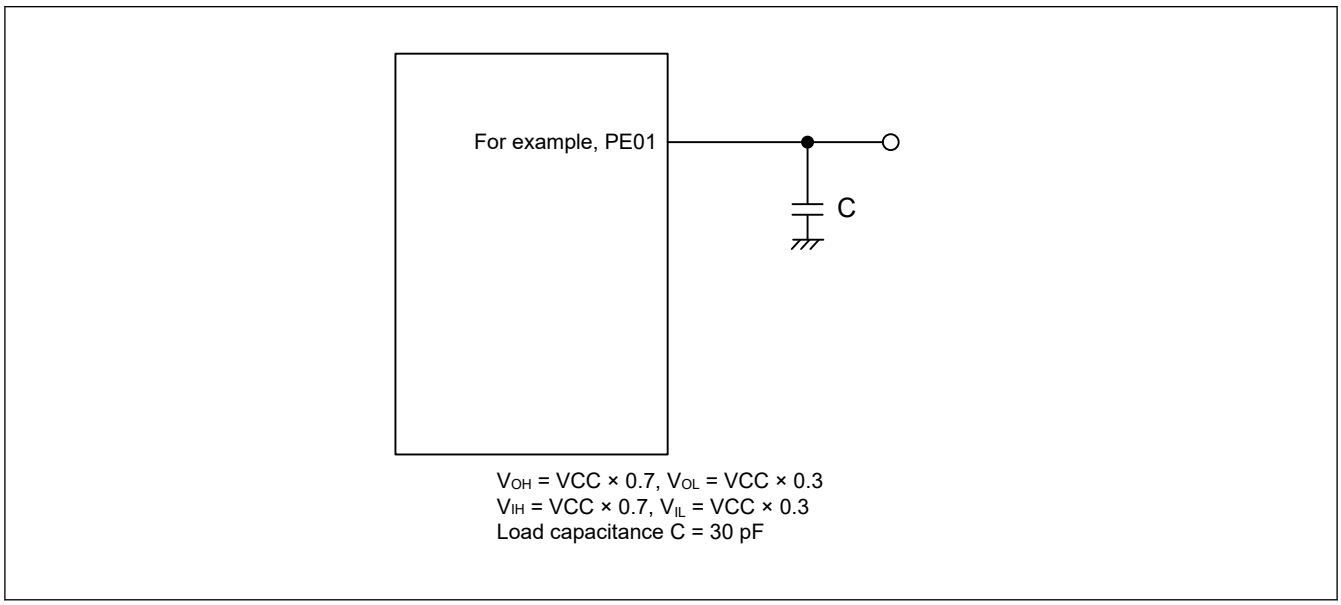


Figure 2.1 Input or output timing measurement conditions

The recommended measurement conditions for the timing specification of each peripheral provided are for the best peripheral operation. Make sure to adjust the driving abilities of each pin to meet your conditions.

2.1 Absolute Maximum Ratings

Table 2.1 Absolute maximum ratings (1 of 2)

Parameter	Symbol	Value	Unit
Power supply voltage	VCC	–0.3 to +4.0	V
Input voltage (except for 5 V-tolerant ports*1)	V_{in}	–0.3 to VCC + 0.3	V
Input voltage (5 V-tolerant ports*1)	V_{in}	–0.3 to VCC + 4.0 (max. 5.8)	V
Reference power supply voltage	VREFH0	–0.3 to VCC + 0.3	V
Analog power supply voltage	AVCC0*2	–0.3 to +4.0	V
Analog input voltage (except for PA00 to PA05, PB02, P002)	V_{AN}	–0.3 to AVCC0 + 0.3	V
Analog input voltage (PA00 to PA05, PB02, P002) when PGA differential input is disabled	V_{AN}	–0.3 to AVCC0 + 0.3	V
Analog input voltage (PA00, PA02, PA04, PB02) when PGA differential input is enabled	V_{AN}	–1.3 to AVCC0 + 0.3	V

Table 2.1 Absolute maximum ratings (2 of 2)

Parameter	Symbol	Value	Unit
Analog input voltage (PA01, PA03, PA05, P002) when PGA differential input is enabled	V_{AN}	–0.8 to AVCC0 + 0.3	V
Operating temperature*3 *4	T_{opr}	–40 to +105	°C
Storage temperature	T_{stg}	–55 to +125	°C

Note 1. Ports PA12 to PA15, PB03, PB05 to PB09, PC10 to PC12, PC14, PC15, PD00 to PD07, PE00, and PE01 are 5 V tolerant.
Note 2. Connect AVCC0 to VCC.
Note 3. See section 2.2.1. Tj/Ta Definition.
Note 4. Contact a Renesas Electronics sales office for information on derating operation when Ta = +85°C to +105°C. Derating is the systematic reduction of load for improved reliability.

Caution: Permanent damage to the MCU might result if absolute maximum ratings are exceeded.

Table 2.2 Recommended operating conditions

Parameter	Symbol	Min	Typ	Max	Unit
Power supply voltages	VCC	2.7	—	3.6	V
	VSS	—	0	—	V
Analog power supply voltages	AVCC0*1	—	VCC	—	V
	AVSS0	—	0	—	V

Note 1. Connect AVCC0 to VCC. When the A/D converter and the D/A converter are not in use, do not leave the AVCC0, VREFH0, AVSS0, and VREFL0 pins open. Connect the AVCC0 and VREFH0 pins to VCC, and the AVSS0 and VREFL0 pins to VSS, respectively.

2.2 DC Characteristics

2.2.1 Tj/Ta Definition

Table 2.3 DC characteristics

Parameter	Symbol	Typ	Max	Unit	Test conditions
Permissible junction temperature	T_j	—	125	°C	High-speed mode Low-speed mode

Note: Make sure that $T_j = T_a + \theta ja \times$ total power consumption (W), where total power consumption = $(VCC - V_{OH}) \times \Sigma I_{OH} + V_{OL} \times \Sigma I_{OL} + I_{CC}max \times VCC$.

2.2.2 I/O V_{IH}, V_{IL}

Table 2.4 I/O V_{IH}, V_{IL}

Parameter			Symbol	Min	Typ	Max	Unit
Input voltage (except for Schmitt trigger input pins)	Peripheral function pin	EXTAL (external clock input), SPI (except RSPCK)	V_{IH}	VCC × 0.8	—	—	V
			V_{IL}	—	—	VCC × 0.2	
		IIC (SMBus)*1	V_{IH}	2.1	—	—	
			V_{IL}	—	—	0.8	
		IIC (SMBus)*2	V_{IH}	2.1	—	VCC + 3.6 (max 5.8)	
			V_{IL}	—	—	0.8	
Schmitt trigger input voltage	Peripheral function pin	IIC (Except for SMBus)*1	V_{IH}	VCC × 0.7	—	—	
			V_{IL}	—	—	VCC × 0.3	
			ΔV_T	VCC × 0.05	—	—	
		IIC (Except for SMBus)*2	V_{IH}	VCC × 0.7	—	VCC + 3.6 (max 5.8)	
			V_{IL}	—	—	VCC × 0.3	
			ΔV_T	VCC × 0.05	—	—	
		5 V-tolerant ports*3 *7	V_{IH}	VCC × 0.8	—	VCC + 3.6 (max 5.8)	
			V_{IL}	—	—	VCC × 0.2	
			ΔV_T	VCC × 0.05	—	—	
		Other input pins*4	V_{IH}	VCC × 0.8	—	—	
			V_{IL}	—	—	VCC × 0.2	
			ΔV_T	VCC × 0.05	—	—	
	Ports	5 V-tolerant ports*5 *7	V_{IH}	VCC × 0.8	—	VCC + 3.6 (max 5.8)	
			V_{IL}	—	—	VCC × 0.2	
			ΔV_T	VCC × 0.05	—	—	
		Other input pins*6	V_{IH}	VCC × 0.8	—	—	
			V_{IL}	—	—	VCC × 0.2	
			ΔV_T	VCC × 0.05	—	—	

Note 1. SCL0_C, SDA0_C, SCL0_D, SDA0_D, SCL0_E, SDA0_E, SCL0_F, SDA0_F, SCL1_C, SDA1_C, SCL1_D, SDA1_D, SCL1_E, SDA1_E (total 14 pins). This is the value when IIC function is selected.
Note 2. SCL0_A, SDA0_A, SCL0_B, SDA0_B, SCL1_A, SDA1_A, SCL1_B, SDA1_B (total 8 pins). This is the value when IIC function is selected.
Note 3. RES and peripheral function pins associated with PA12 to PA15, PB03, PB05 to PB09, PC10 to PC12, PC14, PC15, PD00 to PD07, PE00, and PE01 (total 26 pins).
Note 4. All input pins except for the peripheral function pins already described in the table.
Note 5. PA12 to PA15, PB03, PB05 to PB09, PC10 to PC12, PC14, PC15, PD00 to PD07, PE00, and PE01 (total 25 pins).
Note 6. All input pins except for the ports already described in the table.
Note 7. When VCC is less than 2.7 V, the input voltage of 5 V-tolerant ports should be less than 3.6 V, otherwise breakdown may occur because 5 V-tolerant ports are electrically controlled so as not to violate the break down voltage.

2.2.3 I/O I_{OH}, I_{OL}

Table 2.5 I/O I_{OH}, I_{OL}

Parameter			Symbol	Min	Typ	Max	Unit
Permissible output current (average value per pin)	IIC pins	Standard mode*1	I_{OL}	—	—	3.0	mA
		Fast mode*1	I_{OL}	—	—	6.0	mA
		Fast mode plus*2	I_{OL}	—	—	20	mA
		High speed mode*2	I_{OL}	—	—	3.0	mA
	Other output pins*3	Low drive*4	I_{OH}	—	—	–2.0	mA
			I_{OL}	—	—	2.0	mA
		Middle drive*5	I_{OH}	—	—	–4.0	mA
			I_{OL}	—	—	4.0	mA
		High drive*6	I_{OH}	—	—	–10	mA
			I_{OL}	—	—	10	mA
		High speed high drive*7	I_{OH}	—	—	–10	mA
			I_{OL}	—	—	10	mA
		High current drive*8	I_{OH}	—	—	–10	mA
			I_{OL}	—	—	20	mA
Permissible output current (max value per pin)	IIC pins	Standard mode*1	I_{OL}	—	—	3.0	mA
		Fast mode*1	I_{OL}	—	—	6.0	mA
		Fast mode plus*2	I_{OL}	—	—	20	mA
		High speed mode*2	I_{OL}	—	—	3.0	mA
	Other output pins*3	Low drive*4	I_{OH}	—	—	–2.0	mA
			I_{OL}	—	—	2.0	mA
		Middle drive*5	I_{OH}	—	—	–4.0	mA
			I_{OL}	—	—	4.0	mA
		High drive*6	I_{OH}	—	—	–16	mA
			I_{OL}	—	—	16	mA
		High speed high drive*7	I_{OH}	—	—	–16	mA
			I_{OL}	—	—	16	mA
		High current drive*8	I_{OH}	—	—	–16	mA
			I_{OL}	—	—	20	mA
Permissible output current (max value of total of all pins)	Maximum of all output pins		ΣI_{OH} (max)	—	—	–80	mA
			ΣI_{OL} (max)	—	—	80	mA

Note 1. SCL0_A, SDA0_A, SCL1_A, SDA1_A (total 4 pins). This is the value when IIC function is selected.
Note 2. SCL0_A, SDA0_A (total 2 pins). This is the value when IIC function is selected.
Note 3. Except for P000 to P002, PA00 to PA07, PB00 to PB02, PC00 to PC05, PC13, which are input ports.
Note 4. This is the value when low driving ability is selected in the Port Drive Capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.
Note 5. This is the value when middle driving ability is selected in the Port Drive Capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.
Note 6. This is the value when high driving ability is selected in the Port Drive Capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.

Note 7. This is the value when high speed high driving ability is selected in the Port Drive Capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.
Note 8. This is the value when high current driving ability is selected in the Port Drive Capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.

Caution: To protect the reliability of the MCU, the output current values should not exceed the values in this table. The average output current indicates the average value of current measured during 100 µs.

2.2.4 I/O V_{OH}, V_{OL}, and Other Characteristics

Table 2.6 I/O V_{OH}, V_{OL}, and other characteristics

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Output voltage	IIC*1	V_{OL}	—	—	0.4	V	I_{OL} = 3.0 mA
		V_{OL}	—	—	0.6		I_{OL} = 6.0 mA
	IIC*2	V_{OL}	—	—	0.4		I_{OL} = 15.0 mA (BFCTL.FMPE = 1)
		V_{OL}	—	0.4	—		I_{OL} = 20.0 mA (BFCTL.FMPE = 1)
		V_{OL}	—	—	0.4		I_{OL} = 3.0 mA (BFCTL.HSME = 1)
	Ports PA08 to PA11, PB12 to PB15, PC06 to PC09, PD08 to PD15, PE10 to PE15*3	V_{OH}	VCC – 0.5	—	—		I_{OH} = –1.0 mA
		V_{OL}	—	—	0.6		I_{OL} = 20 mA
	Other output pins	V_{OH}	VCC – 0.5	—	—		I_{OH} = –1.0 mA
		V_{OL}	—	—	0.5		I_{OL} = 1.0 mA
Input leakage current	RES	$\|I_{in}\|$	—	—	5.0	µA	V_{in} = 0 V V_{in} = 5.5 V
	Port P000, P001, PA06, PA07, PB00, PB01, PC00 to PC05, PC13		—	—	1.0		V_{in} = 0 V V_{in} = VCC
	Port PA00, PA02, PA04, PB02 (PGA input pins)		—	—	1.0		V_{in} = 0 V V_{in} = VCC
	Port PA01, PA03, PA05, P002 (PGAVSS pins)*4		—	—	1.0		V_{in} = 0 V V_{in} = VCC
Three-state leakage current (off state)	5 V-tolerant ports	$\|I_{TSI}\|$	—	—	5.0	µA	V_{in} = 0 V V_{in} = 5.5 V
	Other ports (except for input ports)		—	—	1.0		V_{in} = 0 V V_{in} = VCC
Input pull-up MOS current	Ports P0, P2, PA to PE (except for ports P002, PA00 to PA05, PB02)	I_p	–300	—	–10	µA	VCC = 2.7 to 3.6 V V_{in} = 0 V
Pull-up current serving as the SCL current source	IIC*5	I_{CS}	3	—	12	mA	VCC = 3.0 to 3.6 V V_{in} = 0.3 × VCC to 0.7 × VCC
Input capacitance	All input pins	C_{in}	—	—	8	pF	Vbias = 0 V Vamp = 20 mV f = 1 MHz Ta = 25°C

Note 1. SCL0_A, SDA0_A, SCL1_A, SDA1_A (total 4 pins). This is the value when IIC function is selected.
Note 2. SCL0_A, SDA0_A (total 2 pins). This is the value when IIC function is selected.
Note 3. This is the value when high current driving ability is selected in the Port Drive Capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.
Note 4. This is the value when the pseudo-differential input on the PGAn pin is disabled (single-ended input).
Note 5. SCL0_A (1 pin). This is the value when IIC high speed mode is selected.

2.2.5 Operating and Standby Current

Table 2.7 Operating and standby current

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions
Supply current[*1]	High-speed mode	Maximum[*2]		I_{CC}[*3]	—	—	150	mA	ICLK = 240 MHz PCLKA = 120 MHz PCLKB = 60 MHz PCLKC = 60 MHz PCLKD = 120 MHz FCLK = 60 MHz
		CoreMark®[*5] [*6]			—	34	—		
		Normal mode	All peripheral clocks enabled, while (1) code executing from flash[*4]		—	44	—		
			All peripheral clocks disabled, while (1) code executing from flash[*5] [*6]		—	28	—		
		Sleep mode[*5] [*6]			—	13	78		
		Increase during BGO operation	Data flash P/E		—	6	—		
			Code flash P/E		—	8	—		
	Low-speed mode[*5] [*10]				—	5	—		ICLK = 1 MHz
	Software Standby mode		SNZCR.RXDREQEN = 1		—	—	63		ICLK = 32.768 kHz
			SNZCR.RXDREQEN = 0		—	5.1	—		—
	Deep Software Standby mode	Power supplied to Standby SRAM			—	22.7	60	µA	—
		Power not supplied to SRAM	Power-on reset circuit low power function disabled		—	11.3	30		—
			Power-on reset circuit low power function enabled		—	4.4	20		—
	Inrush current on returning from deep software standby mode		Inrush current[*7]	I_{RUSH}	—	160	—	mA	—
			Energy of inrush current[*7]	E_{RUSH}	—	1.0	—	µC	—
Analog power supply current	During A/D conversion (1unit)		Without SH	AI_{CC}	—	4.9	6.0	mA	—
			With SH		—	8.4	11.5	mA	—
	PGA (1channel)				—	1	3	mA	—
	ACMPHS (1unit)				—	0.1	0.2	mA	—
	Temperature sensor				—	0.1	0.2	mA	—
	During D/A conversion (1channel)[*8]		Without AMP output		—	0.2	0.3	mA	—
			With AMP output		—	0.8	1.3	mA	—
	Waiting for A/D, D/A conversion (all units)				—	3.8	4.5	mA	—
	ADC, DAC12 in standby modes (all units)[*9]				—	0.7	10	µA	—
Reference power supply current (VREFH0)	During A/D conversion (1unit)		SAR mode	AI_{REFH0}	—	21	50	µA	—
			Oversampling mode and Hybrid mode		—	100	160	µA	—
	Waiting for A/D conversion (all units)				—	18	50	µA	—
	ADC in standby modes (all units)[*9]				—	0.03	1	µA	—

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. Measured with clocks supplied to the peripheral functions. This does not include the BGO operation.
Note 3. I_{CC} depends on f (ICLK) as follows.
I_{CC} Max. = 0.34 × f + 67 (max. operation in high-speed mode)
I_{CC} Typ. = 0.095 × f + 4.7 (normal operation in high-speed mode, all peripheral clocks disabled)
I_{CC} Typ. = 0.9 × f + 4.1 (low-speed mode)
I_{CC} Max. = 0.045 × f + 67 (sleep mode)
Note 4. This does not include the BGO operation.
Note 5. Supply of the clock signal to peripherals is stopped in this state. This does not include the BGO operation.
Note 6. FCLK, PCLKA, PCLKB, PCLKC, and PCLKD are set to divided by 64 (3.75 MHz).

Note 7. Reference value
Note 8. The DAC12 includes the Reference current in the analog power supply current.
Note 9. When the MCU is in Software Standby mode or the MSTPCRD.MSTPD16 (A/D Converter Module Stop bit) is in the module-stop state.
Note 10. FCLK, PCLKA, PCLKB, PCLKC, and PCLKD are set to divided by 64 (15.6 kHz).

Table 2.8 Coremark and normal mode current

Parameter			Symbol	Typ	Unit	Test conditions
Supply Current*1	Coremark		I_{CC}	139	µA/MHz	ICLK = 240 MHz PCLKA = PCLKB = PCLKC = PCLKD = FCLK = 3.75 MHz
	Normal mode	All peripheral clocks disabled, cache on, while (1) code executing from flash*2		139		
		All peripheral clocks disabled, cache off, while (1) code executing from flash*2		115		

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. Supply of the clock signal to peripherals is stopped in this state. This does not include the BGO operation.

2.2.6 VCC Rise and Fall Gradient and Ripple Frequency

Table 2.9 VCC rise and fall gradient characteristics

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
VCC rising gradient	Voltage monitor 0 reset disabled at startup	SrVCC	0.0084	—	20	ms/V	—
	Voltage monitor 0 reset enabled at startup		0.0084	—	—		—
	SCI boot mode*1		0.0084	—	20		—
VCC falling gradient		SfVCC	0.0084	—	—	ms/V	—

Note 1. At boot mode, the reset from voltage monitor 0 is disabled regardless of the value of the OFS1.LVDAS bit.

Table 2.10 VCC rising and falling gradient and ripple frequency characteristics

The ripple voltage must meet the allowable ripple frequency $f_{r(VCC)}$ within the range between the VCC upper limit (3.6 V) and lower limit (2.7 V). When the VCC change exceeds VCC ±10%, the allowable voltage change rising and falling gradient dt/dVCC must be met.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Allowable ripple frequency	$f_{r\ (VCC)}$	—	—	10	kHz	Figure 2.2 $V_{r\ (VCC)} \leq VCC \times 0.2$
		—	—	1	MHz	Figure 2.2 $V_{r\ (VCC)} \leq VCC \times 0.08$
		—	—	10	MHz	Figure 2.2 $V_{r\ (VCC)} \leq VCC \times 0.06$
Allowable voltage change rising and falling gradient	dt/dVCC	1.0	—	—	ms/V	When VCC change exceeds VCC ±10%

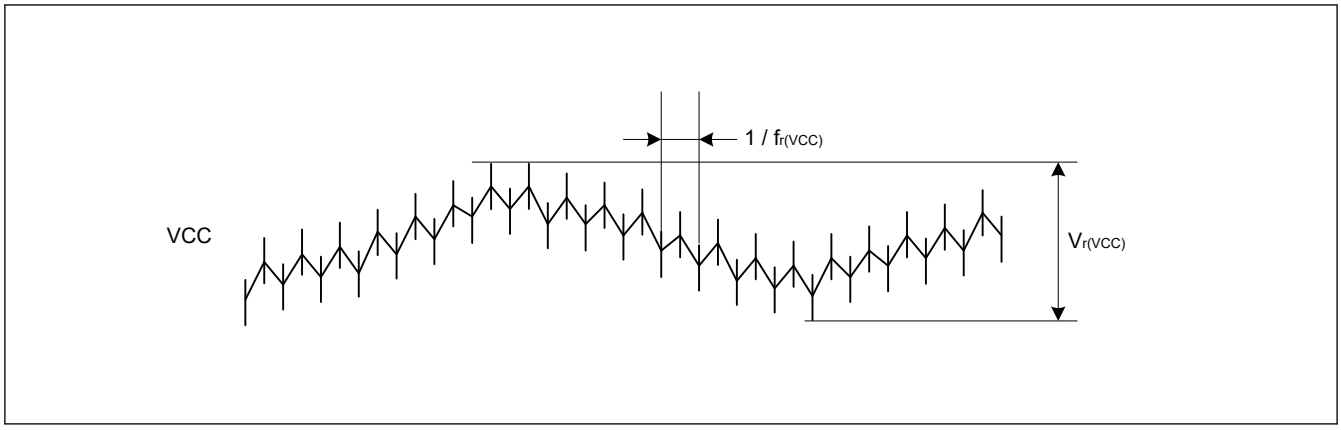


Figure 2.2 Ripple waveform

2.2.7 Thermal Characteristics

Maximum value of junction temperature (Tj) must not exceed the value of section 2.2.1. Tj/Ta Definition.

Tj is calculated by either of the following equations.

- Tj = Ta + θja × Total power consumption
- Tj = Tt + Ψjt × Total power consumption
  - Tj : Junction Temperature (°C)
  - Ta : Ambient Temperature (°C)
  - Tt : Top Center Case Temperature (°C)
  - θja : Thermal Resistance of “Junction”-to-“Ambient” (°C/W)
  - Ψjt : Thermal Resistance of “Junction”-to-“Top Center Case” (°C/W)
- Total power consumption = Voltage × (Leakage current + Dynamic current)
- Leakage current of IO = Σ (I_{OL} × V_{OL}) /Voltage + Σ (|I_{OH}| × |VCC – V_{OH}|) /Voltage
- Dynamic current of IO = Σ IO (C_{in} + C_{load}) × IO switching frequency × Voltage
  - C_{in}: Input capacitance
  - C_{load}: Output capacitance

Regarding θja and Ψjt, see Table 2.11.

Table 2.11 Thermal Resistance

Parameter	Package	Symbol	Value*1	Unit	Test conditions
Thermal Resistance	100-pin LQFP (PLQP0100KB-B)	θja	36	°C/W	JESD 51-2 and 51-7 compliant
	64-pin LQFP (PLQP0064KB-C)		39		
	64-pin QFN (PWQN0064LB-A)		26		
	48-pin LQFP (PLQP0048KB-B)		60		
	48-pin QFN (PWQN0048KC-A)		28		
	100-pin LQFP (PLQP0100KB-B)	Ψjt	0.65	°C/W	JESD 51-2 and 51-7 compliant
	64-pin LQFP (PLQP0064KB-C)		0.69		
	64-pin QFN (PWQN0064LB-A)		0.15		
	48-pin LQFP (PLQP0048KB-B)		2.01		
	48-pin QFN (PWQN0048KC-A)		0.17		

Note 1. The values are reference values when the 4-layer board is used. Thermal resistance depends on the number of layers or size of the board. For details, refer to the JEDEC standards.

2.2.7.1 Calculation guide of ICCmax

Table 2.12 shows the power consumption of each unit.

Table 2.12 Power consumption of each unit

Dynamic current/Leakage current	MCU Domain	Category	Item	Frequency [MHz]	Current [uA/ MHz]	Current*1 [mA]
Leakage current	Analog	LDO and Leak*2	Ta = 75 °C*3	—	—	37.8
			Ta = 85 °C*3	—	—	46.4
			Ta = 95 °C*3	—	—	56.1
			Ta = 105 °C*3	—	—	68.0
Dynamic current	CPU	Operation with Flash and SRAM	Coremark	240	105.324	25.28
	Peripheral Unit	Timer	GPT32 (10ch)*4	120	29.697	3.56
			POEG (4 Groups)*4	60	1.483	0.09
			AGT (2ch)*4	60	3.09	0.19
			WDT	60	0.641	0.04
			IWDT	60	0.225	0.01
		Communication interfaces	SCI (6ch)*4	120	27.683	3.32
			IIC (2ch)*4	120	5.304	0.64
			CANFD	60	5.763	0.35
			SPI (2ch)*4	120	5.738	0.69
		Data processing accelerator	TFU	240	1.188	0.03
			IIRFA	240	34.252	8.22
		Data processing	DOC	120	0.221	0.03
			CRC	120	0.508	0.06
		Analog	ADC (2 Units)*4	60	172.958	10.38
			DAC12 (4ch)*4	120	1.097	0.13
			ACMPHS (4ch)*4	60	0.641	0.04
			TSN	60	0.111	0.01
		Event link	ELC	60	1.852	0.11
		Security	SCE5	120	68.404	8.21
		System	CAC	60	0.63	0.04
			KINT	60	0.072	0.004
		DMA	DMAC	240	5.073	1.22
			DTC	240	4.18	1

Note 1. The values are guaranteed by design.
Note 2. LDO and Leak are internal voltage regulator's current and MCU's leakage current. It is selected according to the temperature of Ta.
Note 3. Δ(Tj-Ta) = 20 °C is considered to measure the current.
Note 4. To determine the current consumption per channel or unit, divide Current [mA] by the number of channels, groups or units.

Table 2.13 Outline of operation for each unit (1 of 2)

Peripheral	Outline of operation
GPT	Operating modes is set to saw-wave PWM mode. GPT is operating with PCLKD.

Table 2.13 Outline of operation for each unit (2 of 2)

Peripheral	Outline of operation
POEG	Only clear module stop bit.
AGT	AGT is operating with PCLKB.
WDT	WDT is operating with PCLKB.
IWDT	IWDT is operating with IWDTCLK.
SCI	SCI is transmitting data in clock synchronous mode.
IIC	Communication format is set to I2C-bus format. IIC is transmitting data in master mode.
CANFD	CANFD is transmitting and receiving data in self-test mode 1.
SPI	SPI mode is set to SPI operation (4-wire method). SPI master/slave mode is set to master mode. SPI is transmitting 8-bit width data.
TFU	Performs sincos operations.
IIRFA	Channel 0 performs 32 stages of channel processing.
DOC	DOC is operating in data addition mode.
CRC	CRC is generating CRC code using 32-bit CRC32-C polynomial.
ADC	Resolution is set to 12-bit accuracy. Conversion Data Operation Control B Register is set to 16 times average mode. ADC is converting the analog input in continuous scan mode. ADC is operating with PCLKC.
DAC12	DAC12 is outputting the conversion result while updating the value of data register.
ACMPHS	Compare between IVCMP2 and IVREF0 and enable compare output.
TSN	TSN is operating.
ELC	Only clear module stop bit.
SCE5	SCE5 is executing built-in self test.
DMAC	Bit length of transfer data is set to 32 bits. Transfer mode is set to block transfer mode. DMAC is transferring data from SRAM0 to SRAM0.
DTC	Bit length of transfer data is set to 32 bits. Transfer mode is set to block transfer mode. DTC is transferring data from SRAM0 to SRAM0.
CAC	Measurement target clocks is set to PCLKB. Measurement reference clocks is set to PCLKB. CAC is measuring the clock frequency accuracy.
KINT	Only clear module stop bit.

2.2.7.2 Example of Tj calculation

Assumption:

- Package 100-pin LQFP: θja = 36.0 °C/W
- Ta = 100 °C
- I_{CC}max = 80 mA
- VCC = 3.5 V (VCC = AVCC0)
- I_{OH} = 1 mA, V_{OH} = VCC – 0.5 V, 12 Outputs
- I_{OL} = 20 mA, V_{OL} = 1.0 V, 8 Outputs
- I_{OL} = 1 mA, V_{OL} = 0.5 V, 12 Outputs
- C_{in} = 8 pF, 16 pins, Input frequency = 10 MHz

- C_{load} = 30 pF, 16 pins, Output frequency = 10 MHz

Leakage current of IO = Σ (V_{OL} × I_{OL}) / Voltage + Σ ((VCC - V_{OH}) × I_{OH}) / Voltage
= (20 mA × 1 V) × 8 / 3.5 V + (1 mA × 0.5 V) × 12 / 3.5 V + ((VCC - (VCC - 0.5 V)) × 1 mA) × 12 / 3.5 V
= 45.7 mA + 1.71 mA + 1.71 mA
= 49.1 mA

Dynamic current of IO = Σ IO (C_{in} + C_{load}) × IO switching frequency × Voltage
= ((8 pF × 16) × 10 MHz + (30 pF × 16) × 10 MHz) × 3.5 V
= 21.3 mA

Total power consumption = Voltage × (Leakage current + Dynamic current)
= (80 mA × 3.5 V) + (49.1 mA + 21.3 mA) × 3.5 V
= 526 mW (0.526 W)

Tj = Ta + θja × Total power consumption
= 100 °C + 36.0 °C/W × 0.526W
= 118.9 °C

2.3 AC Characteristics

2.3.1 Frequency

Table 2.14 Operation frequency value in high-speed mode

Parameter		Symbol	Min	Typ	Max	Unit
Operation frequency	System clock (ICLK)	f	—	—	240	MHz
	Peripheral module clock (PCLKA)		—	—	120	
	Peripheral module clock (PCLKB)		—	—	60	
	Peripheral module clock (PCLKC)		—*2	—	60	
	Peripheral module clock (PCLKD)		—	—	120	
	Flash interface clock (FCLK)		—*1	—	60	

Note 1. FCLK must run at a frequency of at least 4 MHz when programming or erasing the flash memory.
Note 2. When the ADC is used, the PCLKC frequency must be at least 1 MHz.

Table 2.15 Operation frequency value in low-speed mode

Parameter		Symbol	Min	Typ	Max	Unit
Operation frequency	System clock (ICLK)	f	—	—	1	MHz
	Peripheral module clock (PCLKA)		—	—	1	
	Peripheral module clock (PCLKB)		—	—	1	
	Peripheral module clock (PCLKC) *2		—*2	—	1	
	Peripheral module clock (PCLKD)		—	—	1	
	Flash interface clock (FCLK)*1		—	—	1	

Note 1. Programming or erasing the flash memory is disabled in low-speed mode.
Note 2. When the ADC is used, the PCLKC frequency must be set to at least 1 MHz.

2.3.2 Clock Timing

Table 2.16 Clock timing

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
EXTAL external clock input cycle time	t_{EXcyc}	41.66	—	—	ns	Figure 2.3
EXTAL external clock input high pulse width	t_{EXH}	15.83	—	—	ns	
EXTAL external clock input low pulse width	t_{EXL}	15.83	—	—	ns	
EXTAL external clock rise time	t_{EXr}	—	—	5.0	ns	
EXTAL external clock fall time	t_{EXf}	—	—	5.0	ns	
Main clock oscillator frequency	f_{MAIN}	8	—	24	MHz	—
Main clock oscillation stabilization wait time (crystal)*1	$t_{MAINOSCWT}$	—	—	—*1	ms	Figure 2.4
LOCO clock oscillation frequency	f_{LOCO}	29.4912	32.768	36.0448	kHz	—
LOCO clock oscillation stabilization wait time	t_{LOCOWT}	—	—	60.4	µs	Figure 2.5
ILOCO clock oscillation frequency	f_{ILOCO}	13.5	15	16.5	kHz	—
MOCO clock oscillation frequency	F_{MOCO}	6.8	8	9.2	MHz	—
MOCO clock oscillation stabilization wait time	t_{MOCOWT}	—	—	15.0	µs	—
HOCO clock oscillator oscillation frequency	f_{HOCO16}	15.78	16	16.22	MHz	–20 ≤ Ta ≤ 105°C
	f_{HOCO18}	17.75	18	18.25		
	f_{HOCO20}	19.72	20	20.28		
	f_{HOCO16}	15.71	16	16.29		–40 ≤ Ta ≤ –20°C
	f_{HOCO18}	17.68	18	18.32		
	f_{HOCO20}	19.64	20	20.36		
HOCO clock oscillation stabilization wait time*2	t_{HOCOWT}	—	—	64.7	µs	—
HOCO period jitter	—	—	±85	—	ps	—
PLL clock frequency	f_{PLL}	120	—	240	MHz	—
PLL2 clock frequency	f_{PLL2}	120	—	240	MHz	—
PLL/PLL2 clock oscillation stabilization wait time	t_{PLLWT}	—	—	174.9	µs	Figure 2.6
PLL/PLL2 period jitter	—	—	±100	—	ps	—
PLL/PLL2 long term jitter	—	—	±300	—	ps	Term: 1µs, 10µs

Note 1. When setting up the main clock oscillator, ask the oscillator manufacturer for an oscillation evaluation, and use the results as the recommended oscillation stabilization time. Set the MOSCWTCR register to a value equal to or greater than the recommended value.
After changing the setting in the MOSCCR.MOSTP bit to start main clock operation, read the OSCSF.MOSCSF flag to confirm that it is 1, and then start using the main clock oscillator.

Note 2. This is the time from release from reset state until the HOCO oscillation frequency (f_{HOCO}) reaches the range for guaranteed operation.

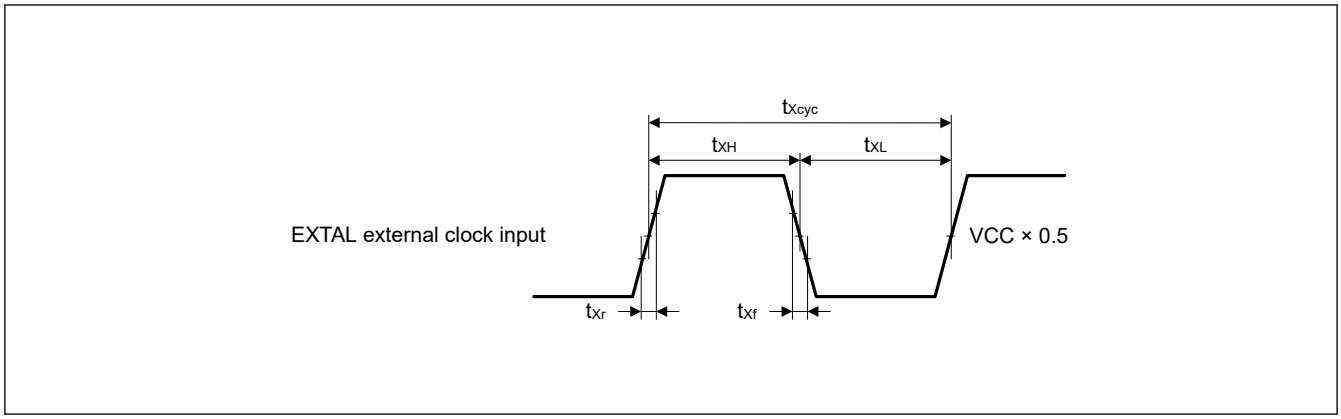


Figure 2.3 EXTAL external clock input timing

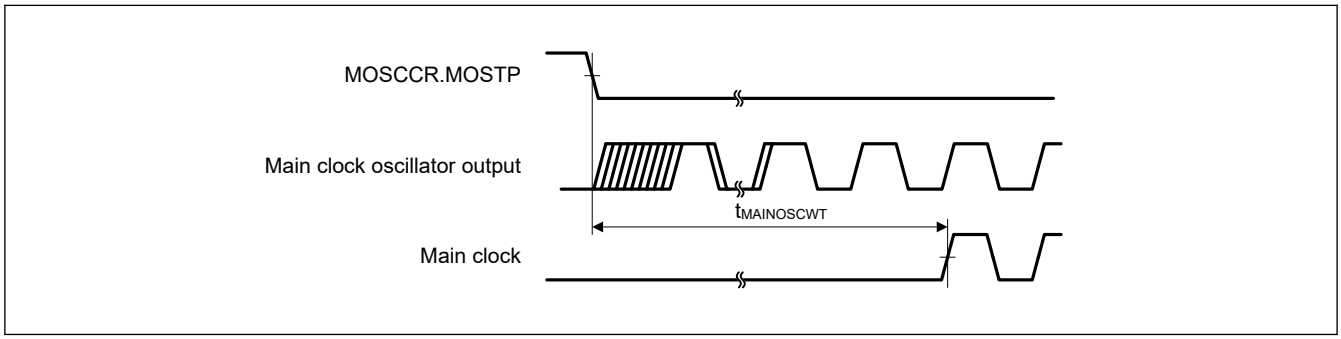


Figure 2.4 Main clock oscillation start timing

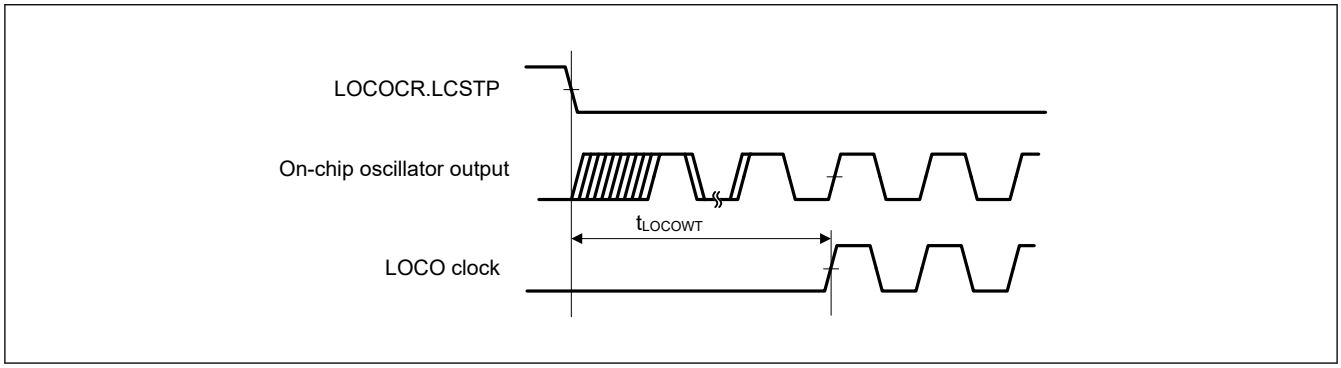


Figure 2.5 LOCO clock oscillation start timing

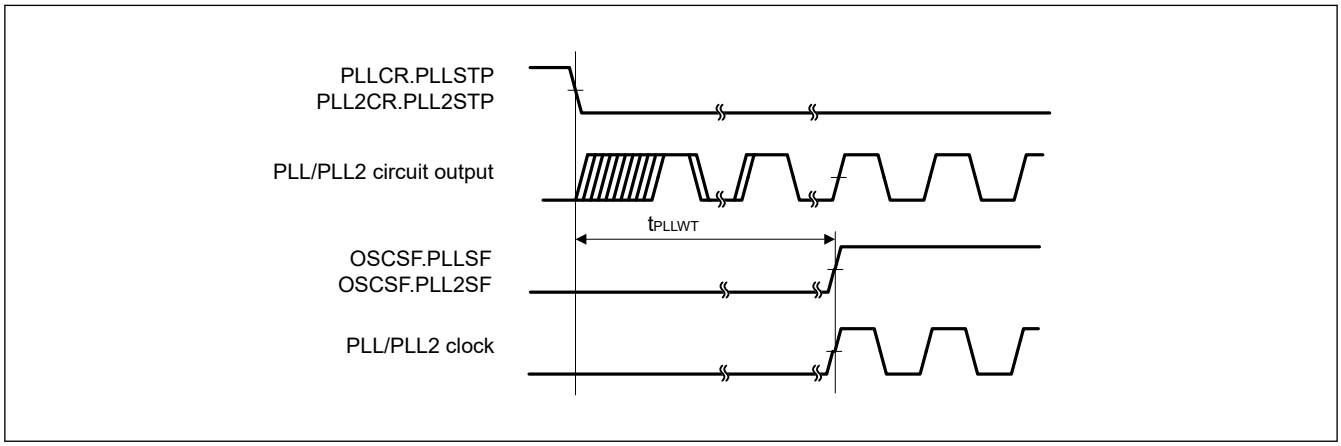


Figure 2.6 PLL/PLL2 clock oscillation start timing

2.3.3 Reset Timing

Table 2.17 Reset timing

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
RES pulse width	Power-on	t_{RESWP}	0.7	—	—	ms	Figure 2.7
	Deep Software Standby mode	t_{RESWD}	0.6	—	—	ms	Figure 2.8
	Software Standby mode	t_{RESWS}	0.3	—	—	ms	
	All other	t_{RESW}	200	—	—	µs	
Wait time after RES cancellation		t_{RESWT}	—	37.3	41.2	µs	Figure 2.7
Wait time after internal reset cancellation (IWDT reset, WDT reset, software reset, SRAM parity error reset, bus master MPU error reset, TrustZone error reset, Cache parity error reset)		t_{RESW2}	—	324	397.7	µs	—

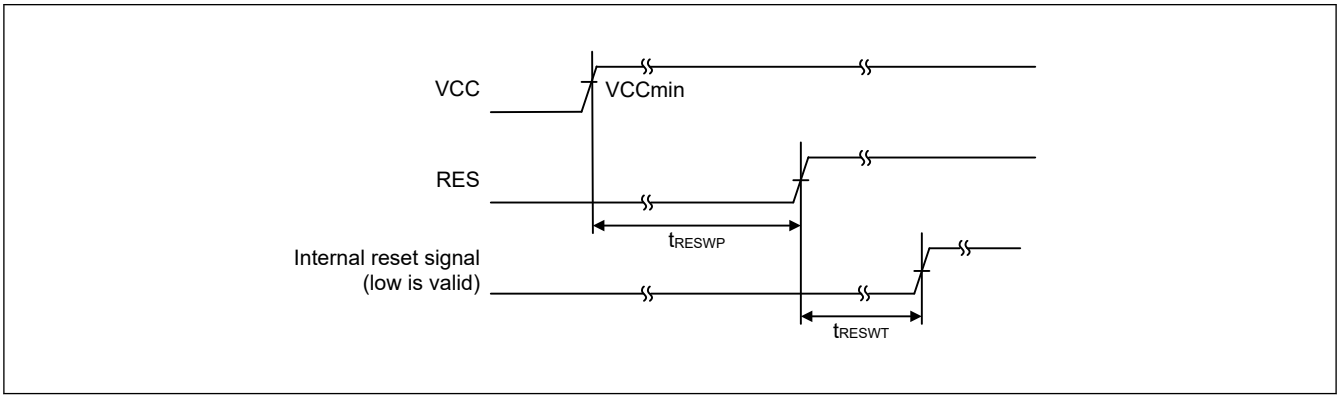


Figure 2.7 RES pin input timing under the condition that VCC exceeds V_{POR} voltage threshold

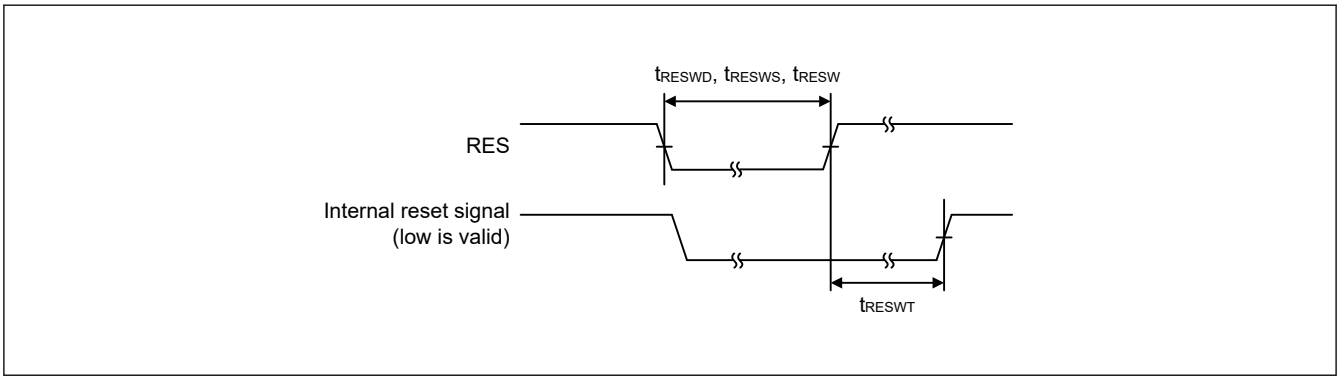


Figure 2.8 Reset input timing

2.3.4 Wakeup Timing

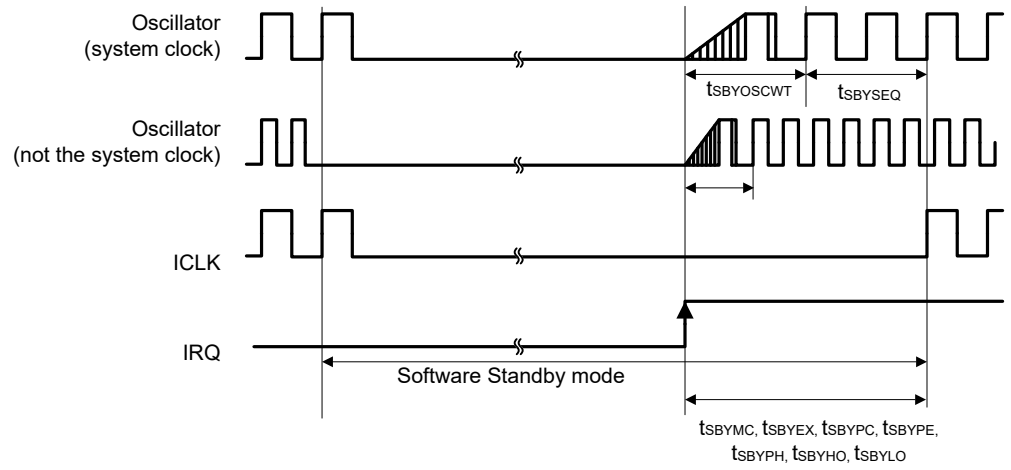
Table 2.18 Timing of recovery from low power modes

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	Crystal resonator connected to main clock oscillator	System clock source is main clock oscillator*2	t_{SBYMC}*11	—	2.1	2.4	ms	Figure 2.9 The division ratio of all oscillators is 1.
		System clock source is PLL with main clock oscillator*3	t_{SBYPC}*11	—	2.2	2.6	ms	
	External clock input to main clock oscillator	System clock source is main clock oscillator*4	t_{SBYEX}*11	—	45	125	µs	
		System clock source is PLL with main clock oscillator*5	t_{SBYPE}*11	—	170	255	µs	
	System clock source is LOCO*6		t_{SBYLO}*11	—	0.7	0.9	ms	
	System clock source is HOCO clock oscillator*7		t_{SBYHO}*11	—	55	130	µs	
	System clock source is PLL with HOCO*8		t_{SBYPH}*11	—	175	265	µs	
	System clock source is MOCO clock oscillator*9		t_{SBYMO}*11	—	35	65	µs	
Recovery time from Deep Software Standby mode	DPSBYCR.DEEPCUT[1] = 0 and DPSWCR.WTSTS[5:0] = 0x0E		t_{DSBY}	—	0.38	0.54	ms	Figure 2.10
	DPSBYCR.DEEPCUT[1] = 1 and DPSWCR.WTSTS[5:0] = 0x19		t_{DSBY}	—	0.55	0.73	ms	
Wait time after cancellation of Deep Software Standby mode			t_{DSBYWT}	56	—	57	t_{cyc}	
Recovery time from Software Standby mode to Snooze mode	High-speed mode when system clock source is HOCO (20 MHz)		t_{SNZ}	—	35*10	70*10	µs	Figure 2.11
	High-speed mode when system clock source is MOCO (8 MHz)		t_{SNZ}	—	11*10	14*10	µs	

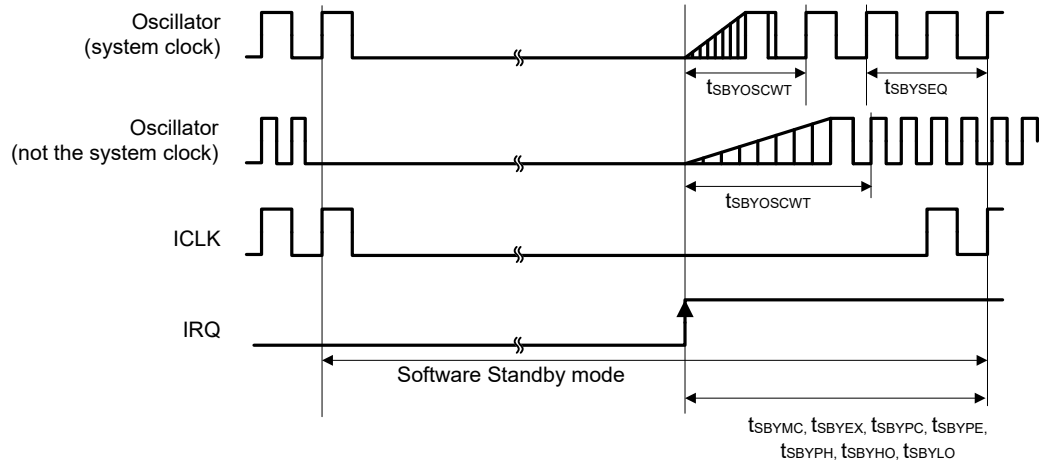
Note 1. The recovery time is determined by the system clock source. When multiple oscillators are active, the recovery time can be determined with the following equation:
Total recovery time = recovery time for an oscillator as the system clock source + the longest tSBYOSCWT in the active oscillators - tSBYOSCWT for the system clock + 2 LOCO cycles (when LOCO is operating)
Note 2. When the frequency of the crystal is 24 MHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x05) and the greatest value of the internal clock division setting is 1.
Note 3. When the frequency of PLL is 240 MHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x05) and the greatest value of the internal clock division setting is 4.
Note 4. When the frequency of the external clock is 24 MHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x00) and the greatest value of the internal clock division setting is 1.
Note 5. When the frequency of PLL is 240 MHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x00) and the greatest value of the internal clock division setting is 4.
Note 6. The LOCO frequency is 32.768 kHz and the greatest value of the internal clock division setting is 1.
Note 7. The HOCO frequency is 20 MHz and the greatest value of the internal clock division setting is 1.
Note 8. The PLL frequency is 240 MHz and the greatest value of the internal clock division setting is 4.
Note 9. The MOCO frequency is 8 MHz and the greatest value of the internal clock division setting is 1.
Note 10. When the SNZCR.RXDREQEN bit is set to 0, the following time is added as the power supply recovery time: 16 µs (typical), 48 µs (maximum).
Note 11. The recovery time can be calculated with the equation of tSBYOSCWT + tSBYSEQ. And they can be determined with the following value and equation. For n, the greatest value is selected from among the internal clock division settings.

Wakeup time	TYP		MAX		Unit
	tSBYOSCWT	tSBYSEQ	tSBYOSCWT	tSBYSEQ	
tSBYMC	(MSTS[7:0]*32 + 3) / 0.262	35 + 18 / fICLK + 4n / fMAIN	(MSTS[7:0]*32 + 14) / 0.236	62 + 18 / fICLK + 4n / fMAIN	µs
tSBYPC	(MSTS[7:0]*32 + 34) / 0.262	35 + 18 / fICLK + 4n / fPLL	(MSTS[7:0]*32 + 45) / 0.236	62 + 18 / fICLK + 4n / fPLL	µs

Wakeup time	TYP		MAX		Unit
	tSBYOSCWT	tSBYSEQ	tSBYOSCWT	tSBYSEQ	
tSBYEX	10	35 + 18 / fICLK + 4n / fEXMAIN	62	62 + 18 / fICLK + 4n / fEXMAIN	µs
tSBYPE	135	35 + 18 / fICLK + 4n / fPLL	192	62 + 18 / fICLK + 4n / fPLL	µs
tSBYLO	0	35 + 18 / fICLK + 4n / fLOCO	0	62 + 18 / fICLK + 4n / fLOCO	µs
tSBYHO	20	35 + 18 / fICLK + 4n / fHOCO	67	62 + 18 / fICLK + 4n / fHOCO	µs
tSBYPH	140	35 + 18 / fICLK + 4n / fPLL	202	62 + 18 / fICLK + 4n / fPLL	µs
tSBYMO	0	35 + 18 / fICLK + 4n / fMOCO	0	62 + 18 / fICLK + 4n / fMOCO	µs



When stabilization of the system clock oscillator is slower



When stabilization of an oscillator other than the system clock is slower

Figure 2.9 Software Standby mode cancellation timing

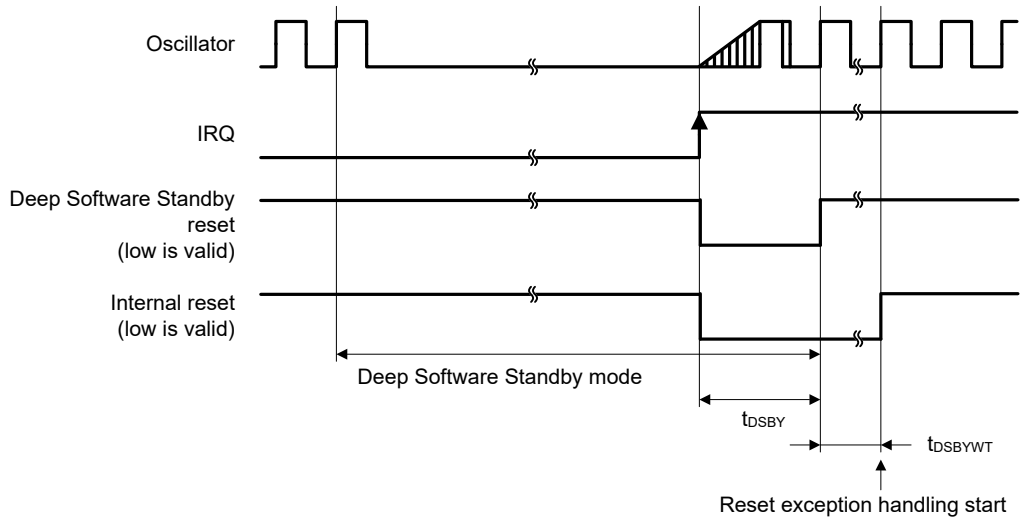
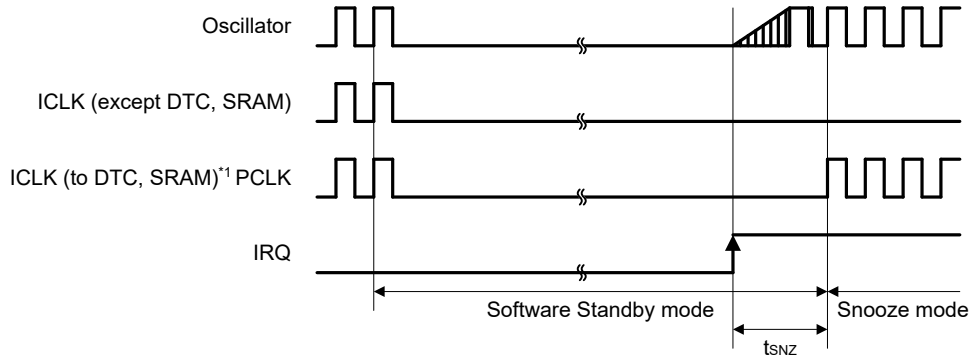


Figure 2.10 Deep Software Standby mode cancellation timing



Note 1. When SNZCR.SNZDTCEN bit is set to 1, ICLK is supplied to DTC and SRAM.

Figure 2.11 Recovery timing from Software Standby mode to Snooze mode

2.3.5 NMI and IRQ Noise Filter

Table 2.19 NMI and IRQ noise filter

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	
NMI pulse width	t_{NMIW}	200	—	—	ns	NMI digital filter disabled	$t_{Pcyc} \times 2 \leq 200$ ns
		$t_{Pcyc} \times 2$*1	—	—			$t_{Pcyc} \times 2 > 200$ ns
		200	—	—		NMI digital filter enabled	$t_{NMICK} \times 3 \leq 200$ ns
		$t_{NMICK} \times 3.5$*2	—	—			$t_{NMICK} \times 3 > 200$ ns
IRQ pulse width	t_{IRQW}	200	—	—	ns	IRQ digital filter disabled	$t_{Pcyc} \times 2 \leq 200$ ns
		$t_{Pcyc} \times 2$*1	—	—			$t_{Pcyc} \times 2 > 200$ ns
		200	—	—		IRQ digital filter enabled	$t_{IRQCK} \times 3 \leq 200$ ns
		$t_{IRQCK} \times 3.5$*3	—	—			$t_{IRQCK} \times 3 > 200$ ns

Note: 200 ns minimum in Software Standby mode.
Note: If the clock source is switched, add 4 clock cycles of the switched source.
Note 1. t_{Pcyc} indicates the PCLKB cycle.
Note 2. t_{NMICK} indicates the cycle of the NMI digital filter sampling clock.
Note 3. t_{IRQCK} indicates the cycle of the IRQi digital filter sampling clock.

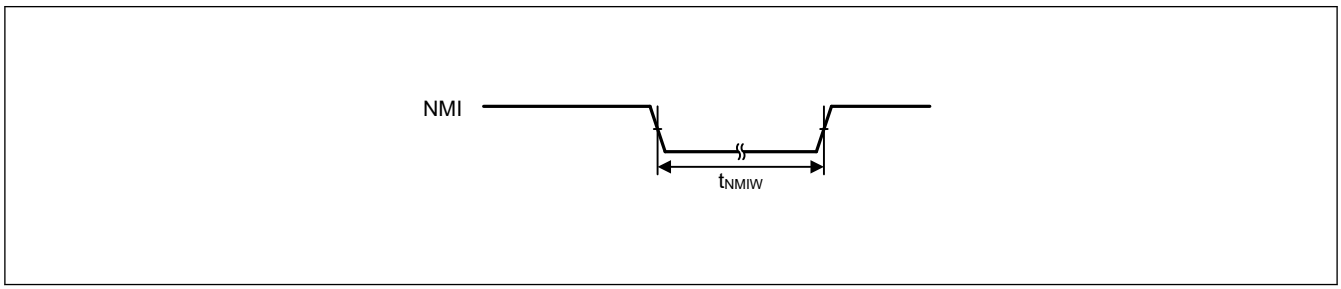


Figure 2.12 NMI interrupt input timing

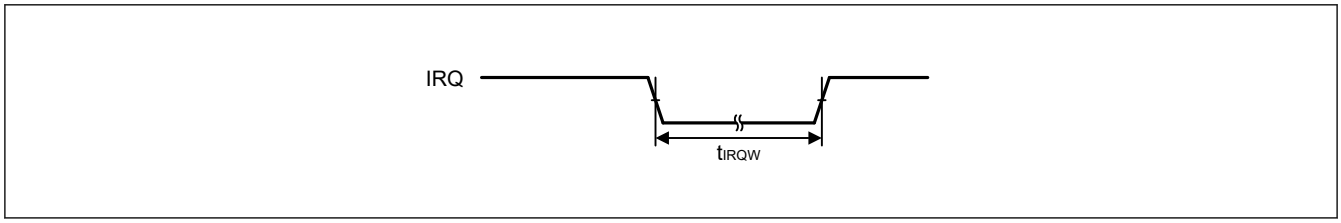


Figure 2.13 IRQ interrupt input timing

2.3.6 I/O Ports, POEG, GPT, AGT, KINT and ADC Trigger Timing

Table 2.20 I/O ports, POEG, GPT, AGT, KINT and ADC trigger timing (1 of 4)

GPT Conditions:
High drive output is selected in the Port Drive Capability bit in the PmnPFS register.
AGT Conditions:
Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
I/O ports	Input data pulse width	t_{PRW}	1.5	—	—	t_{Icyc}	Figure 2.14

Table 2.20 I/O ports, POEG, GPT, AGT, KINT and ADC trigger timing (2 of 4)

GPT Conditions:
High drive output is selected in the Port Drive Capability bit in the PmnPFS register.
AGT Conditions:
Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
POEG	GTETRGn input pulse width		t_{POEW}	1.5	—	—	t_{Pcyc}	Figure 2.15
	Output disable time	Input level detection of the GTETRGn pin (via flag)	t_{POEGDI}	—	—	3 PCLKB + 0.34	µs	Figure 2.16 When the digital noise filter is not in use (POEGGn.NFEN = 0 (n = A to D))
		Detection of the output stopping signal from GPT (deadtime error, simultaneous high output, or simultaneous low output)	t_{POEGDE}	—	—	0.5	µs	Figure 2.17
		Edge detection signal from a comparator	t_{POEGDC}	—	—	4 PCLKB + 0.5	µs	Figure 2.18 The time is that when the noise filter for ACMPHS is not in use (CMPCTL.CDFS[1:0] = 00) and excludes the time for detection by ACMPHS.
		Register setting	t_{POEGDS}	—	—	1 PCLKB + 0.3	µs	Figure 2.19 Time for access to the register is not included.
		Oscillation stop detection*3	$t_{POEGDOS}$	—	≤ 1	—	µs	Figure 2.20
		Input level detection of the GTETRGn pin (direct path)	$t_{POEGDDI}$	—	—	2 PCLKB + 1 PCLKD + 0.34	µs	Figure 2.21
		Level detection signal from a comparator	$t_{POEGDDC}$	—	—	3 PCLKD + 0.3	µs	Figure 2.22 The time is that when the noise filter for ACMPHS is not in use (CMPCTL.CDFS[1:0] = 00) and excludes the time for detection by ACMPHS.

Table 2.20 I/O ports, POEG, GPT, AGT, KINT and ADC trigger timing (3 of 4)

GPT Conditions:
High drive output is selected in the Port Drive Capability bit in the PmnPFS register.
AGT Conditions:
Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions
GPT	Input capture pulse width	Single edge		t_{GTICW}	1.5	—	—	t_{PDcyc}	Figure 2.23
		Dual edge			2.5	—	—		
	GTIOCxY output skew (x = 0 to 3, Y = A or B)	Middle drive buffer		t_{GTISK}*1	—	—	4	ns	Figure 2.24
		High drive buffer			—	—	4		
		High current output buffer			—	—	4		
	GTIOCxY output skew (x = 4 to 6, Y = A or B)	Middle drive buffer			—	—	4		
		High drive buffer			—	—	4		
		High current output buffer			—	—	4		
	GTIOCxY output skew (x = 7 to 9, Y = A or B)	Middle drive buffer			—	—	4		
		High drive buffer			—	—	4		
		High current output buffer			—	—	4		
	GTIOCxY output skew (x = 0 to 9, Y = A or B)	Middle drive buffer			—	—	6		
		High drive buffer			—	—	6		
		High current output buffer			—	—	6		
	OPS output skew GTOUUP, GTOULO, GTOVUP, GTOVLO, GTOWUP, GTOWLO			t_{GTOSK}	—	—	5	ns	Figure 2.25
	External trigger input pulse width	Synchronous clock	Single-edge setting	t_{GTEW}	1.5	—	—	t_{Pcyc}	Figure 2.26
			Both-edge setting		2.5	—	—		
		Asynchronous clock	Single-edge setting		2.5	—	—		
			Both-edge setting		3.5	—	—		
	Timer clock pulse width	Synchronous clock	Single-edge setting	t_{GTCKWH}, t_{GTCKWL}	1.5	—	—	t_{Pcyc}	Figure 2.27
			Both-edge setting		2.5	—	—		
		Asynchronous clock	Single-edge setting		2.5	—	—		
			Both-edge setting		3.5	—	—		
GPT (PWM Delay Generation Circuit)	GTIOCxY_Z skew (x = 0 to 3, Y = A or B, Z = A to D)			t_{HRSK}*2	—	—	4.0	ns	Figure 2.28
AGT	AGTIO, AGTEE input cycle			t_{ACYC}*2	50	—	—	ns	Figure 2.29
	AGTIO, AGTEE input high width, low width			t_{ACKWH}, t_{ACKWL}	20	—	—	ns	
	AGTIO, AGTO, AGTOA, AGTOB output cycle			t_{ACYC2}	33.3	—	—	ns	
KINT	KRn (n = 00 to 07) pulse width			t_{KR}	250	—	—	ns	Figure 2.30

Table 2.20 I/O ports, POEG, GPT, AGT, KINT and ADC trigger timing (4 of 4)

GPT Conditions:
High drive output is selected in the Port Drive Capability bit in the PmnPFS register.
AGT Conditions:
Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
ADC	ADC trigger input pulse width	t_{TRGW}	1.5	—	—	t_{ADcyc}	Figure 2.31

Note: t_{Icyc}: ICLK cycle, t_{Pcyc}: PCLKB cycle, t_{PDcyc}: GTCLK cycle, t_{ADcyc}: ADCLK cycle.
Note 1. This skew applies when the same driver I/O is used. If the I/O of the middle and high drivers is mixed, operation is not guaranteed.
Note 2. Constraints on input cycle:
When not switching the source clock: $t_{Pcyc} \times 2 < t_{ACYC}$ should be satisfied.
When switching the source clock: $t_{Pcyc} \times 6 < t_{ACYC}$ should be satisfied.
Note 3. Reference value.

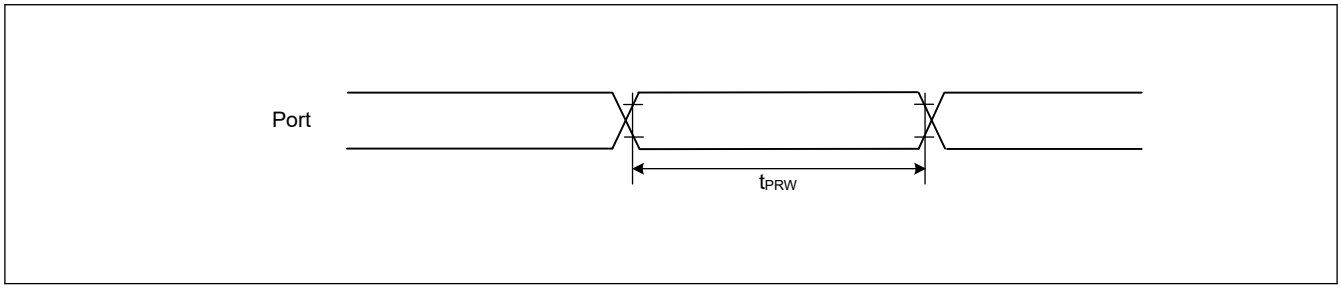


Figure 2.14 I/O ports input timing

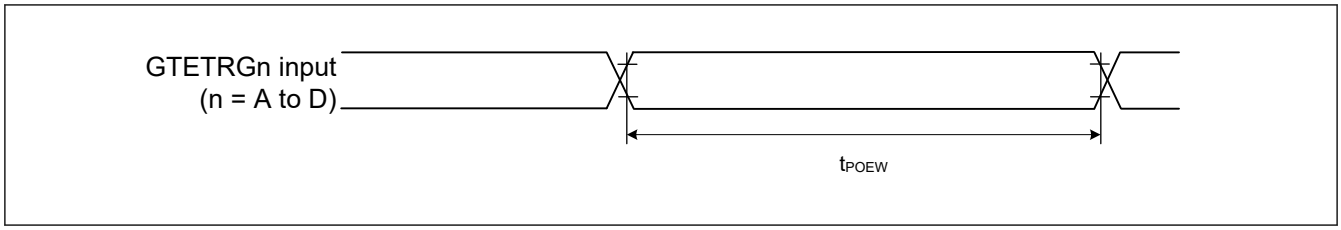


Figure 2.15 POEG input trigger timing

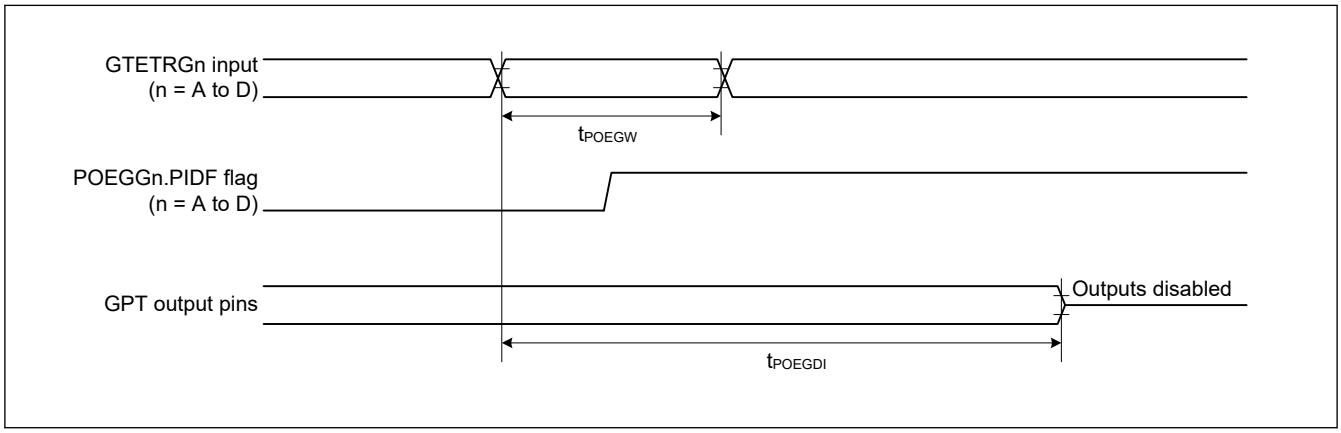
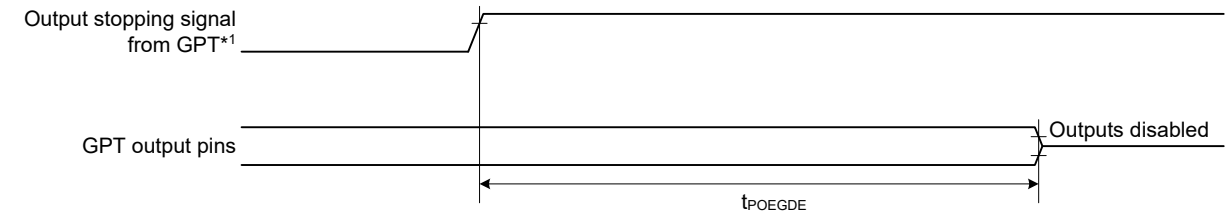


Figure 2.16 Output Disable Time for POEG via Detection Flag in Response to the Input Level Detection of the GTETRGn pin



Note 1. GPT32n.GTST.DTEF (dead time error flag), GPT32n.GTST.OABLF (simultaneous low output flag), or GPT32n.GTST.OABHF (simultaneous high output flag)

Figure 2.17 Output Disable Time for POEG in Response to Detection of the Output Stopping Signal from GPT

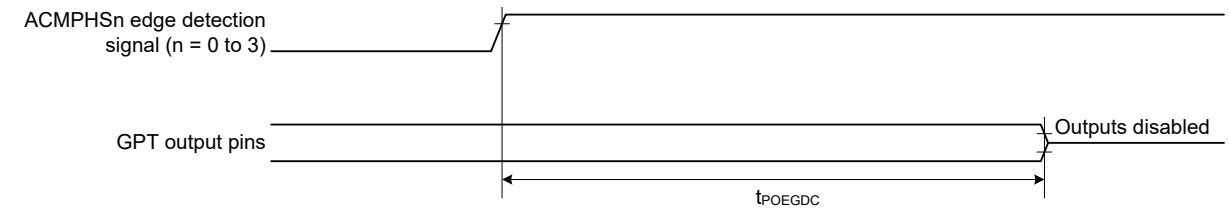


Figure 2.18 Output Disable Time for POEG in Response to Edge Detection Signal from ACMPHS

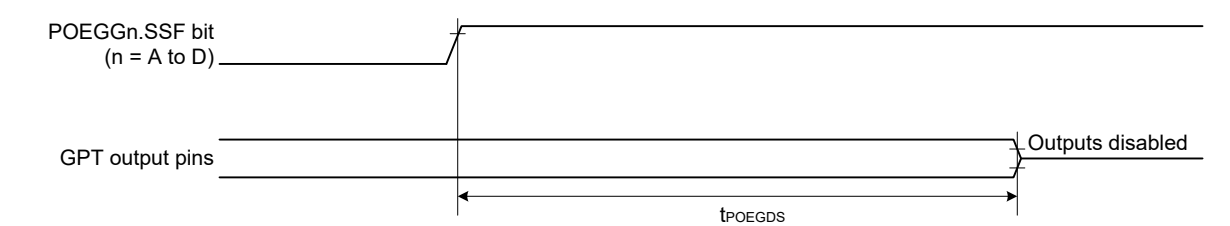


Figure 2.19 Output Disable Time for POEG in Response to the Register Setting

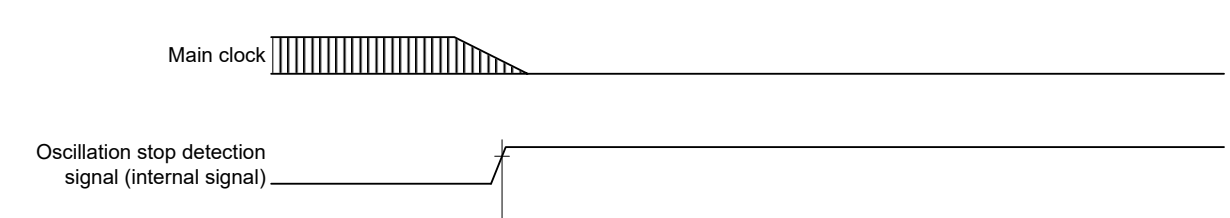


Figure 2.20 Output Disable Time of POEG in Response to the Oscillation Stop Detection

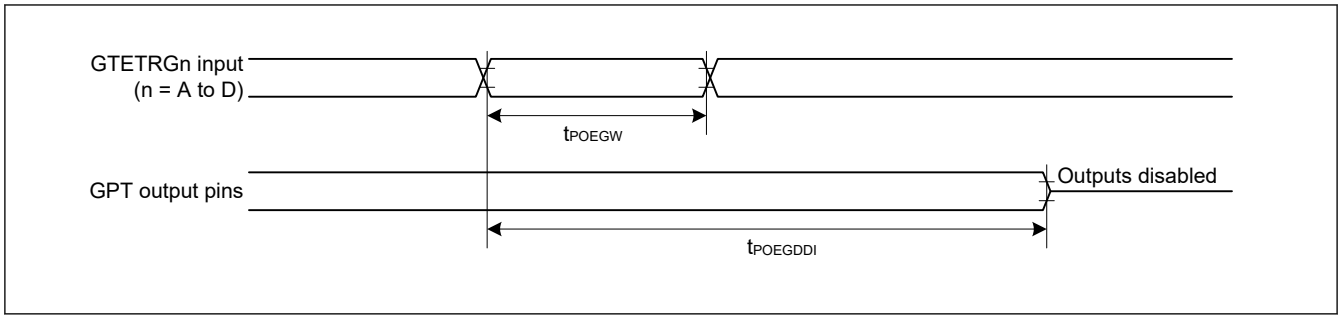


Figure 2.21 Output Disable Time for POEG in Direct Response to the Input Level Detection of the GTETRGn pin

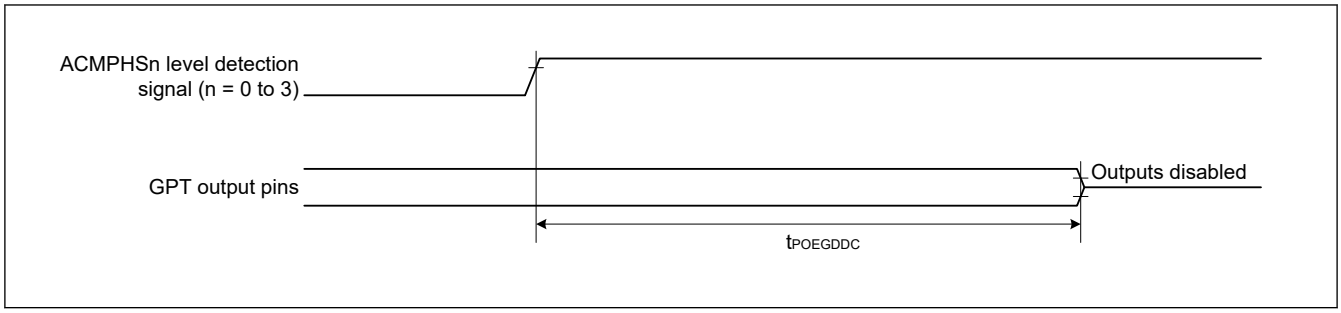


Figure 2.22 Output Disable Time for POEG in Response to Level Detection Signal from ACMPHS

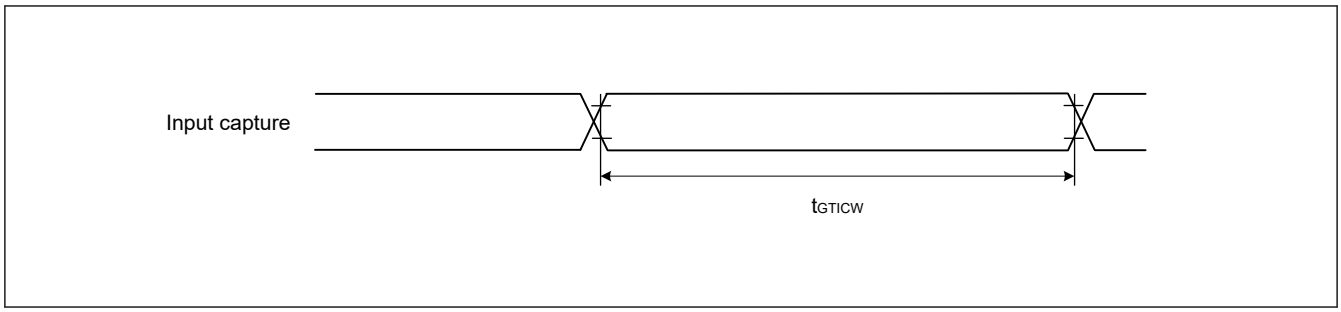


Figure 2.23 GPT input capture timing

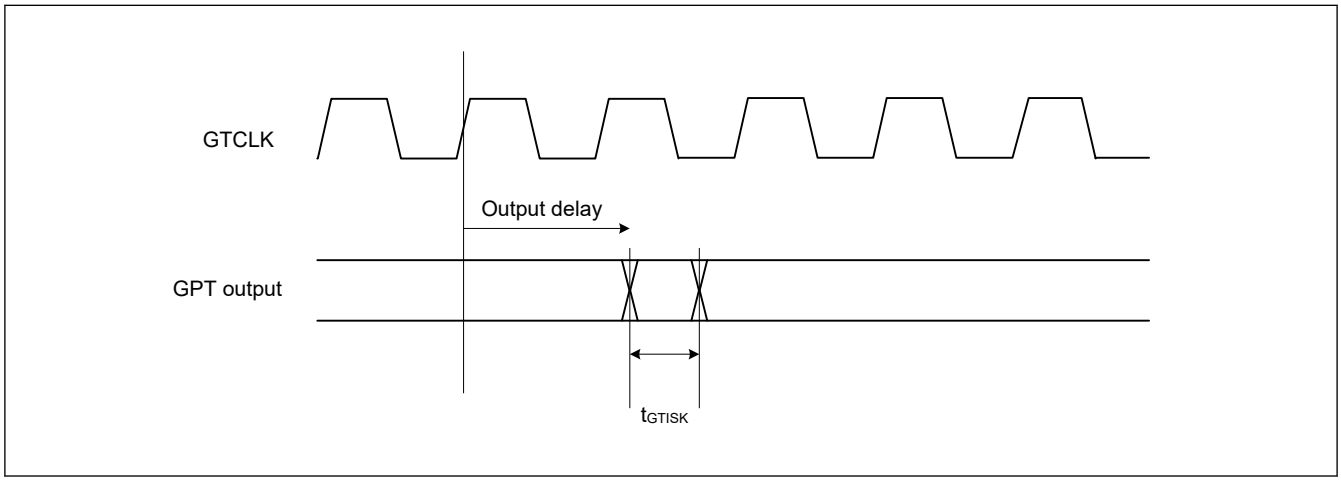


Figure 2.24 GPT output delay skew

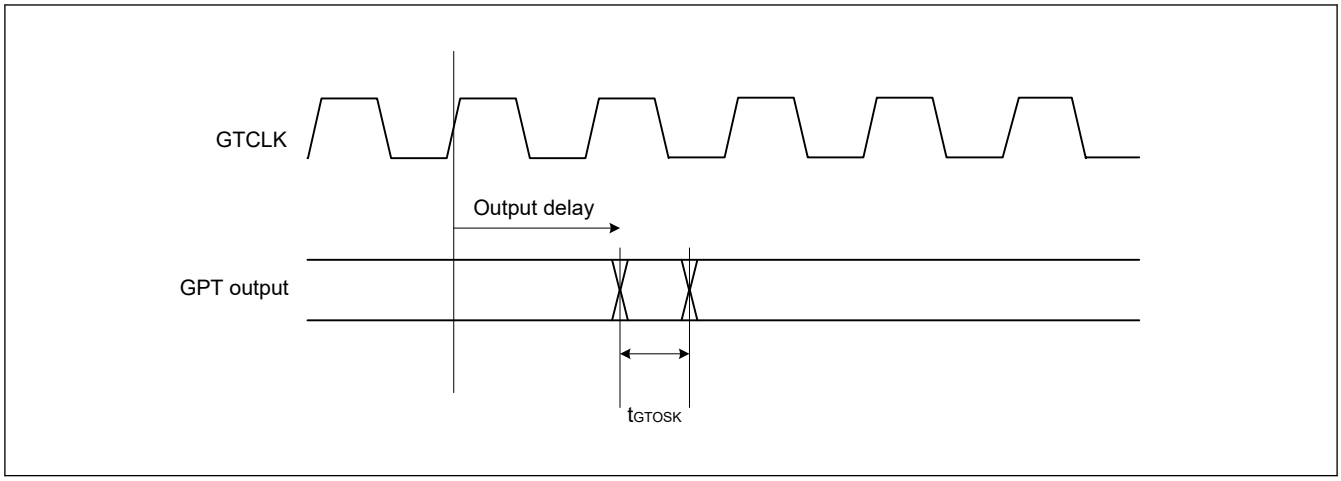


Figure 2.25 GPT output delay skew for OPS

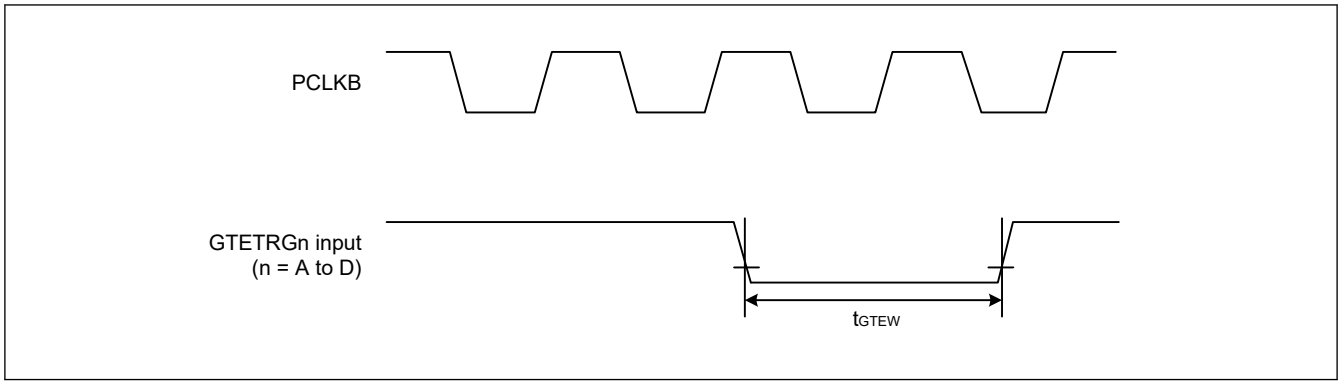


Figure 2.26 GPT External Trigger Input Timing

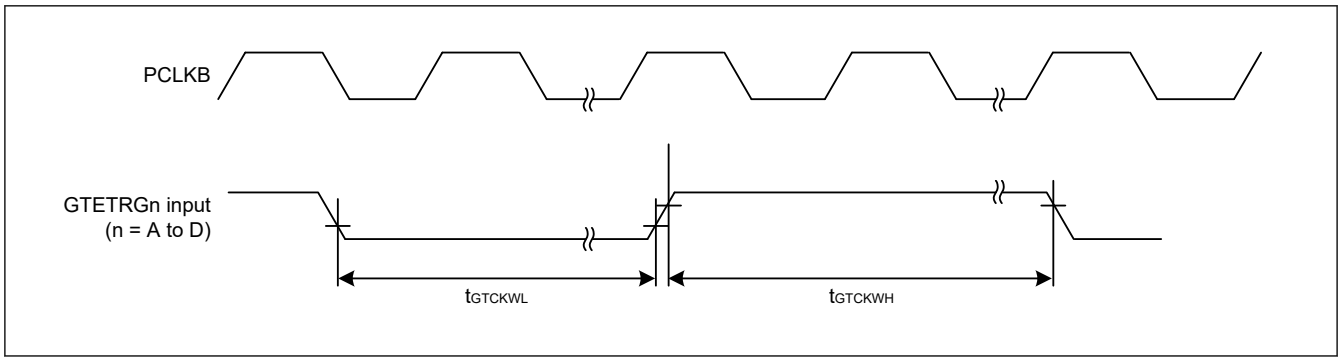


Figure 2.27 GPT Clock Input Timing

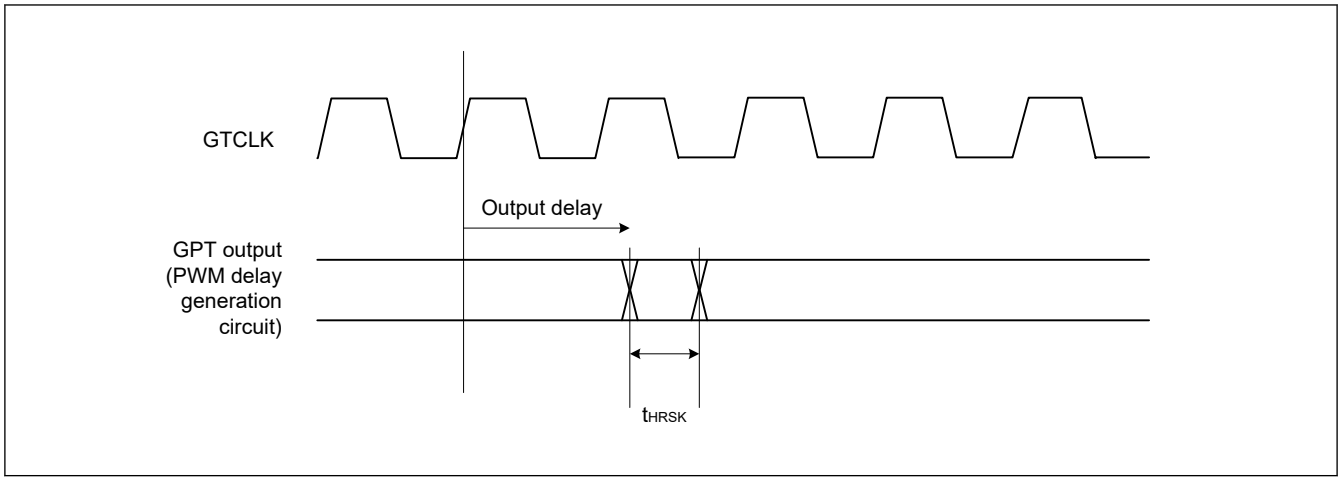


Figure 2.28 GPT (PDG) output delay skew

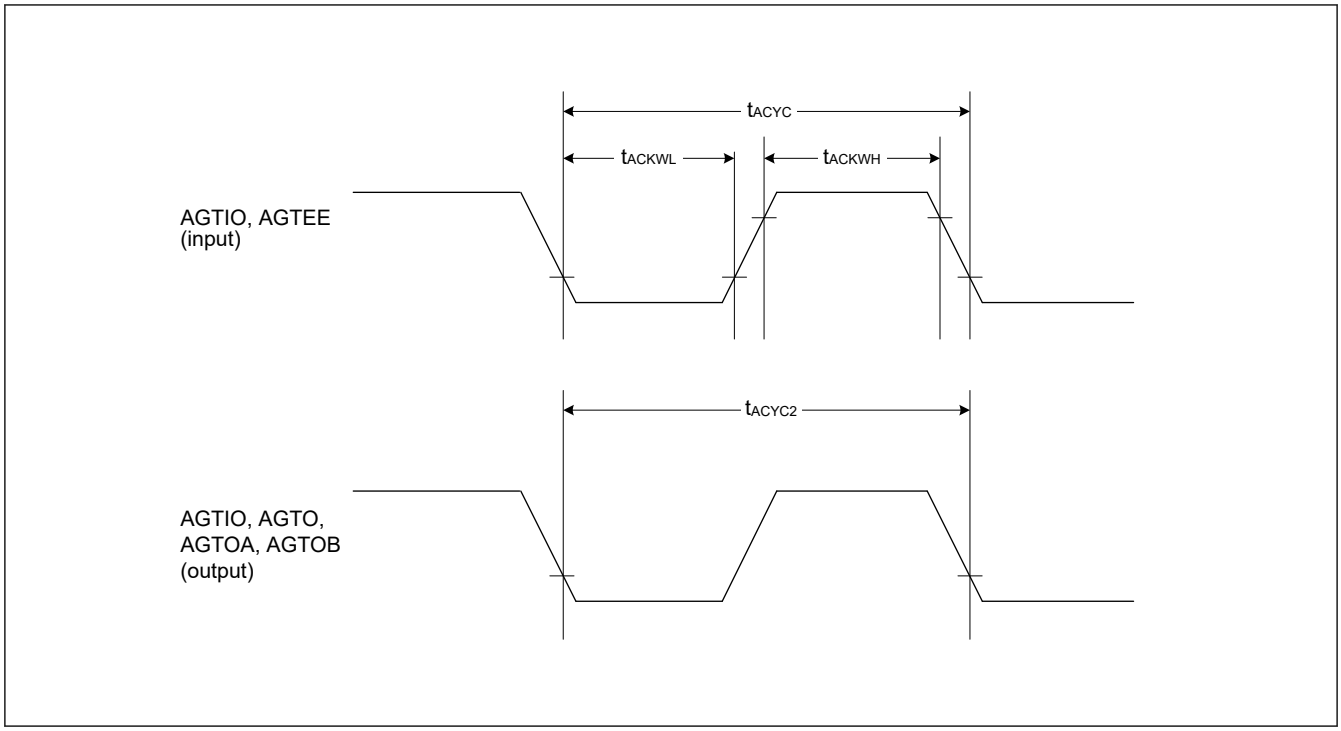


Figure 2.29 AGT input/output timing

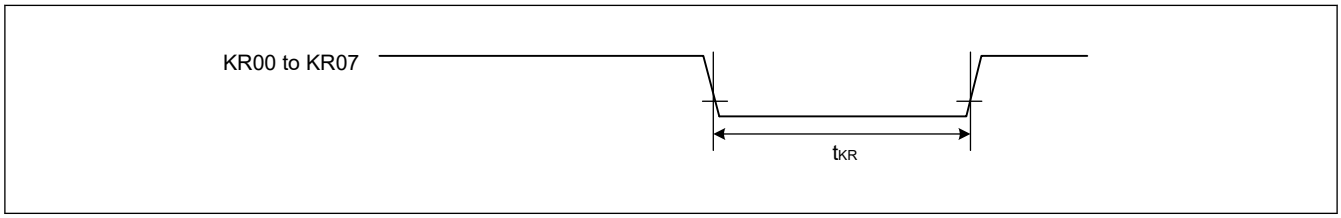


Figure 2.30 Key interrupt input timing

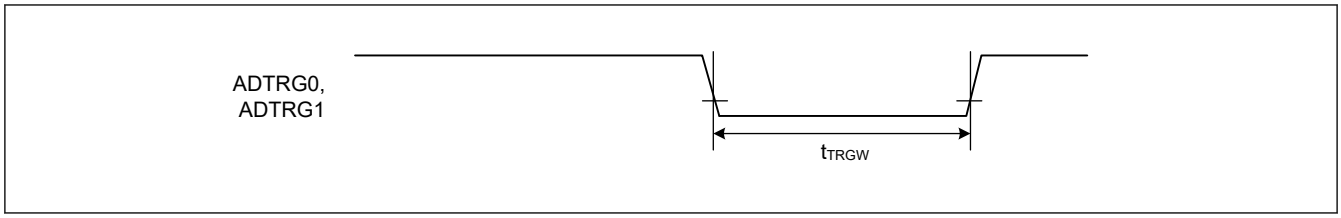


Figure 2.31 ADC trigger input timing

2.3.7 PDG Timing

Table 2.21 PDG timing

Parameter	Min	Typ	Max	Unit	Test conditions
Operation frequency	80	—	200	MHz	—
Resolution	—	156	—	ps	GPTCLK = 200 MHz
DNL*1	—	±2.0	—	LSB	—

Note 1. This value normalizes the differences between lines in 1-LSB resolution.

2.3.8 CAC Timing

Table 2.22 CAC timing

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
CAC	CACREF input pulse width	$t_{PBcyc} \leq t_{cac}$*1	t_{CACREF}	$4.5 \times t_{cac} + 3 \times t_{PBcyc}$	—	—	ns	—
		$t_{PBcyc} > t_{cac}$*1		$5 \times t_{cac} + 6.5 \times t_{PBcyc}$	—	—	ns	

Note: t_{PBcyc}: PCLKB cycle.
Note 1. t_{cac}: CAC count clock source cycle.

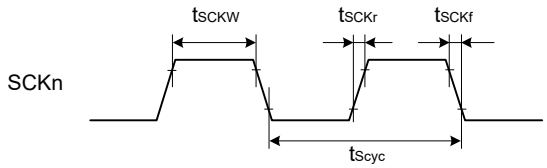
2.3.9 SCI Timing

Table 2.23 SCI timing (Asynchronous mode)

Conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter	Symbol	Min	Max	Unit	Note
Input clock cycle	t_{Scyc}	4	—	t_{Tcyc}	
Input clock pulse width	t_{SCKW}	0.4	0.6	t_{Scyc}	
Input clock rise time	t_{SCKr}	—	5	ns	
Input clock fall time	t_{SCKf}	—	5	ns	
Output clock cycle	t_{Scyc}	6	—	t_{Tcyc}	
Output clock pulse width	t_{SCKW}	0.4	0.6	t_{Scyc}	
Output clock rise time	t_{SCKr}	—	5	ns	
Output clock fall time	t_{SCKf}	—	5	ns	

Note: t_{Tcyc}: SCITCLK cycle.



Note: n = 0 to 4, 9

Figure 2.32 SCK clock input/output timing

Table 2.24 SCI timing (Simple SPI)

Conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter		High Speed/ Default	Symbol	Min	Max	Unit	Note
SCK clock cycle output	Master		t_{SPcyc}	2	65536	t_{Tcyc}	
SCK clock cycle input	Slave			2	—		
SCK clock high pulse width	Master		t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	Slave						
SCK clock low pulse width	Master		t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	Slave						
SCK clock rise and fall time	Output		t_{SPCKr}, t_{SPCKf}	—	5	ns	
	Input			—	1	us	
Data input setup time	Master	High Speed*1	t_{SU}	1.7	—	ns	
		Default*2		3	—	ns	
	Slave			3.3	—	ns	
Data input hold time	Master	High Speed*1	t_H	12	—	ns	
		Default*2		14	—	ns	
	Slave			3	—	ns	
Data output delay	Master	High Speed*1	t_{OD}	—	5	ns	
		Default*2		—	7.3	ns	
	Slave	High Speed*1		—	15	ns	
		Default*2		—	21	ns	
Data output hold time	Master		t_{OH}	0	—	ns	
	Slave			0	—	ns	
Data rise and fall time	Output		t_{Dr}, t_{Df}	—	5	ns	
	Input			—	1	ns	
Slave access time			t_{SA}	—	5	t_{Tcyc}	
Slave output release time			t_{REL}	—	5	t_{Tcyc}	

Note: t_{Tcyc}: SCITCLK cycle.
Note 1. Must use pins that have a letter appended to their name, for instance _A, _B, _C, to indicate group membership. SCI0 is instance _A, SCI2 and SCI3 are instance _B, SCI1 and SCI9 are instance _C, SCI4 is instance _C and RXD is only PD14.
Note 2. All pins of group membership can be used.

Table 2.25 SCI timing (Simple SPI mode) (1 of 2)

Conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter	Symbol	Min	Max	Unit	Note
SS input setup time	t_{LEAD}	1	—	t_{SPcyc}	

Table 2.25 SCI timing (Simple SPI mode) (2 of 2)

Conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter	Symbol	Min	Max	Unit	Note
SS input hold time	t_{LAG}	1	—	t_{SPcyc}	
SS input rise and fall time	t_{SSLr}, t_{SSLf}	—	1	us	

Table 2.26 SCI timing (Clock synchronous mode)

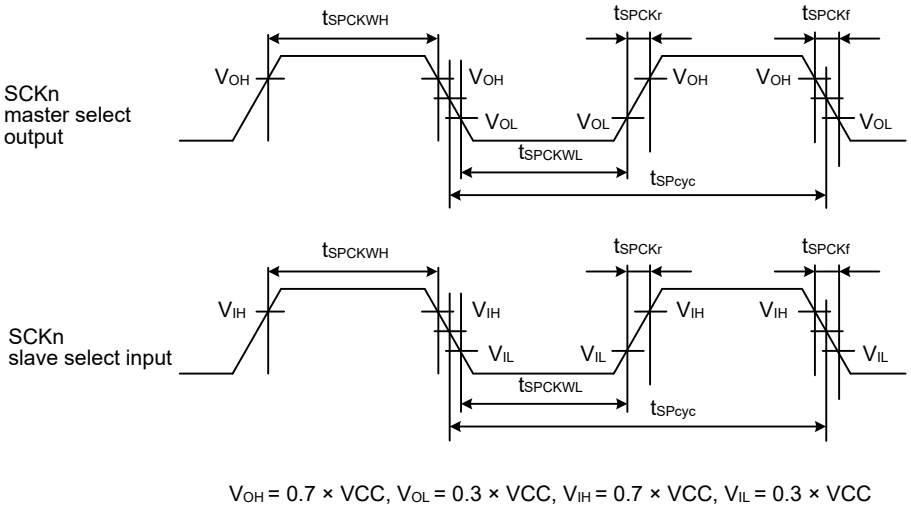
Conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter		High Speed/ Default	Symbol	Min	Max	Unit	Note
SCK clock cycle output	Master		t_{SPcyc}	2	—	t_{Tcyc}	
SCK clock cycle input	Slave			2	—		
SCK clock high pulse width	Master		t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	Slave						
SCK clock low pulse width	Master		t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	Slave						
SCK clock rise and fall time	Output		t_{SPCKr}, t_{SPCKf}	—	5	ns	
	Input						
Data input setup time	Master	High Speed*1	t_{SU}	2.6	—	ns	
		Default*2		2.8	—	ns	
	Slave			3.3	—	ns	
Data input hold time	Master	High Speed*1	t_H	12	—	ns	
		Default*2		14	—	ns	
	Slave			3	—	ns	
Data output delay	Master	High Speed*1	t_{OD}	—	5	ns	
		Default*2		—	7.3	ns	
	Slave	High Speed*1		—	15	ns	
		Default*2		—	21	ns	
Data output hold time	Master		t_{OH}	0	—	ns	
	Slave			0	—	ns	
Data rise and fall time	Output		t_{Dr}, t_{Df}	—	5	ns	
	Input			—	5	ns	

Note: t_{Tcyc}: SCITCLK cycle.

Note 1. Must use pins that have a letter appended to their name, for instance _A, _B, _C, to indicate group membership. SCI0 is instance _A, SCI2 and SCI3 are instance _B, SCI1 and SCI9 are instance _C, SCI4 is instance _C and RXD is only PD14.

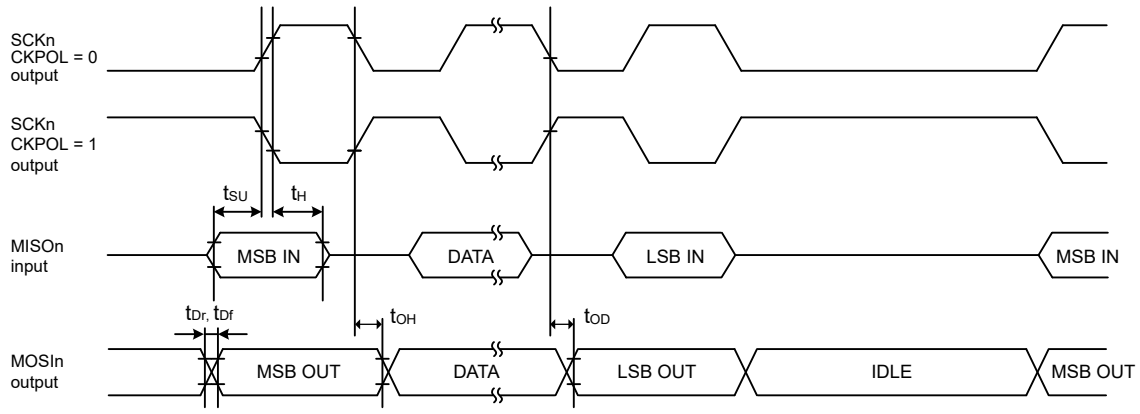
Note 2. All pins of group membership can be used.



V_{OH} = 0.7 × VCC, V_{OL} = 0.3 × VCC, V_{IH} = 0.7 × VCC, V_{IL} = 0.3 × VCC

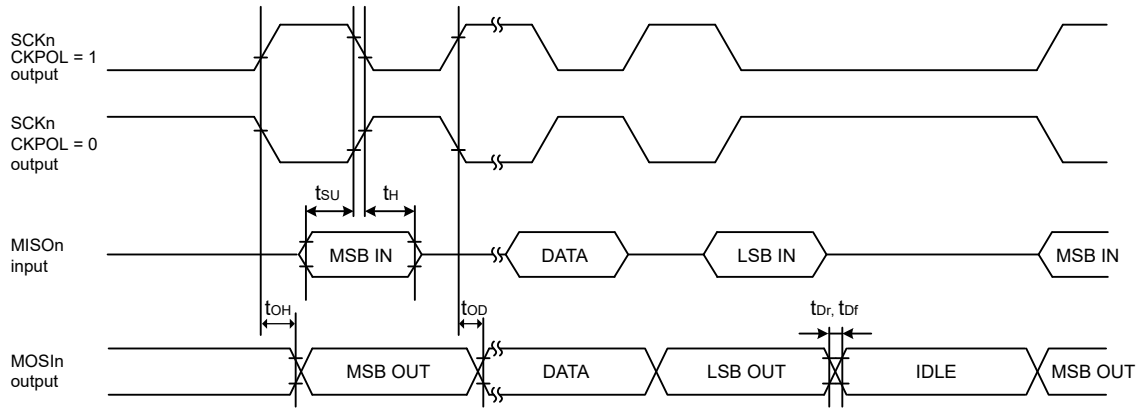
Note: n = 0 to 4, 9

Figure 2.33 SCI simple SPI mode clock timing



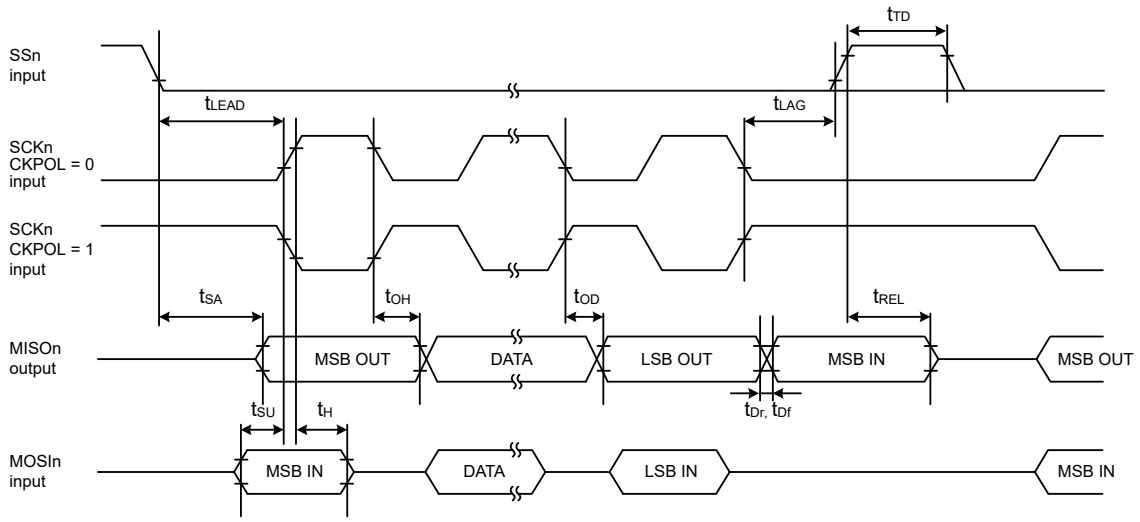
Note: n = 0 to 4, 9

Figure 2.34 SCI simple SPI mode timing for master when CKPH = 1



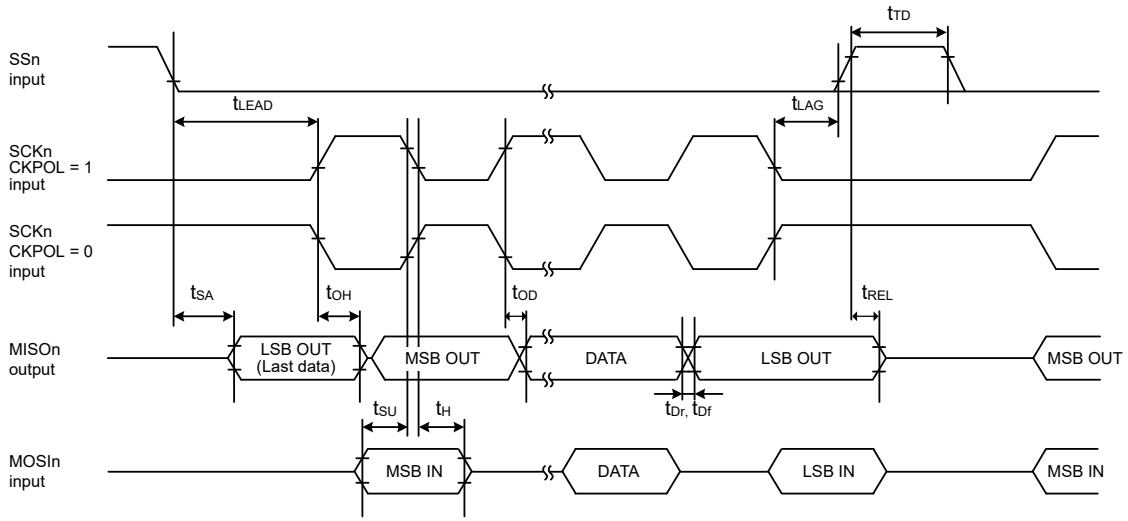
Note: n = 0 to 4, 9

Figure 2.35 SCI simple SPI mode timing for master when CKPH = 0



Note: n = 0 to 4, 9

Figure 2.36 SCI simple SPI mode timing for slave when CKPH = 1



Note: n = 0 to 4, 9

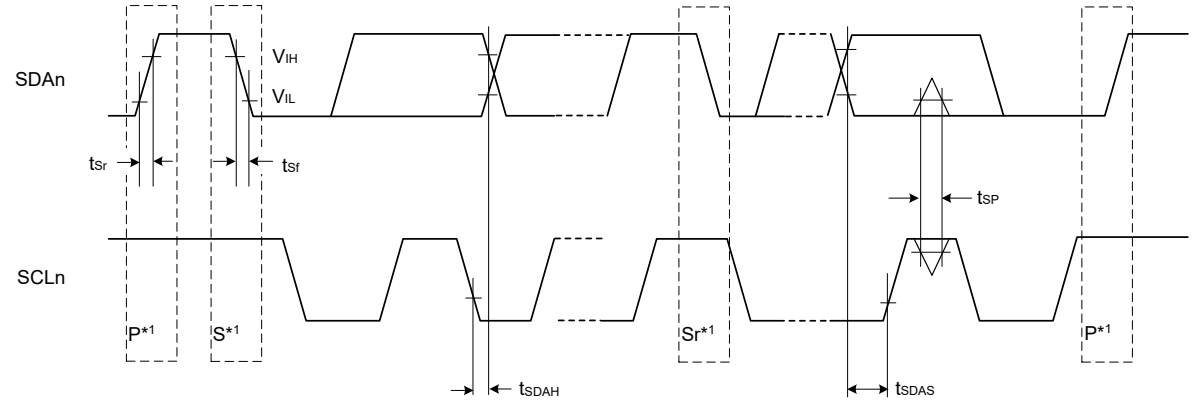
Figure 2.37 SCI simple SPI mode timing for slave when CKPH = 0

Table 2.27 SCI timing (Simple IIC mode)

Conditions: Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter		Symbol	Min	Max	Unit	Note
Simple IIC (Standard mode)	SCL, SDA input rise time	t_{Sr}	—	1000	ns	
	SCL, SDA input fall time	t_{Sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	4 × t_{Tcyc}	ns	
	Data input setup time	t_{SDAS}	250	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b *1	—	400	pF	
Simple IIC (Fast mode)	SCL, SDA input rise time	t_{Sr}	—	300	ns	
	SCL, SDA input fall time	t_{Sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	4 × t_{Tcyc}	ns	
	Data input setup time	t_{SDAS}	100	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b *1	—	400	pF	

Note: t_{Tcyc}: SCITCLK cycle.
Note 1. Cb indicates the total capacity of the bus line.



Test conditions:
$V_{IH} = V_{CC} \times 0.7$, $V_{IL} = V_{CC} \times 0.3$
$V_{OL} = 0.6$ V, $I_{OL} = 6$ mA (ICFER.FMPE = 0)
$V_{OL} = 0.4$ V, $I_{OL} = 20$ mA (ICFER.FMPE = 1)

Note: n = 0 to 4, 9
Note 1. S, P, and Sr indicate the following conditions:
S: Start condition
P: Stop condition
Sr: Restart condition

Figure 2.38 SCI simple IIC mode timing

2.3.10 SPI Timing

Table 2.28 SPI timing (1 of 2)

Conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter		High Speed/ Default	Symbol	VCC = 3.0 to 3.6 V, C = 15 pF		VCC = 2.7 to 3.6 V, C = 30 pF		Unit	Note
				Min	Max	Min	Max		
RSPCK clock cycle	Master		t_{SPcyc}	2	4096	2	4096	t_{Tcyc}	
	Slave			2	—	2	—		
RSPCK clock high pulse width	Master		t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$	—	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$	—	ns	
	Slave			0.4	0.6	0.4	0.6	t_{SPcyc}	
RSPCK clock low pulse width	Master		t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$	—	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$	—	ns	
	Slave			0.4	0.6	0.4	0.6	t_{SPcyc}	
RSPCK clock rise and fall time	Output		t_{SPCKr}, t_{SPCKf}	—	5	—	5	ns	
	Input			—	1	—	1	µs	
Data input setup time	Master	High Speed*1	t_{SU}	0	—	—	—	ns	
		Default*2		—	—	1.3	—	ns	
	Slave			2.5	—	2.7	—	ns	

Table 2.28 SPI timing (2 of 2)

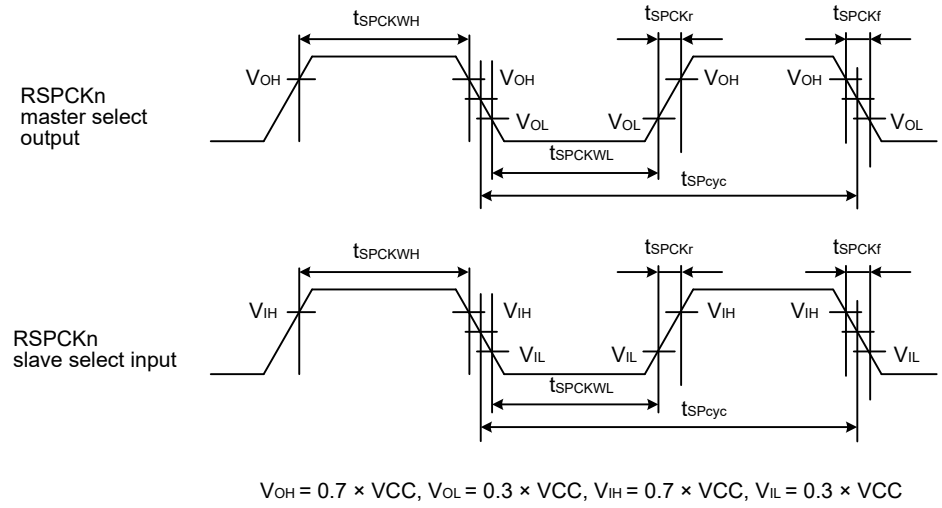
Conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter		High Speed/ Default	Symbol	VCC = 3.0 to 3.6 V, C = 15 pF		VCC = 2.7 to 3.6 V, C = 30 pF		Unit	Note
				Min	Max	Min	Max		
Data input hold time	Master	High Speed*1	t_H	6.2	—	—	—	ns	
		Default*2		—	—	8	—	ns	
	Slave			2.5	—	2.5	—	ns	
SSL setup time	Master		t_{LEAD}	1	8	1	8	t_{SPcyc}	
	Slave			6	—	6	—	t_{Tcyc}	
SSL hold time	Master		t_{LAG}	1	8	1	8	t_{SPcyc}	
	Slave			6	—	6	—	t_{Tcyc}	
TI SSP SS input setup time	Slave		t_{TISS}	2.5	—	2.8	—	ns	
TI SSP SS input hold time	Slave		t_{TISH}	2.5	—	2.5	—	ns	
TI SSP next-access time	Slave		t_{TIND}	2 × t_{Tcyc} + SLNDL × t_{Tcyc}	—	2 × t_{Tcyc} + SLNDL × t_{Tcyc}	—	ns	
TI SSP master SS output delay	Master		t_{TISSOD}	—	8.9	—	8.9	ns	
Data output delay time	Master	High Speed*1	t_{OD}	—	4.6	—	—	ns	
		Default*2		—	—	—	7	ns	
	Slave	High Speed*1		—	14	—	—	ns	
		Default*2		—	—	—	21	ns	
Data output hold time	Master		t_{OH}	0	—	0	—	ns	
	Slave			0	—	0	—	ns	
Successive transmission delay time	Master		t_{TD}	t_{SPcyc} + 2 × t_{Tcyc}	8 × t_{SPcyc} + 2 × t_{Pcyc}	t_{SPcyc} + 2 × t_{Tcyc}	8 × t_{SPcyc} + 2 × t_{Pcyc}	ns	
	Slave			t_{Tcyc}	—	t_{Tcyc}	—	ns	
MOSI and MISO rise and fall time	Output		t_{Dr}	—	5	—	5	ns	
	Input		t_{Df}	—	1	—	1	µs	
SSL rise and fall time	Output		t_{SSLr}	—	5	—	5	ns	
	Input		t_{SSLf}	—	1	—	1	µs	
Slave access time	Slave		t_{SA}	—	20	—	20	ns	
Slave output release time	Slave		t_{REL}	—	20	—	20	ns	

Note: t_{Tcyc}: PCLKA or SCISPICLK cycle.

Note 1. Must use pins that have a letter appended to their name, for instance _A, _B, _C, to indicate group membership. SPIA is instance _B, SPIB is instance _A.

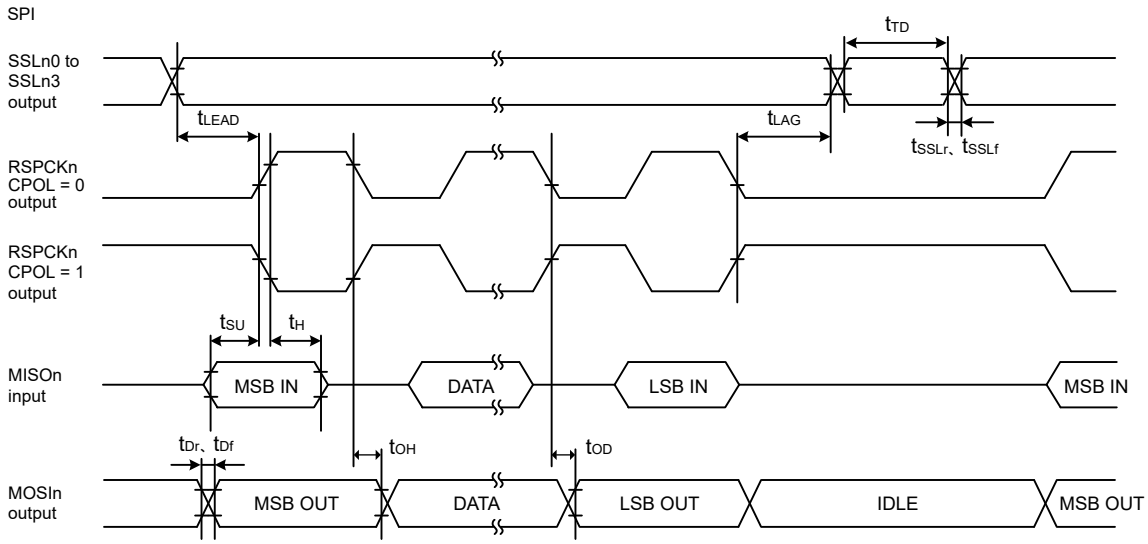
Note 2. All pins of group membership can be used.



V_{OH} = 0.7 × VCC, V_{OL} = 0.3 × VCC, V_{IH} = 0.7 × VCC, V_{IL} = 0.3 × VCC

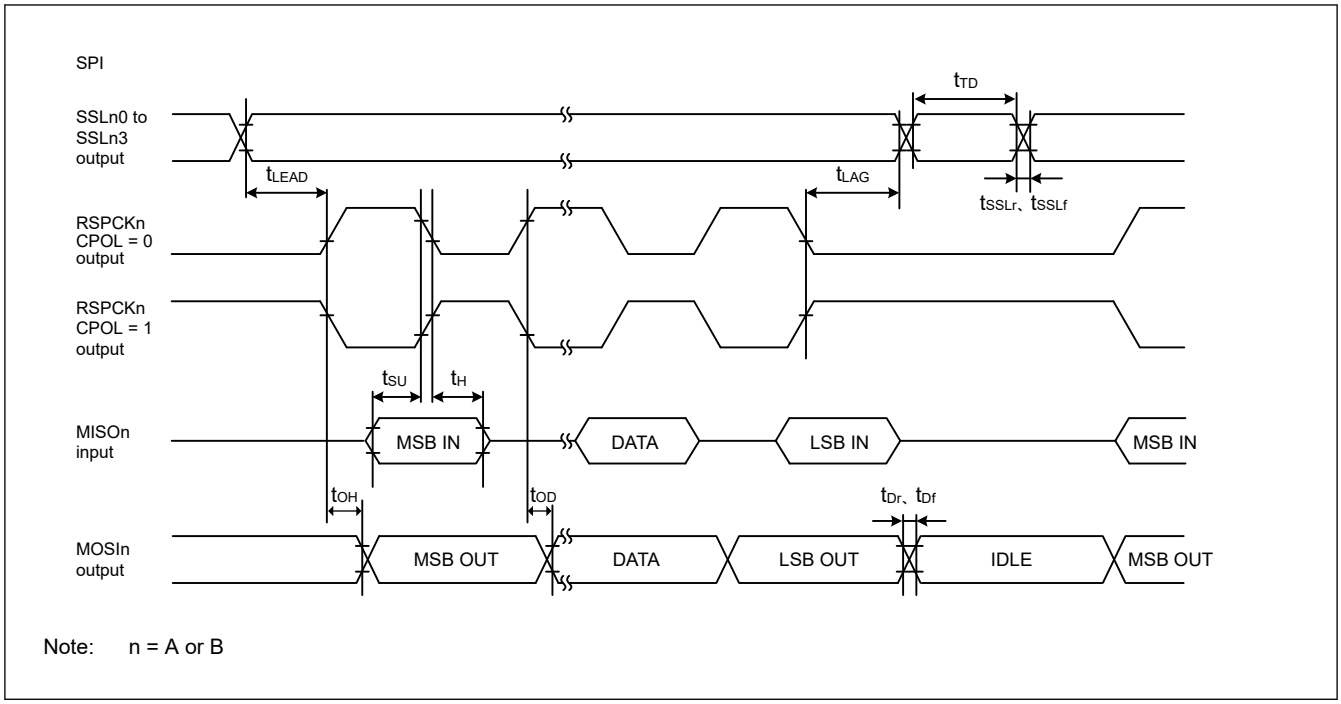
Note: n = A or B

Figure 2.39 SPI clock timing



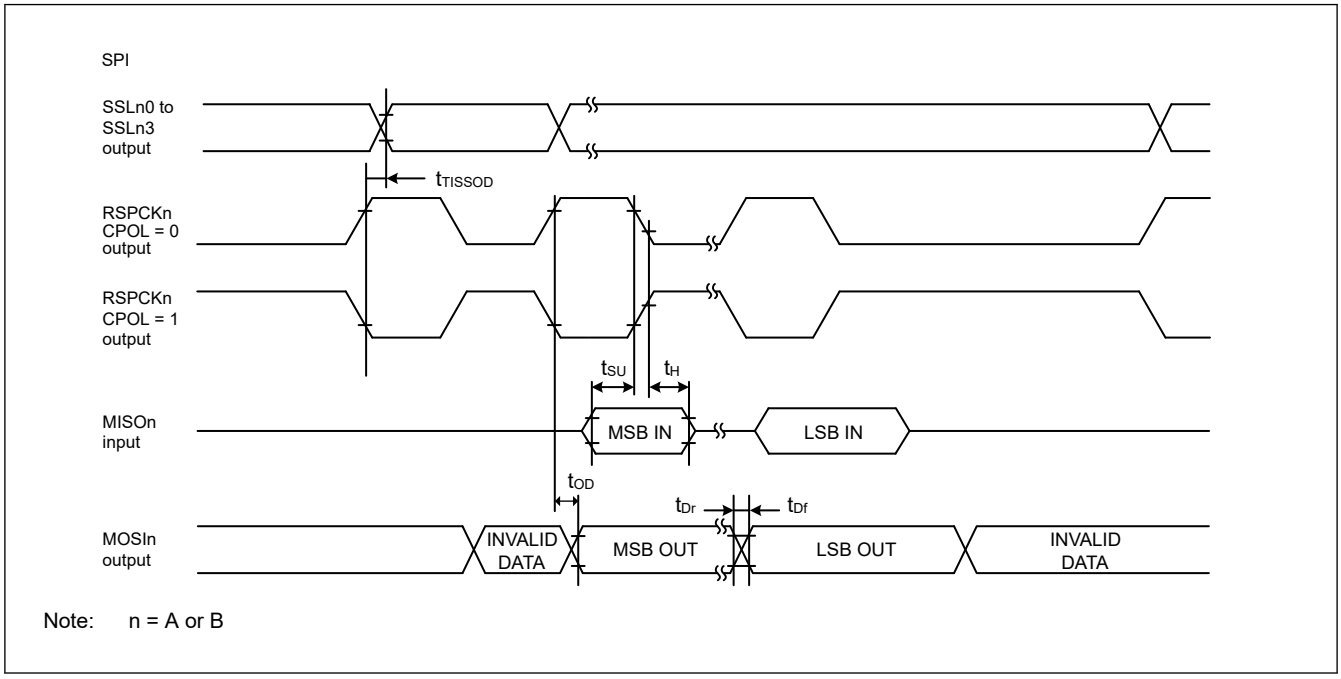
Note: n = A or B

Figure 2.40 SPI timing for Motorola SPI master when CPHA = 0



Note: n = A or B

Figure 2.41 SPI timing for Motorola SPI master when CPHA = 1



Note: n = A or B

Figure 2.42 SPI timing for TI SSP master

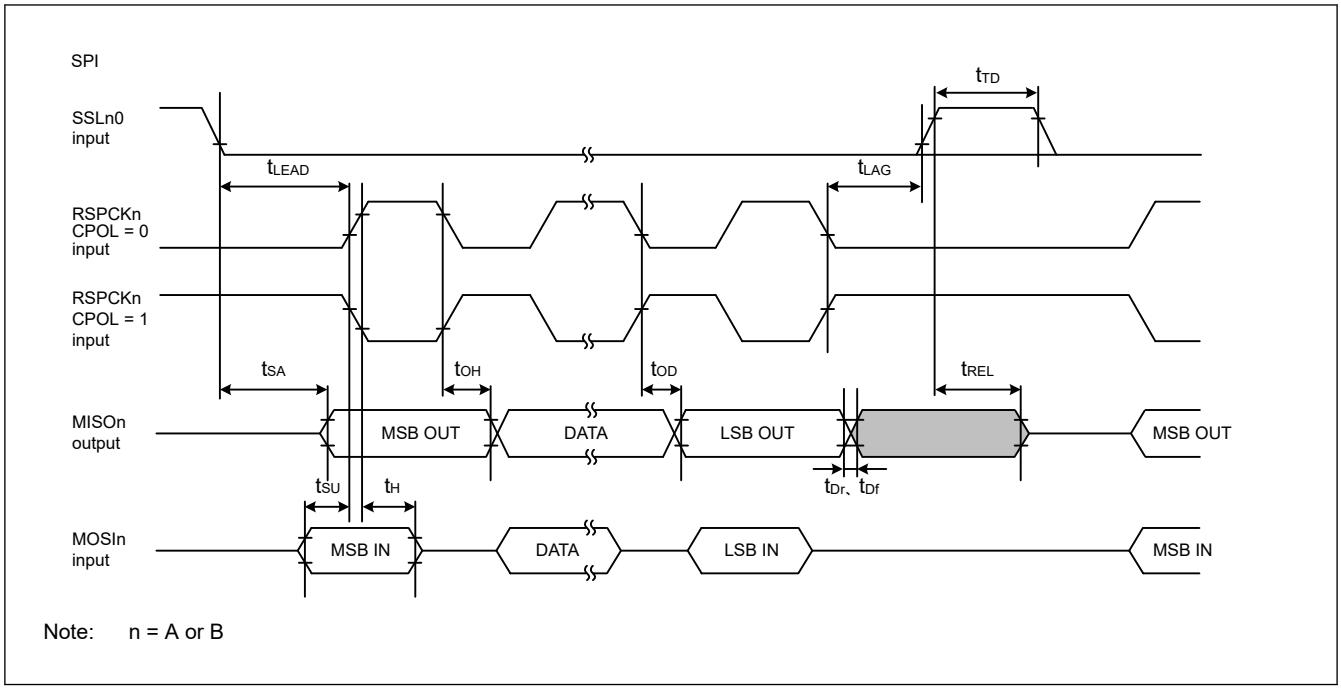


Figure 2.43 SPI timing for Motorola SPI slave when CPHA = 0

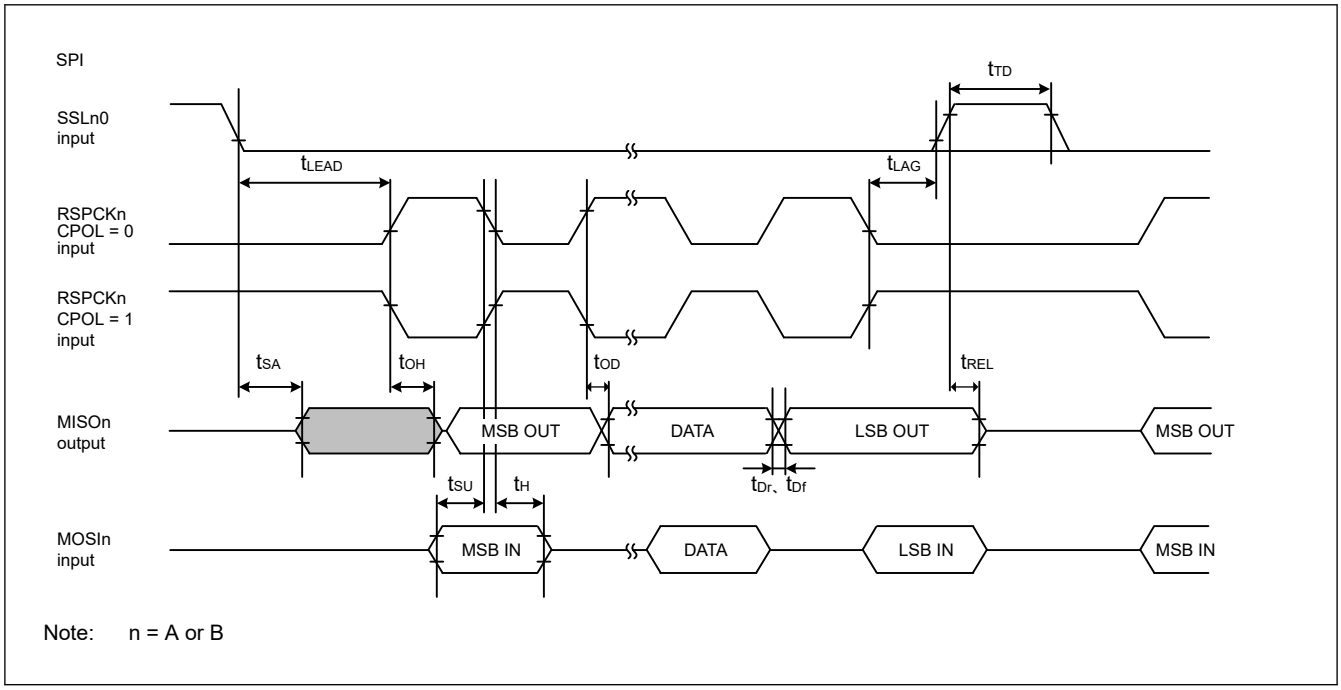


Figure 2.44 SPI timing for Motorola SPI slave when CPHA = 1

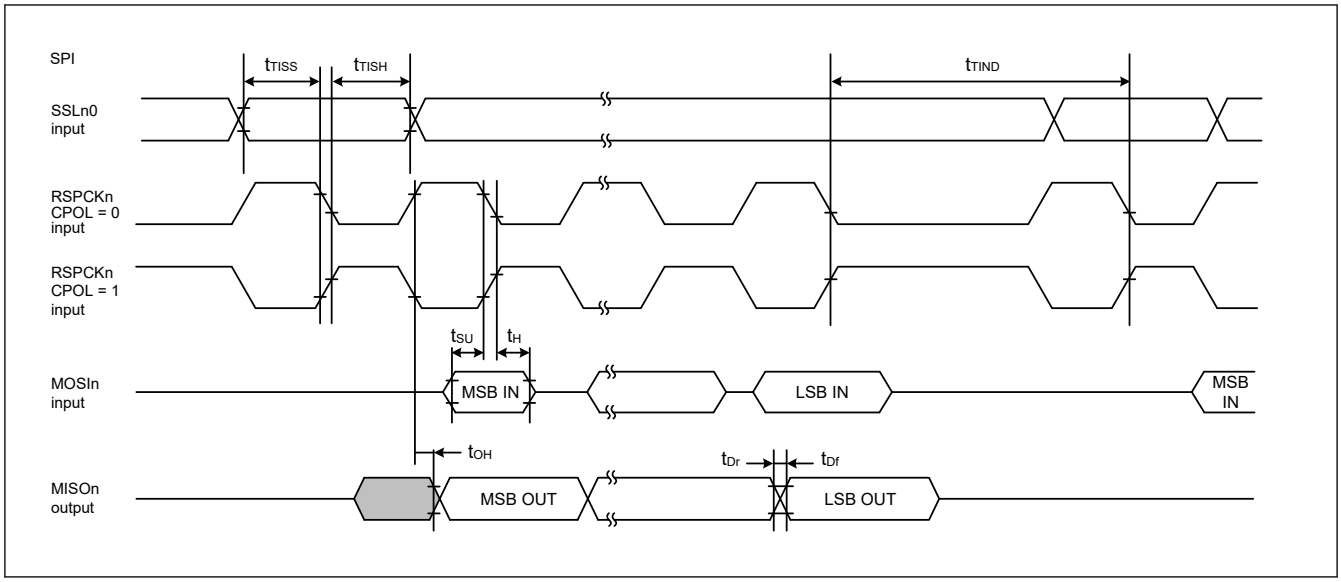


Figure 2.45 SPI timing for TI SSP slave when transmit with delay between frames

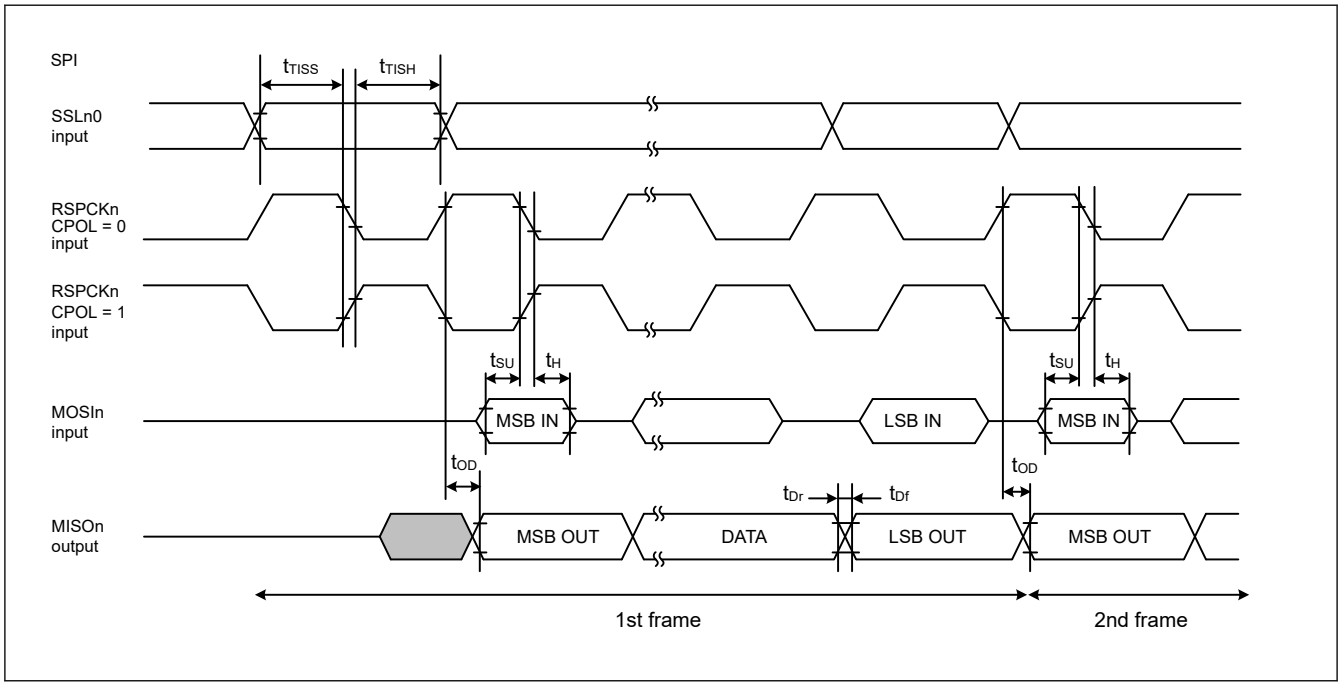


Figure 2.46 SPI timing for TI SSP slave when transmit with no delay between frames

2.3.11 IIC Timing

Table 2.29 IIC timing (1)-1

(1) Conditions: Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register for the following pins: SDA0_B, SCL0_B, SDA1_B, SCL1_B, SCL0_C, SDA0_C, SCL0_D, SDA0_D, SCL0_E, SDA0_E, SCL0_F, SDA0_F, SCL1_C, SDA1_C, SCL1_D, SDA1_D, SCL1_E, SDA1_E.
(2) The following pins do not require setting: SCL0_A, SDA0_A, SCL1_A, SDA1_A.
(3) Use pins that have a letter appended to their names, for instance _A or _B or _C or _D or _E or _F, to indicate group membership. For the IIC interface, the AC portion of the electrical characteristics is measured for each group.

Parameter		Symbol	Min	Max	Unit	Test conditions
IIC (Standard mode, SMBus) BFCTL.FMPE = 0	SCL input cycle time	t_{SCL}	10 (18) × t_{IICcyc} + 1300	—	ns	Figure 2.47
	SCL input high pulse width	t_{SCLH}	5 (9) × t_{IICcyc}	—	ns	
	SCL input low pulse width	t_{SCLL}	5 (9) × t_{IICcyc}	—	ns	
	SCL, SDA rise time	t_{Sr}	—	1000	ns	
	SCL, SDA fall time	t_{Sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA input bus free time	t_{BUF}	5 (9) × t_{IICcyc} + 300	—	ns	
	START condition input hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Repeated START condition input setup time	t_{STAS}	1000	—	ns	
	STOP condition input setup time	t_{STOS}	1000	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b *1	—	400	pF	

Note: t_{IICcyc}: IIC internal reference clock (IICφ) cycle.
Note: Values in parentheses apply when INCTL.DNFS[3:0] is set to 0011b while the digital filter is enabled with INCTL.DNFE set to 1.
Note 1. C_b indicates the total capacity of the bus line.

Table 2.30 IIC timing (1)-2

(1) Conditions: Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register for the following pins: SDA0_B, SCL0_B, SDA1_B, SCL1_B, SCL0_C, SDA0_C, SCL0_D, SDA0_D, SCL0_E, SDA0_E, SCL0_F, SDA0_F, SCL1_C, SDA1_C, SCL1_D, SDA1_D, SCL1_E, SDA1_E.
(2) The following pins do not require setting: SCL0_A, SDA0_A, SCL1_A, SDA1_A.
(3) Use pins that have a letter appended to their names, for instance _A or _B or _C or _D or _E or _F, to indicate group membership. For the IIC interface, the AC portion of the electrical characteristics is measured for each group.

Parameter		Symbol	Min	Max	Unit	Test conditions
IIC (Fast-mode)	SCL input cycle time	t_{SCL}	10 (18) × t_{IICcyc} + 600	—	ns	Figure 2.47
	SCL input high pulse width	t_{SCLH}	5 (9) × t_{IICcyc}	—	ns	
	SCL input low pulse width	t_{SCLL}	5 (9) × t_{IICcyc}	—	ns	
	SCL, SDA rise time	t_{Sr}	20 × (external pullup voltage/ 5.5V)*1	300	ns	
	SCL, SDA fall time	t_{Sf}	20 × (external pullup voltage/ 5.5V)*1	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA input bus free time	t_{BUF}	5 (9) × t_{IICcyc} + 300	—	ns	
	START condition input hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Repeated START condition input setup time	t_{STAS}	300	—	ns	
	STOP condition input setup time	t_{STOS}	300	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b*2	—	400	pF	

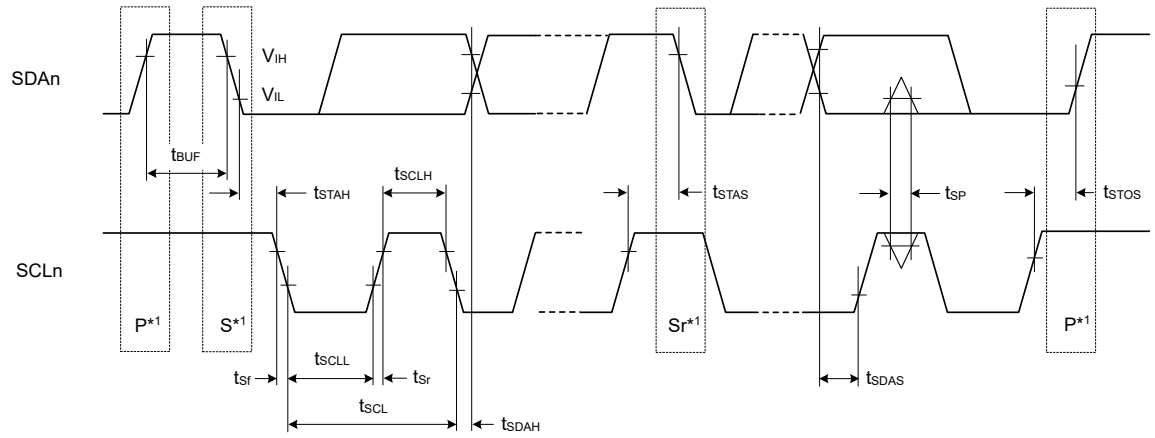
Note: t_{IICcyc}: IIC internal reference clock (IICφ) cycle.
Note: Values in parentheses apply when INCTL.DNFS[3:0] is set to 0011b while the digital filter is enabled with INCTL.DNFE set to 1.
Note: Must use pins that have a letter appended to their name, for instance _A, _B, to indicate group membership. For the IIC interface, the AC portion of the electrical characteristics is measured for each group.
Note 1. Only supported for SCL0_A, SDA0_A, SCL1_A, and SDA1_A. Other ports depend on DC characteristics.
Note 2. C_b indicates the total capacity of the bus line.

Table 2.31 IIC timing (1)-3

Setting of the SCL0_A, SDA0_A pins are not required with the Port Drive Capability bit in the PmnPFS register.

Parameter		Symbol	Min	Max	Unit	Test conditions
IIC (Fast-mode+) BFCTL.FMPE = 1	SCL input cycle time	t_{SCL}	10 (18) × t_{IICcyc} + 240	—	ns	Figure 2.47
	SCL input high pulse width	t_{SCLH}	5 (9) × t_{IICcyc}	—	ns	
	SCL input low pulse width	t_{SCLL}	5 (9) × t_{IICcyc}	—	ns	
	SCL, SDA rise time	t_{Sr}	—	120	ns	
	SCL, SDA fall time	t_{Sf}	—	120	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA input bus free time	t_{BUF}	5 (9) × t_{IICcyc} + 120	—	ns	
	START condition input hold time	t_{STAH}	t_{IICcyc} + 120	—	ns	
	Repeated START condition input setup time	t_{STAS}	120	—	ns	
	STOP condition input setup time	t_{STOS}	120	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 30	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b *1	—	550	pF	

Note: t_{IICcyc}: IIC internal reference clock (IICφ) cycle.
Note: Values in parentheses apply when INCTL.DNFS[3:0] is set to 0011b while the digital filter is enabled with INCTL.DNFE set to 1.
Note: Targets are SCL0_A and SDA0_A.
Note 1. C_b indicates the total capacity of the bus line.



Note 1. S, P, and Sr indicate the following conditions:
S: Start condition
P: Stop condition
Sr: Restart condition

Figure 2.47 I²C bus interface input/output timing

Table 2.32 IIC timing (2)

Setting of the SCL0_A, SDA0_A pins are not required with the Port Drive Capability bit in the PmnPFS register.

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
IIC (Hs-mode) BFCTL.HSME = 1	SCL input cycle time		t_{SCL}	10 (12) × t_{IICcyc} + 80	—	—	ns	Figure 2.48
	SCL input high pulse width		t_{SCLH}	5 (6) × t_{IICcyc}	—	—	ns	
	SCL input low pulse width		t_{SCLL}	5 (6) × t_{IICcyc}	—	—	ns	
	SCL rise time	C_b = 400pF	t_{SrCL}	—	—	80	ns	
		C_b = 100pF		—	—	40	ns	
	SDA rise time	C_b = 400pF	t_{SrDA}	—	—	160	ns	
		C_b = 100pF		—	—	80	ns	
	SCL fall time	C_b = 400pF	t_{SfCL}	—	—	80	ns	
		C_b = 100pF		—	—	40	ns	
	SDA fall time	C_b = 400pF	t_{SfDA}	—	—	160	ns	
		C_b = 100pF		—	—	80	ns	
	SCL, SDA input spike pulse removal time		t_{SP}	0	—	1 (1) × t_{IICcyc}	ns	
	START condition input hold time		t_{STAH}	t_{IICcyc} + 40	—	—	ns	
	Repeated START condition input setup time		t_{STAS}	40	—	—	ns	
	STOP condition input setup time		t_{STOS}	40	—	—	ns	
	Data input setup time		t_{SDAS}	10	—	—	ns	
	Data input hold time	C_b = 400pF	t_{SDAH}	0	—	150	ns	
		C_b = 100pF		0	—	70	ns	
	SCL, SDA capacitive load		C_b *1	—	—	400	pF	
	SCL output minimum high pulse width	C_b = 400pF	t_{SCLH}	—	120	225	ns	
		C_b = 100pF		—	60	130		
	SCL output minimum low pulse width	C_b = 400pF	t_{SCLL}	—	—	320	ns	
		C_b = 100pF		—	—	160		

Note: t_{IICcyc}: IIC internal reference clock (IICφ) cycle.
Note: Values in parentheses apply when INCTL.DNFS[3:0] is set to 0011b while the digital filter is enabled with INCTL.DNFE set to 1.
Note: Targets are SCL0_A and SDA0_A.
Note 1. C_b indicates the total capacity of the bus line.

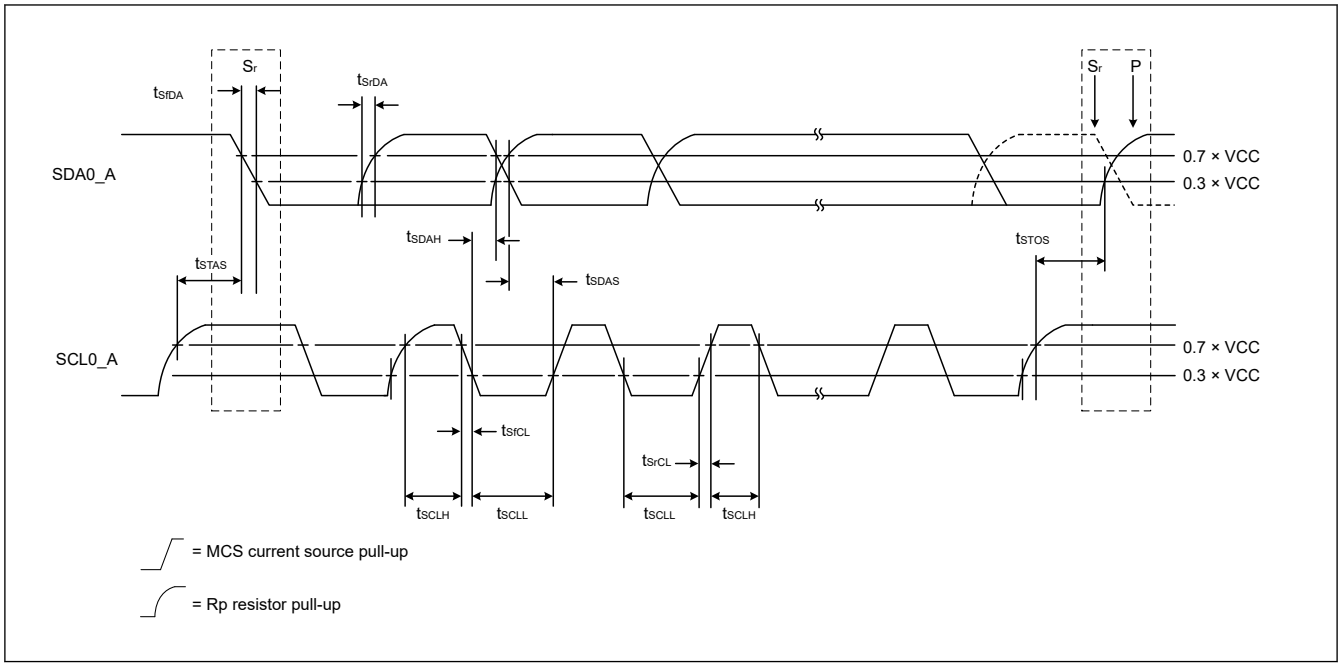


Figure 2.48 I²C bus interface input/output timing (Hs-mode)

2.3.12 CANFD Timing

Table 2.33 CANFD interface timing

Parameter	Symbol	CAN		CAN-FD		Unit	Test conditions
		Min	Max	Min	Max		
Internal delay time	t_{node}	—	100	—	75	ns	Figure 2.49

Note: $t_{node} = t_{d(CTX)} + t_{d(CRX)}$

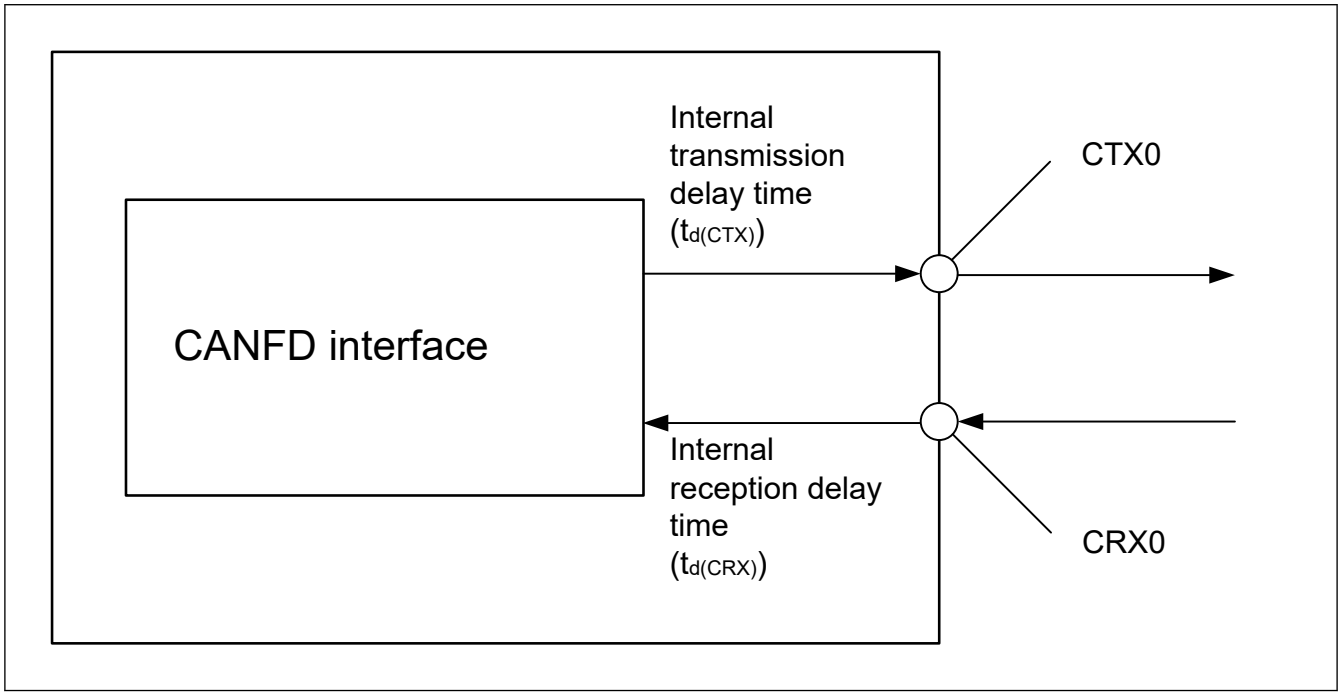


Figure 2.49 CANFD interface condition

2.4 A/D Converter Characteristics

Table 2.34 A/D conversion characteristics (Common)

Parameter						Min	Typ	Max	Unit	Test conditions
A/D conversion clock frequency(ADCLK)						25	50	60	MHz	—
Successive approximation time						100	—	140	ns	—
A/D sampling time	Self-calibration				SAR mode	1 × t_{ADcyc} + 40	—	—	ns	—
					Oversampling mode	1 × t_{ADcyc} + 40	—	—	ns	—
					Hybrid mode	1 × t_{ADcyc} + 60	—	—	ns	—
	Self-diagnosis				SAR mode	1 × t_{ADcyc} + 40	—	—	ns	—
					Oversampling mode	1 × t_{ADcyc} + 40	—	—	ns	—
					Hybrid mode	1 × t_{ADcyc} + 60	—	—	ns	—
	A/D conversion	High-precision high-speed channels	Without channel-dedicated sample-and-hold circuits	(AN000 to AN005) (AN006 to AN011) (AN018 to AN019)	SAR mode	1 × t_{ADcyc} + 40	—	—	ns	—
					Oversampling mode	1 × t_{ADcyc} + 40	—	—	ns	—
					Hybrid mode	1 × t_{ADcyc} + 60	—	—	ns	—
			With channel-dedicated sample-and-hold circuits	(AN000 to AN005) (AN006 to AN011)	SAR mode	1 × t_{ADcyc} + 160	—	—	ns	—
					Hybrid mode	1 × t_{ADcyc} + 160	—	—	ns	—
		High-precision middle-speed channels		(AN012 to AN017)	SAR mode	180	—	—	ns	—
					Oversampling mode	180	—	—	ns	—
					Hybrid mode	180	—	—	ns	—
		Normal-precision low-speed channels		(AN020 to AN028)	SAR mode	400	—	—	ns	—
					Oversampling mode	400	—	—	ns	—
					Hybrid mode	400	—	—	ns	—
Channel-dedicated sample-and-hold circuits	Sampling time	Self-calibration				1 × t_{ADcyc} + 400	—	—	ns	—
		A/D conversion				400	—	—	ns	—
	Hold mode switching time					40	—	—	ns	—
	Hold time					—	—	5	µs	—
Operation stabilization time	A/D start-up time					2.0	—	—	µs	—
	Channel-dedicated sample-and-hold circuits start-up time					2.0	—	—	µs	—
	A/D shut-down time					1.0	—	—	µs	—

Note: t_{ADcyc} : ADCLK cycle

Table 2.35 A/D conversion characteristics (SAR mode) (1 of 2)

Parameter					Min	Typ	Max	Unit	Test conditions
SAR mode	Analog input voltage range				VREFL0	—	VREFH0	V	—
	Resolution				—	—	12	bit	—
	Quantization error				—	±0.5	—	LSB	—
	High-precision high-speed channels (AN000 to AN005) (AN006 to AN011) (AN018 to AN019)*3	Without channel-dedicated sample-and-hold circuits*3	Conversion time*1	Normal conversion	0.16	—	—	µs	• ADCLK: 50 MHz • Sampling time: 3 ADCLK • Successive approximation time: 5 ADCLK • Signal source impedance: 50 Ω or less
				With Averaging mode (4-time conversion)	0.64	—	—	µs	
			Offset error		—	±1.0	±3.0	LSB	—
			Full-scale error		—	±1.5	±2.5	LSB	—
			Absolute accuracy	Normal conversion	—	±5.5	±7.0	LSB	—
				With Averaging mode (4-time conversion)	—	±4.5	±5.5	LSB	—
			Total unadjusted error (TUE)*4		—	±3.5	±4.0	LSB	—
			DNL differential nonlinearity error		—	-1 to +1.5	-1 to +2.5	LSB	—
			INL integral nonlinearity error		—	±2.0	±3.0	LSB	—
		With channel-dedicated sample-and-hold circuits	Conversion time*2	Normal conversion	0.72	—	—	µs	• ADCLK: 50 MHz • Sampling time of channel-dedicated sample-and-hold circuits: 20 ADCLK • Hold mode switching time of channel-dedicated sample-and-hold circuits: 2 ADCLK • Sampling time: 9 ADCLK • Successive approximation time: 5 ADCLK • Signal source impedance: 50 Ω or less
				With Averaging mode (4-time conversion)	2.88	—	—	µs	
			Offset error		—	±0.5	±1.0	LSB	—
			Full-scale error		—	±1.5	±1.5	LSB	—
			Absolute accuracy	Normal conversion	—	±5.0	±7.0	LSB	—
				With Averaging mode (4-time conversion)	—	±4.0	±5.0	LSB	—
			Total unadjusted error (TUE)*4		—	±3.0	±3.4	LSB	—
			DNL differential nonlinearity error		—	-1 to +1.5	-1 to +2.5	LSB	—
			INL integral nonlinearity error		—	±2.0	±3.0	LSB	—

Table 2.35 A/D conversion characteristics (SAR mode) (2 of 2)

Parameter				Min	Typ	Max	Unit	Test conditions
SAR mode	High-precision middle-speed channels (AN012 to AN017)	Conversion time[*1]	Normal conversion	0.28	—	—	µs	• ADCLK: 50 MHz • Sampling time: 9 ADCLK • Successive approximation time: 5 ADCLK • Signal source impedance: 50 Ω or less
			With Averaging mode (4-time conversion)	1.12	—	—	µs	
		Offset error		—	±1.0	±1.5	LSB	—
		Full-scale error		—	±1.0	±2.5	LSB	—
		Absolute accuracy	Normal conversion	—	±4.0	±7.0	LSB	—
			With Averaging mode (4-time conversion)	—	±3.0	±5.5	LSB	—
		Total unadjusted error (TUE)[*4]		—	±3.4	±4.4	LSB	—
		DNL differential nonlinearity error		—	-1 to +1.5	-1 to +2.5	LSB	—
		INL integral nonlinearity error		—	±2.0	±3.0	LSB	—
	Normal-precision low-speed channels (AN020 to AN028)	Conversion time[*1]	Normal conversion	0.50	—	—	µs	• ADCLK: 50 MHz • Sampling time: 20 ADCLK • Successive approximation time: 5 ADCLK • Signal source impedance: 50 Ω or less
			With Averaging mode (4-time conversion)	2.00	—	—	µs	
		Offset error		—	±1.0	±2.5	LSB	—
		Full-scale error		—	±1.5	±2.5	LSB	—
		Absolute accuracy	Normal conversion	—	±5.5	±8.0	LSB	—
			With Averaging mode (4-time conversion)	—	±5.5	±7.0	LSB	—
		Total unadjusted error (TUE)[*4]		—	±4.2	±5.3	LSB	—
		DNL differential nonlinearity error		—	-1 to +1.5	-1 to +2.5	LSB	—
		INL integral nonlinearity error		—	±2.0	±4.0	LSB	—

Note 1. Without channel-dedicated sample-and-hold circuits; The conversion time is the sum of the sampling time and the successive approximation time. Each of the above state is indicated for the test conditions.
Note 2. With channel-dedicated sample-and-hold circuits; The conversion time is the sum of the sampling time of channel-dedicated sample-and-hold circuits, the hold mode switching time, the sampling time and the successive approximation time. Each of the above state is indicated for the test conditions.
Note 3. Channel-dedicated sample-and-hold circuits are not available in these channels.
Note 4. Excludes quantization error (±0.5 LSB).

Table 2.36 A/D conversion characteristics (Oversampling mode and Hybrid mode) (1)

Parameter				Min	Typ	Max	Unit	Test conditions
Oversampling mode and Hybrid mode	Analog input voltage range	Single-ended input voltage		VREFL0	—	VREFH0	V	—
		Differential input voltage*1		-VREFH0	—	+VREFH0	V	—
	Resolution			—	—	16	bit	—
	Oversampling period	Oversampling mode		0.16	—	—	µs	• ADCLK: 50 MHz • Sampling time: 3 ADCLK • Successive approximation time: 5 ADCLK • Without disconnection detection assist function • Signal source impedance: 50 Ω or less
		Hybrid mode*3		0.18	—	—	µs	• ADCLK: 50 MHz • Sampling time: 4 ADCLK • Successive approximation time: 5 ADCLK • Without disconnection detection assist function • Signal source impedance: 50 Ω or less
	Digital filter characteristics *2	Sinc filter	Initial delay	—	22	—	/Fos	—
			Group delay	—	11	—		—
			Normalized Cutoff Frequency	—	0.033	—	Fin/Fos	—
		Minimum phase filter	Initial delay	—	22	—	/Fos	—
			Group delay	—	2	—		—
			Normalized Cutoff Frequency	—	0.116	—	Fin/Fos	—
			Passband ripple	—	<± 0.01	—	dB	—

Note: Fos is oversampling frequency. When in Hybrid mode, Fos is 1/ (the sum of the oversampling periods of each analog channel assigned to the scan group).

Note 1. Differential input voltage is (A_{INP} - A_{INN})
- A_{INP} is input voltage of ANx, and VREFL0 ≤ A_{INP} ≤ VREFH0.
- A_{INN} is input voltage of ANy, and VREFL0 ≤ A_{INN} ≤ VREFH0.
  (x = 2i, y = 2i +1, i = 0, 1, 2… (any integer))

Note 2. See Figure 2.50 and Figure 2.51.

Note 3. Value per channel.

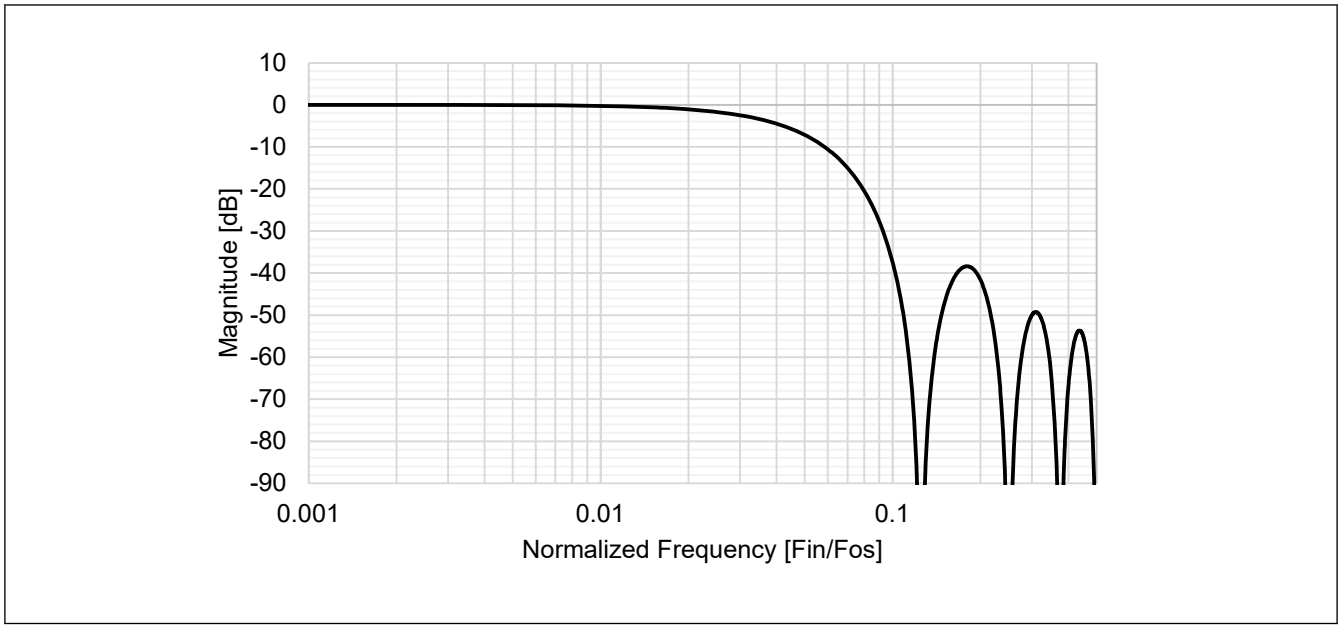


Figure 2.50 Digital filter characteristics (Sinc filter)

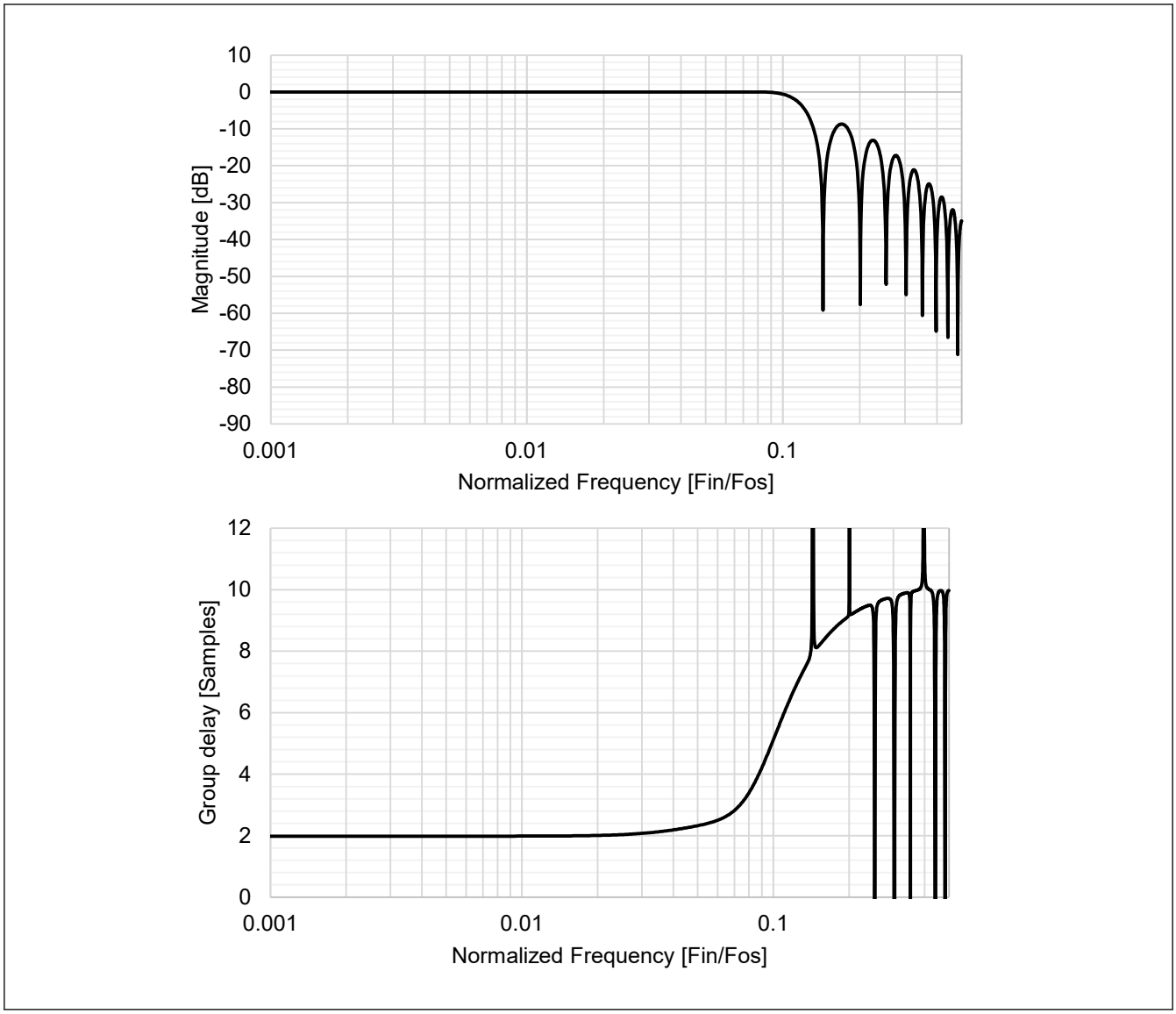


Figure 2.51 Digital filter characteristics (Minimum phase filter)

Table 2.37 A/D conversion characteristics (Oversampling mode and Hybrid mode) (2)

Parameter				Min	Typ	Max	Unit	Test conditions
Oversampling mode and Hybrid mode (AN000 to AN005) (AN006 to AN011) (AN018 to AN019) (AN012 to AN017)	Sinc filter	Single-ended input	SNDR signal-to-noise and distortion ratio	—	80	—	dB	• ADCLK: 50 MHz • Sampling time: High-precision high-speed channels (Oversampling mode): 3 ADCLK High-precision high-speed channels (Hybrid mode): 4 ADCLK High-precision middle-speed channels: 9 ADCLK • Successive approximation time: 5 ADCLK • Signal source impedance: 50 Ω or less • Input frequency: Oversampling mode: 10 kHz Hybrid mode: 4 kHz • Without channel-dedicated sample-and-hold circuits
			ENOB effective number of bits	—	13	—	bit	
		Differential input	SNDR signal-to-noise and distortion ratio	—	86	—	dB	
			ENOB effective number of bits	—	14	—	bit	
	Minimum phase filter	Single-ended input	SNDR signal-to-noise and distortion ratio	—	68	—	dB	
			ENOB effective number of bits	—	11	—	bit	
		Differential input	SNDR signal-to-noise and distortion ratio	—	74	—	dB	
			ENOB effective number of bits	—	12	—	bit	

Table 2.38 A/D conversion characteristics (Oversampling mode)

Parameter				Min	Typ	Max	Unit	Test conditions
Oversampling mode (AN000 to AN005) (AN006 to AN011) (AN018 to AN019) (AN012 to AN017) (AN020 to AN028)	Single-ended input	Unit0	Offset error	—	±8.0	—	LSB	• ADCLK: 50 MHz • Sampling time: High-precision high-speed channels: 3 ADCLK High-precision middle-speed channels: 9 ADCLK Normal-precision low-speed channels: 20 ADCLK • Successive approximation time: 5 ADCLK • Signal source impedance: 50 Ω or less • Digital filter: Sinc filter • Without channel-dedicated sample-and-hold circuits
			Gain error	—	±32.0	—		
			DNL differential nonlinearity error*1	—	±4.0	—		
			INL integral nonlinearity error*1	—	±8.0	—		
		Unit1	Offset error	—	±8.0	—		
			Gain error	—	±32.0	—		
			DNL differential nonlinearity error*1	—	±4.0	—		
			INL integral nonlinearity error*1	—	±8.0	—		
	Differential input	Unit0	Offset error	—	±4.0	—		
			Gain error	—	±14.0	—		
			DNL differential nonlinearity error*1	—	±2.0	—		
			INL integral nonlinearity error*1	—	±4.0	—		
		Unit1	Offset error	—	±4.0	—		
			Gain error	—	±14.0	—		
			DNL differential nonlinearity error*1	—	±2.0	—		
			INL integral nonlinearity error*1	—	±4.0	—		

Note 1. Test conditions: 0.2% to 99.8% of the analog input voltage range.

Table 2.39 A/D conversion characteristics (Hybrid mode) (1 of 2)

Parameter					Min	Typ	Max	Unit	Test conditions
Hybrid mode (AN000 to AN005) (AN006 to AN011) (AN018 to AN019)*1 (AN012 to AN017)*1 (AN020 to AN028)*1	Without channel-dedicated sample-and-hold circuits*1	Single-ended input	Unit0	Offset error	—	±8.0	—	LSB	• ADCLK: 50 MHz • Sampling time: High-precision high-speed channels: 4 ADCLK High-precision middle-speed channels: 9 ADCLK Normal-precision low-speed channels: 20 ADCLK • Successive approximation time: 5 ADCLK • Signal source impedance: 50 Ω or less • Digital filter: Sinc filter
				Gain error	—	±40.0	—		
				DNL differential nonlinearity error*2	—	±4.0	—		
				INL integral nonlinearity error*2	—	±8.0	—		
			Unit1	Offset error	—	±8.0	—		
				Gain error	—	±40.0	—		
				DNL differential nonlinearity error*2	—	±4.0	—		
				INL integral nonlinearity error*2	—	±8.0	—		
		Differential input	Unit0	Offset error	—	±4.0	—		
				Gain error	—	±20.0	—		
				DNL differential nonlinearity error*2	—	±2.0	—		
				INL integral nonlinearity error*2	—	±4.0	—		
			Unit1	Offset error	—	±4.0	—		
				Gain error	—	±20.0	—		
				DNL differential nonlinearity error*2	—	±2.0	—		
				INL integral nonlinearity error*2	—	±4.0	—		

Table 2.39 A/D conversion characteristics (Hybrid mode) (2 of 2)

Parameter					Min	Typ	Max	Unit	Test conditions
Hybrid mode (AN000 to AN005) (AN006 to AN011) (AN018 to AN019)*1 (AN012 to AN017)*1 (AN020 to AN028)*1	With channel-dedicated sample-and-hold circuits	Single-ended input	Unit0	Offset error	—	8 ± 72	—	LSB	• ADCLK: 50 MHz • Sampling time of channel-dedicated sample-and-hold circuits: 20 ADCLK • Hold mode switching time of channel-dedicated sample-and-hold circuits: 2 ADCLK • Sampling time: 9 ADCLK • Successive approximation time: 5 ADCLK • Signal source impedance: 50 Ω or less • Digital filter: Sinc filter
				Gain error	—	-23 ± 72	—		
				DNL differential nonlinearity error*2	—	±4.0	—		
				INL integral nonlinearity error*2	—	±8.0	—		
			Unit1	Offset error	—	36 ± 72	—		
				Gain error	—	-23 ± 72	—		
				DNL differential nonlinearity error*2	—	±4.0	—		
				INL integral nonlinearity error*2	—	±8.0	—		
		Differential input	Unit0	Offset error	—	8 ± 72	—		
				Gain error	—	-15 ± 36	—		
				DNL differential nonlinearity error*2	—	±4.0	—		
				INL integral nonlinearity error*2	—	±8.0	—		
			Unit1	Offset error	—	36 ± 72	—		
				Gain error	—	-15 ± 36	—		
				DNL differential nonlinearity error*2	—	±4.0	—		
				INL integral nonlinearity error*2	—	±8.0	—		

Note 1. Channel-dedicated sample-and-hold circuits are not available in these channels.
Note 2. Test conditions: 0.2% to 99.8% of the analog input voltage range.

Table 2.40 A/D internal reference voltage characteristics

Parameter	Min	Typ	Max	Unit	Test conditions
A/D internal reference voltage	1.13	1.18	1.23	V	
Sampling time	4.15	—	—	µs	

Table 2.41 A/D conversion characteristics of D/A output

Parameter	Min	Typ	Max	Unit	Test conditions
Sampling time	1	—	—	µs	

2.5 DAC12 Characteristics

Table 2.42 D/A conversion characteristics (1 of 2)

Parameter	Min	Typ	Max	Unit	Test conditions
Resolution	—	—	12	Bits	—
Without output amplifier					
Absolute accuracy	—	—	±24	LSB	Resistive load 2 MΩ
INL	—	±2.0	±8.0	LSB	Resistive load 2 MΩ
DNL	—	±1.0	±2.0	LSB	—
Output impedance	—	8.5	—	kΩ	—

Table 2.42 D/A conversion characteristics (2 of 2)

Parameter	Min	Typ	Max	Unit	Test conditions
Conversion time	—	—	3	µs	Resistive load 2 MΩ, Capacitive load 20 pF
Output voltage range	0	—	AVCC0	V	—
With output amplifier					
INL	—	±2.0	±4.0	LSB	—
DNL	—	±1.0	±2.0	LSB	—
Conversion time	—	—	4.0	µs	—
Resistive load	5	—	—	kΩ	—
Capacitive load	—	—	50	pF	—
Output voltage range	0.2	—	AVCC0 – 0.2	V	—

2.6 TSN Characteristics

Table 2.43 TSN characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Relative accuracy	—	—	± 1.0	—	°C	—
Temperature slope	—	—	4.0	—	mV/°C	—
Output voltage (at 25 °C)	—	—	1.24	—	V	—
Temperature sensor start time	t_{START}	—	—	30	µs	—
Sampling time	—	4.15	—	—	µs	—

2.7 ACMPHS Characteristics

Table 2.44 ACMPHS characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input offset voltage	V_{IO}	—	—	40	mV	
Reference voltage range	V_{REF}	0	—	AVCC0	V	
Input voltage range	V_I	0	—	AVCC0	V	
Output delay	$t_{tot(r)}$	—	—	200	ns	VOD = 100 mV CMPCTL.CDFS = 0
	$t_{tot(f)}$	—	—	200	ns	
Waiting time for stabilization following switching of the input	t_{cwait}	300	—	—	ns	
Operation stabilization time	t_{cmp}	—	—	1	µs	

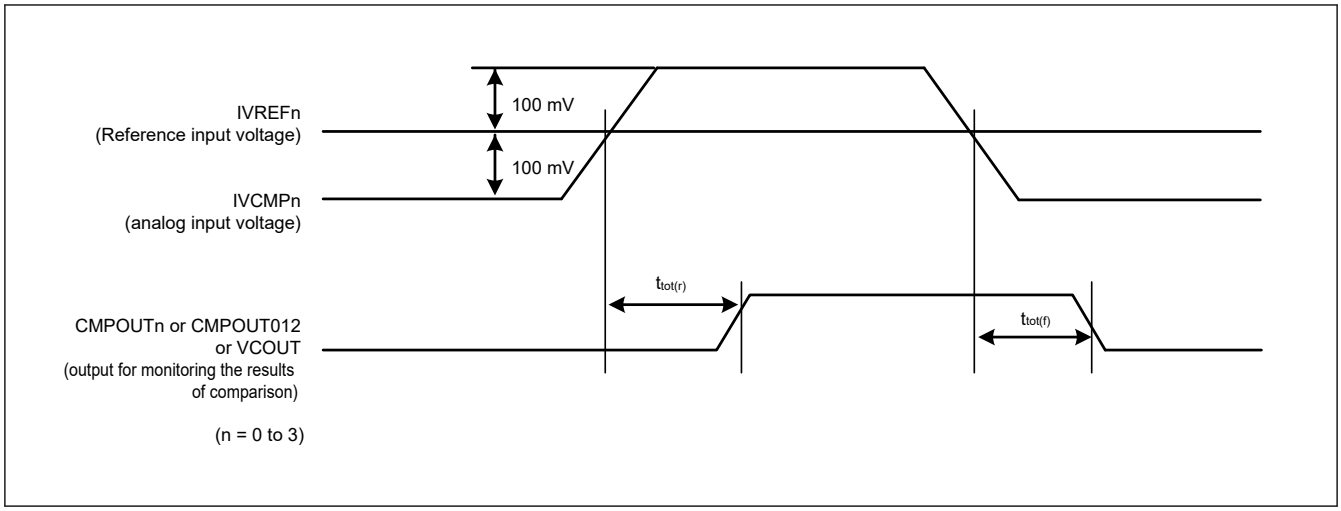


Figure 2.52 Comparator Response Time

2.8 PGA Characteristics

Table 2.45 PGA characteristics in Single-ended input mode (1 of 2)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Offset error	Voff	-8	—	8	mV	
PGAVSS input voltage range	PGAVSS	0	—	0	V	
Single-ended input voltage range	AIN0 (G = 2.000)	0.05 × AVCC0	—	0.45 × AVCC0	V	
	AIN1 (G = 2.500)	0.047 × AVCC0	—	0.36 × AVCC0	V	
	AIN2 (G = 2.667)	0.046 × AVCC0	—	0.337 × AVCC0	V	
	AIN3 (G = 2.857)	0.046 × AVCC0	—	0.32 × AVCC0	V	
	AIN4 (G = 3.077)	0.045 × AVCC0	—	0.292 × AVCC0	V	
	AIN5 (G = 3.333)	0.044 × AVCC0	—	0.265 × AVCC0	V	
	AIN6 (G = 3.636)	0.042 × AVCC0	—	0.247 × AVCC0	V	
	AIN7 (G = 4.000)	0.04 × AVCC0	—	0.212 × AVCC0	V	
	AIN8 (G = 4.444)	0.036 × AVCC0	—	0.191 × AVCC0	V	
	AIN9 (G = 5.000)	0.033 × AVCC0	—	0.17 × AVCC0	V	
	AIN10 (G = 5.714)	0.031 × AVCC0	—	0.148 × AVCC0	V	
	AIN11 (G = 6.667)	0.029 × AVCC0	—	0.127 × AVCC0	V	
	AIN12 (G = 8.000)	0.027 × AVCC0	—	0.09 × AVCC0	V	
	AIN13 (G = 10.000)	0.025 × AVCC0	—	0.08 × AVCC0	V	
	AIN14 (G = 13.333)	0.023 × AVCC0	—	0.06 × AVCC0	V	

Table 2.45 PGA characteristics in Single-ended input mode (2 of 2)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Output voltage range*1	PGAOUT0 (G = 2.000)	0.100 × AVCC0	—	0.900 × AVCC0	V	
	PGAOUT1 (G = 2.500)	0.118 × AVCC0	—	0.900 × AVCC0	V	
	PGAOUT2 (G = 2.667)	0.123 × AVCC0	—	0.899 × AVCC0	V	
	PGAOUT3 (G = 2.857)	0.131 × AVCC0	—	0.914 × AVCC0	V	
	PGAOUT4 (G = 3.077)	0.138 × AVCC0	—	0.898 × AVCC0	V	
	PGAOUT5 (G = 3.333)	0.147 × AVCC0	—	0.883 × AVCC0	V	
	PGAOUT6 (G = 3.636)	0.153 × AVCC0	—	0.898 × AVCC0	V	
	PGAOUT7 (G = 4.000)	0.160 × AVCC0	—	0.848 × AVCC0	V	
	PGAOUT8 (G = 4.444)	0.160 × AVCC0	—	0.849 × AVCC0	V	
	PGAOUT9 (G = 5.000)	0.165 × AVCC0	—	0.850 × AVCC0	V	
	PGAOUT10 (G = 5.714)	0.177 × AVCC0	—	0.846 × AVCC0	V	
	PGAOUT11 (G = 6.667)	0.193 × AVCC0	—	0.847 × AVCC0	V	
	PGAOUT12 (G = 8.000)	0.216 × AVCC0	—	0.720 × AVCC0	V	
	PGAOUT13 (G = 10.000)	0.250 × AVCC0	—	0.800 × AVCC0	V	
	PGAOUT14 (G = 13.333)	0.307 × AVCC0	—	0.800 × AVCC0	V	
Gain error	Gerr0 (G = 2.000)	-1.0	—	1.0	%	
	Gerr1 (G = 2.500)	-1.0	—	1.0	%	
	Gerr2 (G = 2.667)	-1.0	—	1.0	%	
	Gerr3 (G = 2.857)	-1.0	—	1.0	%	
	Gerr4 (G = 3.007)	-1.0	—	1.0	%	
	Gerr5 (G = 3.333)	-1.5	—	1.5	%	
	Gerr6 (G = 3.636)	-1.5	—	1.5	%	
	Gerr7 (G = 4.000)	-1.5	—	1.5	%	
	Gerr8 (G = 4.444)	-2.0	—	2.0	%	
	Gerr9 (G = 5.000)	-2.0	—	2.0	%	
	Gerr10 (G = 5.714)	-2.0	—	2.0	%	
	Gerr11 (G = 6.667)	-2.0	—	2.0	%	
	Gerr12 (G = 8.000)	-2.0	—	2.0	%	
	Gerr13 (G = 10.000)	-2.0	—	2.0	%	
	Gerr14 (G = 13.333)	-2.0	—	2.0	%	
Slew rate	SR	10	—	—	V/µs	
Operation stabilization time	t_{start}	—	—	5	µs	

Note 1. Calculate with the following formula. (n = 0 to 14)
PGAOUTn = AINn × G
Actual output range includes gain error.
PGAOUTn = (AINn × G) × (Gerr + 100%)

Table 2.46 PGA characteristics in Pseudo-differential input mode (1 of 2)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Offset error	Voff	-20	—	20	mV	
PGAVSS input voltage range	PGAVSS	-0.5	—	0.3	V	

Table 2.46 PGA characteristics in Pseudo-differential input mode (2 of 2)

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Differential input voltage range	G = 1.500	AIN-PGAVSS	-0.5	—	0.5	V	
	G = 2.333		-0.4	—	0.4	V	
	G = 4.000		-0.2	—	0.2	V	
	G = 5.667		-0.15	—	0.15	V	
Output voltage range*1	G = 1.500	V_{OR}	0.600	—	2.550	V	
	G = 2.333		0.417	—	2.733	V	
	G = 4.000		0.550	—	2.600	V	
	G = 5.667		0.500	—	2.650	V	
Gain error	G = 1.500	Gerr	-1.0	—	1.0	%	
	G = 2.333		-1.0	—	1.0	%	
	G = 4.000		-1.0	—	1.0	%	
	G = 5.667		-1.0	—	1.0	%	
Slew rate		SR	10	—	—	V/µs	
Operation stabilization time		t_{start}	—	—	5	µs	

Note 1. Calculate with the following formula.
V_{OR} = (AIN - PGAVSS) × G + (0.5 × AVCC0)
Actual output range includes gain error.
V_{OR} = (AIN - PGAVSS) × G × (Gerr + 100%) + (0.5 × AVCC0)

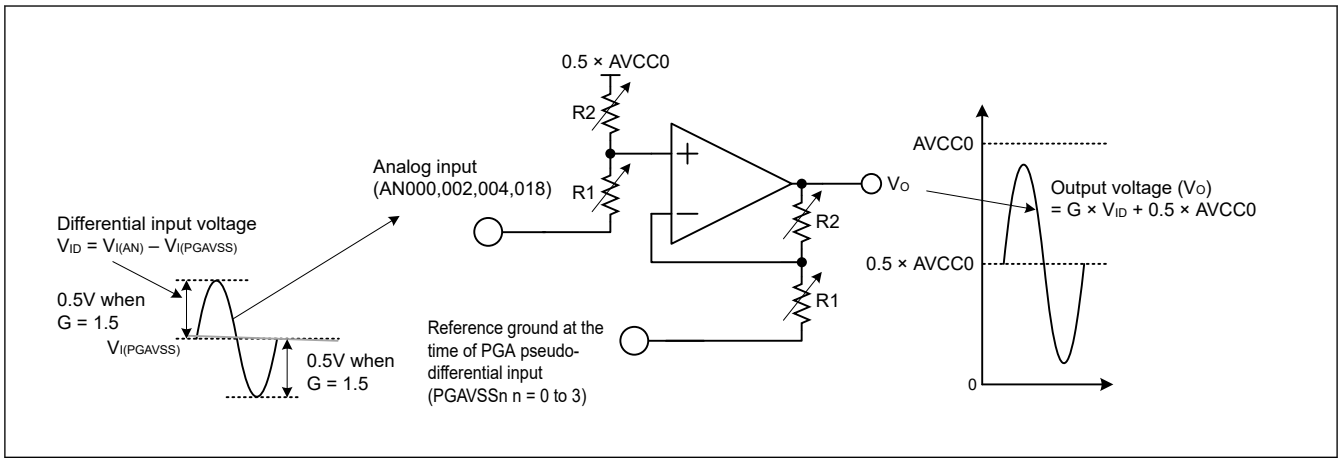


Figure 2.53 Input and Output Signal Levels with the PGA's Pseudo-Differential Setting

2.9 OSC Stop Detect Characteristics

Table 2.47 Oscillation stop detection circuit characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Detection time	t_{dr}	—	—	1	ms	Figure 2.54

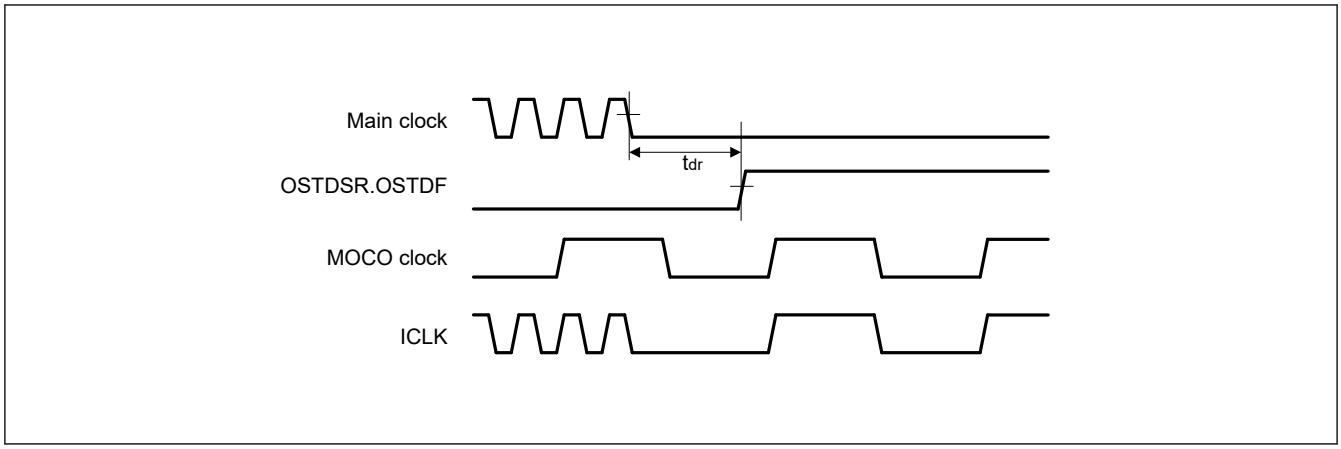


Figure 2.54 Oscillation stop detection timing

2.10 POR and LVD Characteristics

Table 2.48 Power-on reset circuit and voltage detection circuit characteristics (1)

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Voltage detection level	Power-on reset (POR)	DPSBYCR.DEEPCUT[1:0] = 00b or 01b.	V_{POR}	2.5	2.6	2.7	V	Figure 2.55
		DPSBYCR.DEEPCUT[1:0] = 11b.		1.8	2.25	2.7		
	Voltage detection circuit (LVD0)		V_{det0_1}	2.84	2.94	3.04		Figure 2.56
			V_{det0_2}	2.77	2.87	2.97		
			V_{det0_3}	2.70	2.80	2.90		
	Voltage detection circuit (LVD1)		V_{det1_1}	2.89	2.99	3.09		Figure 2.57
			V_{det1_2}	2.82	2.92	3.02		
			V_{det1_3}	2.75	2.85	2.95		
	Voltage detection circuit (LVD2)		V_{det2_1}	2.89	2.99	3.09		Figure 2.58
			V_{det2_2}	2.82	2.92	3.02		
			V_{det2_3}	2.75	2.85	2.95		
Internal reset time	Power-on reset time		t_{POR}	—	4.5	—	ms	Figure 2.55
	LVD0 reset time		t_{LVD0}	—	0.51	—		Figure 2.56
	LVD1 reset time		t_{LVD1}	—	0.38	—		Figure 2.57
	LVD2 reset time		t_{LVD2}	—	0.38	—		Figure 2.58
Minimum VCC down time*1			t_{VOFF}	200	—	—	μs	Figure 2.55, Figure 2.56
Response delay			t_{det}	—	—	200	μs	Figure 2.56 to Figure 2.58
LVD operation stabilization time (after LVD is enabled)			$t_{d(E-A)}$	—	—	10	μs	Figure 2.57, Figure 2.58
Hysteresis width (LVD1 and LVD2)			V_{LVH}	—	70	—	mV	

Note 1. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR}, V_{det0}, V_{det1}, and V_{det2} for POR and LVD.

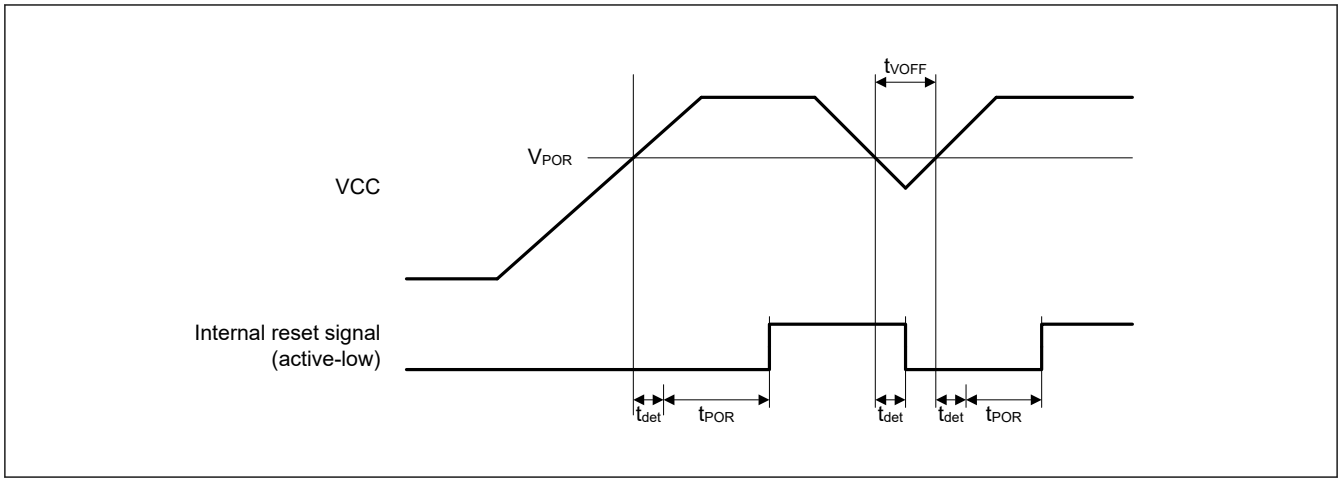


Figure 2.55 Power-on reset timing

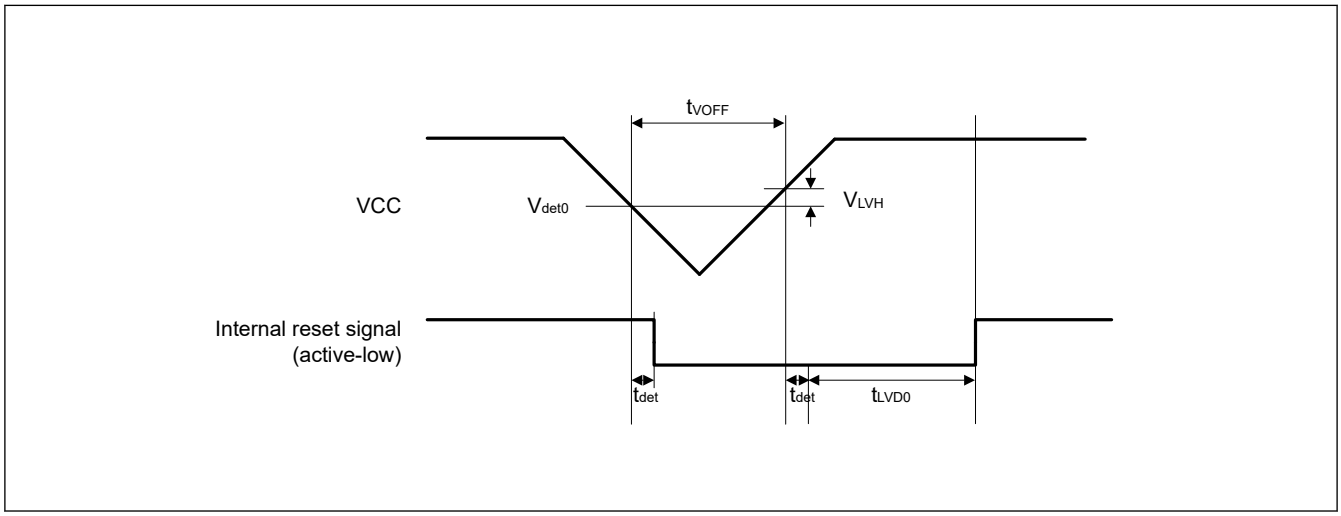


Figure 2.56 Voltage detection circuit timing (V_{det0})

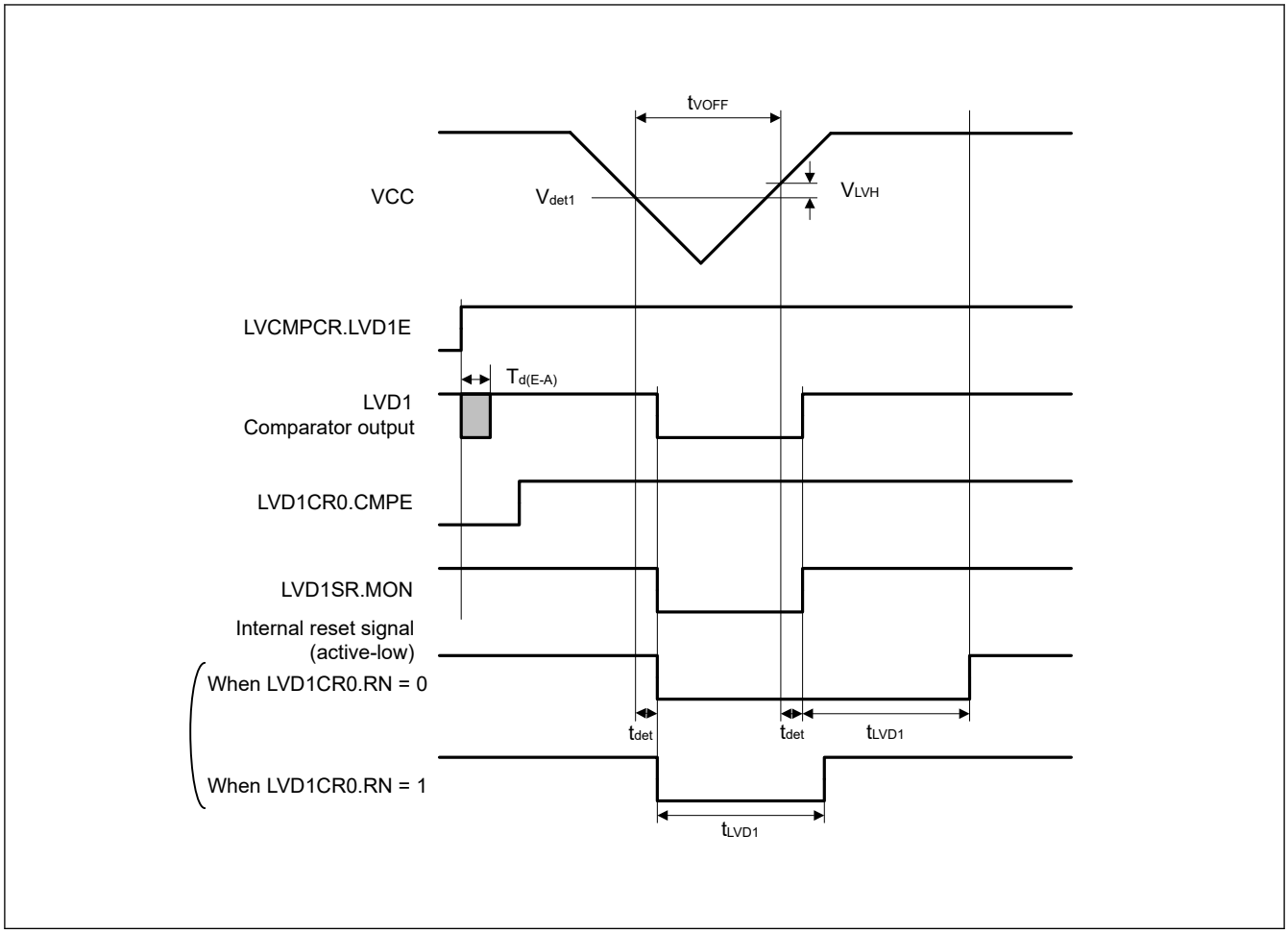


Figure 2.57 Voltage detection circuit timing (V_{det1})

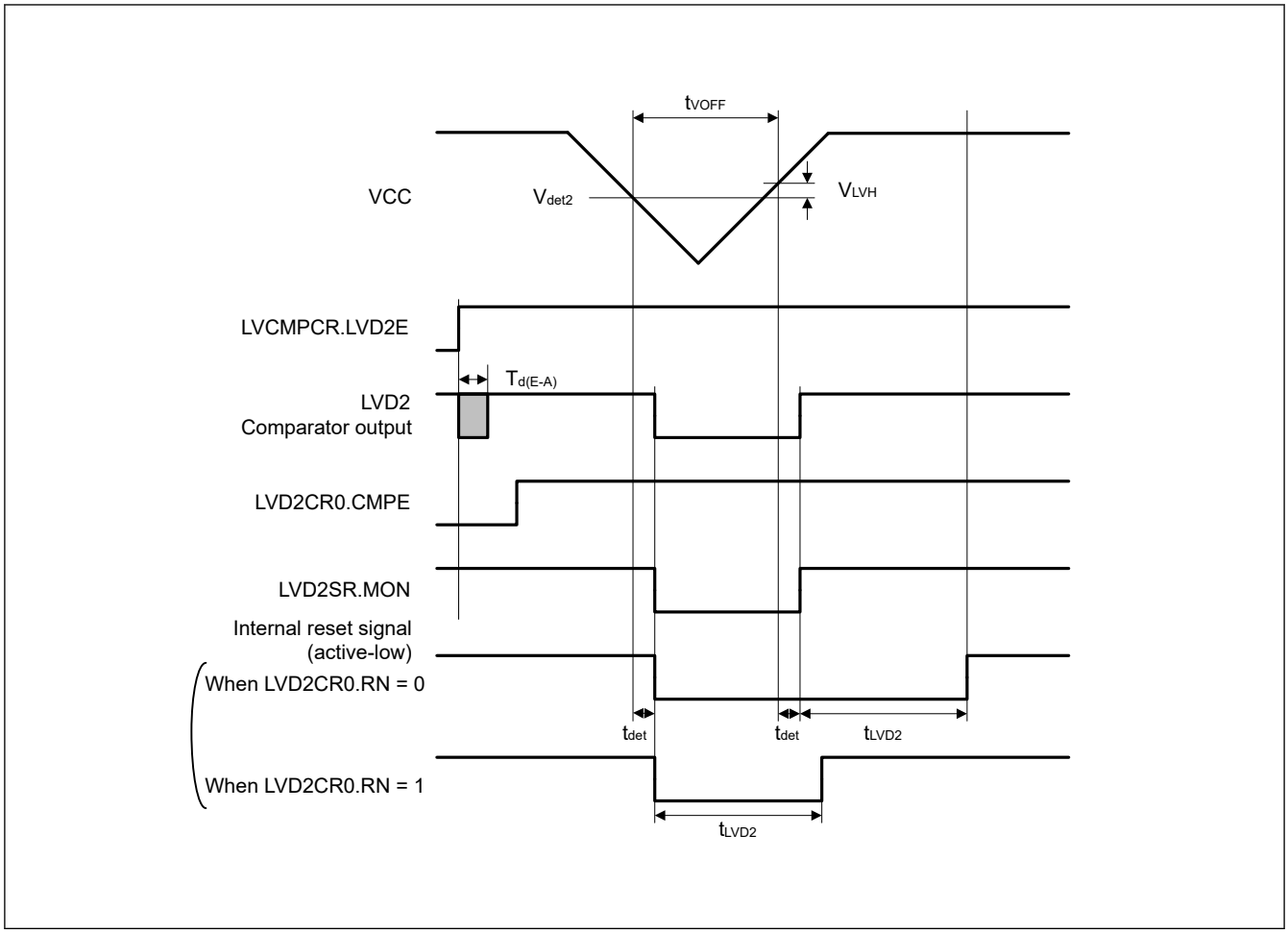


Figure 2.58 Voltage detection circuit timing (V_{det2})

2.11 Flash Memory Characteristics

2.11.1 Code Flash Memory Characteristics

Table 2.49 Code flash memory characteristics (1 of 2)

Conditions: Program or erase: FCLK = 4 to 60 MHz
Read: FCLK ≤ 60 MHz

Parameter		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 60 MHz			Unit	Test conditions
			Min	Typ*6	Max	Min	Typ*6	Max		
Programming time N_{PEC} ≤ 100 times	128-byte	t_{P128}	—	0.75	13.2	—	0.34	6.0	ms	
	8-KB	t_{P8K}	—	49	176	—	22	80	ms	
	32-KB	t_{P32K}	—	194	704	—	88	320	ms	
Programming time N_{PEC} > 100 times	128-byte	t_{P128}	—	0.91	15.8	—	0.41	7.2	ms	
	8-KB	t_{P8K}	—	60	212	—	27	96	ms	
	32-KB	t_{P32K}	—	234	848	—	106	384	ms	
Erasure time N_{PEC} ≤ 100 times	8-KB	t_{E8K}	—	78	216	—	43	120	ms	
	32-KB	t_{E32K}	—	283	864	—	157	480	ms	
Erasure time N_{PEC} > 100 times	8-KB	t_{E8K}	—	94	260	—	52	144	ms	
	32-KB	t_{E32K}	—	341	1040	—	189	576	ms	
Reprogramming/erasure cycle*4		N_{PEC}	10000*1	—	—	10000*1	—	—	Times	

Table 2.49 Code flash memory characteristics (2 of 2)

Conditions: Program or erase: FCLK = 4 to 60 MHz
Read: FCLK ≤ 60 MHz

Parameter	Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 60 MHz			Unit	Test conditions
		Min	Typ*6	Max	Min	Typ*6	Max		
Suspend delay during programming	t_{SPD}	—	—	264	—	—	120	µs	
Programming resume time	t_{PRT}	—	—	110	—	—	50	µs	
First suspend delay during erasure in suspend priority mode	t_{SESD1}	—	—	216	—	—	120	µs	
Second suspend delay during erasure in suspend priority mode	t_{SESD2}	—	—	1.7	—	—	1.7	ms	
Suspend delay during erasure in erasure priority mode	t_{SEED}	—	—	1.7	—	—	1.7	ms	
First erasing resume time during erasure in suspend priority mode*5	t_{REST1}	—	—	1.7	—	—	1.7	ms	
Second erasing resume time during erasure in suspend priority mode	t_{REST2}	—	—	144	—	—	80	µs	
Erasing resume time during erasure in erasure priority mode	t_{REET}	—	—	144	—	—	80	µs	
Forced stop command	t_{FD}	—	—	32	—	—	20	µs	
Data hold time*2	t_{DRP}	10*2 *3	—	—	10*2 *3	—	—	Years	
		30*2 *3	—	—	30*2 *3	—	—		Ta = +85°C

Note 1. This is the minimum number of times to guarantee all the characteristics after reprogramming. The guaranteed range is from 1 to the minimum value.
Note 2. This indicates the minimum value of the characteristic when reprogramming is performed within the specified range.
Note 3. This result is obtained from reliability testing.
Note 4. The reprogram/erase cycle is the number of erasures for each block. When the reprogram/erase cycle is n times (n = 10,000), erasing can be performed n times for each block. For example, when 128-byte programming is performed 64 times for different addresses in 8-KB blocks, and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address several times as one erasure is not enabled. Overwriting is prohibited.
Note 5. Time for resumption includes time for reapplying the erasing pulse (up to one full pulse) that was cut off at the time of suspension.
Note 6. The reference value at VCC = 3.3V and room temperature.

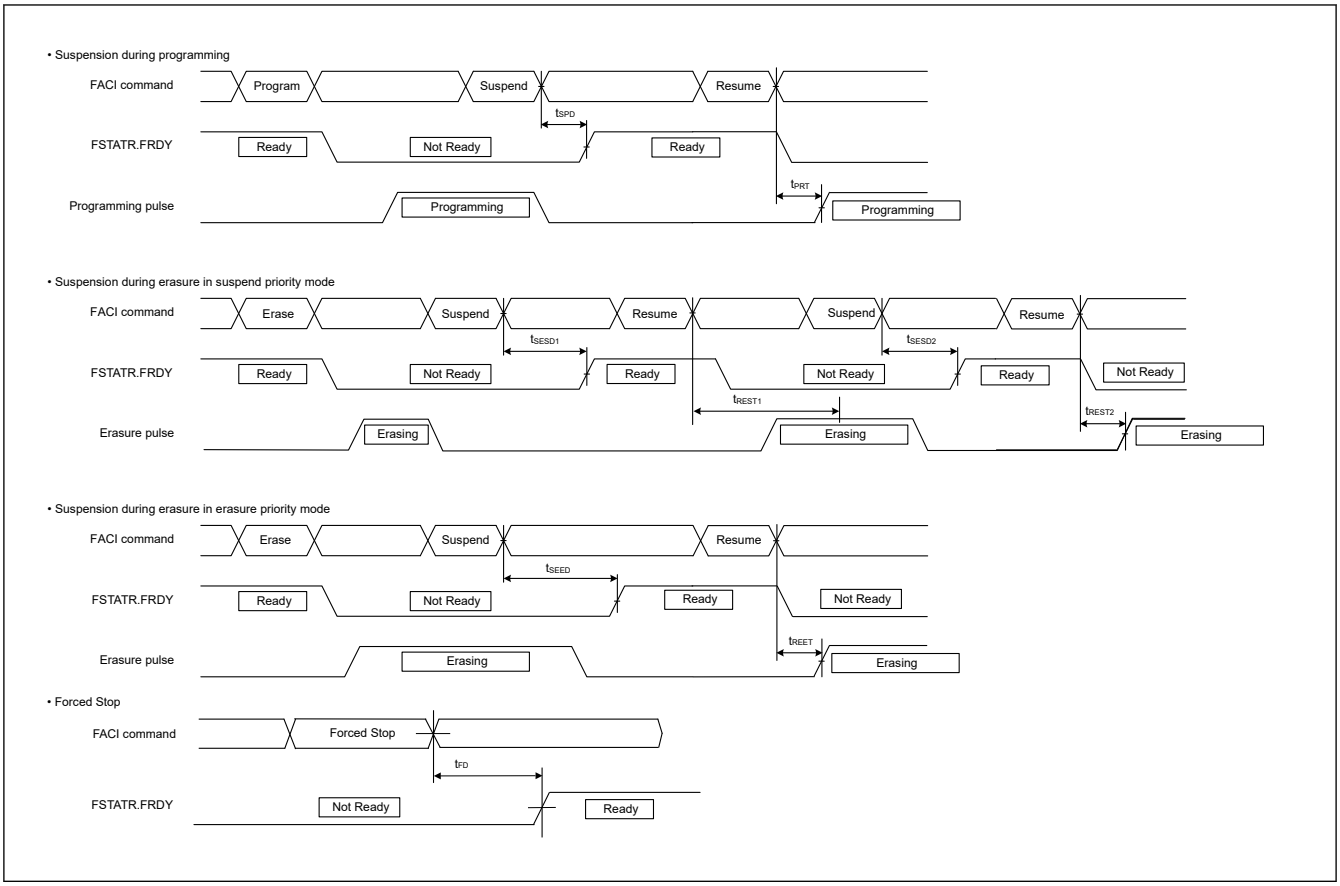


Figure 2.59 Suspension and forced stop timing for flash memory programming and erasure

2.11.2 Data Flash Memory Characteristics

Table 2.50 Data flash memory characteristics (1 of 2)

Conditions: Program or erase: FCLK = 4 to 60 MHz
Read: FCLK ≤ 60 MHz

Parameter		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 60 MHz			Unit	Test conditions
			Min	Typ*6	Max	Min	Typ*6	Max		
Programming time	4-byte	t_{DP4}	—	0.36	3.8	—	0.16	1.7	ms	
	8-byte	t_{DP8}	—	0.38	4.0	—	0.17	1.8		
	16-byte	t_{DP16}	—	0.42	4.5	—	0.19	2.0		
Erasure time	64-byte	t_{DE64}	—	3.1	18	—	1.7	10	ms	
	128-byte	t_{DE128}	—	4.7	27	—	2.6	15		
	256-byte	t_{DE256}	—	8.9	50	—	4.9	28		
Blank check time	4-byte	t_{DBC4}	—	—	84	—	—	30	µs	
Reprogramming/erasure cycle*1		N_{DPEC}	125000*2	—	—	125000*2	—	—	—	
Suspend delay during programming	4-byte	t_{DSPD}	—	—	264	—	—	120	µs	
	8-byte		—	—	264	—	—	120		
	16-byte		—	—	264	—	—	120		
Programming resume time		t_{DPRT}	—	—	110	—	—	50	µs	
First suspend delay during erasure in suspend priority mode	64-byte	t_{DSESD1}	—	—	216	—	—	120	µs	
	128-byte		—	—	216	—	—	120		
	256-byte		—	—	216	—	—	120		

Table 2.50 Data flash memory characteristics (2 of 2)

Conditions: Program or erase: FCLK = 4 to 60 MHz
Read: FCLK ≤ 60 MHz

Parameter		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 60 MHz			Unit	Test conditions
			Min	Typ*6	Max	Min	Typ*6	Max		
Second suspend delay during erasure in suspend priority mode	64-byte	t_{DSESD2}	—	—	300	—	—	300	μs	
	128-byte		—	—	390	—	—	390		
	256-byte		—	—	570	—	—	570		
Suspend delay during erasing in erasure priority mode	64-byte	t_{DSEED}	—	—	300	—	—	300	μs	
	128-byte		—	—	390	—	—	390		
	256-byte		—	—	570	—	—	570		
First erasing resume time during erasure in suspend priority mode*5		t_{DREST1}	—	—	300	—	—	300	μs	
Second erasing resume time during erasure in suspend priority mode		t_{DREST2}	—	—	126	—	—	70	μs	
Erasing resume time during erasure in erasure priority mode		t_{DREET}	—	—	126	—	—	70	μs	
Forced stop command		t_{FD}	—	—	32	—	—	20	μs	
Data hold time*3		t_{DRP}	10*3 *4	—	—	10*3 *4	—	—	Year	
			30*3 *4	—	—	30*3 *4	—	—		Ta = +85°C

Note 1. The reprogram/erase cycle is the number of erasures for each block. When the reprogram/erase cycle is n times (n = 125,000), erasing can be performed n times for each block. For example, when 4-byte programming is performed 16 times for different addresses in 64-byte blocks, and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address several times as one erasure is not enabled. Overwriting is prohibited.
Note 2. This is the minimum number of times to guarantee all the characteristics after reprogramming. The guaranteed range is from 1 to the minimum value.
Note 3. This indicates the minimum value of the characteristic when reprogramming is performed within the specified range.
Note 4. This result is obtained from reliability testing.
Note 5. Time for resumption includes time for reapplying the erasing pulse (up to one full pulse) that was cut off at the time of suspension.
Note 6. The reference value at VCC = 3.3 V and room temperature.

2.11.3 Option Setting Memory Characteristics

Table 2.51 Option setting memory characteristics

Conditions: Program: FCLK = 4 to 60 MHz
Read: FCLK ≤ 60 MHz

Parameter	Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 60 MHz			Unit	Test conditions
		Min	Typ*4	Max	Min	Typ*4	Max		
Programming time N_{OPC} ≤ 100 times	t_{OP}	—	83	309	—	45	162	ms	
Programming time N_{OPC} > 100 times	t_{OP}	—	100	371	—	55	195	ms	
Reprogramming cycle	N_{OPC}	20000*1	—	—	20000*1	—	—	Times	
Data hold time*2	t_{DRP}	10*2 *3	—	—	10*2 *3	—	—	Years	
		30*2 *3	—	—	30*2 *3	—	—		Ta = +85°C

Note 1. This is the minimum number of times to guarantee all the characteristics after reprogramming. The guaranteed range is from 1 to the minimum value.
Note 2. This indicates the minimum value of the characteristic when reprogramming is performed within the specified range.
Note 3. This result is obtained from reliability testing.
Note 4. The reference value at VCC = 3.3 V and room temperature.

2.12 Boundary Scan

Table 2.52 Boundary scan characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
TCK clock cycle time	t_{TCKcyc}	100	—	—	ns	Figure 2.60
TCK clock high pulse width	t_{TCKH}	45	—	—	ns	
TCK clock low pulse width	t_{TCKL}	45	—	—	ns	
TCK clock rise time	t_{TCKr}	—	—	5	ns	
TCK clock fall time	t_{TCKf}	—	—	5	ns	
TMS setup time	t_{TMSS}	20	—	—	ns	Figure 2.61
TMS hold time	t_{TMSH}	20	—	—	ns	
TDI setup time	t_{TDIS}	20	—	—	ns	
TDI hold time	t_{TDIH}	20	—	—	ns	
TDO data delay	t_{TDOD}	—	—	40	ns	
Boundary scan circuit startup time*1	T_{BSSTUP}	t_{RESWP}	—	—	—	Figure 2.62

Note 1. Boundary scan does not function until the power-on reset becomes negative.

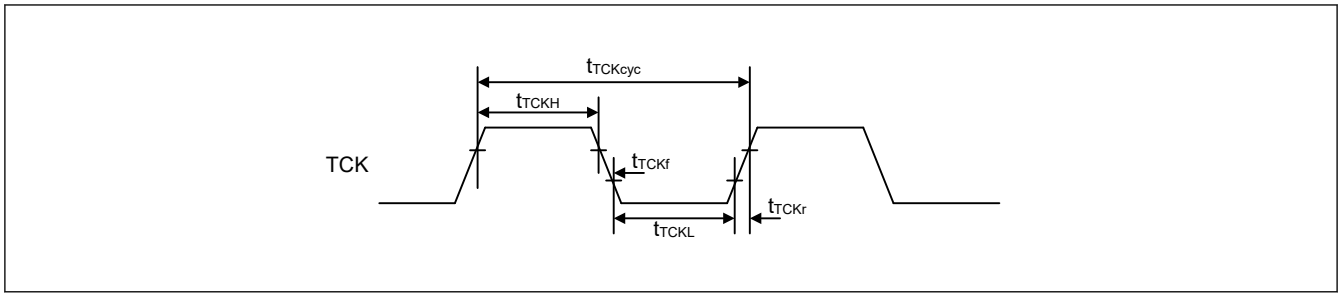


Figure 2.60 Boundary scan TCK timing

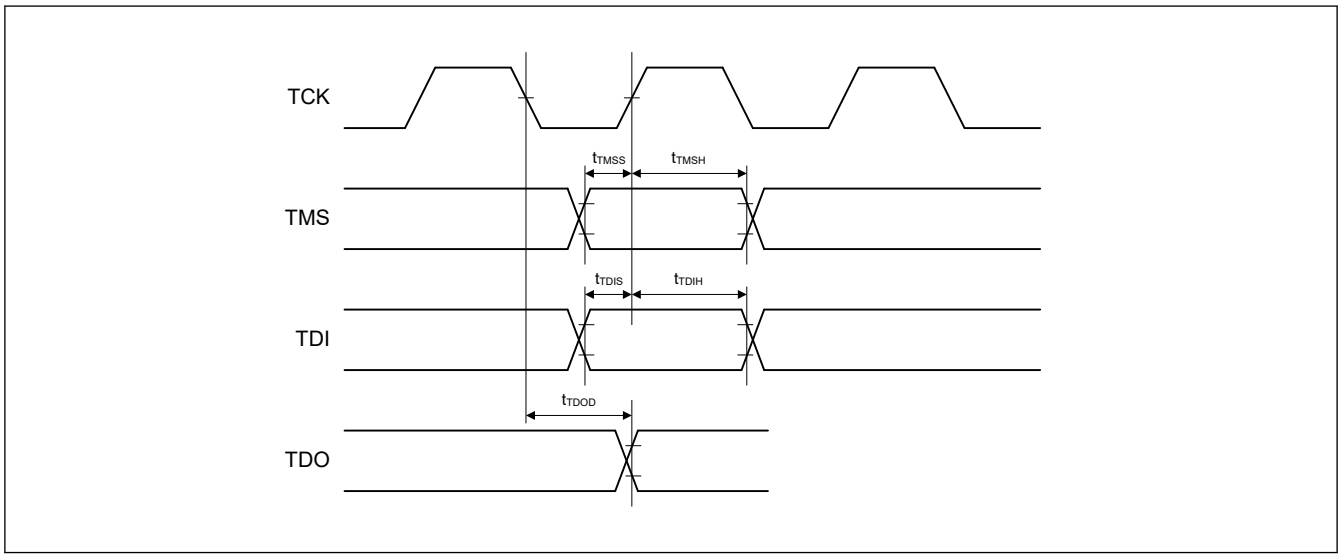


Figure 2.61 Boundary scan input/output timing

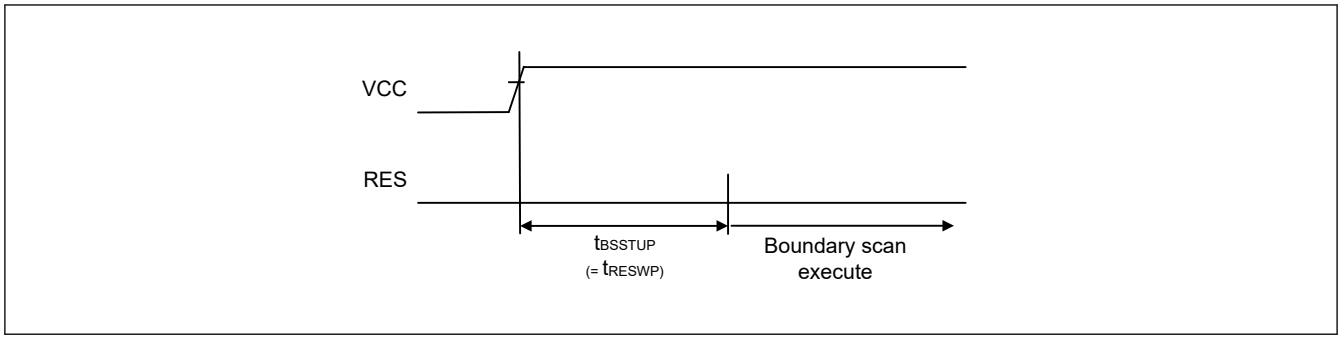


Figure 2.62 Boundary scan circuit startup timing

2.13 Joint Test Action Group (JTAG)

Table 2.53 JTAG

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
TCK clock cycle time	t_{TCKcyc}	40	—	—	ns	Figure 2.63
TCK clock high pulse width	t_{TCKH}	15	—	—	ns	
TCK clock low pulse width	t_{TCKL}	15	—	—	ns	
TCK clock rise time	t_{TCKr}	—	—	5	ns	
TCK clock fall time	t_{TCKf}	—	—	5	ns	
TMS setup time	t_{TMSS}	8	—	—	ns	Figure 2.64
TMS hold time	t_{TMSH}	8	—	—	ns	
TDI setup time	t_{TDIS}	8	—	—	ns	
TDI hold time	t_{TDIH}	8	—	—	ns	
TDO data delay time	t_{TDOD}	—	—	20	ns	

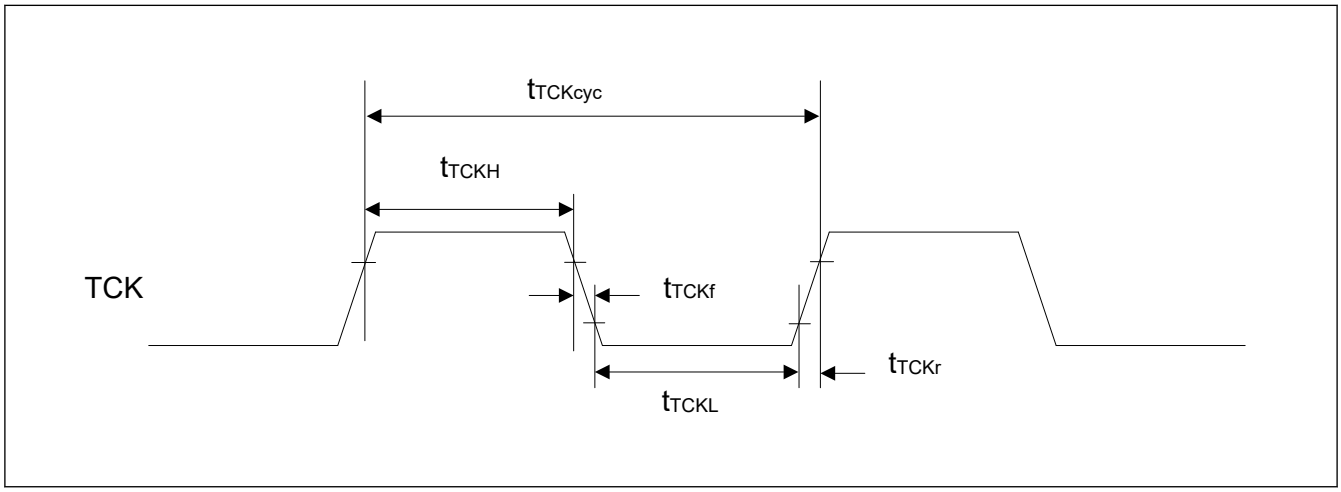


Figure 2.63 JTAG TCK timing

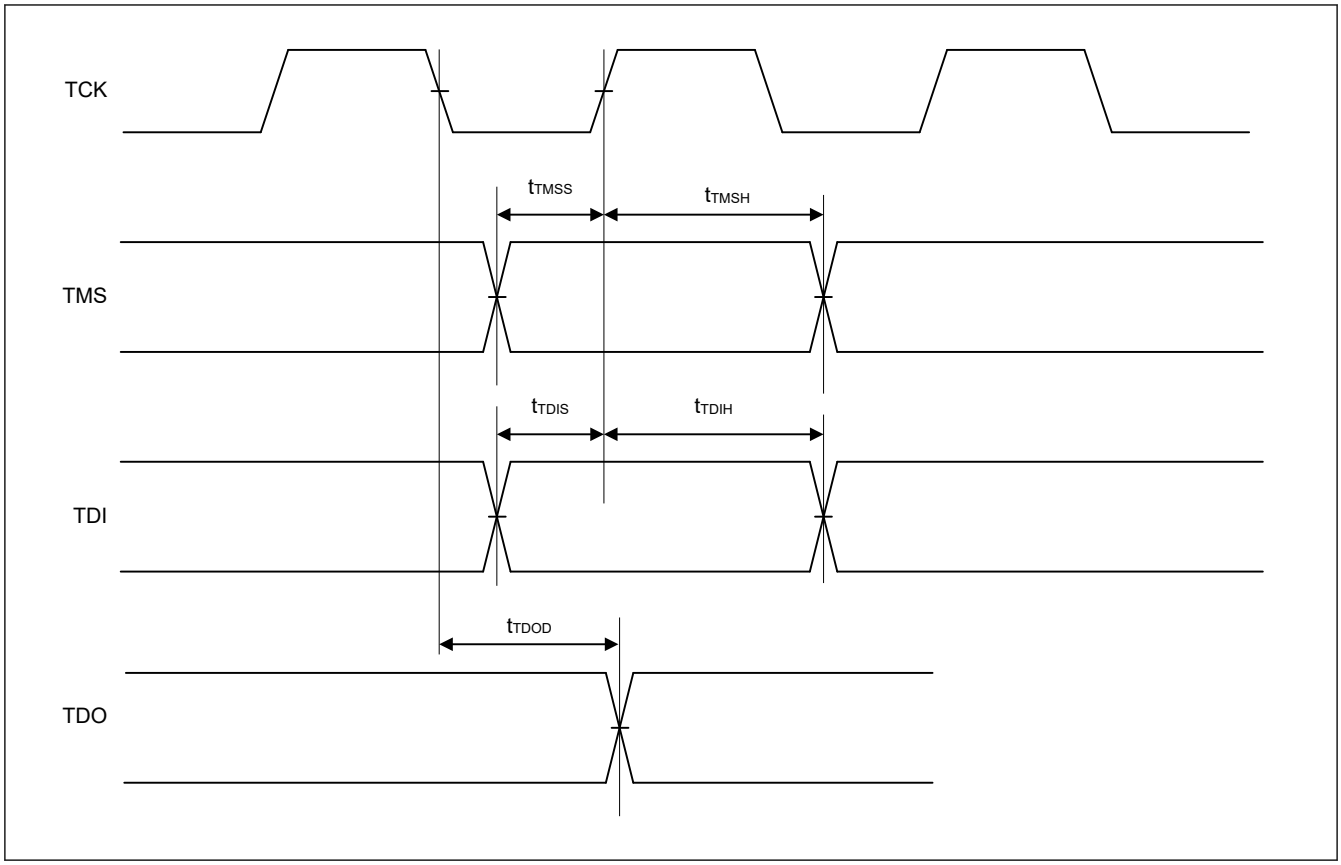


Figure 2.64 JTAG input/output timing

2.14 Serial Wire Debug (SWD)

Table 2.54 SWD

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
SWCLK clock cycle time	$t_{SWCKcyc}$	40	—	—	ns	Figure 2.65
SWCLK clock high pulse width	t_{SWCKH}	15	—	—	ns	
SWCLK clock low pulse width	t_{SWCKL}	15	—	—	ns	
SWCLK clock rise time	t_{SWCKr}	—	—	5	ns	
SWCLK clock fall time	t_{SWCKf}	—	—	5	ns	
SWDIO setup time	t_{SWDS}	8	—	—	ns	Figure 2.66
SWDIO hold time	t_{SWDH}	8	—	—	ns	
SWDIO data delay time	t_{SWDD}	2	—	28	ns	

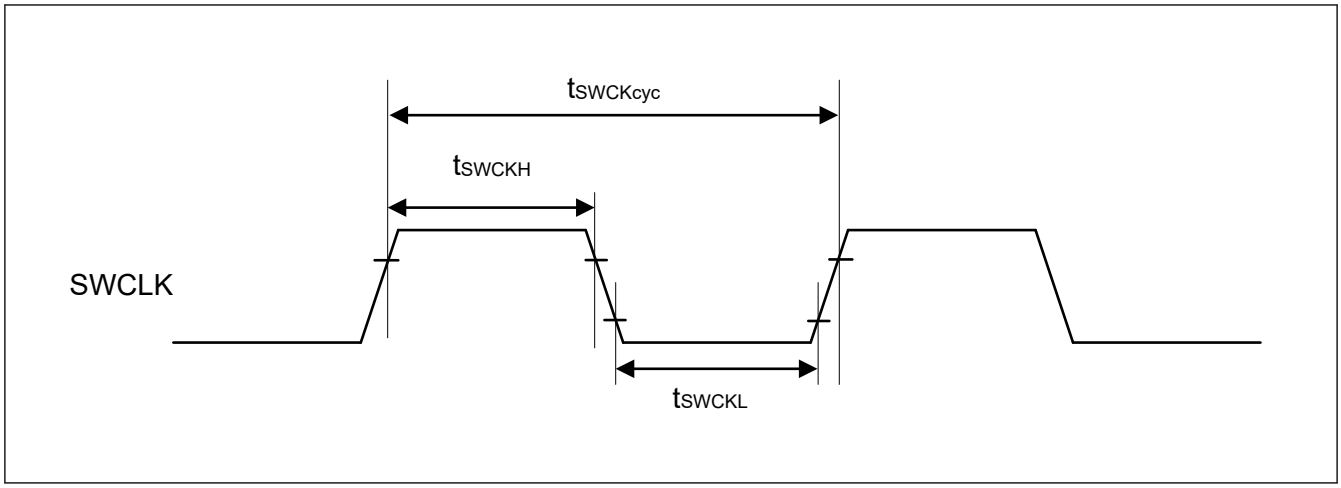


Figure 2.65 SWD SWCLK timing

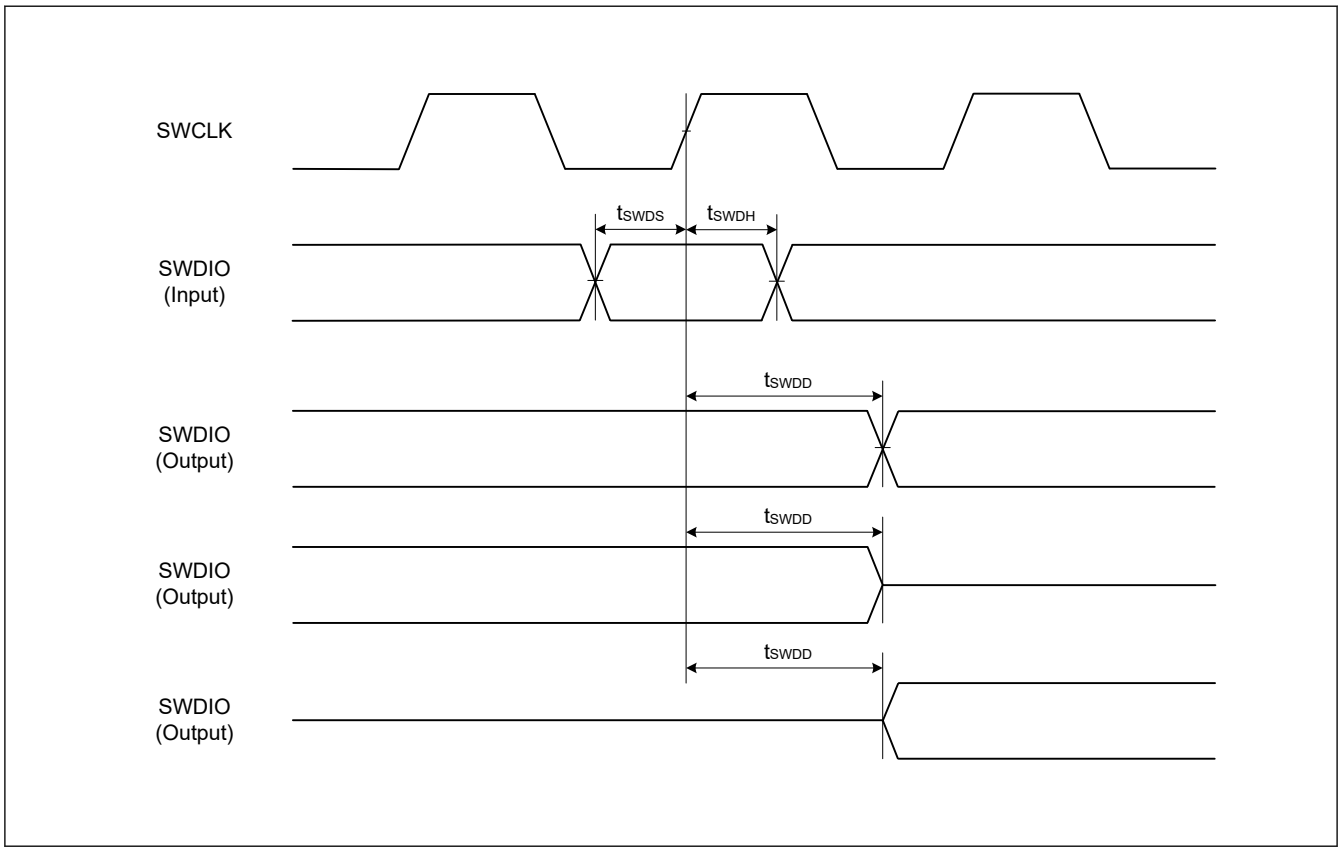


Figure 2.66 SWD input/output timing

2.15 Embedded Trace Macro Interface (ETM)

Table 2.55 ETM (1 of 2)

Conditions: High speed high drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
TCLK clock cycle time	$t_{TCLKcyc}$	16.7	—	—	ns	Figure 2.67
TCLK clock high pulse width	t_{TCLKH}	7.35	—	—	ns	
TCLK clock low pulse width	t_{TCLKL}	7.35	—	—	ns	
TCLK clock rise time	t_{TCLKr}	—	—	1	ns	
TCLK clock fall time	t_{TCLKf}	—	—	1	ns	

Table 2.55 ETM (2 of 2)

Conditions: High speed high drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
TDATA[3:0] output setup time	t_{TRDS}	2.5	—	—	ns	Figure 2.68
TDATA[3:0] output hold time	t_{TRDH}	1.5	—	—	ns	

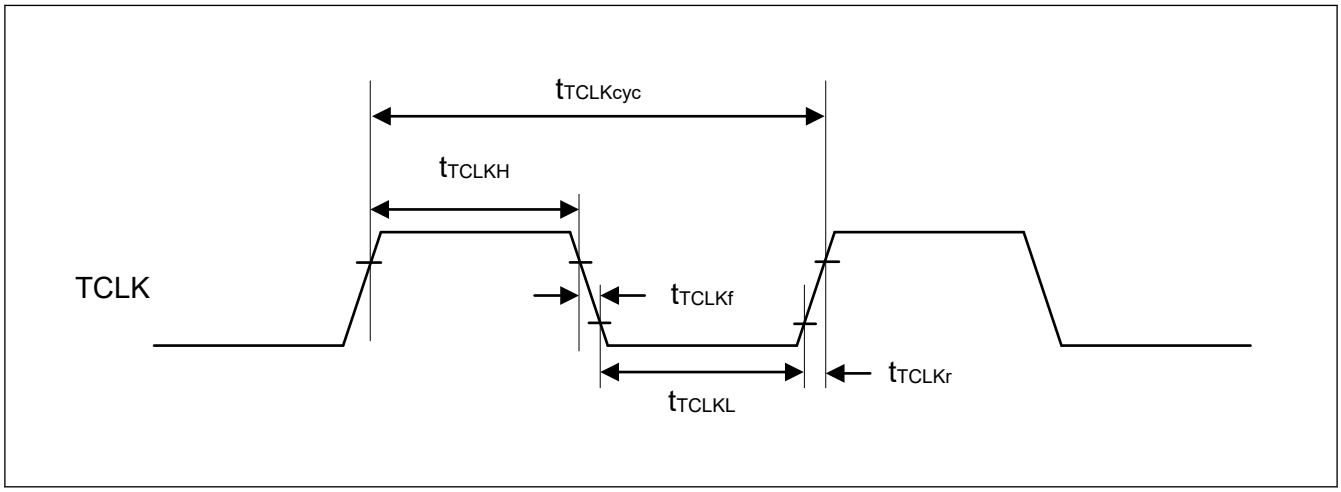


Figure 2.67 ETM TCLK timing

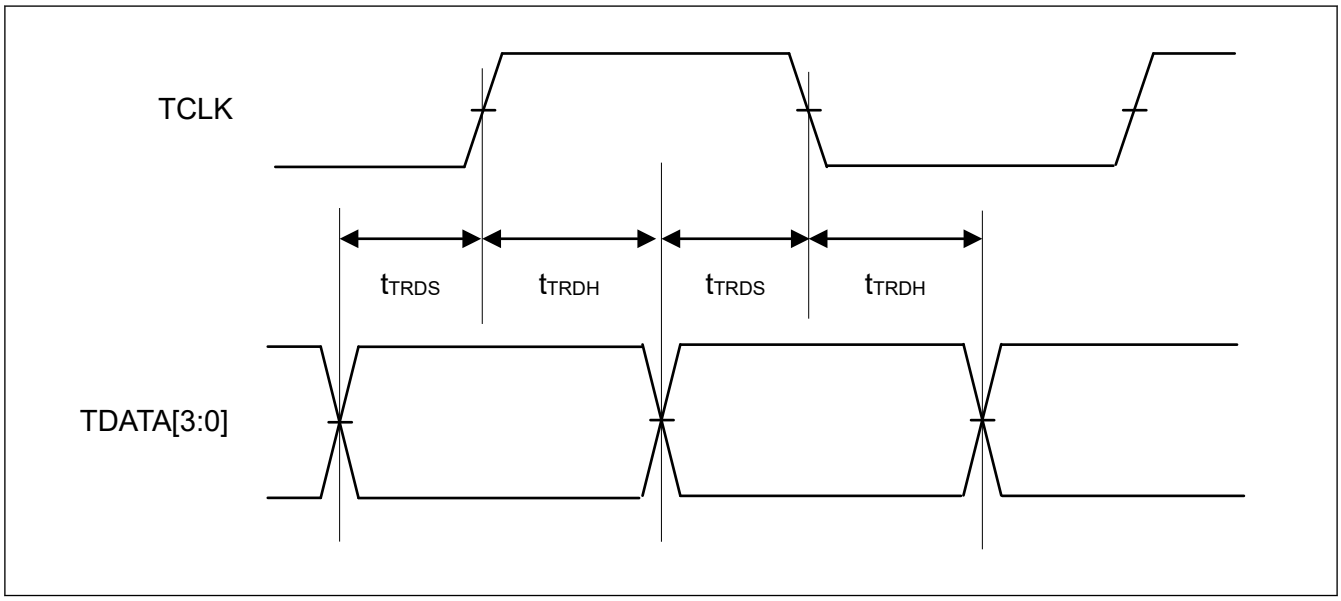


Figure 2.68 ETM output timing

Appendix 1. Port States in Each Processing Mode

Function	Pin function	Reset	Software Standby mode	Deep Software Standby mode	After Deep Software Standby mode is canceled (return to startup mode)	
					IOKEEP = 0	IOKEEP = 1*1
Mode	MD	Pull-up	Keep-O	Keep	Hi-Z	Keep
JTAG	TCK/TMS/TDI	Pull-up	Keep-O	Keep	Hi-Z	Keep
	TDO	TDO output	Keep-O	Keep	TDO output	Keep
Trace	TCLK/TDATAx	Hi-Z	Keep-O	Keep	Hi-Z	Keep
IRQ	IRQx	Hi-Z	Keep-O*2	Keep	Hi-Z	Keep
	IRQx-DS	Hi-Z	Keep-O*2	Keep*3	Hi-Z	Keep
KINT	KRxx	Hi-Z	Keep-O*2	Keep	Hi-Z	Keep
AGT	AGTIOn	Hi-Z	Keep-O*2	Keep	Hi-Z	Keep
IIC	SCLn/SDAn	Hi-Z	Keep-O*2	Keep	Hi-Z	Keep
CLKOUT	CLKOUT	Hi-Z	[CLKOUT selected] CLKOUT output	Keep	Hi-Z	Keep
ACMPHS	VCOUT, CMPOUTm, CMPOUT012	Hi-Z	Hi-Z (Keep-O)	Hi-Z (Keep-O)	Hi-Z	Keep
	IVREFn	Hi-Z	Hi-Z (Keep-O)	Hi-Z (Keep-O)	Hi-Z	Hi-Z
	IVCMPmn	Hi-Z	Hi-Z (Keep-O)	Hi-Z (Keep-O)	Hi-Z	Hi-Z
DAC12	DAn	Hi-Z	[DAn output (DAOE = 1)] D/A output retained	Keep	Hi-Z	Keep
ADC	ANxxx	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
	PGAINn	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
	PGAVSSn	Pull-up*4	Pull-up*5 / Keep	Pull-up*5 / Keep	Pull-up*5 / Keep	Pull-up*5 / Keep
	PGAOUTn	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Others	—	Hi-Z	Keep-O	Keep	Hi-Z	Keep

Note: H: High-level
L: Low-level
Hi-Z: High-impedance
Keep-O: Output pins retain their previous values. Input pins go to high-impedance.
Keep: Pin states are retained during periods in Software Standby mode.

Note 1. Retains the I/O port state until the DPSBYCR.IOKEEP bit is cleared to 0.

Note 2. Input is enabled if the pin is specified as the Software Standby canceling source while it is used as an external interrupt pin.

Note 3. Input is enabled if the pin is specified as the Deep Software Standby canceling source.

Note 4. The built-in pull-up is turned on to protect the circuit from negative potential inputs.

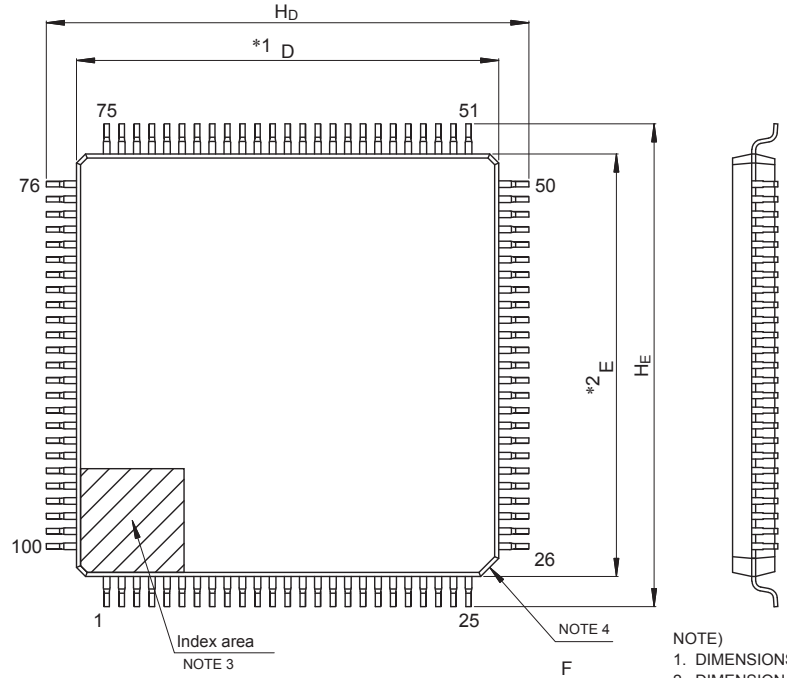
Note 5. Regardless of whether the PGA is enabled or disabled, when the PGA is set to pseudo-differential mode, the built in pull-up is turned on to protect the circuit from negative potential inputs. To turn off the built-in pull-up, turn off the PGA's pseudo-differential mode and set it to single mode.

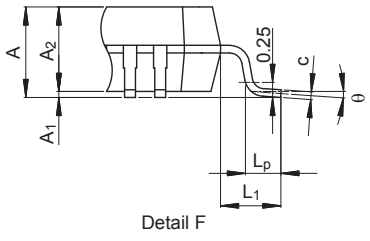
Appendix 2. Package Dimensions

Information on the latest version of the package dimensions or mountings is displayed in Packages on the Renesas Electronics Corporation website.

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP100-14x14-0.50	PLQP0100KB-B	—	0.6

Unit: mm





NOTE)
1. DIMENSIONS “*1” AND “*2” DO NOT INCLUDE MOLD FLASH.
2. DIMENSION “*3” DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

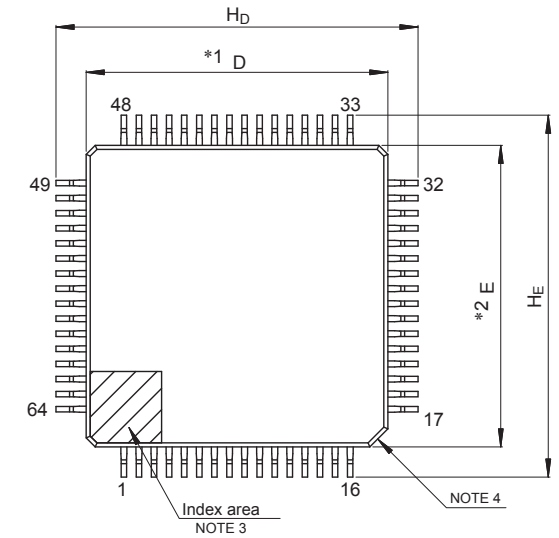
Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

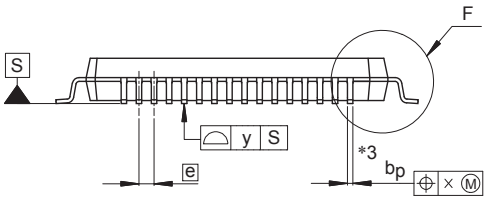
© 2015 Renesas Electronics Corporation. All rights reserved.

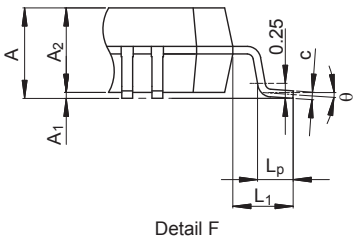
Figure A2.1 LQFP 100-pin

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP64-10x10-0.50	PLQP0064KB-C	—	0.3

Unit: mm







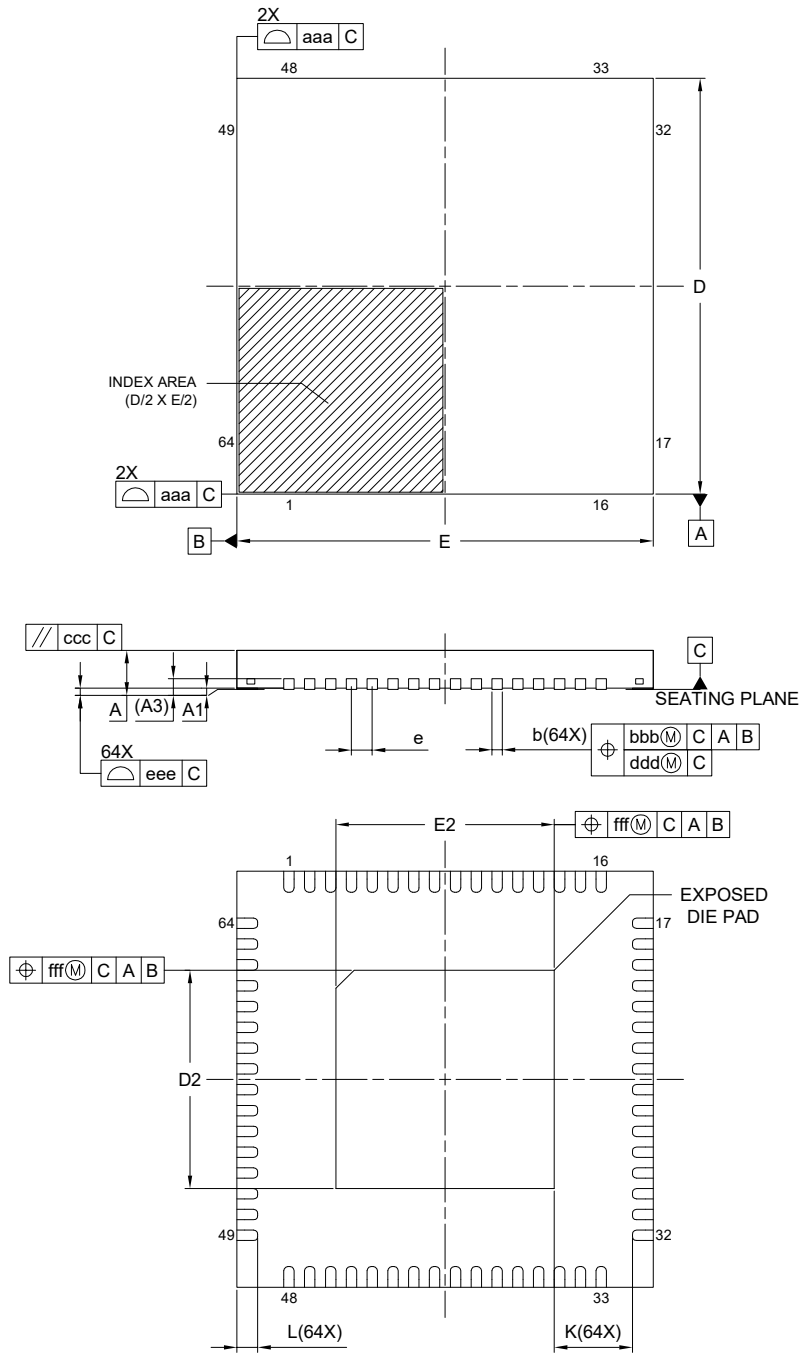
NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A_2	—	1.4	—
H_D	11.8	12.0	12.2
H_E	11.8	12.0	12.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

© 2015 Renesas Electronics Corporation. All rights reserved.

Figure A2.2 LQFP 64-pin

JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-HWQFN064-8x8-0.40	PWQN0064LB-A	0.18

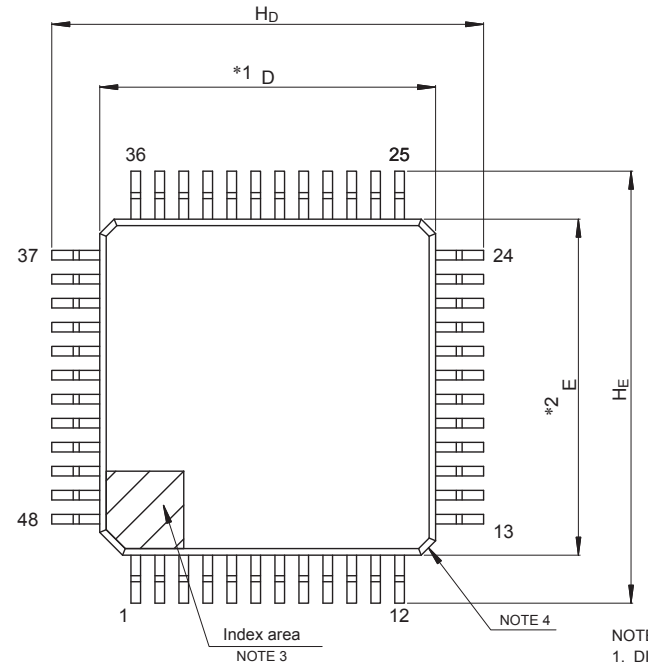


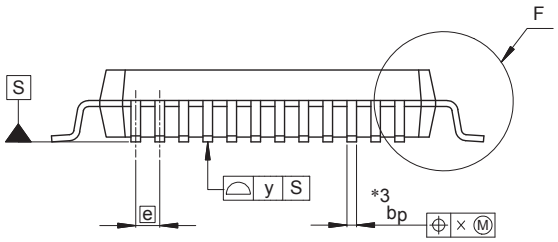
Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	—	—	0.80
A_1	0.00	0.02	0.05
A_3		0.203 REF.	
b	0.15	0.20	0.25
D		8.00 BSC	
E		8.00 BSC	
e		0.40 BSC	
L	0.35	0.40	0.45
K	0.20	—	—
D_2	4.15	4.20	4.25
E_2	4.15	4.20	4.25
aaa		0.10	
bbb		0.07	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

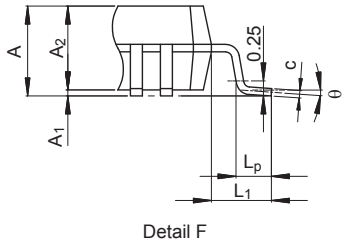
Figure A2.3 QFN 64-pin

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP48-7x7-0.50	PLQP0048KB-B	—	0.2

Unit: mm







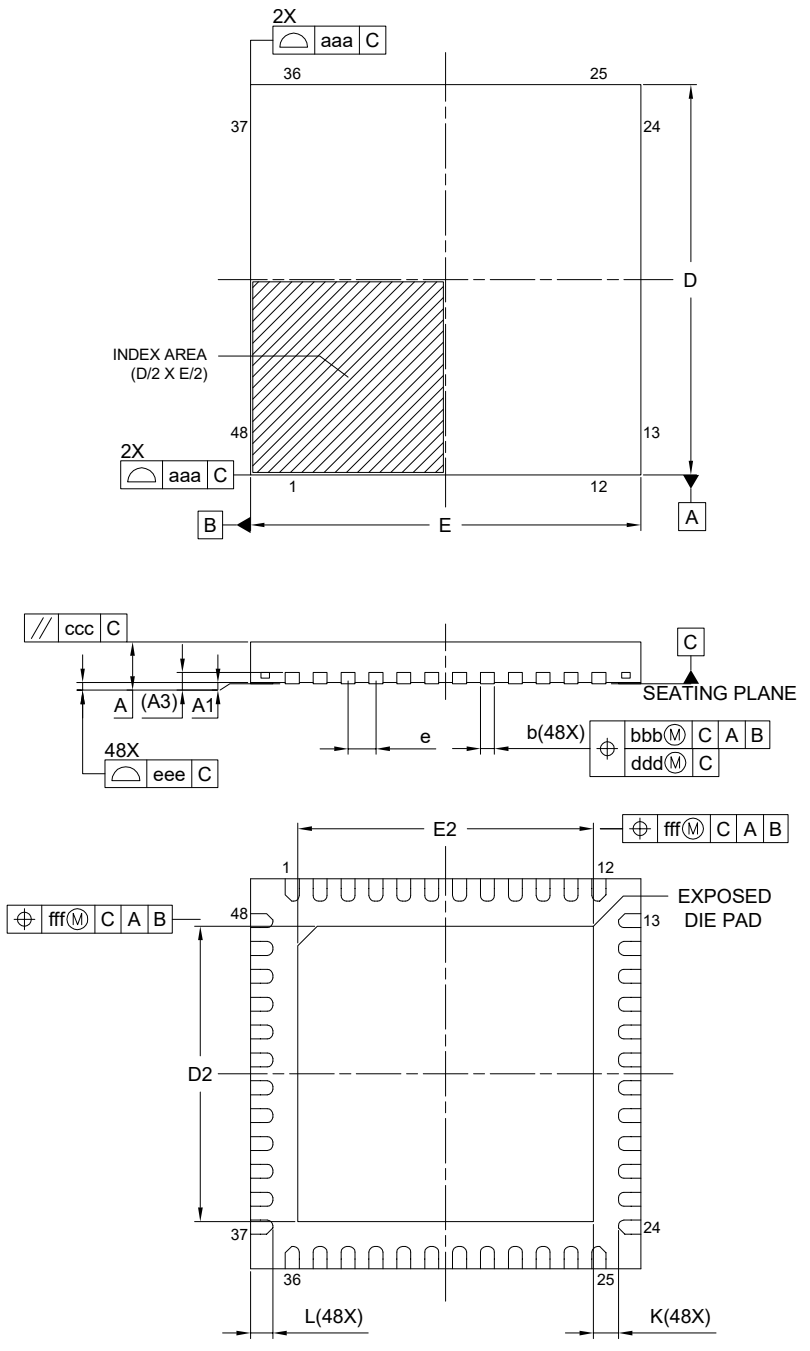
Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	6.9	7.0	7.1
E	6.9	7.0	7.1
A_2	—	1.4	—
H_D	8.8	9.0	9.2
H_E	8.8	9.0	9.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.17	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

Figure A2.4 LQFP 48-pin

JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-HWQFN048-7x7-0.50	PWQN0048KC-A	0.13 g



Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	—	—	0.80
A_1	0.00	0.02	0.05
A_3		0.203 REF.	
b	0.20	0.25	0.30
D		7.00 BSC	
E		7.00 BSC	
e		0.50 BSC	
L	0.30	0.40	0.50
K	0.20	—	—
D_2	5.25	5.30	5.35
E_2	5.25	5.30	5.35
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

Figure A2.5 QFN 48-pin

Appendix 3. I/O Registers

This appendix describes I/O register address and access cycles by function.

3.1 Peripheral Base Addresses

This section provides the base addresses for peripherals described in this manual. Table A3.1 shows the name, description, and the base address of each peripheral.

Table A3.1 Peripheral base address (1 of 3)

Name	Description	Base address
RMPU	Renesas Memory Protection Unit	0x4000_0000
TZF	TrustZone Filter	0x4000_0E00
SRAM	SRAM Control	0x4000_2000
BUS	BUS Control	0x4000_3000
DMAC0	Direct memory access controller 0	0x4000_5000
DMAC1	Direct memory access controller 1	0x4000_5040
DMAC2	Direct memory access controller 2	0x4000_5080
DMAC3	Direct memory access controller 3	0x4000_50C0
DMAC4	Direct memory access controller 4	0x4000_5100
DMAC5	Direct memory access controller 5	0x4000_5140
DMAC6	Direct memory access controller 6	0x4000_5180
DMAC7	Direct memory access controller 7	0x4000_51C0
DMA	DMAC Module Activation	0x4000_5200
DTC	Data Transfer Controller	0x4000_5400
ICU	Interrupt Controller	0x4000_6000
CACHE	CACHE	0x4000_7000
CPSCU	CPU System Security Control Unit	0x4000_8000
DBG	Debug Function	0x4001_B000
FCACHE	Flash Cache	0x4001_C100
SYSC	System Control	0x4001_E000
PORT0	Port 0 Control Registers	0x4001_F000
PORT2	Port 2 Control Registers	0x4001_F040
PORTA	Port A Control Registers	0x4001_F140
PORTB	Port B Control Registers	0x4001_F160
PORTC	Port C Control Registers	0x4001_F180
PORTD	Port D Control Registers	0x4001_F1A0
PORTE	Port E Control Registers	0x4001_F1C0
PFS_B	Pmn Pin Function Control Register	0x4001_F800
IIRFA	IIR Filter Accelerator	0x4002_0000
TFU	Trigonometric Function Unit	0x4002_1000
ELC_B	Event Link Controller	0x4008_2000
IWDT	Independent Watchdog Timer	0x4008_3200
WDT	Watchdog Timer	0x4008_3400
CAC	Clock Frequency Accuracy Measurement Circuit	0x4008_3600
MSTP	Module Stop Control A, B, C, D, E	0x4008_4000

Table A3.1 Peripheral base address (2 of 3)

Name	Description	Base address
KINT	Key Interrupt Function	0x4008_5000
POEG	Port Output Enable for GPT	0x4008_A000
CANFD	CANFD Module Control	0x400B_0000
PSCU	Peripheral Security Control Unit	0x400E_0000
AGTW_B0	Low Power Asynchronous General purpose Timer 0	0x400E_8000
AGTW_B1	Low Power Asynchronous General purpose Timer 1	0x400E_8100
TSN	Temperature Sensor	0x400F_3000
ACMPHS0	High-Speed Analog Comparator	0x400F_4000
ACMPHS1	High-Speed Analog Comparator	0x400F_4100
ACMPHS2	High-Speed Analog Comparator	0x400F_4200
ACMPHS3	High-Speed Analog Comparator	0x400F_4300
CRC	Cyclic Redundancy Check	0x4010_8000
DOC_B	Data Operation Circuit	0x4010_9000
SCI_B0	Serial Communication Interface 0	0x4011_8000
SCI_B1	Serial Communication Interface 1	0x4011_8100
SCI_B2	Serial Communication Interface 2	0x4011_8200
SCI_B3	Serial Communication Interface 3	0x4011_8300
SCI_B4	Serial Communication Interface 4	0x4011_8400
SCI_B9	Serial Communication Interface 9	0x4011_8900
SPI_B0	Serial Peripheral Interface 0	0x4011_A000
SPI_B1	Serial Peripheral Interface 1	0x4011_A100
IIC_B0	Inter-Integrated Circuit 0	0x4011_F000
IIC0WU_B	Inter-Integrated Circuit 0 Wake-up Unit	0x4011_F098
IIC_B1	Inter-Integrated Circuit 1	0x4011_F400
ECCMB	CANFD ECC Module	0x4012_F200
SCE5_B	Secure Cryptographic Engine	0x4016_1000
GPT320	General PWM Timer 0	0x4016_9000
GPT321	General PWM Timer 1	0x4016_9100
GPT322	General PWM Timer 2	0x4016_9200
GPT323	General PWM Timer 3	0x4016_9300
GPT324	General PWM Timer 4	0x4016_9400
GPT325	General PWM Timer 5	0x4016_9500
GPT326	General PWM Timer 6	0x4016_9600
GPT327	General PWM Timer 7	0x4016_9700
GPT328	General PWM Timer 8	0x4016_9800
GPT329	General PWM Timer 9	0x4016_9900
GPT_OPS	Output Phase Switching Controller	0x4016_9A00
GPT_GTCLK	General PWM Timer	0x4016_9B00
PDG	PWM Delay Generation	0x4016_A000
ADC_B	A/D Converter	0x4017_0000
DAC120	12-bit D/A converter	0x4017_2000
DAC121	12-bit D/A converter	0x4017_2100

Table A3.1 Peripheral base address (3 of 3)

Name	Description	Base address
FLAD	Data Flash	0x407F_C000
FACI	Flash Application Command Interface	0x407F_E000

Note: Name = Peripheral name
Description = Peripheral functionality
Base address = Lowest reserved address or address used by the peripheral

3.2 Access Cycles

This section provides access cycle information for the I/O registers described in this manual.

- Registers are grouped by associated module.
- The number of access cycles indicates the number of cycles based on the specified reference clock.
- In the internal I/O area, reserved addresses that are not allocated to registers must not be accessed, otherwise operations cannot be guaranteed.
- The number of I/O access cycles depends on bus cycles of the internal peripheral bus, divided clock synchronization cycles, and wait cycles of each module. Divided clock synchronization cycles differ depending on the frequency ratio between ICLK and PCLK.
- When the frequency of ICLK is equal to that of PCLK, the number of divided clock synchronization cycles is always constant.
- When the frequency of ICLK is greater than that of PCLK, at least 1 PCLK cycle is added to the number of divided clock synchronization cycles.
- The number of write access cycles indicates the number of cycles obtained by non-bufferable write access.

Note: This applies to the number of cycles when access from the CPU does not conflict with bus access from other bus masters such as DTC or DMAC.

Table A3.2 Access cycles (1 of 3)

Peripherals	Address		Number of access cycles					
			ICLK = PCLK		ICLK > PCLK*1		Cycle Unit	Related function
	From	To	Read	Write	Read	Write		
RMPU, TZF, SRAM, BUS, DMACn, DMA, DTC, ICU	0x4000_0000	0x4000_6FFF	4	3	4	3	ICLK	Renesas Memory Protection Unit, TrustZone Filter, SRAM Control, BUS Control, Direct memory access controller n, DMAC Module Activation, DTC Control Register, Interrupt Controller
CACHE	0x4000_7000	0x4000_7FFF	4	5	4	5	ICLK	CACHE
CPSCU, DBG, FCACHE	0x4000_8000	0x4001_CFFF	4	3	4	3	ICLK	CPU System Security Control Unit, Debug Function, Flash Cache
SYSC	0x4001_E000	0x4001_E3FF	5	4	5	4	ICLK	System Control
SYSC	0x4001_E400	0x4001_E5FF	9	8	5 to 8	5 to 8	PCLKB	System Control
PORTn	0x4001_F000	0x4001_F7FF	5	3	5	3	ICLK	PORTn Control Register 1/3/4
PORTn (PCNTR2)	0x4001_F000	0x4001_F7FF	8	3	8	3	ICLK	PORTn Control Register 2
PFS	0x4001_F800	0x4001_FFFF	8	3	8	3	ICLK	Pmn Pin Function Control Register
IIRFA	0x4002_0000	0x4002_03FF	4	3	4	3	ICLK	IIR Filter Accelerator
IIRFA	0x4002_0400	0x4002_0FFF	6	3	6	3	ICLK	IIR Filter Accelerator

Table A3.2 Access cycles (2 of 3)

Peripherals	Address		Number of access cycles				Cycle Unit	Related function
			ICLK = PCLK		ICLK > PCLK*1			
	From	To	Read	Write	Read	Write		
TFU	0x4002_1000	0x4002_1FFF	4	3	4	3	ICLK	Trigonometric Function Unit
ELC	0x4008_2000	0x4008_2FFF	5	4	3 to 5	2 to 4	PCLKB	Event Link Controller
IWDT, WDT, CAC	0x4008_3000	0x4008_3FFF	5	4	3 to 5	2 to 4	PCLKB	Independent Watchdog Timer, Watchdog Timer, Clock Frequency Accuracy Measurement Circuit
MSTP	0x4008_4000	0x4008_4FFF	5	4	2 to 4	2 to 4	PCLKB	Module Stop Control
KINT	0x4008_5000	0x4008_5FFF	4	3	1 to 4	1 to 3	PCLKB	Key Interrupt Function
POEG	0x4008_A000	0x4008_AFFF	5	4	3 to 5	2 to 4	PCLKB	Port Output Enable for GPT
CANFD	0x400B_0000	0x400C_1FFF	5	4	2 to 5	2 to 4	PCLKB	CANFD Module
PSCU	0x400E_0000	0x400E_0FFF	5	4	2 to 5	2 to 4	PCLKB	Peripheral Security Control Unit
AGTn	0x400E_8000	0x400E_8FFF	7	4	4 to 7	2 to 4	PCLKB	Low Power Asynchronous General Purpose Timer n
TSN	0x400F_3000	0x400F_3FFF	5	4	2 to 5	2 to 4	PCLKB	Temperature Sensor
ACMPHSn	0x400F_4000	0x400F_4FFF	4	3	1 to 3	1 to 3	PCLKB	High-Speed Analog Comparator
CRC, DOC	0x4010_8000	0x4010_9FFF	5	4	2 to 5	2 to 4	PCLKA	Cyclic Redundancy Check, Data Operation Circuit
SCIn	0x4011_8000	0x4011_8FFF	5	4	2 to 4	2 to 4	PCLKA	Serial Communication Interface n
SPIn	0x4011_A000	0x4011_AFFF	5	4	2 to 5	2 to 4	PCLKA	Serial Peripheral Interface n
IICn	0x4011_F000	0x4011_FFFF	5	4	2 to 4	2 to 4	PCLKA	Inter-Integrated Circuit n
CANFD ECC	0x4012_F200	0x4012_FFFF	5	4	2 to 5	2 to 4	PCLKA	CANFD ECC Module
SCE5	0x4016_1000	0x4016_1FFF	6	4	3 to 6	2 to 4	PCLKA	Secure Cryptographic Engine
GPT32n, GPT_OPS (core clock = PCLKD)	0x4016_9000	0x4016_9FFF	8	5	5 to 8	3 to 5	PCLKA	General PWM Timer n, Output Phase Switching Controller
GPT32n, GPT_OPS (core clock = GPTCLK)	0x4016_9000	0x4016_9FFF	10	7	7 to 10	5 to 7	PCLKA	General PWM Timer n, Output Phase Switching Controller
GPT (GTCKCR)	0x4016_9B00	0x4016_9B00	5	4	2 to 4	2 to 4	PCLKA	GPT Clock Control Register
PDG	0x4016_A000	0x4016_AFFF	4	3	1 to 3	1 to 3	PCLKA	PWM Delay Generation
ADC	0x4017_0000	0x4017_0FFF	5	4	2 to 5	2 to 4	PCLKA	A/D Converter
ADC	0x4017_1000	0x4017_1FFF	4	3	1 to 3	1 to 3	PCLKA	A/D Converter
DAC12n	0x4017_2000	0x4017_2FFF	5	4	2 to 4	2 to 4	PCLKA	12-bit D/A Converter

Table A3.2 Access cycles (3 of 3)

Peripherals	Address		Number of access cycles				Cycle Unit	Related function
			ICLK = FCLK		ICLK > FCLK*1			
	From	To	Read	Write	Read	Write		
FLAD, FACI	0x407F_C000	0x407F_EFFF	5	4	2 to 5	2 to 4	FCLK	Data Flash, Flash Application Command Interface

Note 1. If the number of PCLK or FCLK cycles is non-integer (for example 1.5), the minimum value is without the decimal point, and the maximum value is rounded up to the decimal point. For example, 1.5 to 2. 5 is 1 to 3.

Appendix 4. Peripheral Variant

Table A4.1 shows the correspondence between the module name used in this manual and the Peripheral Variant.

Table A4.1 Module name vs Peripheral Variant

Module name	Peripheral Variant
ELC	ELC_B
AGTW	AGTW_B
SCI	SCI_B
IIC	IIC_B
CANFD	CANFD
SPI	SPI_B
SCE5	SCE5_B
ADC	ADC_B
DOC	DOC_B

Appendix 5. Related Documents

Component	Document Type	Description
Microcontrollers	Data sheet	Features, overview, and electrical characteristics of the MCU
	User's Manual: Hardware	MCU specifications such as pin assignments, memory maps, peripheral functions, electrical characteristics, timing diagrams, and operation descriptions
	Application Notes	Technical notes, board design guidelines, and software migration information
	Technical Update (TU)	Preliminary reports on product specifications such as restriction and errata
Software	User's Manual: Software	Command set, API reference and programming information
	Application Notes	Project files, guidelines for software programming, and application examples to develop embedded software applications
Tools & Kits, Solutions	User's Manual: Development Tools	User's manuals and quick start guides for developing embedded software applications with Software Packages, Development Kits, Starter Kits, Promotion Kits, Product Examples, and Application Examples
	Quick Start Guide	
	Application Notes	Project files, guidelines for software programming, and application examples to develop embedded software applications

Revision History

Revision 1.10 — Dec 9, 2021

First edition, issued

Revision 1.20 — Mar 31, 2022

1. Overview:
- Changed Package code in Table 1.11.
- Changed number of ACMPHS in Table 1.12.
- Changed description of KINT in Table 1.13.

2. Electrical Characteristics:
- Removed DAC12 from Reference power supply current in Table 2.7.
- Changed Package code in Table 2.11.
- Added parameter in Table 2.35.
- Changed full-scale error value in Table 2.35.
- Removed pseudo from DNL error in Table 2.35.

Appendix 2. Package Dimensions:
- Changed image in Figure 2.3 and Figure 2.5.

Appendix 3. I/O Registers:
- Changed Base address of IIC0WU_B.
- Changed module name of GPT320 to GPT329.

Revision 1.30 — Aug 05, 2022

Features:
- Updated Features.

1. Overview:
- Updated Table 1.3 System.
- Updated Table 1.8 Analog.
- Updated Table 1.10 Data processing accelerator.

2. Electrical Characteristics:
- Updated Note. 1 in Table 2.1 Absolute maximum ratings.
- Updated Table 2.7 Operating and standby current.
- Updated 2.4 A/D Converter Characteristics.
- Updated Table 2.45 PGA characteristics in Single-ended input mode.
- Updated Table 2.46 PGA characteristics in Pseudo-differential input mode.

Revision 1.40 — May 31, 2024

1. Overview:
- Updated Figure 1.2 Part numbering scheme.

2. Electrical Characteristics:
- Updated Table 2.32 IIC timing (2).
- Updated Table 2.36 A/D conversion characteristics (Oversampling mode and Hybrid mode) (1).
- Updated Figure 2.51 Digital filter characteristics (Minimum phase filter).

Appendix 3. I/O Registers:
- Changed CANFD_B to CANFD in Table 3.1 Peripheral base address.

Appendix 4. Peripheral Variant:
- Changed CANFD_B to CANFD in Table 4.1 Module name vs Peripheral Variant.

Revision 1.50 — Jul 2, 2025

2. Electrical Characteristics:
- Updated Table 2.33 CANFD interface timing

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You shall be responsible for determining what licenses are required from any third parties, and obtaining such licenses for the lawful import, export, manufacture, sales, utilization, distribution or other disposal of any products incorporating Renesas Electronics products, if required.
5. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
6. Renesas Electronics products are classified according to the following two quality grades: “Standard” and “High Quality”. The intended applications for each Renesas Electronics product depends on the product’s quality grade, as indicated below.
   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.
   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.

   Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user’s manual or other Renesas Electronics document.
7. No semiconductor product is absolutely secure. Notwithstanding any security measures or features that may be implemented in Renesas Electronics hardware or software products, Renesas Electronics shall have absolutely no liability arising out of any vulnerability or security breach, including but not limited to any unauthorized access to or use of a Renesas Electronics product or a system that uses a Renesas Electronics product. RENESAS ELECTRONICS DOES NOT WARRANT OR GUARANTEE THAT RENESAS ELECTRONICS PRODUCTS, OR ANY SYSTEMS CREATED USING RENESAS ELECTRONICS PRODUCTS WILL BE INVULNERABLE OR FREE FROM CORRUPTION, ATTACK, VIRUSES, INTERFERENCE, HACKING, DATA LOSS OR THEFT, OR OTHER SECURITY INTRUSION (“Vulnerability Issues”). RENESAS ELECTRONICS DISCLAIMS ANY AND ALL RESPONSIBILITY OR LIABILITY ARISING FROM OR RELATED TO ANY VULNERABILITY ISSUES. FURTHERMORE, TO THE EXTENT PERMITTED BY APPLICABLE LAW, RENESAS ELECTRONICS DISCLAIMS ANY AND ALL WARRANTIES, EXPRESS OR IMPLIED, WITH RESPECT TO THIS DOCUMENT AND ANY RELATED OR ACCOMPANYING SOFTWARE OR HARDWARE, INCLUDING BUT NOT LIMITED TO THE IMPLIED WARRANTIES OF MERCHANTABILITY, OR FITNESS FOR A PARTICULAR PURPOSE.
8. When using Renesas Electronics products, refer to the latest product information (data sheets, user’s manuals, application notes, “General Notes for Handling and Using Semiconductor Devices” in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
12. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
13. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
14. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note1) “Renesas Electronics” as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.

(Note2) “Renesas Electronics product(s)” means any product developed or manufactured by or for Renesas Electronics.

(Rev.5.0-1 October 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/.

© 2022 Renesas Electronics Corporation. All rights reserved.