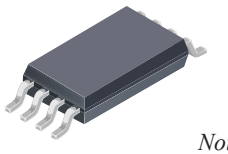
A1359

Factory-Programmed Dual-Output Linear-Hall Effect-Sensor IC with Analog and Pulse-Width-Modulated Outputs

FEATURES AND BENEFITS

- Dual tracking outputs: analog voltage output and pulse-width-modulated (PWM) output
- Matched analog and PWM outputs enable user to detect various output error conditions
- Factory-programmed offset, sensitivity, and polarity
- Sensitivity temperature coefficient (TC) and QVO/QD temperature coefficient programmed at Allegro™ for improved accuracy
- High-speed chopping scheme minimizes quiescent voltage output (QVO) drift across temperature
- Temperature-stable QVO and sensitivity
- Output voltage clamps provide short-circuit diagnostic capabilities
- Wide ambient temperature range: –40°C to 150°C
- Immune to mechanical stress
- Enhanced EMC performance for stringent automotive applications

PACKAGE: 8-pin TSSOP (suffix LE) surface mount



Not to scale

DESCRIPTION

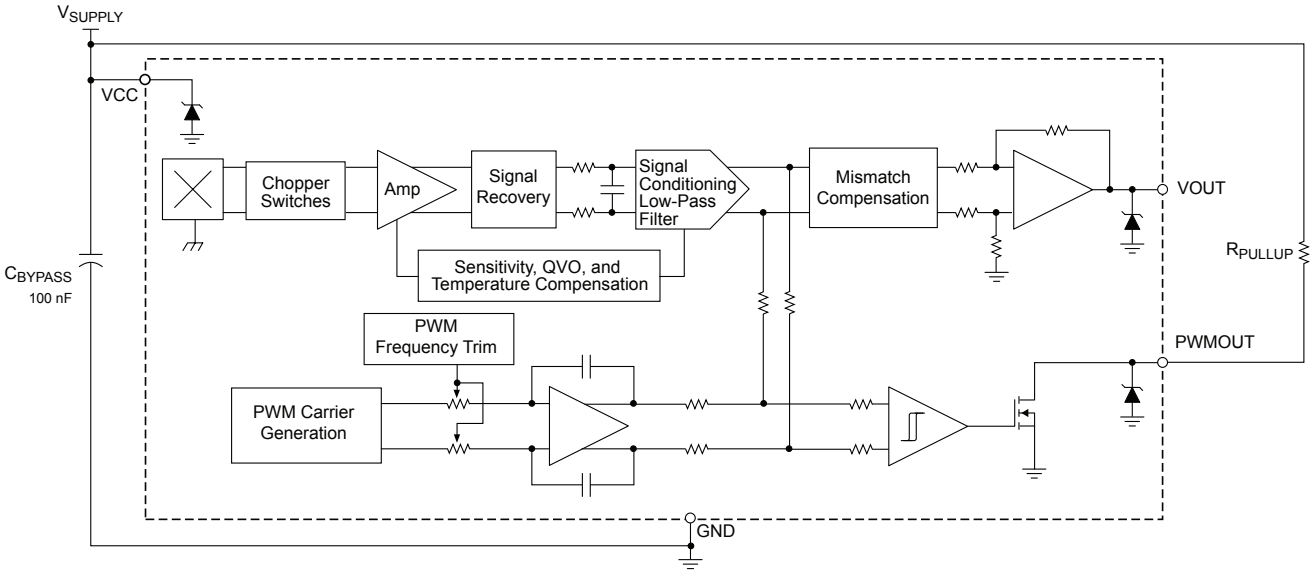
New applications for linear output Hall-effect sensors, such as displacement and angular position, require high accuracy in conjunction with redundant outputs. The Allegro A1359 programmable, linear, Hall effect sensor IC has been designed specifically to achieve both goals. The features associated with this linear device make it ideal for use in automotive and industrial applications requiring high accuracy, and this temperature-stable device operates across an extended temperature range: –40°C to 150°C.

The accuracy of the device is enhanced via programmability at the Allegro factory for optimization of device sensitivity, the quiescent voltage output (QVO: output with no magnetic field), and quiescent duty cycle (QD) for a given application or circuit. The A1359 also allows optimized performance across the entire operating temperature range via programming the temperature coefficients for both sensitivity and QVO/QD at Allegro end-of-line test. This ratiometric Hall-effect sensor IC provides an analog voltage, and a PWM signal with duty cycle, that are proportional to the applied magnetic field.

Each BiCMOS monolithic circuit integrates a Hall element, temperature-compensating circuitry to reduce the intrinsic sensitivity drift of the Hall element, a small-signal high-gain amplifier, a clamped low-impedance output stage and a proprietary dynamic offset cancellation technique.

The A1359 is provided in an 8-contact surface-mount TSSOP (suffix LE) which is lead (Pb) free, with 100% matte-tin leadframe plating.

Functional Block Diagram



SELECTION GUIDE

Part Number	Factory-Programmed Output Polarity	Packing*
A1359LLETR-MS-T	Forward: Output voltage increases with increasing positive (south) applied magnetic field	4000 units / reel
A1359LLETR-RP-MS-T	Reverse: Output voltage increases with increasing negative (north) applied magnetic field	4000 units / reel

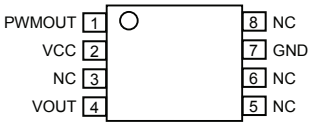
*Contact Allegro for additional packing options

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Unit
Forward Supply Voltage	V_{CC}	Refer to Power Derating section	6	V
Reverse Supply Voltage	V_{RCC}		–0.1	V
Forward Output Voltage	V_{OUT}	Refer to Power Derating section	7	V
Reverse Output Voltage	V_{ROUT}		–0.1	V
Forward PWM Output Voltage	V_{PWM}	Refer to Power Derating section	7	V
Reverse PWM Output Voltage	V_{RPWM}		–0.1	V
Output Source Current	$I_{OUT(SOURCE)}$	VOUT to GND	2	mA
Output Sink Current	$I_{OUT(SINK)}$	VCC to VOUT	10	mA
PWM Output Source Current	$I_{PWM(SOURCE)}$	V_{PWM} > –0.5 V, T_A = 25°C	–50	mA
PWM Output Sink Current	$I_{PWM(SINK)}$	Internal current limiting is intended to protect the device from momentary short circuits and not intended for continuous operation	25	mA
Operating Ambient Temperature	T_A	Temperature range L	–40 to 150	ºC
Storage Temperature	T_{stg}		–65 to 170	ºC
Maximum Junction Temperature	T_J(max)		165	ºC

PINOUT DIAGRAM AND TERMINAL LIST TABLE

Pinout Diagram



Terminal List Table

Number	Name	Function
1	PWMOUT	Open-drain PWM output
2	VCC	Input power supply; tie to GND with bypass capacitor
3	NC	No connect, tie to either GND or VCC
4	VOUT	Output signal
5	NC	No connect, tie to either GND or VCC
6	NC	No connect, tie to either GND or VCC
7	GND	Device ground
8	NC	No connect, tie to either GND or VCC

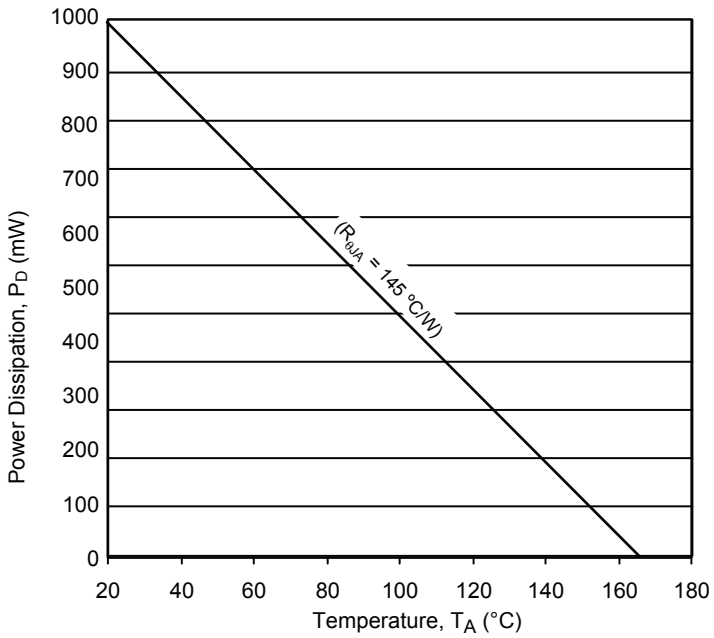
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THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	On 4-layer PCB based on JEDEC standard	145	ºC/W

*Additional thermal information available on the Allegro website

Power Dissipation versus Ambient Temperature



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OPERATING CHARACTERISTICS: Valid over full operating temperature range, T_A, C_{BYPASS} = 0.1 µF , V_{CC} = 5 V, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit[1]
ELECTRICAL CHARACTERISTICS						
Supply Voltage	V_{CC}		4.5	5	5.5	V
Undervoltage Threshold[2]	V_{UVLOHI}	T_A = 25°C (device powers on)	–	–	3	V
	$V_{UVLOLOW}$	T_A = 25°C (device powers off)	2.5	–	–	V
Supply Current	I_{CC}	V_{CC} = 5 V	–	10	13.5	mA
Supply Zener Clamp Voltage	V_Z	T_A = 25°C, I_{CC} = 20 mA	6	8.3	–	V
Internal Bandwidth[3]	BW_i	Small signal, –3 dB	–	2	–	kHz
Chopping Frequency[3,4]	f_C	T_A = 25°C	–	400	–	kHz
ANALOG OUTPUT CHARACTERISTICS						
Output Referred Noise[3]	V_N	T_A = 25°C, C_{BYPASS} = 0.1 µF, Sens = 5 mV/G, no load on VOUT	–	6	–	mV(p-p)
Input Referred RMS Noise Density[3]	V_{NRMS}	T = 25°C, C_{BYPASS} = open, no load on VOUT, f << BW_i	–	1.9	–	mG/√Hz
DC Output Resistance[3]	R_{OUT}		–	< 1	–	Ω
Output Load Resistance[3]	R_L	VOUT to GND	4.7	–	–	kΩ
Output Load Capacitance[3]	C_L	VOUT to GND	–	–	10	nF
Analog Output Current Limit	$I_{LIMIT(ALG)}$	R_{PULLUP} = 0 Ω	10	–	80	mA
Output Voltage Clamp[5]	V_{CLPH}	T_A = 25°C, B = +350 G, R_L = 10 kΩ (VOUT to GND)	4.25	4.5	4.65	V
	V_{CLPL}	T_A = 25°C, B = –350 G, R_L = 10 kΩ (VOUT to VCC)	0.4	0.5	0.7	V
Response Time[3]	$t_{RESPONSE_VOUT}$	Impulse magnetic field of 300 G	–	–	500	µs
Settling Time[3]	$t_{SETTLEVOUT}$	T_A = 25°C, Primary Overload > 5000 G	–	–	750	µs
Power-On Time for Analog[3]	t_{POVOUT}	T_A = 25°C, C_L (probe) = 10 pF, on VOUT	–	250	–	µs
Delay to Clamp for Analog[3]	$t_{CLPVOUT}$	T_A = 25°C, C_L = 10 nF, on VOUT	–	30	–	µs
PWM OUTPUT CHARACTERISTICS						
PWMOUT Saturation Voltage	V_{SAT}	$I_{PWMOUT(SINK)}$ ≤ 20 mA, PWMOUT transistor on	–	_	0.6	V
		$I_{PWMOUT(SINK)}$ ≤ 10 mA, PWMOUT transistor on	–	–	0.5	V
PWMOUT Current Limit	I_{LIMIT}	R_{PULLUP} = 0 Ω	30	60	110	mA
PWMOUT Leakage Current	I_{LEAK}	VCC = GND, 0 V ≤ V_{PWMOUT} ≤ 5 V, PWMOUT transistor off	–	0.1	10	µA
PWMOUT Zener Clamp Voltage	V_{ZOUT}	$I_{PWMOUT(SINK)}$ = 10 mA, T_A = 25ºC	28	–	–	V
PWMOUT Rise Time[3]	t_r	T_A = 25°C, R_{PULLUP} = 2 kΩ, C_L = 20 pF	–	3	–	µs
PWMOUT Fall Time[3]	t_f	T_A = 25°C, R_{PULLUP} = 2 kΩ, C_L = 20 pF	–	3	–	µs
Power-On Time for PWM[3]	t_{POPWM}	T_A = 25°C, C_L (probe) = 10 pF, on PWMOUT	–	500	–	µs
Delay to Clamp for PWM[3]	t_{CLPPWM}	T_A = 25°C, C_L = 10 nF, on PWMOUT	–	250	–	µs
Response Time[3]	$t_{RESPONSE_PWM}$	T_A = 25°C, Impulse magnetic field of 300 G	–	–	1.5	ms
Settling Time[3]	$t_{SETTLEPWM}$	T_A = 25°C, Primary Overload > 5000 G	–	–	2.25	ms

Continued on the next page…

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OPERATING CHARACTERISTICS (continued): Valid over full operating temperature range, T_A, C_{BYPASS} = 0.1 µF, V_{CC} = 5 V, unless otherwise noted

Characteristics	Symbol	Test Conditions		Min.	Typ.	Max.	Unit[1]
PWM OUTPUT CHARACTERISTICS (continued)							
Load Resistance[3,6]	R_{PULLUP}	PWMOUT to VCC		2000	–	–	Ω
Load Capacitance[3,6]	C_L	PWMOUT to GND		–	–	10	nF
Duty Cycle Jitter[3]	$Jitter_{PWM}$	Measured over 1000 PWM output clock periods, 3 sigma values, Sens = 9 mV/G		–	±0.18	–	%D
QUIESCENT VOLTAGE OUTPUT (QVO)							
Quiescent Voltage Output	$V_{OUT(Q)}$	T_A = 25°C		2.45	2.5	2.55	V
Quiescent Voltage Output Equivalent PWM	$D_{(Q)}$	T_A = 25°C, V_{CC} = 4.5 to 5.5 V		49	50	51	%D
PWM CARRIER FREQUENCY							
Carrier Frequency	f_{PWM}	T_A = 25°C		3.6	4	4.4	kHz
SENSITIVITY							
Sensitivity Temperature Coefficient	TC_{SENS}	Programmed at T_A = 150°C, calculated relative to Sens at 25°C		0.08	0.12	0.16	%/°C
Analog Sensitivity[7]	Sen	A1359LLETR-T, A1359LLETR-MS-T	B = ±125 G, T_A = 25°C	8.73	9.0	9.27	mV/G
		A1359LLETR-RP-T, A1359LLETR-RP-MS-T	B = ±125 G, T_A = 25°C	–9.27	–9.0	–8.73	mV/G
ERROR COMPONENTS							
PWM to Analog Output Mismatch[8]	V_{OUTERR}	1.75 V < V_{OUT} < 3.25 V		–57.4	–	+57.4	mV
		V_{OUT} = 1.25 V, V_{OUT} = 3.75 V		–85	–	+85	mV
Linearity Sensitivity Error[9]	Lin_{ERR}			–	±0.5	–	%
Symmetry Sensitivity Error[9]	Sym_{ERR}			–	±0.5	–	%
Ratiometry Quiescent Voltage Output Error[10]	$Rat_{VOUT(Q)}$	Across supply voltage range, (relative to V_{CC} = 5 V)		–	±0.5	–	%
Ratiometry Sensitivity Error[9]	Rat_{Sens}	Across supply voltage range, (relative to V_{CC} = 5 V)		–	±0.5	–	%
Ratiometry Clamp Error[10]	$Rat_{VOUTCLP}$	T_A = 25°C, across supply voltage range, (relative to V_{CC} = 5 V)		–	±0.5	–	%
Quiescent Voltage Output Drift Through Temperature Range	$\Delta V_{OUT(Q)}$	T_A =150°C		–17	–	+17	mV
Sensitivity Drift Due to Package Hysteresis	$\Delta Sens_{PKG}$	T_A = 25°C, after temperature cycling		–	±2	–	%

[1] 1 G (gauss) = 0.1 mT (millitesla).
[2] At power-up, the output is held low until V_{CC} exceeds V_{UVLOHI}. When the device reaches the operational power level, the output remains valid until V_{CC} drops below V_{UVLOLO}, when the output is pulled low.
[3] Determined by design and characterization, not evaluated at final test.
[4] f_c varies as much as approximately ±20% across the full operating ambient temperature range and process.
[5] V_{CLPL} and V_{CLPH} scale with V_{CC}, due to ratiometry.
[6] Load capacitance and resistance directly effects the rise time of the PWM output by $t_r = 0.35 \times 2 \times \pi \times R_L \times C_L$.
[7] Room temperature sensitivity can drift, $\Delta Sens_{LIFE}$, by an additional 3% (typical worst case) over the life of the product.
[8] See Characteristic Definitions section.
[9] Applicable to both analog and PWM channels. Tested at Allegro factory for only the analog channel, and determined by design and characterization for the PWM channel.
[10] Applies only to the analog channel.

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CHARACTERISTIC DEFINITIONS

Power-On Time: When the supply is ramped to its operating voltage, the device requires a finite time to power its internal components before supplying a valid PWM output duty-cycle. Power-On Time for analog output, t_{POVOUT}, is defined as the time it takes for the output voltage to settle within ±10% of its steady-state value after the power supply has reached its minimum specified operating voltage, $V_{CC(min)}$. (See Figure 1.)

Power-On Time is specified in a different way for the PWM output than the analog output. For the PWM output, the Power-On Time, t_{POPWM}, is defined as the time it takes for the duty cycle to settle within ±10% of the target steady state value from the time the power supply has reached the minimum specified operating voltage, $V_{CC(min)}$. (See Figure 2.)

Response Time: The time interval, $t_{RESPONSEPWM}$ or $t_{RESPONSEVOUT}$, between: a) when the applied magnetic field reaches 90% of its final value, and b) when the sensor IC reaches 90% of its output corresponding to the applied magnetic field (PWM duty cycle or analog V_{OUT}). Figure 3 illustrates an example with the PWM output. Response time is conceptually the same for the analog output.

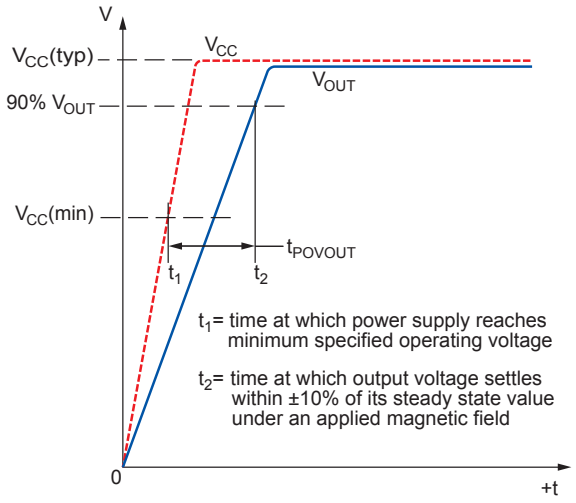


Figure 1: Definition of Analog Power-On Time, t_{POVOUT}

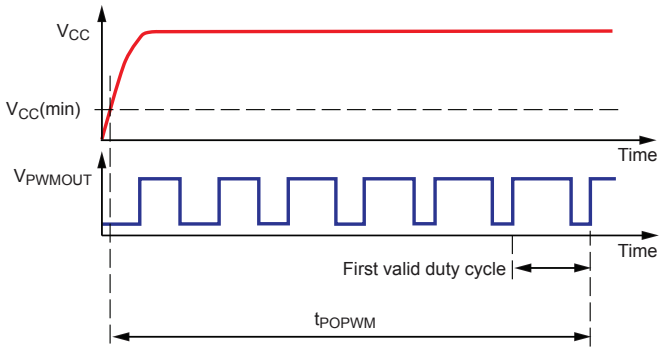


Figure 2: Definition of PWM Power-On Time, t_{POPWM}

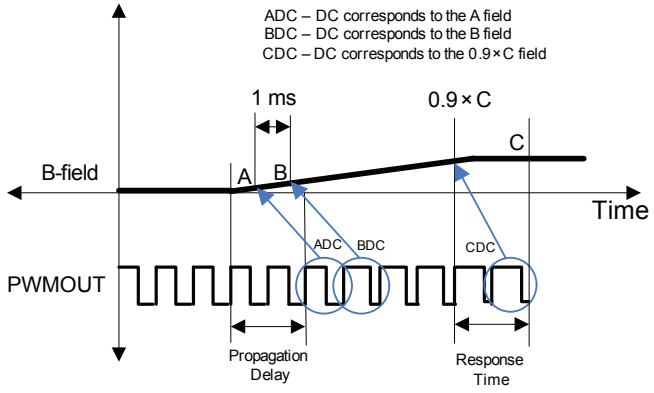


Figure 3: Definition of Response Time for PWM output

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Delay to Clamp: A large magnetic input step may cause the clamp to overshoot its steady-state value. The delay to clamp, $t_{CLPVOUT}$, is defined as the time it takes for the output voltage to settle within 1% of its steady-state value after initially passing through its steady-state voltage. This is conceptually the same for the PWM output duty cycle settling to the steady-state value. (See Figure 4.)

Quiescent Voltage Output: In the quiescent state (no significant magnetic field: B = 0 G), the analog output, V_{OUT}, is ratiometric to the supply voltage, V_{CC}, throughout the entire operating range of V_{CC}. The PWM output, V_{PWMOUT}, by virtue of being a % duty-cycle will remain at 50% nominal throughout the entire V_{CC} operating range (4.5 to 5.5 V).

Quiescent Output Drift through Temperature Range: Due to internal component tolerances and thermal considerations, the Quiescent Voltage Output, $V_{OUT(Q)}$, may drift from its nominal value across the operating ambient temperature, T_A. For purposes of specification, the Quiescent Voltage Output Drift Through Temperature Range, $\Delta V_{OUT(Q)}$ (mV), is defined as:

$$\Delta V_{OUT(Q)} = V_{OUT(Q)(TA)} - V_{OUT(Q)(25°C)} \quad (1)$$

Sensitivity: Assuming the sensitivity of the device is positive (Positive Polarity: A1359LLETR-T, A1359LLETR-MS-T), the presence of a south-polarity magnetic field perpendicular to the branded surface of the package face increases the output voltage from its quiescent value toward the supply voltage rail.

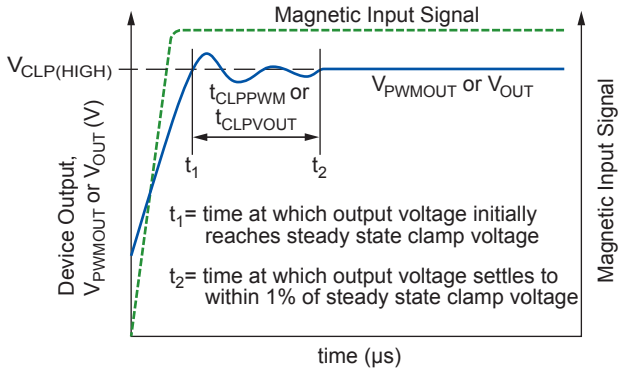


Figure 4: Definition of Delay to Clamp

The amount of the output voltage increase is proportional to the magnitude of the magnetic field applied. Conversely, the application of a north-polarity field decreases the output voltage from its quiescent value. For the case of the reverse polarity device (A1359LLETR-RP-T, A1359LLETR-RP-MS-T), the presence of a south-polarity magnetic field perpendicular to the branded surface of the package face decreases the output voltage from its quiescent value toward the ground rail. The amount of the output voltage decrease is proportional to the magnitude of the magnetic field applied. Conversely, the application of a north-polarity field increases the output voltage from its quiescent value. This proportionality is specified as the magnetic sensitivity, Sens (mV/G), of the device and is defined as:

$$\text{Sens} = \frac{V_{OUT(BPOS)} - V_{OUT(BNEG)}}{\text{BPOS} - \text{BNEG}} \quad (2)$$

where BPOS and BNEG are two magnetic fields with opposite polarities.

Sensitivity Temperature Coefficient: Device sensitivity changes as temperature changes, with respect to its programmed Sensitivity Temperature Coefficient, TC_{SENS}. TC_{SENS} is programmed at 150°C, and calculated relative to the nominal sensitivity programming temperature of 25°C. TC_{SENS} (%/°C) is defined as:

$$TC_{SENS} = \left(\frac{Sens_{T2} - Sens_{T1}}{Sens_{T1}} \times 100\%\right)\left(\frac{1}{T2 - T1}\right) \quad (3)$$

where T1 is the nominal Sens programming temperature of 25°C, and T2 is the TC_{SENS} programming temperature of 150°C. The ideal value of Sens through the full ambient temperature range, $Sens_{IDEAL(TA)}$, is defined as:

$$Sens_{IDEAL(TA)} = Sens_{T1} \times [100\% + TC_{SENS}(T_A - T1)] \quad (4)$$

Sensitivity Drift Due to Package Hysteresis: Package stress and relaxation can cause the device sensitivity at T_A = 25°C to change during and after temperature cycling. This change in sensitivity follows a hysteresis curve. For purposes of specification, the Sensitivity Drift Due to Package Hysteresis, $\Delta Sens_{PKG}$, is defined as:

$$\Delta Sens_{PKG} = \frac{Sens_{(25°C)2} - Sens_{(25°C)1}}{Sens_{(25°C)1}} \times 100\ (\%) \quad (5)$$

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where $Sens_{(25°C)1}$ is the programmed value of sensitivity at T_A = 25°C, and $Sens_{(25°C)2}$ is the value of sensitivity at T_A = 25°C, after temperature cycling T_A up to 150°C, down to –40°C, and back to up 25°C.

Linearity Sensitivity Error: The A1359 is designed to provide linear output in response to a ramping applied magnetic field. Consider two magnetic fields, B1 and B2. Ideally, the sensitivity of a device is the same for both fields, for a given supply voltage and temperature. Linearity error is present when there is a difference between the sensitivities measured at B1 and B2.

Linearity Sensitivity Error is calculated separately for the positive (Lin_{ERRPOS}) and negative (Lin_{ERRNEG}) applied magnetic fields. Linearity error (%) is measured and defined as:

$$Lin_{ERRPOS} = \left(1 - \frac{Sens_{BPOS2}}{Sens_{BPOS1}}\right) \times 100\ (\%)$$

$$Lin_{ERRNEG} = \left(1 - \frac{Sens_{BNEG2}}{Sens_{BNEG1}}\right) \times 100\ (\%) \quad (6)$$

where:

$$Sens_{Bx} = \frac{|V_{OUT(Bx)} - V_{OUT(Q)}|}{B_x} \quad (7)$$

and BPOSx and BNEGx are positive and negative magnetic fields, with respect to the quiescent voltage output such that $B_{POS2} > B_{POS1}$ and $B_{NEG2} > B_{NEG1}$.

Then:

$$Lin_{ERR} = \max(|Lin_{ERRPOS}|, |Lin_{ERRNEG}|) \quad (8)$$

Clamping Range: The output voltage clamps, V_{CLPH} and V_{CLPL}, limit the operating magnetic range of the applied field in which the device provides a linear output. The maximum positive and negative applied magnetic fields in the operating range can be calculated:

$$|BPOS(max)| = \frac{V_{CLP(HIGH)} - V_{OUT(Q)}}{Sens}$$

$$|BNEG(max)| = \frac{V_{OUT(Q)} - V_{CLP(LOW)}}{Sens} \quad (9)$$

Symmetry Sensitivity Error: The magnetic sensitivity of the A1359 device is constant for any two applied magnetic fields of equal magnitude and opposite polarities. Symmetry Sensitivity Error, Sym_{ERR} (%), is measured and defined as:

$$Sym_{ERR} = \left(1 - \frac{Sens_{BPOS}}{Sens_{BNEG}}\right) \times 100\ (\%) \quad (10)$$

where $Sens_{Bx}$ is as defined in equation 7, and BPOS and BNEG are positive and negative magnetic fields such that $|B_{POS}| = |B_{NEG}|$.

Ratiometry Error: The A1359 provides a ratiometric output. This means that the quiescent voltage output, $V_{OUT(Q)}$, magnetic sensitivity, Sens, and clamp voltage, V_{CLPH} and V_{CLPL}, are proportional to the supply voltage, V_{CC}. In other words, when the supply voltage increases or decreases by a certain percentage, each characteristic also increases or decreases by the same percentage. Error is the difference between the measured change in the supply voltage relative to 5 V, and the measured change in each characteristic.

The ratiometric error in quiescent voltage output, $Rat_{VOUT(Q)}$ (%), for a given supply voltage, V_{CC}, is defined as:

$$Rat_{ERRVOUT(Q)} = \left(1 - \frac{V_{OUT(Q)(VCC)} / V_{OUT(Q)(5V)}}{V_{CC} / 5\ V}\right) \times 100\ (\%) \quad (11)$$

The ratiometric error in magnetic sensitivity, Rat_{Sens} (%), for a given supply voltage, V_{CC}, is defined as:

$$Rat_{ERRSens} = \left(1 - \frac{Sens_{(VCC)} / Sens_{(5V)}}{V_{CC} / 5\ V}\right) \times 100\ (\%) \quad (12)$$

The ratiometric error in the clamp voltages, $Rat_{VOUTCLP}$ (%), for a given supply voltage, V_{CC}, is defined as:

$$Rat_{VOUTCLP} = \left(1 - \frac{V_{CLP(VCC)} / V_{CLP(5V)}}{V_{CC} / 5\ V}\right) \times 100\ (\%) \quad (13)$$

where V_{CLP} is either V_{CLPH} or V_{CLPL}.

Note: Equations 11 and 13 apply to the analog channel (V_{OUT}), only. Recall that for the PWM output, the 0 G output is 50% from 4.5 to 5.5 V. However, as sensitivity is ratiometric with V_{CC} for both analog and PWM channels, equation 12 applies to both the analog and the PWM channels.

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Duty Cycle Jitter: The duty cycle of the PWM output may vary slightly over time despite the presence of a constant applied magnetic field and a constant Carrier Frequency, f_{PWM}, for the PWM signal. This phenomenon is known as jitter, $Jitter_{PWM}$ (%), and is defined as:

$$Jitter_{PWM} = \pm \frac{D_B(max) - D_B(min)}{2} \quad (14)$$

where $D_B(max)$ and $D_B(min)$ are the maximum and minimum duty cycles, measured in 1000 PWM clock periods, in a constant applied magnetic field.

Undervoltage Lockout: The A1359 features an undervoltage lockout function that ensures that the device will output a valid signal when V_{CC} is above a certain threshold, V_{UVLOHI}, and remains valid until V_{CC} falls below a lower threshold, $V_{UVLOLOW}$. The undervoltage lockout feature provides a hysteresis of operation to eliminate indeterminate output states.

The output of the A1359 is held low (GND) until V_{CC} exceeds V_{UVLOHI} . When V_{CC} exceeds V_{UVLOHI}, the device powers-up and the output provides a ratiometric output voltage proportional to the input magnetic signal, and V_{CC} . If V_{CC} should drop back down below $V_{UVLOLOW}$ for more than t_{uvlo} after the device is powered-up, the output would be pulled low. (See Figure 5.)

PWM to Analog Output Mismatch: When comparing the PWM output to the analog output for channel mismatch, the following equation is used to convert PWM (% D, duty cycle) to voltage (V):

$$V_{PWMOUT} = D_{(Q)} + D_{(field)} = V_{OUT(Q)} \times 20.0\ \%D/V + V_{OUT(B)} \times 21.0\%D/V \quad (15)$$

where:

$D_{(Q)}$ is the quiescent PWM signal with no input field (B = 0 G), and $D_{(field)}$ is the PWM signal in response to the input magnetic field. In other words, the product of PWM sensitivity (%D/G) and input magnetic field (G). (See Figure 6.)

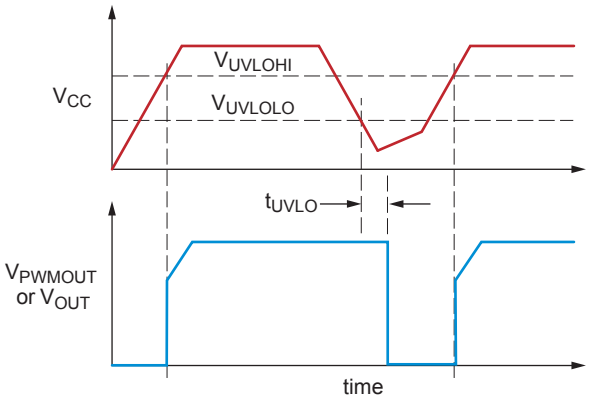


Figure 5: UVLO operation

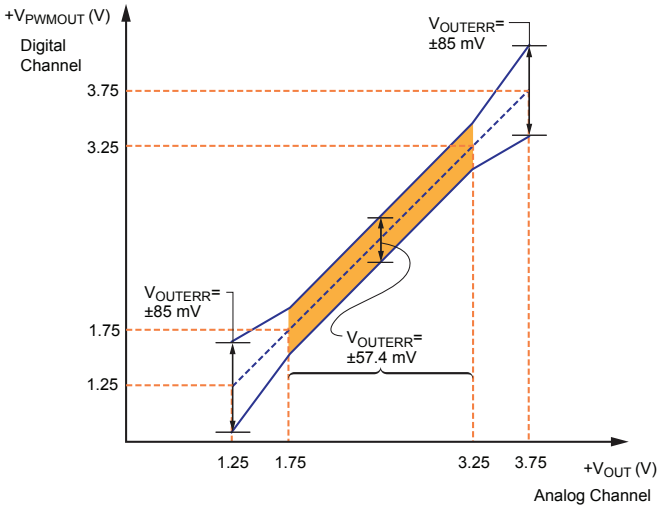


Figure 6: Definition of PWM to Analog Output Mismatch, V_{OUTERR}

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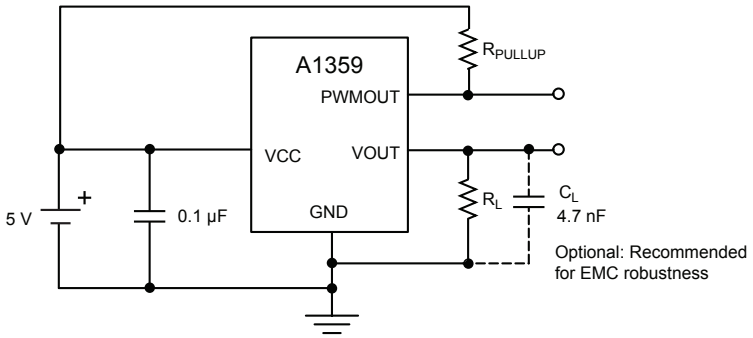


Figure 7: Typical Application Circuit

Chopper Stabilization Technique

When using Hall-effect technology, a limiting factor for switch point accuracy is the small-signal voltage developed across the Hall element. This voltage is disproportionally small relative to the offset that can be produced at the output of the Hall sensor IC. This makes it difficult to process the signal while maintaining an accurate, reliable output over the specified operating temperature and voltage ranges. Chopper stabilization is a unique approach used to minimize Hall offset on the chip. Allegro employs a technique to remove key sources of the output drift induced by thermal and mechanical stresses. This offset reduction technique is based on a signal modulation-demodulation process. The undesired offset signal is separated from the magnetic field-induced signal in the frequency domain, through modulation. The subsequent demodulation acts as a modulation process for the offset, causing the magnetic field-induced signal to recover its original spectrum at base band, while the DC offset becomes a high-frequency signal. The magnetic-sourced signal then can pass through a low-pass filter, while the modulated DC offset is suppressed. In addition to the removal of the thermal- and stress-related offset, this novel technique also reduces the amount of thermal noise in the Hall sensor while completely removing the modulated residue resulting from the chopper operation. The chopper stabilization technique uses a high-frequency sampling clock. For demodulation process, a sample-and-hold technique is used. This high-frequency operation allows a greater sampling rate, which results in higher accuracy and faster signal-processing capability. This approach desensitizes the chip to the effects of thermal and mechanical stresses, and produces devices that have extremely stable quiescent Hall output voltages and precise recoverability after temperature cycling. This technique is made possible through the use of a BiCMOS process, which allows the use of low-offset, low-noise amplifiers in combination with high-density logic integration and sample-and-hold circuits.

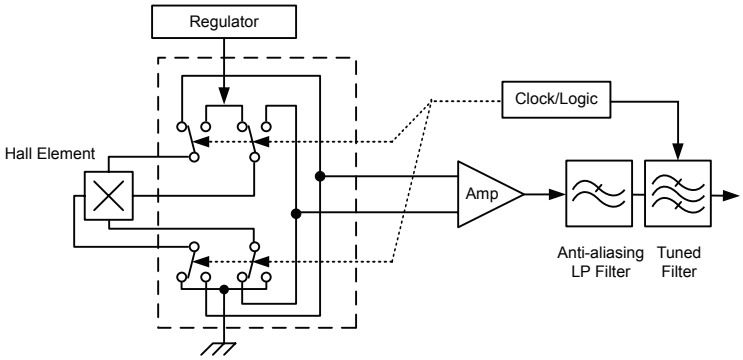


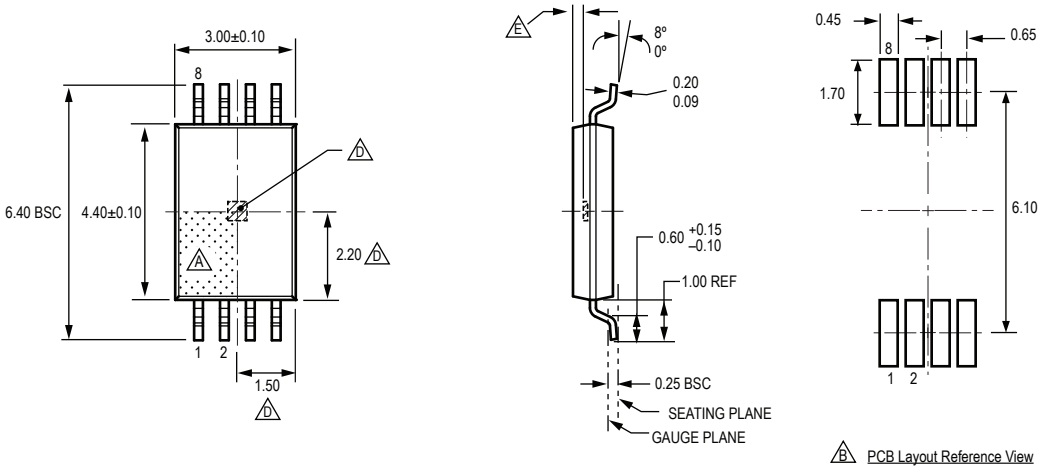
Figure 8: Concept of Chopper Stabilization Technique

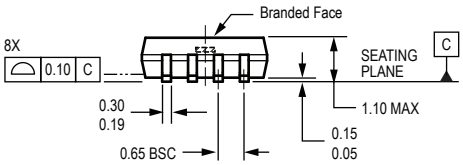
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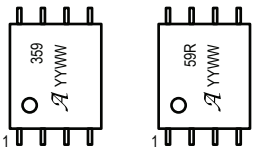
Package LE, 8-Pin TSSOP

For Reference Only – Not for Tooling Use

(Reference Allegro DWG-0000381, Rev. 1 and JEDEC MO-153AA)
Dimensions in millimeters - NOT TO SCALE
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown







A1359LLETR-T A1359LLETR-RP-T

A Terminal #1 mark area

B Reference land pattern layout (reference IPC7351 SOP65P640X110-8M); All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

Branding scale and appearance at supplier discretion

D Hall element, not to scale

E Active Area Depth 0.36 mm REF

C Branding Reference View

Top line is device designator
A = Supplier emblem
Y = Last two digits of year of manufacture
W = Week of manufacture

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Revision History

Revision	Revision Date	Description of Revision
1	June 18, 2013	Update I_{CC} and package drawing.
2	February 26, 2016	Added A1359LLETR-MS-T and A1359LLETR-RP-MS-T part options.
3	February 19, 2019	Minor editorial updates
4	March 13, 2020	Minor editorial updates
5	March 7, 2022	Updated package drawing reference number (page 11)
6	February 24, 2026	Removed A1359LLETR-RP-T and A1359LLETR-T from the selection guide (page 2)

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