20 mΩ, Fast Turn On, 2.5 A Load Switch with Discharge

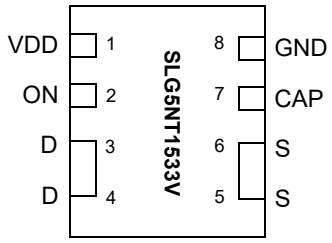
General Description

The SLG5NT1533V is a 20 mΩ 2.5 A single-channel load switch with configurable slew rate control. The device can enable fast power rail turn on with big cap loading. Internal circuit limits max inrush current to prevent device damage. The product is packaged in an ultra-small 1.0 x 1.6 mm package.

Features

- 1.0 x 1.6 x 0.55 mm FC-STDFN package (2 fused pins for drain and 2 fused pins for source)
- Logic level ON pin capable of supporting 0.85 V CMOS Logic
- Discharged Load when off
- Fast Turn On time
  - 32 µs, C_{SLEW} = 0.1 nF, C_{LOAD} = 1 µF, I_{DS} = 100 mA
  - 102 µs, C_{SLEW} = 0.5 nF, C_{LOAD} = 10 µF, I_{DS} = 2.5 A
- Low RDS_{ON} while supporting 2.5 A
  - 20 mΩ, V_{DD} = 5 V, V_D = 1 V
  - 27.5 mΩ, V_{DD} = 3.3 V, V_D = 1 V
- Pb-Free / Halogen-Free / RoHS compliant
- Operating Temperature: -40 °C to 85°C
- Operating Voltage: 2.5 V to 5.5 V
- Power Rail Switching V_D = 0.85 V to V_D = V_{DD} - 1.5 V

Pin Configuration

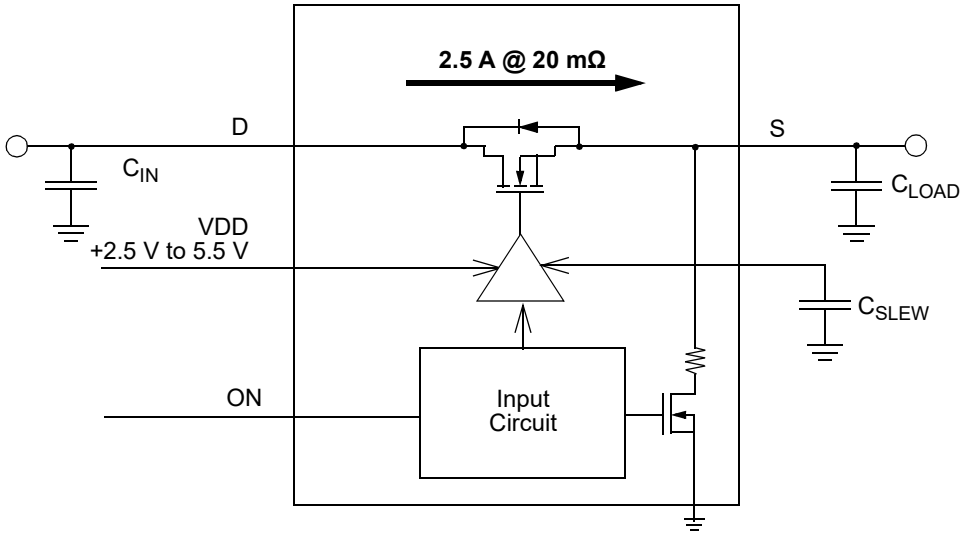


8-pin FC-STDFN
(Top View)

Applications

- Fast Turn On/Off power rail switching with big load capacitance
- Frequent wake & sleep power cycle
- Mobile devices and portable devices

Block Diagram



©2022 Renesas Electronics Corporation

Pin Description

Pin #	Pin Name	Type	Pin Description
1	VDD	PWR	VDD supplies the power for the operation of the load switch and internal control circuitry. Bypass the VDD pin to GND with a 0.1 µF (or larger) capacitor.
2	ON	Input	A low-to-high transition on this pin initiates the operation of the SLG5NT1533V's state machine. ON is a CMOS input with ON_V_{IL} < 0.3 V and ON_V_{IH} > 0.85 V thresholds. While there is an internal pull-down circuit to GND (~4 MΩ), connect this pin directly to a general-purpose output (GPO) of a microcontroller, an application processor, or a system controller.
3, 4	D	MOSFET	Drain terminal connection of the n-channel MOSFET (2 pins fused for V_D). Connect at least a low-ESR 0.1 µF capacitor from this pin to ground. Capacitors used at V_D should be rated at 10 V or higher.
5, 6	S	MOSFET	Source terminal connection of the n-channel MOSFET (2 pins fused for V_S). Connect a low-ESR capacitor from this pin to ground and consult the Electrical Characteristics table for recommended C_{LOAD} range. Capacitors used at V_S should be rated at 10 V or higher.
7	CAP	Input	A low-ESR, stable dielectric, ceramic surface-mount capacitor connected from CAP pin to GND sets the V_S slew rate and overall turn-on time of the SLG5NT1533V. Capacitors at CAP pin should be rated at 10 V or higher.
8	GND	GND	Ground connection. Connect this pin to system analog or power ground plane.

Ordering Information

Part Number	Type	Production Flow
SLG5NT1533V	FC-STDFN 8L	Industrial, -40 °C to 85 °C
SLG5NT1533VTR	FC-STDFN 8L (Tape and Reel)	Industrial, -40 °C to 85 °C

©2022 Renesas Electronics Corporation

Absolute Maximum Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Power Supply		--	--	7	V
V_D to GND	Load Switch Input Voltage to GND		-0.3	--	V_{DD}	V
V_S to GND	Load Switch Output Voltage to GND		-0.3	--	V_D	V
ON and CAP to GND	ON and CAP Pin Voltages to GND		-0.3	--	V_{DD}	V
T_S	Storage Temperature		-65	--	150	°C
T_J	Junction Temperature		--	--	150	°C
ESD_{HBM}	ESD Protection	Human Body Model	2000	--	--	V
MSL	Moisture Sensitivity Level			1		
θ_{JA}	Thermal Resistance	1.6 x 1 mm, 8L STDFN; Determined using 1 in^2, 1 oz. copper pads under each VD and VS terminals and FR4 pcb material	--	75	--	°C/W
W_{DIS}	Package Power Dissipation		--	--	0.4	W
MOSFET IDS_{PK}	Peak Current from Drain to Source	For no more than 20 µs with 1% duty cycle	--	--	25.0	A
		For no more than 50 µs with 1% duty cycle	--	--	12.5	A
		For no more than 1 ms with 1% duty cycle	--	--	3.5	A

Note: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Electrical Characteristics

T_A = -40 °C to 85 °C. Typical values are at T_A = 25 °C unless otherwise noted.

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Power Supply Voltage	-40 °C to 85 °C	2.5	--	5.5	V
I_{DD}	Power Supply Current (PIN 1)	when OFF	--	--	1	µA
		when ON, No load	--	--	10	µA
RDS_{ON}	ON Resistance, T_A = 25°C	V_{DD} = 5 V, V_D = 1.0 V, V_{DD} - V_D = 4.0 V, R_{LOAD} = 0.5 Ω	--	20	24	mΩ
		V_{DD} = 3.3 V, V_D = 1.0 V, V_{DD} - V_D = 2.3 V, R_{LOAD} = 0.5 Ω	--	27.5	31	mΩ
	ON Resistance, T_A = 70°C	V_{DD} = 5 V, V_D = 1.0 V, V_{DD} - V_D = 4.0 V, R_{LOAD} = 0.5 Ω	--	23.5	27	mΩ
		V_{DD} = 3.3 V, V_D = 1.0 V, V_{DD} - V_D = 2.3 V, R_{LOAD} = 0.5 Ω	--	31	35	mΩ
	ON Resistance, T_A = 85°C	V_{DD} = 5 V, V_D = 1.0 V, V_{DD} - V_D = 4.0 V, R_{LOAD} = 0.5 Ω	--	24.5	28	mΩ
		V_{DD} = 3.3 V, V_D = 1.0 V, V_{DD} - V_D = 2.3 V, R_{LOAD} = 0.5 Ω	--	33	37	mΩ
MOSFET IDS	Current from D to S	Continuous, V_D = 0.85 V to 3.3 V	--	--	2.5	A
V_D	Drain Voltage		0.85	--	V_{DD} - 1.5	V

©2022 Renesas Electronics Corporation

Electrical Characteristics (continued)

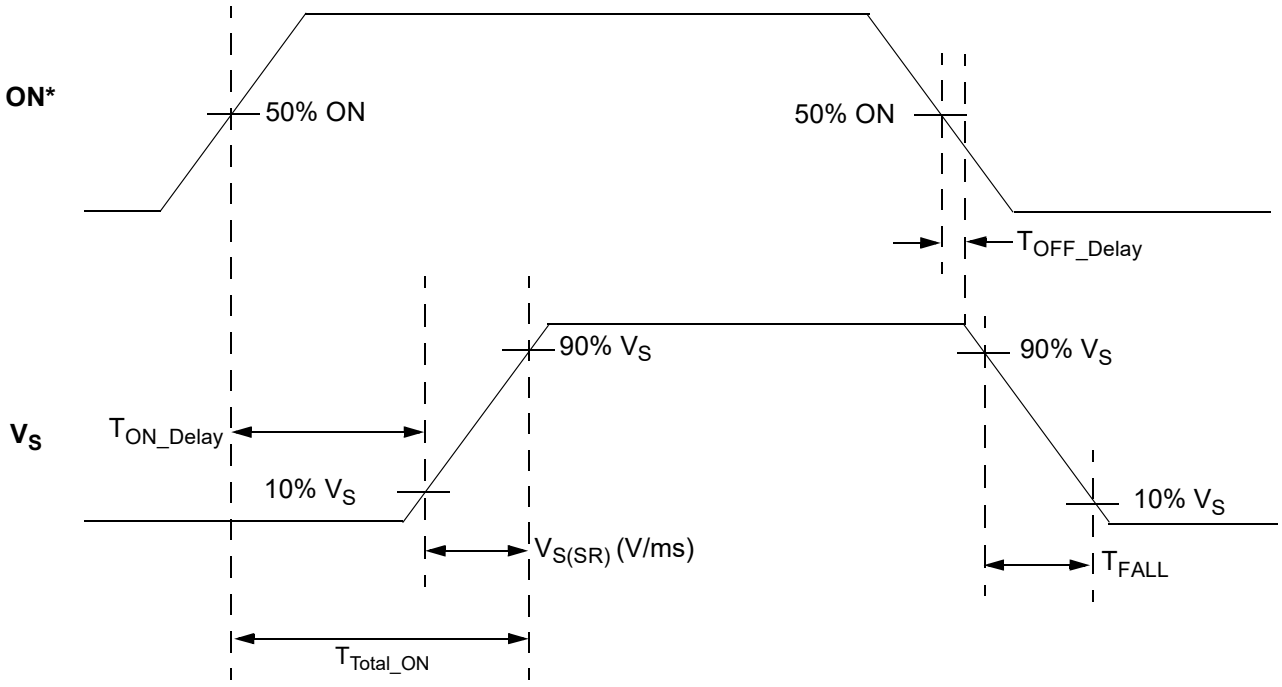
T_A = -40 °C to 85 °C. Typical values are at T_A = 25 °C unless otherwise noted.

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
T_{ON_Delay}	ON Delay Time	50% ON to 10% V_S, V_{DD} = 5 V, V_D = 1.0 V, C_{SLEW} = 0.1 nF	--	12	15	µs
		50% ON to 10% V_S, V_{DD} = 5 V, V_D = 1.0 V, C_{SLEW} = 0.5 nF	--	32	35	µs
T_{Total_ON}	Total Turn On Time	50% ON to 90% V_S	Set by External C_{SLEW}[1]			µs
		50% ON to 90% V_S, V_{DD} = 5 V, V_D = 1.0 V, C_{LOAD} = 1 µF, I_{DS} = 50 mA, C_{SLEW} = 0.1 nF	--	32	39	µs
		50% ON to 90% V_S, V_{DD} = 5 V, V_D = 1.0 V, C_{LOAD} = 1 µF, I_{DS} = 100 mA, C_{SLEW} = 0.1 nF	--	32	39	µs
		50% ON to 90% V_S, V_{DD} = 5 V, V_D = 1.0 V, C_{LOAD} = 4.7 µF, I_{DS} = 2.5 A, C_{SLEW} = 0.5 nF	--	102	123	µs
		50% ON to 90% V_S, V_{DD} = 5 V, V_D = 1.0 V, C_{LOAD} = 10 µF, I_{DS} = 2.5 A, C_{SLEW} = 0.5 nF	--	102	123	µs
$V_{S(SR)}$	Slew Rate	10% V_S to 90% V_S	Set by External C_{SLEW}[1]			V/ms
		10% V_S to 90% V_S, V_{DD} = 5 V, V_D = 1.0 V, C_{LOAD} = 1 µF, I_{DS} = 50 mA, C_{SLEW} = 0.1 nF	--	65	78	V/ms
		10% V_S to 90% V_S, V_{DD} = 5 V, V_D = 1.0 V, C_{LOAD} = 1 µF, I_{DS} = 100 mA, C_{SLEW} = 0.1 nF	--	65	78	V/ms
		10% V_S to 90% V_S, V_{DD} = 5 V, V_D = 1.0 V, C_{LOAD} = 4.7 µF, I_{DS} = 2.5 A, C_{SLEW} = 0.5 nF	--	13	16	V/ms
		10% V_S to 90% V_S, V_{DD} = 5 V, V_D = 1.0 V, C_{LOAD} = 10 µF, I_{DS} = 2.5 A, C_{SLEW} = 0.5 nF	--	13.5	16.5	V/ms
C_{LOAD}	Output Load Capacitance	C_{LOAD} connected from S to GND	--	--	10	µF
$R_{DISCHRGE}$	Discharge Resistance		100	150	300	Ω
ON_V_{IH}	High Input Voltage on ON pin		0.85	--	V_{DD}	V
ON_V_{IL}	Low Input Voltage on ON pin		-0.3	0	0.3	V
T_{OFF_Delay}	OFF Delay Time	50% ON to V_S Fall Start, no C_{LOAD}, R_{LOAD} = 20 Ω, V_{DD} = 5 V, V_D = 1.0 V, No C_{SLEW}	--	120	150	µs
$THERM_{OFF}$	Thermal shutoff turn-off temperature	Programmable, automatic shutoff temperature	--	125	--	°C
$THERM_{OFFACC}$	Thermal Sensor Accuracy		--	--	±20	%
$THERM_{DT}$	Thermal Disable Time	Thermal sensor disable for the ON rising edge to 100 µs. Prevent thermal shutdown from inrush current	--	--	100	µs

Notes:
1. Refer to typical timing parameter vs. C_{SLEW} performance charts for additional information when available.

©2022 Renesas Electronics Corporation

T_{ON_Delay}, $V_{S(SR)}$, and T_{Total_ON} Timing Details

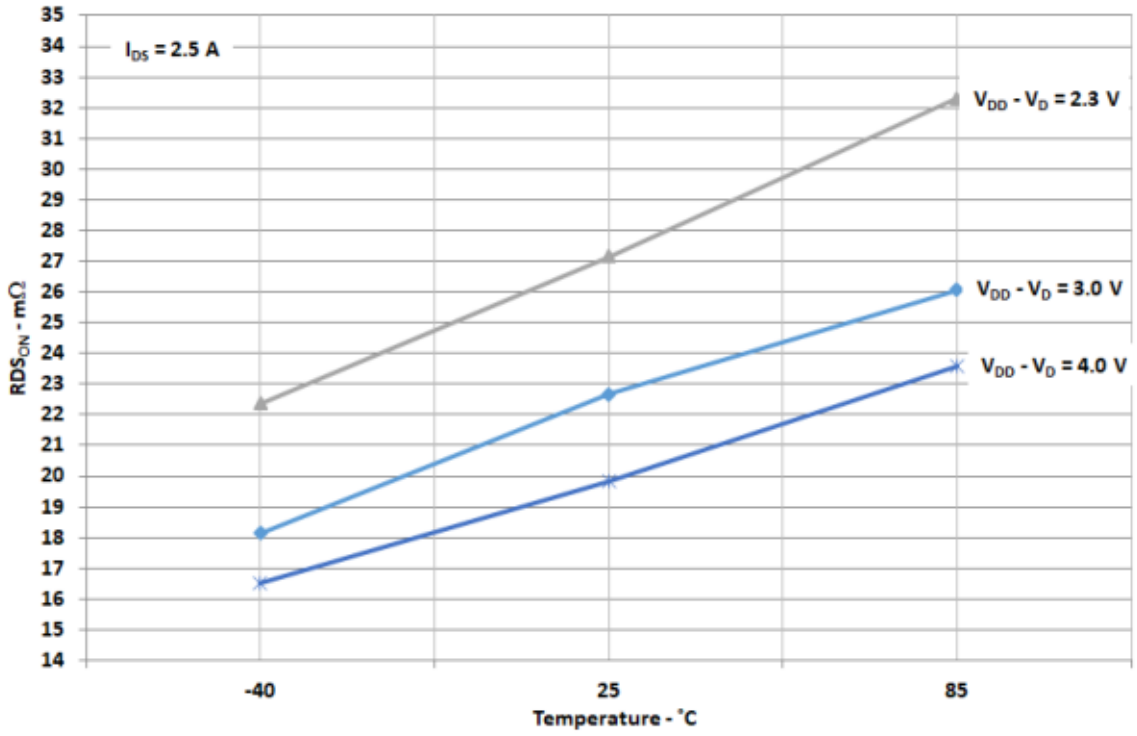


Note: * Rise and Fall times of the ON signal are 100 ns

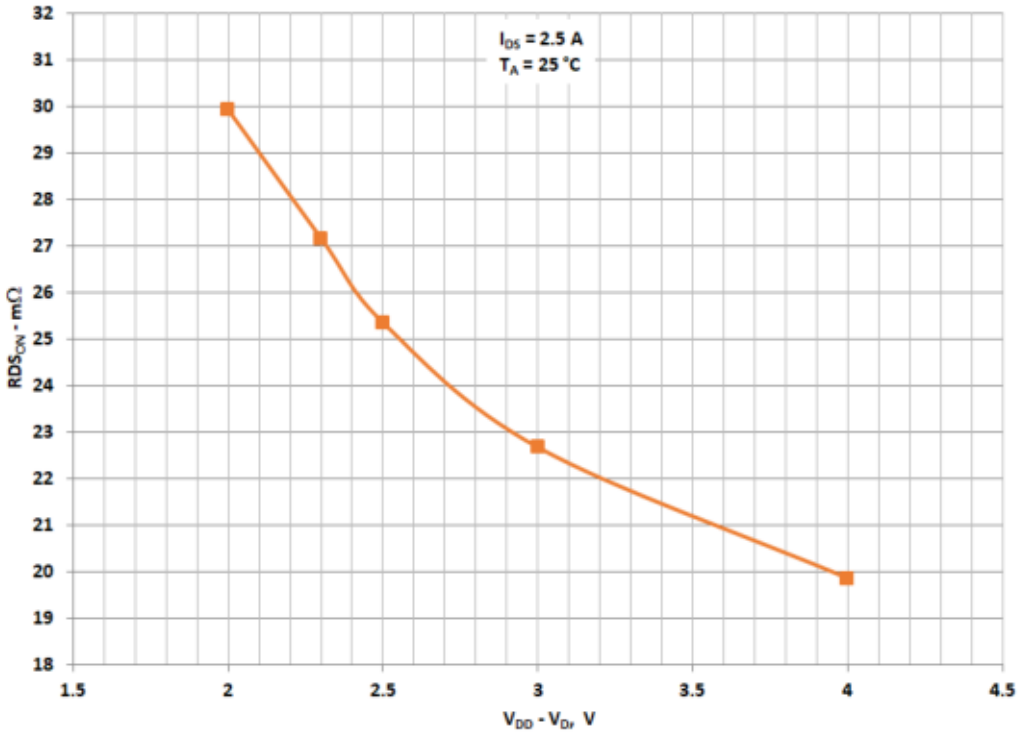
©2022 Renesas Electronics Corporation

Typical Performance Characteristics

RDS_{ON} vs. Temperature and V_{DD} - V_D

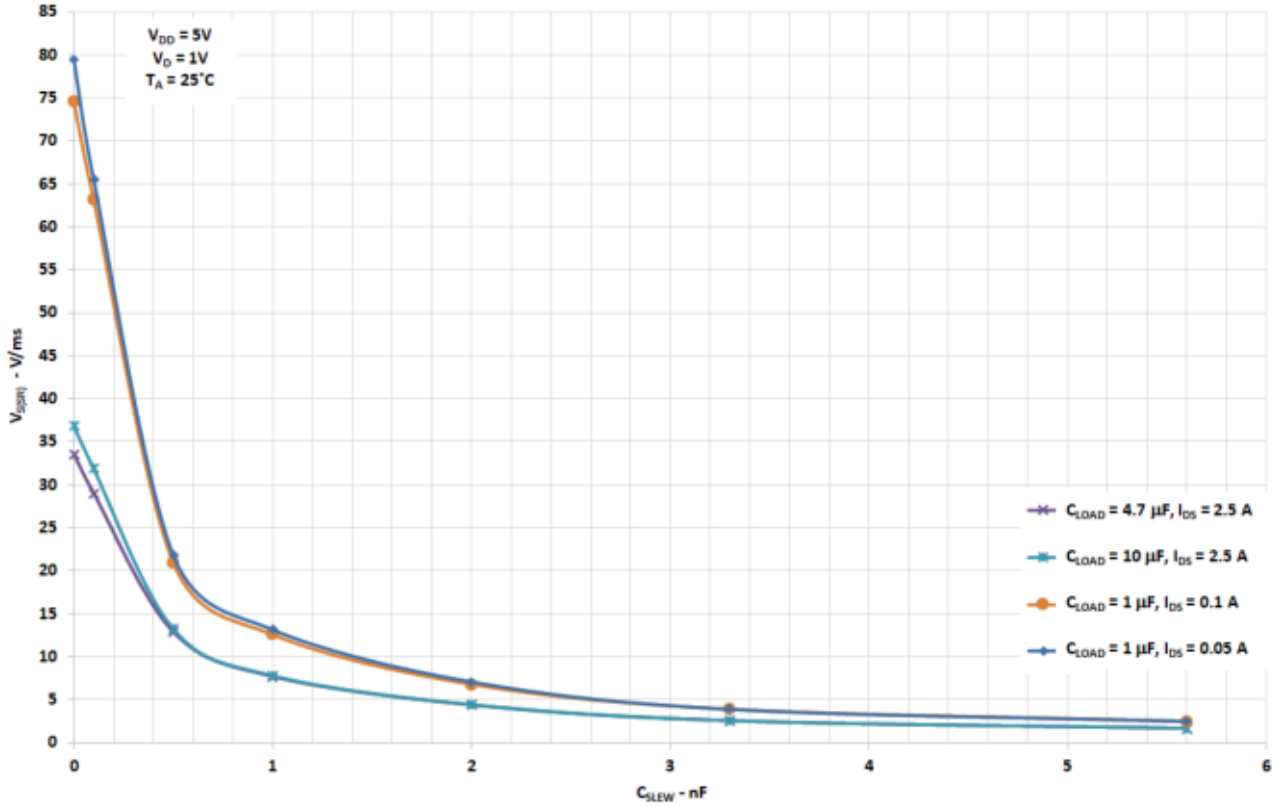


RDS_{ON} vs. V_{DD} - V_D

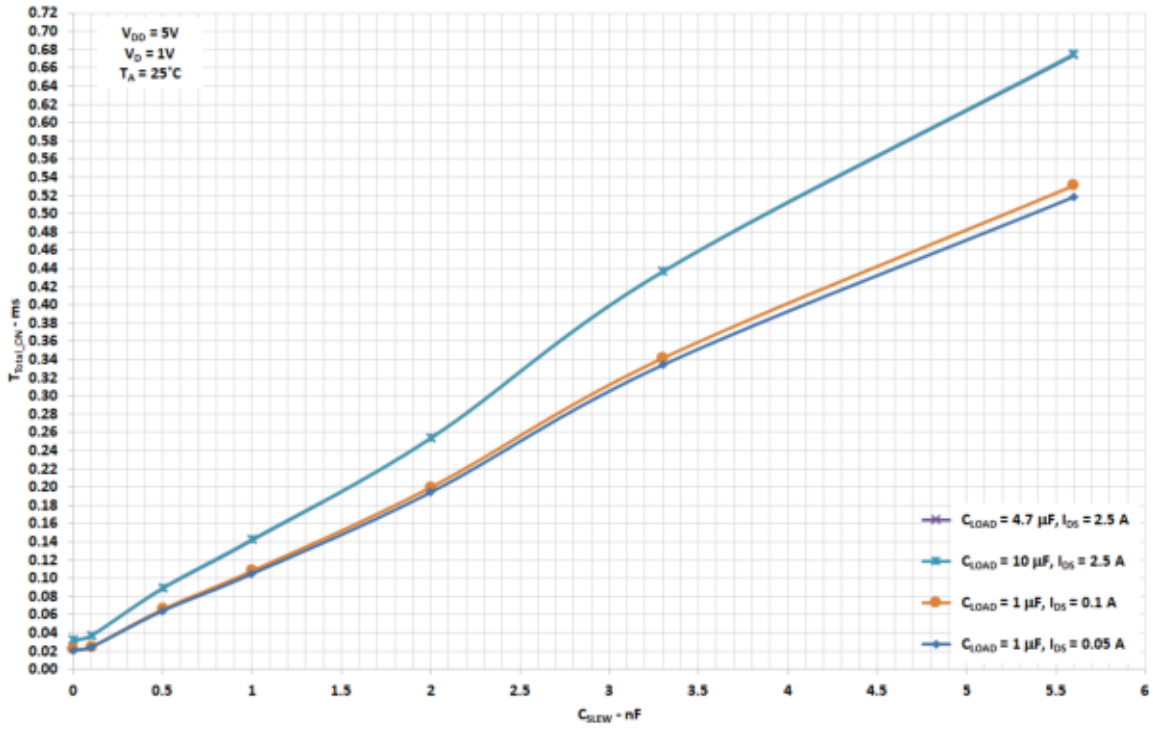


©2022 Renesas Electronics Corporation

V_S Slew Rate vs. C_{SLEW}



T_{Total_ON} vs. C_{SLEW}



©2022 Renesas Electronics Corporation

SLG5NT1533V Power-Up/Power-Down Sequence Considerations

A nominal power-up sequence is to apply V_{DD} first, followed by V_D only after V_{DD} is > 90 % of final V_{DD}, and finally toggling the ON pin LOW-to-HIGH after V_D is at least 90% of its final value.

A nominal power-down sequence is the power-up sequence in reverse order.

If V_{DD} and V_D are applied at the same time, a voltage glitch may appear on the output pin at V_S. To prevent glitches at the output, it is recommended to connect at least a 1 µF capacitor from the S pin to GND and to keep the V_{DD} and V_D ramp times higher than 2 ms.

If the ON pin is toggled HIGH before V_{DD} and V_D have reached their steady-state values the load switch timing parameters may differ from datasheet specifications.

Power Dissipation

The junction temperature of the SLG5NT1533V depends on different factors such as board layout, ambient temperature, and other environmental factors. The primary contributor to the increase in the junction temperature of the SLG5NT1533V is the power dissipation of its power MOSFET. Its power dissipation and the junction temperature in nominal operating mode can be calculated using the following equations:

$$PD = (RDS_{ON} \times I_{DS}^2) + (V_{DD} \times I_{DD})$$

where:
PD = Power dissipation, in Watts (W)
RDS_{ON} = Power MOSFET ON resistance, in Ohms (Ω)
I_{DS} = Output current, in Amps (A)
V_{DD} = Power supply voltage applied to the SLG5NT1533V, in Volts (V)
I_{DD} = Power supply current of the SLG5NT1533V at V_{DD}, in Amps (A)

and

$$T_J = PD \times \theta_{JA} + T_A$$

where:
T_J = Junction temperature, in Celsius degrees (°C)
θ_{JA} = Package thermal resistance, in Celsius degrees per Watt (°C/W) = 75 °C/W for the SLG5NT1533V's STDFN package.
T_A = Ambient temperature, in Celsius degrees (°C)

For more information on GreenFET load switch features, please visit our website and see App Note "AN-1068 GreenFET and High Voltage GreenFET Load Switch Basics".

©2022 Renesas Electronics Corporation

Layout Guidelines:

1. The VDD pin needs a 0.1µF (or larger) external capacitor to smooth pulses from the power supply. Locate this capacitor as close as possible to the SLG5NT1533V's pin 1.

2. Since the D and S pins dissipate most of the heat generated during high-load current operation, it is highly recommended to make power traces as short, direct, and wide as possible. A good practice is to make power traces with absolute minimum widths of 15 mils (0.381 mm) per Ampere. A representative layout, shown in Figure 1, illustrates proper techniques for heat to transfer as efficiently as possible out of the device;

3. To minimize the effects of parasitic trace inductance on normal operation, it is recommended to connect input C_{IN} and output C_{LOAD} low-ESR capacitors as close as possible to the SLG5NT1533V's D and S pins;

4. The GND pin should be connected to system analog or power ground plane.

5. 2 oz. copper is recommended for high current operation.

SLG5NT1533V Evaluation Board:

A GFET3 Evaluation Board for SLG5NT1533V is designed according to the statements above and is illustrated on Figure 1. Please note that evaluation board has D_Sense and S_Sense pads. They cannot carry high currents and dedicated only for RDS_{ON} evaluation.

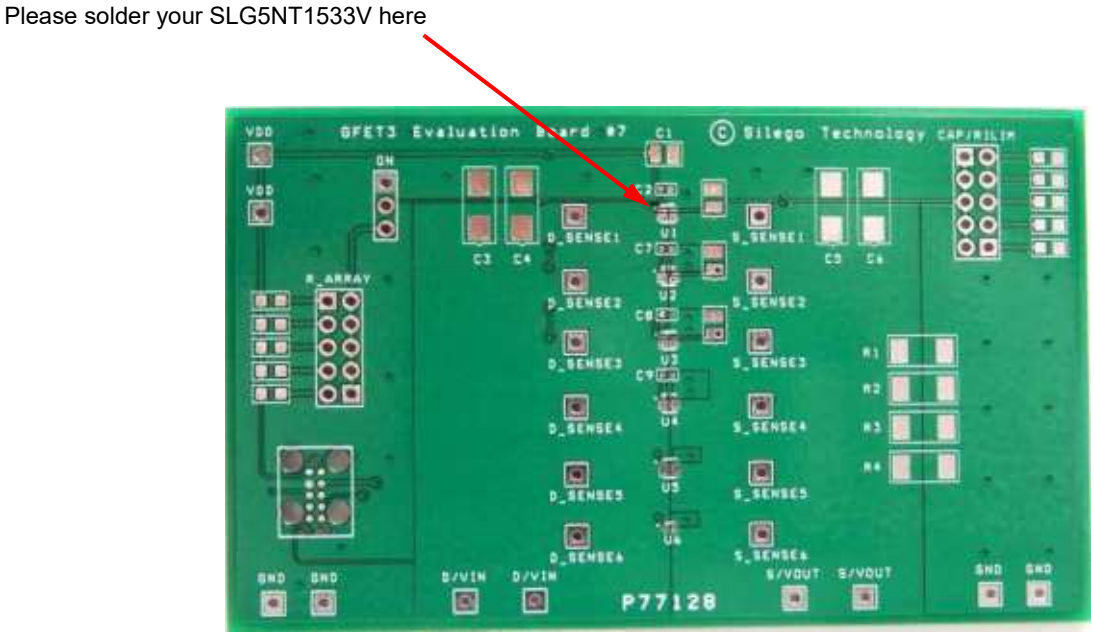


Figure 1. SLG5NT1533V Evaluation Board

©2022 Renesas Electronics Corporation

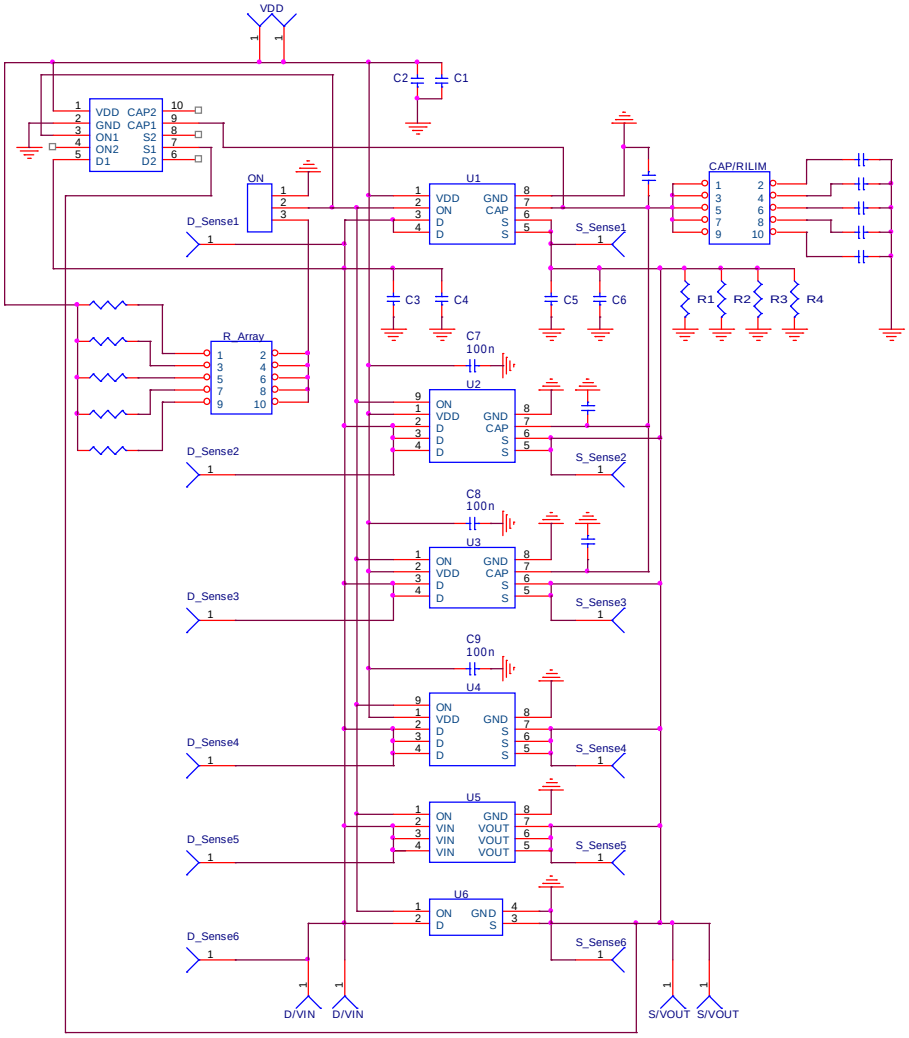


Figure 2. SLG5NT1533V Evaluation Board Connection Circuit

©2022 Renesas Electronics Corporation

Basic Test Setup and Connections

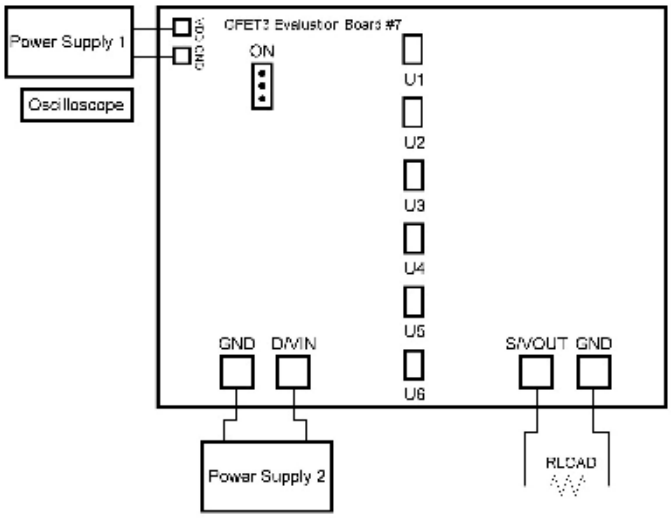


Figure 3. SLG5NT1533V Evaluation Board Connection Circuit

EVB Configuration

1. Connect oscilloscope probes to D/VIN, S/VOUT, ON, etc.;

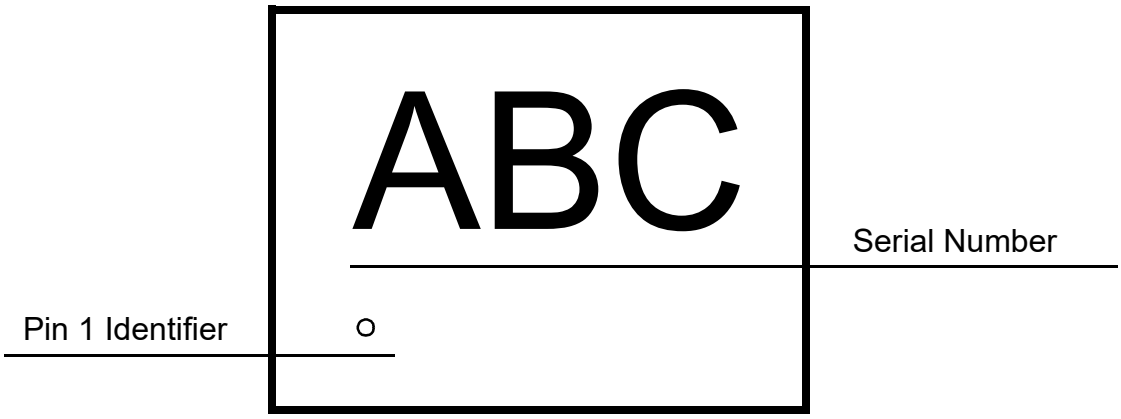
2. Turn on Power Supply 1 and set desired V_{DD} from 2.5 V…5.5 V range;

3. Turn on Power Supply 2 and set desired V_D from 0.85 V…V_{DD} - 1.5 V range;

4 .Toggle the ON signal High or Low to observe SLG5NT1533V operation.

©2022 Renesas Electronics Corporation

Package Top Marking System Definition

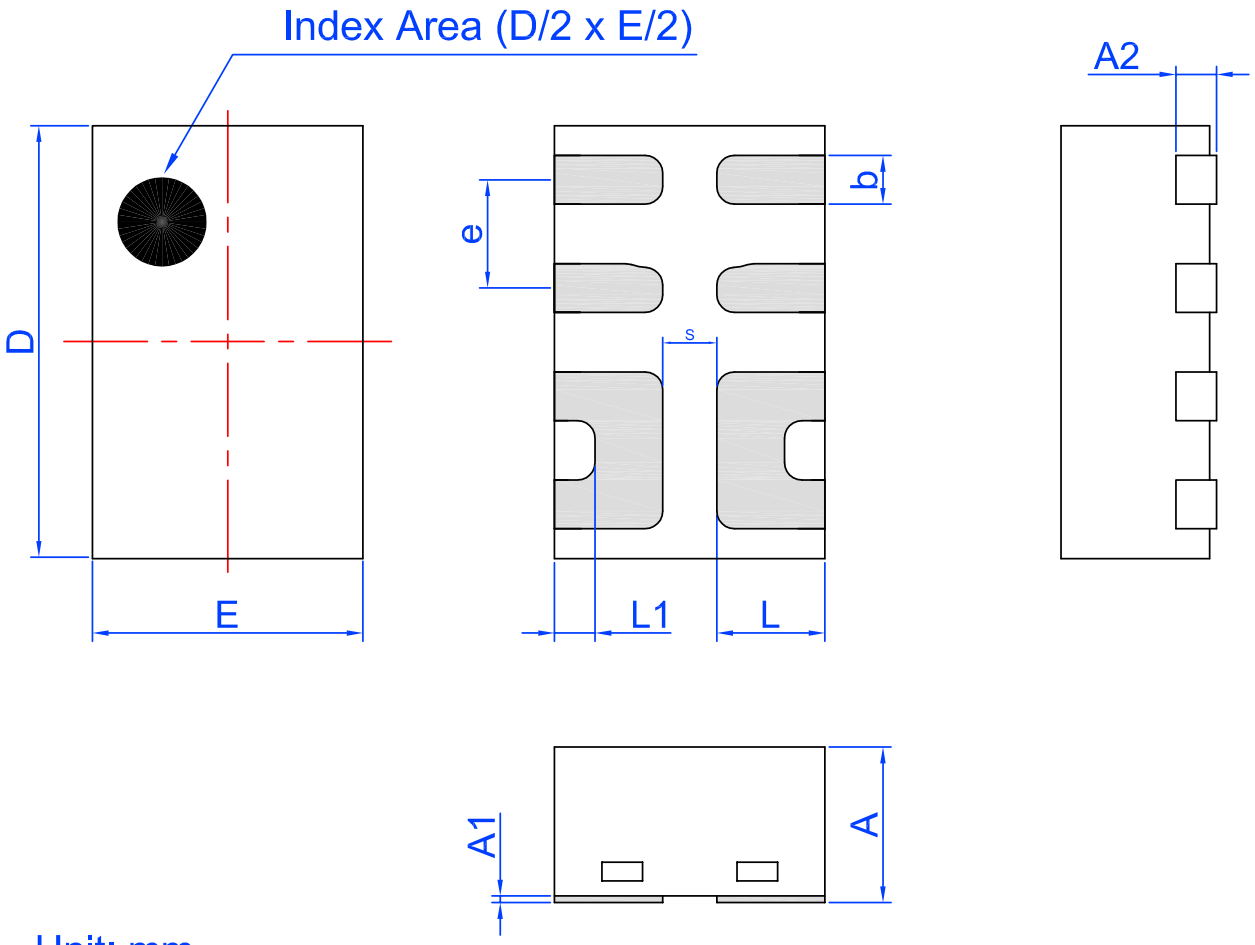


Each character in Serial Number field can be alphanumeric A-Z

©2022 Renesas Electronics Corporation

Package Drawing and Dimensions

8 Lead STDFN Package 1.0 x 1.6 mm (Fused Lead)



Unit: mm

Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	1.55	1.60	1.65
A1	0.005	-	0.060	E	0.95	1.00	1.05
A2	0.10	0.15	0.20	L	0.35	0.40	0.45
b	0.13	0.18	0.23	L1	0.10	0.15	0.20
e	0.40 BSC			S	0.2 REF		

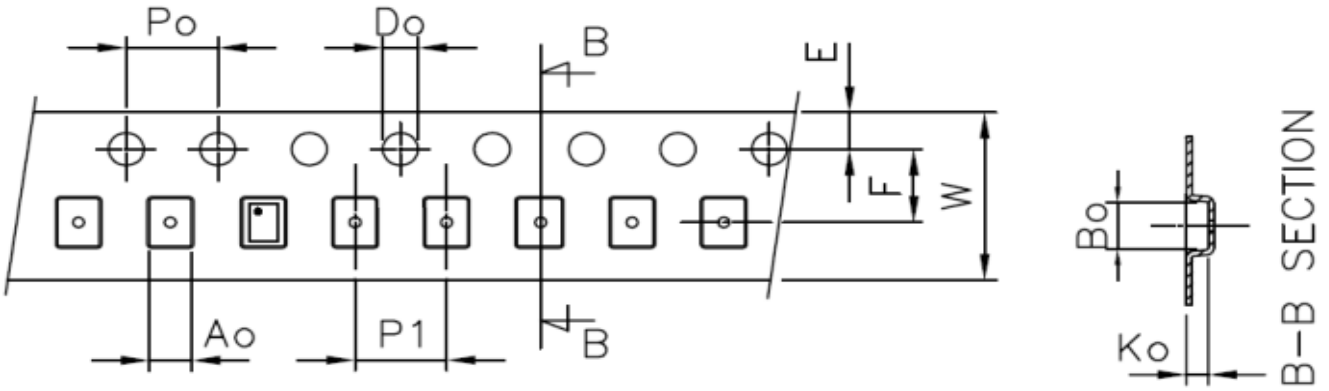
©2022 Renesas Electronics Corporation

Tape and Reel Specifications

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
STDFN 8L 1x1.6mm 0.4P FC Green	8	1.0 x 1.6 x 0.55	3,000	3,000	178 / 60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
STDFN 8L 1x1.6mm 0.4P FC Green	1.12	1.72	0.7	4	4	1.55	1.75	3.5	8



Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 0.88 mm^3 (nominal). More information can be found at www.jedec.org.

©2022 Renesas Electronics Corporation

Revision History

Date	Version	Change
2/3/2022	1.07	Updated Company name and logo Fixed typos
11/26/2018	1.06	Added Junction Temperature to Abs Max Table
11/8/2018	1.05	Updated Style and formatting Updated Abs, Max and Electrical Characteristics tables Added Applications information Added Layout Guidelines
8/14/2015	1.04	Add support for 0.85 VD
4/22/2015	1.03	Removed TBD from Timing Diagram
4/20/2015	1.02	Fixed Block Diagram (added Discharge Resistor)
9/15/2014	1.01	Added MSL
6/16/2014	1.0	Production release

©2022 Renesas Electronics Corporation

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

© 2026 Renesas Electronics Corporation. All rights reserved.