MPQ20056

Low-Noise, High-PSRR, 250mA Linear Regulator AEC-Q100 Qualified

DESCRIPTION

The MPQ20056 is a low-dropout linear regulator that supplies up to 250mA current with a 100mV dropout voltage and can operate from 2.5V to 5.5V input. The output voltage is preset at 1.8V, 2.5V,3.3V or adjustable for the two different packages. An external resistor divider can adjust the output voltage from 0.8V to 5V.

An internal PMOS pass element allows for a low 150µA ground current, making the MPQ20056 suitable for battery-powered devices. Other features include low-power shutdown, short-circuit protection, and thermal protection. The MPQ20056 is available in a 2mm×2mm 8-pin QFN and a 5-pin TSOT23-5 packages.

FEATURES

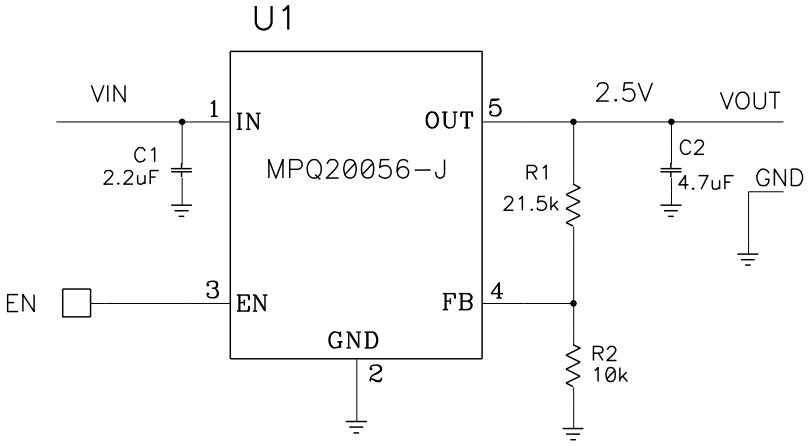
- Guaranteed Industrial/Automotive Temp. Range Limits
- Up to 250mA Output Current
- Low 100mV Dropout at 250mA
- Low 150µA Ground Current
- Low Noise: 13µV_{RMS} typical (10Hz to 100kHz)
- 63dB PSRR @1kHz
- Stable with Ceramic Capacitor
- Excellent Load/Line Transient Response
- Current Limiting and Thermal Protection
- Fixed output voltage 1.8V, 2.5V, 2.9V, and 3.3V
- Adjustable Output Voltage from 0.8V to 5V Using an External Resistor Divider
- Available in AEC-Q100 Qualified Grade

APPLICATIONS

- Notebook Computers
- Cordless Phones
- Cellular Phones
- Wireless Communication Equipment
- Hand-Held Instruments

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TYPICAL APPLICATION



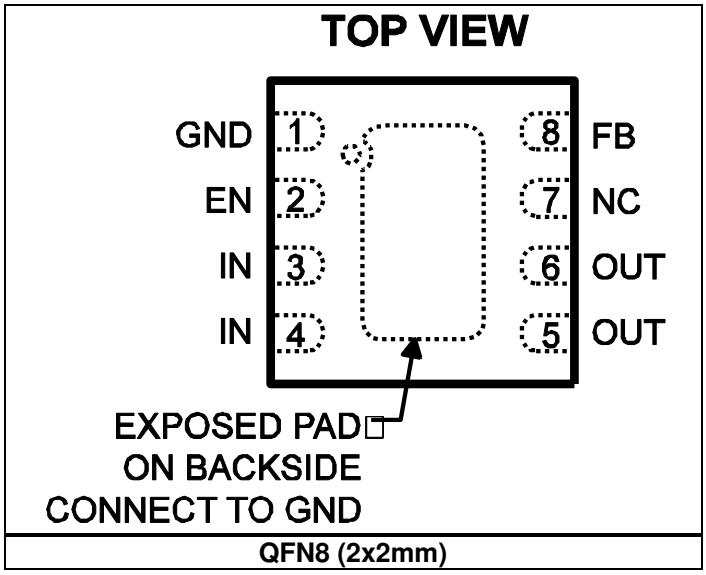
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ORDERING INFORMATION

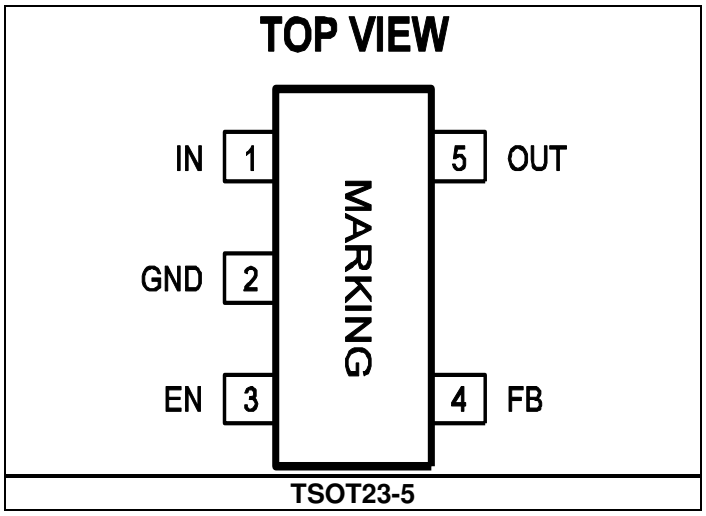
Part Number*	Package	Top Marking
MPQ20056GG-18	QFN8(2x2mm)	BK
MPQ20056GG-18-AEC1	QFN8(2x2mm)	BK
MPQ20056GJ-25	TSOT23-5	ALA
MPQ20056GJ-25-AEC1	TSOT23-5	ALA
MPQ20056GJ-33	TSOT23-5	AFT
MPQ20056GJ-33-AEC1	TSOT23-5	AFT
MPQ20056GG-33	QFN8(2x2mm)	BV
MPQ20056GG-33-AEC1	QFN8(2x2mm)	BV
MPQ20056GJ	TSOT23-5	AWZ
MPQ20056GJ-AEC1	TSOT23-5	AWZ
MPQ20056GJ-18-AEC1	TSOT23-5	AWZ
MPQ20056GJ-29-AEC1	TSOT23-5	AWZ

* For Tape & Reel, add suffix -Z (e.g. MPQ20056GG-18-Z).

PACKAGE REFERENCE



QFN8 (2x2mm)



TSOT23-5

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ABSOLUTE MAXIMUM RATINGS (1)

VIN, EN, FB to GND .....-0.3V to +6V
OUT to GND ..... -0.5V to (V_{IN} + 0.5V)
Continuous Power Dissipation .....(T_A=25°C) (2)
QFN8 (2x2mm).....1.6W
TSOT23-5 ..... 0.57W
Junction Temperature……..150°C
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (Soldering, 10sec).....260°C

ESD SUSCEPTIBILITY(3)

HBM (Human Body Mode)..... 2kV
MM (Machine Mode) 200V

Recommended Operating Conditions (4)

Supply Input Voltage.....2.5V to 5.5V
Enable Input Voltage .....0V to 5.5V
Operating Junction Temp. (T_J). -40°C to +125°C

Thermal Resistance (5) θ_{JA} θ_{JC}

QFN8 (2x2mm) .....80 ..... 16 ... °C/W
TSOT23-5 .....220 .... 110 .. °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the device will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Devices are ESD sensitive. Handling precaution recommended.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN}=V_{OUT}+0.5V or V_{IN}=2.5V, EN=V_{IN}, V_{OUT} =1.8V or 3.3V. T_J=-40ºC to +125ºC, Typical values are at T_j=25°C, unless otherwise specified.

Parameter	Condition		Min	Typ	Max	Units
Input Voltage			2.5		5.5	V
Input Under-Voltage Lockout	V_{IN} rising, V_{OUT}=1.8V		1.95		2.3	V
Hysteresis of UVLO				160		mV
FB Voltage	V_{OUT}=0.8V, I_{OUT}=1mA, T_J=25°C		0.784	0.8	0.816	V
	V_{OUT}=0.8V, I_{OUT}=1mA, -40°C≤T_J≤+125°C		0.776		0.824	V
Output Voltage Accuracy	I_{OUT}=1mA, T_J=25°C		-2		2	%
	I_{OUT}=1mA, -40°C≤T_J≤125°C		-3		3	
Maximum Output Current	Continuous		250			mA
Short-Circuit Current Limit	V_{OUT}=0, V_{IN}≥2.5V		350	550	850	mA
In-Regulation Current Limit	V_{OUT} within 4% of normal output voltage V_{IN}=5.5V		300	550	800	mA
Ground Current	I_{OUT}=0.1mA			150	250	µA
	I_{OUT}=250mA			220	330	
Dropout Voltage[6]	I_{OUT}=250mA, V_{OUT}=3.3V,	T_J=25°C		100	150	mV
		-40°C≤T_J≤125°C		100	200	
Line Regulation[7]	V_{IN} from V_{OUT}+0.5V or 2.5V to 5.5V, I_{OUT}=100mA,		-0.15		0.15	%/V
Load Regulation@Vtyp[8]	I_{OUT} from 100mA to 250mA	V_{OUT}=3.3V	-0.3		0.3	%
		V_{OUT}=2.5V	-0.4		0.4	
		Vout=1.8V(QFN8)	-0.3		0.3	
		Vout=1.8V(TSOT23-5)	-0.4		0.4	
Output-Voltage Noise[9]	I_{OUT}=100mA, f ranges from 10Hz to 100kHz	V_{OUT}=1.8V		20		μV_{RMS}
		V_{OUT}=3.3V		35		
PSRR[9]	V_{OUT} = 1.8V, 2.5V, 3.3V I_{OUT} = 250mA	f=100Hz		65		dB
		f=1kHz		63		
		f=10kHz		63		
		f=1MHz		33		
Shutdown Supply Current	V_{IN}=+5.5V	T_J=25°C		0.1	0.3	µA
		-40°C≤T_J≤125°C		10	30	
EN Pin Current , Enabled	V_{IN}=V_{EN}=+5.5V			0.1	0.3	µA
Startup Time	C_{OUT}=4.7µF, V_{OUT}=10% to 90%$V_{OUT(NOM)}$	V_{OUT}=1.8V	100		300	µs
		V_{OUT}=3.3V, 2.5V	100		450	
EN PIN Threshold	EN Logic High		1.5			V
	EN Logic Low				0.4	
Thermal Shutdown[9]				150		°C
Thermal Shutdown Hysteresis[9]				20		°C

Notes:

6) Dropout Voltage is defined as the input to output differential when the output voltage drops 100mV below its nominal value.

7) Line Regulation= $\frac{\left|V_{OUT[V_{IN(MAX)}]} - V_{OUT[V_{IN(MIN)}]}\right|}{\left[V_{IN(MAX)} - V_{IN(MIN)}\right] \times V_{OUT(NOM)}} \times (\% / V)$

8) Load Regulation= $\frac{\left|V_{OUT[I_{OUT(MAX)}]} - V_{OUT[I_{OUT(MIN)}]}\right|}{V_{OUT(NOM)}} \times (\%)$

9) Design guarantee, no test in production

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PIN FUNCTIONS

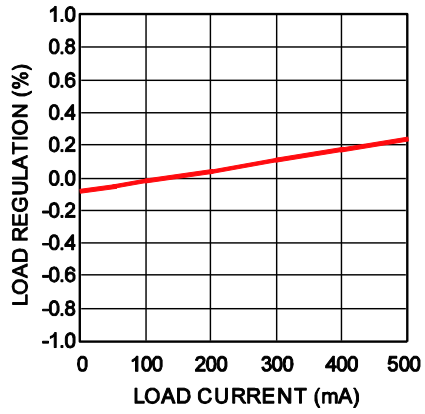
Pin # QFN8 (2x2mm)	Pin # TSOT23-5	Name	Pin Function
1, Exposed Pad	2	GND	Ground. Connect exposed pad to GND plane for optimal thermal performance.
2	3	EN	Regulator Enable Control Input. Drive EN above 1.5V to turn on the MPQ20056. Drive EN below 0.4V to turn it off. Do not float the EN pin.
3, 4	1	IN	Regulator Input. Supply voltage ranges from 2.5V to 5.5V. Bypass with a 2.2µF capacitor. These pins must be externally connected for proper operation even if they are internally connected.
5, 6	5	OUT	Regulator Output. Bypass with a standard 4.7µF ceramic capacitor to GND. Connect all the pins together externally.
7		NC	No Connection. Leave this NC pin open.
8	4	FB	Feedback Input. Connect FB to the center point of the external resistor divider. The feedback threshold voltage is 0.8V.

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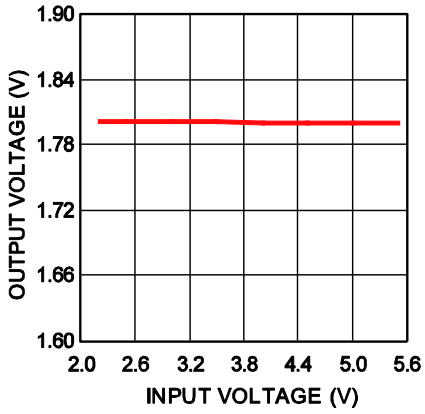
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN}=2.5V/3.7V, V_{OUT}=1.8V/3.3V, T_A=25ºC, unless otherwise noted.

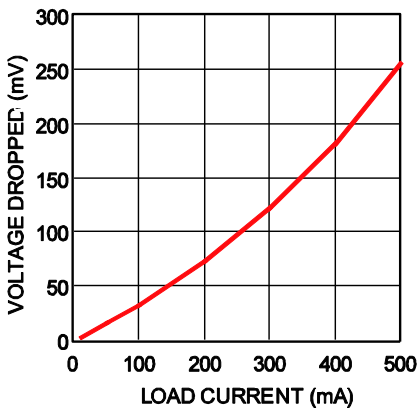
Load Regulation
V_{IN}=2.5V, V_{OUT}=1.8V



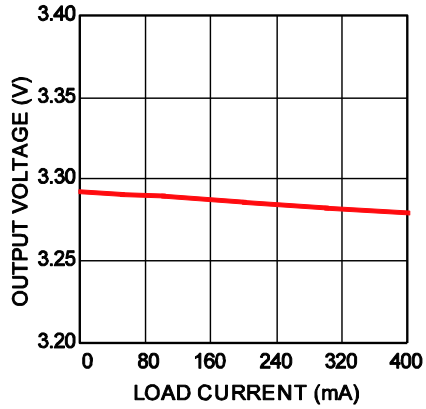
Line Regulation
I_{OUT}=50mA



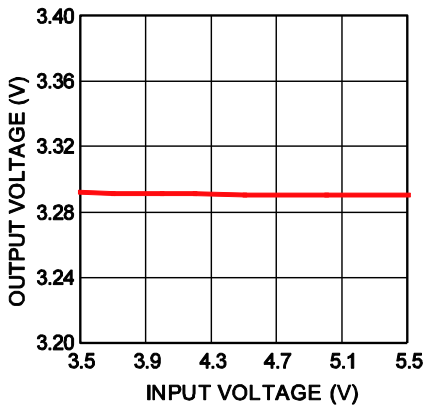
Voltage Dropped
V_{OUT}=3.3V



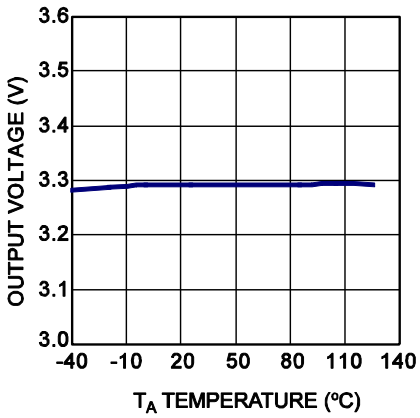
Load Regulation
V_{IN}=3.5V, V_{OUT}=3.3V



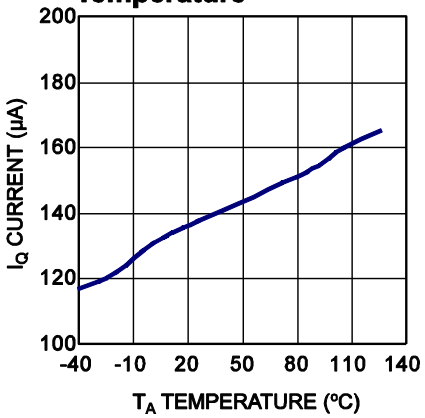
Line Regulation
I_{OUT}=50mA



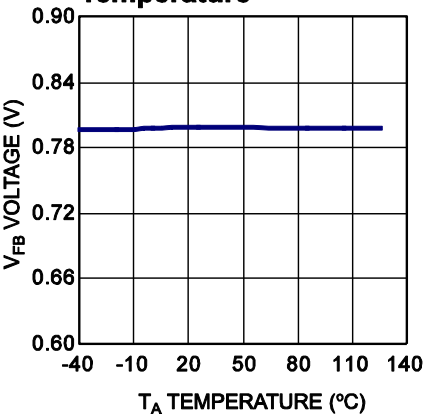
V_{OUT} vs. T_A



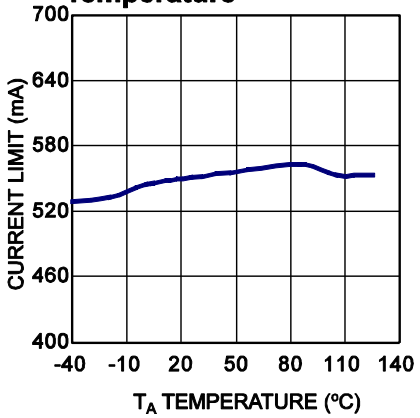
I_Q Current vs. Temperature



V_{FB} Voltage vs. Temperature



Current Limit vs. Temperature

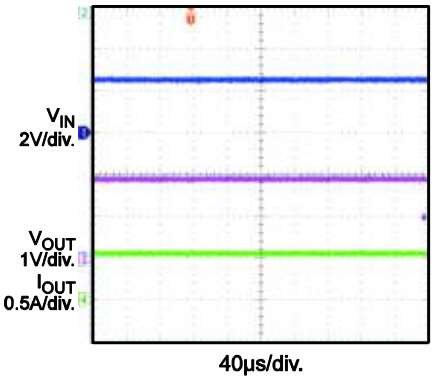


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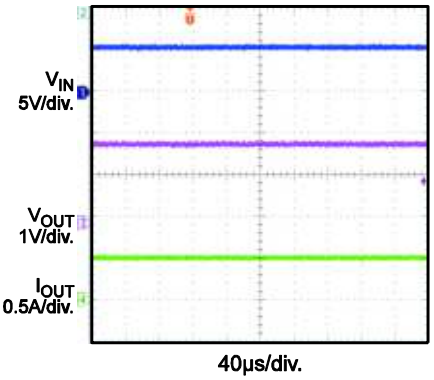
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN}=2.5V, V_{OUT}=1.8V, T_A=25ºC, unless otherwise noted.

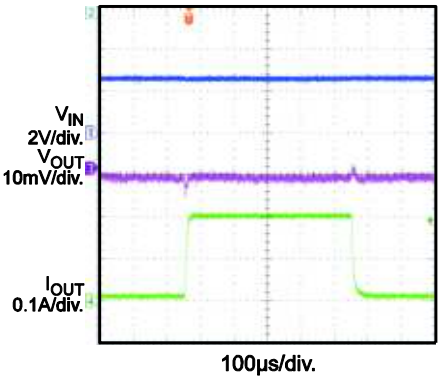
Steady State
I_{OUT} = 0.5A



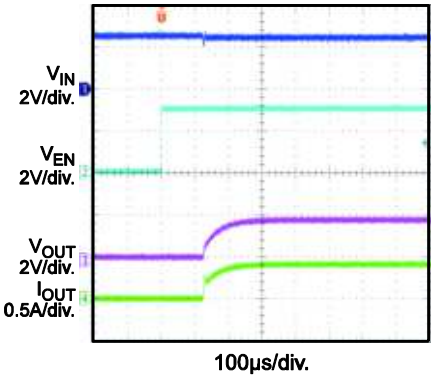
Steady State
V_{IN} = 5.5V, I_{OUT} = 0.5A



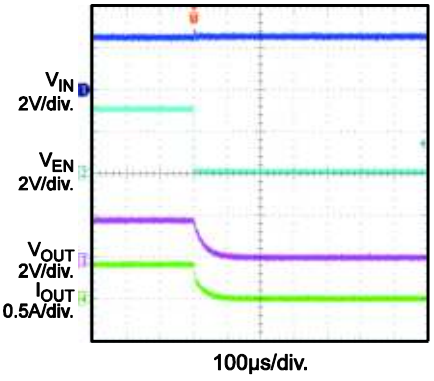
Load Transient
I_{OUT} = 10mA-0.2A



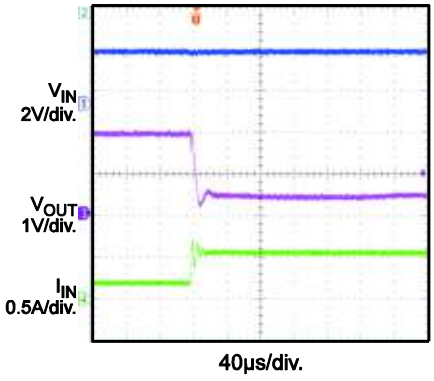
Enable On
I_{OUT} = 0.4A



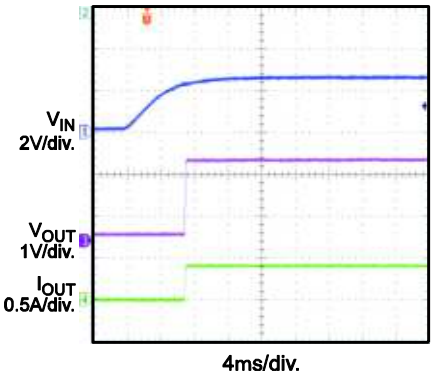
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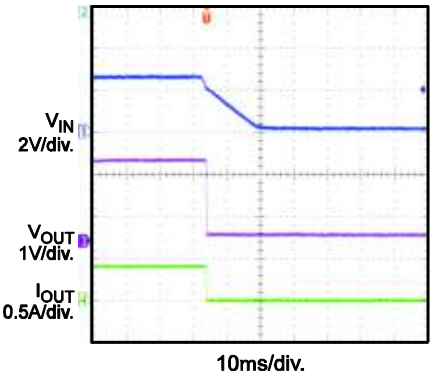
Short Output
I_{OUT} = 0.2A



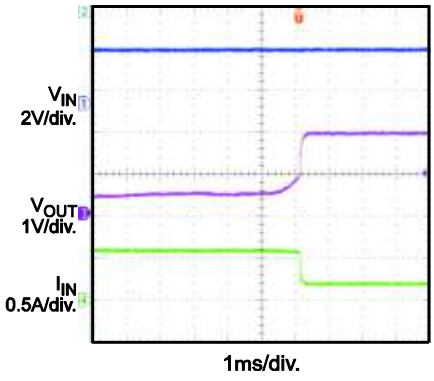
Power Ramp Up
I_{OUT} = 0.4A



Power Ramp Down
I_{OUT} = 0.4A



Short Output Recovery
I_{OUT} = 0.2A

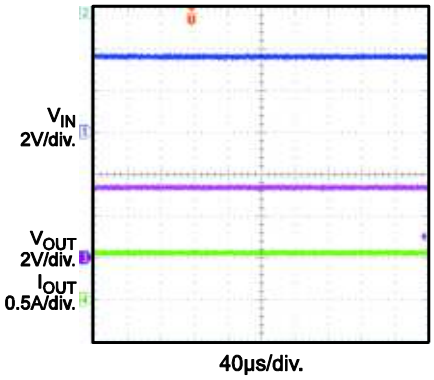


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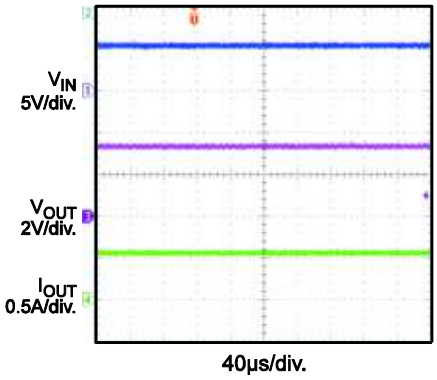
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN}=3.7V, V_{OUT}=3.3V, T_A=25ºC, unless otherwise noted.

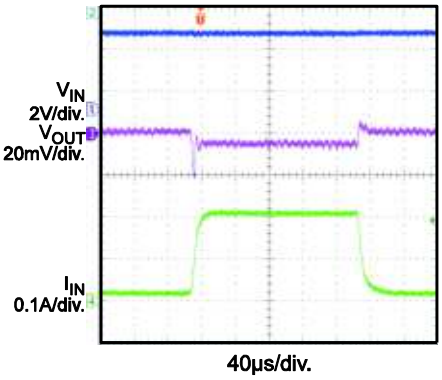
Steady State
I_{OUT} = 0.5A



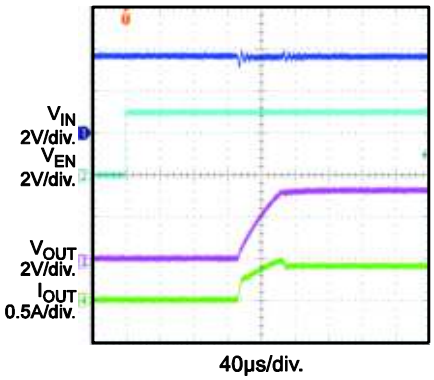
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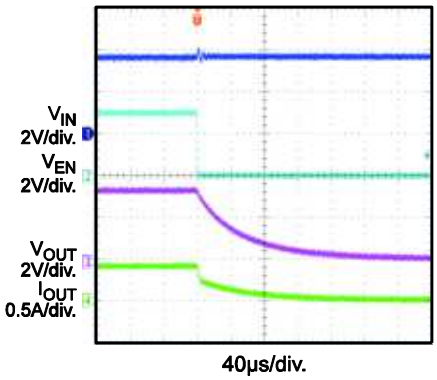
Load Transient
I_{OUT} = 50mA-0.2A



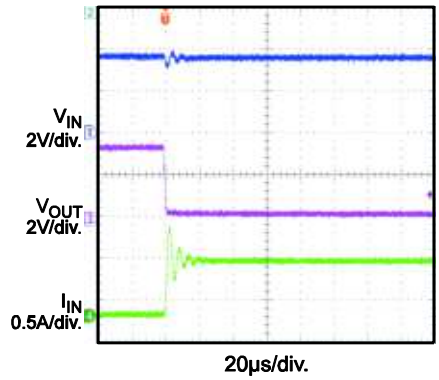
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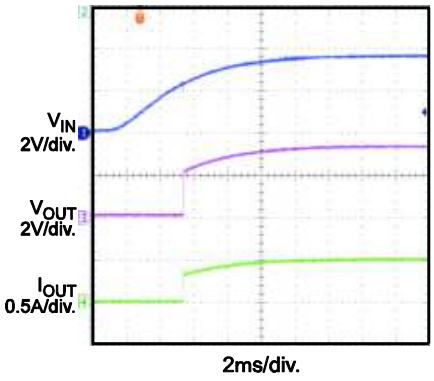
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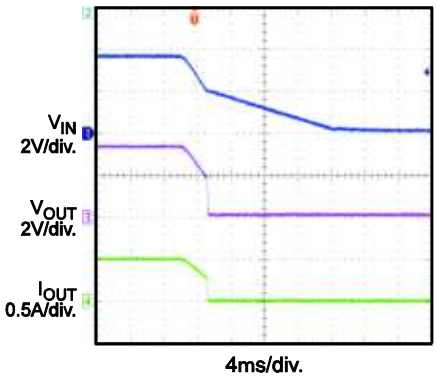
Short Output



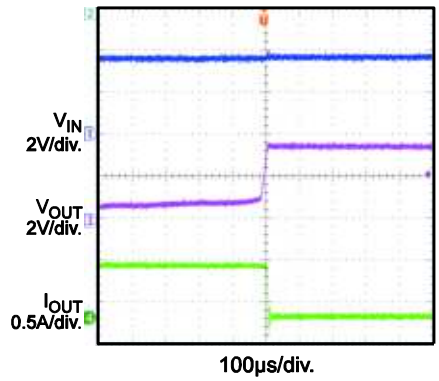
Power Ramp Up
I_{OUT} = 0.5A



Power Ramp Down
I_{OUT} = 0.5A



Short Output Recovery



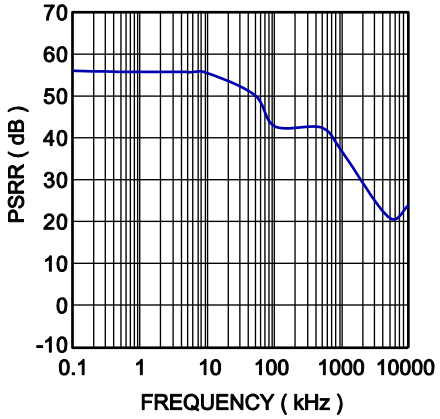
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

T_A=25ºC, unless otherwise noted.

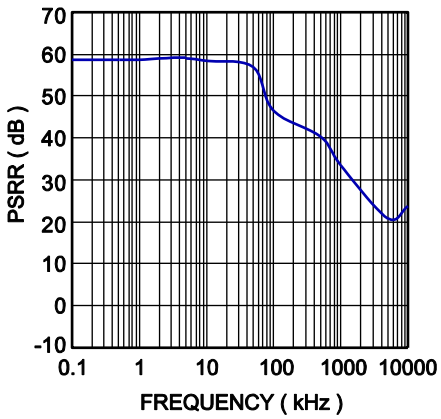
PSRR

V_{IN}=5V, V_{OUT}=2.9V, I_{OUT}=10mA



PSRR

V_{IN}=3.5V, V_{OUT}=1.8V, I_{OUT}=10mA



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FUNCTIONAL BLOCK DIAGRAM

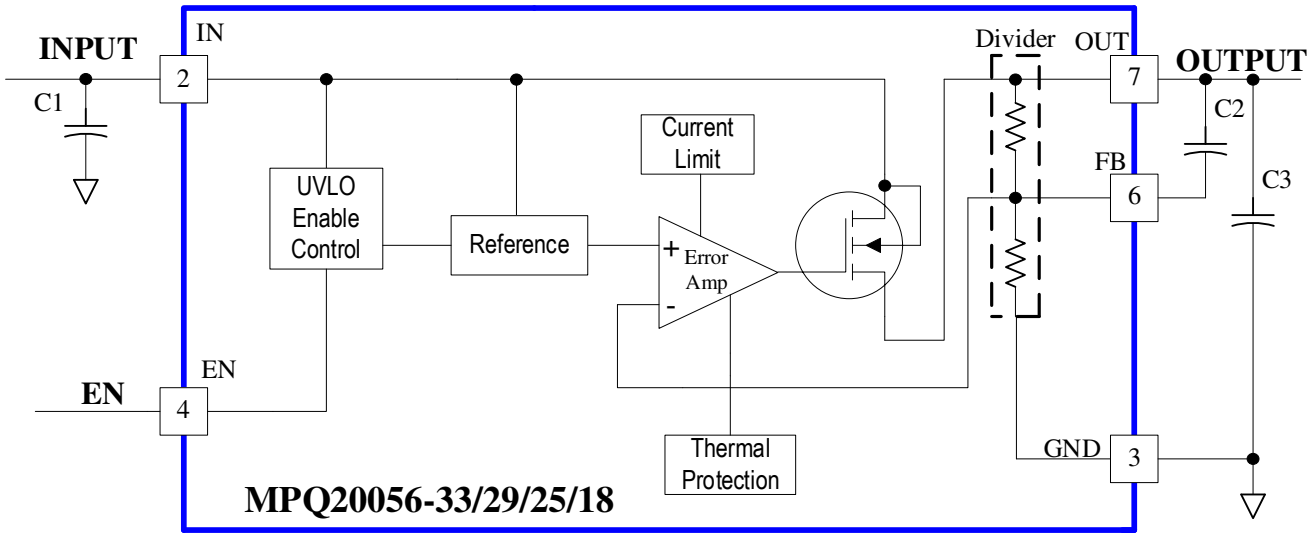


Figure 1: Fixed Output Functional Diagram

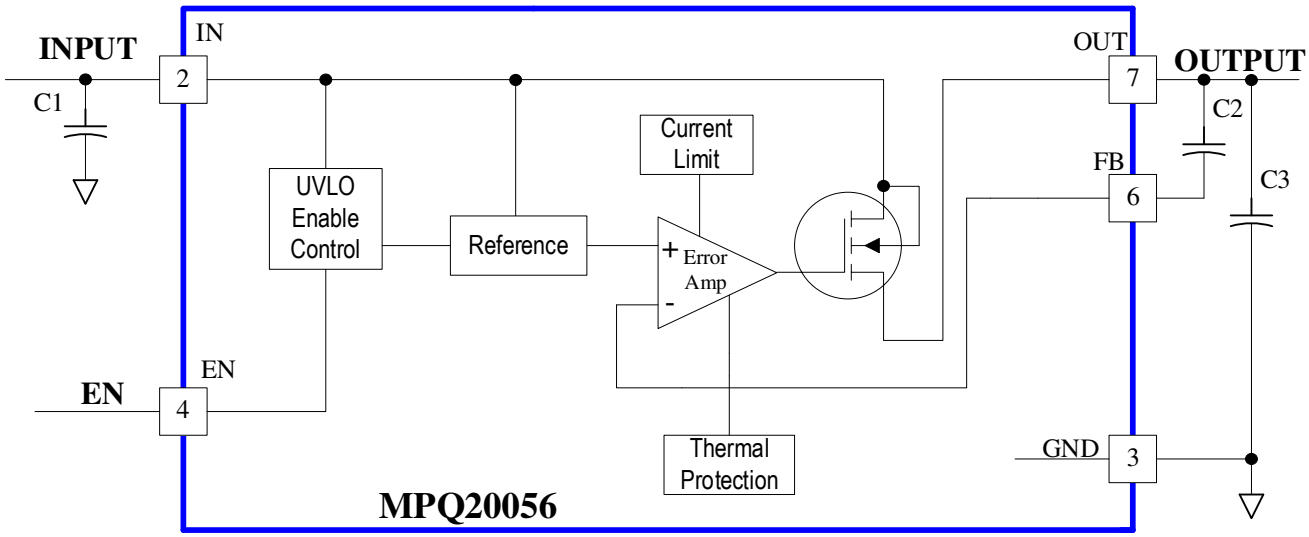


Figure 2: Adjustable Output Functional Block Diagram

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OPERATION

The MPQ20056 is a low-dropout linear regulator that can supply up to 250mA current, which makes it suitable for very low voltage, low quiescent, low noise, and high PSRR applications, such as wireless LAN transceivers, notebook computers, smartphones, and other low-power electronics.

The MPQ20056 uses an internal PMOS as the pass element and includes both thermal shutdown and an internal current-limiting circuit.

Dropout Voltage

Dropout voltage is the minimum input to output differential voltage required for the regulator to maintain an output voltage within 100mV of its nominal value. Because the PMOS pass element behaves as a low-value resistor.

Shutdown

The MPQ20056 can be switched ON or OFF by a logic input at the EN pin: Logic high turns the regulator on and logic low turns it off. Tie the EN pin to VIN if the application does not require the shutdown feature. Do not float the EN pin.

Current Limit

The MPQ20056 includes a current limit structure that monitors and controls the PMOS gate voltage to limit the guaranteed maximum output current to 0.4A.

Thermal Protection

Thermal protection turns off the PMOS when the junction temperature exceeds 150°C, allowing the IC to cool. When the IC's junction temperature drops by 20°C, the PMOS will turn on again. Thermal protection limits total power dissipation in the MPQ20056. For reliable operation, limit the junction temperature to a maximum of 125°C.

Load-Transient Considerations

The output response of the load-transient consists of a transient response and DC shift—the MPQ20056's excellent load regulation effectively limits the DC shift. The output voltage transient depends on the output capacitor's value and ESR. Increasing the capacitance and decreasing the ESR will improve the transient response.

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APPLICATION INFORMATION

Setting the Output Voltage

The output voltage of the MPQ20056 is preset to 1.8V, 2.5V, 2.9V, or 3.3V by internal resistor divider. The output voltage also can be adjusted by using an external resistor divider (R1 and R2 in Figure 3).

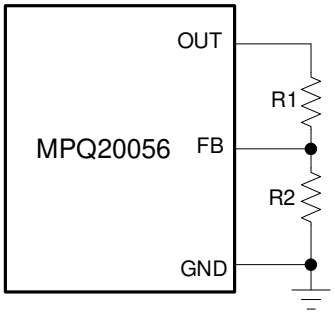


Figure 3: Setting the Output Voltage

However, the sum of R1 and R2 should not exceed 10kΩ to minimize their impact on the internal resistor divider. For an accurate output-voltage setting, use 1kΩ (±1%) for R2, and determine R1 with:

$$R1 = R2 \times \left(\frac{V_{OUT} - V_{FB}}{V_{FB}} \right)$$

For example, for a 1.1V output voltage, R2 is 1kΩ, and R1 is 374Ω. You can select a standard 374Ω (±1%) resistor for R1.

Power Dissipation

The power dissipation for any package depends on the thermal resistance of the case and circuit board, the temperature differential between the junction and ambient air, and the rate of air flow. The power dissipation across the device can be represented by the equation:

$$P = (V_{IN} - V_{OUT}) \times I_{OUT}$$

The allowable power dissipation can be calculated using the following equation:

$$P_{(MAX)} = (T_{Junction} - T_{Ambient}) / \theta_{JA}$$

Where ($T_{Junction}$ − $T_{Ambient}$) is the temperature differential between the junction and the surrounding environment, θ_{JA} is the thermal resistance from the junction to the ambient environment. Connecting the exposed GND pad to a large ground pad or plane helps to channel away heat.

Output Capacitor Selection

The MPQ20056 is specifically designed to work with a standard ceramic output capacitor to save space and improve performance. Use a 4.7µF ceramic capacitor for most applications. Larger output capacitors will improve load transient response and reduce noise at the cost of increased size.

External Reverse Voltage Protection

In some situations, e.g. a backup battery is connected as MPQ20056 load, the output voltage may be held up while the input is either pulled to ground to some intermediated voltage or is floating. Thus, the output voltage is higher than input voltage. Since MPQ20056 internal PMOS pass element has a body diode, a current will conduct from the output to input and is not internally limited. It's possible that the IC will be damaged by this unlimited reverse current. To avoid this, it's recommended to place an external diode at input like below.

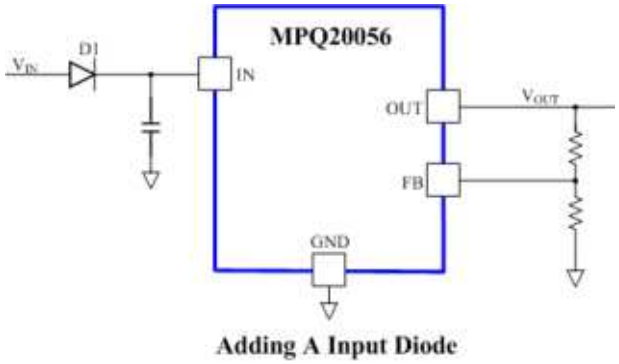


Figure 4: External Reverse Voltage Protection Reference Circuit

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TYPICAL APPLICATION CIRCUITS

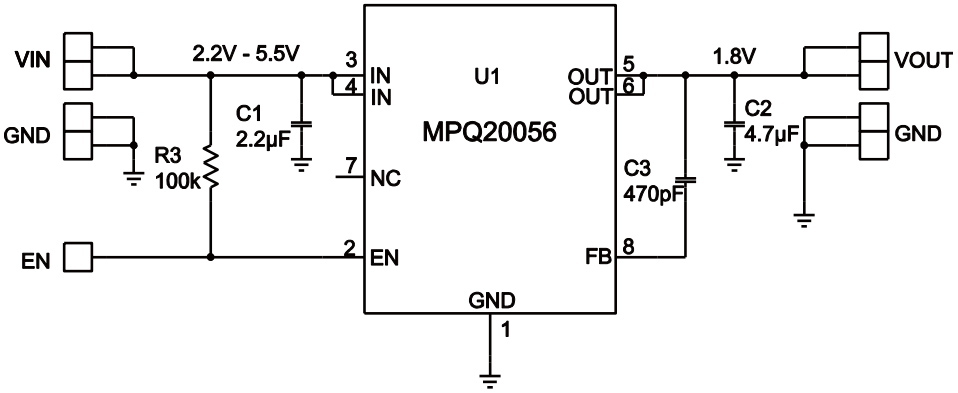


Figure 5: 1.8V Fixed-Output Application (QFN-8L)

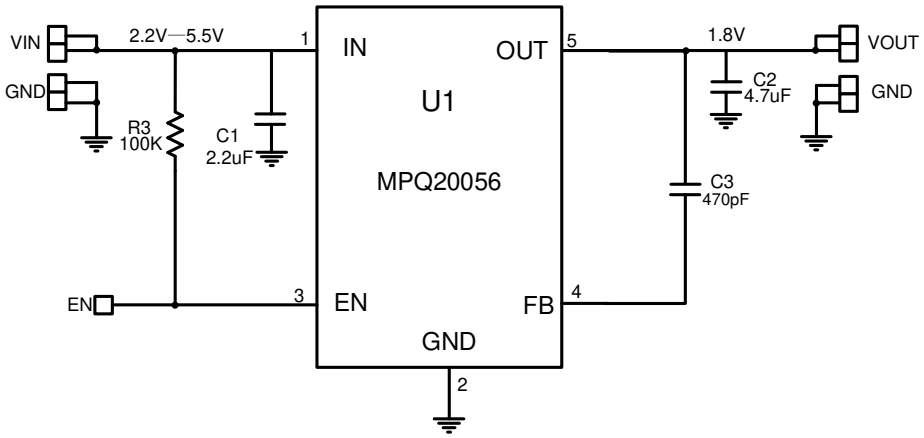


Figure 6: 1.8V Fixed-Output Application (TSOT23-5L)

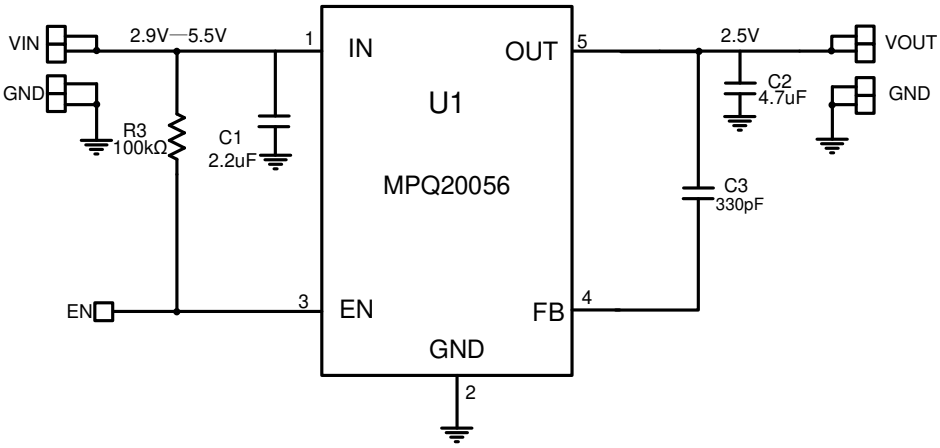


Figure 7: 2.5V Fixed-Output Application (TSOT23-5L)

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TYPICAL APPLICATION CIRCUITS *(continued)*

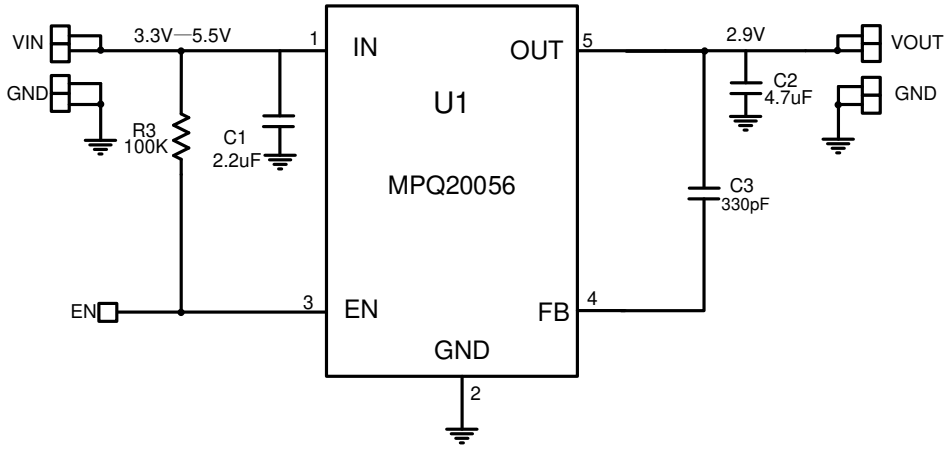


Figure 8: 2.9V Fixed-Output Application (TSOT23-5L)

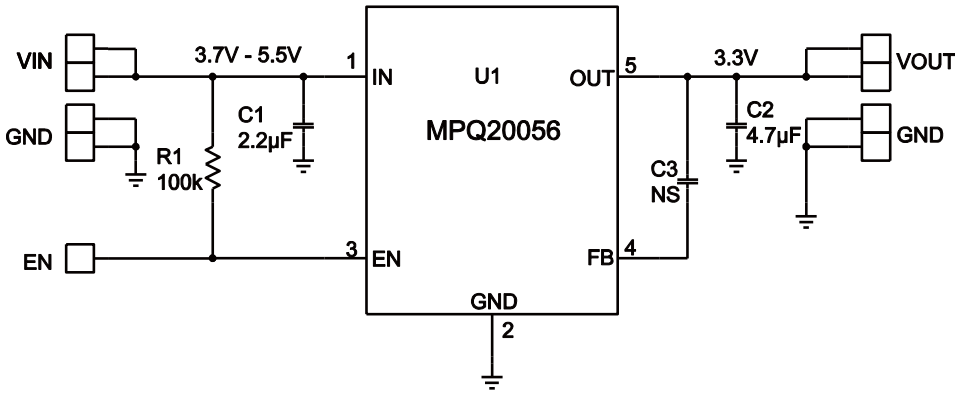


Figure9: 3.3V Fixed-Output Application (TSOT23-5L)

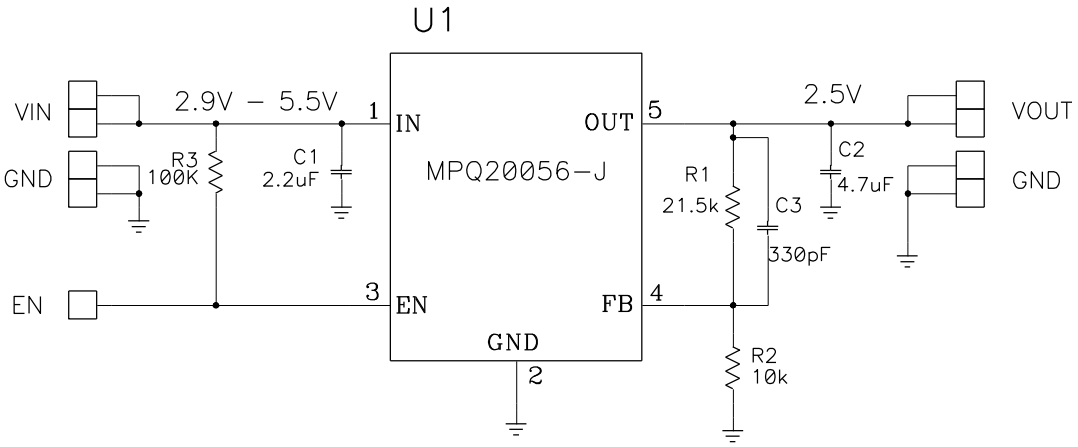
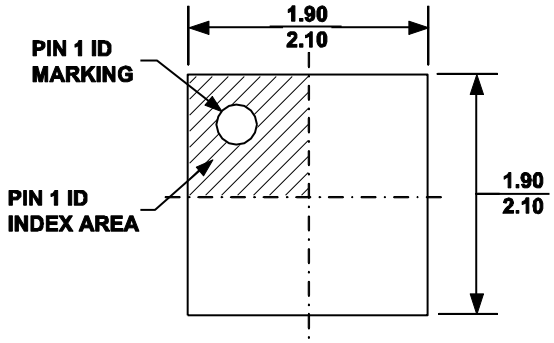


Figure 10: Adjustable-Output Application (TSOT23-5L)

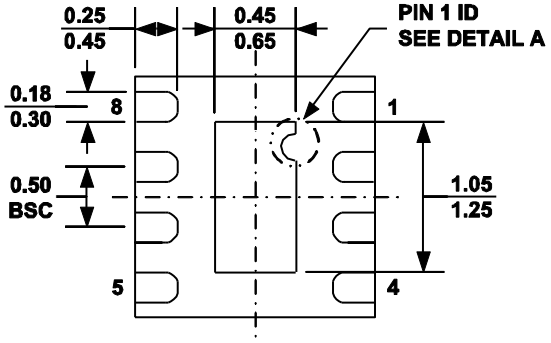
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PACKAGE INFORMATION

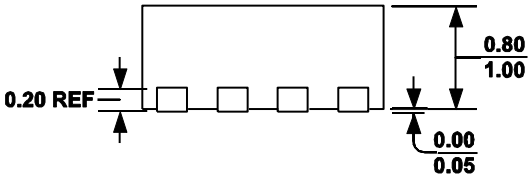
QFN8 (2×2mm)



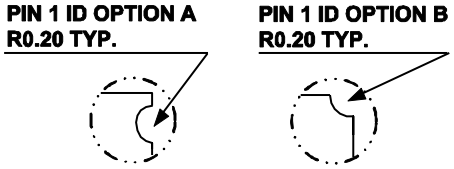
TOP VIEW



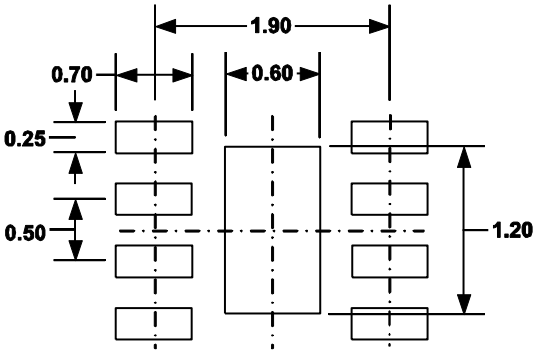
BOTTOM VIEW



SIDE VIEW



DETAIL A



RECOMMENDED LAND PATTERN

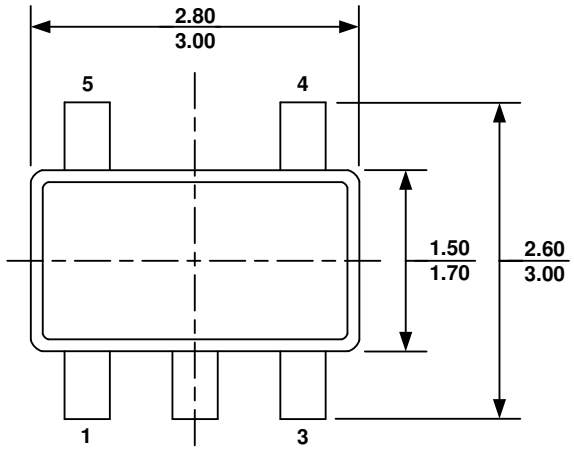
NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
4) DRAWING CONFORMS TO JEDEC MO-229, VARIATION VCCD-3.
5) DRAWING IS NOT TO SCALE.

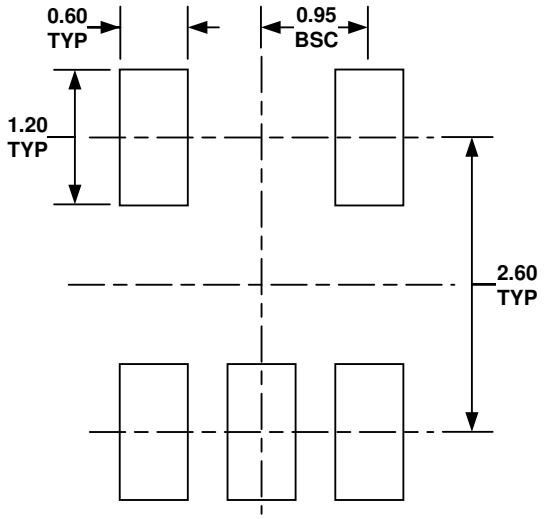
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PACKAGE INFORMATION

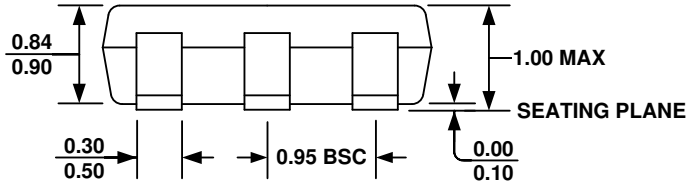
TSOT23-5



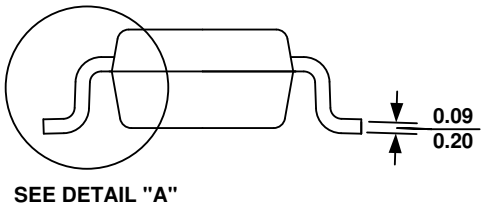
TOP VIEW



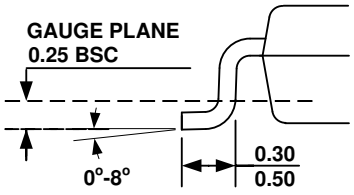
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-193, VARIATION AA.
6) DRAWING IS NOT TO SCALE.

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	9/13/2013	Final Release	-
1.01	2/24/2014	Added two PSRR curves.	9
1.02	7/3/2014	Added 2.5V output option.	1
1.1	4/8/2016	Updated the EC table: change Load regulation at Vout=5V from ±3% to ±4%.	4
1.11	6/28/2016	Added adjustable output version.	2
1.12	4/12/2018	Updated the PSRR curves.	9
1.13	10/16/2018	Added “External Reverse Voltage Protection” section.	12
1.2	9/10/2024	• Added the MPQ20056GJ-18-AEC1 SKU to the Ordering Information section. • Updated the package name from FN8 to QFN8 and made minor formatting edits in the Package Reference section.	2
		Divided the Load Regulation@Vtyp parameter at V_{OUT} = 1.8V by package type (QFN8 and TSOT23-5), ranging between -0.3% and +0.3% for QFN8, and ranging between -0.4% and +0.4% for TSOT23-5.	4
		• Updated the VIN pin name (pins 3 and 4 for QFN8; pin 1 for TSOT23-5) to IN • Updated the VOUT pin name (pins 5 and 6 for QFN8; pin 5 for TSOT23-5) to OUT in the Pin Functions section.	5
		Updated the VIN pin name to IN in Figure 1 and Figure 2.	10
		Updated the VOUT pin name to OUT in Figure 3.	12
1.3	12/18/2025	Added the 2.9V fixed V_{OUT} option to the Features section.	1
		Added the MPQ20056GJ-29-AEC1 SKU and corrected “–Z” to “-Z” in the Ordering Information section.	2
		Added the MPQ20056-29 to Figure 1.	10
		• Added the 2.9V fixed V_{OUT} option in the Setting the Output Voltage section • Added a title for the figure number to Figure 4 • Minor formatting corrections	12

		• Updated Figure 4 to Figure 5
		• Added a new Figure 6 (1.8V fixed-output application circuit in a TSOT23-5L package)
		• Updated Figure 5 to Figure 7
		  ○ Updated Figure 7 R3 value from “NS” to “100kΩ”
		  ○ Minor formatting corrections
			13

		• Added a new Figure 8 (2.9V fixed-output application circuit in a TSOT23-5L package) • Updated Figure 6 to Figure 9 • Updated Figure 7 to Figure 10 • Minor formatting corrections	14

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