X4043, X4045

4k, 512 x 8 Bit CPU Supervisor with 4kbit EEPROM

FN8118
Rev 3.00
December 9, 2015

FEATURES

- **Selectable watchdog timer**
- **Low V_{CC} detection and reset assertion**
  - **—Five standard reset threshold voltages**
  - **—Adjust low V_{CC} reset threshold voltage using special programming sequence**
  - **—Reset signal valid to V_{CC} = 1V**
- **Low power CMOS**
  - **—<20µA max standby current, watchdog on**
  - **—<1µA standby current, watchdog OFF**
  - **—3mA active current**
- **4kbits of EEPROM**
  - **—16-byte page write mode**
  - **—Self-timed write cycle**
  - **—5ms write cycle time (typical)**
- **Built-in inadvertent write protection**
  - **—Power-up/power-down protection circuitry**
  - **—Protect 0, 1/4, 1/2, all or 16, 32, 64 or 128 bytes of EEPROM array with Block Lock™ protection**
- **400kHz 2-wire interface**
- **2.7V to 5.5V power supply operation**
- **Available packages**
  - **—8 Ld SOIC**
  - **—8 Ld MSOP**
  - **—8 Ld PDIP**
- **Pb-free plus anneal available (RoHS compliant)**

DESCRIPTION

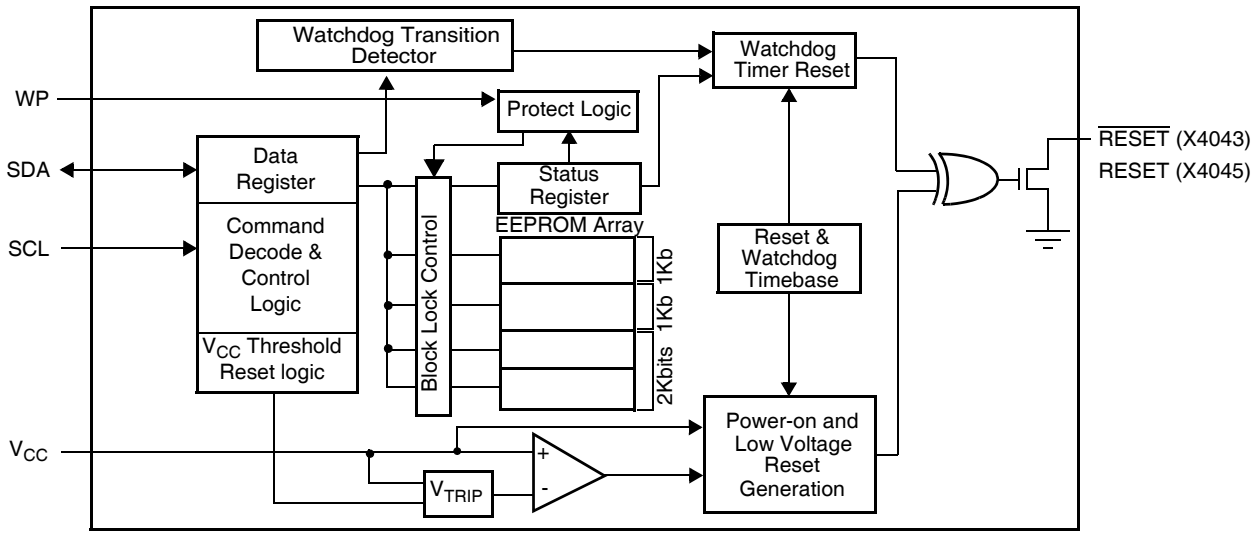
The X4043/45 combines four popular functions, Power-on Reset Control, Watchdog Timer, Supply Voltage Supervision, and Block Lock Protect Serial EEPROM Memory in one package. This combination lowers system cost, reduces board space requirements, and increases reliability.

Applying power to the device activates the power-on reset circuit which holds $\overline{\text{RESET}}$/RESET active for a period of time. This allows the power supply and oscillator to stabilize before the processor can execute code.

The Watchdog Timer provides an independent protection mechanism for microcontrollers. When the microcontroller fails to restart a timer within a selectable time out interval, the device activates the $\overline{\text{RESET}}$/RESET signal. The user selects the interval from three preset values. Once selected, the interval does not change, even after cycling the power.

The device's low V_{CC} detection circuitry protects the user's system from low voltage conditions, resetting the system when V_{CC} falls below the minimum V_{CC} trip point. $\overline{\text{RESET}}$/RESET is asserted until V_{CC} returns to proper operating level and stabilizes. Five industry standard V_{TRIP} thresholds are available, however, Intersil's unique circuits allow the threshold to be reprogrammed to meet custom requirements or to fine-tune the threshold for applications requiring higher precision.

BLOCK DIAGRAM



Ordering Information

PART NUMBER $\overline{\text{RESET}}$ (ACTIVE LOW)	PART MARKING	PART NUMBER RESET (ACTIVE HIGH)	PART MARKING	V_{CC} RANGE (V)	V_{TRIP} RANGE (V)	TEMP RANGE (°C)	PACKAGE
X4043S8Z-4.5A (Note)	X4043 Z AL	X4045S8Z-4.5A (Note)	X4045 Z AL	4.5-5.5	4.5-4.75	0 to 70	8 Ld SOIC (Pb-free)
X4043S8IZ-4.5A (Note)	X4043 Z AM	X4045S8IZ-4.5A (Note)	X4045 Z AM			-40 to 85	8 Ld SOIC (Pb-free)
X4043M8Z-4.5A (Note)	DAZ	X4045M8Z-4.5A (Note) **(No longer available, recommended replacement: X4045S8Z-4.5A)**	DBH			0 to 70	8 Ld MSOP (Pb-free)
X4043M8IZ-4.5A (Note)	DAU	X4045M8IZ-4.5A (Note) **(No longer available, recommended replacement: X4045S8IZ-4.5A)**	DBE			-40 to 85	8 Ld MSOP (Pb-free)
X4043PZ-4.5A (Note) **(No longer available, recommended replacement: X4043M8Z-4.5A)**	X4043P Z AL	X4045PZ-4.5A (Note) **(No longer available, recommended replacement: X4045S8Z-4.5A)**	X4045P Z AL			0 to 70	8 Ld PDIP (Pb-free)
X4043PIZ-4.5A (Note) **(No longer available, recommended replacement: X4043M8IZ-4.5A)**	X4043P Z AM	X4045PIZ-4.5A (Note) **(No longer available, recommended replacement: X4045S8IZ-4.5A)**	X4045P Z AM			-40 to 85	8 Ld PDIP (Pb-free)
X4043S8Z* (Note)	X4043 Z	X4045S8Z* (Note)	X4045 Z	4.5-5.5	4.25-4.5	0 to 70	8 Ld SOIC (Pb-free)
X4043S8IZ* (Note)	X4043 Z I	X4045S8IZ (Note)	X4045 Z I			-40 to 85	8 Ld SOIC (Pb-free)
X4043M8Z* (Note)	DAW	X4045M8Z (Note) **(No longer available, recommended replacement: X4045S8Z)**	DBD			0 to 70	8 Ld MSOP (Pb-free)
X4043M8IZ (Note)	DAR	X4045M8IZ (Note) **(No longer available, recommended replacement: X4045S8IZ)**	DBA			-40 to 85	8 Ld MSOP (Pb-free)
X4043PZ (Note) **(No longer available, recommended replacement: X4043M8Z)**	X4043P	X4045PZ (Note) **(No longer available, recommended replacement: X4045S8Z)**	X4045P Z			0 to 70	8 Ld PDIP (Pb-free)
X4043PIZ (Note) **(No longer available, recommended replacement: X4043M8IZ)**	X4043P Z I	X4045PIZ (Note) **(No longer available, recommended replacement: X4045S8IZ)**	X4045P Z I			-40 to 85	8 Ld PDIP (Pb-free)

Ordering Information

PART NUMBER $\overline{\text{RESET}}$ (ACTIVE LOW)	PART MARKING	PART NUMBER RESET (ACTIVE HIGH)	PART MARKING	V_{CC} RANGE (V)	V_{TRIP} RANGE (V)	TEMP RANGE (°C)	PACKAGE
X4043S8Z-2.7A* (Note)	X4043 Z AN	X4045S8Z-2.7A (Note)	X4045 Z AN	2.7-5.5	2.85-3.0	0 to 70	8 Ld SOIC (Pb-free)
X4043S8IZ-2.7A* (Note)	X4043 Z AP	X4045S8IZ-2.7A (Note)	X4045 Z AP			-40 to 85	8 Ld SOIC (Pb-free)
X4043M8Z-2.7A (Note)	DAY	X4045M8Z-2.7A (Note) **(No longer available, recommended replacement: X4045S8Z-2.7A)**	DBG			0 to 70	8 Ld MSOP (Pb-free)
X4043M8IZ-2.7A (Note)	DAT	X4045M8IZ-2.7A (Note) **(No longer available, recommended replacement: X4045S8IZ-2.7A)**	DBC			-40 to 85	8 Ld MSOP (Pb-free)
X4043PZ-2.7A (Note) **(No longer available, recommended replacement: X4043M8Z-2.7A)**	X4043P Z AN	X4045PZ-2.7A (Note) **(No longer available, recommended replacement: X4045S8Z-2.7A)**	X4045P Z AN			0 to 70	8 Ld PDIP (Pb-free)
X4043PIZ-2.7A (Note) **(No longer available, recommended replacement: X4043M8IZ-2.7A)**	X4043P Z AP	X4045PIZ-2.7A (Note) **(No longer available, recommended replacement: X4045S8IZ-2.7A)**	X4045P Z AP			-40 to 85	8 Ld PDIP (Pb-free)
X4043S8Z-2.7* (Note)	X4043 Z F	X4045S8Z-2.7* (Note)	X4045 Z F	2.7-5.5	2.55-2.7	0 to 70	8 Ld SOIC (Pb-free)
X4043S8IZ-2.7 (Note)	X4043 Z G	X4045S8IZ-2.7 (Note)	X4045 Z G			-40 to 85	8 Ld SOIC (Pb-free)
X4043M8Z-2.7 (Note)	DAX	X4045M8Z-2.7 (Note) **(No longer available, recommended replacement: X4045S8Z-2.7)**	DBF			0 to 70	8 Ld MSOP (Pb-free)
X4043M8IZ-2.7(Note)	DAS	X4045M8IZ-2.7 (Note) **(No longer available, recommended replacement: X4045S8IZ-2.7)**	DBB			-40 to 85	8 Ld MSOP (Pb-free)
X4043PZ-2.7 (Note) **(No longer available, recommended replacement: X4043M8Z-2.7)**	X4043P Z F	X4045PZ-2.7 (Note) **(No longer available, recommended replacement: X4045S8Z-2.7)**	X4045P Z F			0 to 70	8 Ld PDIP (Pb-free)
X4043PIZ-2.7 (Note) **(No longer available, recommended replacement: X4043M8IZ-2.7)**	X4043P Z G	X4045PIZ-2.7 (Note) **(No longer available, recommended replacement: X4045S8IZ-2.7)**	X4045P Z G			-40 to 85	8 Ld PDIP (Pb-free)

*Add "T1" suffix for tape and reel.

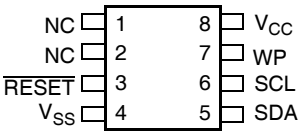
NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

The memory portion of the device is a CMOS Serial EEPROM array with Intersil's block lock protection. The array is internally organized as x 8. The device features an 2-wire interface and software protocol allowing operation on an I^2C bus.

The device utilizes Intersil's proprietary Direct Write™ cell, providing a minimum endurance of 1,000,000 cycles and a minimum data retention of 100 years.

PIN CONFIGURATION

8-Pin JEDEC SOIC, MSOP
(PDIP no longer available or supported)



Pin (SOIC/MSOP/DIP)	Name	Function
1	NC	No internal connections
2	NC	No internal connections
3	$\overline{RESET}$/RESET	**Reset Output**. $\overline{RESET}$ is an active LOW, open drain output which goes active whenever V_{CC} falls below V_{TRIP}. It will remain active until V_{CC} rises above the V_{TRIP} for t_{PURST}. $\overline{RESET}$/RESET goes active if the Watchdog Timer is enabled and SDA remains either HIGH or LOW longer than the selectable Watchdog time out period. $\overline{RESET}$/RESET goes active on power-uppower-up and remains active for 250ms after the power supply stabilizes. RESET is an active high open drain output. An external pull up resistor is required on the $\overline{RESET}$/RESET pin.
4	V_{SS}	**Ground**
5	SDA	**Serial Data.** SDA is a bidirectional pin used to transfer data into and out of the device. It has an open drain output and may be wire ORed with other open drain or open collector outputs. This pin requires a pull up resistor and the input buffer is always active (not gated).
6	SCL	**Serial Clock.** The Serial Clock input controls the serial bus timing for data input and output.
7	WP	**Write Protect.** WP HIGH prevents writes to any location in the device (including the control register). Connect WP pin to V_{SS} when it is not used.
8	V_{CC}	**Supply Voltage**

PRINCIPLES OF OPERATION

Power-on Reset

Application of power to the X4043/45 activates a Power-on Reset Circuit that pulls the $\overline{RESET}$/RESET pin active. This signal provides several benefits.

– It prevents the system microprocessor from starting to operate with insufficient voltage.

– It prevents the processor from operating prior to stabilization of the oscillator.

– It allows time for an FPGA to download its configuration prior to initialization of the circuit.

When V_{CC} exceeds the device V_{TRIP} threshold value for 200ms (nominal) the circuit releases $\overline{RESET}$/RESET allowing the system to begin operation.

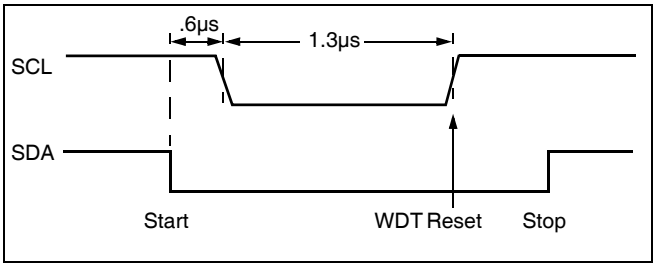
Low Voltage Monitoring

During operation, the X4043/45 monitors the V_{CC} level and asserts $\overline{RESET}$/RESET if supply voltage falls below a preset minimum V_{TRIP}. The $\overline{RESET}$/RESET signal prevents the microprocessor from operating in a power fail or brownout condition. The $\overline{RESET}$/RESET signal remains active until the voltage drops below 1V. It also remains active until V_{CC} returns and exceeds V_{TRIP} for 200ms.

Watchdog Timer

The Watchdog Timer circuit monitors the microprocessor activity by monitoring the SDA and SCL pins. A standard read or write sequence to any slave address byte restarts the watchdog timer and prevents the ($\overline{RESET}$/RESET) signal going active. A minimum sequence to reset the watchdog timer requires four microprocessor intructions namely, a Start, Clock Low, Clock High and Stop. (See Page 18) The state of two nonvolatile control bits in the status register determine the watchdog timer period. The microprocessor can change these watchdog bits, or they may be “locked” by tying the WP pin HIGH.

Figure 1. Watchdog Restart



EEPROM Inadvertent Write Protection

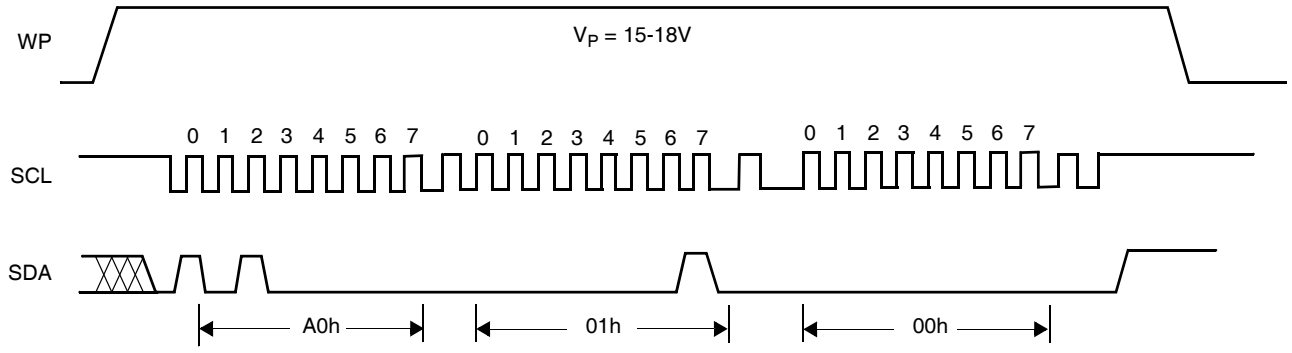
When $\overline{RESET}$/RESET goes active as a result of a low voltage condition ($V_{CC} < V_{TRIP}$), any in-progress communications are terminated. While $V_{CC} < V_{TRIP}$, no new communications are allowed and no nonvolatile write operation can start. Nonvolatile writes in-progress when $\overline{RESET}$/RESET goes active are allowed to finish.

Additional protection mechanisms are provided with memory block lock and the Write Protect (WP) pin. These are discussed elsewhere in this document.

V_{TRIP} Programming

The X4043/45 is shipped with a standard V_{CC} threshold (V_{TRIP}) voltage. This value will not change over normal operating and storage conditions. However, in applications where the standard V_{TRIP} is not exactly right, or if higher precision is needed in the V_{TRIP} value, the X4043/45 threshold may be adjusted. The procedure is described below, and uses the application of a high voltage control signal.

Figure 2. Set V_{TRIP} Level Sequence (V_{CC} = desired V_{TRIP} values WEL bit set)



Setting a V_{TRIP} Voltage

There are two procedures used to set the threshold voltages (V_{TRIP}), depending if the threshold voltage to be stored is higher or lower than the present value. For example, if the present V_{TRIP} is 2.9 V and the new V_{TRIP} is 3.2 V, the new voltage can be stored directly into the V_{TRIP} cell. If however, the new setting is to be lower than the present setting, then it is necessary to "reset" the V_{TRIP} voltage before setting the new value.

Setting a Higher V_{TRIP} Voltage

To set a V_{TRIP} threshold to a new voltage which is higher than the present threshold, the user must apply the desired V_{TRIP} threshold voltage to the V_{CC}. Then, a programming voltage (Vp) must be applied to the WP pin before a START condition is set up on SDA. Next, issue on the SDA pin the Slave Address A0h, followed by the Byte Address 01h for V_{TRIP} and a 00h Data Byte in order to program V_{TRIP}. The STOP bit following a valid write operation initiates the programming sequence. WP pin must then be brought LOW to complete the operation.

To check if the V_{TRIP} has been set, first power-down the device. Slowly ramp up V_{CC} and observe when the output, $\overline{\text{RESET}}$ (4043) or RESET (4045) switches. The voltage at which this occurs is the V_{TRIP} (actual) (see Figure 2).

CASE A

Now if the desired V_{TRIP} is greater than the V_{TRIP} (actual), then add the difference between V_{TRIP} (desired) - V_{TRIP} (actual) to the original V_{TRIP} desired. This is your new V_{TRIP} that should be applied to V_{CC} and the whole sequence should be repeated again (see Figure 5).

CASE B

Now if the V_{TRIP} (actual), is higher than the V_{TRIP} (desired), perform the reset sequence as described in the next section. The new V_{TRIP} voltage to be applied to V_{CC} will now be: V_{TRIP} (desired) - (V_{TRIP} (actual) - V_{TRIP} (desired)).

Note: This operation does not corrupt the memory array.

Setting a Lower V_{TRIP} Voltage

In order to set V_{TRIP} to a lower voltage than the present value, then V_{TRIP} must first be "reset" according to the procedure described below. Once V_{TRIP} has been "reset", then V_{TRIP} can be set to the desired voltage using the procedure described in "Setting a Higher V_{TRIP} Voltage".

Resetting the V_{TRIP} Voltage

To reset a V_{TRIP} voltage, apply the programming voltage (Vp) to the WP pin before a START condition is set up on SDA. Next, issue on the SDA pin the Slave Address A0h followed by the Byte Address 03h followed by 00h for the Data Byte in order to reset V_{TRIP}. The STOP bit following a valid write operation initiates the programming sequence. Pin WP must then be brought LOW to complete the operation.

After being reset, the value of V_{TRIP} becomes a nominal value of 1.7V or lesser.

Note: This operation does not corrupt the memory array.

Figure 3. Reset V_{TRIP} Level Sequence (V_{CC} > 3V. WP = 15-18V, WEL bit set)

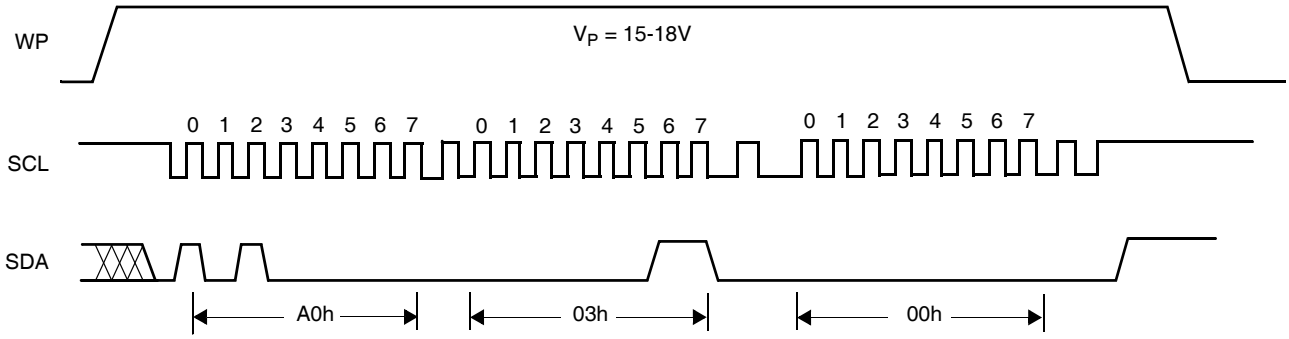


Figure 4. Sample V_{TRIP} Reset Circuit

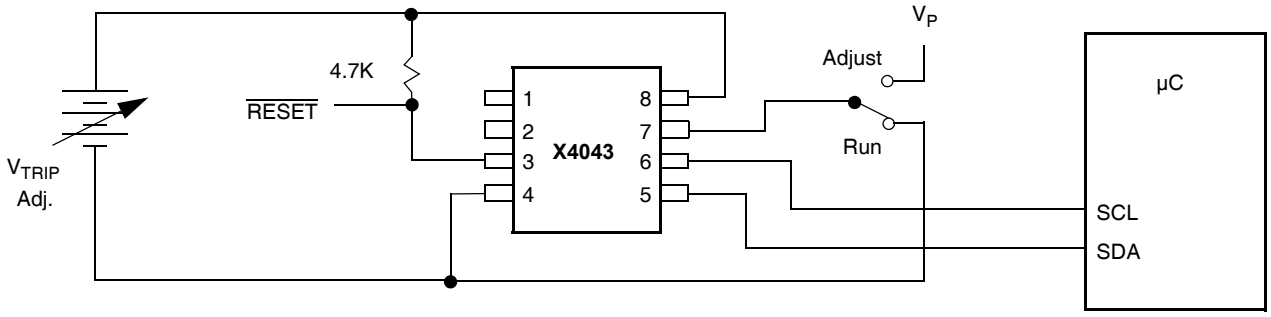
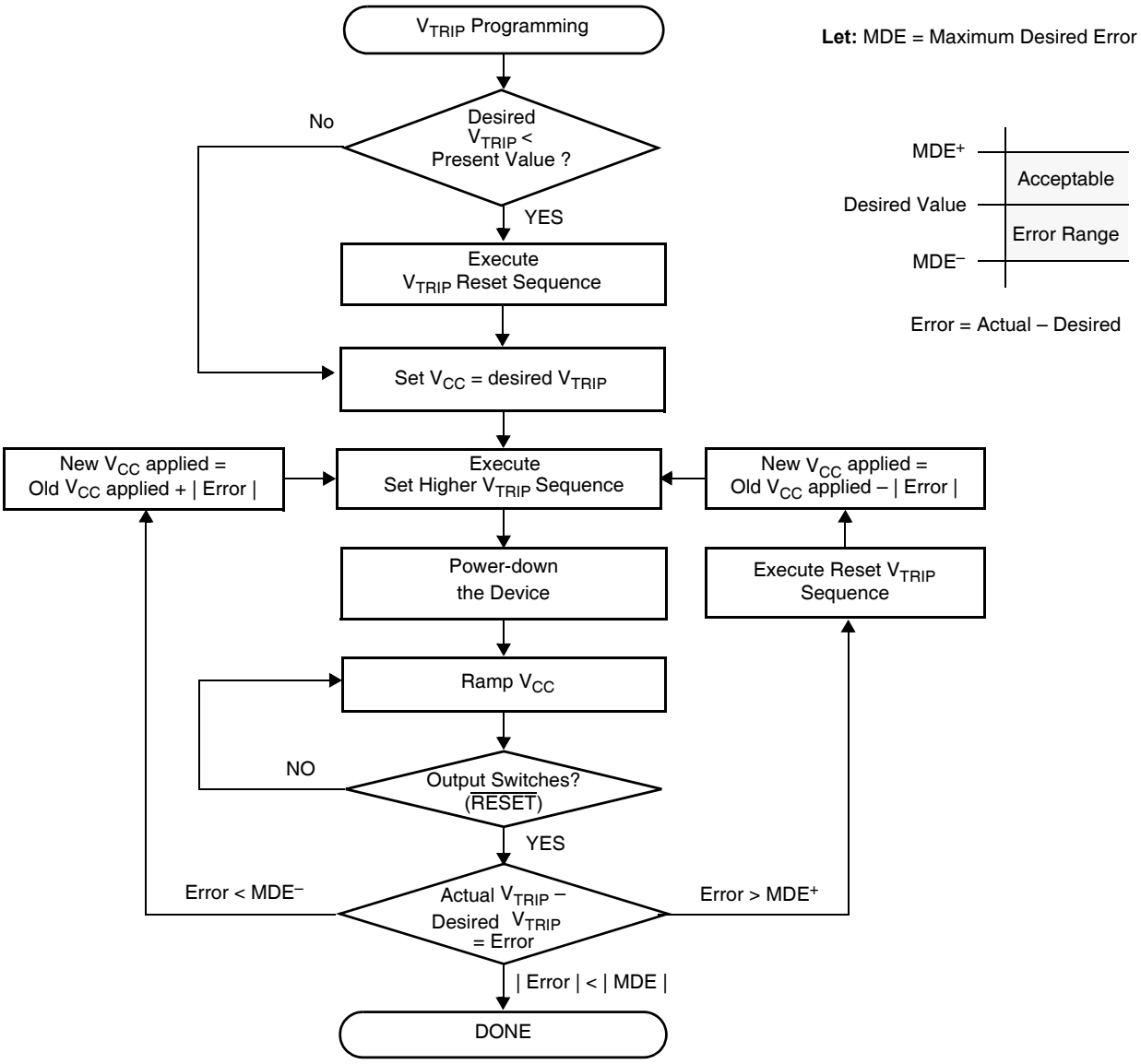


Figure 5. V_{TRIP} Programming Sequence



Control Register

The control register provides the user a mechanism for changing the block lock and watchdog timer settings. The block lock and watchdog timer bits are nonvolatile and do not change when power is removed.

The control register is accessed with a special preamble in the slave byte (1011) and is located at address 1FFh. It can only be modified by performing a byte write operation directly to the address of the register and only one data byte is allowed for each register write operation. Prior to writing to the control register, the WEL and RWEL bits must be set using a two step process, with the whole sequence requiring 3 steps. See "Writing to the Control Register".

The user must issue a stop after sending this byte to the register to initiate the nonvolatile cycle that stores WD1, WD0, BP2, BP1, and BP0. The X4043/45 will not acknowledge any data bytes written after the first byte is entered.

The state of the control register can be read at any time by performing a random read at address 1FFh, using the special preamble. Only one byte is read by each register read operation. The X4043/45 resets itself after the first byte is read. The master should supply a stop condition to be consistent with the bus protocol, but a stop is not required to end this operation.

7	6	5	4	3	2	1	0
0	WD1	WD0	BP1	BP0	RWEL	WEL	BP2

RWEL: Register Write Enable Latch (Volatile)

The RWEL bit must be set to “1” prior to a write to the Control Register.

WEL: Write Enable Latch (Volatile)

The WEL bit controls the access to the memory and to the Register during a write operation. This bit is a volatile latch that powers up in the LOW (disabled) state. While the WEL bit is LOW, writes to any address, including any control registers will be ignored (no acknowledge will be issued after the Data Byte). The WEL bit is set by writing a “1” to the WEL bit and zeroes to the other bits of the control register. Once set, WEL remains set until either it is reset to 0 (by writing a “0” to the WEL bit and zeroes to the other bits of the control register) or until the part powers up again. Writes to the WEL bit do not cause a nonvolatile write cycle, so the device is ready for the next operation immediately after the stop condition.

BP2, BP1, BP0: Block Protect Bits (Nonvolatile)

The block protect bits, BP2, BP1 and BP0, determine which blocks of the array are write protected. A write to a protected block of memory is ignored. The block protect bits will prevent write operations to one of eight segments of the array.

BP2	BP1	BP0	Protected Addresses (Size)	Array Lock
0	0	0	None (factory setting)	None
0	0	1	180h - 1FFh (128 bytes)	Upper 1/4 (Q4)
0	1	0	100h - 1FFh (256 bytes)	Upper 1/2 (Q3,Q4)
0	1	1	000h - 1FFh (512 bytes)	Full Array (All)
1	0	0	000h - 00Fh (16 bytes)	First Page (P1)
1	0	1	000h - 01Fh (32 bytes)	First 2 pgs (P2)
1	1	0	000h - 03Fh (64 bytes)	First 4 pgs (P4)
1	1	1	000h - 07Fh (128 bytes)	First 8 pgs (P8)

WD1, WD0: Watchdog Timer Bits

The bits WD1 and WD0 control the period of the watchdog timer. The options are shown below.

WD1	WD0	Watchdog Time Out Period
0	0	1.4 seconds
0	1	600 milliseconds
1	0	200 milliseconds
1	1	Disabled (factory setting)

Writing to the Control Register

Changing any of the nonvolatile bits of the control register requires the following steps:

– Write a 02H to the control register to set the write enable latch (WEL). This is a volatile operation, so there is no delay after the write. (Operation preceeded by a start and ended with a stop).

– Write a 06H to the control register to set both the register write enable latch (RWEL) and the WEL bit. This is also a volatile cycle. The zeros in the data byte are required. (Operation preceeded by a start and ended with a stop).

– Write a value to the control register that has all the control bits set to the desired state. This can be represented as *0xys t*01*r* in binary, where *xy* are the WD bits, and *rst* are the BP bits. (Operation preceeded by a start and ended with a stop). Since this is a nonvolatile write cycle it will take up to 10ms to complete. The RWEL bit is reset by this cycle and the sequence must be repeated to change the nonvolatile bits again. If bit 2 is set to ‘1’ in this third step (*0xys t*11*r*) then the RWEL bit is set, but the WD1, WD0, BP2, BP1 and BP0 bits remain unchanged. Writing a second byte to the control register is not allowed. Doing so aborts the write operation and returns a NACK.

– A read operation occurring between any of the previous operations will not interrupt the register write operation.

– The RWEL bit cannot be reset without writing to the nonvolatile control bits in the control register, power cycling the device or attempting a write to a write protected block.

To illustrate, a sequence of writes to the device consisting of [02H, 06H, 02H] will reset all of the nonvolatile bits in the control register to 0. A sequence of [02H, 06H, 06H] will leave the nonvolatile bits unchanged and the RWEL bit remains set.

SERIAL INTERFACE

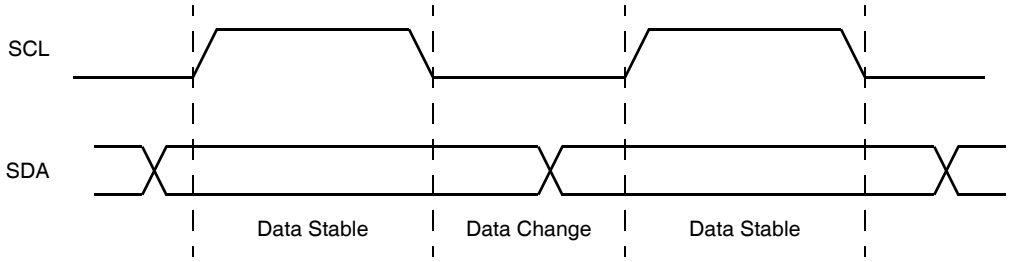
Serial Interface Conventions

The device supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter, and the receiving device as the receiver. The device controlling the transfer is called the master and the device being controlled is called the slave. The master always initiates data transfers, and provides the clock for both transmit and receive operations. Therefore, the devices in this family operate as slaves in all applications.

Serial Clock and Data

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. See Figure 6.

Figure 6. Valid Data Changes on the SDA Bus



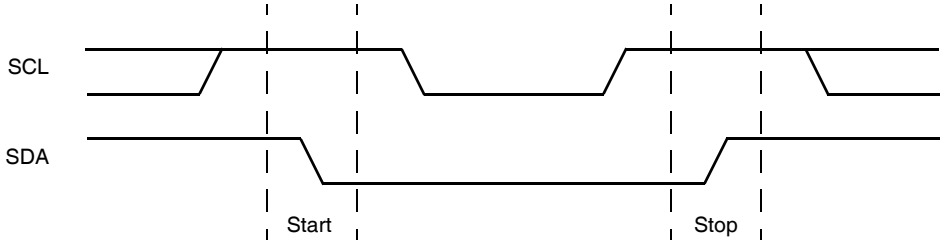
Serial Start Condition

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met. See Figure 7.

Serial Stop Condition

All communications must be terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used to place the device into the standby power mode after a read sequence. A stop condition can only be issued after the transmitting device has released the bus. See Figure 6.

Figure 7. Valid Start and Stop Conditions



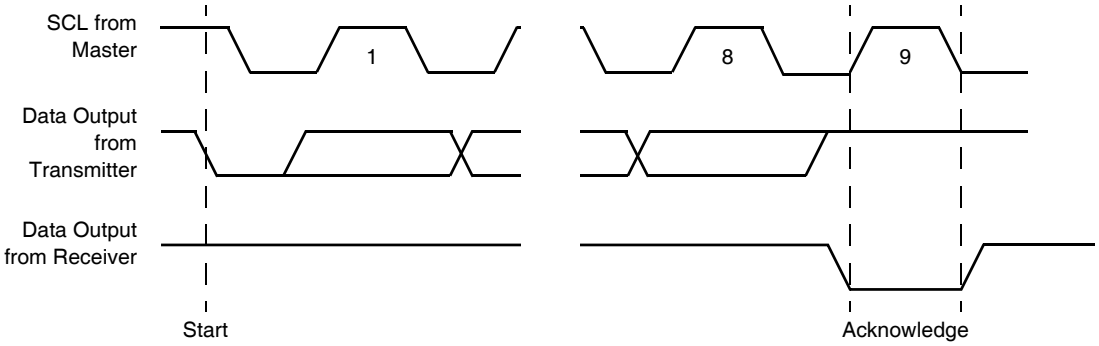
Serial Acknowledge

Acknowledge is a software convention used to indicate successful data transfer. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data. Refer to Figure 8.

The device will respond with an acknowledge after recognition of a start condition and if the correct device identifier and select bits are contained in the slave address byte. If a write operation is selected, the device will respond with an acknowledge after the receipt of each subsequent eight bit word. The device will acknowledge all incoming data and address bytes, except for the slave address byte when the device identifier and/or select bits are incorrect.

In the read mode, the device will transmit eight bits of data, release the SDA line, then monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the device will continue to transmit data. The device will terminate further data transmissions if an acknowledge is not detected. The master must then issue a stop condition to return the device to standby mode and place the device into a known state.

Figure 8. Acknowledge Response From Receiver



X4043/45 ADDRESSING

Slave Address Byte

Following a start condition, the master must output a slave address byte. This byte consists of several parts:

– a device type identifier that is ‘1010’ to access the array and ‘1011’ to access the control register.

– two bits of ‘0’.

– one bit that becomes the MSB of the address.

– one bit of the slave command byte is a R/$\overline{W}$ bit. The R/$\overline{W}$ bit of the slave address byte defines the operation to be performed. When the R/$\overline{W}$ bit is a one, then a read operation is selected. A zero selects a write operation. Refer to Figure 8.

– After loading the entire slave address byte from the SDA bus, the device compares the input slave byte data to the proper slave byte. Upon a correct compare, the device outputs an acknowledge on the SDA line.

Word Address

The word address is either supplied by the master or obtained from an internal counter. The internal counter is undefined on a power-up condition.

Slave Address Byte

Figure 9. X4043/45 Addressing

	Slave Byte							
Array Control Reg.	1	0	1	0	0	0	A8	R/W
	1	0	1	1				
	Word Address							
	A7	A6	A5	A4	A3	A2	A1	A0

Operational Notes

The device powers-up in the following state:

– The device is in the low power standby state.

– The WEL bit is set to ‘0’. In this state it is not possible to write to the device.

– SDA pin is the input mode.

– $\overline{RESET}$ signal is active for t_{PURST}.

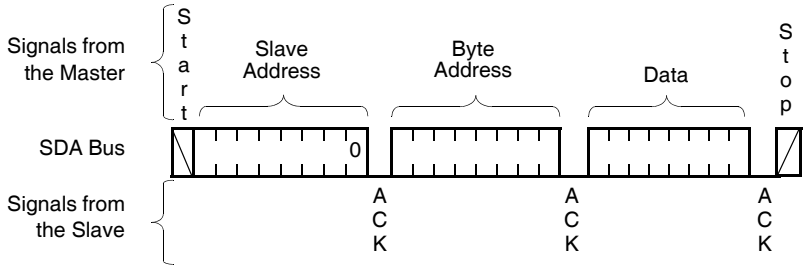
SERIAL WRITE OPERATIONS

Byte Write

For a write operation, the device requires the slave address byte and a word address byte. This gives the master access to any one of the words in the array. After receipt of the word address byte, the device responds with an acknowledge, and awaits the next eight bits of data. After receiving the 8 bits of the data byte, the device again responds with an acknowledge. The master then terminates the transfer by generating a stop condition, at which time the device begins the internal write cycle to the nonvolatile memory. During this internal write cycle, the device inputs are disabled, so the device will not respond to any requests from the master. The SDA output is at high impedance. See Figure 10.

A write to a protected block of memory will suppress the acknowledge bit.

Figure 10. Byte Write Sequence



Page Write

The device is capable of a page write operation. It is initiated in the same manner as the byte write operation; but instead of terminating the write cycle after the first data byte is transferred, the master can transmit an unlimited number of 8-bit bytes. After the receipt of each byte, the device will respond with an acknowledge, and the address is internally incremented by one. The page address remains constant. When the counter reaches the end of the page, it “rolls over” and goes back to ‘0’ on the same page. This means that the master can write 16 bytes to the page starting at any location on that page. If the master begins writing at location 10, and loads 12 bytes, then the first 5 bytes are written to locations 10 through 15, and the last 7 bytes are written to locations 0 through 6. Afterwards, the address counter would point to location 7 of the page that was just written. If the master supplies more than 16 bytes of data, then new data over-writes the previous data, one byte at a time.

Figure 11. Page Write Operation

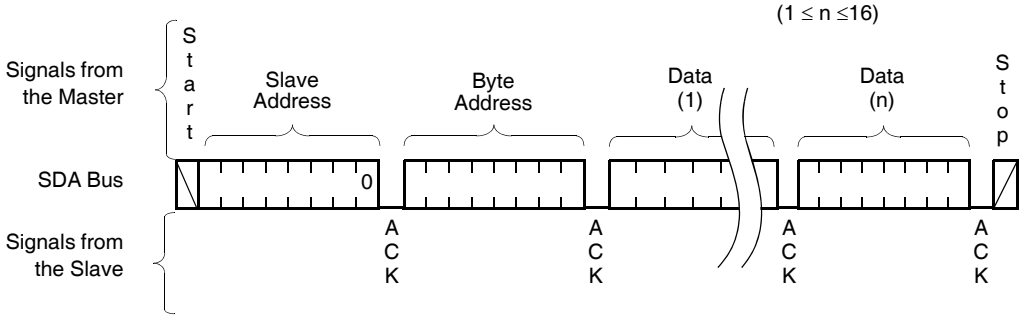
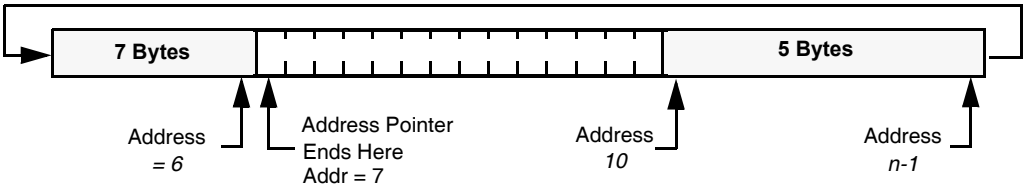


Figure 12. Writing 12-bytes to a 16-byte page starting at location 10



The master terminates the data byte loading by issuing a stop condition, which causes the device to begin the nonvolatile write cycle. As with the byte write operation, all inputs are disabled until completion of the internal write cycle. See Figure 11 for the address, acknowledge, and data transfer sequence.

Stops and Write Modes

Stop conditions (that terminate write operations) must be sent by the master after sending at least 1 full data byte, plus the subsequent ACK signal. If a stop is issued in the middle of a data byte, or before 1 full data byte plus its associated ACK is sent, then the device will reset itself without performing the write. The contents of the array will not be effected.

Acknowledge Polling

The disabling of the inputs during nonvolatile cycles can be used to take advantage of the typical 5kHz write cycle time. Once the stop condition is issued to indicate the end of the master's byte load operation, the device initiates the internal nonvolatile cycle. Acknowledge polling can be initiated immediately. To do this, the master issues a start condition followed by the slave address byte for a write or read operation. If the device is still busy with the nonvolatile cycle then no ACK will be returned. If the device has completed the write operation, an ACK will be returned and the host can then proceed with the read or write operation. Refer to the flow chart in Figure 13.

Serial Read Operations

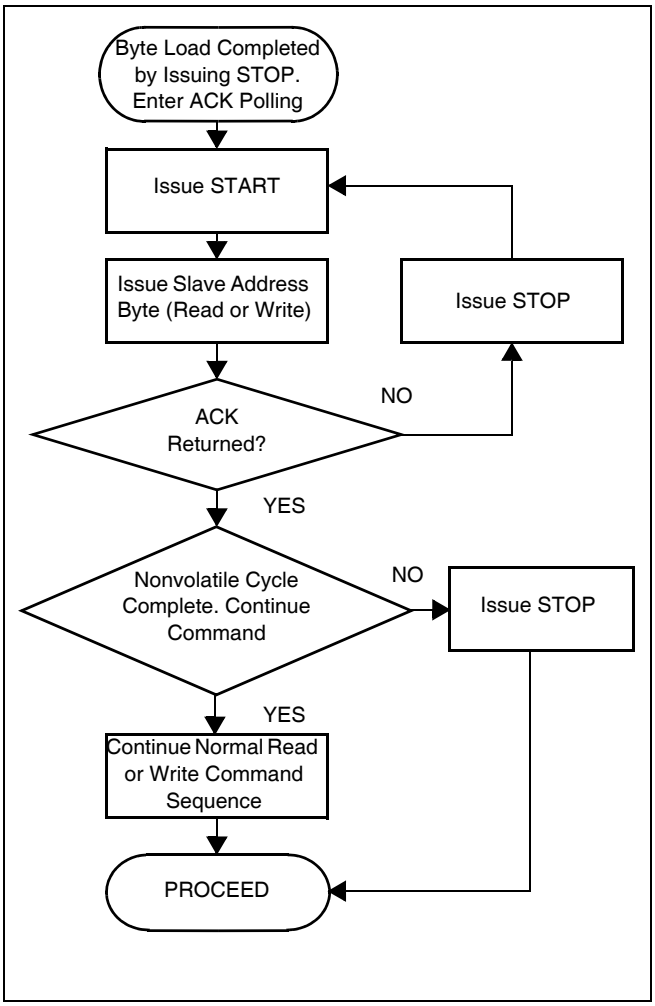
Read operations are initiated in the same manner as write operations with the exception that the R/$\overline{W}$ bit of the slave address byte is set to one. There are three basic read operations: Current Address Reads, Random Reads, and Sequential Reads.

Current Address Read

Internally the device contains an address counter that maintains the address of the last word read incremented by one. Therefore, if the last read was to address n, the next read operation would access data from address n+1. On power-up, the address of the address counter is undefined, requiring a read or write operation for initialization.

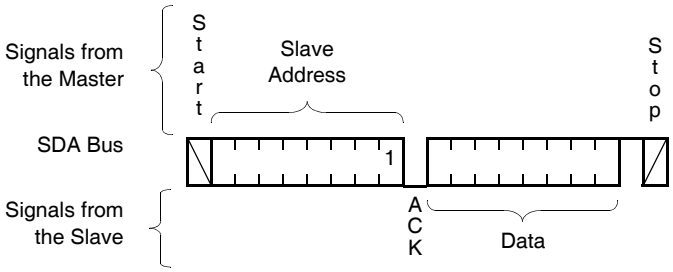
Upon receipt of the slave address byte with the R/$\overline{W}$ bit set to one, the device issues an acknowledge and then transmits the eight bits of the data byte. The master terminates the read operation when it does not respond with an acknowledge during the ninth clock and then issues a stop condition. Refer to Figure 13 for the address, acknowledge, and data transfer sequence.

Figure 13. Acknowledge Polling Sequence



It should be noted that the ninth clock cycle of the read operation is not a "don't care." To terminate a read operation, the master must either issue a stop condition during the ninth cycle or hold SDA HIGH during the ninth clock cycle and then issue a stop condition.

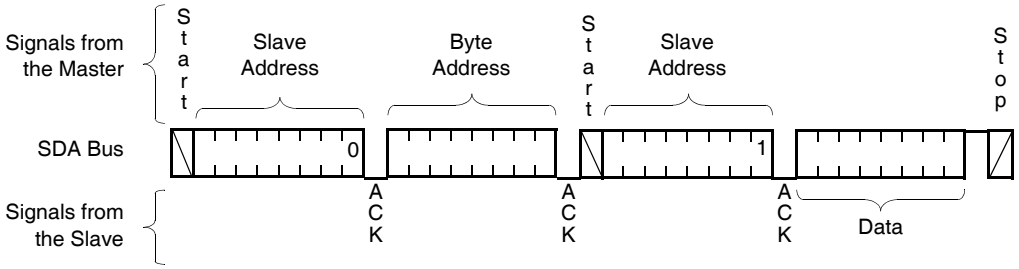
Figure 14. Current Address Read Sequence



Random Read

Random read operation allows the master to access any memory location in the array. Prior to issuing the slave address byte with the R/$\overline{W}$ bit set to one, the master must first perform a “dummy” write operation. The master issues the start condition and the slave address byte, receives an acknowledge, then issues the word address bytes. After acknowledging receipts of the word address bytes, the master immediately issues another start condition and the slave address byte with the R/$\overline{W}$ bit set to one. This is followed by an acknowledge from the device and then by the eight bit word. The master terminates the read operation by not responding with an acknowledge and then issuing a stop condition. Refer to Figure 15 for the address, acknowledge, and data transfer sequence.

Figure 15. Random Address Read Sequence



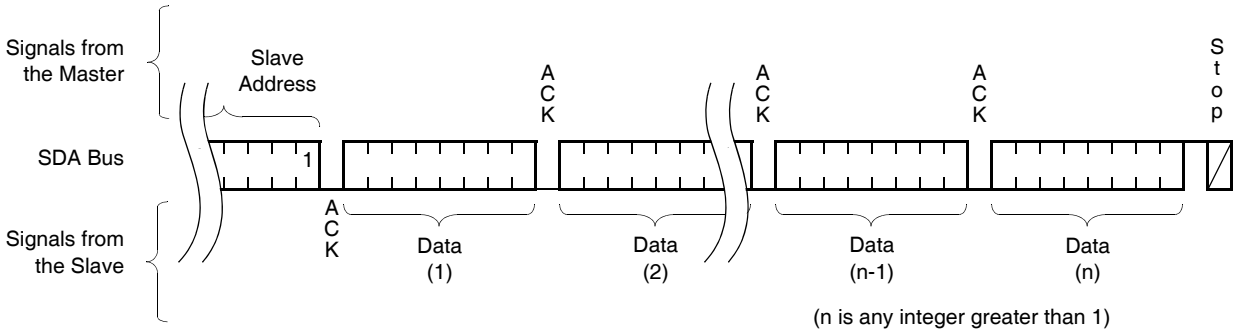
There is a similar operation, called “Set Current Address” where the device does no operation, but enters a new address into the address counter if a stop is issued instead of the second start shown in Figure 14. The device goes into standby mode after the stop and all bus activity will be ignored until a start is detected. The next current address read operation reads from the newly loaded address. This operation could be useful if the master knows the next address it needs to read, but is not ready for the data.

Sequential Read

Sequential reads can be initiated as either a current address read or random address read. The first data byte is transmitted as with the other modes; however, the master now responds with an acknowledge, indicating it requires additional data. The device continues to output data for each acknowledge received. The master terminates the read operation by not responding with an acknowledge and then issuing a stop condition.

The data output is sequential, with the data from address n followed by the data from address n + 1. The address counter for read operations increments through all page and column addresses, allowing the entire memory contents to be serially read during one operation. At the end of the address space the counter “rolls over” to address 0000_H and the device continues to output data for each acknowledge received. Refer to Figure 16 for the acknowledge and data transfer sequence.

Figure 16. Sequential Read Sequence



Data Protection

The following circuitry has been included to prevent inadvertent writes:

– The WEL bit must be set to allow write operations.

– The proper clock count and bit sequence is required prior to the stop bit in order to start a nonvolatile write cycle.

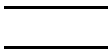
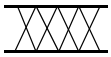
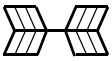
– A three step sequence is required before writing into the control register to change watchdog timer or block lock settings.

– The WP pin, when held HIGH, prevents all writes to the array and the control register.

– Communication to the device is inhibited as a result of a low voltage condition ($V_{CC} < V_{TRIP}$)any in-progress communication is terminated.

– Block lock bits can protect sections of the memory array from write operations.

Symbol Table

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

ABSOLUTE MAXIMUM RATINGS

Temperature under bias ..... -65°C to +135°C
Storage temperature ..... -65°C to +150°C
Voltage on any pin with
respect to V_{SS} ..... -1.0V to +7V
D.C. output current 5mA
Lead temperature (soldering, 10 seconds) ..... 300°C

COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only; the functional operation of the device (at these or any other conditions above those listed in the operational sections of this specification) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	70°C
Industrial	-40°C	+85°C

Option	Supply Voltage Limits
-2.7 and -2.7A	2.7V to 5.5V
Blank and -4.5A	4.5V to 5.5V

D.C. OPERATING CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified.)

Symbol	Parameter	V_{CC} = 2.7 to 5.5V Min.	V_{CC} = 2.7 to 5.5V Max.	Unit	Test Conditions
I_{CC1}(1)	Active supply current read		1.0	mA	$V_{IL} = V_{CC}$ x 0.1, $V_{IH} = V_{CC}$ x 0.9 f_{SCL} = 400kHz
I_{CC2}(1)	Active supply current write		3.0	mA	
I_{SB1}(2)	Standby current AC (WDT off)		1	µA	$V_{IL} = V_{CC}$ x 0.1, $V_{IH} = V_{CC}$ x 0.9 f_{SCL}= 400kHz, SDA = open V_{CC} = 1.22 x V_{CC} min
I_{SB2}(2)	Standby current DC (WDT off)		1	µA	$V_{SDA} = V_{SCL} = V_{SB}$ Others = GND or V_{SB}
I_{SB3}(2)	Standby current DC (WDT on)		20	µA	$V_{SDA} = V_{SCL} = V_{SB}$ Others = GND or V_{SB}
I_{LI}	Input leakage current		10	µA	V_{IN} = GND to V_{CC}
I_{LO}	Output leakage current		10	µA	V_{SDA} = GND to V_{CC} device is in standby
V_{IL}(3)	Input LOW voltage	-0.5	V_{CC} x 0.3	V	
V_{IH}(3)	Input nonvolatile	V_{CC} x 0.7	V_{CC} + 0.5	V	
V_{HYS}	Schmitt trigger input hysteresis Fixed input level V_{CC} related level	 0.2 .05 x V_{CC}		 V V	
V_{OL}	Output LOW voltage		0.4	V	I_{OL} = 3.0mA (2.7-5.5V) I_{OL} = 1.8mA (2.0-3.6V)

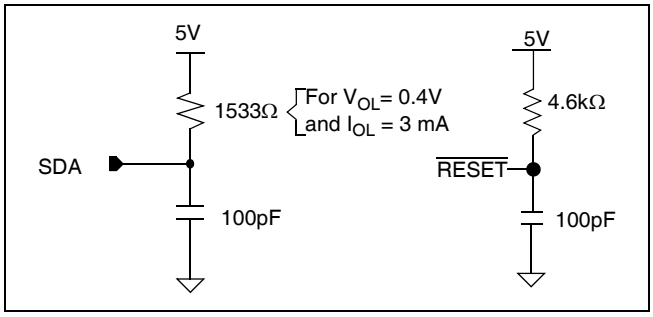
Notes: (1) The device enters the active state after any start, and remains active until: 9 clock cycles later if the device select bits in the slave address byte are incorrect; 200ns after a stop ending a read operation; or t_{WC} after a stop ending a write operation.
(2) The device goes into standby: 200ns after any stop, except those that initiate a nonvolatile write cycle; t_{WC} after a stop that initiates a nonvolatile cycle; or 9 clock cycles after any start that is not followed by the correct device select bits in the slave address byte.
(3) V_{IL} min. and V_{IH} max. are for reference only and are not tested.

CAPACITANCE (T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V)

Symbol	Parameter	Max.	Unit	Test Conditions
C_{OUT}(4)	Output capacitance (SDA, $\overline{RESET}$/RESET)	8	pF	V_{OUT} = 0V
C_{IN}(4)	Input capacitance (SCL, WP)	6	pF	V_{IN} = 0V

Notes: (4) This parameter is periodically sampled and not 100% tested.

EQUIVALENT A.C. LOAD CIRCUIT



A.C. TEST CONDITIONS

Input pulse levels	0.1 V_{CC} to 0.9 V_{CC}
Input rise and fall times	10ns
Input and output timing levels	0.5 V_{CC}
Output load	Standard output load

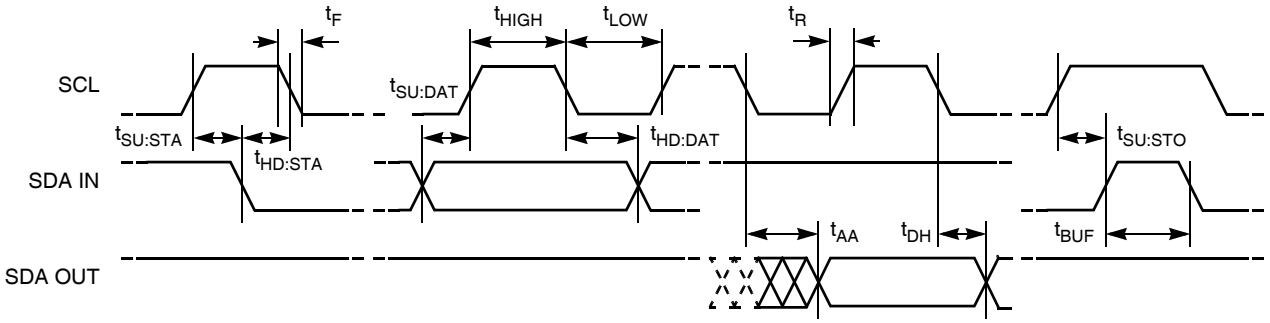
A.C. CHARACTERISTICS (Over recommended operating conditions, unless otherwise specified)

Symbol	Parameter	100kHz		400kHz		Unit
		Min.	Max.	Min.	Max.	
f_{SCL}	SCL clock frequency	0	100	0	400	kHz
t_{IN}	Pulse width suppression time at inputs	n/a	n/a	50		ns
t_{AA}	SCL LOW to SDA data out valid	0.1	0.9	0.1	0.9	µs
t_{BUF}	Time the bus free before start of new transmission	4.7		1.3		µs
t_{LOW}	Clock LOW time	4.7		1.3		µs
t_{HIGH}	Clock HIGH time	4.0		0.6		µs
$t_{SU:STA}$	Start condition setup time	4.7		0.6		µs
$t_{HD:STA}$	Start condition hold time	4.0		0.6		µs
$t_{SU:DAT}$	Data in setup time	250		100		ns
$t_{HD:DAT}$	Data in hold time	5.0		0		µs
$t_{SU:STO}$	Stop condition setup time	0.6		0.6		µs
t_{DH}	Data output hold time	50		50		ns
t_R	SDA and SCL rise time		1000	20 + .1Cb(6)	300	ns
t_F	SDA and SCL fall time		300	20 + .1Cb(6)	300	ns
$t_{SU:WP}$	WP setup time	0.4		0.6		µs
$t_{HD:WP}$	WP hold time	0		0		µs
Cb	Capacitive load for each bus line		400		400	pF

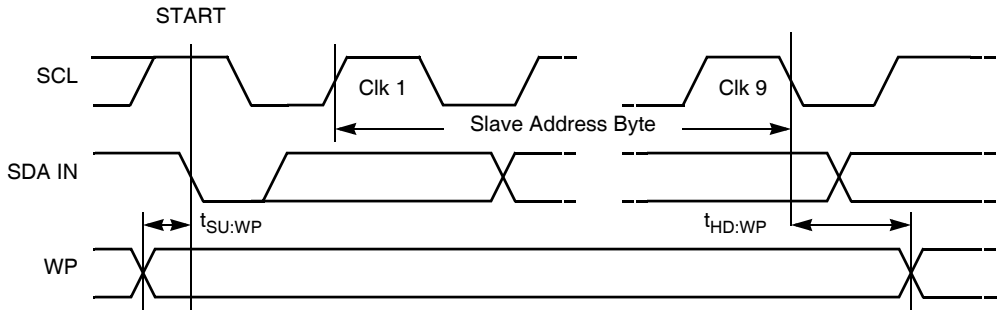
Notes: (5) Typical values are for T_A = 25°C and V_{CC} = 5.0V
(6) Cb = total capacitance of one bus line in pF.

TIMING DIAGRAMS

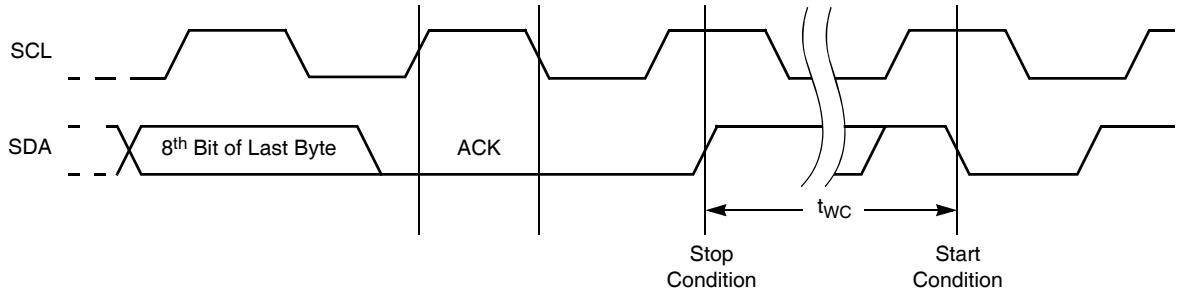
Bus Timing



WP Pin Timing



Write Cycle Timing

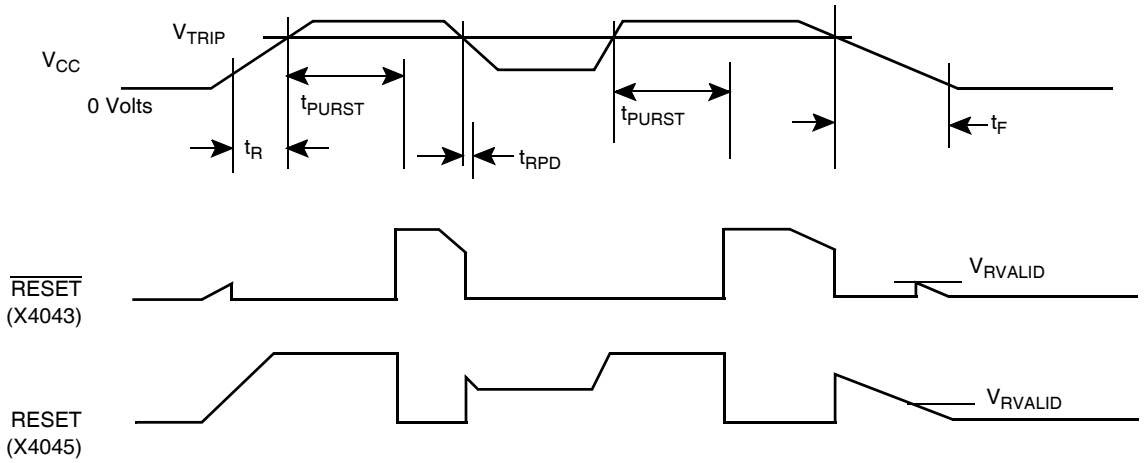


Nonvolatile Write Cycle Timing

Symbol	Parameter	Min.	Typ.(7)	Max.	Unit
t_{WC}(7)	Write cycle time		5	10	ms

Notes: (7) t_{WC} is the time from a valid stop condition at the end of a write sequence to the end of the self-timed internal nonvolatile write cycle. It is the minimum cycle time to be allowed for any nonvolatile write by the user, unless acknowledge polling is used.

Power-Up and Power-Down Timing

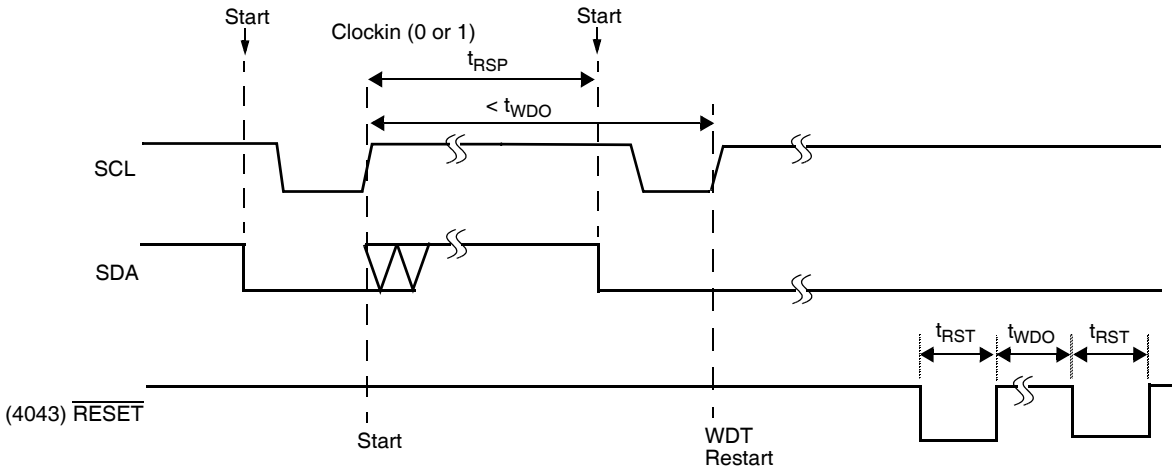


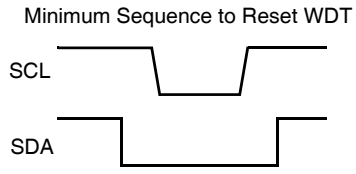
$\overline{RESET}$ Output Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{TRIP}	Reset trip point voltage, X4043/45-4.5A Reset trip point voltage, X4043/45 Reset trip point voltage, X4043/45-2.7A Reset trip point voltage, X4043/45-2.7	4.5 4.25 2.85 2.55	4.62 4.38 2.92 2.62	4.75 4.5 3.0 2.7	V
t_{PURST}	Power-up reset time out	100	200	400	ms
t_{RPD}(8)	V_{CC} detect to $\overline{RESET}$/RESET		10	20	µs
t_F(8)	V_{CC} fall time	20			mV/µs
t_R(8)	V_{CC} rise time	20			mV/µs
V_{RVALID}	Reset valid V_{CC}	1			V
t_{WDO}	Watchdog time out period, WD1 = 1, WD0 = 0 WD1 = 0, WD0 = 1 WD1 = 0, WD0 = 0	 100 450 1	 200 600 1.4	 300 800 2	 ms ms sec
t_{RSP}	Watchdog Time Restart pulse width	1			µs
t_{RST}	Reset time out	100	200	400	ms

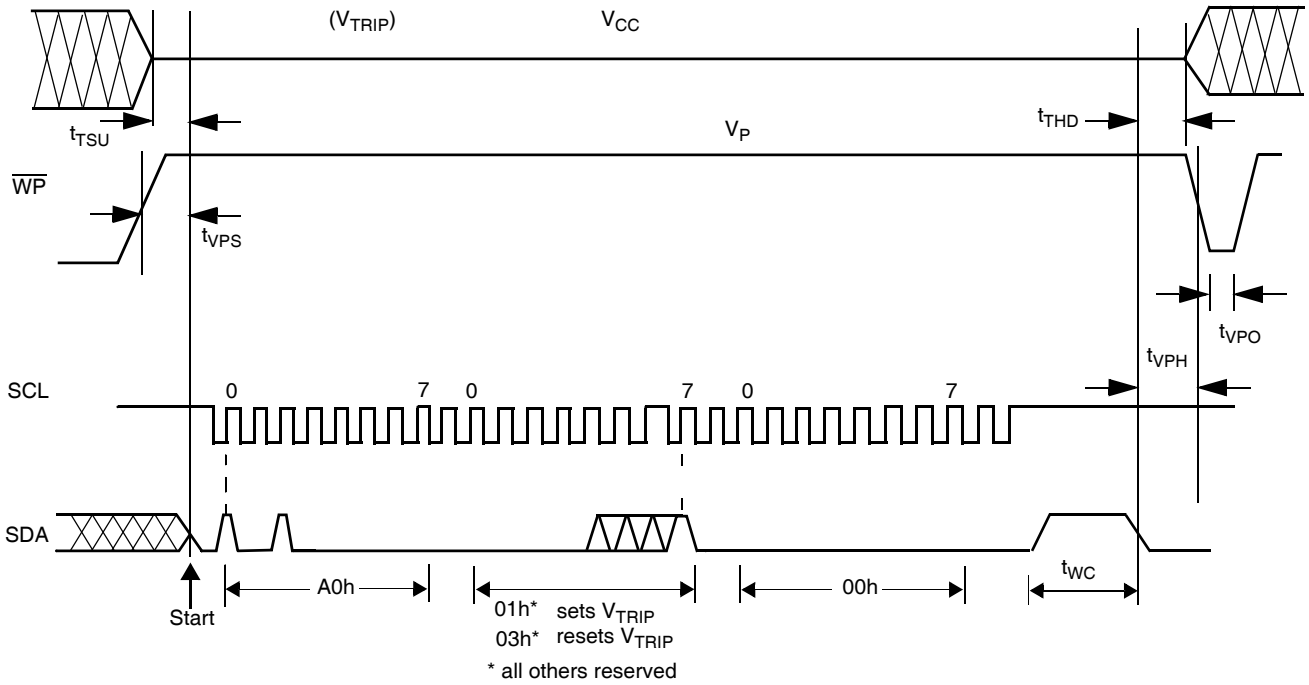
Notes: (8) This parameter is periodically sampled and not 100% tested.

Watchdog Time Out For 2-Wire Interface





V_{TRIP} Set/Reset Conditions



V_{TRIP} Programming Specifications: V_{CC} = 2.0-5.5V; Temperature = 25°C

Parameter	Description	Min.	Max.	Unit
t_{VPS}	WP Program Voltage Setup time	10		µs
t_{VPH}	WP Program Voltage Hold time	10		µs
t_{TSU}	V_{TRIP} Level Setup time	10		µs
t_{THD}	V_{TRIP} Level Hold (stable) time	10		µs
t_{WC}	V_{TRIP} Program Cycle	10		ms
t_{VPO}	Program Voltage Off time before next cycle	1		ms
V_P	Programming Voltage	15	18	V
V_{TRAN}	V_{TRIP} Set Voltage Range	2.0	4.75	V
V_{tv}	V_{TRIP} Set Voltage variation after programming (-40 to +85°C).	-25	+25	mV
t_{VPS}	WP Program Voltage Setup time	10		µs

REVISION HISTORY

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
December 9, 2015	FN8118.3	Updated Ordering Information Table on page 2. Added Revision History and About Intersil sections.

ABOUT INTERSIL

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

Reliability reports are also available from our website at www.intersil.com/support

© Copyright Intersil Americas LLC 2005-2015. All Rights Reserved.
All trademarks and registered trademarks are the property of their respective owners.

For additional products, see www.intersil.com/en/products.html

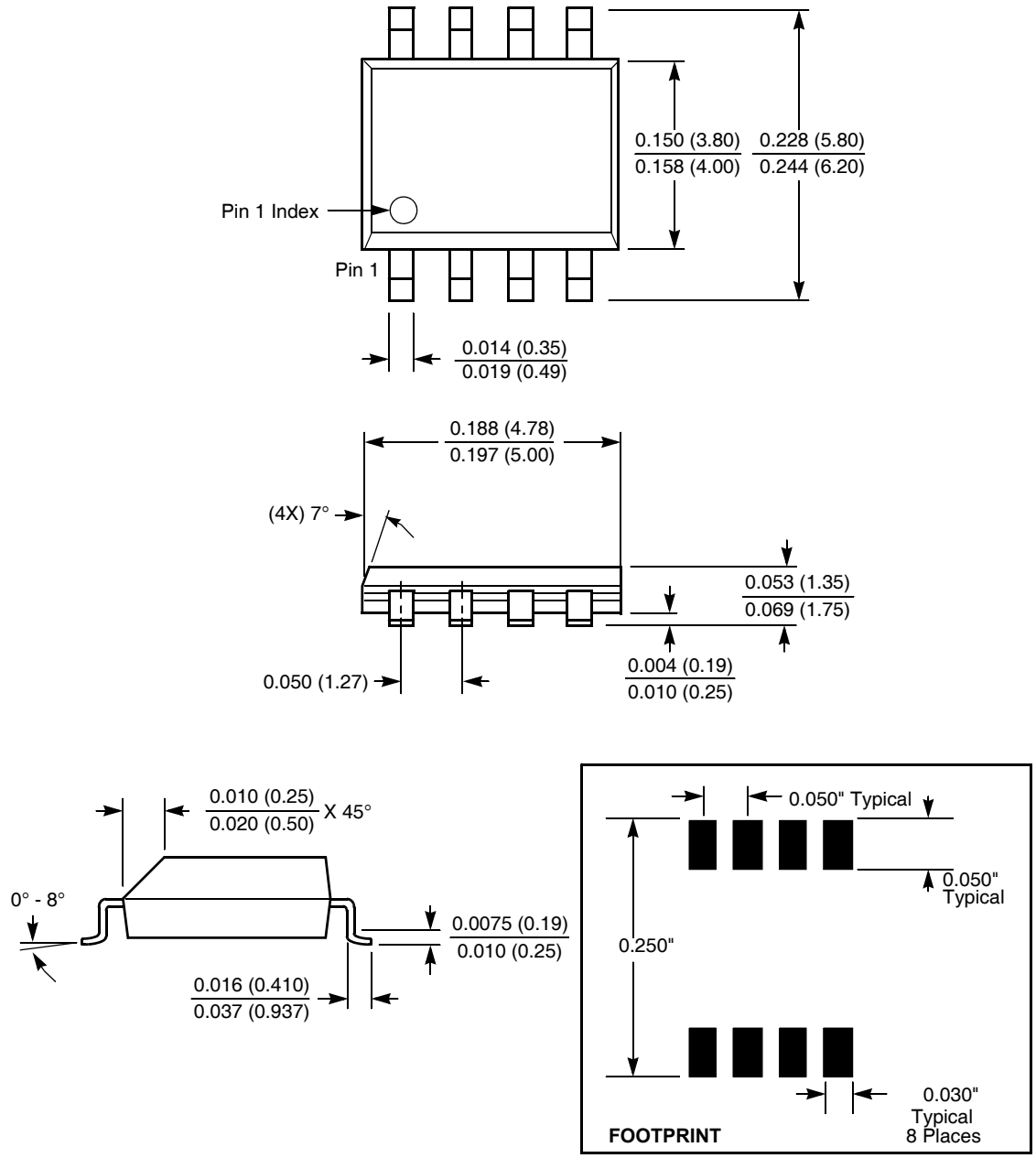
Intersil products are manufactured, assembled and tested utilizing ISO9001 quality systems as noted in the quality certifications found at www.intersil.com/en/support/qualandreliability.html

Intersil products are sold by description only. Intersil may modify the circuit design and/or specifications of products at any time without notice, provided that such modification does not, in Intersil's sole judgment, affect the form, fit or function of the product. Accordingly, the reader is cautioned to verify that datasheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see www.intersil.com

PACKAGING INFORMATION

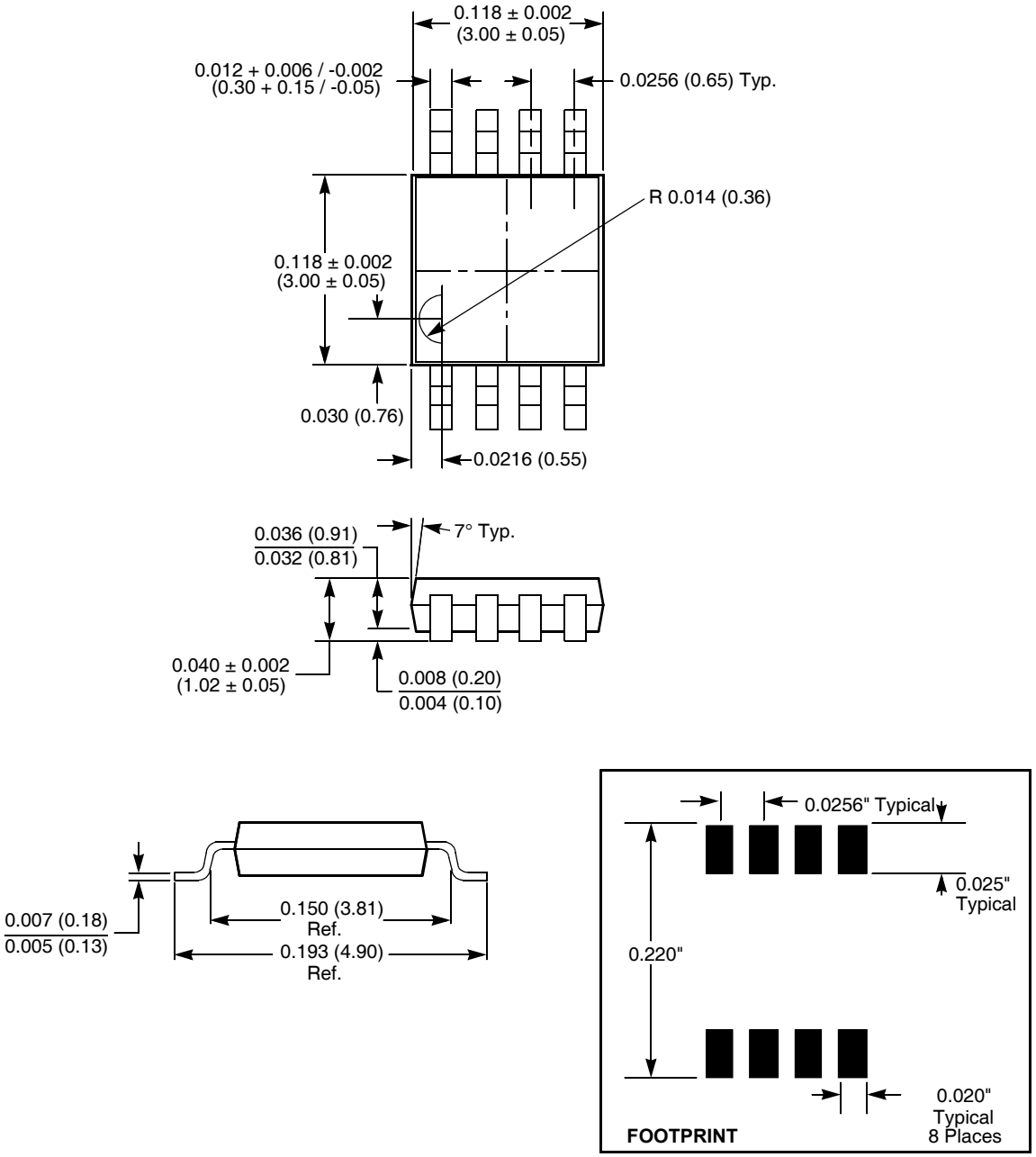
8-Lead Plastic Small Outline Gull Wing Package Type S



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

PACKAGING INFORMATION

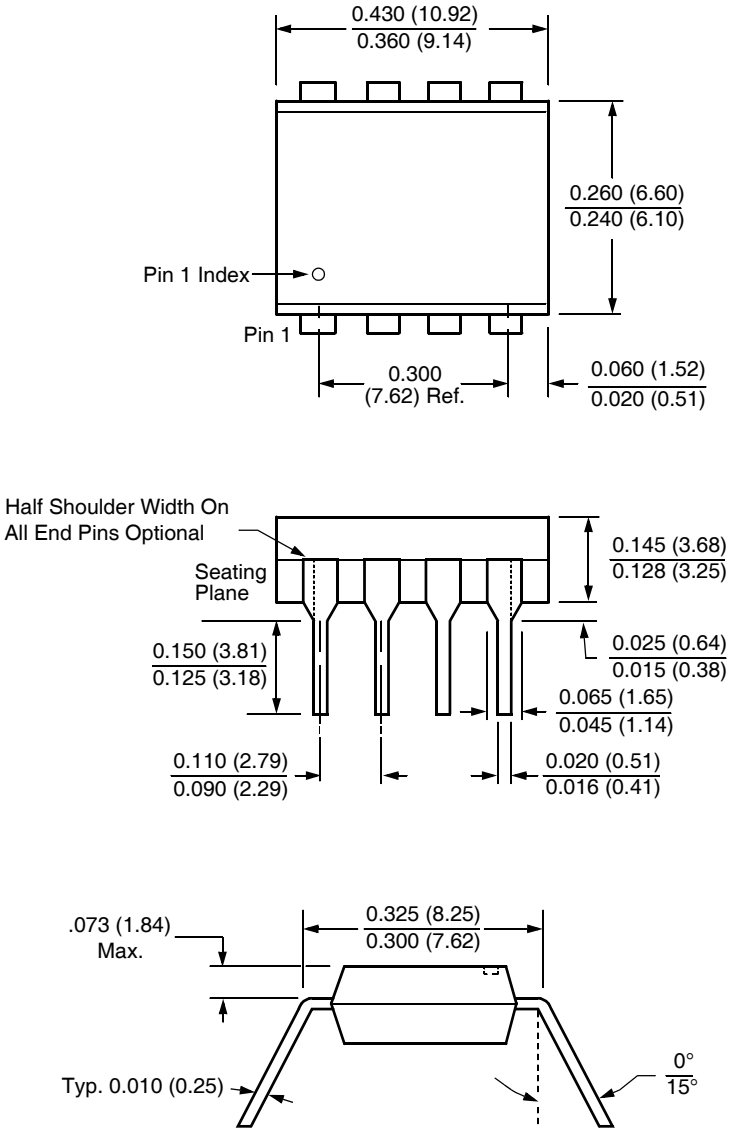
8-Lead Miniature Small Outline Gull Wing Package Type M



NOTE:
1. ALL DIMENSIONS IN INCHES AND (MILLIMETERS)

PACKAGING INFORMATION

8-Lead Plastic Dual In-Line Package Type P



NOTE:

1. **ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)**
2. **PACKAGE DIMENSIONS EXCLUDE MOLDING FLASH**