UCCx895 BiCMOS Advanced Phase-Shift PWM Controller

1 Features

- Programmable-output turnon delay
- Adaptive delay set
- Bidirectional oscillator synchronization
- Voltage-mode, peak current-mode, or average current-mode control
- Programmable soft start, soft stop, and chip disable via a single pin
- 0% to 100% duty-cycle control
- 7-MHz error amplifier
- Operation to 1 MHz
- Typical 5-mA operating current at 500 kHz
- Very low 150-μA current during UVLO

2 Applications

- Phase-shifted full-bridge converters
- Off-line, telecom, datacom, and servers
- Distributed power architecture
- High-density power modules

3 Description

The UCC3895 is a phase-shift PWM controller that implements control of a full-bridge power stage by phase shifting the switching of one half-bridge with respect to the other. The device allows constant frequency pulse-width modulation in conjunction with resonant zero-voltage switching to provide high efficiency at high frequencies. The part is used either as a voltage-mode or current-mode controller.

While the UCC3895 maintains the functionality of the UC3875/6/7/8 family and UC3879, it improves on that controller family with additional features such as enhanced control logic, adaptive delay set, and shutdown capability. Because the device is built using the BCDMOS process, it operates with dramatically less supply current than it's bipolar counterparts. The UCC3895 operates with a maximum clock frequency of 1 MHz.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
UCCx895	CDIP (20)	24.20 mm × 6.92 mm
	LCCC (20	8.89 mm × 8.89 mm
	SOIC (20)	12.80 mm × 7.50 mm
	PDIP (20)	24.33 mm × 6.35 mm
	TSSOP (20)	6.50 mm × 4.40 mm
	PLCC (20)	8.96 mm × 8.96 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Application Diagram

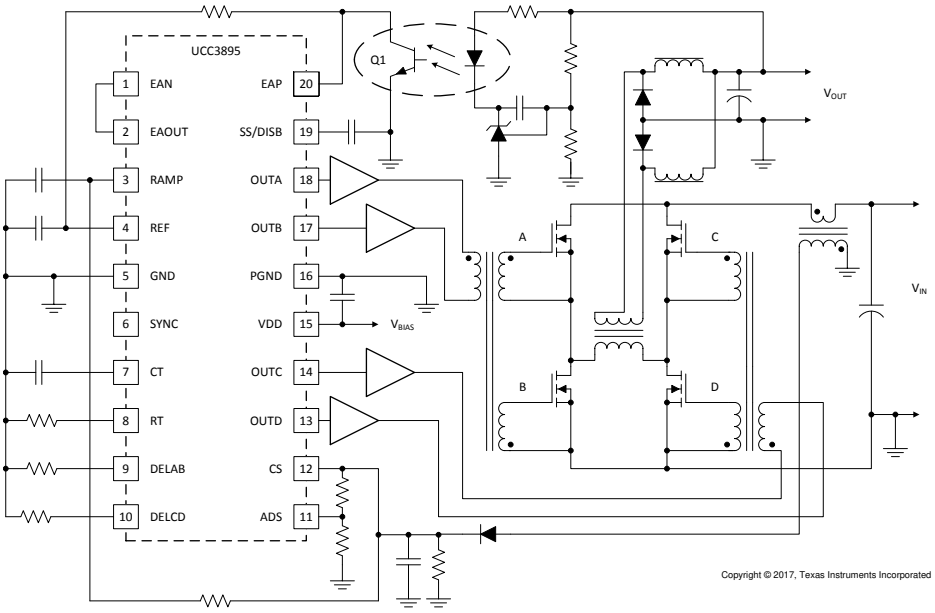


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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision P (June 2013) to Revision Q — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Changed UCC1895 V_{OL} MAX, From 250 mV : To 300 mV in *Electrical Characteristics* ... 8
- Changed UCC1895 RAMP sink current MIN, From 12 mA : To 10 mA in *Electrical Characteristics* ... 8
- Changed the F_{SW} note in the *Detailed Design Procedure* section ... 23
- Changed the voltage drop across the $R_{DS(on)}$ from 0.5-V to 4.5-V forward voltage drop in the output rectifiers ... 23
- Added *Output Voltage Setpoint* section ... 34
- Added *Setting the Switching Frequency* section ... 36
- Added *Soft Start* section ... 36
- Added *Setting the Switching Delays* section ... 36
- Added *Setting the Slope Compensation* section ... 38

Changes from Revision O (April 2010) to Revision P — **Page**

- Added *The CS input connects to* text to the beginning of the CS Detailed Pin Description. ... 14
- Added second paragraph to detailed REF Pin Description and included the UCC1895 at the end of the first paragraph to differentiate capacitance capabilities of the devices. ... 16
- Changed *UCC3895 Timing Diagram* in the Application Information section to reflect the maximum duty cycle conditions 19

Changes from Revision N (May 2009) to Revision O — **Page**

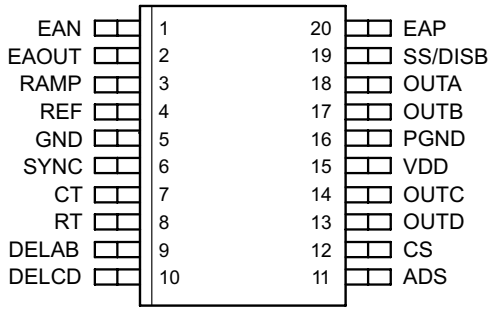
- Changed REF pin description from “Do not use more than 1.0 μF of total capacitance on this pin.” to “Do not use more than 4.7 μF of total capacitance on this pin.” ... 16

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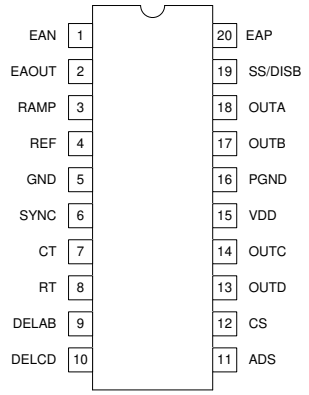
5 Pin Configuration and Functions

PW AND DW PACKAGE DRAWINGS (TOP VIEW)

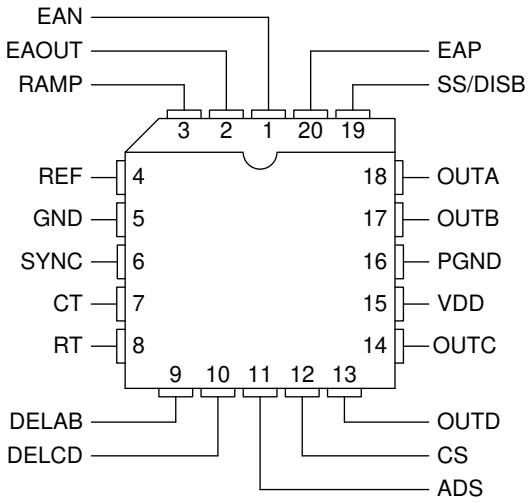
PW and DW PACKAGE
(TOP VIEW)



N AND J PACKAGE DRAWINGS (TOP VIEW)



FN AND FK PACKAGE DRAWINGS (TOP VIEW)



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
ADS	11	I	The adaptive-delay-set pin sets the ratio between the maximum and minimum programmed output delay dead time.
CS	12	I	Current sense input for cycle-by-cycle current limiting and for over-current comparator.
CT	7	I	Oscillator timing capacitor for programming the switching frequency. The UCC3895 oscillator charges CT via a programmed current.
DELAB	9	I	The delay-programming between complementary-outputs pin, DELAB, programs the dead time between switching of output A and output B.
DELCD	10	I	The delay-programming between complementary-outputs pin, DELCD, programs the dead time between switching of output C and output D.
EAOUT	2	I/O	Error amplifier output.
EAP	20	I	Non-inverting input to the error amplifier. Keep below 3.6 V for proper operation.
EAN	1	I	Inverting input to the error amplifier. Keep below 3.6 V for proper operation.
GND	5	—	Chip ground for all circuits except the output stages.
OUTA	18	O	The four outputs are 100-mA complementary MOS drivers, and are optimized to drive FET driver circuits such as UCC27714 or gate drive transformers.
OUTB	17	O	
OUTC	14	O	
OUTD	13	O	
PGND	16	—	Output stage ground.
RAMP	3	I	Inverting input of the PWM comparator.
REF	4	O	5-V, ±1.2%, 5-mA voltage reference. For best performance, bypass with a 0.1-μF low ESR, low ESL capacitor to ground. Do not use more than 4.7 μF of total capacitance on this pin.
RT	8	I	Oscillator timing resistor for programming the switching frequency.
SS/DISB	19	I	Soft-start and disable pin which combines the two independent functions.
SYNC	6	I/O	The oscillator synchronization pin is bidirectional.
VDD	15	I	The power supply input pin, VDD, must be bypassed with a minimum of a 1-μF low ESR, low ESL capacitor to ground. The addition of a 10-μF low ESR, low ESL between VDD and PGND is recommended.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
	Supply voltage			17	V
	Output current			100	mA
	Reference current			15	mA
	Supply current			30	mA
	Analog inputs	EAP, EAN, EAOUT, RAMP, SYNC, ADS, CS, SS/DISB	–0.3	REF + 0.3	V
	Drive outputs	OUTA, OUTB, OUTC, OUTD	–0.3	VCC + 0.3	V
	Power dissipation at T_A = 25°C	DW-20 package		650	mW
		N-20 package		1	W
T_J	Junction temperature		–55	150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	10		16.5	V
V_{DD}	Supply voltage bypass capacitor(2)		10 × C_{REF}		µF
C_{REF}	Reference bypass capacitor (UCC1895)(3)	0.1		1	µF
C_{REF}	Reference bypass capacitor (UCC2895, UCC3895)(3)	0.1		4.7	µF
C_T	Timing capacitor (for 500-kHz switching frequency)		220		pF
R_T	Timing resistor (for 500-kHz switching frequency)		82		kΩ
R_{DEL_AB}, R_{DEL_CD}	Delay resistor	2.5		40	kΩ
T_J	Operating junction temperature(4)	–55		125	°C

(1) TI recommends that there be a single point grounded between GND and PGND directly under the device. There must be a separate ground plane associated with the GND pin and all components associated with pins 1 through 12, plus 19 and 20, be located over this ground plane. Any connections associated with these pins to ground must be connected to this ground plane.
(2) The V_{DD} capacitor must be a low ESR, ESL ceramic capacitor located directly across the VDD and PGND pins. A larger bulk capacitor must be located as physically close as possible to the V_{DD} pins.
(3) The V_{REF} capacitor must be a low ESR, ESL ceramic capacitor located directly across the REF and GND pins. If a larger capacitor is desired for the V_{REF} then it must be located near the V_{REF} cap and connected to the V_{REF} pin with a resistor of 51 Ω or greater. The bulk capacitor on V_{DD} must be a factor of 10 greater than the total V_{REF} capacitance.
(4) TI does not recommended that the device operate under conditions beyond those specified in this table for extended periods of time.

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6.4 Thermal Information

THERMAL METRIC(1)		UCC1895		UCC2895 UCC3895		UCC2895 UCC3895	UCC3895	UNIT
		J (CDIP)	FK (LCCC)	DW (SOIC)	PW (TSSOP)	FN (PLCC)	N (PDIP)	
		20 PINS	20 PINS	20 PINS	20 PINS	20 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	N/A	N/A	66.4	91.0	54.8	48.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	34.2	31.2	31.6	26.1	32.8	35.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	48.9	30.9	34.1	42.2	19.0	29.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	N/A	N/A	8.6	1.3	9.0	16.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	N/A	N/A	33.7	41.6	18.7	29.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	8.9	3.3	N/A	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

V_{DD} = 12 V, R_T = 82 kΩ, C_T = 220 pF, R_{DELAB} = 10 kΩ, R_{DELCD} = 10 kΩ, C_{REF} = 0.1 µF, C_{VDD} = 0.1 µF and no load on the outputs, $T_A = T_J$. T_A = 0°C to 70°C for UCC3895x, T_A = –40°C to 85°C for UCC2895x and T_A = –55°C to 125°C for the UCC1895x (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
UVLO (UNDERVOLTAGE LOCKOUT)						
$UVLO_{(on)}$	Start-up voltage threshold		10.2	11	11.8	V
$UVLO_{(off)}$	Minimum operating voltage after start-up		8.2	9	9.8	V
$UVLO_{(hys)}$	Hysteresis		1	2	3	V
SUPPLY						
I_{START}	Start-up current	VDD = 8 V		150	250	µA
I_{DD}	Operating current			5	6	mA
V_{DD_CLAMP}	V_{DD} clamp voltage	IDD = 10 mA	16.5	17.5	18.5	V
VOLTAGE REFERENCE						
V_{REF}	Output voltage	T_J = 25°C	4.94	5	5.06	V
		10 V < VDD < V_{DD_CLAMP}, 0 mA < IREF < 5 mA, temperature	4.85	5	5.15	
I_{SC}	Short circuit current	REF = 0 V, T_J = 25°C	10	20		mA
ERROR AMPLIFIER						
	Common-mode input voltage range		–0.1		3.6	V
V_{IO}	Offset voltage		–7		7	mV
I_{BIAS}	Input bias current (EAP, EAN)		–1		1	µA
$EAOUT_{_VOH}$	High-level output voltage	EAP – EAN = 500 mV, I_{EAOUT} = –0.5 mA	4	4.5	5	V
$EAOUT_{_VOL}$	Low-level output voltage	EAP – EAN = –500 mV, I_{EAOUT} = 0.5 mA	0	0.2	0.4	V
I_{SOURCE}	Error amplifier output source current	EAP – EAN = 500 mV, EAOUT = 2.5 V	1	1.5		mA
I_{SINK}	Error amplifier output sink current	EAP – EAN = –500 mV, EAOUT = 2.5 V	2.5	4.5		mA
A_{VOL}	Open-loop dc gain		75	85		dB
GBW	Unity gain bandwidth(1)		5	7		mHz
	Slew rate(1)	1 V < EAN < 0 V, EAP = 500 mV, 0.5 V < EAOUT < 3 V	1.5	2.2		V/µs
	No-load comparator turn-off threshold		0.45	0.5	0.55	V
	No-load comparator turn-on threshold		0.55	0.6	0.69	V

(1) Ensured by design. Not production tested.

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Electrical Characteristics (continued)

V_{DD} = 12 V, R_T = 82 kΩ, C_T = 220 pF, R_{DELAB} = 10 kΩ, R_{DELCD} = 10 kΩ, C_{REF} = 0.1 µF, C_{VDD} = 0.1 µF and no load on the outputs, $T_A = T_J$. T_A = 0°C to 70°C for UCC3895x, T_A = –40°C to 85°C for UCC2895x and T_A = –55°C to 125°C for the UCC1895x (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	No-load comparator hysteresis		0.035	0.1	0.165	V
OSCILLATOR						
f_{OSC}	Frequency	T_J = 25°C	473	500	527	kHz
	Frequency total variation	Over line, temperature		2.5%	5%	
V_{IH_SYNC}	SYNC input threshold, SYNC		2.05	2.1	2.4	V
V_{OH_SYNC}	High-level output voltage, SYNC	I_{SYNC} = –400 µA, V_{CT} = 2.6 V	4.1	4.5	5	V
V_{OL_SYNC}	Low-level output voltage, SYNC	I_{SYNC} = 100 µA, V_{CT} = 0 V	0	0.5	1	V
	Sync output pulse width	$LOAD_{SYNC}$ = 3.9 kΩ and 30 pF in parallel		85	135	ns
V_{RT}	Timing resistor voltage		2.9	3	3.1	V
$V_{CT(peak)}$	Timing capacitor peak voltage		2.25	2.35	2.55	V
$V_{CT(valley)}$	Timing capacitor valley voltage		0	0.2	0.4	V
CURRENT SENSE						
$I_{CS(bias)}$	Current sense bias current	0 V < CS < 2.5 V, 0 V ADS < 2.5 V	–4.5		20	µA
	Peak current threshold		1.9	2	2.1	V
	Overcurrent threshold		2.4	2.5	2.6	V
	Current sense to output delay	0 V ≤ CS ≤ 2.3 V, DELAB = DELCD = REF		75	110	ns
SOFT START/SHUTDOWN						
I_{SOURCE}	Soft-start source current	SS/DISB = 3.0 V, CS = 1.9 V	–40	–35	–30	µA
I_{SINK}	Soft-start sink current	SS/DISB = 3.0 V, CS = 2.6 V	325	350	375	µA
	Soft-start/disable comparator threshold		0.44	0.5	0.56	V
ADAPTIVE DELAY SET (ADS)						
	DELAB/DELCD output voltage	ADS = CS = 0 V	0.45	0.5	0.55	V
		ADS = 0 V, CS = 2 V	1.9	2	2.1	
t_{DELAY}	Output delay[1][2]	ADS = CS = 0 V	450	560	620	ns
	ADS bias current	0 V < ADS < 2.5 V, 0 V < CS < 2.5 V	–20		20	µA

(2) Output delay is measured between OUTA and OUTB, or OUTC and OUTD. Output delay is defined as shown below where: $t_{f(OUTA)}$ = falling edge of OUTA signal, $t_{r(OUTB)}$ = rising edge of OUTB signal (see Figure 1 and Figure 2).

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Electrical Characteristics (continued)

V_{DD} = 12 V, R_T = 82 kΩ, C_T = 220 pF, R_{DELAB} = 10 kΩ, R_{DELCD} = 10 kΩ, C_{REF} = 0.1 µF, C_{VDD} = 0.1 µF and no load on the outputs, $T_A = T_J$. T_A = 0°C to 70°C for UCC3895x, T_A = –40°C to 85°C for UCC2895x and T_A = –55°C to 125°C for the UCC1895x (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OUTPUT							
V_{OH}	High-level output voltage (all outputs)	I_{OUT} = –10 mA, VDD to output			250	400	mV
V_{OL}	Low-level output voltage (all outputs)	I_{OUT} = 10 mA	UCC1895		150	300	mV
			UCC2895, UCC3895		150	250	
t_R	Rise time(1)	C_{LOAD} = 100 pF			20	35	ns
t_F	Fall time(1)	C_{LOAD} = 100 pF			20	35	ns
PWM COMPARATOR							
	EAOUT to RAMP input offset voltage	RAMP = 0 V, DELAB = DELCD = REF		0.72	0.85	1.05	V
	Minimum phase shift(3) (OUTA to OUTC, OUTB to OUTD)	RAMP = 0 V, EAOUT = 650 mV		0.0%	0.85%	1.4%	
t_{DELAY}	Delay(2) (RAMP to OUTC, RAMP to OUTD)	0 V < RAMP < 2.5 V, EAOUT = 1.2 V, DELAB = DELCD = REF			70	120	ns
$I_{R(bias)}$	RAMP bias current	RAMP < 5 V, CT = 2.2 V		–5		5	µA
$I_{R(sink)}$	RAMP sink current	RAMP = 5 V, CT = 2.6 V	UCC1895	10	19		mA
			UCC2895, UCC3895	12	19		

(3) Minimum phase shift is defined as:

$$\Phi = 180 \times \frac{t_{f(OUTC)} - t_{f(OUTA)}}{t_{PERIOD}} \quad \text{or} \quad \Phi = 180 \times \frac{t_{f(OUTC)} - t_{f(OUTB)}}{t_{PERIOD}}$$

where

(a) $t_{f(OUTA)}$ = falling edge of OUTA signal
(b) $t_{f(OUTB)}$ = falling edge of OUTB signal
(c) $t_{f(OUTC)}$ = falling edge of OUTC signal
(d) $t_{f(OUTD)}$ = falling edge of OUTD signal
(e) t_{PERIOD} = period of OUTA or OUTB signal

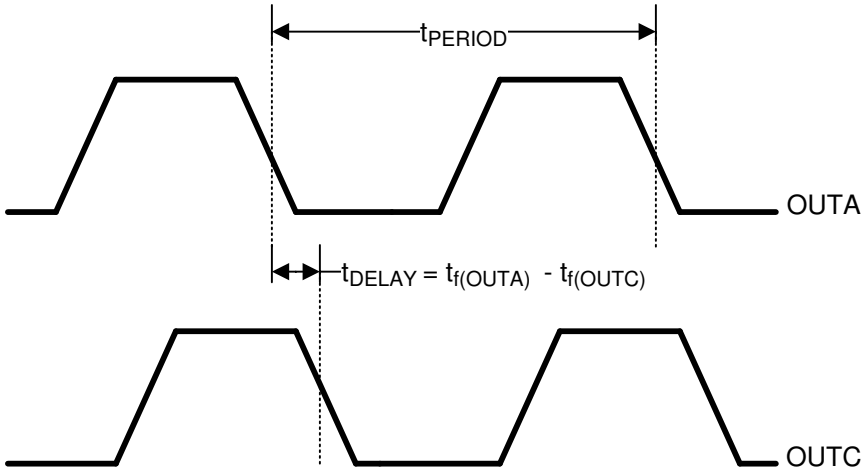


Figure 1. Same Applies to OUTB and OUTD

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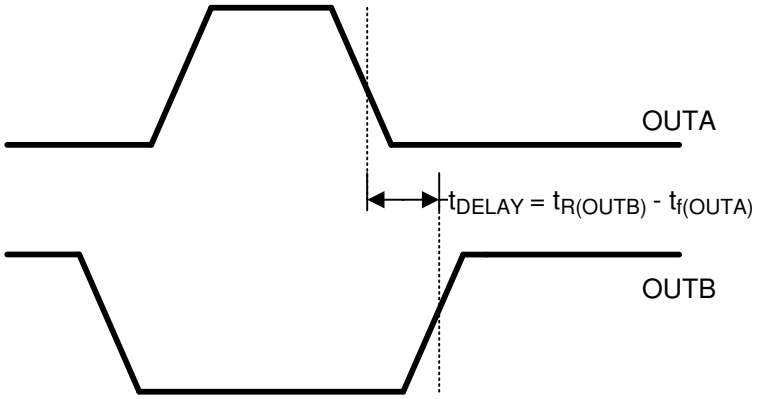


Figure 2. Same Applies to OUTC and OUTD

6.6 Typical Characteristics

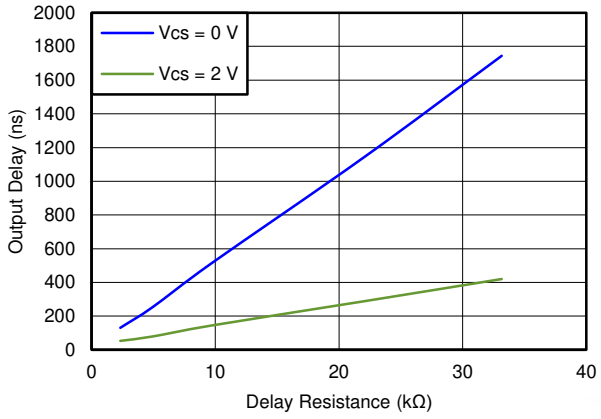


Figure 3. Output Delay (tDELAY) vs Delay Resistance (RDEL)

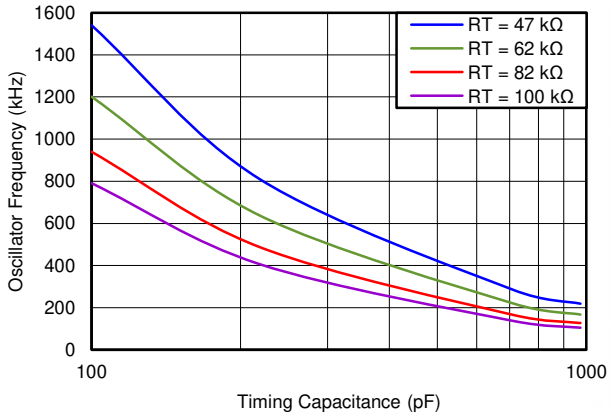


Figure 4. Oscillator Frequency (fSW) vs Timing Capacitance (CT)

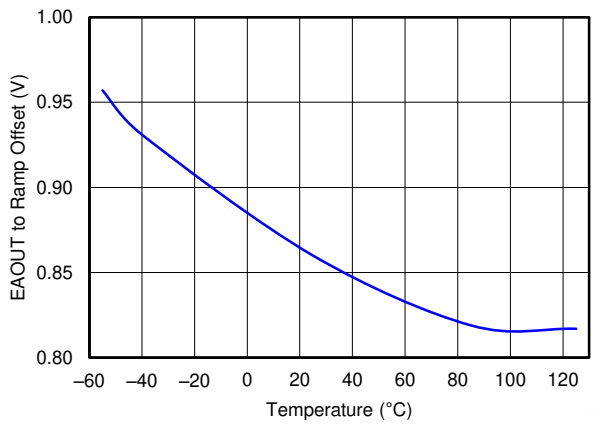


Figure 5. EAOUT to Ramp Offset (VOFFSET) vs Temperature (TA)

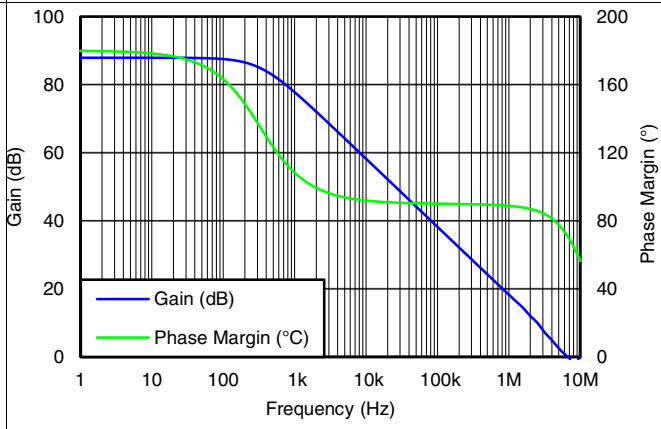


Figure 6. Amplifier Gain and Phase Margin vs Frequency (fOSC)

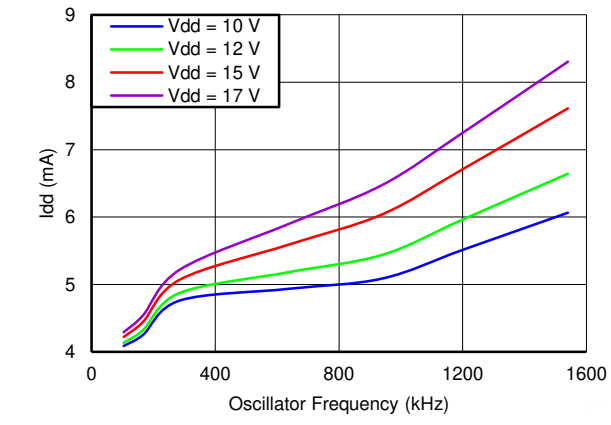


Figure 7. Input Current (IDD) vs Oscillator Frequency (fOSC)

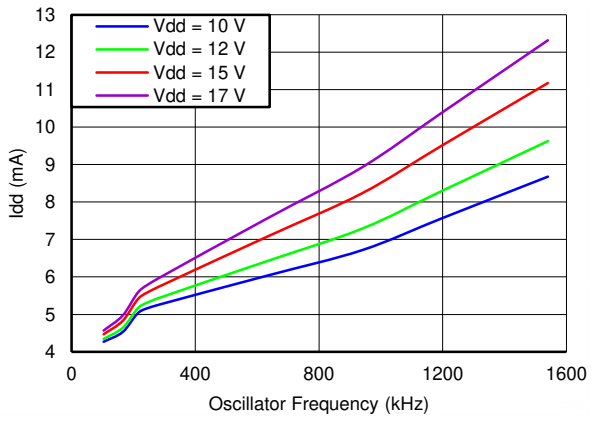


Figure 8. Input Current (IDD) vs Oscillator Frequency (fOSC)

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7 Detailed Description

7.1 Overview

The UCC3895 device combines all the functions necessary to control a phase-shifted full bridge power stage in a 20-pin package. It includes all the outputs needed to drive the four switches in the full-bridge circuit. The dead times between the upper and lower switches in the full bridge may be set using the DELAB and DELCD inputs. Further, this dead time may be dynamically adjusted according to the load level using the ADS pin allowing the user to optimize the dead time for their particular power circuit and to achieve ZVS over the entire operating range. At light loads a no-load comparator forces cycle skipping to maintain output voltage regulation. At higher-power levels, two or more UCC3895 devices may be easily synchronized for parallel operation. The SS/DISB input may be used to set the length of the soft-start process and to turn the controller on and off. The controller may be used in Voltage mode or Current mode control and cycle-by-cycle current limiting is provided in both modes. The switching frequency may be set over a wide range making this device suited to both IGBT and MOSFET based designs.

7.2 Functional Block Diagrams

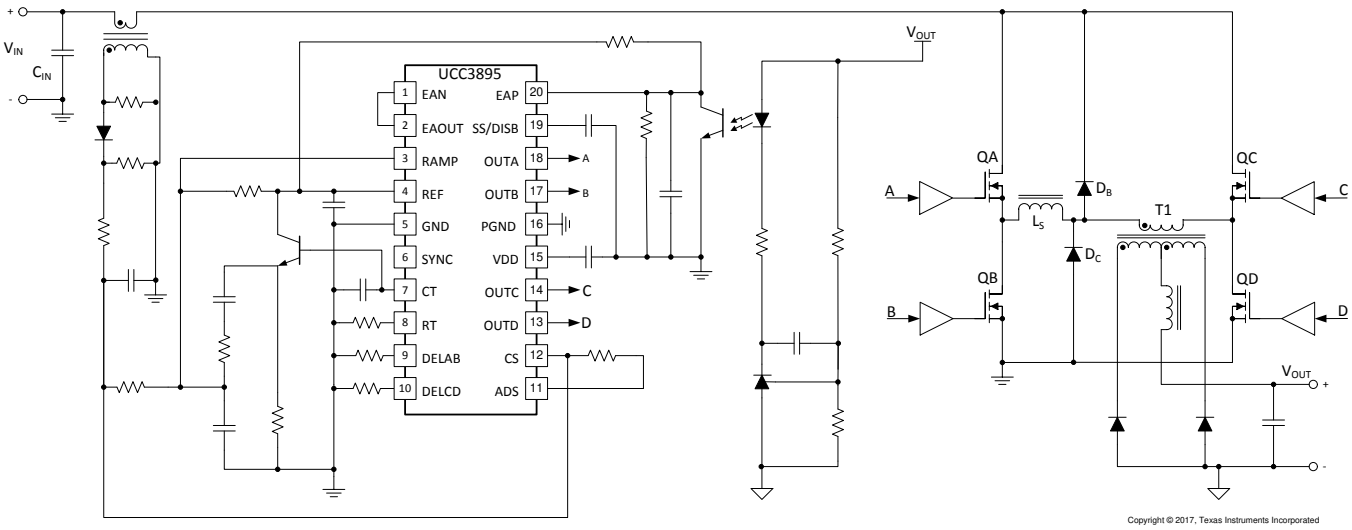
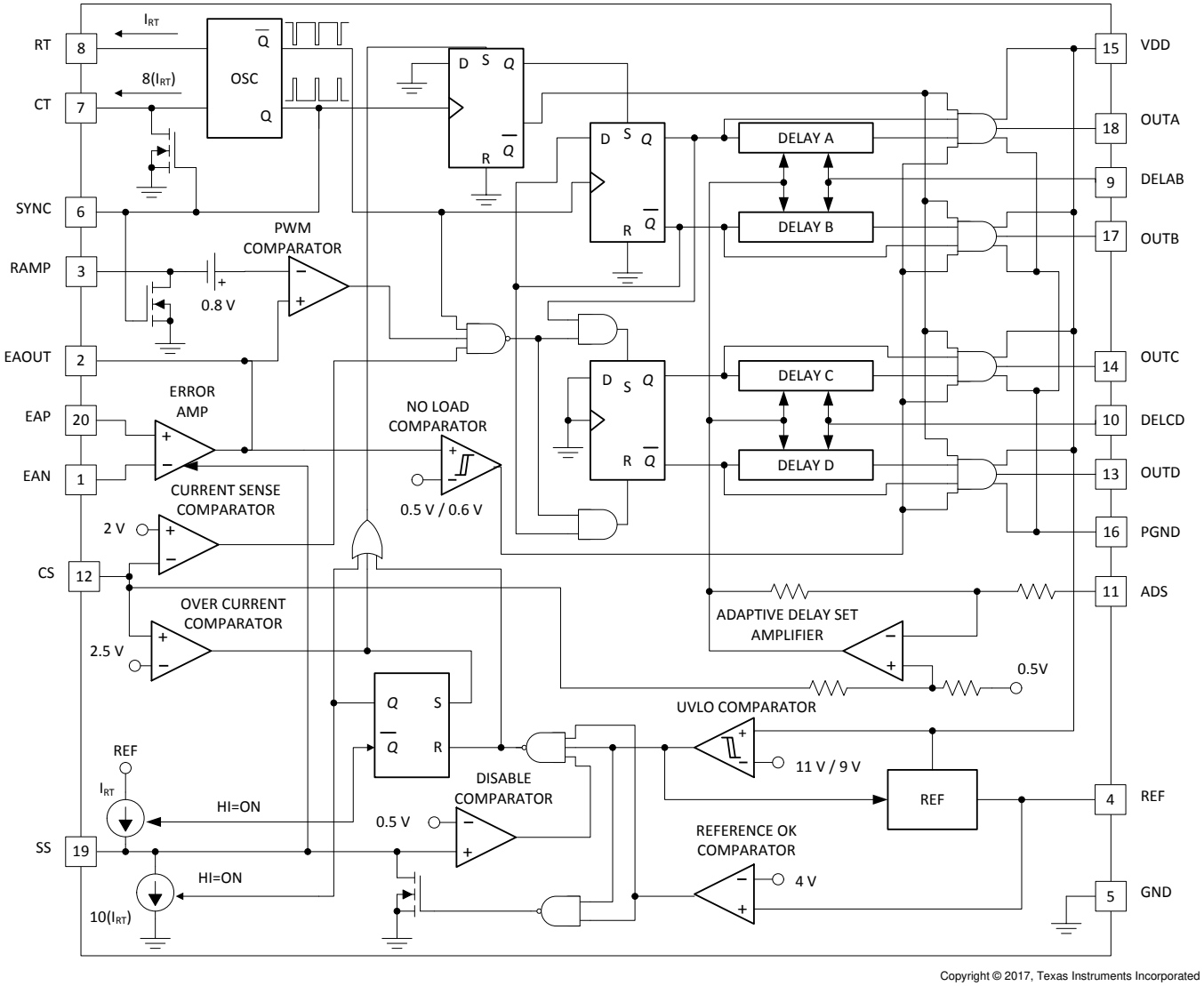


Figure 9. Simplified Application Diagram

Functional Block Diagrams (continued)



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Figure 10. Block Diagram

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Functional Block Diagrams (continued)

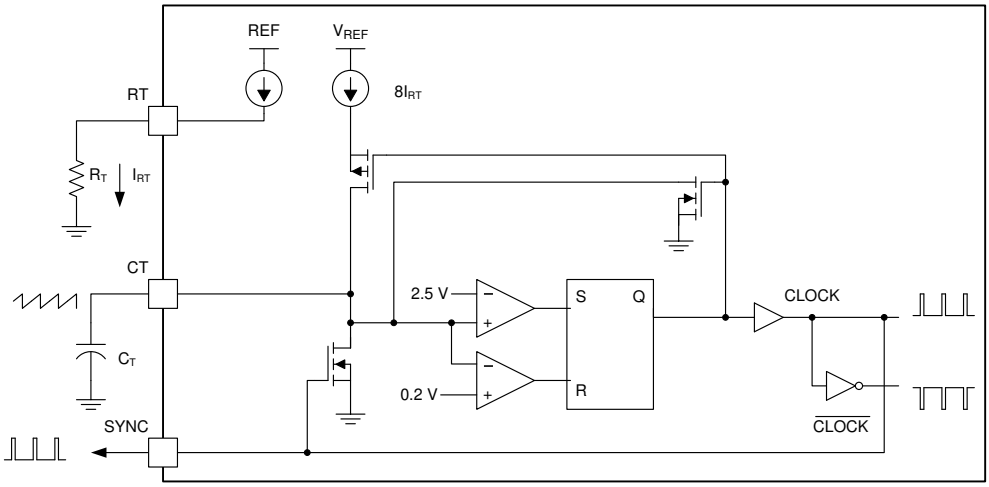


Figure 11. Oscillator Block Diagram

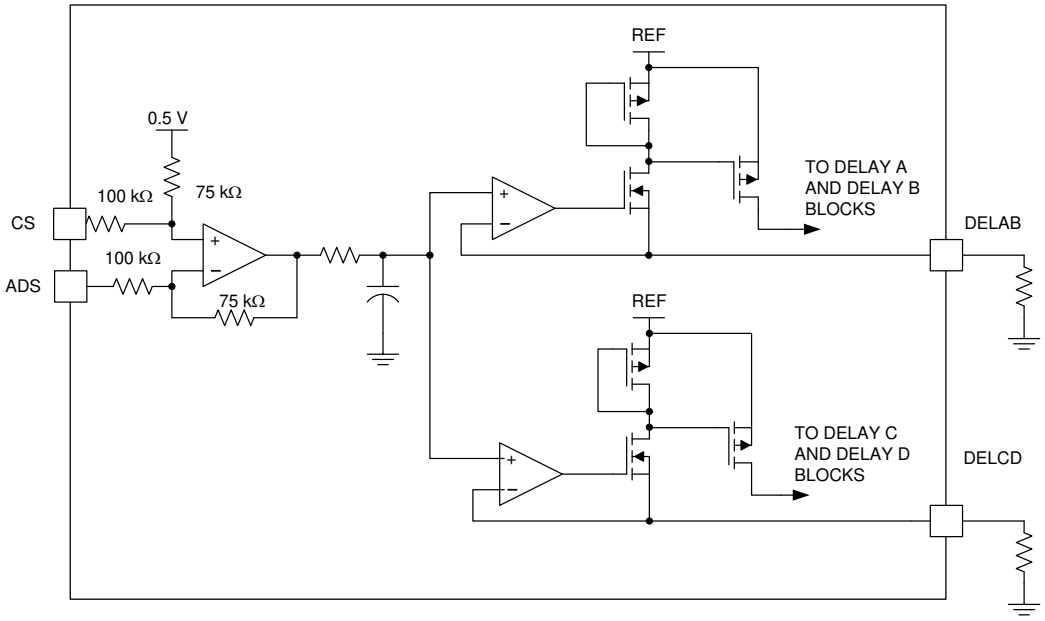


Figure 12. Adaptive Delay Set Block Diagram

Functional Block Diagrams (continued)

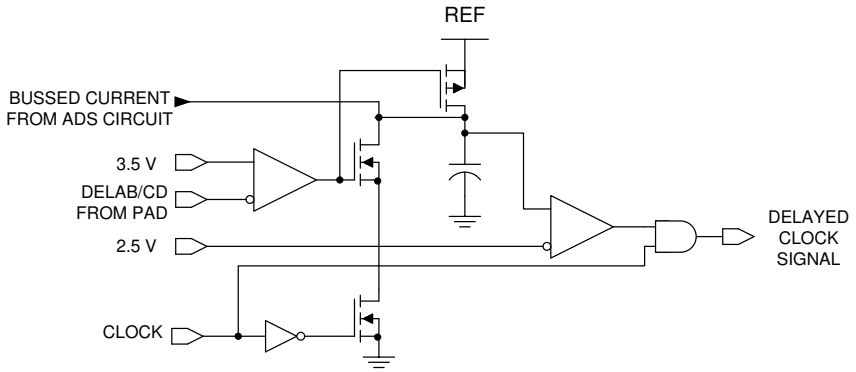


Figure 13. Delay Block Diagram (One Delay Block Per Outlet)

7.3 Feature Description

7.3.1 ADS (Adaptive Delay Set)

This function sets the ratio between the maximum and minimum programmed output-delay dead time. When the ADS pin is directly connected to the CS pin, no delay modulation occurs. The maximum delay modulation occurs when ADS is grounded. In this case, delay time is four-times longer when CS = 0 than when CS = 2 V (the peak-current threshold), ADS changes the output voltage on the delay pins DELAB and DELCD by Equation 1.

$$V_{DEL} = \left[0.75 \times \left(V_{CS} - V_{ADS}\right)\right] + 0.5\ V \quad (1)$$

where

- V_{CS} and V_{ADS} are in volts

ADS must be limited to between 0 V and 2.5 V and must be less-than or equal-to CS. DELAB and DELCD are clamped to a minimum of 0.5 V.

7.3.2 CS (Current Sense)

The CS input connects to the inverting input of the current-sense comparator and the non-inverting input of the overcurrent comparator and the ADS amplifier. The current sense signal is used for cycle-by-cycle current limiting in peak current-mode control, and for overcurrent protection in all cases with a secondary threshold for output shutdown. An output disable initiated by an overcurrent fault also results in a restart cycle, called soft stop, with full soft start.

7.3.3 CT (Oscillator Timing Capacitor)

The UCC3895 oscillator charges CT via a programmed current. The waveform on C_T is a sawtooth, with a peak voltage of 2.35 V. The approximate oscillator period is calculated by Equation 2.

$$t_{OSC} = \frac{5 \times R_T \times C_T}{48} + 120\ ns \quad (2)$$

where

- C_T is in Farads
- R_T is in Ohms
- t_{OSC} is in seconds
- C_T can range from 100 to 880 pF

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Feature Description (continued)

NOTE

A large C_T and a small R_T combination results in extended fall times on the C_T waveform. The increased fall time increases the SYNC pulse width, hence limiting the maximum phase shift between OUTA, OUTB and OUTC, OUTD outputs, which limits the maximum duty cycle of the converter (see Figure 11).

7.3.4 DELAB and DELCD (Delay Programming Between Complementary Outputs)

DELAB programs the dead time between switching of OUTA and OUTB. DELCD programs the dead time between OUTC and OUTD. This delay is introduced between complementary outputs in the same leg of the external bridge. The UCC3895 allows the user to select the delay, in which the resonant switching of the external power stages takes place. Separate delays are provided for the two half-bridges to accommodate differences in resonant-capacitor charging currents. The delay in each stage is set according to Equation 3.

$$t_{DELAY} = \frac{\left(25 \times 10^{-12}\right) \times R_{DEL}}{V_{DEL}} + 25\ ns \quad (3)$$

where

- V_{DEL} is in volts
- R_{DEL} is in Ohms
- t_{DELAY} is in seconds

DELAB and DELCD source about 1-mA maximum. Choose the delay resistors so that this maximum is not exceeded. Programmable output delay is defeated by tying DELAB and, or, DELCD to REF. For an optimum performance keep stray capacitance on these pins at less than 10 pF.

7.3.5 EAOUT, EAP, and EAN (Error Amplifier)

EAOUT connects internally to the non-inverting input of the PWM comparator and the no-load comparator. EAOUT is internally clamped to the soft-start voltage. The no-load comparator shuts down the output stages when EAOUT falls below 500 mV, and allows the outputs to turn on again when EAOUT rises above 600 mV.

EAP is the non-inverting and the EAN is the inverting input to the error amplifier.

7.3.6 OUTA, OUTB, OUTC, and OUTD (Output MOSFET Drivers)

The four outputs are 100-mA complementary MOS drivers, and are optimized to drive MOSFET driver circuits. OUTA and OUTB are fully complementary, (assuming no programming delay) and operate near 50% duty cycle and one-half the oscillator frequency. OUTA and OUTB are intended to drive one half-bridge circuit in an external power stage. OUTC and OUTD drive the other half-bridge and have the same characteristics as OUTA and OUTB. OUTC is phase shifted with respect to OUTA, and OUTD is phase shifted with respect to OUTB.

NOTE

Changing the phase relationship of OUTC and OUTD with respect to OUTA and OUTB requires other than the nominal 50% duty ratio on OUTC and OUTD during those transients.

7.3.7 PGND (Power Ground)

To keep output switching noise from critical analog circuits, the UCC3895 has two different ground connections. PGND is the ground connection for the high-current output stages. Both GND and PGND must be electrically tied together. Also, because PGND carries high current, board traces must be low impedance.

7.3.8 RAMP (Inverting Input of the PWM Comparator)

This pin receives either the C_T waveform in voltage and average current-mode controls, or the current signal (plus slope compensation) in peak current-mode control.

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Feature Description (continued)

7.3.9 REF (Voltage Reference)

The 5-V ± 1.2% reference supplies power to internal circuitry, and also supplies up to 5 mA to external loads. The reference is shutdown during undervoltage lockout but is operational during all other disable modes. For best performance, bypass with a 0.1-μF low-ESR low-ESL capacitor to GND. To ensure the stability of the internal reference, do not use more than 1 μF of total capacitance on this pin for the UCC1895.

For the UCC2895 and the UCC3895, this capacitance increases as per the limits defined in the *Recommended Operating Conditions* of this specification.

7.3.10 RT (Oscillator Timing Resistor)

The oscillator in the UCC3895 operates by charging an external timing capacitor, C_T, with a fixed current programmed by R_T. R_T current is calculated with Equation 4.

$$I_{RT}(A) = \frac{3\ V}{R_T(\Omega)} \tag{4}$$

R_T ranges from 40 kΩ to 120 kΩ. Soft-start charging and discharging currents are also programmed by I_{RT} (Refer to Figure 11).

7.3.11 GND (Analog Ground)

This pin is the chip ground for all internal circuits except the output stages.

7.3.12 SS/DISB (Soft Start/Disable)

This pin combines two independent functions.

Disable Mode: A rapid shutdown of the chip is accomplished by externally forcing SS/DISB below 0.5 V, externally forcing REF below 4 V, or if VDD drops below the undervoltage lockout threshold. In the case of REF being pulled below 4 V or an undervoltage condition, SS/DISB is actively pulled to ground via an internal MOSFET switch.

If an overcurrent fault is sensed (CS = 2.5 V), a soft stop is initiated. In this mode, SS/DISB sinks a constant current of (10 × I_{RT}). The soft stop continues until SS/DISB falls below 0.5 V. When any of these faults are detected, all outputs are forced to ground immediately.

NOTE

If SS/DISB is forced below 0.5 V, the pin starts to source current equal to I_{RT}. The only time the part switches into low I_{DD} current mode, though, is when the part is in undervoltage lockout.

Soft Start Mode: After a fault or disable condition has passed, VDD is above the start threshold, and, or, SS/DISB falls below 0.5 V during a soft stop, SS/DISB switches to a soft-start mode. The pin then sources current, equal to I_{RT}. A user-selected resistor/capacitor combination on SS/DISB determines the soft-start time constant.

NOTE

SS/DISB actively clamps the EAOUT pin voltage to approximately the SS/DISB pin voltage during soft-start, soft-stop, and disable conditions.

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Feature Description (continued)

7.3.13 SYNC (Oscillator Synchronization)

This pin is bidirectional (refer to Figure 11). When used as an output, SYNC is used as a clock, which is the same as the internal clock of the device. When used as an input, SYNC overrides the internal oscillator of the chip and acts as the clock signal. This bidirectional feature allows synchronization of multiple power supplies. Also, the SYNC signal internally discharge the C_T capacitor and any filter capacitors that are present on the RAMP pin. The internal SYNC circuitry is level sensitive, with an input-low threshold of 1.9 V, and an input-high threshold of 2.1 V. A resistor as small as 3.9 kΩ may be tied between SYNC and GND to reduce the sync pulse width.

7.3.14 VDD (Chip Supply)

This is the input pin to the chip. VDD must be bypassed with a minimum of 1-μF low ESR, low ESL capacitor to ground. The addition of a 10-μF low ESR, low ESL between VDD and PGND is recommended.

7.4 Device Functional Modes

The UCC3895 has a number of operational modes. These modes are described in detail in *Feature Description* section.

- Current mode - The UCC3895 device may be operated in current mode control. The CS pin is connected to the current sense signal plus slope compensation. The RAMP pin is connected to the CS pin.
- Voltage mode - The UCC3895 may be operated in voltage mode control. The RAMP pin is connected to the signal at CT.
- Light load mode - Under light load conditions the signal at the EAOUT pin can fall below the threshold of the No-Load-Comparator. When this happens the UCC3895 maintains output regulation by skipping cycles.
- Synchronized mode - Multiple UC3895 devices may be synchronised to each other or to an external clock signal.
- Disable mode - The device will stop if the EN/DISB pin is pulled below 0.5 V.
- Soft-start mode - This mode protects the power stage from excessive stresses during the start-up process.

7.5 Programming

7.5.1 Programming DELAB, DELCD and the Adaptive Delay Set

The UCC3895 allows the user to set the delay between switch commands within each leg of the full-bridge power circuit according to Equation 5.

$$t_{DELAY} = \frac{\left(25 \times 10^{-12}\right) \times R_{DEL}}{V_{DEL}} + 25\ ns \tag{5}$$

From Equation 5 VDEL is determined in conjunction with the desire to use (or not) the ADS feature from Equation 6.

$$V_{DEL} = \left[0.75 \times \left(V_{CS} - V_{ADS}\right)\right] + 0.5\ V \tag{6}$$

Figure 14 illustrates the resistors needed to program the delay periods and the ADS function.

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Programming (continued)

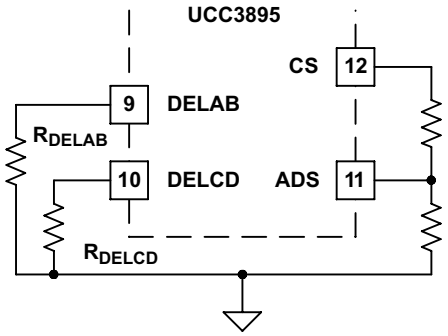


Figure 14. Programming Adaptive Delay Set

The ADS allows the user to vary the delay times between switch commands within each of the two legs of the converter. The delay-time modulation is implemented by connecting ADS (pin 11) to CS, GND, or a resistive divider from CS through ADS to GND to set V_{ADS} as shown in Figure 14. From Equation 6 for V_{DEL}, if ADS is tied to GND then V_{DEL} rises in direct proportion to V_{CS}, causing a decrease in t_{DELAY} as the load increases. In this condition, the maximum value of V_{DEL} is 2 V.

If ADS is connected to a resistive divider between CS and GND, the term (V_{CS} – V_{ADS}) becomes smaller, reducing the level of V_{DEL}. This reduction decreases the amount of delay modulation. In the limit of ADS tied to CS, V_{DEL} = 0.5 V and no delay modulation occurs. Figure 15 graphically shows the delay time versus load for varying adaptive delay set feature voltages (V_{ADS}).

In the case of maximum delay modulation (ADS = GND), when the circuit goes from light load to heavy load, the variation of V_{DEL} is from 0.5 to 2 V. This change causes the delay times to vary by a 4:1 ratio as the load is changed.

The ability to program an adaptive delay is a desirable feature because the optimum delay time is a function of the current flowing in the primary winding of the transformer, and changes by a factor of 10:1 or more as circuit loading changes. Reference 7 (see the *Related Documentation* section) describes the many interrelated factors for choosing the optimum delay times for the most efficient power conversion, and illustrates an external circuit to enable ADS using the UC3879. Implementing this adaptive feature is simplified in the UCC3895 controller, giving the user the ability to tailor the delay times to suit a particular application with a minimum of external parts.

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Programming (continued)

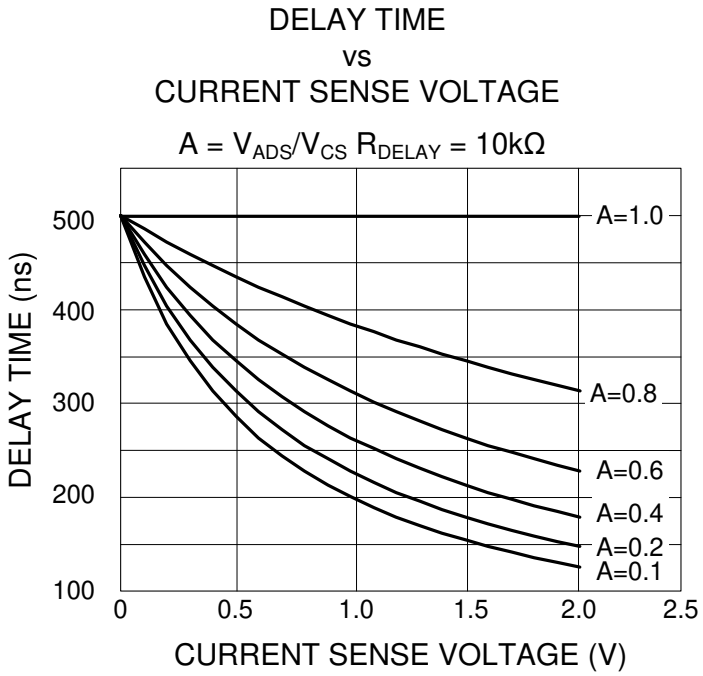
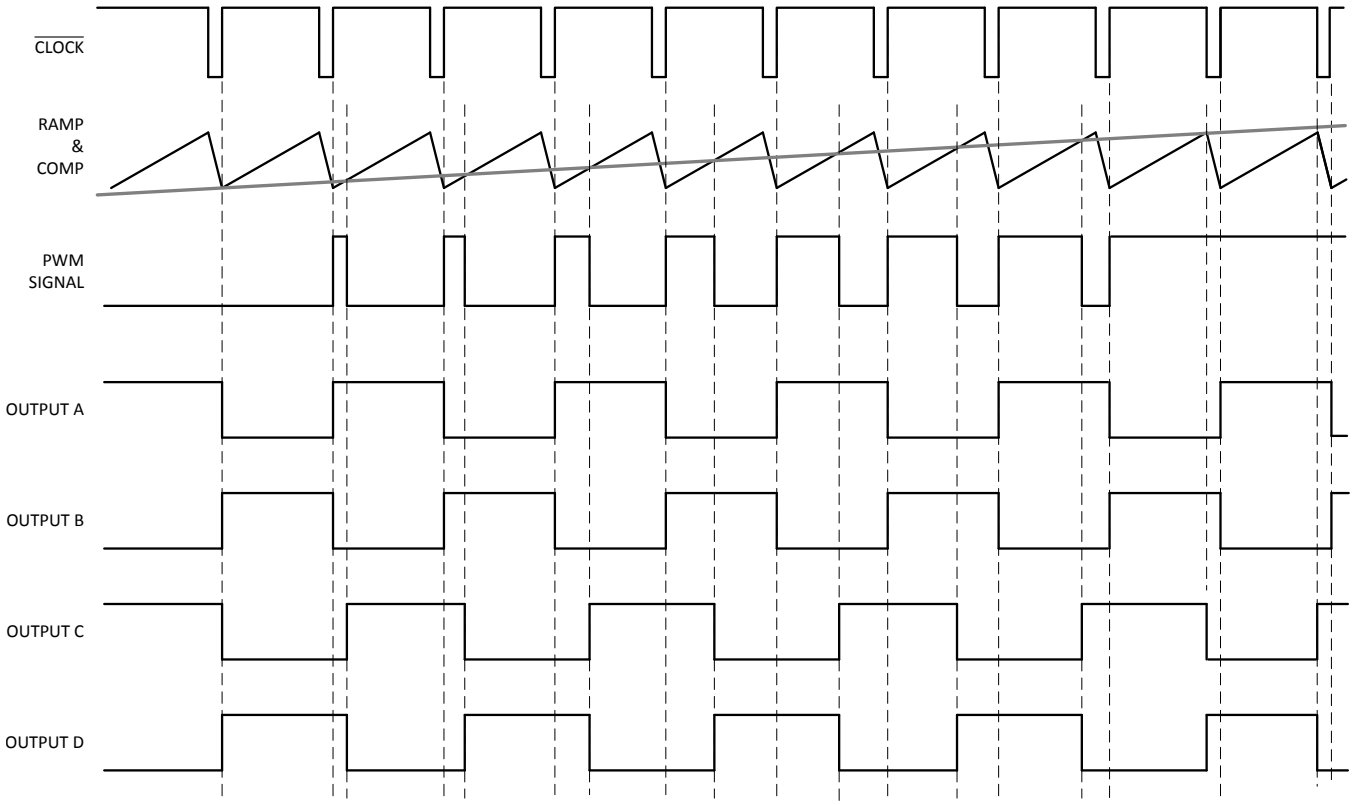


Figure 15. Delay Time Under Varying ADS Voltages



No Output Delay Shown, COMP to RAMP offset not included.

Figure 16. UCC3895 Timing Diagram

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

A simplified electrical diagram of this converter is shown in Figure 18. The controller device is located on the primary side of converter to allow easy bias power generation.

The power stage includes primary side MOSFETs, QA, QB, QC and QD. Diode rectification is used here for simplicity but synchronous rectification is also possible and is described in application notes SLUU109 *Using the UCC3895 in a Direct Control Driven Synchronous Rectifier Applications* and SLUA287 *Control Driven Synchronous Rectifiers In Phase Shifted Full Bridge Converters*. The centre-tapped rectifier scheme with L-C output filter is a popular choice for the 12-V output converters in server power supplies.

The major waveforms of the phase-shifted converter during normal operation are shown in Figure 17. The upper four waveforms show the output drive signals of the controller. Current, I_{PR}, is the current flowing through the primary winding of the power transformer. The bottom two waveforms show the voltage at the output inductor, V_{LOUT}, and the current through the output inductor, I_{LOUT}. ZVS is an important feature for high input voltage converters in reducing switching losses associated with the internal parasitic capacitances of power switches and transformers. The controller ensures ZVS conditions over the entire load current range by adjusting the delay time between the primary MOSFETs switching in the same leg in accordance to the load variation. At light loads the output of the error amplifier (EAOUT) will drop below the threshold of the No-Load Comparator and the controller will enter a pulse skipping mode.

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Application Information (continued)

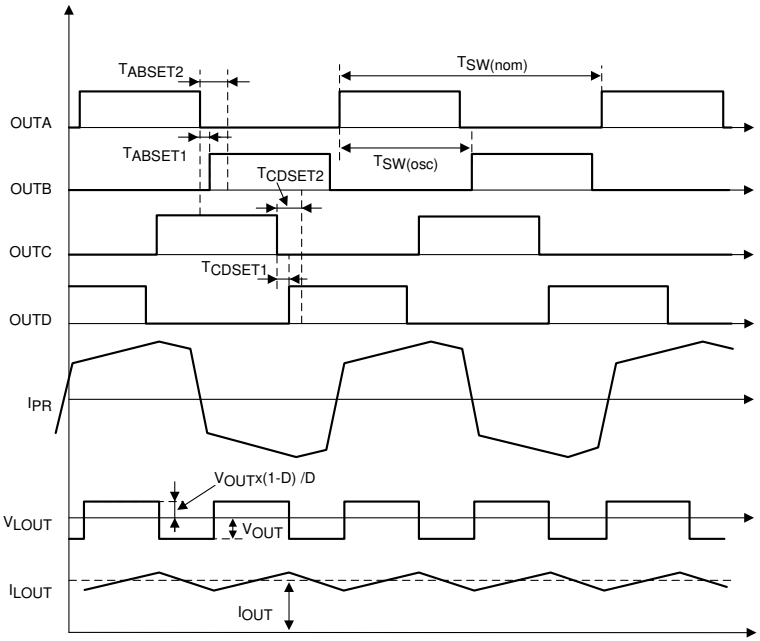


Figure 17. Major Waveforms of Phase-Shifted Converter

8.2 Typical Application

A typical application for the UCC3895 device is a controller for a phase-shifted full-bridge converter that converts a 390-V_{DC} input to a regulated 12-V output.

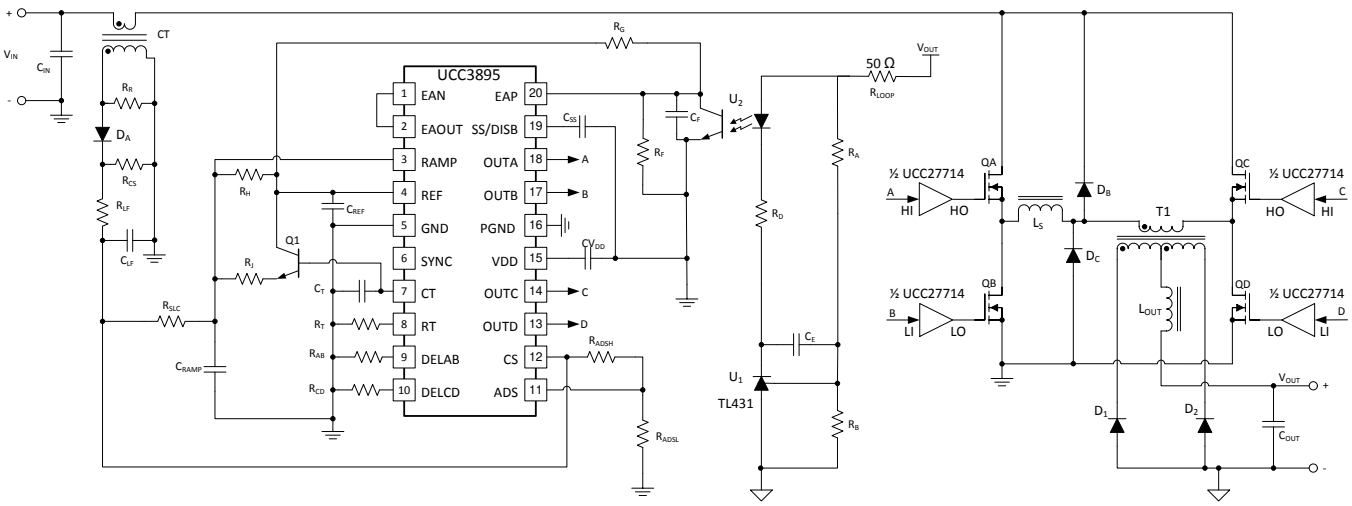


Figure 18. UCC3895 Typical Application

8.2.1 Design Requirements

Table 1 lists the requirements for this application.

Table 1. UCC3895 Typical Application Design Requirements

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
V_{IN}	DC input voltage range		370	390	410	V
$I_{IN(max)}$	Maximum input current	V_{IN}= 370 V_{DC} to 410 V_{DC}			2	A
OUTPUT CHARACTERISTICS						
V_{OUT}	Output voltage	V_{IN}= 370 V_{DC} to 410 V_{DC}	11.4	12	12.6	V
I_{OUT}	Output current	V_{IN}= 370 V_{DC} to 410 V_{DC}			50	A
	Output voltage transient	90% load step		600		mV
P_{OUT}	Continuous output power	V_{IN}= 370 V_{DC} to 410 V_{DC}			600	W
	Load regulation	V_{IN} = 370 V_{DC} to 410 V_{DC}, I_{OUT}= 5 A to 50 A			140	mV
	Line regulation	V_{IN} = 370 V_{DC} to 410 V_{DC}, I_{OUT}= 5 A to 50 A			140	mV
	Output ripple voltage	V_{IN} = 370 V_{DC} to 410 V_{DC}, I_{OUT}= 5 A to 50 A			200	mV
SYSTEM						
F_{SW}	Switching frequency			100		kHz
	Full-load efficiency	V_{IN}= 370 V_{DC} to 410 V_{DC}, P_{OUT}= 500 W	92%	93%		

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8.2.2 Detailed Design Procedure

The phase-shifted full-bridge converter topology is well suited to high-power server applications. This is because the phase-shifted, full-bridge converter can obtain zero-voltage switching on the primary side of the converter, reducing switching losses and EMI and increasing overall efficiency. This is a review of the design of a 600-W, phase-shifted, full-bridge converter for one of these power systems using TI's UCC3895 device. The review is based on typical values. In a production design, the values may need to be modified for worst-case conditions.

NOTE

F_{SW} refers to the switching frequency applied to the power transformer. The oscillator on the UCC2895 is set to 2 × F_{SW}. The output inductor also experiences a switching frequency which is 2 × F_{SW}.

8.2.2.1 Power Loss Budget

To meet the efficiency goal a power loss budget needs to be set.

$$P_{BUDGET} = P_{OUT} \times \left(\frac{1-\eta}{\eta} \right) \approx 52W \tag{7}$$

8.2.2.2 Preliminary Transformer Calculations (T1)

Transformer turns ratio (a1):

$$a1 = \frac{N_P}{N_S} \tag{8}$$

The voltage drop across the $R_{DS(on)}$ of the primary side FETs is negligible. We assume a 0.5-V forward voltage drop in the output rectifiers.

$$V_f = 0.45V \tag{9}$$

Select transformer turns based on 70% duty cycle (D_{MAX}) at minimum specified input voltage. This will give some room for dropout if a PFC front end is used.

$$a1 = \frac{N_P}{N_S} \tag{10}$$

$$a1 = \frac{V_{INMIN} \times D_{MAX}}{V_{OUT} - V_f} \approx 21 \tag{11}$$

Turns ratio rounded to the nearest whole turn.

$$a1 = 21 \tag{12}$$

Calculated typical duty cycle (D_{TYP}) based on average input voltage.

$$D_{TYP} = \frac{(V_{OUT} + V_f) \times a1}{V_{IN}} \approx 0.66 \tag{13}$$

Output inductor peak-to-peak ripple current is set to 20% of the output current.

$$\Delta I_{LOUT} = \frac{P_{OUT} \times 0.2}{V_{OUT}} = 10\,A \tag{14}$$

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Care must be taken in selecting the correct amount of magnetizing inductance (L_{MAG}). The following equations calculate the minimum magnetizing inductance of the primary of the transformer (T1) to ensure the converter operates in current-mode control. As L_{MAG} reduces, the increasing magnetizing current becomes an increasing proportion of the signal at the CS pin. If the magnetizing current increases enough it can swamp out the current sense signal across R_{CS} and the converter will operate increasingly as if it were in voltage mode control rather than current mode.

$$L_{MAG} \geq \frac{V_{IN} \times (1 - D_{TYP})}{\frac{\Delta I_{LOUT} \times 0.5}{a1} \times 2 \times F_{SW}} \approx 2.78\,mH \quad (15)$$

Figure 19 shows the transformer primary and secondary currents during normal operation.

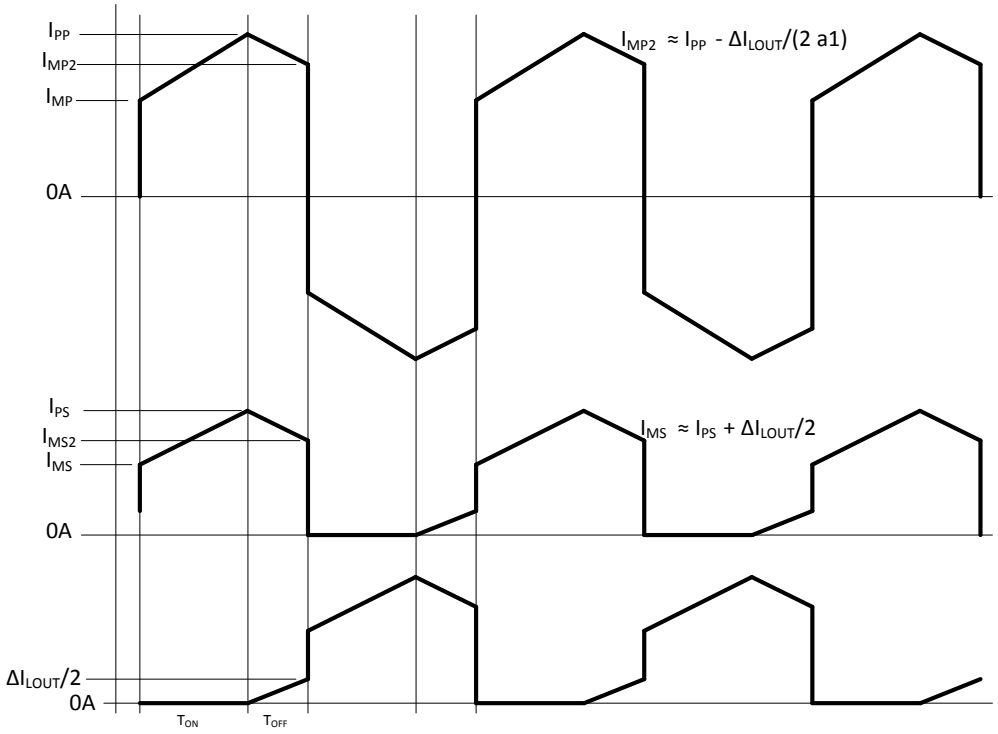


Figure 19. T1 Primary and Secondary Currents

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Calculate T1 secondary RMS current (I_{SRMS}):

$$I_{PS} = \frac{P_{OUT}}{V_{OUT}} + \frac{\Delta I_{LOUT}}{2} \approx 55\,A \quad (16)$$

$$I_{MS} = \frac{P_{OUT}}{V_{OUT}} - \frac{\Delta I_{LOUT}}{2} \approx 45\,A \quad (17)$$

$$I_{MS2} = I_{PS} - \frac{\Delta I_{LOUT}}{2} \approx 50\,A \quad (18)$$

Secondary RMS current (I_{SRMS1}) when energy is being delivered to the secondary: (OUTA = OUTD = HI or OUTB = OUTC = HI).

$$I_{SRMS1} = \sqrt{\left(\frac{D_{MAX}}{2}\right)\left[I_{PS} \times I_{MS} + \frac{\left(I_{PS} - I_{MS}\right)^2}{3}\right]} \approx 29.6\,A \quad (19)$$

Secondary RMS current (I_{SRMS2}) during freewheeling period: (OUTA = OUTC = HI or OUTB = OUTD = HI).

$$I_{SRMS2} = \sqrt{\left(\frac{1 - D_{MAX}}{2}\right)\left[I_{PS} \times I_{MS2} + \frac{\left(I_{PS} - I_{MS2}\right)^2}{3}\right]} \approx 20.3\,A \quad (20)$$

Secondary RMS current (I_{SRMS3}) caused by the negative current in the opposing winding during freewheeling period, please refer to Figure 19.

$$I_{SRMS3} = \frac{\Delta I_{LOUT}}{2}\sqrt{\left(\frac{1 - D_{MAX}}{2 \times 3}\right)} \approx 1.1A \quad (21)$$

Total secondary RMS current (I_{SRMS}):

$$I_{SRMS} = \sqrt{I_{SRMS1}^{\,2} + I_{SRMS2}^{\,2} + I_{SRMS3}^{\,2}} \approx 36.0\,A \quad (22)$$

Calculate T1 Primary RMS Current (I_{PRMS}):

$$\Delta I_{LMAG} = \frac{V_{INMIN} \times D_{MAX}}{L_{MAG} \times 2 \times F_{SW}} \approx 0.47\,A \quad (23)$$

$$I_{PP} = \left(\frac{P_{OUT}}{V_{OUT} \times \eta} + \frac{\Delta I_{LOUT}}{2}\right)\frac{1}{a1} + \Delta I_{LMAG} \approx 3.3\,A \quad (24)$$

$$I_{MP} = \left(\frac{P_{OUT}}{V_{OUT} \times \eta} - \frac{\Delta I_{LOUT}}{2}\right)\frac{1}{a1} + \Delta I_{LMAG} \approx 2.8A \quad (25)$$

$$I_{PRMS1} = \sqrt{(D_{MAX})\left[I_{PP} \times I_{MP} + \frac{\left(I_{PP} - I_{MP}\right)^2}{3}\right]} \approx 2.5\,A \quad (26)$$

$$I_{MP2} = I_{PP} - \left(\frac{\Delta I_{LOUT}}{2}\right)\frac{1}{a1} \approx 3.0\,A \quad (27)$$

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T1 Primary RMS (I_{PRMS1}) current when energy is being delivered to the secondary.

$$I_{PRMS1} = \sqrt{(D_{MAX})\left[I_{PP} \times I_{MP} + \frac{(I_{PP} - I_{MP})^2}{3}\right]} \approx 2.5\,A \tag{28}$$

T1 Primary RMS (I_{PRMS2}) current when the converter is free wheeling.

$$I_{PRMS2} = \sqrt{(1 - D_{MAX})\left[I_{PP} \times I_{MP2} + \frac{(I_{PP} - I_{MP2})^2}{3}\right]} \approx 1.7\,A \tag{29}$$

Total T1 primary RMS current (I_{PRMS}):

$$I_{PRMS} = \sqrt{I_{PRMS1}^{\ 2} + I_{PRMS2}^{\ 2}} \approx 3.1A \tag{30}$$

We select a transformer with the following specifications:

$$a1 = 21 \tag{31}$$

$$L_{MAG} = 2.8\,mH \tag{32}$$

Transformer Primary DC resistance:

$$DCR_P = 0.215\,\Omega \tag{33}$$

Transformer Secondary DC resistance:

$$DCR_S = 0.58\,\Omega \tag{34}$$

Estimated transformer core losses (P_{T1}) are twice the copper loss.

NOTE

This is just an estimate and the total losses may vary based on magnetic design.

$$P_{T1} \approx 2 \times \left(I_{PRMS}^{\ 2} \times DCR_P + 2 \times I_{SRMS}^{\ 2} \times DCR_S\right) \approx 7.0\,W \tag{35}$$

Calculate remaining power budget:

$$P_{BUDGET} = P_{BUDGET} - P_{T1} \approx 45W \tag{36}$$

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8.2.2.3 QA, QB, QC, QD FET Selection

In this design to meet efficiency and voltage requirements 20 A, 650 V, CoolMOS FETs from Infineon are chosen for QA..QD.

FET drain to source on resistance:

$$R_{ds(on)QA} = 0.220\,\Omega \tag{37}$$

FET Specified C_{OSS}:

$$C_{OSS_QA_SPEC} = 780\,pF \tag{38}$$

Voltage across drain-to-source (V_{dsQA}) where C_{OSS} was measured, data sheet parameter:

$$V_{dsQA} = 25\,V \tag{39}$$

Calculate average C_{oss} [2]:

$$C_{OSS_QA_AVG} = C_{OSS_QA_SPEC}\sqrt{\frac{V_{dsQA}}{V_{INMAX}}} \approx 193\,pF \tag{40}$$

QA FET gate charge:

$$QA_g = 15\,nC \tag{41}$$

Voltage applied to FET gate to activate FET:

$$V_g = 12\,V \tag{42}$$

Calculate QA losses (P_{QA}) based on $R_{ds(on)QA}$ and gate charge (QA_g):

$$P_{QA} = I_{PRMS}{}^2 \times R_{DS(on)QA} + 2 \times QA_g \times V_g \times f_{SW} \approx 2.1W \tag{43}$$

Recalculate power budget:

$$P_{BUDGET} = P_{BUDGET} - 4 \times P_{QA} \approx 36.6W \tag{44}$$

8.2.2.4 Selecting L_S

Calculating the value of the shim inductor (L_S) is based on the amount of energy required to achieve zero voltage switching. This inductor needs to able to deplete the energy from the parasitic capacitance at the switch node. The following equation selects L_S to achieve ZVS at 100% load down to 50% load based on the primary FET's average total C_{OSS} at the switch node.

NOTE

The actual parasitic capacitance at the switched node may differ from the estimate and L_S may have to be adjusted accordingly.

$$L_S \geq \left(2 \times C_{OSS_QA_AVG}\right) \frac{V_{INMAX}^{\ 2}}{\left(\frac{I_{PP}}{2} - \frac{\Delta I_{LOUT}}{2 \times a1}\right)^2} - L_{LK} \approx 26\,\mu H \tag{45}$$

$$L_S = 26\,\mu H \tag{46}$$

Typical shim inductor DC resistance:

$$DCR_{LS} = 27\,m\Omega \tag{47}$$

Estimate L_S power loss (P_{LS}) and readjust remaining power budget:

$$P_{LS} = 2 \times I_{PRMS}^{\ 2} \times DCR_{LS} \approx 0.5\,W \tag{48}$$

$$P_{BUDGET} = P_{BUDGET} - P_{LS} \approx 36.1W \tag{49}$$

8.2.2.5 Selecting Diodes D_B and D_C

There is a potential for high voltage ringing on the secondary rectifiers, caused by the difference in current between the transformer and the shim inductor when the transformer comes out of freewheeling. Diodes D_B and D_C provide a path for this current and prevent any ringing by clamping the transformer primary to the primary side power rails. Normally these diodes do not dissipate much power but they should be sized to carry the full primary current. The worse case power dissipated in these diodes is:

$$P = 0.5 \times L_S \times I^2_{PRMS} \times F_{SW} \tag{50}$$

The diodes should be ultra-fast types and rated for the input voltage of the converter – V_{IN} (410 VDC in this case).

A MURS360 part is suitable at this power level.

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8.2.2.6 Output Inductor Selection (L_{OUT})

Inductor L_{OUT} is designed for 20% inductor ripple current (ΔI_{LOUT}):

$$\Delta I_{LOUT} = \frac{P_{OUT} \times 0.2}{V_{OUT}} = \frac{600\,W \times 0.2}{12\,V} \approx 10\,A \quad (51)$$

$$L_{OUT} = \frac{V_{OUT} \times (1 - D_{TYP})}{\Delta I_{LOUT} \times 2 \times f_{SW}} \approx 2\,\mu H \quad (52)$$

Calculate output inductor RMS current (I_{LOUT_RMS}):

$$I_{LOUT_RMS} = \sqrt{\left(\frac{P_{OUT}}{V_{OUT}}\right)^2 + \left(\frac{\Delta I_{LOUT}}{\sqrt{3}}\right)^2} = 50.3\,A \quad (53)$$

$$L_{OUT} = 2\,\mu H \quad (54)$$

Typical output inductor DC resistance:

$$DCR_{LOUT} = 750\,\mu\Omega \quad (55)$$

Estimate output inductor losses (P_{LOUT}) and recalculate power budget. Note P_{LOUT} is an estimate of inductor losses that is twice the copper loss. Note this may vary based on magnetic manufactures. It is advisable to double check the magnetic loss with the magnetic manufacture.

$$P_{LOUT} = 2 \times I_{LOUT_RMS}^2 \times DCR_{LOUT} \approx 3.8\,W \quad (56)$$

$$P_{BUDGET} = P_{BUDGET} - P_{LOUT} \approx 32.8W \quad (57)$$

8.2.2.7 Output Capacitance (C_{OUT})

The output capacitor is selected based on holdup and transient (V_{TRAN}) load requirements.

Time it takes L_{OUT} to change 90% of its full load current:

$$t_{HU} = \frac{\frac{L_{OUT} \times P_{OUT} \times 0.9}{V_{OUT}}}{V_{OUT}} = 7.5\,\mu s \tag{58}$$

During load transients most of the current will immediately go through the capacitors equivalent series resistance (ESR_{COUT}). The following equations are used to select ESR_{COUT} and C_{OUT} based on a 90% load step in current. The ESR is selected for 90% of the allowable transient voltage (V_{TRAN}), while the output capacitance (C_{OUT}) is selected for 10% of V_{TRAN}.

$$ESR_{COUT} \le \frac{V_{TRAN} \times 0.9}{\frac{P_{OUT} \times 0.9}{V_{OUT}}} = 12\,m\Omega \tag{59}$$

$$C_{OUT} \ge \frac{\frac{P_{OUT} \times 0.9 \times t_{HU}}{V_{OUT}}}{V_{TRAN} \times 0.1} \approx 5.6\,mF \tag{60}$$

Before selecting the output capacitor, the output capacitor RMS current (I_{COUT_RMS}) must be calculated.

$$I_{COUT_RMS} = \frac{\Delta I_{LOUT}}{\sqrt{3}} \approx 5.8\,A \tag{61}$$

To meet the design requirements five 1500-µF, aluminum electrolytic capacitors are chosen for the design from United Chemi-Con™, part number EKY-160ELL152MJ30S. These capacitors have an ESR of 31 mΩ.

Number of output capacitors:

$$n = 5 \tag{62}$$

Total output capacitance:

$$C_{OUT} = 1500\,\mu F \times n \approx 7500\,\mu F \tag{63}$$

Effective output capacitance ESR:

$$ESR_{COUT} = \frac{31\,m\Omega}{n} = 6.2\,m\Omega \tag{64}$$

Calculate output capacitor loss (P_{COUT}):

$$P_{COUT} = I_{COUT_RMS}{}^2 \times ESR_{COUT} \approx 0.21W \tag{65}$$

Recalculate remaining Power Budget:

$$P_{BUDGET} = P_{BUDGET} - P_{COUT} \approx 32.6W \tag{66}$$

8.2.2.8 Select Rectifier Diodes

Selecting the rectifier diodes begins with determining the voltage and current ratings necessary. In this case the peak diode reverse voltage is given by:

$$V_r = 2 \times \frac{V_{IN_{MAX}}}{a1} \approx 38V \tag{67}$$

The average output diode current is given by:

$$I_f = \frac{I_{OUT_avg}}{2} \approx 30A \tag{68}$$

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For this design we select dual 40-A, 45-V Schottky diodes type STPS40L45CT. This is a dual diode and we connect both of the diodes in parallel for current sharing. Each diode in the package will carry approximately half of the I_f calculated above, or about 15 A. The forward voltage drop of these diodes at maximum output current will be typically 0.45 V.

The power loss in the output rectifiers is dominated by the $V_f I_f$ product.

The loss in each dual diode package is given by:

$$P_{Diode} = V_f \times I_f \approx 13.5W \tag{69}$$

The device will require a heatsink to keep its junction temperature at a reasonable level.

The heatsink thermal resistance will have to be less than:

$$R_{TH_HSK_D} = \frac{T_{J_max} - T_A}{P_{Diode}} - R_{TH_{JC}} \approx 4.5^{\circ}CW^{-1} \tag{70}$$

where T_{j_max} = 125°C, T_A = 50°C, and R_{TH_jc} = 0.8°CW^{-1}.

A typical heatsink with this thermal resistance would have dimensions 63.5 mm × 42 mm × 25 mm.

Recalculate the power budget.

$$P_{BUDGET} = P_{BUDGET} - 2 \times P_{Diode} \approx 5.6W \tag{71}$$

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8.2.2.9 Input Capacitance (C_{IN})

The input voltage in this design is 390 V_{DC}, which is generally fed by the output of a PFC boost pre-regulator. The input capacitance is generally selected based on holdup and ripple requirements.

NOTE

The delay time needed to achieve ZVS can act as a duty cycle clamp (D_{CLAMP}).

Calculate tank frequency:

$$f_R = \frac{1}{2\pi\sqrt{L_S \times (2 \times C_{OSS_QA_AVG})}} \tag{72}$$

Estimated delay time:

$$t_{DELAY} = \frac{2}{f_R \times 4} \approx 314\,ns \tag{73}$$

Effective duty cycle clamp (D_{CLAMP}):

$$D_{CLAMP} = \left(\frac{1}{2 \times f_{SW}} - t_{DELAY} \right) \times 2 \times f_{SW} = 94\% \tag{74}$$

V_{DROP} is the minimum input voltage where the converter can still maintain output regulation. The converter's input voltage would only drop down this low during a brownout or line-drop condition if this converter was following a PFC pre-regulator.

$$V_{DROP} = \frac{a1 \times (V_{OUT} + V_f)}{D_{CLAMP}} \approx 278V \tag{75}$$

C_{IN} was calculated based on one line cycle of holdup:

$$C_{IN} \geq \frac{2 \times P_{OUT} \times \frac{1}{60\,Hz}}{\left(V_{IN}^2 - V_{DROP}^2\right)} \approx 364\,\mu F \tag{76}$$

Calculate high frequency input capacitor RMS current (I_{CINRMS}).

$$I_{CINRMS} = \sqrt{I_{PRMS1}^2 - \left(\frac{P_{OUT}}{V_{INMIN} \times a1} \right)^2} = 1.8\,A \tag{77}$$

To meet the input capacitance and RMS current requirements for this design a 330-µF capacitor was chosen from Panasonic part number EETHC2W331EA.

$$C_{IN} = 330\,\mu F \tag{78}$$

This capacitor has a high frequency (ESR_{CIN}) of 150 mΩ, measured with an impedance analyzer at 200 kHz.

$$ESR_{CIN} = 0.150\,\Omega \tag{79}$$

Estimate C_{IN} power dissipation (P_{CIN}):

$$P_{CIN} = I_{CINRMS}^2 \times ESR_{CIN} = 0.5\,W \tag{80}$$

Recalculate remaining power budget:

$$P_{BUDGET} = P_{BUDGET} - P_{CIN} \approx 5.0\,W \tag{81}$$

There is roughly 5.0 W left in the power budget left for the current sensing network, and biasing the control device and all resistors supporting the control device.

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8.2.2.10 Current Sense Network (CT, R_{CS}, R_R, D_A)

The CT chosen for this design has a turns ratio (CT_{RAT}) of 100:1.

$$CT_{RAT} = \frac{I_P}{I_S} = 100 \tag{82}$$

Calculate nominal peak current (I_{P1}) at V_{INMIN}:

Peak primary current:

$$I_{P1} = \left(\frac{P_{OUT}}{V_{OUT} \times \eta} + \frac{\Delta I_{LOUT}}{2} \right) \frac{1}{a1} + \frac{V_{INMIN} \times D_{MAX}}{L_{MAG} \times 2 \times F_{SW}} \approx 3.3\,A \tag{83}$$

The CS pin voltage where peak current limit will trip.

$$V_P = 2\,V \tag{84}$$

Calculate current sense resistor (R_{CS}) and leave 300 mV for slope compensation. Include a 1.1 factor for margin:

$$R_{CS} = \frac{V_P - 0.3\,V}{\frac{I_{P1}}{CT_{RAT}} \times 1.1} \approx 47\,\Omega \tag{85}$$

Select a standard resistor for R_{CS}:

$$R_{CS} = 47\,\Omega \tag{86}$$

Estimate power loss for R_{CS}:

$$P_{RCS} = \left(\frac{I_{PRMS1}}{CT_{RAT}} \right)^2 \times R_{CS} \approx 0.03\,W \tag{87}$$

Calculate maximum reverse voltage (V_{DA}) on D_A:

$$V_{DA} = V_P \frac{D_{CLAMP}}{1 - D_{CLAMP}} \approx 29.8\,V \tag{88}$$

Estimate D_A power loss (P_{DA}):

$$P_{DA} = \frac{P_{OUT} \times 0.6\,V}{V_{INMIN} \times \eta \times CT_{RAT}} \approx 0.01W \tag{89}$$

Calculate reset resistor R_R:

Resistor R_R is used to reset the current sense transformer CT.

$$R_R = 100 \times R_{CS} = 4.7k\Omega \tag{90}$$

Resistor R_{LF} and capacitor C_{LF} form a low pass filter for the current sense signal (Pin 15). For this design we chose the following values. This filter has a low frequency pole (f_{LFP}) at 482 kHz. This should work for most applications but may be adjusted to suit individual layouts and EMI present in the design.

$$R_{LF} = 1k\Omega \tag{91}$$

$$C_{LF} = 330\,pF \tag{92}$$

$$f_{LFP} = \frac{1}{2\pi f \times R_{LF} \times C_{LF}} = 482\,kHz \tag{93}$$

The UCC3895 REF output (Pin 4) needs a high frequency bypass capacitor to filter out high frequency noise. The maximum amount of capacitance allowed is given in the *Recommended Operating Conditions*.

$$C_{REF} = 1\,\mu F \tag{94}$$

The voltage amplifier reference voltage (Pin 2, EA+) can be set with a voltage divider (R1, R2), for this design example, the error amplifier reference voltage (V1) will be set to 2.5 V. Select a standard resistor value for R1 and then calculate resistor value R2.

UCC3895 reference voltage:

$$V_{REF} = 5\,V \tag{95}$$

Set voltage amplifier reference voltage:

$$V1 = 2.5\,V \tag{96}$$

$$R1 = 2.37\,k\Omega \tag{97}$$

$$R2 = \frac{R1 \times (V_{REF} - V1)}{V1} = 2.37\,k\Omega \tag{98}$$

Voltage divider formed by resistor R3 and R4 are chosen to set the DC output voltage (V_{OUT}) at Pin 3 (EA–).

Select a standard resistor for R3:

$$R3 = 2.37\,k\Omega \tag{99}$$

Calculate R4:

$$R4 = \frac{R3 \times (V_{OUT} - V1)}{V1} \approx 9\,k\Omega \tag{100}$$

Then choose a standard resistor for R4:

$$R4 = \frac{R3 \times (V_{OUT} - V1)}{V1} \approx 9.09\,k\Omega \tag{101}$$

8.2.2.10.1 Output Voltage Setpoint

Peak current mode control is chosen for this design and a TL431 (U1) acts as the output voltage error amplifier. It has a 2.5-V internal reference and we want to regulate V_{OUT} to 12 V. We set R_B, the lower resistor of the output voltage divider chain to 10 kΩ. R_A the upper resistor is given by:

$$R_A = R_B\left(\frac{V_{OUT}}{V_{REF}} - 1\right) = 38\ k\Omega \tag{102}$$

It is possible, but not necessary, to add a small resistor, R_{LOOP}, in series with the feedback network as a signal injection point for loop stability tests, R_{LOOP}.

The output of U_1 is transferred across the isolation barrier by the optocoupler U_2 and fed into the EAP pin of the UCC3895 as a current demand signal. The UCC2895 internal error amplifier is configured as a voltage follower by connecting EAN to EAOUT.

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8.2.2.10.2 Voltage Loop Compensation

We choose a standard configuration for a TL431 / optocoupler based feedback network. Type 2 loop compensation is appropriate for a design using peak current mode control. First we set the DC operating points for the TL431 (U1) and the optocoupler (U2).

We assume that the optocoupler (U2) has a current transfer ratio (CTR) of 1 and choose to operate it at a maximum LED current, I_F of 10 mA. R_D is then given by:

$$R_D = \frac{V_{OUT} - V_F - V_{k_MIN}}{I_F} \approx 820\ \Omega \tag{103}$$

We set the parallel combination of R_G and R_F to 2.4 kΩ for a nominal 10-dB gain for output perturbations via the direct path from R_D to the optocoupler diode. This path exists in parallel with the path through R_A and the TL431. The direct path is important at frequencies where the gain of the TL431 integrator has fallen to 0 dB.

R_G and R_F form a potential divider whose function is to keep the EAP pin within the upper limit of its common mode input range (V_{CM_MAX} = 3.6 V) when there is no current in the photo-transistor. R_G is connected to VREF and this constraint on the voltage at the EAP pin gives:

$$R_G = R_F \frac{V_{REF}}{V_{CM_MAX}} - 1 = 0.39\, R_F \tag{104}$$

Since we know the parallel value of R_F and R_G and their ratio (R_F/R_G), we calculate RF as follows:

$$R_F = R_F \,||\, R_G \frac{1.39}{0.39} \approx 8.6 k\Omega \tag{105}$$

and

$$R_G = 0.39\ R_F = 3.3\ k\Omega \tag{106}$$

At low frequencies the gain is dominated by the response of the TL431 error amplifier which is configured as a pure integrator. The TL431 has a typical open loop gain of about 60 dB at DC, which decreases at the normal –20 dB per decade. Its gain will be 0 dB when the impedance of CE falls to that of RA. Even though the TL431 gain has fallen to 0 dB, the system still has 10-dB gain due to the direct path through RD.

We put the zero due to capacitor C_E and resistor R_A at the desired 0-dB gain frequency of 2 kHz. Since R_A is already selected from V_{OUT} setpoint considerations we calculate C_E as follows:

$$C_E = \frac{1}{2\pi 2000 Hz 38 k\Omega} \approx 22\ nF \tag{107}$$

The optocoupler has a 10-dB response through the direct path, to perturbations on V_{OUT}. At higher frequencies the capacitance at the collector of the optocoupler (C_F) forms a pole with the resistor in series with the optocoupler LED. The gain then rolls off in half a decade to reach 0 dB. With CF = 68 nF this pole is at about 2.8 kHz.

Having chosen the component values in the feedback path around the TL431 we can draw a Bode Plot of the VOUT to EAP transfer function $G_C(f)$.

The control to output transfer function of the power train is approximated by:

$$G_{CO(f)} = \frac{\Delta V_{OUT}}{\Delta V_C} \approx a1 \times CT_{RAT} \times \frac{R_{LOAD}}{R_{CS}} \times \left(\frac{1 + s\ ESR_{COUT} \times C_{OUT}}{1 + s\ R_{LOAD} \times C_{OUT}} \right) \times \frac{1}{1 + \frac{s}{s_{PP}} + \left(\frac{s}{s_{PP}} \right)^2} \tag{108}$$

where

- s = 2πjf is the complex frequency
- s_{PP} is F_{SW} / 2 = 50 kHz in this case
- The overall loop response is then given by $G_C(f)$. $G_C(o)$.

This loop response has a crossover frequency of 7.5 kHz. TI recommends that you check the loop stability of the final design with load transient tests and by checking that the gain and phase margins are sufficient. R_{LOOP} provides a convenient point to inject signals for loop gain and phase measurements. The feedback network may need to be adjusted to achieve satisfactory performance.

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8.2.2.10.3 Setting the Switching Frequency

In this design we set the UCC2895 oscillator frequency to 200 kHz to give a switching frequency (F_{SW}) of 100 kHz at the transformer primary. We set R_T = 82 kΩ, within the limits given in the *RT (Oscillator Timing Resistor)* section and rearrange Equation 2 to find the needed value of C_T.

$$C_T = \frac{48 \times \left[t_{OSC} - 120ns \right]}{5 \times R_T} \approx 560\ pF \tag{109}$$

This value is within the limits for C_T in the *CT (Oscillator Timing Capacitor)* section.

8.2.2.10.4 Soft Start

$$I_{R_T} = \frac{3\ V}{R_T} \approx 36\ \mu A \tag{110}$$

The UCC3895 has a soft-start function to reduce component stresses during the start-up phase. For this design we set the soft-start time to 50 ms. This time is controlled by the value of the capacitor C_{SS} at the SS/DISB pin and the charging current set by R_T (Equation 4).

$$C_{SS} = I_{RT} \times \frac{t_{SS}}{3.6\ V} = \frac{3\ V}{R_T} \times \frac{t_{SS}}{3.6\ V} \approx 470\ nF \tag{111}$$

8.2.2.10.5 Setting the Switching Delays

Higher power designs will benefit from the adaptive delays provided by the ADS pin but that feature is not used in this example. Setting RADSH = 0 Ω defeats the adaptive delay and a fixed value for t_{DELAB} and t_{DELCD} is used. If it is planned to use the adaptive delay feature then the resistor RADSL should be included in the layout but not populated until delay optimisation is being done on actual hardware.

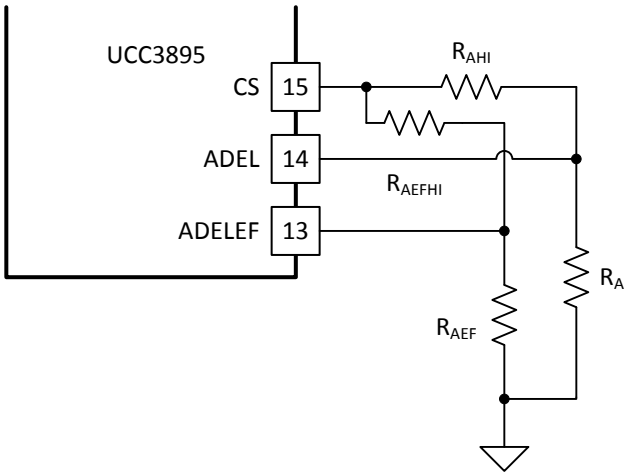


Figure 20. UCC3895 Adaptive Delays

We set the delay times as follows. The resonant frequency of the shim inductor L_S with the stray capacitance at the switched node is given by:

$$f_R = \frac{1}{2\pi\sqrt{L_S \times 2 \times C_{OSS_AVG}}} \approx 1.6\ MHz \tag{112}$$

Set the initial t_{ABSET} and t_{CDSET} values to half the resonant period

$$t_{DELAY} = 314\ ns \tag{113}$$

The resistors R_{AB} and R_{CD} are given by a modified version of Equation 5 and Equation 6.

$$R_{AB} = R_{CD} = \frac{\left(t_{DELAY} - 25\ ns \right) \times 0.5\ V}{25 \times 10^{-12}} \approx 5.6\ k\Omega \tag{114}$$

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It is important to recognise that the delay times set by R_{AB} and R_{CD} are those measured at the device pins. Propagation delays mean that the delay times seen at the primary of the transformer will be different and this is the reason why the delays have to be optimised on actual hardware. Once the prototype is up and running it is recommended that you fine tune t_{ABSET} and t_{CDSET} at light load. Refer to Figure 21 and Figure 22. It is easier to achieve ZVS at the drain of QD than at the drain of QA because the output inductor current reflected in the transformer primary is greater at QD and QC turn-off than it is at QA and QB turn-off.

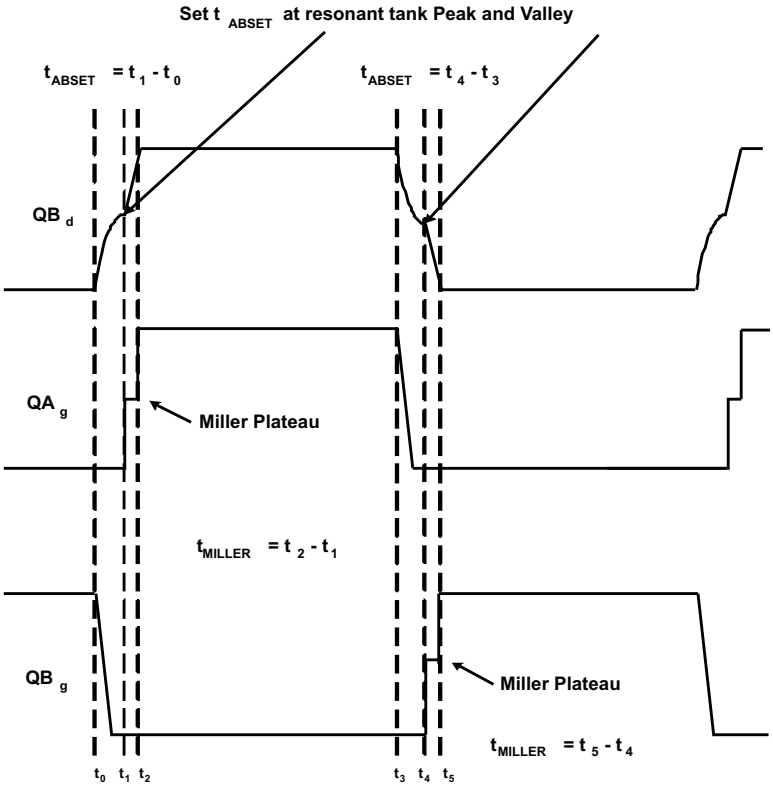


Figure 21. t_{ABSET} to Achieve Valley Switching at Light Loads

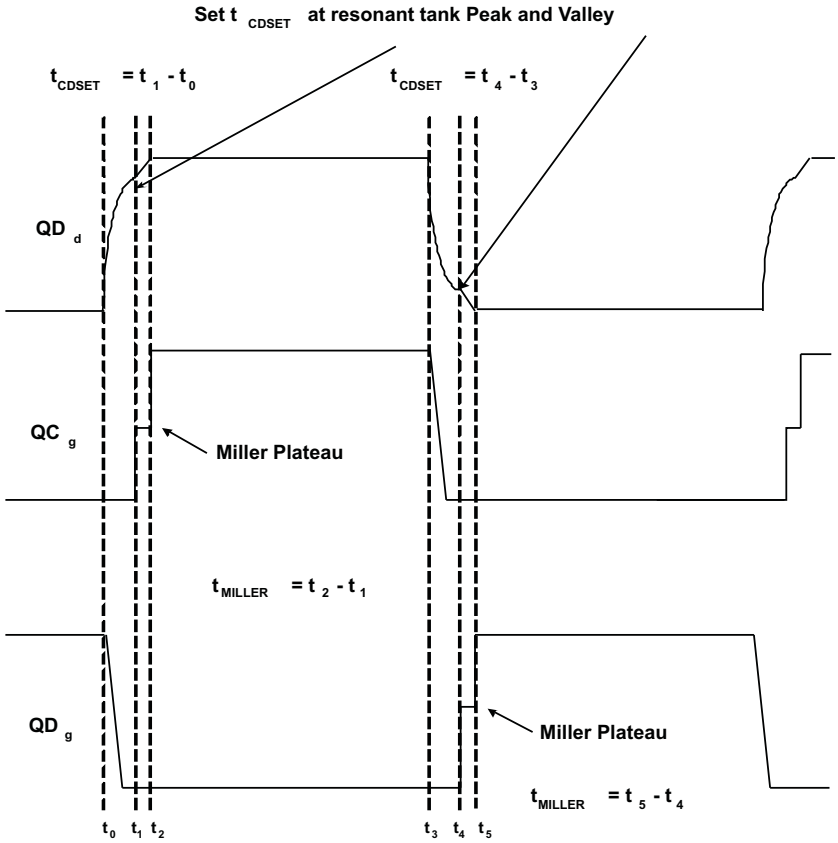


Figure 22. t_{CDSET} to Achieve Valley Switching at Light Loads

8.2.2.10.6 Setting the Slope Compensation

Slope compensation is necessary to stabilise a converter operating in peak current mode at duty cycles greater than 50%. The optimum slope compensation ramp should be half the inductor current ramp downslope during the off time. This slope is calculated as follows:

$$m_e = 0.5 \frac{V_{OUT} \times R_{CS}}{L_{OUT} \times a1 \times CT_{RAT}} = 67\ mv\,\mu s^{-1} \tag{115}$$

The magnetizing current of the power transformer provides part of the compensating ramp and is calculated as follows. The V_{IN} x D_{TYP} factor takes account of the fact that the slope of the magnetizing current is less at lower input voltages.

$$m_{MAG} = \frac{V_{IN} \times D_{TYP} \times R_{CS}}{L_{MAG} \times CT_{RAT}} \approx 43\ mv\,\mu s^{-1} \tag{116}$$

The added slope compensation ramp is then:

$$m_{SUM} = m_e - m_{MAG} \approx 24\ mv\,\mu s^{-1} \tag{117}$$

The resistor R_{SC} sets the added slope compensation ramp, m_{SUM} and is chosen as follows:

$$R_{SC} = R_{LF} \times \frac{8 \times I_{RT}}{m_{MAG} \times C_T} = 21\ k\Omega \tag{118}$$

A small AC coupling capacitor is used in the emitter of Q1 to eliminate the need for offset biasing circuitry. C_C = 1 nF.

The resistor R_{EL} is a DC load resistor for the emitter of Q1. It should have the same value as R_{SC}.

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A small capacitor at the RAMP pin input helps suppress high frequency noise, we set C_{RAMP} = 56 pF. Transistor Q1 is a small signal NPN type.

In peak current mode control the RAMP pin receives the current sense signal, plus the slope compensation ramp, through the 510-Ω resistor R_{RCS}. The 10-kΩ resistor R_{RB} provides approximately 250-mV offset bias. The value of this resistor may be adjusted up or down to alter the point at which the internal no load comparator trips.

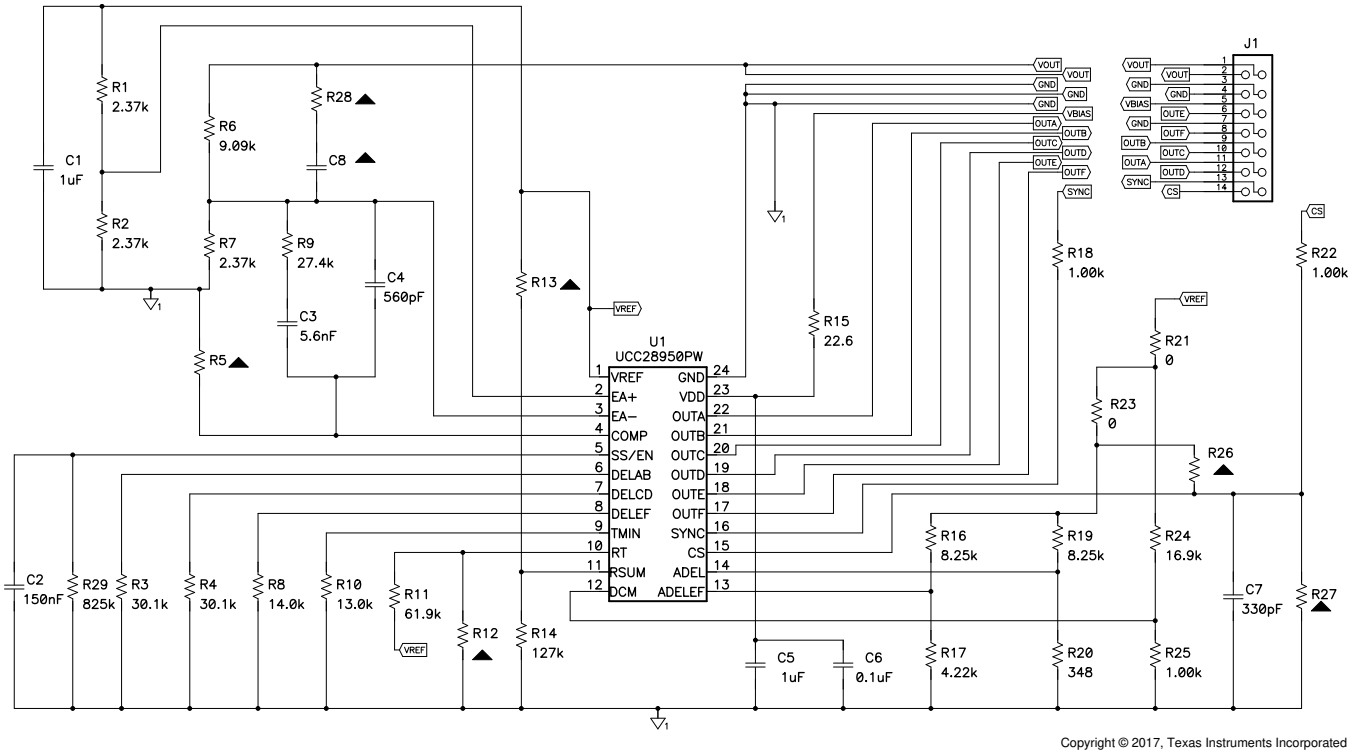


Figure 23. Daughter Board Schematic

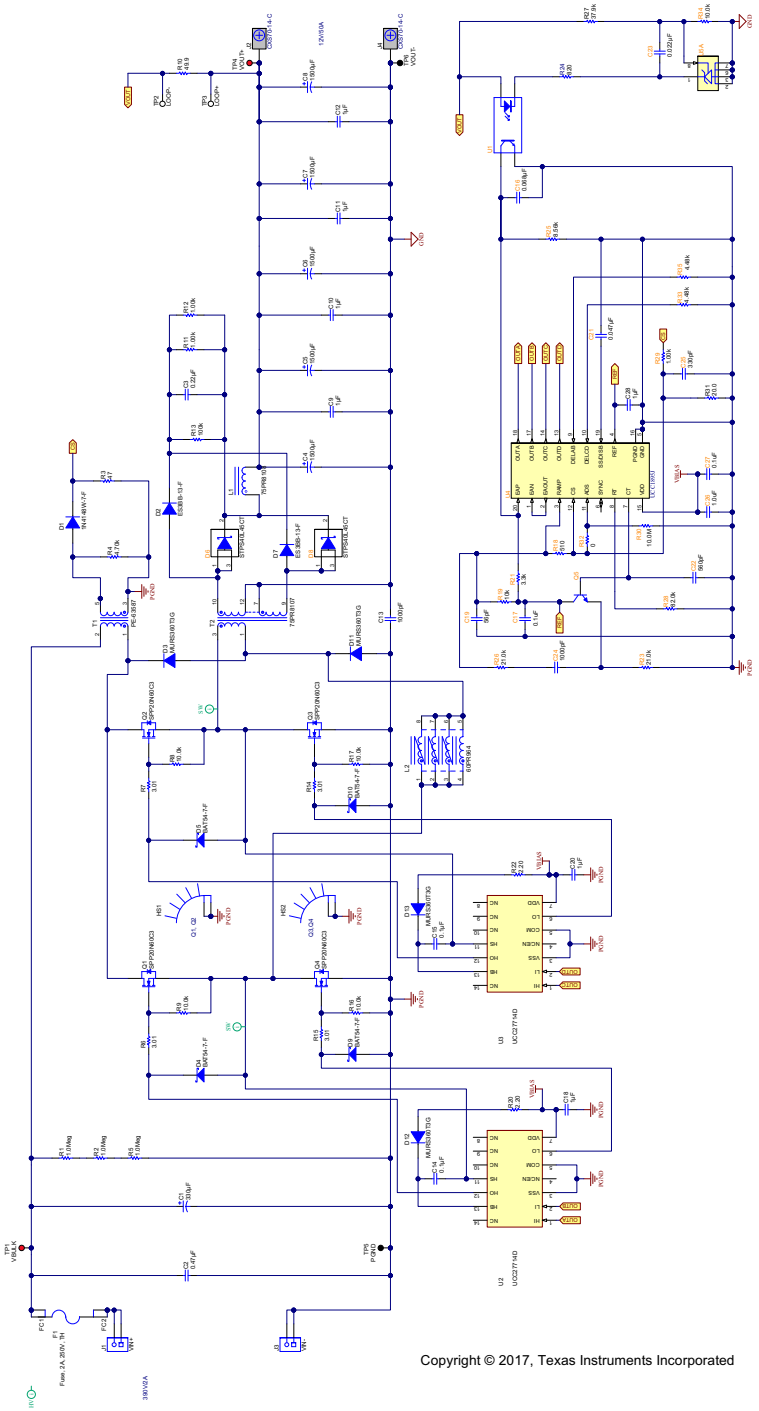
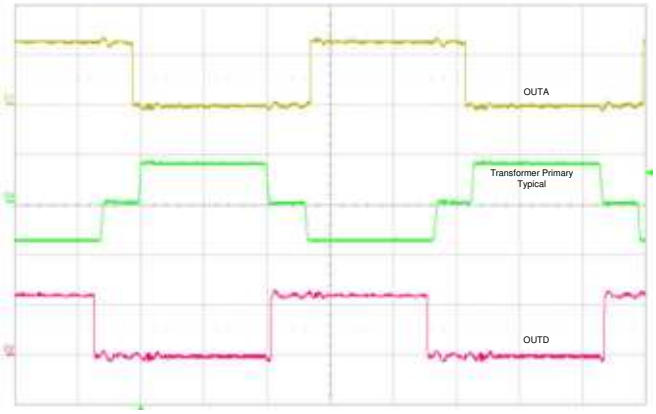


Figure 24. Power Stage Schematic

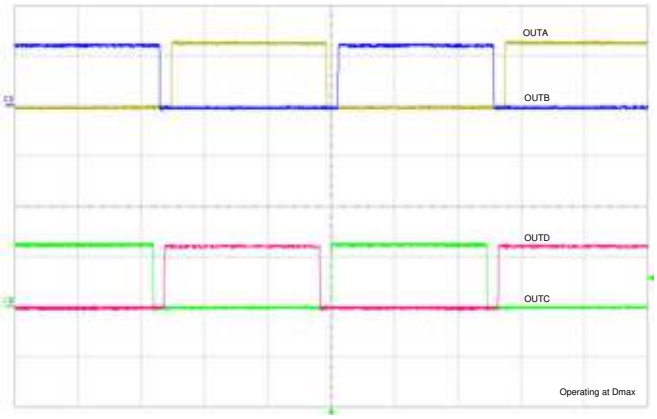
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8.2.3 Application Curves



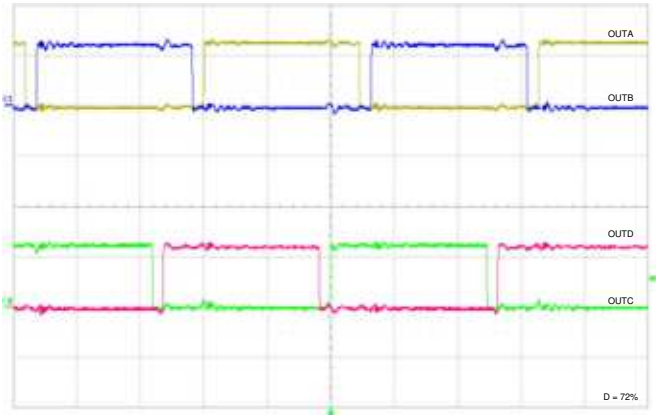
V_{IN} = 390 V
I_{OUT} = 5 A

Figure 25. Full Bridge Gate Drives and Primary Switched Nodes



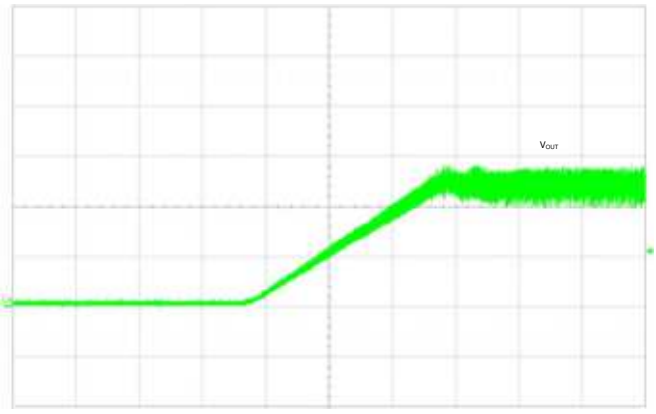
V_{IN} = 390 V
I_{OUT} = 5 A

Figure 26. Gate Drive Signals at DMAX



V_{IN} = 390 V
I_{OUT} = 10 A

Figure 27. Gate Drive Signals D = 72%



V_{IN} = 390 V
I_{OUT} = 10 A

Figure 28. Typical Start-up (Into 50% Full Load)

9 Power Supply Recommendations

The UCC3895 device should be operated from a V_{DD} rail within the limits given in the *Recommended Operating Conditions* of this data sheet. To avoid the possibility that the device might stop switching, V_{DD} must not be allowed to fall into the UVLO(off) range. In order to minimize power dissipation in the device, V_{DD} should not be unnecessarily high. Keeping V_{DD} at 12 V is a good compromise between these competing constraints. The gate drive outputs from the UCC3895 device deliver large-current pulses into their loads. This indicates the need for a low-ESR decoupling capacitor to be connected as directly as possible between the V_{DD} and PGND terminals.

TI recommends ceramic capacitors with stable dielectric characteristics over temperature, such as X7R. Avoid capacitors which have a large drop in capacitance with applied DC voltage bias. For example, use a part that has a low-voltage co-efficient of capacitance. The recommended decoupling capacitance is 1 µF, X7R, with at least a 25-V rating with a 0.1-µF NPO capacitor in parallel.

10 Layout

10.1 Layout Guidelines

In order to increase the reliability and robustness of the design, it is recommended that the following layout guidelines are followed.

- EAN pin - This is the inverting input to the error amplifier. It is a high impedance pin and is susceptible to noise pickup. Keep tracks from this pin as short as possible.
- EAP pin - This is the non-inverting input to the error amplifier. It is a high impedance pin and is susceptible to noise pickup. Keep tracks from this pin as short as possible.
- EAOUT - pin Keep tracks from this pin as short as possible.
- RAMP,CT, RT, DELAB, DELCD and ADS pins - The components connected to these pins are used to set important operating parameters. Keep these components close to the IC and provide short, low impedance return connections to the GND pin.
- REF pin - Decouple this pin to GND with a good quality ceramic capacitor. A 1-µF, X7R, 25-V capacitor is recommended. Keep REF PCB tracks as far away as possible from sources of switching noise.
- SYNC pin - This pin is essentially a digital I/O port. If it is unused, then it may be left open circuit. If Synchronisation is used, then route the incoming Synchronisation signal as far away from noise sensitive input pins as possible.
- CS pin - This connection is arguably the most important single connection in the entire PSU system. Avoid running the CS signal traces near to sources of high dv/dt. Provide a simple RC filter as close as possible to the pin to help filter out leading edge noise spikes which will occur at the beginning of each switching cycle.
- SS/DISB pin - Keep tracks from this pin as short as possible. If the Enable signal is coming from a remote source then avoid running it close to any source of high dv/dt (MOSFET Drain connections for example) and add a simple RC filter at the SS/DISB pin.
- OUTA, OUTB, OUTC, and OUTD pins - These are the gate drive output pins and will have a high dv/dt rate associated with their rising and falling edges. Keep the tracks from these pins as far away from noise sensitive input pins as possible. Ensure that the return currents from these outputs do not cause voltage changes in the analog ground connections to noise sensitive input pins.
- VDD pin - This pin must be decoupled to PGND using ceramic capacitors as detailed in the *Power Supply Recommendations* section. Keep this capacitor as close to the VDD and PGND pins as possible.
- GND pin - This pin provides the analog ground reference to the controller. Use this pin to provide a return path for the components at the RAMP, REF, CT, RT, DELAB, DELCD, ADS, CS, and SS/DISB pins. Use a Ground Plane to minimise the impedance of the ground connection and to reduce noise pickup. It is important to have a low impedance connection from GND to PGND.
- PGND pin - This pin provides the ground reference to the controller. This pin should be used to return the currents from the OUTX and SYNC pins. Use a Ground Plane to minimise the impedance of the ground connection and to reduce noise pickup.

An ideal ground plane provides an equipotential surface to which the controller ground pins can be connected. However, real ground planes have a non-zero impedance and having separate ground planes for analog and driver circuits is an easy way to prevent the analog ground from being disturbed by driver return currents. A single ground plane may be used if care is taken to ensure that the driver return currents are kept away from the part of the ground plane used for analog connections.

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10.2 Layout Example

Further layout information for this device is given in application report SLUA501.

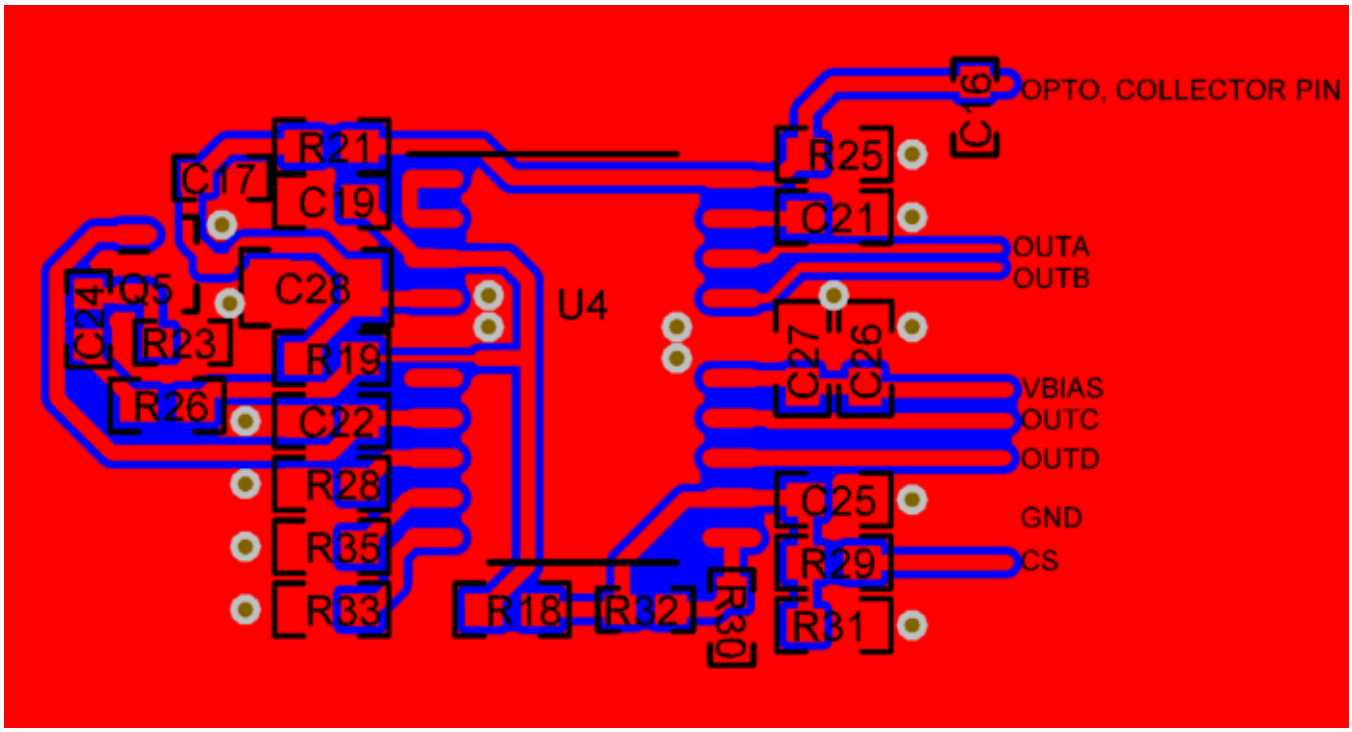


Figure 29. Suggested PCB Layout

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

See the following for related documentation:

1. *UCC2895 Layout and Grounding Recommendations*, (SLUA501).
2. *Using the UCC3895 in a Direct Control Driven Synchronous Rectifier Applications*, (SLUU109).
3. M. Dennis, *A Comparison Between the BiCMOS UCC3895 Phase Shift Controller and the UC3875*, Application Note (SLUA246).
4. L. Balogh, *The Current-Doubler Rectifier: An Alternative Rectification Technique for Push-Pull and Bridge Converters*, Application Note (SLUA121).
5. W. Andreycak, *Phase Shifted, Zero Voltage Transition Design Considerations*, Application Note (SLUA107).
6. L. Balogh, *The New UC3879 Phase Shifted PWM Controller Simplifies the Design of Zero Voltage Transition Full-Bridge Converters*, Application Note (SLUA122).
7. L. Balogh, Design Review: *100 W, 400 kHz, dc-to-dc Converter With Current Doubler Synchronous Rectification Achieves 92% Efficiency*, Unitrode Power Supply Design Seminar Manual, SEM-1100, 1996, Topic 2.
8. *UC3875 Phase Shift Resonant Controller*, Data Sheet (SLUS229).
9. *UC3879 Phase Shift Resonant Controller*, Data Sheet (SLUS230).
10. UCC3895EVM-1, *Using the UCC3895 in a Direct Control Driven Synchronous Rectifier Applications*, User's Guide (SLUU109).
11. UCC3895,*OUTC/OUTD Asymmetric Duty Cycle Operation*, Application Report (SLUA275).
12. *Current Doubler Rectifier Offers Ripple Current Cancellation*, Application Note (SLUA323).
13. *Control Driven Synchronous Rectifiers In Phase Shifted Full Bridge Converters*, Application Note (SLUA287).

11.1.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
UCC1895	Click here	Click here	Click here	Click here	Click here
UCC2895	Click here	Click here	Click here	Click here	Click here
UCC3895	Click here	Click here	Click here	Click here	Click here

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resource

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.4 Trademarks

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11.4 Trademarks (continued)

United Chemi-Con is a trademark of United Chemi-Con.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC1895J	NRND	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	UCC1895J
UCC1895J.A	NRND	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	UCC1895J
UCC1895L	NRND	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	UCC1895L
UCC1895L.A	NRND	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	UCC1895L
UCC2895DW	Active	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UCC2895DW
UCC2895DW.A	Active	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UCC2895DW
UCC2895DWG4	Active	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UCC2895DW
UCC2895DWTR	NRND	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UCC2895DW
UCC2895DWTR.A	NRND	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UCC2895DW
UCC2895DWTRG4	NRND	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UCC2895DW
UCC2895N	NRND	Production	PDIP (N) | 20	18 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	UCC2895N
UCC2895N.A	NRND	Production	PDIP (N) | 20	18 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	UCC2895N
UCC2895PW	NRND	Production	TSSOP (PW) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UCC2895
UCC2895PW.A	NRND	Production	TSSOP (PW) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UCC2895
UCC2895PWTR	NRND	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UCC2895
UCC2895PWTR.A	NRND	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UCC2895
UCC3895DW	NRND	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UCC3895DW
UCC3895DW.A	NRND	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UCC3895DW
UCC3895DWG4	NRND	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UCC3895DW
UCC3895DWTR	NRND	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UCC3895DW
UCC3895DWTR.A	NRND	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UCC3895DW
UCC3895DWTRG4	NRND	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UCC3895DW
UCC3895N	NRND	Production	PDIP (N) | 20	18 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	UCC3895N
UCC3895N.A	NRND	Production	PDIP (N) | 20	18 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	UCC3895N
UCC3895NG4	NRND	Production	PDIP (N) | 20	18 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	UCC3895N
UCC3895PW	NRND	Production	TSSOP (PW) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UCC3895
UCC3895PW.A	NRND	Production	TSSOP (PW) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UCC3895
UCC3895PWTR	NRND	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UCC3895
UCC3895PWTR.A	NRND	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UCC3895

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC3895PWTRG4	NRND	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UCC3895

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF UCC1895, UCC2895, UCC3895 :

- Catalog : UCC3895
- Automotive : UCC2895-Q1
- Enhanced Product : UCC2895-EP

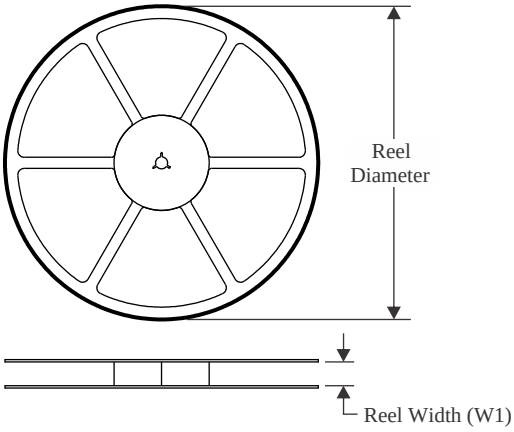
- Military : UCC1895

NOTE: Qualified Version Definitions:

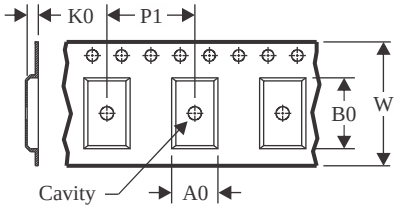
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

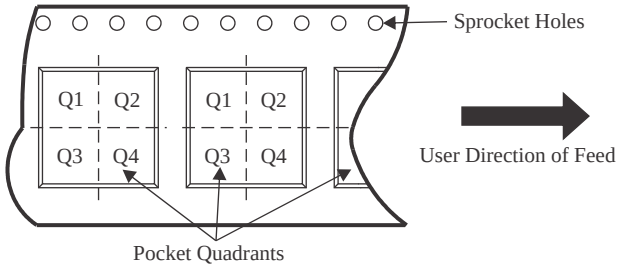


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

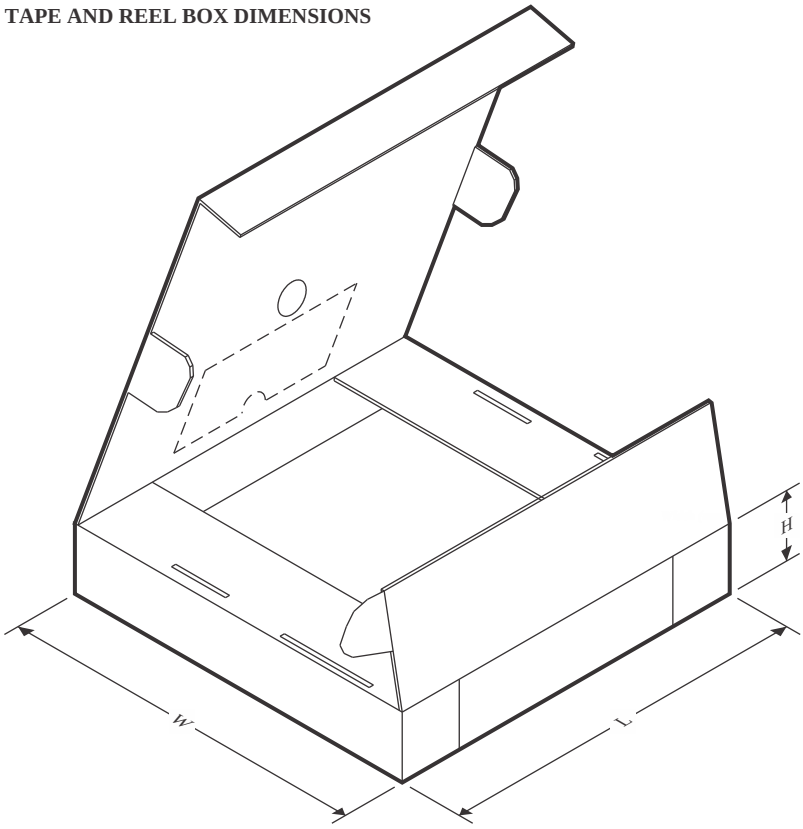
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC2895DWTR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
UCC2895PWTR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
UCC3895DWTR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
UCC3895PWTR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

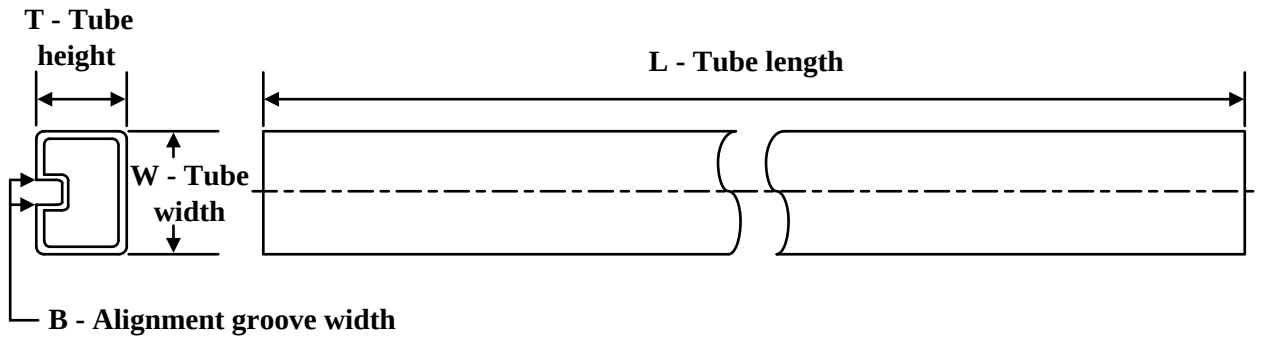
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC2895DWTR	SOIC	DW	20	2000	356.0	356.0	45.0
UCC2895PWTR	TSSOP	PW	20	2000	353.0	353.0	32.0
UCC3895DWTR	SOIC	DW	20	2000	350.0	350.0	43.0
UCC3895PWTR	TSSOP	PW	20	2000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

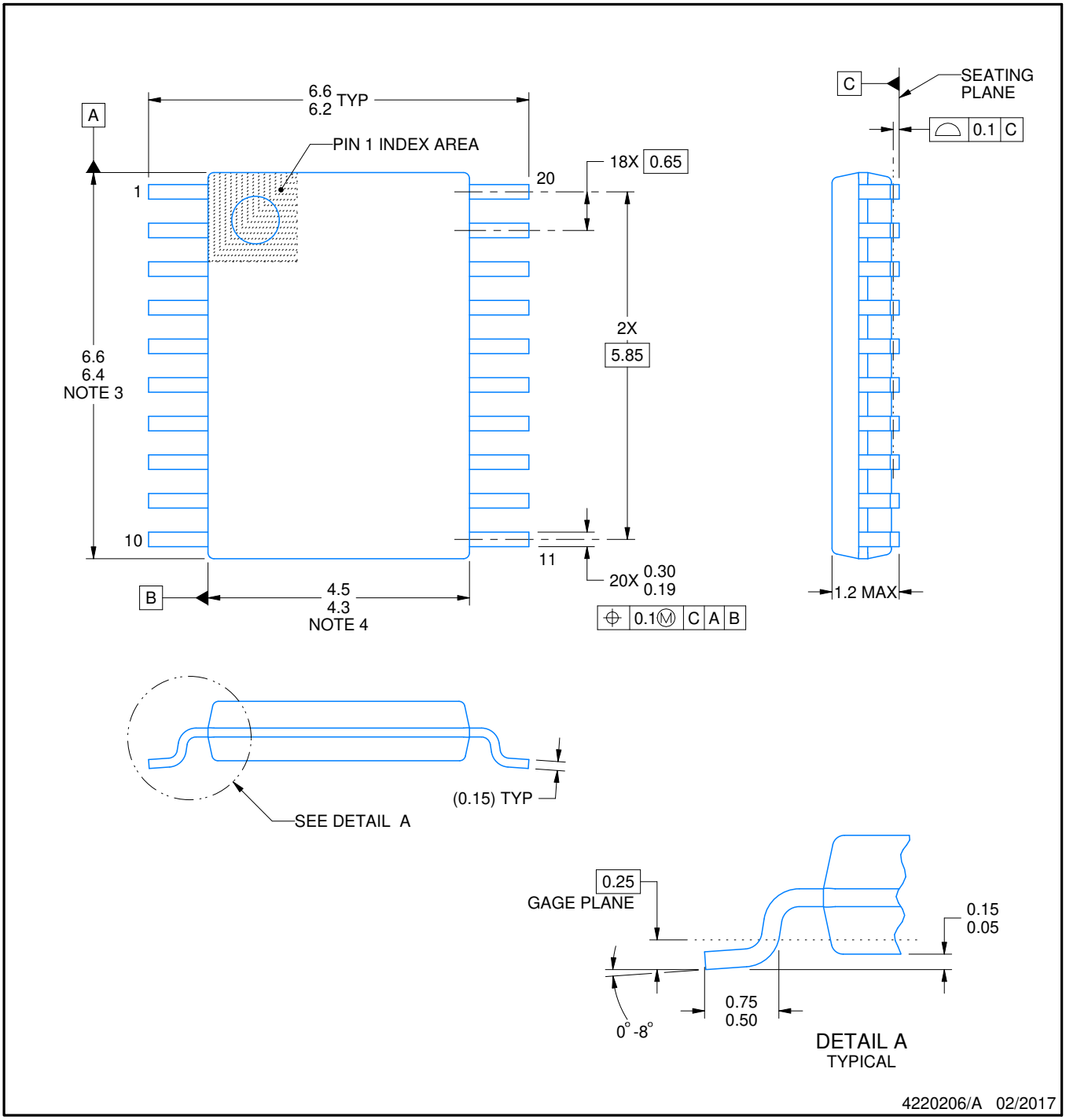
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
UCC1895L	FK	LCCC	20	55	506.98	12.06	2030	NA
UCC1895L.A	FK	LCCC	20	55	506.98	12.06	2030	NA
UCC2895DW	DW	SOIC	20	25	507	12.83	5080	6.6
UCC2895DW.A	DW	SOIC	20	25	507	12.83	5080	6.6
UCC2895DWG4	DW	SOIC	20	25	507	12.83	5080	6.6
UCC2895N	N	PDIP	20	18	506	13.97	11230	4.32
UCC2895N.A	N	PDIP	20	18	506	13.97	11230	4.32
UCC2895PW	PW	TSSOP	20	70	530	10.2	3600	3.5
UCC2895PW.A	PW	TSSOP	20	70	530	10.2	3600	3.5
UCC3895DW	DW	SOIC	20	25	507	12.83	5080	6.6
UCC3895DW.A	DW	SOIC	20	25	507	12.83	5080	6.6
UCC3895DWG4	DW	SOIC	20	25	507	12.83	5080	6.6
UCC3895N	N	PDIP	20	18	506	13.97	11230	4.32
UCC3895N.A	N	PDIP	20	18	506	13.97	11230	4.32
UCC3895NG4	N	PDIP	20	18	506	13.97	11230	4.32
UCC3895PW	PW	TSSOP	20	70	530	10.2	3600	3.5
UCC3895PW.A	PW	TSSOP	20	70	530	10.2	3600	3.5

PACKAGE OUTLINE

PW0020A

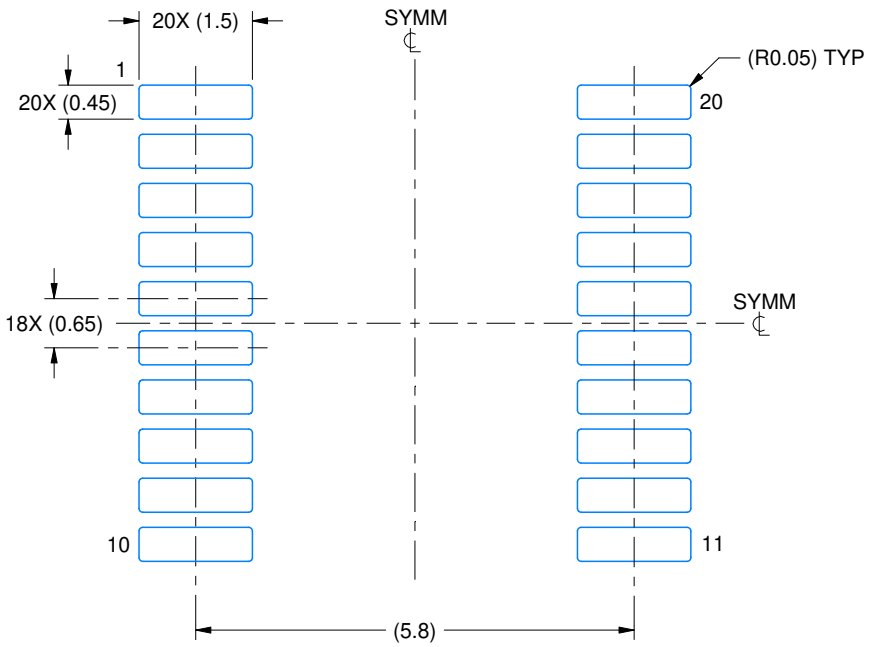
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

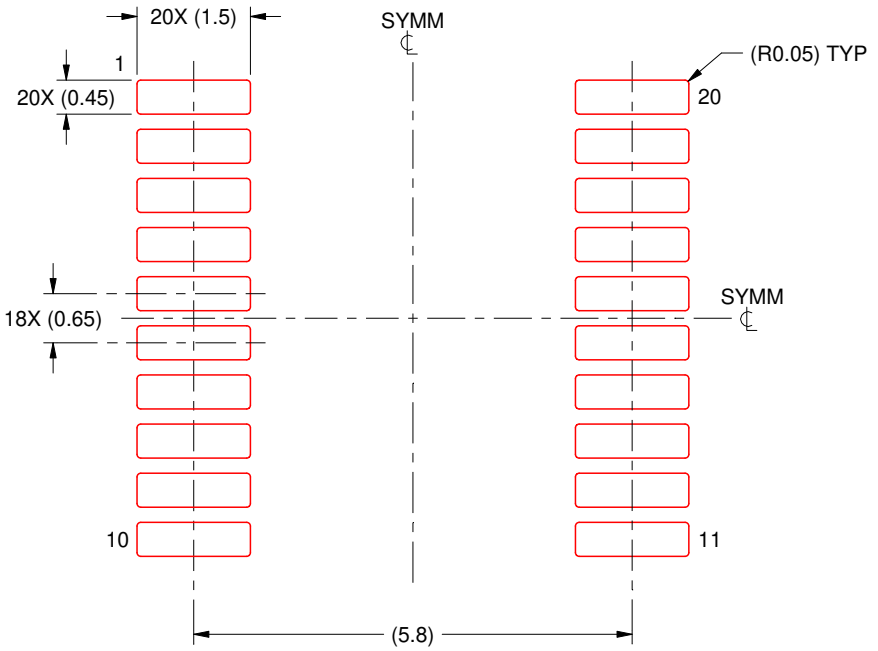


SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

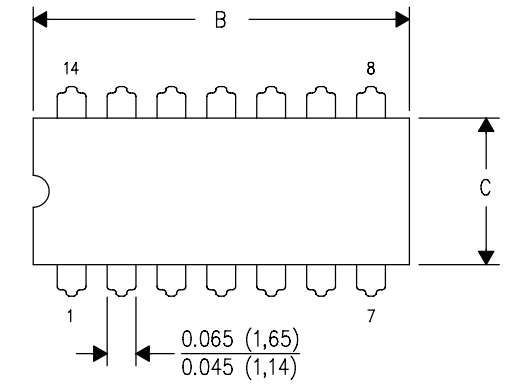
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

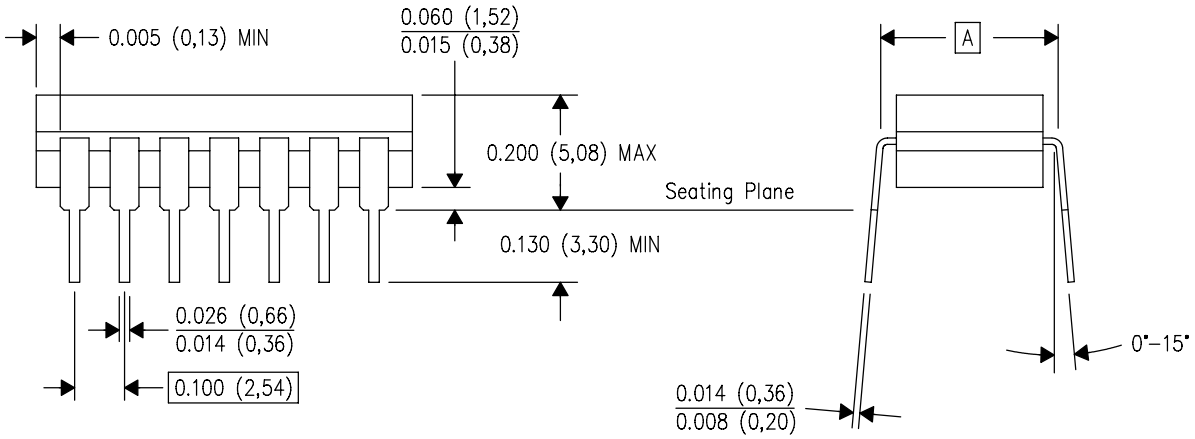
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

GENERIC PACKAGE VIEW

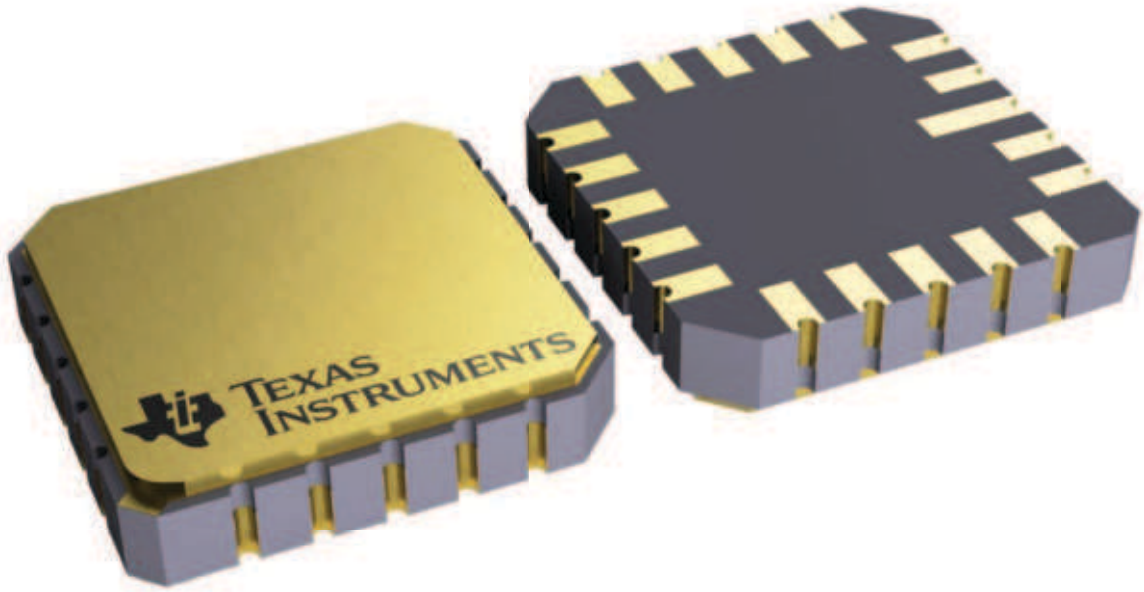
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

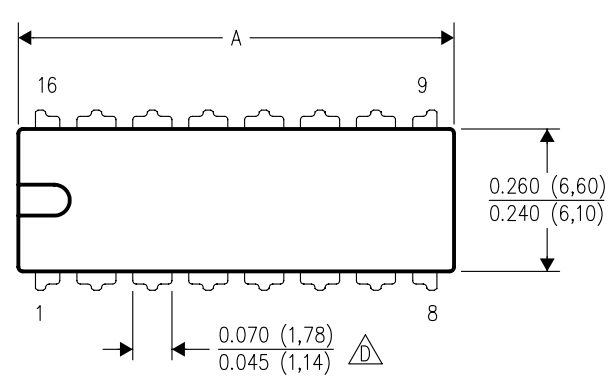


4229370\VA\

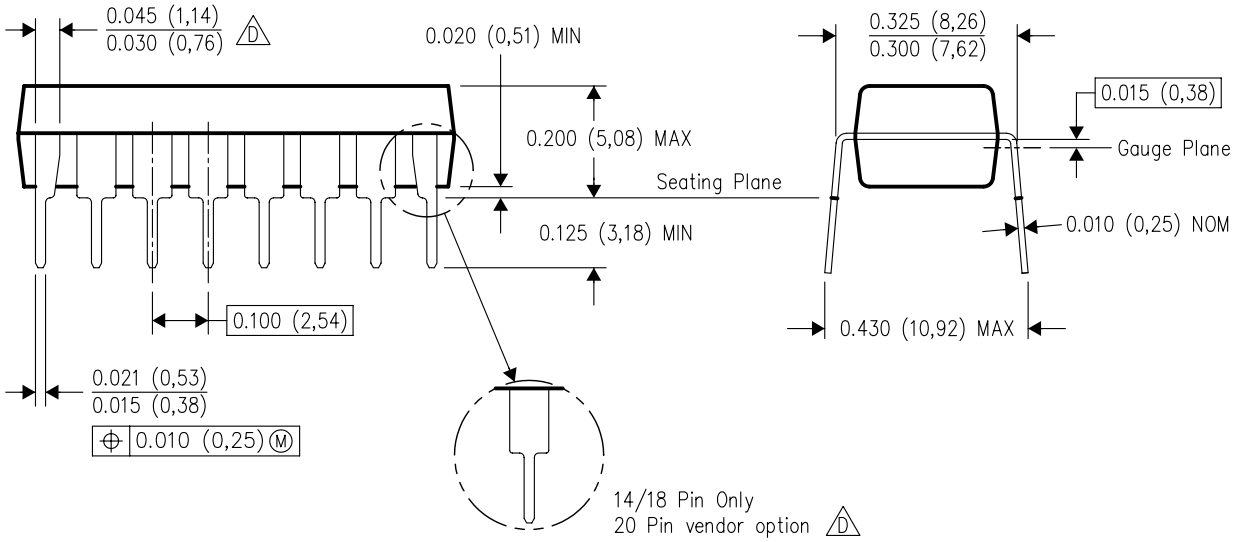
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

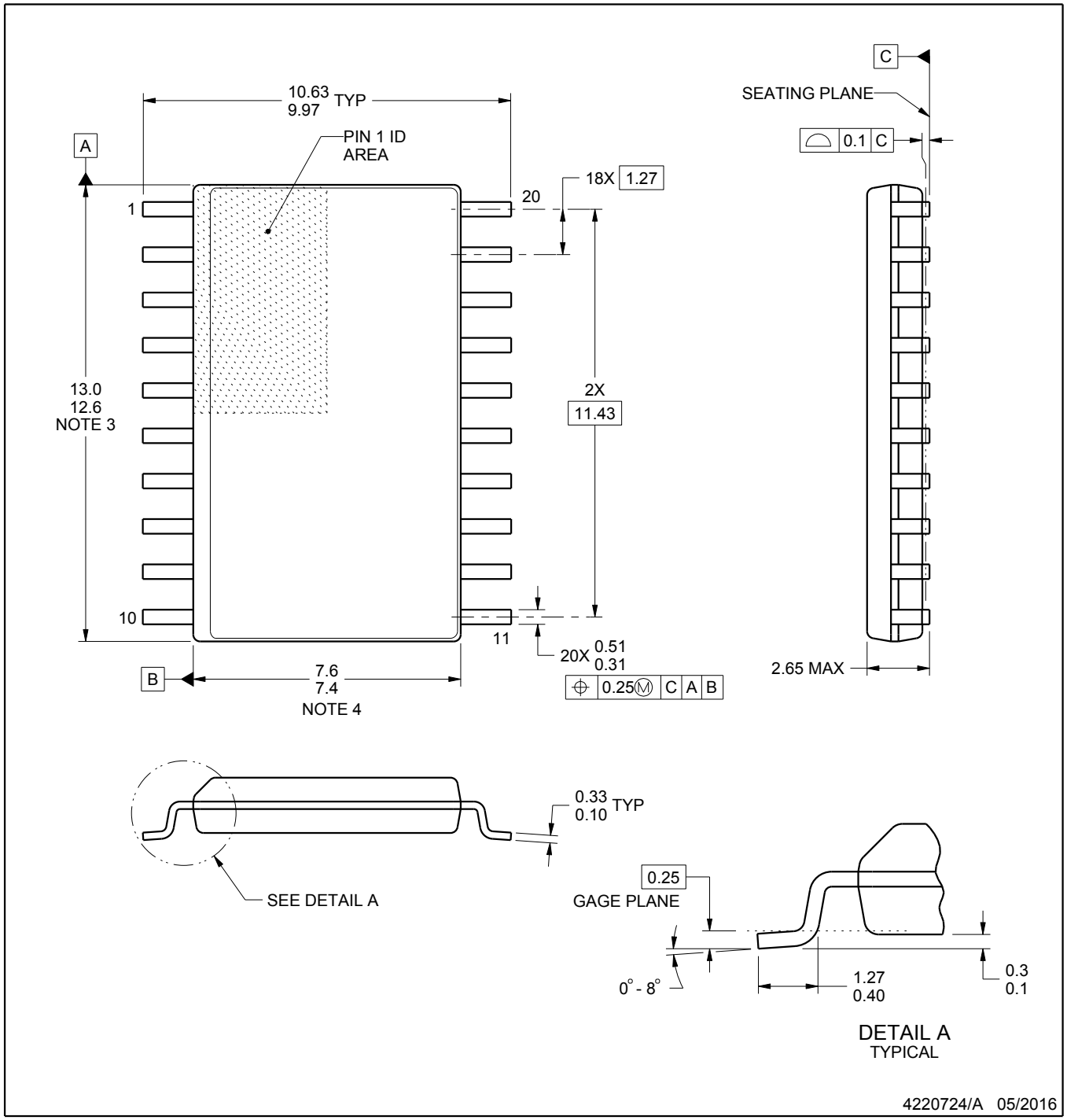


PACKAGE OUTLINE

DW0020A

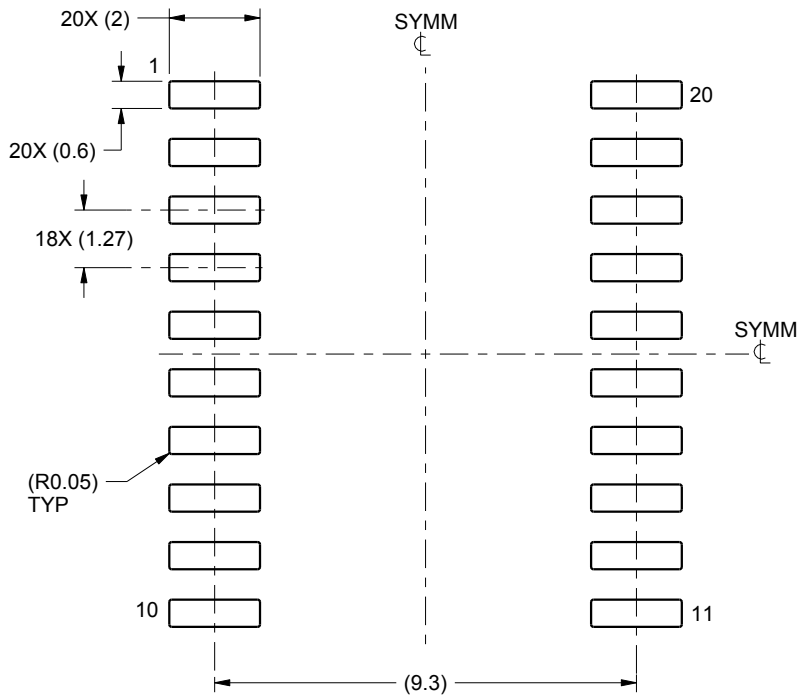
SOIC - 2.65 mm max height

SOIC

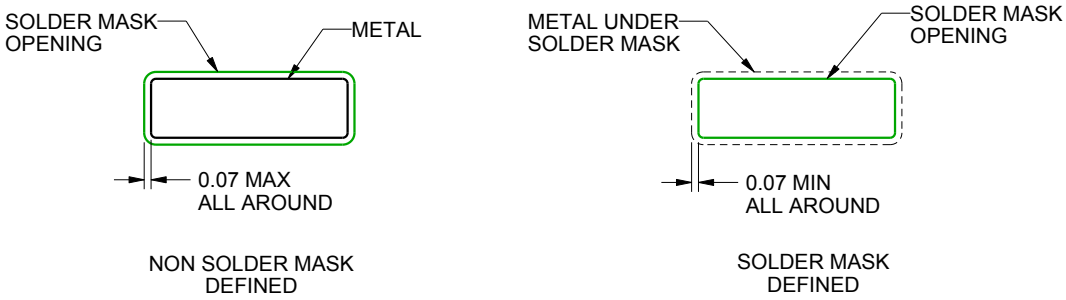


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

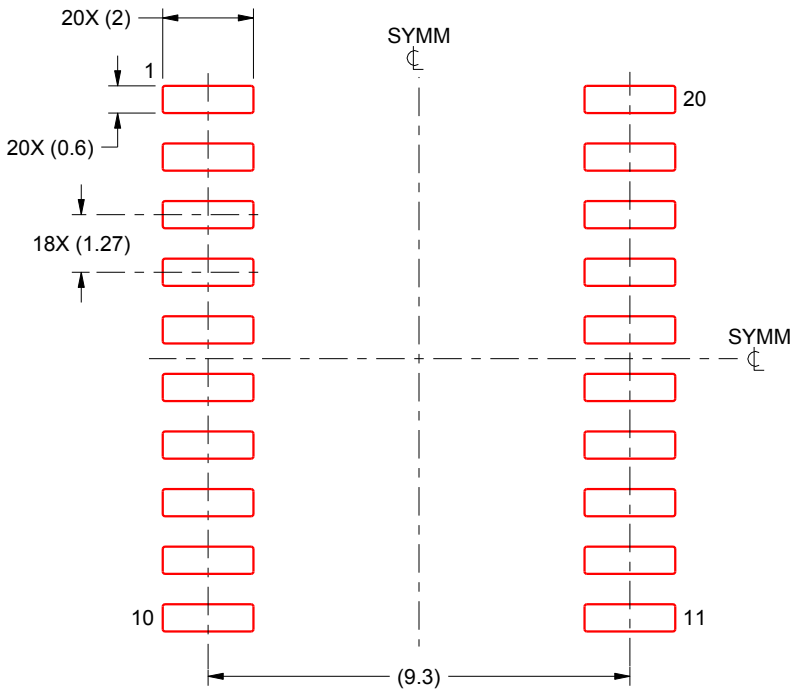


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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