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CY14V101LA
CY14V101NA

1-Mbit (128 K × 8/64 K × 16) nvSRAM

Features

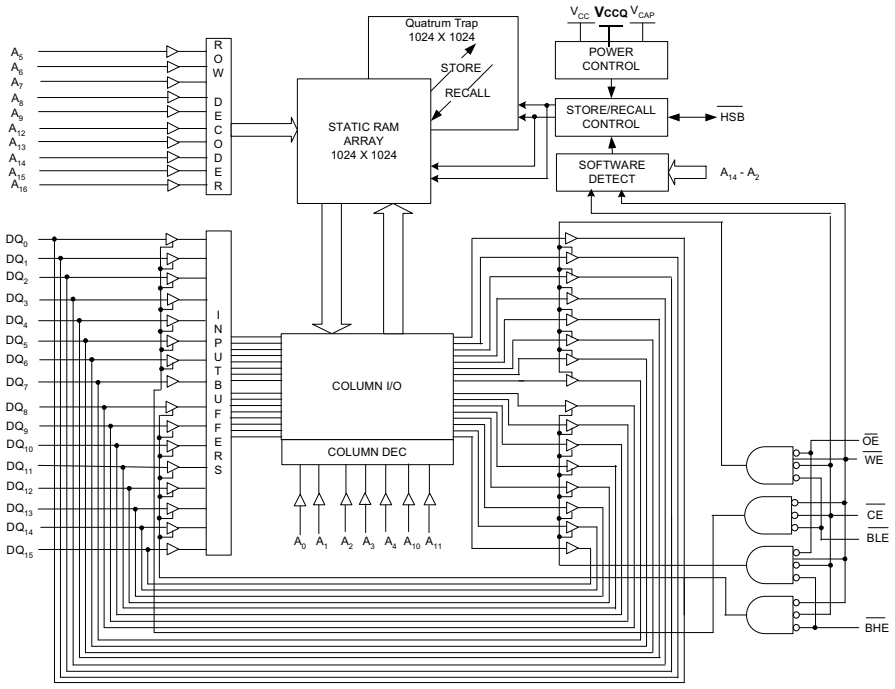
- 25 ns and 45 ns access times
- Internally organized as 128 K × 8 (CY14V101LA) or 64 K × 16 (CY14V101NA)
- Hands off automatic STORE on power down with only a small capacitor
- STORE to QuantumTrap non-volatile elements initiated by software, device pin, or AutoStore on power down
- RECALL to SRAM initiated by software or power up
- Infinite read, write, and recall cycles
- 1 million STORE cycles to QuantumTrap
- 20 year data retention
- Core V_{CC} = 3.0 V to 3.6 V; I/O V_{CCQ} = 1.65 V to 1.95 V
- Industrial temperature
- 48-ball fine-pitch ball grid array (FBGA) package
- Pb-free and restriction of hazardous substances (RoHS) compliance

Functional Description

The Cypress CY14V101LA/CY14V101NA is a fast static RAM, with a non-volatile element in each memory cell. The memory is organized as 128 K bytes of 8 bits each or 64 K words of 16 bits each. The embedded non-volatile elements incorporate QuantumTrap technology, producing the world's most reliable non-volatile memory. The SRAM provides infinite read and write cycles, while independent non-volatile data resides in the highly reliable QuantumTrap cell. Data transfers from the SRAM to the non-volatile elements (the STORE operation) takes place automatically at power down. On power-up, data is restored to the SRAM (the RECALL operation) from the non-volatile memory. Both the STORE and RECALL operations are also available under software control.

For a complete list of related documentation, click here.

Logic Block Diagram [1, 2, 3]



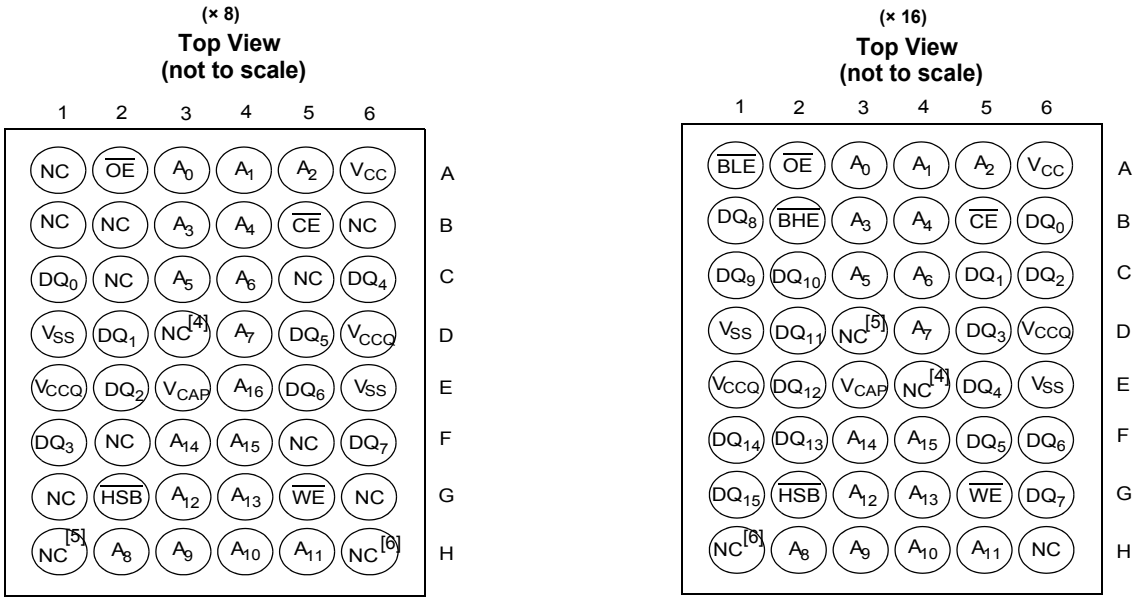
Notes
1. Address A_0–A_{16} for × 8 configuration and Address A_0–A_{15} for × 16 configuration.
2. Data DQ_0–DQ_7 for × 8 configuration and Data DQ_0–DQ_{15} for × 16 configuration.
3. BHE and BLE are applicable for × 16 configuration only.

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Pinouts

Figure 1. 48-ball FBGA pinout



Pin Definitions

Pin Name	I/O Type	Description
A_0–A_{16}	Input	Address inputs. Used to select one of the 131,072 bytes of the nvSRAM for × 8 configuration.
A_0–A_{15}		Address inputs. Used to select one of the 65,536 words of the nvSRAM for × 16 configuration.
DQ_0–DQ_7	Input/Output	Bidirectional data I/O lines for × 8 configuration. Used as input or output lines depending on operation.
DQ_0–DQ_{15}		Bidirectional data I/O lines for × 16 configuration. Used as input or output lines depending on operation.
$\overline{WE}$	Input	Write enable input, active LOW. When the chip is enabled and $\overline{WE}$ is LOW, data on the I/O pins is written to the specific address location.
$\overline{CE}$	Input	Chip enable input, active LOW. When LOW, selects the chip. When HIGH, deselects the chip.
$\overline{OE}$	Input	Output enable, active LOW. The active LOW $\overline{OE}$ input enables the data output buffers during read cycles. I/O pins are tri-stated on deasserting $\overline{OE}$ HIGH.
$\overline{BHE}$	Input	Byte high enable, active LOW. Controls DQ_{15}–DQ_8.
$\overline{BLE}$	Input	Byte low enable, active LOW. Controls DQ_7–DQ_0.
V_{SS}	Ground	Ground for the device. Must be connected to the ground of the system.
V_{CC}	Power supply	Power supply inputs to the core of the device.
V_{CCQ}	Power supply	Power supply inputs for the inputs and outputs of the device.
$\overline{HSB}$	Input/Output	Hardware STORE busy ($\overline{HSB}$). Output: Indicates busy status of nvSRAM when LOW. After each Hardware and Software STORE operation, $\overline{HSB}$ is driven HIGH for a short time (t_{HHHD}) with standard output high current and then a weak internal pull-up resistor keeps this pin HIGH (external pull-up resistor connection optional). Input: Hardware STORE implemented by pulling this pin LOW externally.
V_{CAP}	Power supply	AutoStore capacitor. Supplies power to the nvSRAM during power loss to store data from SRAM to non-volatile elements.
NC	No connect	No connect. This pin is not connected to the die.

Notes
4. Address expansion for 2-Mbit. NC pin not connected to die.
5. Address expansion for 4-Mbit. NC pin not connected to die.
6. Address expansion for 8-Mbit. NC pin not connected to die.

Device Operation

The CY14V101LA/CY14V101NA nvSRAM is made up of two functional components paired in the same physical cell. They are an SRAM memory cell and a non-volatile QuantumTrap cell. The SRAM memory cell operates as a standard fast static RAM. Data in the SRAM is transferred to the non-volatile cell (the STORE operation), or from the non-volatile cell to the SRAM (the RECALL operation). Using this unique architecture, all cells are stored and recalled in parallel. During the STORE and RECALL operations, SRAM read and write operations are inhibited. The CY14V101LA/CY14V101NA supports infinite reads and writes similar to a typical SRAM. In addition, it provides infinite RECALL operations from the non-volatile cells and up to 1 million STORE operations. Refer to the Truth Table For SRAM Operations on page 16 for a complete description of read and write modes.

SRAM Read

The CY14V101LA/CY14V101NA performs a read cycle when $\overline{CE}$ and $\overline{OE}$ are LOW and $\overline{WE}$ and $\overline{HSB}$ are HIGH. The address specified on pins $A_{0–16}$ or $A_{0–15}$ determines which of the 131,072 data bytes or 65,536 words of 16 bits each are accessed. Byte enables ($\overline{BHE}$, $\overline{BLE}$) determine which bytes are enabled to the output, in the case of 16-bit words. When the read is initiated by an address transition, the outputs are valid after a delay of t_{AA} (read cycle 1). If the read is initiated by $\overline{CE}$ or $\overline{OE}$, the outputs are valid at t_{ACE} or at t_{DOE}, whichever is later (read cycle 2). The data output repeatedly responds to address changes within the t_{AA} access time without the need for transitions on any control input pins. This remains valid until another address change or until $\overline{CE}$ or $\overline{OE}$ is brought HIGH, or $\overline{WE}$ or $\overline{HSB}$ is brought LOW.

SRAM Write

A write cycle is performed when $\overline{CE}$ and $\overline{WE}$ are LOW and $\overline{HSB}$ is HIGH. The address inputs must be stable before entering the write cycle and must remain stable until $\overline{CE}$ or $\overline{WE}$ goes HIGH at the end of the cycle. The data on the common I/O pins $DQ_{0–15}$ are written into the memory if the data is valid t_{SD} before the end of a $\overline{WE}$-controlled write or before the end of a $\overline{CE}$-controlled write. The Byte Enable inputs ($\overline{BHE}$, $\overline{BLE}$) determine which bytes are written, in the case of 16-bit words. Keep $\overline{OE}$ HIGH during the entire write cycle to avoid data bus contention on common I/O lines. If $\overline{OE}$ is left LOW, internal circuitry turns off the output buffers t_{HZWE} after $\overline{WE}$ goes LOW.

AutoStore Operation

The CY14V101LA/CY14V101NA stores data to the nvSRAM using one of the following three storage operations: Hardware STORE activated by $\overline{HSB}$; Software STORE activated by an address sequence; AutoStore on device power down. The AutoStore operation is a unique feature of QuantumTrap technology and is enabled by default on the CY14V101LA/CY14V101NA.

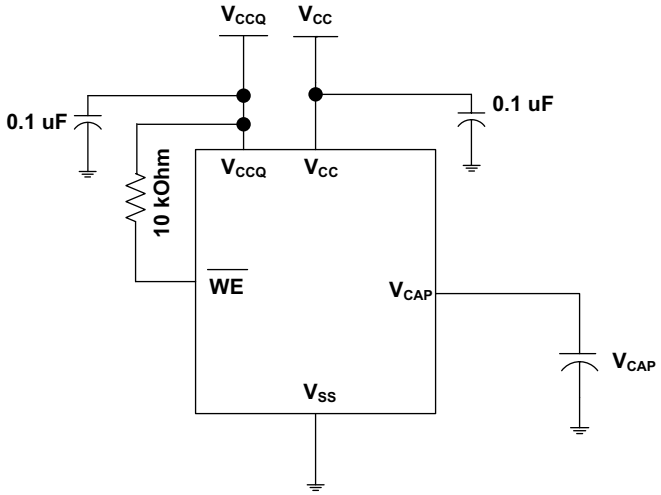
During a normal operation, the device draws current from V_{CC} to charge a capacitor connected to the V_{CAP} pin. This stored charge is used by the chip to perform a single STORE operation. If the voltage on the V_{CC} pin drops below V_{SWITCH} the part automatically disconnects the V_{CAP} pin from V_{CC}. A STORE operation is initiated with power provided by the V_{CAP} capacitor.

Note If a capacitor is not connected to V_{CAP} pin, AutoStore must be disabled using the soft sequence specified in Preventing AutoStore on page 6. If AutoStore is enabled without a capacitor on V_{CAP} pin, the device attempts an AutoStore operation without sufficient charge to complete the Store. This corrupts the data stored in nvSRAM.

Figure 2 shows the proper connection of the storage capacitor (V_{CAP}) for automatic STORE operation. Refer to DC Electrical Characteristics on page 7 for the size of V_{CAP}. The voltage on the V_{CAP} pin is driven to V_{CC} by a regulator on the chip. Place a pull-up on $\overline{WE}$ to hold it inactive during power up. This pull-up is only effective if the $\overline{WE}$ signal is tristate during power up. Many MPUs tristate their controls on power-up. This must be verified when using the pull-up. When the nvSRAM comes out of power-on-RECALL, the MPU must be active or the $\overline{WE}$ held inactive until the MPU comes out of reset.

To reduce unnecessary non-volatile stores, AutoStore and Hardware STORE operations are ignored unless at least one write operation has taken place since the most recent STORE or RECALL cycle. Software initiated STORE cycles are performed regardless of whether a write operation has taken place.

Figure 2. AutoStore Mode



Hardware STORE Operation

The CY14V101LA/CY14V101NA provides the $\overline{HSB}$ pin to control and acknowledge the STORE operations. Use the $\overline{HSB}$ pin to request a Hardware STORE cycle. When the $\overline{HSB}$ pin is driven LOW, the CY14V101LA/CY14V101NA conditionally initiates a STORE operation after t_{DELAY}. An actual STORE cycle only begins if a write to the SRAM has taken place since the last STORE or RECALL cycle. The $\overline{HSB}$ pin also acts as an open drain driver (internal 100 kΩ weak pull-up resistor) that is internally driven LOW to indicate a busy condition when the STORE (initiated by any means) is in progress.

Note After each Hardware and Software STORE operation $\overline{HSB}$ is driven HIGH for a short time (t_{HHHD}) with standard output high current and then remains HIGH by internal 100 kΩ pull-up resistor.

SRAM write operations that are in progress when $\overline{HSB}$ is driven LOW by any means are given time (t_{DELAY}) to complete before the STORE operation is initiated. However, any SRAM write

cycles requested after $\overline{HSB}$ goes LOW are inhibited until $\overline{HSB}$ returns HIGH. In case the write latch is not set, $\overline{HSB}$ is not driven LOW by the CY14V101LA/CY14V101NA. But any SRAM read and write cycles are inhibited until $\overline{HSB}$ is returned HIGH by MPU or other external source.

During any STORE operation, regardless of how it is initiated, the CY14V101LA/CY14V101NA continues to drive the $\overline{HSB}$ pin LOW, releasing it only when the STORE is complete. Upon completion of the STORE operation, the nvSRAM memory access is inhibited for t_{LZHSB} time after $\overline{HSB}$ pin returns HIGH. Leave the $\overline{HSB}$ unconnected if it is not used.

Hardware RECALL (Power-Up)

During power up or after any low power condition (V_{CC}< V_{SWITCH}), an internal RECALL request is latched. When V_{CC} again exceeds the sense voltage of V_{SWITCH}, a RECALL cycle is automatically initiated and takes $t_{HRECALL}$ to complete. During this time, $\overline{HSB}$ is driven LOW by the $\overline{HSB}$ driver.

Software STORE

Data is transferred from the SRAM to the non-volatile memory by a software address sequence. The CY14V101LA/CY14V101NA Software STORE cycle is initiated by executing sequential $\overline{CE}$ or $\overline{OE}$ controlled read cycles from six specific address locations in exact order. During the STORE cycle an erase of the previous non-volatile data is first performed, followed by a program of the non-volatile elements. After a STORE cycle is initiated, further input and output are disabled until the cycle is completed.

Because a sequence of READs from specific addresses is used for STORE initiation, it is important that no other read or write accesses intervene in the sequence, or the sequence is aborted and no STORE or RECALL takes place.

To initiate the Software STORE cycle, the following read sequence must be performed:

1. Read Address 0x4E38 Valid READ
2. Read Address 0xB1C7 Valid READ
3. Read Address 0x83E0 Valid READ
4. Read Address 0x7C1F Valid READ
5. Read Address 0x703F Valid READ
6. Read Address 0x8FC0 Initiate STORE Cycle

The software sequence may be clocked with $\overline{CE}$ controlled reads or $\overline{OE}$ controlled reads, with $\overline{WE}$ kept HIGH for all the six READ sequences. After the sixth address in the sequence is entered, the STORE cycle commences and the chip is disabled. $\overline{HSB}$ is driven LOW. After the t_{STORE} cycle time is fulfilled, the SRAM is activated again for the read and write operation.

Software RECALL

Data is transferred from the non-volatile memory to the SRAM by a software address sequence. A Software RECALL cycle is initiated with a sequence of read operations in a manner similar to the Software STORE initiation. To initiate the RECALL cycle, the following sequence of $\overline{CE}$ or $\overline{OE}$ controlled read operations must be performed:

1. Read Address 0x4E38 Valid READ
2. Read Address 0xB1C7 Valid READ
3. Read Address 0x83E0 Valid READ
4. Read Address 0x7C1F Valid READ
5. Read Address 0x703F Valid READ
6. Read Address 0x4C63 Initiate RECALL Cycle

Internally, RECALL is a two step procedure. First, the SRAM data is cleared. Next, the non-volatile information is transferred into the SRAM cells. After the t_{RECALL} cycle time, the SRAM is again ready for read and write operations. The RECALL operation does not alter the data in the non-volatile elements.

Table 1. Mode Selection

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$, $\overline{BLE}$[7]	A_{15}–A_0[8]	Mode	I/O	Power
H	X	X	X	X	Not selected	Output High Z	Standby
L	H	L	L	X	Read SRAM	Output data	Active
L	L	X	L	X	Write SRAM	Input data	Active
L	H	L	X	0x4E38 0xB1C7 0x83E0 0x7C1F 0x703F 0x8B45	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM AutoStore Disable	Output data Output data Output data Output data Output data Output data	Active[9]

Notes
7. $\overline{BHE}$ and $\overline{BLE}$ are applicable for x16 configuration only.
8. While there are 17 address lines on the CY14V101LA (16 address lines on the CY14V101NA), only the 13 address lines (A_{14}–A_2) are used to control software modes. Rest of the address lines are don't care.
9. The six consecutive address locations must be in the order listed. $\overline{WE}$ must be HIGH during all six cycles to enable a non-volatile cycle.

Table 1. Mode Selection (continued)

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$, $\overline{BLE}$[7]	A_{15}–A_0[8]	Mode	I/O	Power
L	H	L	X	0x4E38 0xB1C7 0x83E0 0x7C1F 0x703F 0x4B46	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM AutoStore Enable	Output data Output data Output data Output data Output data Output data	Active[10]
L	H	L	X	0x4E38 0xB1C7 0x83E0 0x7C1F 0x703F 0x8FC0	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Non-volatile STORE	Output data Output data Output data Output data Output data Output High Z	Active I_{CC2}[10]
L	H	L	X	0x4E38 0xB1C7 0x83E0 0x7C1F 0x703F 0x4C63	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Non-volatile RECALL	Output Data Output Data Output Data Output Data Output Data Output High Z	Active[10]

Preventing AutoStore

The AutoStore function is disabled by initiating an AutoStore disable sequence. A sequence of read operations is performed in a manner similar to the Software STORE initiation. To initiate the AutoStore disable sequence, the following sequence of $\overline{CE}$ controlled read operations must be performed:

1. Read address 0x4E38 Valid READ
2. Read address 0xB1C7 Valid READ
3. Read address 0x83E0 Valid READ
4. Read address 0x7C1F Valid READ
5. Read address 0x703F Valid READ
6. Read address 0x8B45 AutoStore Disable

The AutoStore is reenabled by initiating an AutoStore enable sequence. A sequence of read operations is performed in a manner similar to the Software RECALL initiation. To initiate the AutoStore enable sequence, the following sequence of $\overline{CE}$ controlled read operations must be performed:

1. Read address 0x4E38 Valid READ
2. Read address 0xB1C7 Valid READ
3. Read address 0x83E0 Valid READ
4. Read address 0x7C1F Valid READ
5. Read address 0x703F Valid READ
6. Read address 0x4B46 AutoStore Enable

If the AutoStore function is disabled or reenabled, a manual STORE operation (Hardware or Software) must be issued to save the AutoStore state through subsequent power down cycles. The part comes from the factory with AutoStore enabled and 0x00 written in all cells.

Data Protection

The CY14V101LA/CY14V101NA protects data from corruption during low voltage conditions by inhibiting all externally initiated STORE and write operations. The low voltage condition is detected when V_{CC} < V_{SWITCH}. If the CY14V101LA/CY14V101NA is in a write mode (both $\overline{CE}$ and $\overline{WE}$ are LOW) at power up, after a RECALL or STORE, the write is inhibited until the SRAM is enabled after t_{LZHSB} (HSB to output active). When V_{CCQ} < V_{IODIS}, I/Os are disabled (no STORE takes place). This protects against inadvertent writes during brown out conditions on V_{CCQ} supply.

Note
10. The six consecutive address locations must be in the order listed. $\overline{WE}$ must be HIGH during all six cycles to enable a non-volatile cycle.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. These user guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Maximum accumulated storage time:

At 150 °C ambient temperature ..... 1000 h

At 85 °C ambient temperature ..... 20 Years

Maximum junction temperature ..... 150 °C

Supply voltage on V_{CC} relative to V_{SS} .....–0.5 V to 4.1 V

Supply voltage on V_{CCQ} relative to V_{SS} .....–0.5 V to 2.45 V

Voltage applied to outputs in High Z State .....–0.5 V to V_{CCQ} + 0.5 V

Input voltage .....–0.5 V to V_{CCQ} + 0.5 V

Transient voltage (< 20 ns) on any pin to ground potential .....–2.0 V to V_{CCQ} + 2.0 V

Package power dissipation capability (T_A = 25 °C) ..... 1.0 W

Surface mount Pb soldering temperature (3 seconds) ..... +260 °C

DC output current (1 output at a time, 1s duration) ..... 15 mA

Static discharge voltage (per MIL-STD-883, Method 3015) ..... > 2001 V

Latch up current ..... > 140 mA

Operating Range

Range	Ambient Temperature	V_{CC}	V_{CCQ}
Industrial	–40 °C to +85 °C	3.0 V to 3.6 V	1.65 V to 1.95 V

DC Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	Min	Typ [11]	Max	Unit
V_{CC}	Power supply voltage		3.0	3.3	3.6	V
V_{CCQ}			1.65	1.8	1.95	V
I_{CC1}	Average V_{CC} current	t_{RC} = 25 ns	–	–	70	mA
		t_{RC} = 45 ns	–	–	52	mA
I_{CCQ1}	Average V_{CCQ} current	Values obtained without output loads (I_{OUT} = 0 mA)	–	–	25	mA
			–	–	15	mA
I_{CC2}	Average V_{CC} current during STORE	All inputs don't care, V_{CC} = Max Average current for duration t_{STORE}	–	–	10	mA
I_{CC3}	Average V_{CC} current at t_{RC}= 200 ns, $V_{CC(Typ)}$, 25 °C	All inputs cycling at CMOS levels. Values obtained without output loads (I_{OUT} = 0 mA)	–	35	–	mA
I_{CCQ3}	Average V_{CCQ} current at t_{RC}= 200 ns, $V_{CCQ(Typ)}$, 25 °C		–	5	–	mA
I_{CC4}	Average V_{CAP} current during AutoStore cycle	All inputs don't care. Average current for duration t_{STORE}	–	–	8	mA
I_{SB}	V_{CC} standby current	$\overline{CE} \geq (V_{CCQ} - 0.2\ V)$. $V_{IN} \leq 0.2\ V$ or $\geq (V_{CCQ} - 0.2\ V)$. Standby current level after non-volatile cycle is complete. Inputs are static. f = 0 MHz	–	–	8	mA
I_{IX}[12]	Input leakage current (except $\overline{HSB}$)	V_{CCQ} = Max, $V_{SS} \leq V_{IN} \leq V_{CCQ}$	–1	–	+1	µA
	Input leakage current (for $\overline{HSB}$)	V_{CCQ} = Max, $V_{SS} \leq V_{IN} \leq V_{CCQ}$	–100	–	+1	µA

Notes

11. Typical values are at 25 °C, V_{CC} = $V_{CC(Typ)}$ and V_{CCQ}= $V_{CCQ(Typ)}$. Not 100% tested.
12. The $\overline{HSB}$ pin has I_{OUT} = –4 µA for V_{OH} of 1.07 V when both active HIGH and LOW drivers are disabled. When they are enabled standard V_{OH} and V_{OL} are valid. This parameter is characterized but not tested.

DC Electrical Characteristics (continued)

Over the Operating Range

Parameter	Description	Test Conditions	Min	Typ [11]	Max	Unit
I_{OZ}	Off-state output leakage current	V_{CCQ} = Max, $V_{SS} \le V_{OUT} \le V_{CCQ}$, $\overline{CE}$ or $\overline{OE} \ge V_{IH}$ or $\overline{BHE}/\overline{BLE} \ge V_{IH}$ or $\overline{WE} \le V_{IL}$	–1	–	+1	µA
V_{IH}	Input HIGH voltage	–	0.7 × V_{CCQ}	–	V_{CCQ} + 0.3	V
V_{IL}	Input LOW voltage	–	– 0.3	–	0.3 × V_{CCQ}	V
V_{OH}	Output HIGH voltage	I_{OUT} = –1 mA	V_{CCQ} – 0.45	–	–	V
V_{OL}	Output LOW voltage	I_{OUT} = 2 mA	–	–	0.45	V
V_{CAP}[13]	Storage capacitor	Between V_{CAP} pin and V_{SS}	61	68	180	µF
V_{VCAP}[14, 15]	Maximum voltage driven on V_{CAP} pin by the device	V_{CC} = Max	–	–	V_{CC}	V

Data Retention and Endurance

Parameter	Description	Min	Unit
$DATA_R$	Data retention	20	Years
NV_C	Non-volatile STORE operations	1,000	K

Capacitance

Parameter[14]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance (except $\overline{BHE}$, $\overline{BLE}$ and $\overline{HSB}$)	T_A = 25 °C, f = 1 MHz, V_{CC} = $V_{CC(Typ)}$, V_{CCQ} = $V_{CCQ(Typ)}$	7	pF
	Input capacitance (for $\overline{BHE}$, $\overline{BLE}$ and $\overline{HSB}$)		8	pF
C_{OUT}	Output capacitance (except $\overline{HSB}$)		7	pF
	Output capacitance (for $\overline{HSB}$)		8	pF

Thermal Resistance

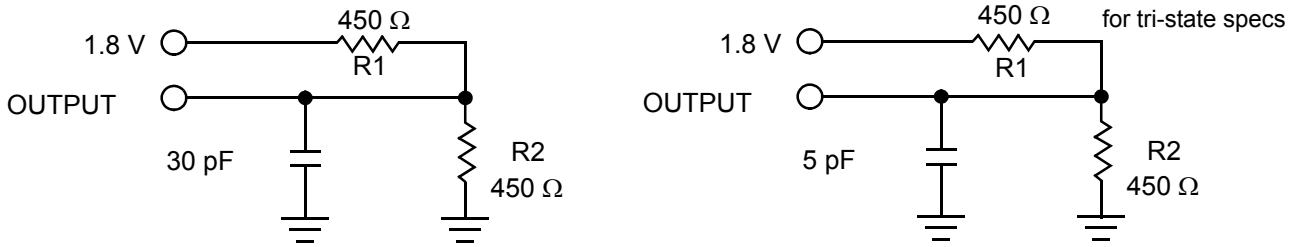
Parameter[14]	Description	Test Conditions	48-ball FBGA	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, in accordance with EIA/JESD51.	48.19	°C/W
Θ_{JC}	Thermal resistance (junction to case)		6.5	°C/W

Notes

13. Min V_{CAP} value guarantees that there is a sufficient charge available to complete a successful AutoStore operation. Max V_{CAP} value guarantees that the capacitor on V_{CAP} is charged to a minimum voltage during a Power-Up RECALL cycle so that an immediate power-down cycle can complete a successful AutoStore. Therefore it is always recommended to use a capacitor within the specified min and max limits. Refer application note AN43593 for more details on V_{CAP} options.
14. Maximum voltage on V_{CAP} pin (V_{VCAP}) is provided for guidance when choosing the V_{CAP} capacitor. The voltage rating of the V_{CAP} capacitor across the operating temperature range should be higher than the V_{VCAP} voltage.
15. These parameters are guaranteed by design and are not tested.

AC Test Loads

Figure 3. AC Test Loads



AC Test Conditions

Input pulse levels.....0 V to 1.8 V
Input rise and fall times (10% to 90%)..... ≤ 1.8 ns
Input and output timing reference levels..... 0.9 V

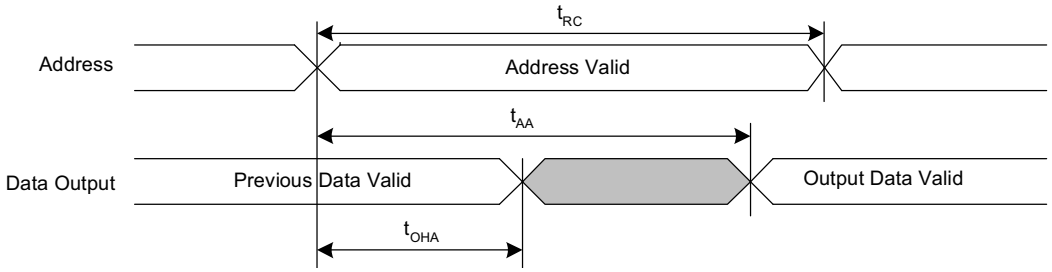
AC Switching Characteristics

Over the Operating Range

Parameters [16]		Description	25 ns		45 ns		Unit
Cypress Parameters	Alt Parameters		Min	Max	Min	Max	
SRAM Read Cycle							
t_{ACE}	t_{ACS}	Chip enable access time	–	25	–	45	ns
t_{RC}[17]	t_{RC}	Read cycle time	25	–	45	–	ns
t_{AA}[18]	t_{AA}	Address access time	–	25	–	45	ns
t_{DOE}	t_{OE}	Output enable to data valid	–	12	–	20	ns
t_{OHA}[18]	t_{OH}	Output hold after address change	3	–	3	–	ns
t_{LZCE}[19, 20]	t_{LZ}	Chip enable to output active	3	–	3	–	ns
t_{HZCE}[19, 20]	t_{HZ}	Chip disable to output inactive	–	10	–	15	ns
t_{LZOE}[19, 20]	t_{OLZ}	Output enable to output active	0	–	0	–	ns
t_{HZOE}[19, 20]	t_{OHZ}	Output disable to output inactive	–	10	–	15	ns
t_{PU}[19]	t_{PA}	Chip enable to power active	0	–	0	–	ns
t_{PD}[19]	t_{PS}	Chip disable to power standby	–	25	–	45	ns
t_{DBE}[19]	–	Byte enable to data valid	–	12	–	20	ns
t_{LZBE}[19]	–	Byte enable to output active	0	–	0	–	ns
t_{HZBE}[19]	–	Byte disable to output inactive	–	10	–	15	ns
SRAM Write Cycle							
t_{WC}	t_{WC}	Write cycle time	25	–	45	–	ns
t_{PWE}	t_{WP}	Write pulse width	20	–	30	–	ns
t_{SCE}	t_{CW}	Chip enable to end of write	20	–	30	–	ns
t_{SD}	t_{DW}	Data setup to end of write	10	–	15	–	ns
t_{HD}	t_{DH}	Data hold after end of write	0	–	0	–	ns
t_{AW}	t_{AW}	Address setup to end of write	20	–	30	–	ns
t_{SA}	t_{AS}	Address setup to start of write	0	–	0	–	ns
t_{HA}	t_{WR}	Address hold after end of write	0	–	0	–	ns
t_{HZWE}[19, 20, 21]	t_{WZ}	Write enable to output disable	–	10	–	15	ns
t_{LZWE}[19, 20]	t_{OW}	Output active after end of write	3	–	3	–	ns
t_{BW}	–	Byte enable to end of write	20	–	30	–	ns

Switching Waveforms

Figure 4. SRAM Read Cycle #1 (Address Controlled) [17, 18, 22]



Notes

16. Test conditions assume signal transition time of 1.8 ns or less, timing reference levels of $V_{CCQ}/2$, input pulse levels of 0 to $V_{CC\,Q(typ)}$, and output loading of the specified I_{OL}/I_{OH} and load capacitance shown in Figure 3 on page 9.
17. WE must be HIGH during SRAM read cycles.
18. Device is continuously selected with CE, OE and BHE / BLE LOW.
19. These parameters are guaranteed by design and are not tested.
20. Measured ±200 mV from steady state output voltage.
21. If WE is low when CE goes low, the outputs remain in the high-impedance state.
22. HSB must remain HIGH during READ and WRITE cycles.

Switching Waveforms (continued)

Figure 5. SRAM Read Cycle #2 ($\overline{CE}$ and $\overline{OE}$ Controlled) [23, 24, 25]

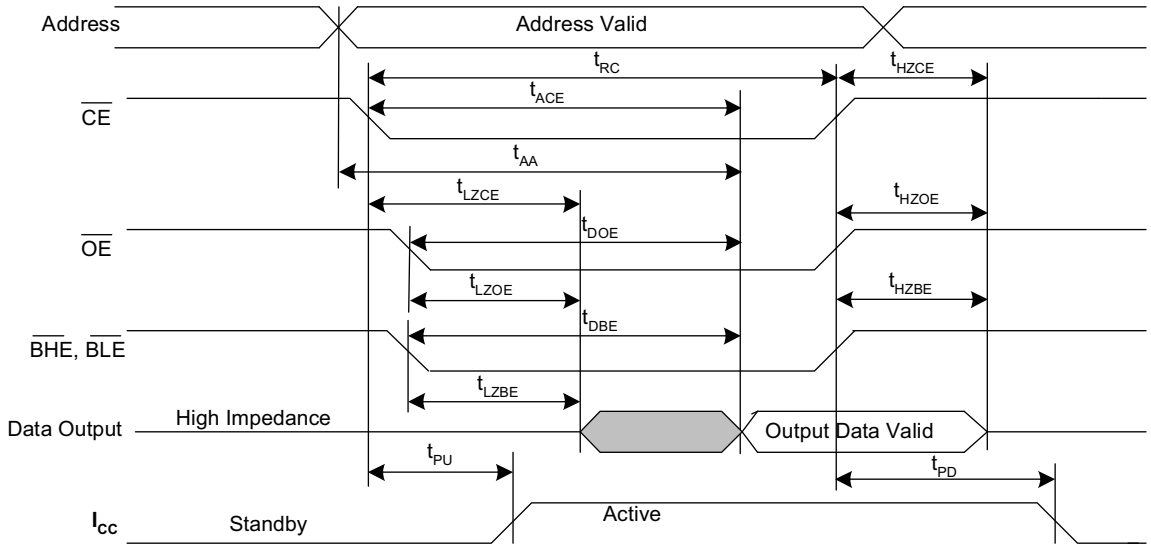
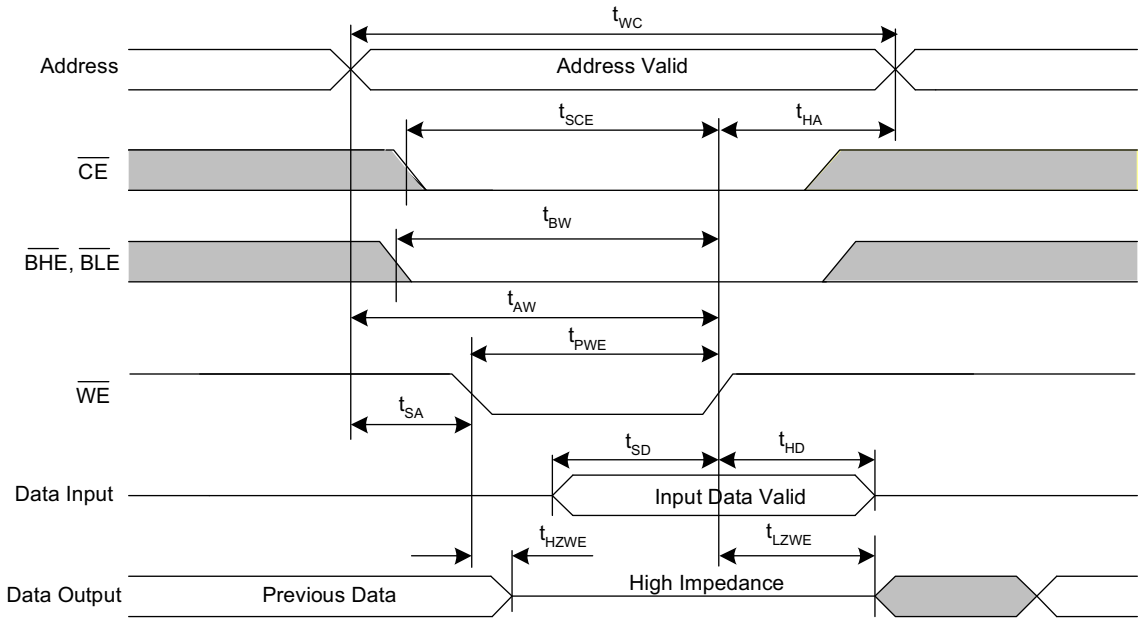


Figure 6. SRAM Write Cycle #1 ($\overline{WE}$ Controlled) [23, 25, 26, 27]



Notes
23. $\overline{BHE}$ and $\overline{BLE}$ are applicable for × 16 configuration only.
24. $\overline{WE}$ must be HIGH during SRAM read cycles.
25. $\overline{HSB}$ must remain HIGH during READ and WRITE cycles.
26. If $\overline{WE}$ is low when $\overline{CE}$ goes low, the outputs remain in the high impedance state.
27. $\overline{CE}$ or $\overline{WE}$ must be ≥ V_{IH} during address transitions.

Switching Waveforms (continued)

Figure 7. SRAM Write Cycle #2 ($\overline{CE}$ Controlled) [28, 29, 30, 31]

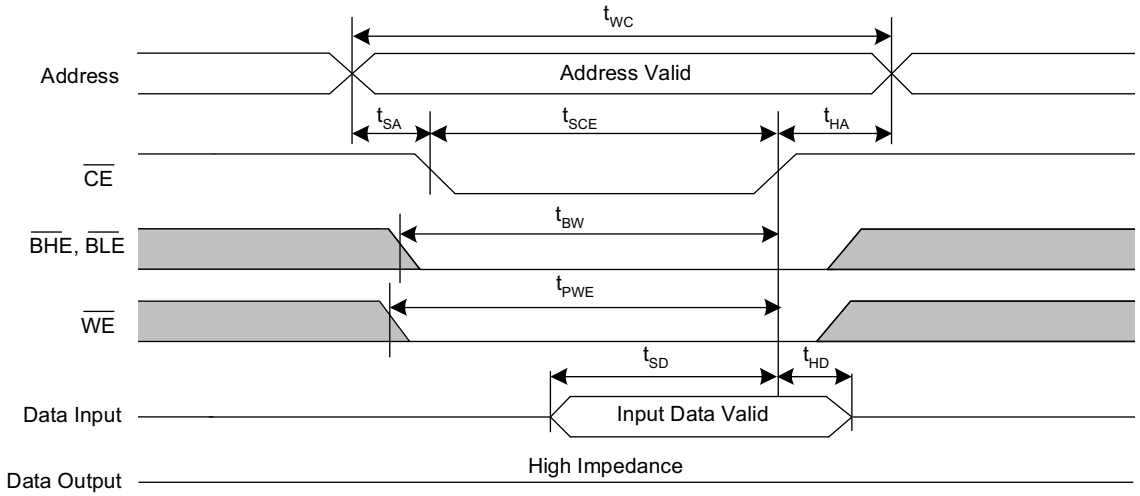
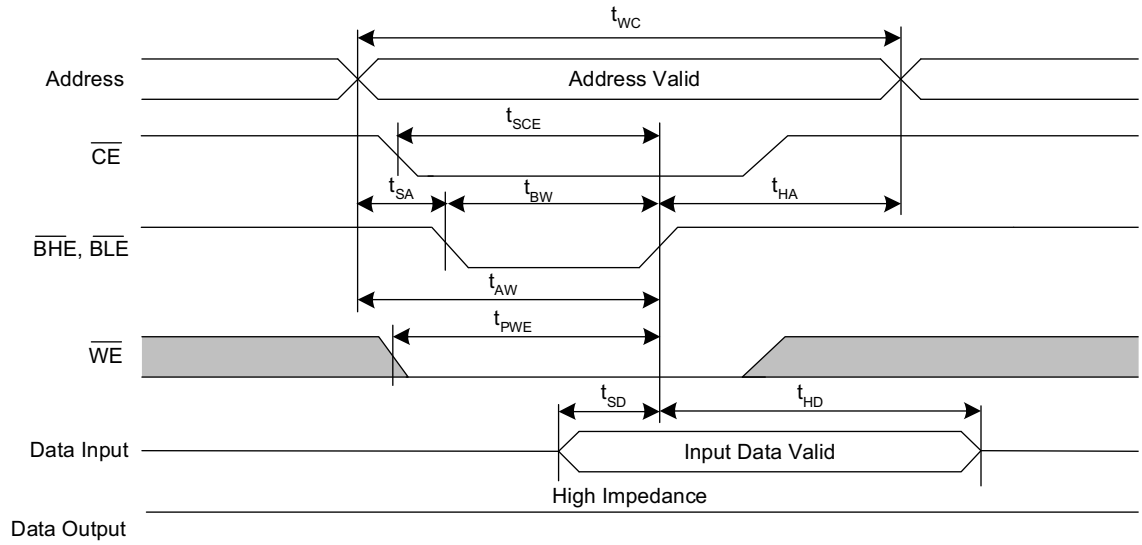


Figure 8. SRAM Write Cycle #3 ($\overline{BHE}$ and $\overline{BLE}$ Controlled) [28, 29, 30, 31]



Notes
28. $\overline{BHE}$ and $\overline{BLE}$ are applicable for x16 configuration only.
29. $\overline{HSB}$ must remain HIGH during READ and WRITE cycles.
30. If $\overline{WE}$ is low when $\overline{CE}$ goes low, the outputs remain in the high impedance state.
31. $\overline{CE}$ or $\overline{WE}$ must be $\geq V_{IH}$ during address transitions.

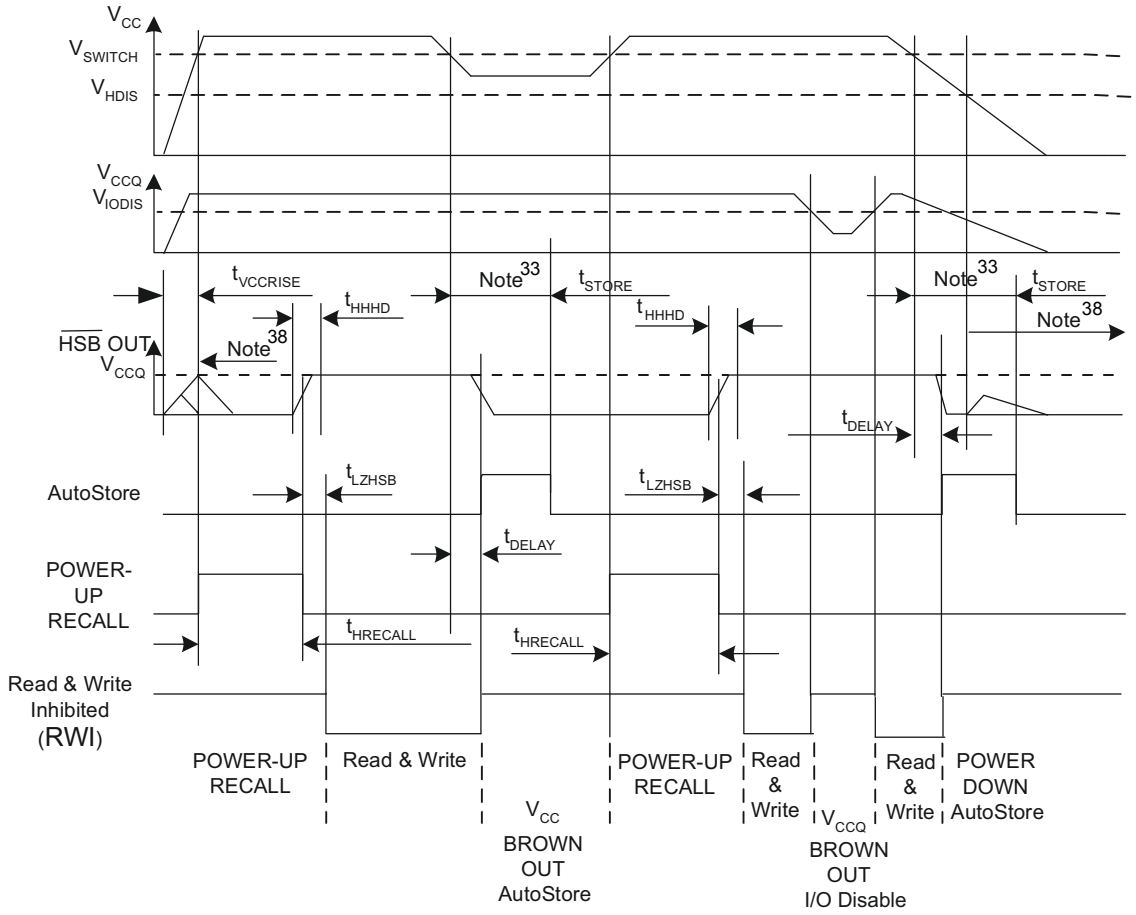
AutoStore/Power-up RECALL

Over the Operating Range

Parameter	Description	CY14V101LA/CY14V101NA		Unit
		Min	Max	
$t_{HRECALL}$ [32]	Power-up RECALL duration	–	20	ms
t_{STORE} [33]	STORE cycle duration	–	8	ms
t_{DELAY} [34]	Time allowed to complete SRAM write cycle	–	25	ns
V_{SWITCH}	Low voltage trigger level for V_{CC}	–	2.90	V
V_{IODIS} [35]	I/O disable voltage on V_{CCQ}	–	1.50	V
$t_{VCCRISE}$ [36]	V_{CC} rise time	150	–	µs
V_{HDIS} [36]	$\overline{HSB}$ output disable voltage on V_{CC}	–	1.9	V
t_{LZHSB} [36]	$\overline{HSB}$ to output active time	–	5	µs
t_{HHHD} [36]	$\overline{HSB}$ high active time	–	500	ns

Switching Waveforms

Figure 9. AutoStore or Power-up RECALL[37]



Notes
32. $t_{HRECALL}$ starts from the time V_{CC} rises above V_{SWITCH}.
33. If an SRAM write has not taken place since the last non-volatile cycle, no AutoStore or Hardware STORE takes place.
34. On a Hardware STORE and AutoStore initiation, SRAM write operation continues to be enabled for time t_{DELAY}.
35. $\overline{HSB}$ is not defined below V_{IODIS} voltage.
36. These parameters are guaranteed by design and are not tested.
37. Read and write cycles are ignored during STORE, RECALL, and while V_{CC} is below V_{SWITCH}.
38. During power-up and power-down, $\overline{HSB}$ glitches when $\overline{HSB}$ pin is pulled up through an external resistor.

Software Controlled STORE/RECALL Cycle

Over the Operating Range

Parameters[39, 40]	Description	25 ns		45 ns		Unit
		Min	Max	Min	Max	
t_{RC}	STORE/RECALL initiation cycle time	25	–	45	–	ns
t_{SA}	Address setup time	0	–	0	–	ns
t_{CW}	Clock pulse width	20	–	30	–	ns
t_{HA}	Address hold time	0	–	0	–	ns
t_{RECALL}	RECALL duration	–	200	–	200	µs

Switching Waveforms

Figure 10. $\overline{CE}$ and $\overline{OE}$ Controlled Software STORE/RECALL Cycle [40]

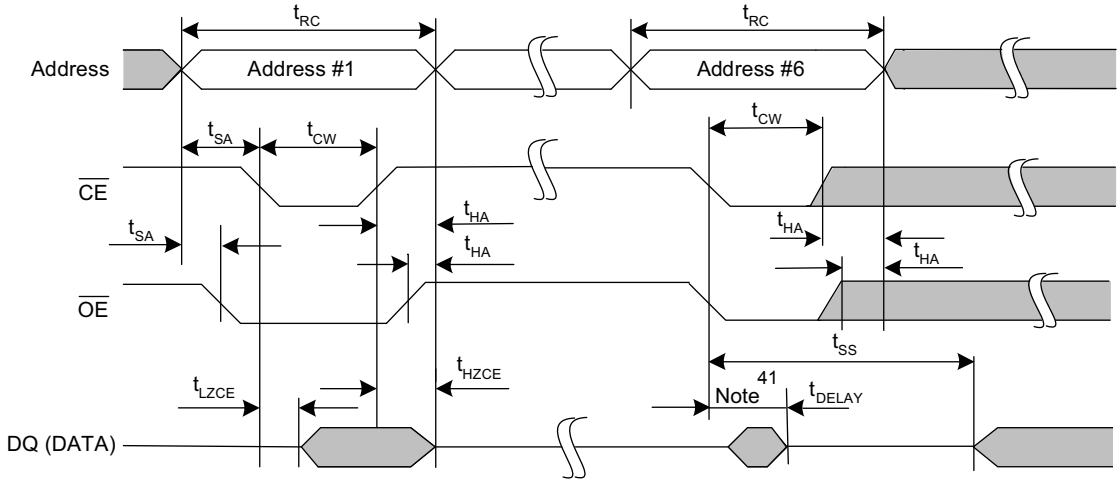
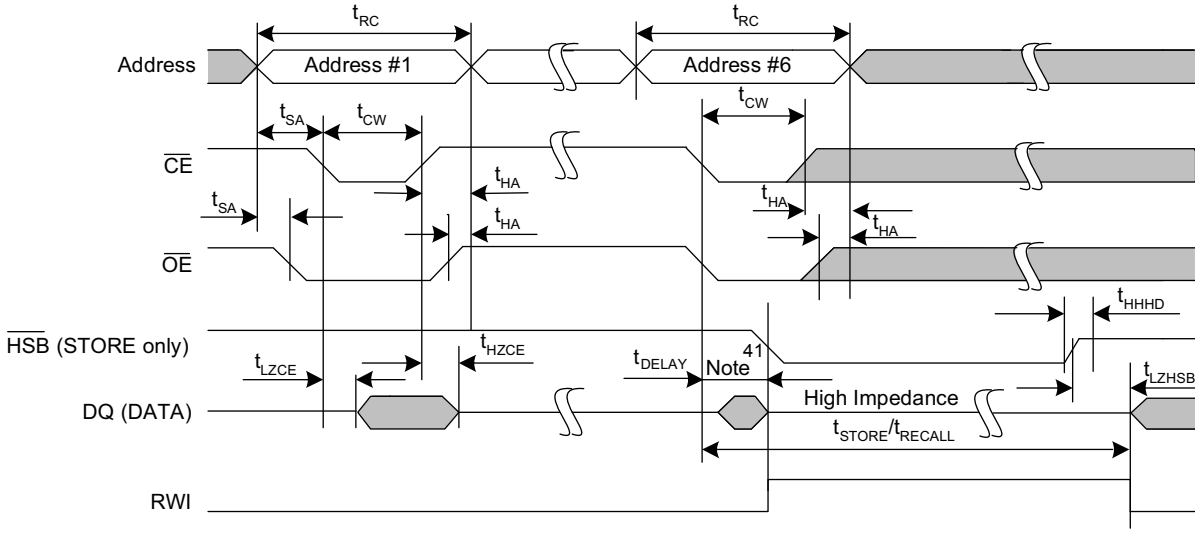


Figure 11. AutoStore Enable / Disable Cycle



Notes
39. The software sequence is clocked with $\overline{CE}$ controlled or $\overline{OE}$ controlled reads.
40. The six consecutive addresses must be read in the order listed in Table 1 on page 5. $\overline{WE}$ must be HIGH during all six consecutive cycles.
41. DQ output data at the sixth read may be invalid since the output is disabled at t_{DELAY} time.

Hardware STORE Cycle

Over the Operating Range

Parameters	Description	CY14V101LA/CY14V101NA		Unit
		Min	Max	
t_{DHSB}	$\overline{HSB}$ to output active time when write latch not set	–	25	ns
t_{PHSB}	Hardware STORE pulse width	15	–	ns
t_{SS} [42, 43]	Soft sequence processing time	–	100	µs

Switching Waveforms

Figure 12. Hardware STORE Cycle [44]

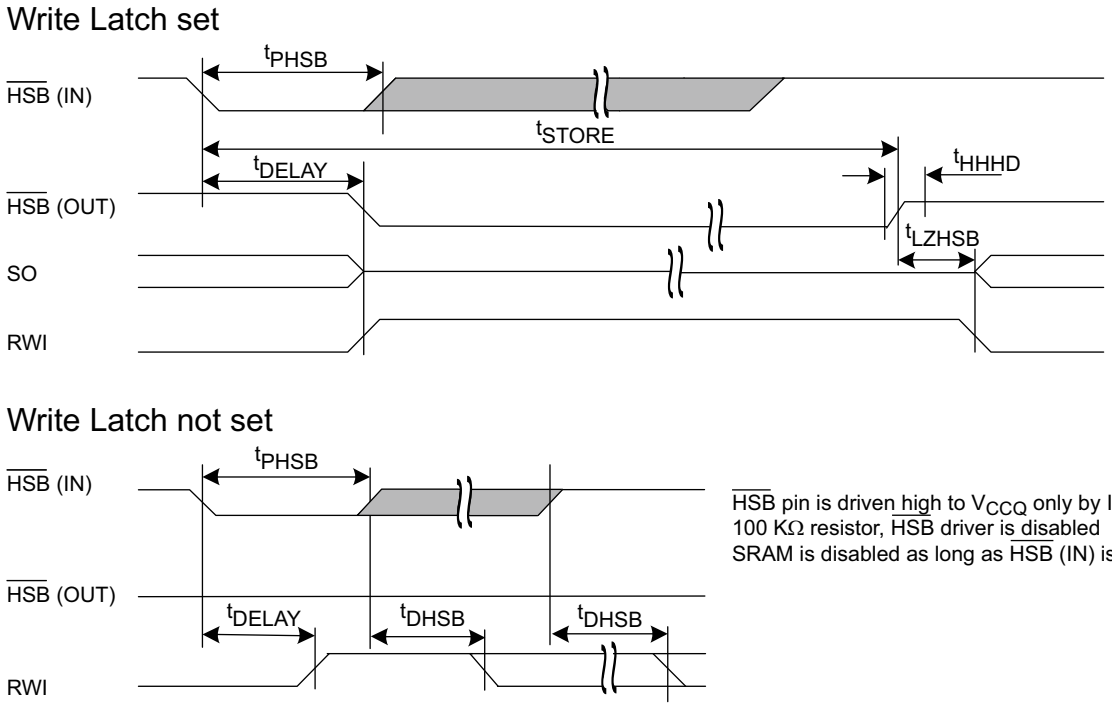
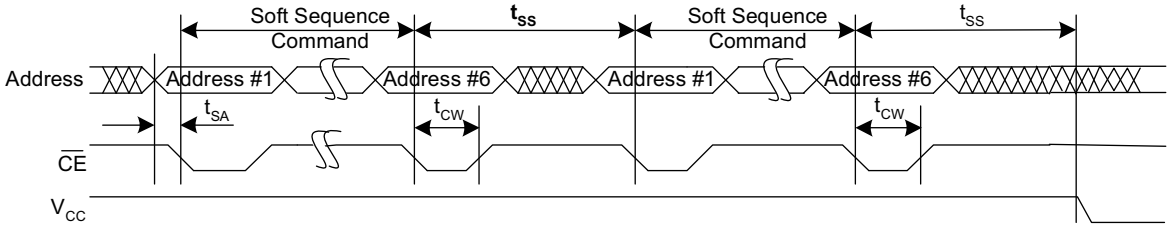


Figure 13. Soft Sequence Processing [42, 43]



Notes
42. This is the amount of time it takes to take action on a soft sequence command. V_{CC} and V_{CCQ} power must remain HIGH to effectively register command.
43. Commands such as STORE and RECALL lock out I/O until operation is complete which further increases this time. See the specific command.
44. If an SRAM write has not taken place since the last non-volatile cycle, no AutoStore or Hardware STORE takes place.

Truth Table For SRAM Operations

$\overline{HSB}$ must remain HIGH for SRAM operations.

Table 2. Truth Table for × 8 Configuration

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs[45]	Mode	Power
H	X	X	High Z	Deselect / Power-down	Standby
L	H	L	Data out (DQ_0–DQ_7)	Read	Active
L	H	H	High Z	Output disabled	Active
L	L	X	Data in (DQ_0–DQ_7)	Write	Active

Table 3. Truth Table for × 16 Configuration

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$[46]	$\overline{BLE}$[46]	Inputs/Outputs[45]	Mode	Power
H	X	X	X	X	High Z	Deselect / Power-down	Standby
L	X	X	H	H	High Z	Output disabled	Active
L	H	L	L	L	Data out (DQ_0–DQ_{15})	Read	Active
L	H	L	H	L	Data out (DQ_0–DQ_7); DQ_8–DQ_{15} in High Z	Read	Active
L	H	L	L	H	Data out (DQ_8–DQ_{15}); DQ_0–DQ_7 in High Z	Read	Active
L	H	H	L	L	High Z	Output disabled	Active
L	H	H	H	L	High Z	Output disabled	Active
L	H	H	L	H	High Z	Output disabled	Active
L	L	X	L	L	Data in (DQ_0–DQ_{15})	Write	Active
L	L	X	H	L	Data in (DQ_0–DQ_7); DQ_8–DQ_{15} in High Z	Write	Active
L	L	X	L	H	Data in (DQ_8–DQ_{15}); DQ_0–DQ_7 in High Z	Write	Active

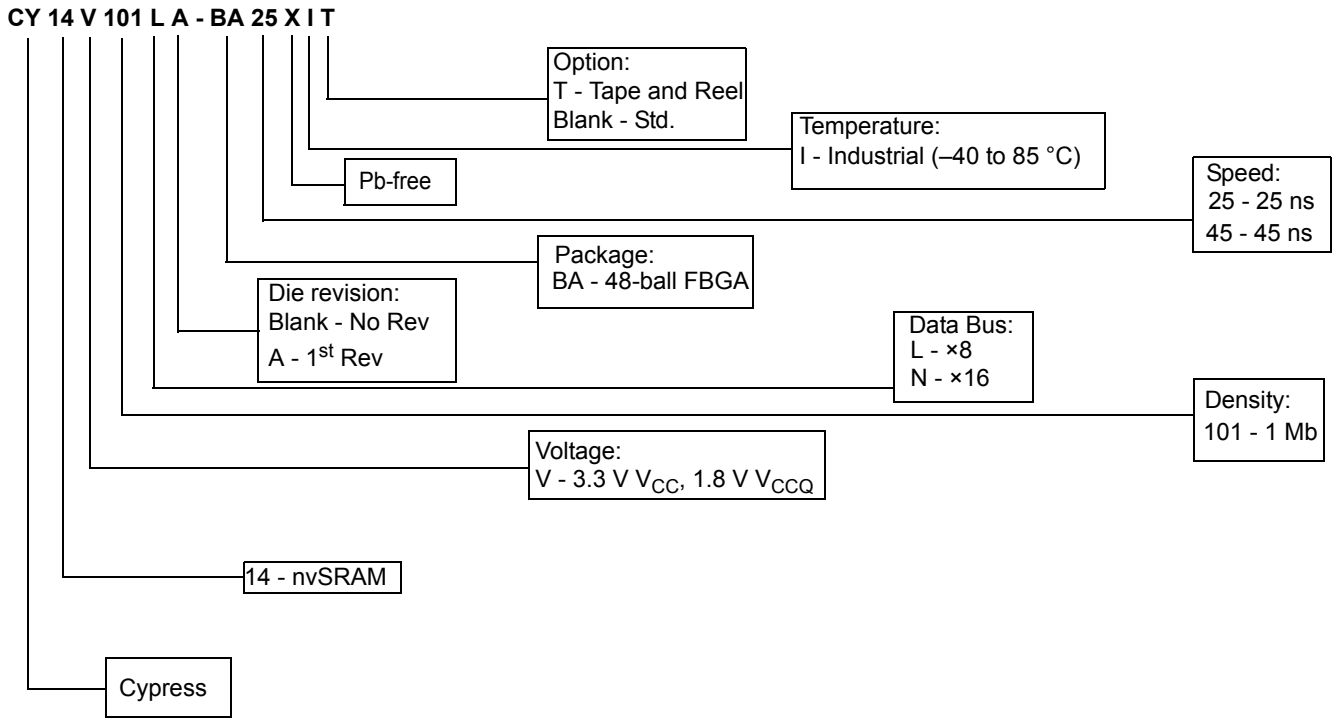
Notes
45. Data DQ_0–DQ_7 for × 8 configuration and Data DQ_0–DQ_{15} for × 16 configuration.
46. $\overline{BHE}$ and $\overline{BLE}$ are applicable for × 16 configuration only.

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
25	CY14V101LA-BA25XIT	51-85128	48-ball FBGA	Industrial
	CY14V101LA-BA25XI			
	CY14V101NA-BA25XIT			
	CY14V101NA-BA25XI			
45	CY14V101LA-BA45XIT			
	CY14V101LA-BA45XI			
	CY14V101NA-BA45XIT			
	CY14V101NA-BA45XI			

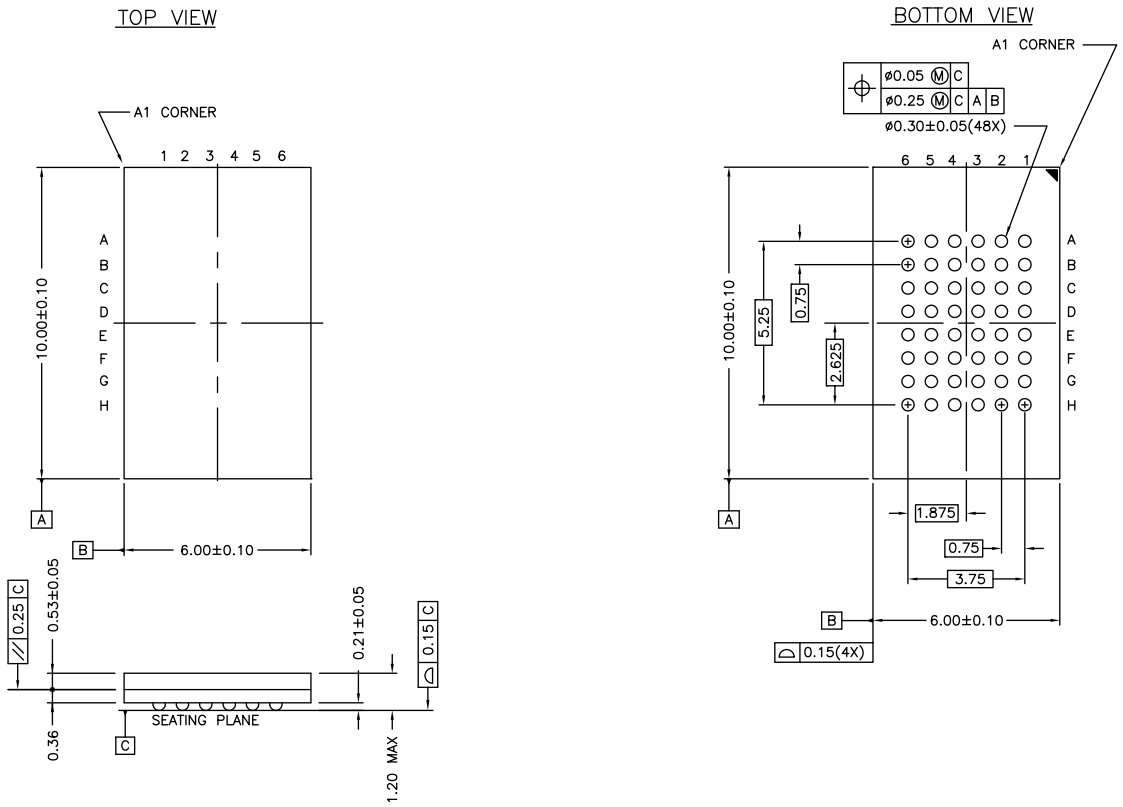
All parts are Pb-free. The above table contains final information. Contact your local Cypress sales representative for availability of these parts.

Ordering Code Definitions



Package Diagrams

Figure 14. 48-ball FBGA (6 × 10 × 1.2 mm) BA48B Package Outline, 51-85128



51-85128 *F

Acronyms

Acronym	Description
$\overline{BHE}$	Byte High Enable
$\overline{BLE}$	Byte Low Enable
$\overline{CE}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
EIA	Electronic Industries Alliance
FBGA	Fine-Pitch Ball Grid Array
$\overline{HSB}$	Hardware STORE Busy
I/O	Input/Output
nvSRAM	non-volatile Static Random Access Memory
$\overline{OE}$	Output Enable
SRAM	Static Random Access Memory
RoHS	Restriction of Hazardous Substances
RWI	Read and Write Inhibited
$\overline{WE}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
kΩ	kilohm
µA	microampere
mA	milliampere
mm	millimeter
µF	microfarad
MHz	megahertz
µs	microsecond
ms	millisecond
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY14V101LA/CY14V101NA, 1-Mbit (128 K × 8/64 K × 16) nvSRAM Document Number: 001-53953				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	2729117	GVCH / AESA	07/02/09	New data sheet.
*A	2765890	GVCH	09/18/09	Removed commercial temperature related specs Changed part number from CY14A101L/CY14A101N to CY14V101LA/CY14V101NA Removed 20 ns Access speed specs Figure 3: Updated Autostore Mode Page 4; Updated Hardware STORE ($\overline{HSB}$) Operation description Page 5; Updated Software STORE Operation description Added I_{CCQ1} and I_{CCQ3} for V_{CCQ} operation Updated V_{IH}/V_{IL} as 70%/30% of V_{CCQ} Updated V_{OH} test condition Updated footnote 24 and added footnote 25, 30 Updated V_{IODIS} parameter value from 1.6 V to 1.5 V Updated Footnote 10 Added Contents on page 2
*B	2767333	GVCH / PYRS	01/06/10	Removed 44-TSOP II package related specs Changed Latch Up Current from 200 mA to 140 mA Changed STORE cycles to QuantumTrap from 200 K to 1 Million Added Contents
*C	2923525	GVCH	04/27/10	Pin Definitions: Added more clarity on $\overline{HSB}$ pin operation Hardware STORE Operation: Added more clarity on $\overline{HSB}$ pin operation Table 1: Added more clarity on status of $\overline{BHE}$/$\overline{BLE}$ pin operation Updated $\overline{HSB}$ pin operation in Figure 9 Updated footnote 24
*D	2999981	GVCH	08/04/2010	Changed datasheet status from “Preliminary” to “Final”
*E	3033088	GVCH	09/22/2010	Changed I_{SB} and I_{CC4} value from 5 mA to 8 mA Added Acronyms and Units of Measure table Updated as per new template
*F	3123639	GVCH	12/30/2010	Removed Note “Address expansion for 16 Mbit. NC pin not connected to die.” in page 3 as 16 Mb address expansion is not supported in 48-ball FBGA package. Added CY14V101LA-BA25XI and CY14V101NA-BA25XI parts in Ordering Information.
*G	3150308	GVCH	01/21/2011	Updated input capacitance for $\overline{BHE}$ and $\overline{BLE}$ pin Updated input and output capacitance for $\overline{HSB}$ pin Updated Ordering Information
*H	3301833	GVCH	07/04/2011	Updated DC Electrical Characteristics (Added Note 13 and referred the same note in V_{CAP} parameter). Updated AC Switching Characteristics (Added Note 16 and referred the same note in Parameters). Updated Thermal Resistance (Values of Θ_{JA} and Θ_{JC} for 48-ball FBGA package). Updated Package Diagrams.
*I	3759015	GVCH	09/28/2012	Removed Best Practices. Updated Maximum Ratings (Removed “Ambient temperature with power applied” and included “Maximum junction temperature”). Updated DC Electrical Characteristics (Added V_{VCAP} parameter and its details, added Note 14 and referred the same note in V_{VCAP} parameter, also referred Note 15 in V_{VCAP} parameter).

Document History Page (continued)

Document Title: CY14V101LA/CY14V101NA, 1-Mbit (128 K × 8/64 K × 16) nvSRAM Document Number: 001-53953				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
*J	4075544	GVCH	07/24/2013	Updated Pin Definitions: Updated description of $\overline{HSB}$ pin (Added more clarity). Updated Device Operation: Updated AutoStore Operation (Removed sentence “The $\overline{HSB}$ signal is monitored by the system to detect if an AutoStore cycle is in progress.”). Updated in new template. Completing Sunset Review.
*K	4563189	GVCH	11/06/2014	Added related documentation hyperlink in page 1

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