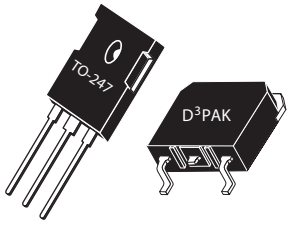
APT42F50B
APT42F50S

500V, 42A, 0.13Ω Max, t_{rr}, ≤260ns

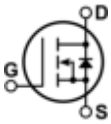
N-Channel FREDFET

Power MOS 8™ is a high speed, high voltage N-channel switch-mode power MOSFET. This 'FREDFET' version has a drain-source (body) diode that has been optimized for high reliability in ZVS phase shifted bridge and other circuits through reduced t_{rr}, soft recovery, and high recovery dv/dt capability. Low gate charge, high gain, and a greatly reduced ratio of C_{rss}/C_{iss} result in excellent noise immunity and low switching loss. The intrinsic gate resistance and capacitance of the poly-silicon gate structure help control di/dt during switching, resulting in low EMI and reliable paralleling, even when switching at very high frequency.



APT42F50B **APT42F50S**

Single die FREDFET



FEATURES

- **Fast switching with low EMI**
- **Low t_{rr} for high reliability**
- **Ultra low C_{rss} for improved noise immunity**
- **Low gate charge**
- **Avalanche energy rated**
- **RoHS compliant**

TYPICAL APPLICATIONS

- **ZVS phase shifted and other full bridge**
- **Half bridge**
- **PFC and other boost converter**
- **Buck converter**
- **Single and two switch forward**
- **Flyback**

Absolute Maximum Ratings

Symbol	Parameter	Ratings	Unit
I_D	Continuous Drain Current @ T_C = 25°C	42	A
	Continuous Drain Current @ T_C = 100°C	27	
I_{DM}	Pulsed Drain Current ①	135	
V_{GS}	Gate-Source Voltage	±30	V
E_{AS}	Single Pulse Avalanche Energy ②	930	mJ
I_{AR}	Avalanche Current, Repetitive or Non-Repetitive	21	A

Thermal and Mechanical Characteristics

Symbol	Characteristic	Min	Typ	Max	Unit
P_D	Total Power Dissipation @ T_C = 25°C			625	W
$R_{\theta JC}$	Junction to Case Thermal Resistance			0.20	°C/W
$R_{\theta CS}$	Case to Sink Thermal Resistance, Flat, Greased Surface		0.11		
T_J,T_{STG}	Operating and Storage Junction Temperature Range	-55		150	°C
T_L	Soldering Temperature for 10 Seconds (1.6mm from case)			300	
W_T	Package Weight		0.22		oz
			6.2		g
Torque	Mounting Torque (TO-247 Package), 6-32 or M3 screw			10	in·lbf
				1.1	N·m

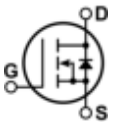
Static Characteristics — T_J = 25°C unless otherwise specified — AP42F50B_S

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
$V_{BR(DSS)}$	Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 250μA		500			V
$\Delta V_{BR(DSS)}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	Reference to 25°C, I_D = 250μA			0.60		V/°C
$R_{DS(on)}$	Drain-Source On Resistance③	V_{GS} = 10V, I_D = 21A			0.11	0.13	Ω
$V_{GS(th)}$	Gate-Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 1mA		2.5	4	5	V
$\Delta V_{GS(th)}/\Delta T_J$	Threshold Voltage Temperature Coefficient				-10		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 500V, V_{GS} = 0V	T_J = 25°C			250	μA
			T_J = 125°C			1000	
I_{GSS}	Gate-Source Leakage Current	V_{GS} = ±30V				±100	nA

Dynamic Characteristics — T_J = 25°C unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
g_{fs}	Forward Transconductance	V_{DS} = 50V, I_D = 21A		32		S
C_{iss}	Input Capacitance	V_{GS} = 0V, V_{DS} = 25V f = 1MHz		6810		pF
C_{rss}	Reverse Transfer Capacitance			90		
C_{oss}	Output Capacitance			735		
$C_{o(cr)}$ ④	Effective Output Capacitance, Charge Related	V_{GS} = 0V, V_{DS} = 0V to 333V		425		
$C_{o(er)}$ ⑤	Effective Output Capacitance, Energy Related			215		
Q_g	Total Gate Charge	V_{GS} = 0 to 10V, I_D = 21A, V_{DS} = 250V		170		nC
Q_{gs}	Gate-Source Charge			38		
Q_{gd}	Gate-Drain Charge			80		
$t_{d(on)}$	Turn-On Delay Time	**Resistive Switching** V_{DD} = 333V, I_D = 21A R_G = 4.7Ω⑥, V_{GG} = 15V		29		ns
t_r	Current Rise Time			35		
$t_{d(off)}$	Turn-Off Delay Time			80		
t_f	Current Fall Time			26		

Source-Drain Diode Characteristics

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
I_S	Continuous Source Current (Body Diode)	MOSFET symbol showing the integral reverse p-n junction diode (body diode) 				42	A
I_{SM}	Pulsed Source Current (Body Diode)①					135	
V_{SD}	Diode Forward Voltage	I_{SD} = 21A, T_J = 25°C, V_{GS} = 0V				1.2	V
t_{rr}	Reverse Recovery Time	I_{SD} = 21A③ di_{SD}/dt = 100A/μs V_{DD} = 100V	T_J = 25°C		225	260	ns
			T_J = 125°C		400	480	
Q_{rr}	Reverse Recovery Charge		T_J = 25°C		1.00		μC
			T_J = 125°C		2.50		
I_{rrm}	Reverse Recovery Current		T_J = 25°C		9.1		A
			T_J = 125°C		12.9		
dv/dt	Peak Recovery dv/dt	I_{SD} ≤ 21A, di/dt ≤1000A/μs, V_{DD} = 333V, T_J = 125°C				20	V/ns

① Repetitive Rating: Pulse width and case temperature limited by maximum junction temperature.

② Starting at T_J = 25°C, L = 4.22mH, R_G = 25Ω, I_{AS} = 21A.

③ Pulse test: Pulse Width < 380μs, duty cycle < 2%.

④ $C_{o(cr)}$ is defined as a fixed capacitance with the same stored charge as C_{OSS} with V_{DS} = 67% of $V_{(BR)DSS}$.

⑤ $C_{o(er)}$ is defined as a fixed capacitance with the same stored energy as C_{OSS} with V_{DS} = 67% of $V_{(BR)DSS}$. To calculate $C_{o(er)}$ for any value of V_{DS} less than $V_{(BR)DSS,}$ use this equation: $C_{o(er)}$ = -1.84E-7/V_{DS}^2 + 3.75E-8/V_{DS} + 1.05E-10.

⑥ R_G is external gate resistance, not including internal gate resistance or gate driver impedance. (MIC4452)

Microsemi reserves the right to change, without notice, the specifications and information contained herein.

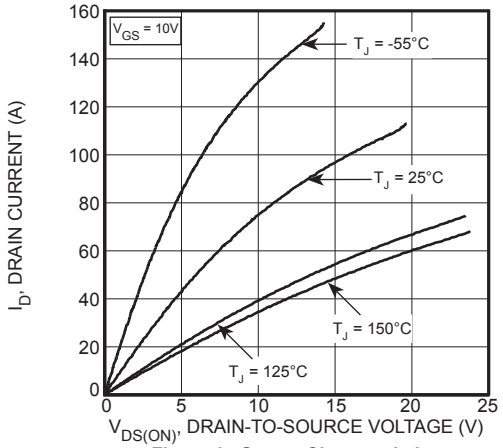


Figure 1, Output Characteristics

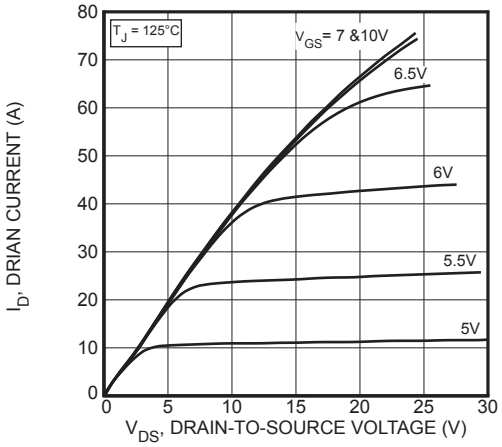


Figure 2, Output Characteristics

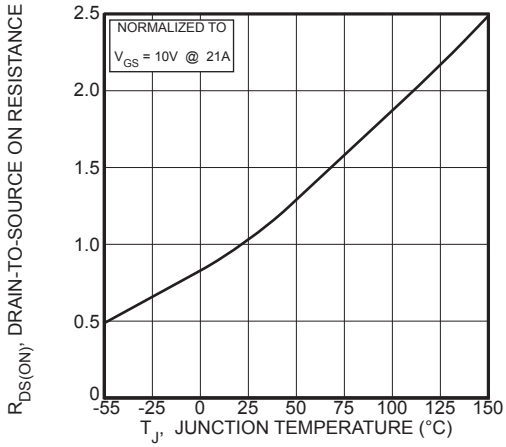


Figure 3, $R_{DS(ON)}$ vs Junction Temperature

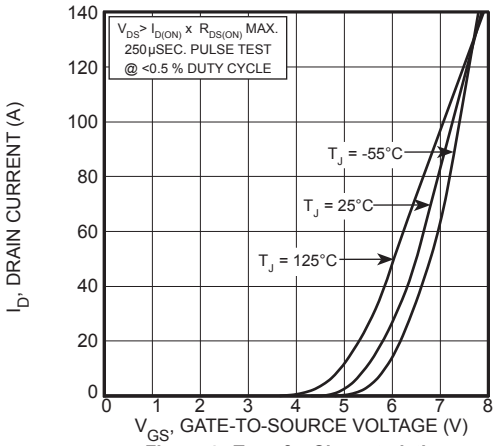


Figure 4, Transfer Characteristics

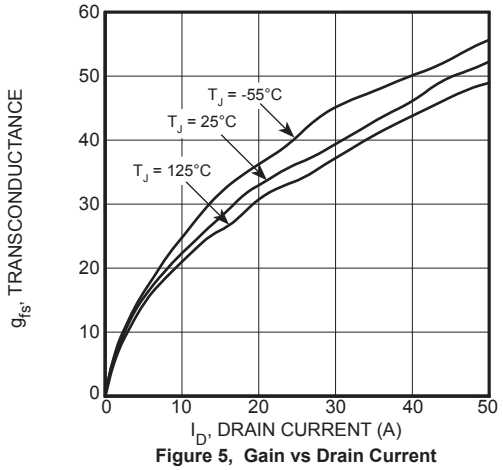


Figure 5, Gain vs Drain Current

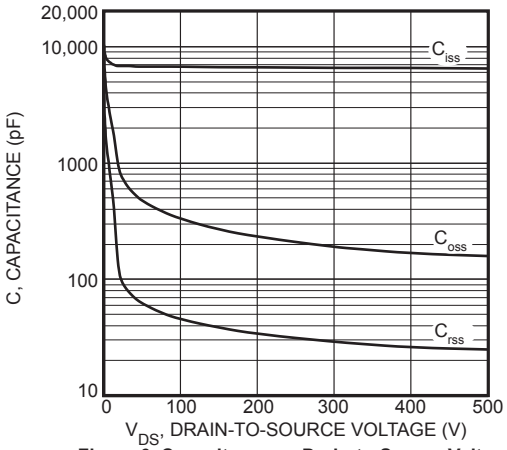


Figure 6, Capacitance vs Drain-to-Source Voltage

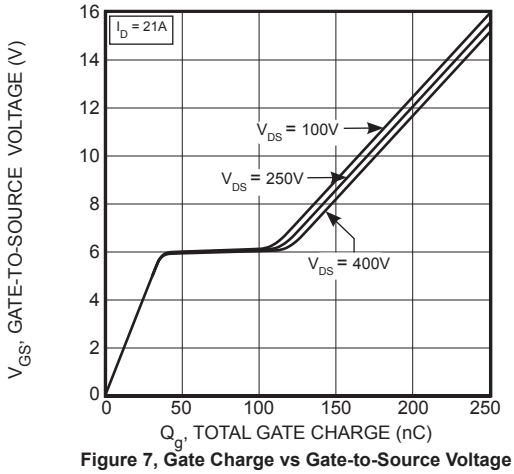


Figure 7, Gate Charge vs Gate-to-Source Voltage

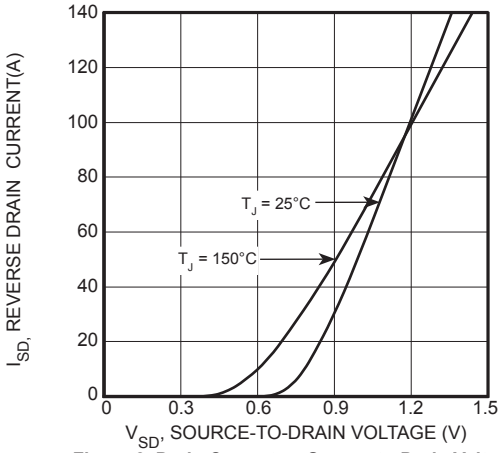


Figure 8, Drain Current vs Source-to-Drain Voltage

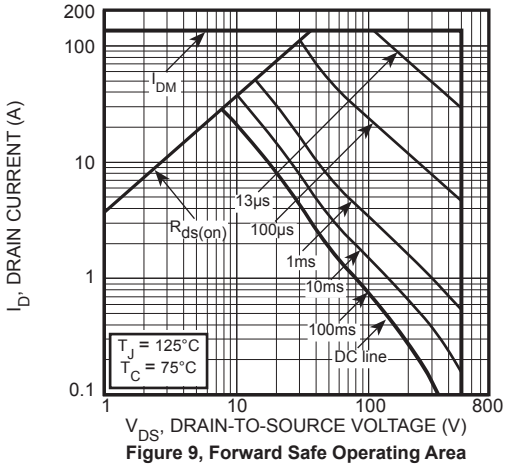


Figure 9, Forward Safe Operating Area

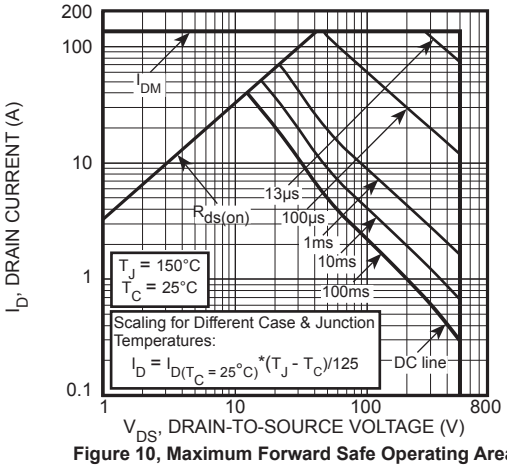


Figure 10, Maximum Forward Safe Operating Area

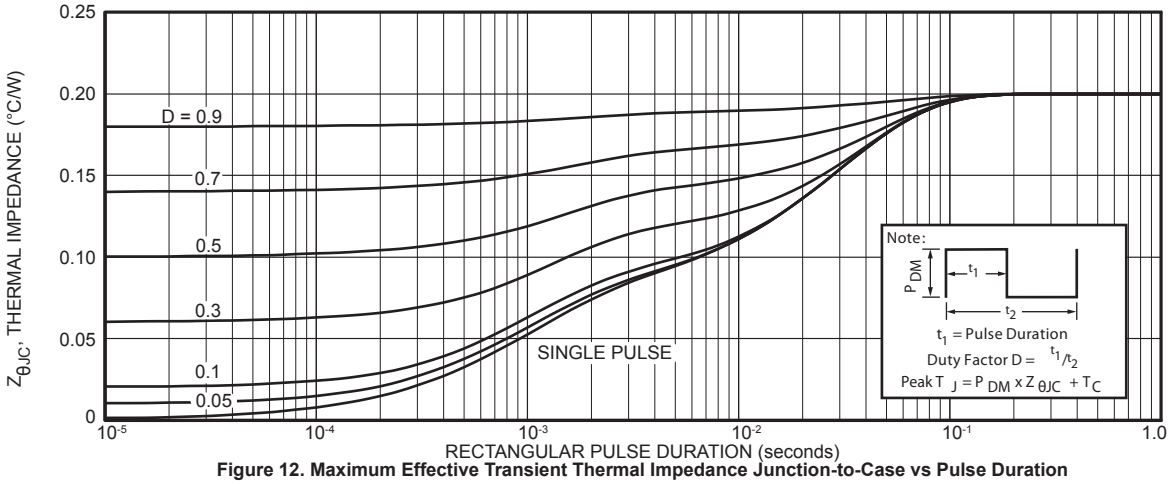
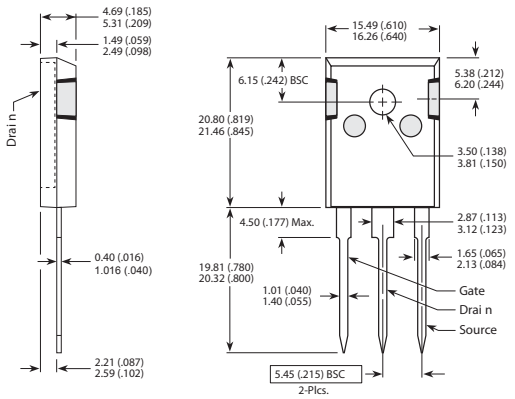


Figure 12. Maximum Effective Transient Thermal Impedance Junction-to-Case vs Pulse Duration

TO-247 (B) Package Outline

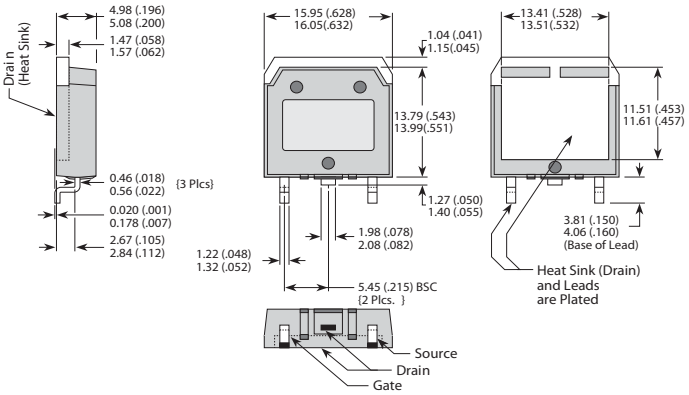
(e1) SAC: Tin, Silver, Copper



Dimensions in Millimeters (Inches)

D^3PAK Package Outline

(e3) 100% Sn Plated



Dimensions in Millimeters (Inches)