Datasheet

Lyra P

Version 2.1

Revision History

Version	Date	Notes	Contributors	Approver
1.0	18 Feb 2022	Initial release.	Raj Khatri, Dave Drogowski	Jonathan Kaye
1.1	10 June 2022	Updates to 5 Reference Diagrams and added 5.3 Boot.	Greg Leach, Raj Khatri, Dave Drogowski	Jonathan Kaye
1.2	7 Sept 2022	Fixed typo in 2 Ordering Information.	Dave Drogowski	Jonathan Kaye
1.3	10 Feb 2023	Added new Wireless Xpress SKU information. Updated section 2 Ordering Information and 5.3 Boot for Wireless Xpress part (453-00147).	Greg Leach	Jonathan Kaye
1.4	30 Oct 2024	Updated Bluetooth SIG Qualification	Dave Drogowski	Jonathan Kaye
2.0	24 Jan 2025	Ezurio rebranding	Sue White	Dave Drogowski
2.1	22 Dec 2025	Updated to MSL 3	Dave Drogowski	Jonathan Kaye

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1 Introduction

The Lyra P is a module designed and built to meet the performance, security, and reliability requirements of battery-powered IoT products running on Bluetooth networks.

Based on the EFR32BG22 SoC, the Lyra P enables Bluetooth® Low Energy connectivity while delivering best-in-class RF range and performance, future-proof capability for feature and OTA firmware updates, enhanced security features, and low energy consumption.

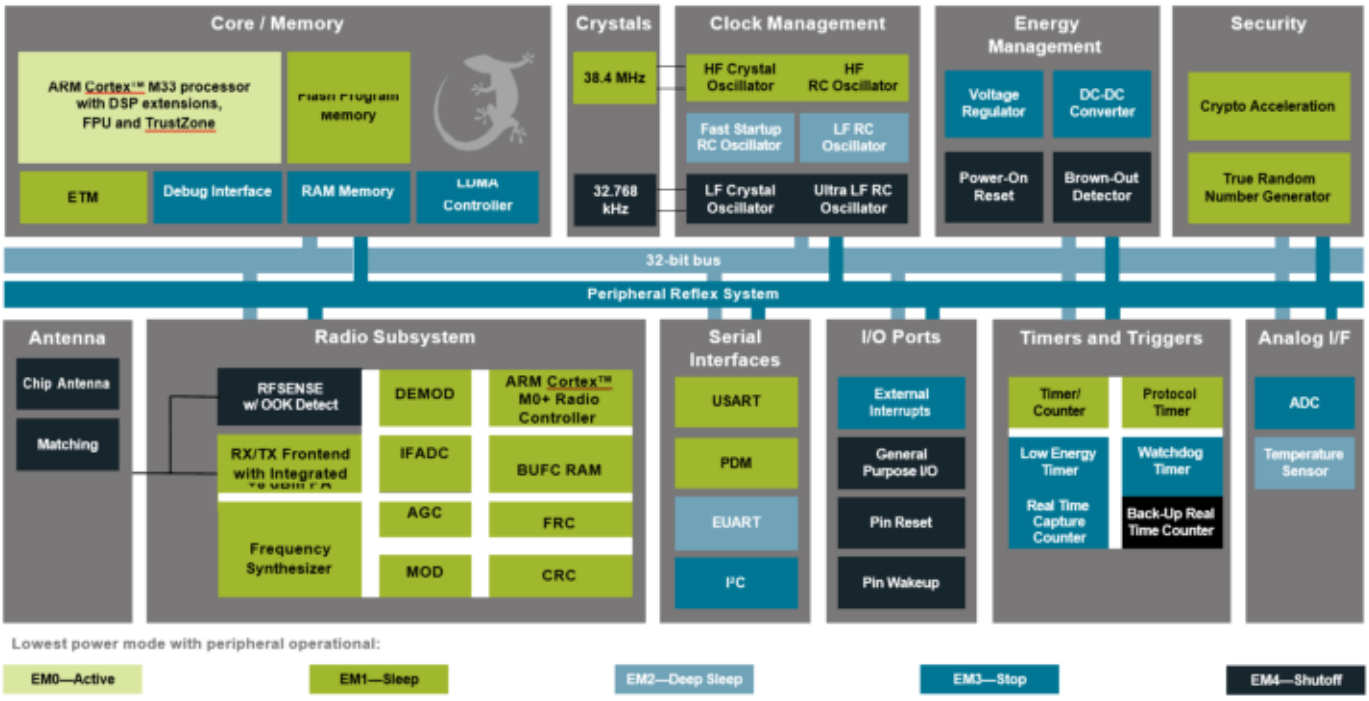
Lyra P modules are a full solution that comes with fully upgradeable, robust software stacks, world-wide regulatory certifications, advanced development and debugging tools, and support that will minimize and simplify the engineering and development of your end-products helping to accelerate their time-to-market.

The Lyra P is intended for a broad range of applications, including:

- Asset Tags and Beacons
- Sports, Fitness, and Wellness devices
- Portable Medical
- Connected Home
- Industrial and Building Automation
- Bluetooth mesh Low Power Node

1.1 Key Features

- Bluetooth 5.3
- Bluetooth mesh Low Power Node
- Built-in antenna
- Up to 8 dBm TX power
- -98.9 dBm BLE RX sensitivity at 1 Mbps
- 32-bit ARM Cortex-M33 core at up to 76.8 MHz
- 512/32 kB of Flash/RAM memory
- Optimal selection of MCU peripherals
- Up to 24 GPIO pins
- 12.9 mm x 15.0 mm



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1.2 Hardware Features

- **Supported Protocols**
  - Bluetooth Low Energy (Bluetooth 5.3)
    - Direction finding
    - 1M, 2M and LE Coded PHYs
  - Bluetooth Mesh Low Power Node
- **Wireless System-on-Chip**
  - 2.4 GHz radio
  - TX power up to +8 dBm
  - High-performance 32-bit ARM Cortex-M33® with DSP instruction and floating-point unit for efficient signal processing
  - 512 kB flash program memory
  - 32 kB RAM data memory
  - Embedded Trace Macrocell (ETM) for advanced debugging
- **High-Receiver Performance**
  - -106.7 dBm sensitivity (0.1% BER) at 125 kbps GFSK
  - -102.5 dBm sensitivity (0.1% BER) at 500 kbps GFSK
  - -98.9 dBm sensitivity (0.1% BER) at 1 Mbps GFSK
  - -96.2 dBm sensitivity (0.1% BER) at 2 Mbps GFSK
- **Low-Energy Consumption**
  - 4.3 mA RX current at 1 Mbps GFSK
  - 4.8 mA TX current at 0 dBm output power
  - 10.6 mA TX current at 8 dBm output power
  - 26 µA/MHz in Active Mode (EM0)
  - 1.40 µA EM2 DeepSleep current (RTCC running from LFXO, Full RAM retention)
- **Regulatory Certifications**
  - FCC
  - CE
  - ISED
  - MIC/TELEC
  - KCC
- **Wide Operating Range**
  - 1.8 to 3.8 V
  - -40 to +105°C
- **Dimensions**
  - 12.9 mm x 15.0 mm x 2.2 mm
- **Security Features**
  - Secure Boot with Root of Trust and Secure Loader (RTSL)
  - Hardware Cryptographic Acceleration for AES128/256, SHA-1, SHA-2 (up to 256-bit), ECC (up to 256-bit), ECDSA, and ECDH
  - True Random Number Generator (TRNG) compliant with NIST SP800-90 and AIS-31
  - ARM® TrustZone®
  - Secure Debug with lock/unlock
- **Wide Selection of MCU Peripherals**
  - Analog to Digital Converter (ADC)
    - 12-bit @ 1 Msps
    - 16-bit @ 76.9 ksps
  - Up to 24 General Purpose I/O pins with output state retention and asynchronous interrupts
  - 8 Channel DMA Controller
  - 12 Channel Peripheral Reflex System (PRS)
  - 4 × 16-bit Timer/Counter with 3 Compare/Capture/PWM channels
  - 1 × 32-bit Timer/Counter with 3 Compare/Capture/PWM channels
  - 32-bit Real Time Counter
  - 24-bit Low Energy Timer for waveform generation
  - 1 × Watchdog Timer
  - 2 × Universal Synchronous/Asynchronous Receiver/Transmitter (UART/SPI/SmartCard (ISO 7816)/IrDA/I2S)
  - 1 × Enhanced Universal Asynchronous Receiver/Transmitter (EUART)
  - 2 × I2C interface with SMBus support
  - Digital microphone interface (PDM)
  - RFSENSE with selective OOK mode

1.3 Firmware Options

The Lyra series supports three different firmware options for software development:

AT Command Set – Fully featured and extensible to suit any developer's needs.

- Proven over 5+ years
- Basic Bluetooth LE cable replacement
- Simplest implementation possible
- Includes all key features of Wireless Xpress and more

Wireless Xpress – Frozen at current release, path for existing Silicon Labs customers

- Basic Bluetooth LE cable replacement
- Secure FOTA capable FW
- Xpress command API for iOS & Android

C Code – Full software development with Silicon Labs SDK and Toolchain

- Native C code development
- Use Simplicity Studio IDE
- Full functionality of Silicon Labs HW / SW

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2 Ordering Information

Table 1: Ordering Information

Part	Description
453-00090R	Lyra Series - Bluetooth v5.3 PCB Module with integrated antenna (Silicon Labs EFR32BG22) - Tape / Reel
453-00090C	Lyra Series - Bluetooth v5.3 PCB Module with integrated antenna (Silicon Labs EFR32BG22) – Cut / Tape
453-00147R	Lyra Series - Bluetooth v5.3 PCB Module, Integrated Antenna, Wireless Xpress FW (Silicon Labs EFR32BG22) - Tape / Reel
453-00147C	Lyra Series - Bluetooth v5.3 PCB Module, Integrated Antenna, Wireless Xpress FW (Silicon Labs EFR32BG22) – Cut / Tape
453-00090-K1	Lyra Series - Development Kit - Bluetooth v5.3 PCB Module with integrated antenna

Note: Part 453-00147 ships from the factory configured with Ezurio's Organizational Unique Identifier (OUI) (18-C2-93) in One Time Programmable memory. This is used as the basis for the part Bluetooth address.

Legacy BGX220P parts shipped with Silabs' OUI (60-A4-23).

3 System Overview

3.1 Block Diagram

The Lyra P module combines an energy friendly MCU with a highly integrated radio transceiver in a PCB module with a robust, integrated antenna. This section gives a short introduction to the features of the module.

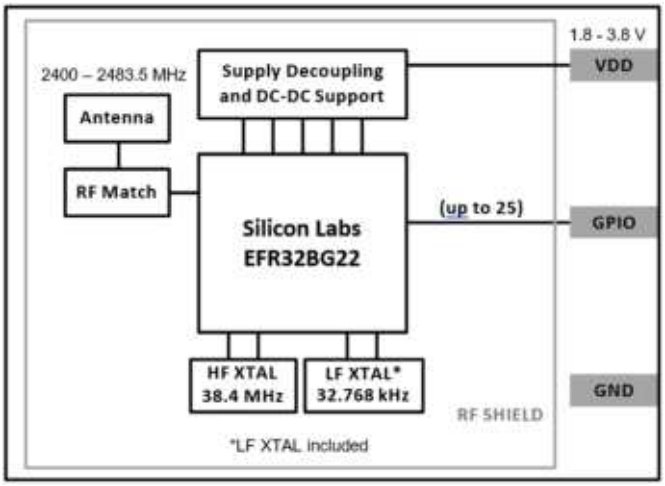


Figure 1: Lyra P Block Diagram

The block diagram for the Lyra P module is shown in Figure 1. The wireless module includes the EFR32BG22 wireless System on a Chip (SoC), required decoupling capacitors and inductors, 38.4 MHz and 32.768 kHz crystals, RF matching circuit, and integrated chip antenna.

A simplified internal schematic for the Lyra P module is shown in Figure 2.

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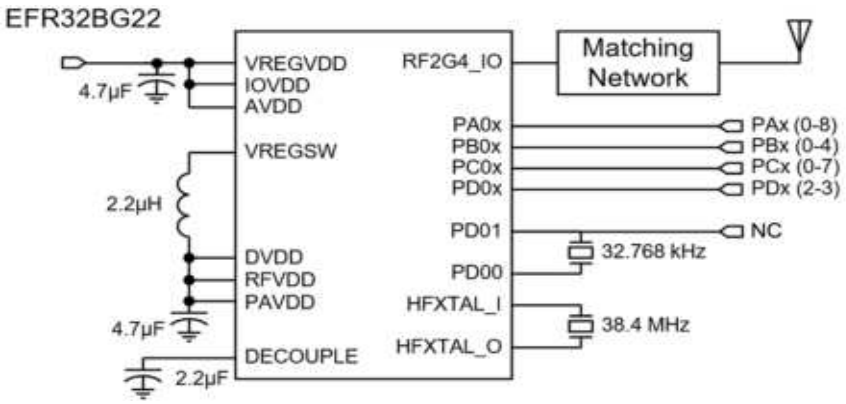


Figure 2: Lyra P Module Schematic

3.2 EFR32BG22 SoC

The EFR32BG22 SoC features a 32-bit ARM Cortex M33 core, a 2.4 GHz high-performance radio, 512 kB of flash memory, a rich set of MCU peripherals, and various clock management and serial interfacing options. Consult the EFR32xG22 Wireless Gecko Reference Manual and the EFR32BG22 Data Sheet for details.

3.3 Antenna

Lyra P modules include a ceramic chip antenna on board with the characteristics detailed in the table below.

Table 2: Antenna Efficiency and Peak Gain

Parameter	With optimal layout	Note
Efficiency	-1 dB	Antenna efficiency, gain and radiation pattern are highly dependent on the application PCB layout and mechanical design. Refer to Design Guidelines for recommendations to achieve optimal antenna performance.
Peak gain	1.86 dBi	

3.4 Power Supply

The Lyra P requires a single nominal supply level of 3.0 V to operate. All necessary decoupling and filtering components are included in the module.

4 Electrical Characteristics

All electrical parameters in all tables are specified under the following conditions, unless stated otherwise:

- Typical values are based on T_A=25 °C and VDD supply at 3.0 V, by production test and/or technology characterization.
- Radio performance numbers are measured in conducted mode, based on Silicon Laboratories reference designs using output power-specific external RF impedance-matching networks for interfacing to a 50 Ω antenna.
- Minimum and maximum values represent the worst conditions across supply voltage, process variation, and operating temperature, unless stated otherwise.

4.1 Absolute Maximum Ratings

Stresses beyond those listed below may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions beyond those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 3: Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Storage temperature range	T_{STG}		-40	—	+105	°C
Voltage on VDD supply pin	V_{DDMAX}		-0.3	—	3.8	V

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Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Voltage ramp rate on VDD supply pin	$V_{DDRAMPMAX}$		—	—	1.0	V / µs
DC voltage on any GPIO pin	V_{DIGPIN}		-0.3	—	V_{VDD} + 0.3	V
Total current into VDD pin	I_{VDDMAX}	Source	—	—	200	mA
Total current into GND pin	I_{GNDMAX}	Sink	—	—	200	mA
Current per I/O pin	I_{IOMAX}	Sink	—	—	50	mA
		Source	—	—	50	mA
Current for all I/O pins	$I_{IOALLMAX}$	Sink	—	—	200	mA
		Source	—	—	200	mA

4.2 General Operating Conditions

This table specifies the general operating temperature range and supply voltage range for all supplies. The minimum and maximum values of all other tables are specified over this operating range, unless otherwise noted.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating ambient temperature range	T_A	-G temperature grade	-40	—	+85	°C
		-N temperature grade	-40	—	+105	°C
VDD operating supply voltage	V_{VDD}	DCDC in regulation[1]	2.2	3.0	3.8	V
		DCDC in bypass	1.8	3.0	3.8	V
HCLK and SYSCLK frequency	f_{HCLK}	VSCALE2, MODE = WS1	—	—	76.8	MHz
		VSCALE2, MODE = WS0	—	—	40	MHz
		VSCALE1, MODE = WS0	—	—	40	MHz
PCLK frequency	f_{PCLK}	VSCALE2	—	—	50	MHz
		VSCALE1	—	—	40	MHz
EM01 Group A clock frequency	$f_{EM01GRPACLK}$	VSCALE2	—	—	76.8	MHz
		VSCALE1	—	—	40	MHz
EM01 Group B clock frequency	$f_{EM01GRPBCLK}$	VSCALE2	—	—	76.8	MHz
		VSCALE1	—	—	40	MHz
Radio HCLK frequency	f_{RHCLK}	VSCALE2 or VSCALE1	—	38.4	—	MHz

Note:

1. The supported maximum V_{VDD} in regulation mode is a function of temperature and 10-year lifetime average load current. See more details in DC-DC Operating Limits.

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4.2.1 DC-DC Operating Limits

The maximum supported voltage on the VDD supply pin is limited under certain conditions. Maximum input voltage is a function of temperature and the average load current over a 10-year lifetime. Figure 3 shows the safe operating region under specific conditions. Exceeding this safe operating range may impact the reliability and performance of the DC-DC converter.

The average load current for an application can typically be determined by examining the current profile during the time the device is powered. For example, an application that is continuously powered which spends 99% of the time asleep consuming 2 µA and 1% of the time active and consuming 10 mA has an average lifetime load current of about 102 µA.

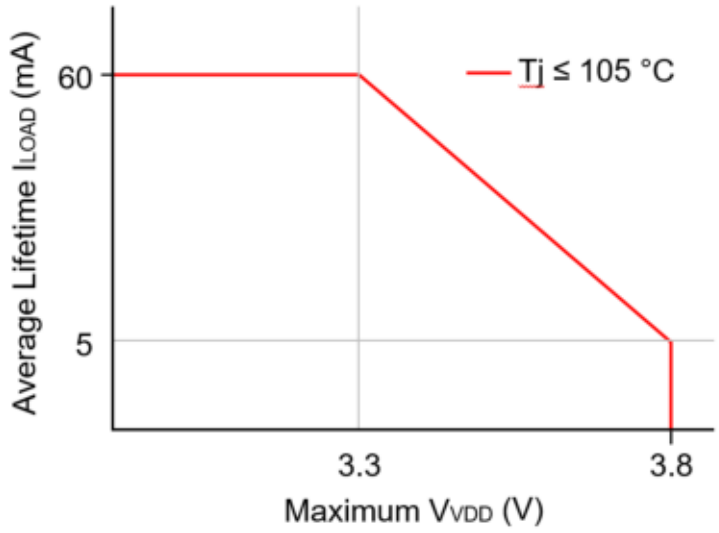


Figure 3: Lifetime average load current limit vs. maximum input voltage

The minimum input voltage for the DC-DC in EM0/EM1 mode is a function of the maximum load current, and the peak current setting. Figure 4 shows the max load current vs. input voltage for different DC-DC peak inductor current settings.

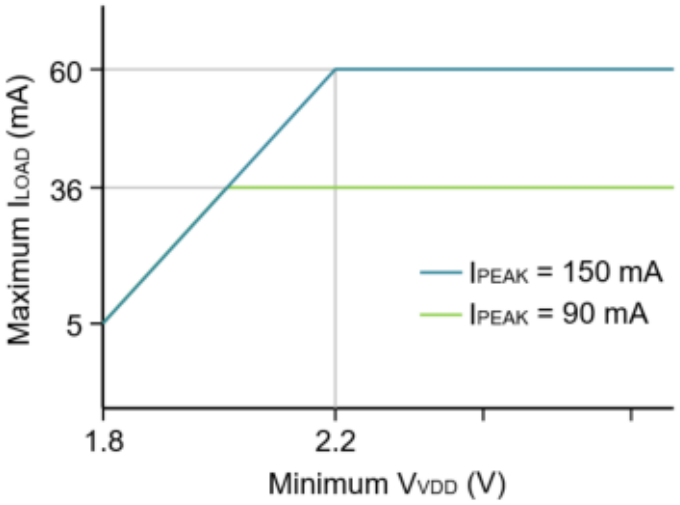


Figure 4: Transient maximum load current vs. Minimum input voltage

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4.3 MCU Current Consumption with 3 V Supply

Unless otherwise indicated, typical conditions are: Module supply voltage = 3.0 V. Voltage scaling level = VSCALE1. T_A = 25 °C. Mini mum and maximum values in this table represent the worst conditions across process variation at T_A = 25 °C.

Table 4: MCU Current Consumption with 3 V Supply

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 mode with all peripherals disabled	I_{ACTIVE}	76.8 MHz HFRCO w/ DPLL referenced to 38.4 MHz crystal, CPU running while loop from flash, VSCALE2	—	27	—	µA/MHz
		76.8 MHz HFRCO w/ DPLL referenced to 38.4 MHz crystal, CPU running CoreMark loop from flash, VSCALE2	—	37	—	µA/MHz
		38.4 MHz crystal, CPU running Prime from flash	—	28	—	µA/MHz
		38.4 MHz crystal, CPU running while loop from flash	—	26	—	µA/MHz
		38.4 MHz crystal, CPU running CoreMark loop from flash	—	38	—	µA/MHz
		38 MHz HFRCO, CPU running while loop from flash	—	22	—	µA/MHz
		76.8 MHz HFRCO w/ DPLL referenced to 38.4 MHz crystal, CPU running Prime from flash, VSCALE2	—	28	—	µA/MHz
Current consumption in EM1 mode with all peripherals disabled	I_{EM1}	76.8 MHz HFRCO w/ DPLL referenced to 38.4 MHz crystal, VSCALE2	—	17	—	µA/MHz
		38.4 MHz crystal	—	17	—	µA/MHz
		38 MHz HFRCO	—	13	—	µA/MHz
Current consumption in EM2 mode, VSCALE0	I_{EM2_VS}	Full RAM retention and RTC running from LFXO	—	1.40	—	µA
		Full RAM retention and RTC running from LFRCO	—	1.40	—	µA
		Full RAM retention and RTC running from LFRCO in precision mode	—	1.75	—	µA
		24 kB RAM retention and RTC running from LFXO	—	1.32	—	µA
		24 kB RAM retention and RTC running from LFRCO in precision mode	—	1.66	—	µA
		8 kB RAM retention and RTC running from LFXO	—	1.21	—	µA
		8 kB RAM retention and RTC running from LFRCO	—	1.20	—	µA

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Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM3 mode, VSCALE0	I_{EM3_VS}	8 kB RAM retention and RTC running from ULFRCO	—	1.05	—	µA
Current consumption in EM4 mode	I_{EM4}	No BURTC, No LF Oscillator, DCDC bypassed	—	0.17	—	µA
Additional current in EM2 or EM3 when any peripheral in PD0B is enabled[1]	I_{PD0B_VS}		—	0.37	—	µA

Note: 1. Extra current consumed by power domain. Does not include current associated with the enabled peripherals. See for a list of the peripherals in each power domain.

4.4 Radio Current Consumption with 3 V Supply

RF current consumption measured with MCU in EM1, HCLK = 38.4 MHz, and all MCU peripherals disabled. Unless otherwise indicated, typical conditions are: VDD = 3.0 V. T_A = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation at T_A = 25 °C.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
System current consumption in receive mode, active packet reception	I_{RX_ACTIVE}	125 kbit/s, 2GFSK, f = 2.4 GHz, Bluetooth stack running	—	4.5	—	mA
		500 kbit/s, 2GFSK, f = 2.4 GHz, Bluetooth stack running	—	4.5	—	mA
		1 Mbit/s, 2GFSK, f = 2.4 GHz, Bluetooth stack running	—	4.3	—	mA
		2 Mbit/s, 2GFSK, f = 2.4 GHz, Bluetooth stack running	—	4.8	—	mA
System current consumption in receive mode, listening for packet	I_{RX_LISTEN}	125 kbit/s, 2GFSK, f = 2.4 GHz, Bluetooth stack running	—	4.4	—	mA
		500 kbit/s, 2GFSK, f = 2.4 GHz, Bluetooth stack running	—	4.4	—	mA
		1 Mbit/s, 2GFSK, f = 2.4 GHz, Bluetooth stack running	—	4.2	—	mA
		2 Mbit/s, 2GFSK, f = 2.4 GHz, Bluetooth stack running	—	4.7	—	mA
System current consumption in transmit mode	I_{TX}	f = 2.4 GHz, CW, 0 dBm output power	—	4.8	—	mA
		f = 2.4 GHz, CW, 6 dBm output power	—	8.8	—	mA
		f = 2.4 GHz, CW, 8 dBm output power	—	10.6	—	mA

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4.5 RF Transmitter General Characteristics for the 2.4 GHz Band

Unless otherwise indicated, typical conditions are: T_A = 25 °C, VDD = 3.0V. RF center frequency 2.45 GHz.

Parameter	Symbol	Test Condition (Output Power)	Min	Typ	Max	Unit
RF tuning frequency range	F_{RANGE}		2400	—	2483.5	MHz
Maximum TX power	$POUT_{MAX}$	8 dBm	—	8.2	—	dBm
Minimum active TX Power	$POUT_{MIN}$	8 dBm	—	-27	—	dBm
Output power variation vs VDD supply voltage variation, frequency = 2450 MHz	$POUT_{VAR_V}$	8 dBm with VDD voltage swept from 1.8 V to 3.0 V	—	0.04	—	dB
Output power variation vs temperature, Frequency = 2450 MHz	$POUT_{VAR_T}$	8 dBm, (-40 to +105 °C)	—	0.9	—	dB
Output power variation vs RF frequency	$POUT_{VAR_F}$	8 dBm	—	0.2	—	dB

4.6 RF Receiver General Characteristics for the 2.4 GHz Band

Unless otherwise indicated, typical conditions are: T_A = 25 °C, VDD = 3.0V. RF center frequency 2.45 GHz.

Tale 5: RF Receiver General Characteristics for the 2.4 GHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF tuning frequency range	F_{RANGE}		2400	—	2483.5	MHz

4.7 RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 1 Mbps Data Rate

Unless otherwise indicated, typical conditions are: T_A = 25 °C, VDD = 3.0V. RF center frequency 2.45 GHz.

Table 6: RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 1 Mbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Max usable receiver input level	SAT	Signal is reference signal[1]	—	10	—	dBm
Sensitivity	SENS	Signal is reference signal, 37 byte payload[2]	—	-98.9	—	dBm
		Signal is reference signal, 255 byte payload[1]	—	-97.4	—	dBm
		With non-ideal signals[3 1]	—	-96.9	—	dBm
Signal to co-channel interferer	C/I_{CC}	(see notes)[1 4]	—	8.7	—	dB
N ± 1 Adjacent channel selectivity	C/I_1	Interferer is reference signal at +1 MHz offset[1 5 4 6]	—	-6.6	—	dB
		Interferer is reference signal at -1 MHz offset[1 5 4 6]	—	-6.5	—	dB
N ± 2 Alternate channel selectivity	C/I_2	Interferer is reference signal at +2 MHz offset[1 5 4 6]	—	-40.9	—	dB
		Interferer is reference signal at -2 MHz offset[1 5 4 6]	—	-39.9	—	dB
N ± 3 Alternate channel selectivity	C/I_3	Interferer is reference signal at +3 MHz offset[1 5 4 6]	—	-45.9	—	dB
		Interferer is reference signal at -3 MHz offset[1 5 4 6]	—	-46.2	—	dB
Selectivity to image frequency	C/I_{IM}	Interferer is reference signal at image frequency with 1 MHz precision[1 6]	—	-23.5	—	dB
Selectivity to image frequency ± 1 MHz	C/I_{IM_1}	Interferer is reference signal at image frequency +1 MHz with 1 MHz precision[1 6]	—	-40.9	—	dB

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Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
		Interferer is reference signal at image frequency -1 MHz with 1 MHz precision[1 6]	—	-6.6	—	dB
Intermodulation performance	IM	n = 3 (see note[7])	—	-17.1	—	dBm

Note:

1. 0.017% Bit Error Rate.
2. 0.1% Bit Error Rate.
3. With non-ideal signals as specified in Bluetooth Test Specification RF-PHY.TS.5.0.1 section 4.7.1
4. Desired signal -67 dBm.
5. Desired frequency 2402 MHz ≤ Fc ≤ 2480 MHz.
6. With allowed exceptions.
7. As specified in Bluetooth Core specification version 5.1, Vol 6, Part A, Section 4.4

4.8 RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 2 Mbps Data Rate

Unless otherwise indicated, typical conditions are: T_A = 25 °C, VDD = 3.0V. RF center frequency 2.45 GHz.

Table 7: RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 2 Mbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Max usable receiver input level	SAT	Signal is reference signal[1]	—	10	—	dBm
Sensitivity	SENS	Signal is reference signal, 37 byte payload[2]	—	-96.2	—	dBm
		Signal is reference signal, 255 byte payload[1]	—	-94.6	—	dBm
		With non-ideal signals[3 1]	—	-94.4	—	dBm
Signal to co-channel interferer	C/I_{CC}	(see notes)[1 4]	—	8.8	—	dB
N ± 1 Adjacent channel selectivity	C/I_1	Interferer is reference signal at +2 MHz offset[1 5 4 6]	—	-9.2	—	dB
		Interferer is reference signal at -2 MHz offset[1 5 4 6]	—	-6.6	—	dB
N ± 2 Alternate channel selectivity	C/I_2	Interferer is reference signal at +4 MHz offset[1 5 4 6]	—	-43.3	—	dB
		Interferer is reference signal at -4 MHz offset[1 5 4 6]	—	-44.0	—	dB
N ± 3 Alternate channel selectivity	C/I_3	Interferer is reference signal at +6 MHz offset[1 5 4 6]	—	-48.6	—	dB
		Interferer is reference signal at -6 MHz offset[1 5 4 6]	—	-50.7	—	dB
Selectivity to image frequency	C/I_{IM}	Interferer is reference signal at image frequency with 1 MHz precision[1 6]	—	-23.8	—	dB
Selectivity to image frequency ± 2 MHz	C/I_{IM_1}	Interferer is reference signal at image frequency +2 MHz with 1 MHz precision[1 6]	—	-43.3	—	dB
		Interferer is reference signal at image frequency -2 MHz with 1 MHz precision[1 6]	—	-9.2	—	dB
Intermodulation performance	IM	n = 3 (see note[7])	—	-18.8	—	dBm

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Parameter	Symbol	Test Condition	Min	Typ	Max	Unit

Note:

1. 0.017% Bit Error Rate.
2. 0.1% Bit Error Rate.
3. With non-ideal signals as specified in Bluetooth Test Specification RF-PHY.TS.5.0.1 section 4.7.1
4. Desired signal -64 dBm.
5. Desired frequency 2402 MHz ≤ Fc ≤ 2480 MHz.
6. With allowed exceptions.
7. As specified in Bluetooth Core specification version 5.1, Vol 6, Part A, Section 4.4

4.9 RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 500 kbps Data Rate

Unless otherwise indicated, typical conditions are: T_A = 25 °C, VDD = 3.0V. RF center frequency 2.45 GHz.

Table 8: RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 500 kbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Max usable receiver input level	SAT	Signal is reference signal[1]	—	10	—	dBm
Sensitivity	SENS	Signal is reference signal, 37 byte payload[2]	—	-102.5	—	dBm
		Signal is reference signal, 255 byte payload[1]	—	-101.2	—	dBm
		With non-ideal signals[3 1]	—	-100.2	—	dBm
Signal to co-channel interferer	C/I_{CC}	(see notes)[1 4]	—	2.7	—	dB
N ± 1 Adjacent channel selectivity	C/I_1	Interferer is reference signal at +1 MHz offset[1 5 4 6]	—	-8.0	—	dB
		Interferer is reference signal at -1 MHz offset[1 5 4 6]	—	-7.9	—	dB
N ± 2 Alternate channel selectivity	C/I_2	Interferer is reference signal at +2 MHz offset[1 5 4 6]	—	-46.5	—	dB
		Interferer is reference signal at -2 MHz offset[1 5 4 6]	—	-49.9	—	dB
N ± 3 Alternate channel selectivity	C/I_3	Interferer is reference signal at +3 MHz offset[1 5 4 6]	—	-48.9	—	dB
		Interferer is reference signal at -3 MHz offset[1 5 4 6]	—	-53.8	—	dB
Selectivity to image frequency	C/I_{IM}	Interferer is reference signal at image frequency with 1 MHz precision[1 6]	—	-48.3	—	dB
Selectivity to image frequency ± 1 MHz	C/I_{IM_1}	Interferer is reference signal at image frequency +1 MHz with 1 MHz precision[1 6]	—	-49.9	—	dB
		Interferer is reference signal at image frequency -1 MHz with 1 MHz precision[1 6]	—	-46.5	—	dB

Note:

1. 0.017% Bit Error Rate.
2. 0.1% Bit Error Rate.
3. With non-ideal signals as specified in Bluetooth Test Specification RF-PHY.TS.5.0.1 section 4.7.1
4. Desired signal -72 dBm.
5. Desired frequency 2402 MHz ≤ Fc ≤ 2480 MHz.
6. With allowed exceptions.

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4.10 RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 125 kbps Data Rate

Unless otherwise indicated, typical conditions are: T_A = 25 °C, VDD = 3.0V. RF center frequency 2.45 GHz.

Table 9: RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 125 kbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Max usable receiver input level	SAT	Signal is reference signal[1]	—	10	—	dBm
Sensitivity	SENS	Signal is reference signal, 37 byte payload[2]	—	-106.7	—	dBm
		Signal is reference signal, 255 byte payload[1]	—	-106.4	—	dBm
		With non-ideal signals[3 1]	—	-105.8	—	dBm
Signal to co-channel interferer	C/I_{CC}	(see notes)[1 4]	—	0.9	—	dB
N ± 1 Adjacent channel selectivity	C/I_1	Interferer is reference signal at +1 MHz offset[1 5 4 6]	—	-13.6	—	dB
		Interferer is reference signal at -1 MHz offset[1 5 4 6]	—	-13.4	—	dB
N ± 2 Alternate channel selectivity	C/I_2	Interferer is reference signal at +2 MHz offset[1 5 4 6]	—	-52.6	—	dB
		Interferer is reference signal at -2 MHz offset[1 5 4 6]	—	-55.8	—	dB
N ± 3 Alternate channel selectivity	C/I_3	Interferer is reference signal at +3 MHz offset[1 5 4 6]	—	-53.7	—	dB
		Interferer is reference signal at -3 MHz offset[1 5 4 6]	—	-59.0	—	dB
Selectivity to image frequency	C/I_{IM}	Interferer is reference signal at image frequency with 1 MHz precision[1 6]	—	-52.7	—	dB
Selectivity to image frequency ± 1 MHz	C/I_{IM_1}	Interferer is reference signal at image frequency +1 MHz with 1 MHz precision[1 6]	—	-53.7	—	dB
		Interferer is reference signal at image frequency -1 MHz with 1 MHz precision[1 6]	—	-52.6	—	dB

Note:

1. 0.017% Bit Error Rate.
2. 0.1% Bit Error Rate.
3. With non-ideal signals as specified in Bluetooth Test Specification RF-PHY.TS.5.0.1 section 4.7.1
4. Desired signal -79 dBm.
5. Desired frequency 2402 MHz ≤ Fc ≤ 2480 MHz.
6. With allowed exceptions.

4.11 High-Frequency Crystal

Table 10: High-Frequency Crystal

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal frequency	f_{HFXTAL}		—	38.4	—	MHz
Initial calibrated accuracy	ACC_{HFXTAL}		-10	±5	10	ppm
Temperature drift	$DRIFT_{HFXTAL}$	Across specified temperature range	-20	—	20	ppm

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4.12 Low-Frequency Crystal

Table 11: Low-Frequency Crystal

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal frequency[1]	f_{LFXTAL}		—	32.768	—	kHz
Temperature drift	$DRIFT_{LFXTAL}$	-40 °C to +85 °C	-100	—	100	ppm
		-40 °C to +105 °C	-150	—	150	ppm

Note:
1. Nominal frequency tolerance of the crystal is ± 20 ppm.

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4.13 Precision Low Frequency RC Oscillator (LFRCO)

Table 12: Precision Low Frequency RC Oscillator (LFRCO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Nominal oscillation frequency	F_{LFRCO}		—	32.768	—	kHz
Frequency accuracy	F_{LFRCO_ACC}	Normal mode	-3	—	3	%
		Precision mode[1], across operating temperature range[2]	-500	—	500	ppm
Startup time	$t_{STARTUP}$	Normal mode	—	204	—	µs
		Precision mode[1]	—	11.7	—	ms
Current consumption	I_{LFRCO}	Normal mode	—	175	—	nA
		Precision mode[1], T = stable at 25 °C [3]	—	655	—	nA

Note:

1. The LFRCO operates in high-precision mode when CFG_HIGHPRECEN is set to 1. High-precision mode is not available in EM4.
2. Includes ± 40 ppm frequency tolerance of the HFXO crystal.
3. Includes periodic re-calibration against HFXO crystal oscillator.

4.14 GPIO Pins

Unless otherwise indicated, typical conditions are: VDD = 3.0 V.

Table 13: GPIO Pins

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Leakage current	I_{LEAK_IO}	MODEx = DISABLED, VDD = 3.0 V	—	2.5	—	nA
Input low voltage[1]	V_{IL}	Any GPIO pin	—	—	0.3 * VDD	V
		RESETn	—	—	0.3 * DVDD	V
Input high voltage[1]	V_{IH}	Any GPIO pin	0.7 * VDD	—	—	V
		RESETn	0.7 * DVDD	—	—	V
Hysteresis of input voltage	V_{HYS}	Any GPIO pin	0.05*VDD	—	—	V
		RESETn	0.05*DVDD	—	—	V
Output low voltage	V_{OL}	Sinking 20mA, VDD = 3.0 V	—	—	0.2 * VDD	V
		Sinking 8mA, VDD = 1.62 V	—	—	0.4 * VDD	V
Output high voltage	V_{OH}	Sourcing 20mA, VDD = 3.0 V	0.8 * VDD	—	—	V
		Sourcing 8mA, VDD = 1.62 V	0.6 * VDD	—	—	V
GPIO rise time	T_{GPIO_RISE}	VDD = 3.0V, C_{load} = 50pF, SLEWRATE = 4, 10% to 90%	—	8.4	—	ns

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Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
		VDD = 1.7V, C_{load} = 50pF, SLEWRATE = 4, 10% to 90%	–	13	–	ns
GPIO fall time	T_{GPIO_FALL}	VDD = 3.0V, C_{load} = 50pF, SLEWRATE = 4, 90% to 10%	—	7.1	—	ns
		VDD = 1.7V, C_{load} = 50pF, SLEWRATE = 4, 90% to 10%	—	11.9	—	ns
Pull up/down resistance	R_{PULL}	GPIO pull-up to VDD: MODEn = DISABLE, DOUT=1. GPIO pull-down to VSS: MODEn = WIREDORPULLDOWN, DOUT = 0. RESETn pin pull-up to DVDD.	35	44	55	kΩ
Maximum filtered glitch width	T_{GF}	MODE = INPUT, DOUT = 1	—	27	—	ns

Note:

1. GPIO input thresholds are proportional to the VDD pin. RESETn input thresholds are proportional to the internal DVDD supply, which is generated by the DC-DC converter. DVDD is equal to 1.8 V when DC-DC is active and bypassed to VDD when DC-DC is inactive.

4.15 Microcontroller Peripherals

The MCU peripherals set available in Lyra P modules includes:

- ADC: 12-bit at 1 Msps, 16-bit at 76.9 ksps
- 16-bit and 32-bit Timers/Counters
- 24-bit Low Energy Timer for waveform generation
- 32-bit Real Time Counter
- USART (UART/SPI/SmartCards/IrDA/I2S)
- EUART (UART/IrDA)
- I^2C peripheral interfaces
- PDM interface
- 12 Channel Peripheral Reflex System

For details on their electrical performance, consult the relevant portions of Section 4 in the SoC datasheet.

To learn which GPIO ports provide access to every peripheral, consult Analog Peripheral Connectivity and Digital Peripheral Connectivity.

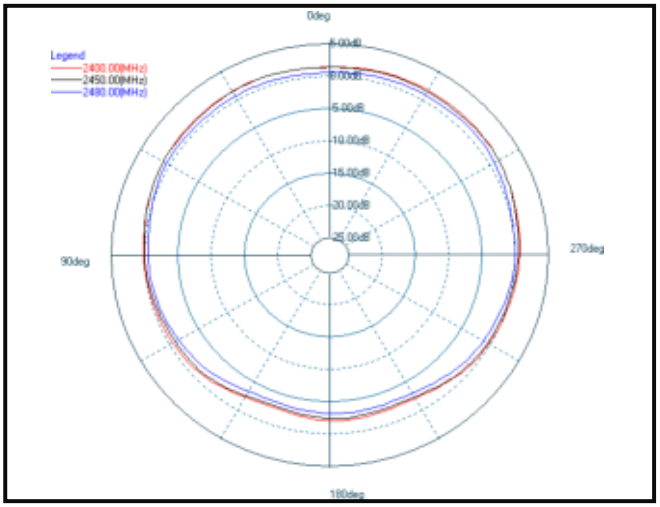
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4.16 Typical Performance Curves

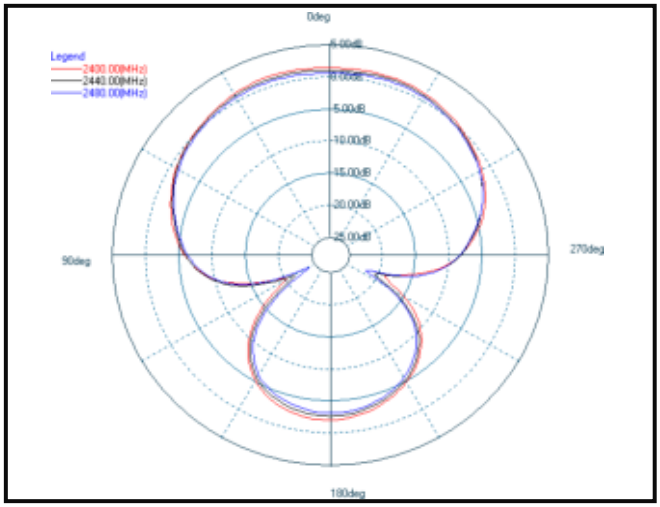
Typical performance curves indicate typical characterized performance under the stated conditions.

4.16.1 Antenna Radiation and Efficiency

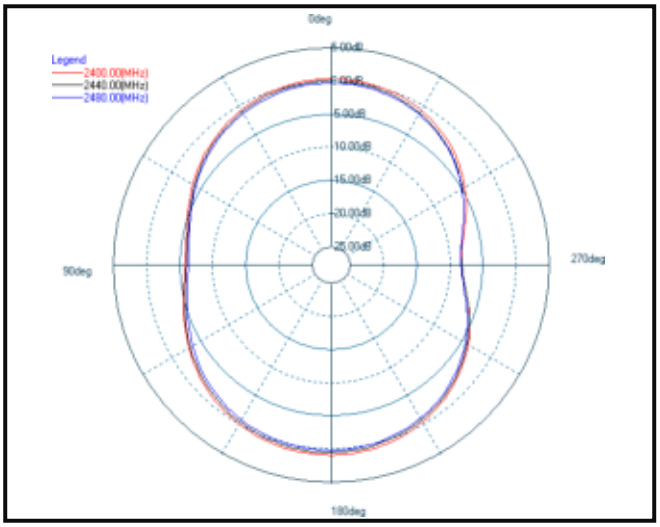
Typical Lyra P radiation patterns and efficiency for the on-board chip antenna under optimal operating conditions are plotted in the figures that follow. Antenna gain and radiation patterns have a strong dependence on the size and shape of the application PCB the module is mounted on, as well as on the proximity of any mechanical design to the antenna.



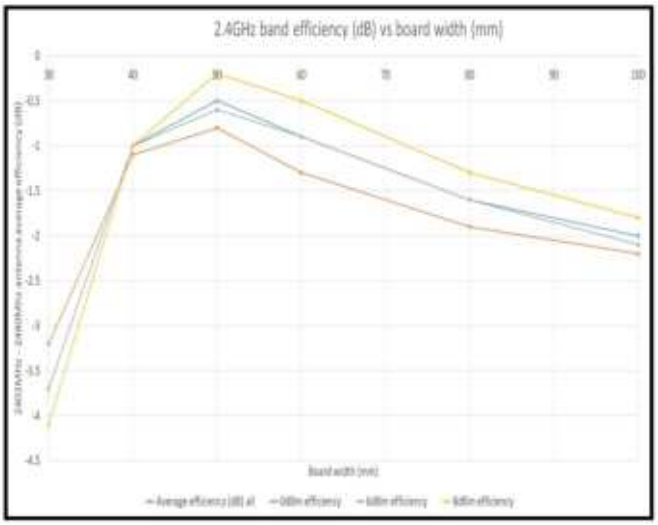
Phi 0°



Phi 90°



Theta 90°



Radiation Efficiency vs Application Board GND Plane Width

Figure 5: Typical 2D Antenna Radiation Patterns and Efficiency

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5 Reference Diagrams

5.1 Network Co-Processor (NCP) Application with UART Host

The Lyra P can be controlled over the UART interface as a peripheral to an external host processor. Typical power supply, programming/debug interface, and host interface connections are shown in the figure below.

Note: For boot pin, see section 5.3 Boot.

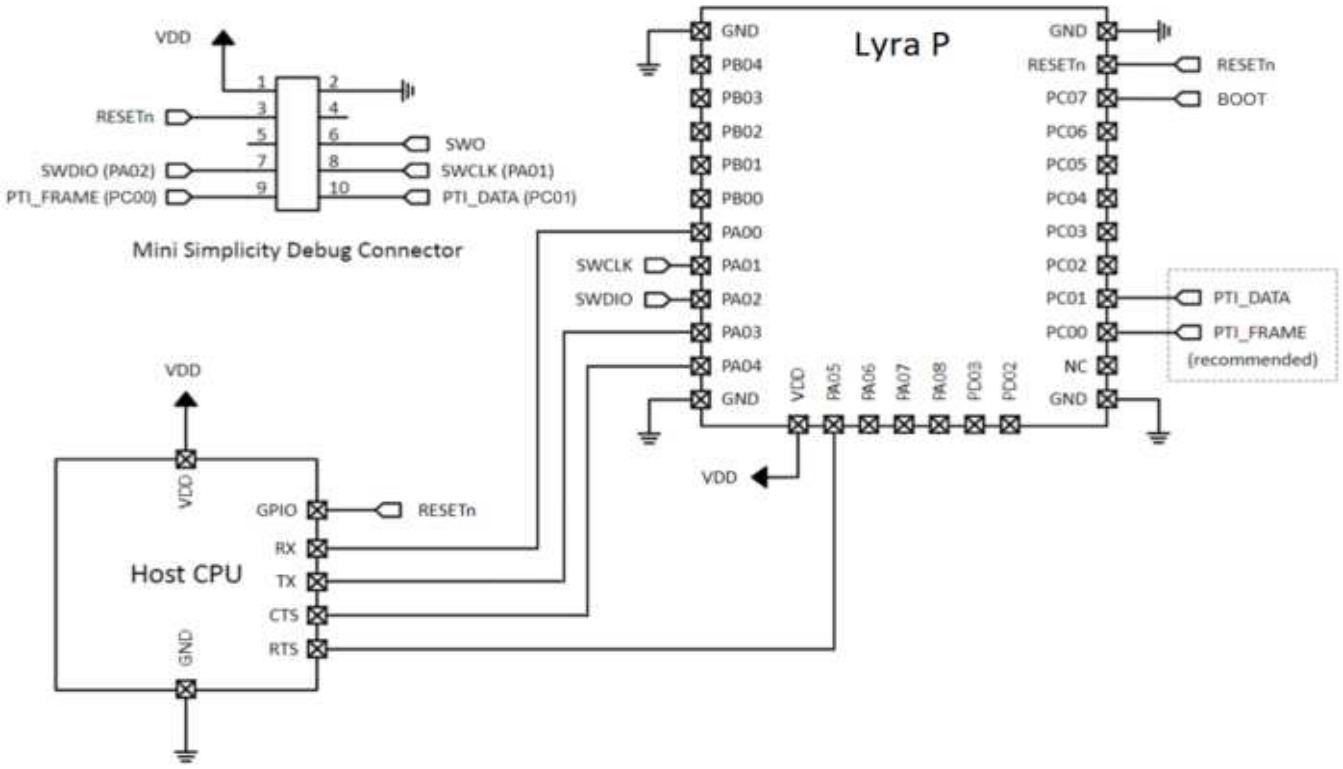


Figure 6: UART NCP Configuration

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5.2 SoC Application

The Lyra P can be used in a stand-alone SoC configuration without an external host processor. Typical power supply and programming/debug interface connections are shown in the figure below.

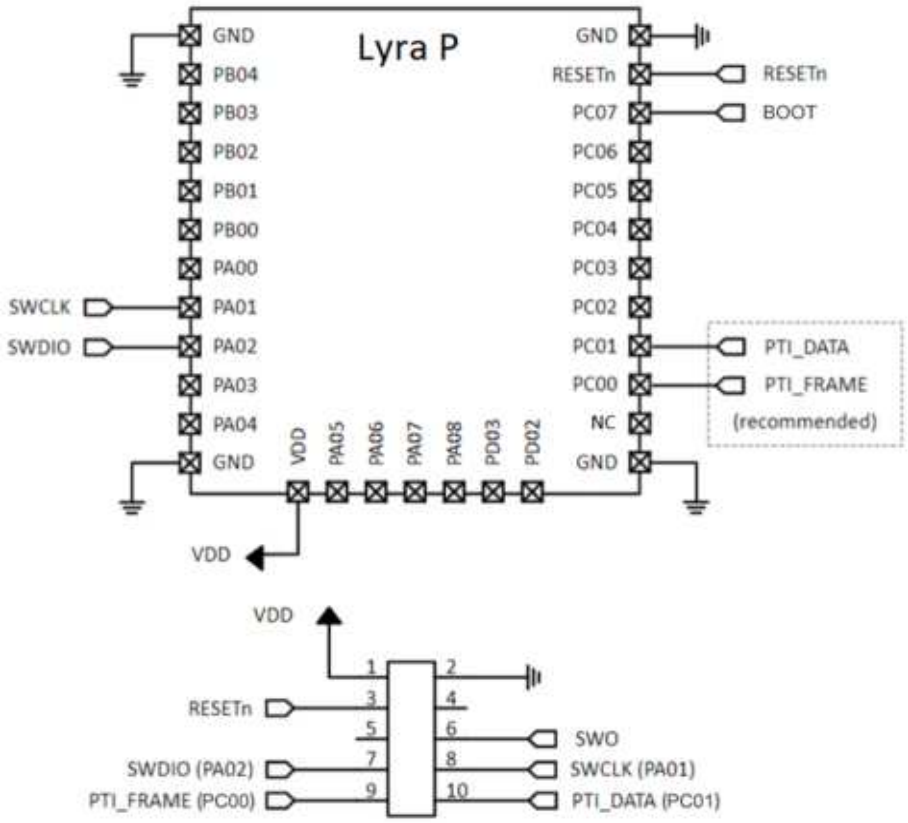


Figure 7: Stand-Alone SoC Configuration

5.3 Boot

The BOOT pin is used to determine when execution of the bootloader is required. Upon reset, execution of the bootloader begins. The state of the BOOT pin is read immediately upon start-up of the bootloader. If LOW, execution of the bootloader continues, facilitating firmware update via the UART. If the BOOT pin is HIGH, the bootloader will stop execution and pass control to the main application firmware.

Note: To maintain backwards compatibility with legacy BGX220P Wireless Xpress parts, the BOOT pin for 453-00147 is mapped to the legacy part BOOT pin location. Refer to the table below for details of the appropriate part BOOT pin location.

Table 14: Different BOOT Pin Locations for Lyra P

Part	BOOT Pin Location	
	Pin Number	Pin Description
453-00090	29	PC07
453-00147	19	PD02

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6 Pin Definitions

6.1 Lyra P 31-Pin PCB Module Pinout

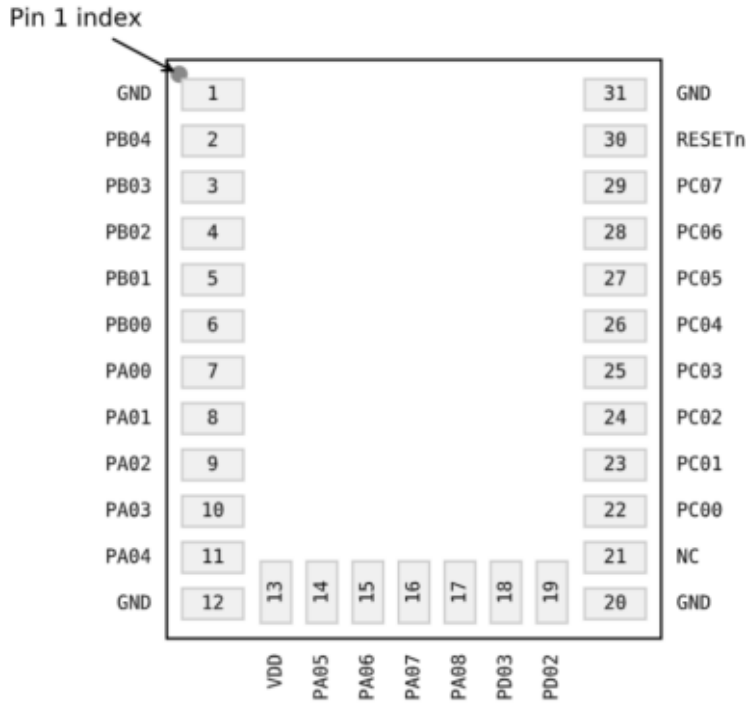


Figure 8: Lyra P 31-Pin PCB Module With LF Crystal Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see Table 15: GPIO alternate function table, Analog Peripheral Connectivity, and Digital Peripheral Connectivity.

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
GND	1	Ground	PB04	2	GPIO
PB03	3	GPIO	PB02	4	GPIO
PB01	5	GPIO	PB00	6	GPIO
PA00	7	GPIO	PA01	8	GPIO
PA02	9	GPIO	PA03	10	GPIO
PA04	11	GPIO	GND	12	Ground
VDD	13	Power supply	PA05	14	GPIO
PA06	15	GPIO	PA07	16	GPIO
PA08	17	GPIO	PD03	18	GPIO
PD02	19	GPIO	GND	20	Ground
NC	21	Do not connect	PC00	22	GPIO
PC01	23	GPIO	PC02	24	GPIO
PC03	25	GPIO	PC04	26	GPIO

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Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PC05	27	GPIO	PC06	28	GPIO
PC07	29	GPIO	RESETn	30	Reset Pin. The RESETn pin is pulled up to an internal DVDD supply. An external pull-up is not recommended. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. The RESETn pin can be left unconnected if no external reset switch or source is used.
GND	31	Ground			

6.2 Alternate Function Table

A wide selection of alternate functionality is available for multiplexing to various pins. The following table shows what functions are available on each device pin.

Table 15: GPIO alternate function table

GPIO	Alternate Function		
PB03	GPIO.EM4WU4		
PB01	GPIO.EM4WU3		
PB00	IADC0.VREFN		
PA00	IADC0.VREFP		
PA01	GPIO.SWCLK		
PA02	GPIO.SWDIO		
PA03	GPIO.SWV	GPIO.TDO	GPIO.TRACEDATA0
PA04	GPIO.TDI	GPIO.TRACECLK	
PA05	GPIO.EM4WU0		
PD02	GPIO.EM4WU9		
PC00	GPIO.EM4WU6	GPIO.THMSW_EN	
PC05	GPIO.EM4WU7		
PC07	GPIO.EM4WU8		

6.3 Analog Peripheral Connectivity

Many analog resources are routable and can be connected to numerous GPIO's. The table below indicates which peripherals are available on each GPIO port. When a differential connection is being used, positive inputs are restricted to the EVEN pins and Negative inputs are restricted to the ODD pins. When a single ended connection is being used positive input is available on all pins. See the SoC Reference Manual for more details on the ABUS and analog peripherals.

Table 16: ABUS Routing Table

Peripheral	Signal	PA		PB		PC		PD	
		EVEN	ODD	EVEN	ODD	EVEN	ODD	EVEN	ODD
IADC0	ana_neg	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	ana_pos	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

6.4 Digital Peripheral Connectivity

Many digital resources are routable and can be connected to numerous GPIO's. The table below indicates which peripherals are available on each GPIO port.

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Table 17: DBUS routing table

Peripheral.Resource	PORT			
	PA	PB	PC	PD
CMU.CLKIN0			Available	Available
CMU.CLKOUT0			Available	Available
CMU.CLKOUT1			Available	Available
CMU.CLKOUT2	Available	Available		
EUART0.CTS	Available	Available	Available	Available
EUART0.RTS	Available	Available	Available	Available
EUART0.RX	Available	Available	Available	Available
EUART0.TX	Available	Available	Available	Available
FRC.DCLK			Available	Available
FRC.DFRAME			Available	Available
FRC.DOUT			Available	Available
I2C0.SCL	Available	Available	Available	Available
I2C0.SDA	Available	Available	Available	Available
I2C1.SCL			Available	Available
I2C1.SDA			Available	Available
LETIMER0.OUT0	Available	Available		
LETIMER0.OUT1	Available	Available		
MODEM.ANT0	Available	Available	Available	Available
MODEM.ANT1	Available	Available	Available	Available
MODEM.ANT_ROLL_OVER			Available	Available
MODEM.ANT_RR0			Available	Available
MODEM.ANT_RR1			Available	Available
MODEM.ANT_RR2			Available	Available
MODEM.ANT_RR3			Available	Available
MODEM.ANT_RR4			Available	Available
MODEM.ANT_RR5			Available	Available
MODEM.ANT_SW_EN			Available	Available
MODEM.ANT_SW_US			Available	Available
MODEM.ANT_TRIG			Available	Available
MODEM.ANT_TRIG_STOP			Available	Available
MODEM.DCLK	Available	Available		
MODEM.DIN	Available	Available		
MODEM.DOUT	Available	Available		
PDM.CLK	Available	Available	Available	Available
PDM.DAT0	Available	Available	Available	Available
PDM.DAT1	Available	Available	Available	Available
PRS.ASYNCH0	Available	Available		
PRS.ASYNCH1	Available	Available		

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Peripheral.Resource	PORT			
	PA	PB	PC	PD
PRS.ASYNCH10			Available	Available
PRS.ASYNCH11			Available	Available
PRS.ASYNCH2	Available	Available		
PRS.ASYNCH3	Available	Available		
PRS.ASYNCH4	Available	Available		
PRS.ASYNCH5	Available	Available		
PRS.ASYNCH6			Available	Available
PRS.ASYNCH7			Available	Available
PRS.ASYNCH8			Available	Available
PRS.ASYNCH9			Available	Available
PRS.SYNCH0	Available	Available	Available	Available
PRS.SYNCH1	Available	Available	Available	Available
PRS.SYNCH2	Available	Available	Available	Available
PRS.SYNCH3	Available	Available	Available	Available
TIMER0.CC0	Available	Available	Available	Available
TIMER0.CC1	Available	Available	Available	Available
TIMER0.CC2	Available	Available	Available	Available
TIMER0.CDTI0	Available	Available	Available	Available
TIMER0.CDTI1	Available	Available	Available	Available
TIMER0.CDTI2	Available	Available	Available	Available
TIMER1.CC0	Available	Available	Available	Available
TIMER1.CC1	Available	Available	Available	Available
TIMER1.CC2	Available	Available	Available	Available
TIMER1.CDTI0	Available	Available	Available	Available
TIMER1.CDTI1	Available	Available	Available	Available
TIMER1.CDTI2	Available	Available	Available	Available
TIMER2.CC0	Available	Available		
TIMER2.CC1	Available	Available		
TIMER2.CC2	Available	Available		
TIMER2.CDTI0	Available	Available		
TIMER2.CDTI1	Available	Available		
TIMER2.CDTI2	Available	Available		
TIMER3.CC0			Available	Available
TIMER3.CC1			Available	Available
TIMER3.CC2			Available	Available
TIMER3.CDTI0			Available	Available
TIMER3.CDTI1			Available	Available
TIMER3.CDTI2			Available	Available

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Peripheral.Resource	PORT			
	PA	PB	PC	PD
TIMER4.CC0	Available	Available		
TIMER4.CC1	Available	Available		
TIMER4.CC2	Available	Available		
TIMER4.CDTI0	Available	Available		
TIMER4.CDTI1	Available	Available		
TIMER4.CDTI2	Available	Available		
USART0.CLK	Available	Available	Available	Available
USART0.CS	Available	Available	Available	Available
USART0.CTS	Available	Available	Available	Available
USART0.RTS	Available	Available	Available	Available
USART0.RX	Available	Available	Available	Available
USART0.TX	Available	Available	Available	Available
USART1.CLK	Available	Available		
USART1.CS	Available	Available		
USART1.CTS	Available	Available		
USART1.RTS	Available	Available		
USART1.RX	Available	Available		
USART1.TX	Available	Available		

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7 Design Guidelines

7.1 Layout and Placement

For optimal performance of the Lyra P:

- Place the module aligned to the edge of the application PCB, as illustrated in the figures below.
- Leave the antenna clearance area void of any traces, components, or copper on all layers of the application PCB.
- Connect all ground pads directly to a solid ground plane.
- Place the ground vias as close to the ground pads as possible.
- Avoid plastic or any other dielectric material in contact with the antenna.

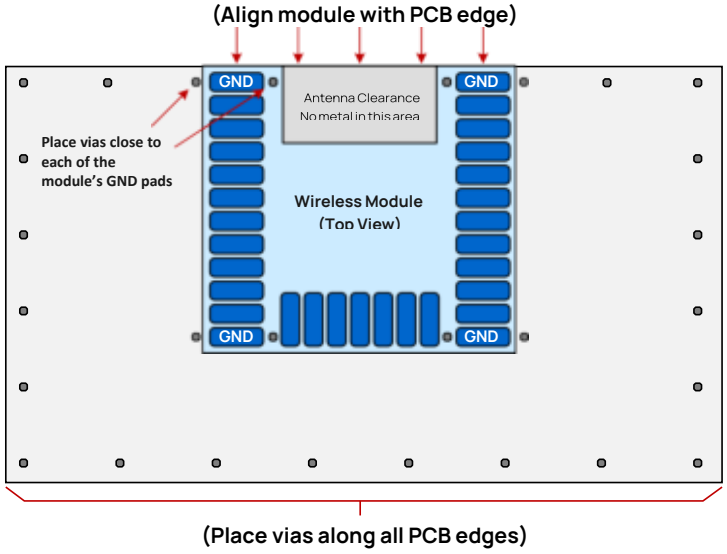


Figure 9: Recommended Layout for Lyra P

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The figure below illustrates layout scenarios that will lead to severely degraded RF performance for the module.



Figure 10: Non-optimal layout examples

The width of the GND plane to the sides the module will impact the efficiency of the on-board chip antenna. To achieve optimal performance, a GND plane width of 50 mm is recommended. See Antenna Radiation and Efficiency for reference.

7.2 Proximity to Other Materials

Avoid plastic or any other dielectric material in contact with the antenna. Conformal coating and other thin dielectric layers are acceptable directly on top of the antenna region, but this will also negatively impact antenna efficiency and reduce range.

Any metallic objects in close proximity to the antenna will prevent the antenna from radiating freely. The minimum recommended distance of metallic and/or conductive objects is 10 mm in any direction from the antenna except in the directions of the application PCB ground planes.

7.3 Proximity to Human Body

Placing the module in contact with or very close to the human body will negatively impact antenna efficiency and reduce range.

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8 Mechanical Specifications

8.1 Dimensions

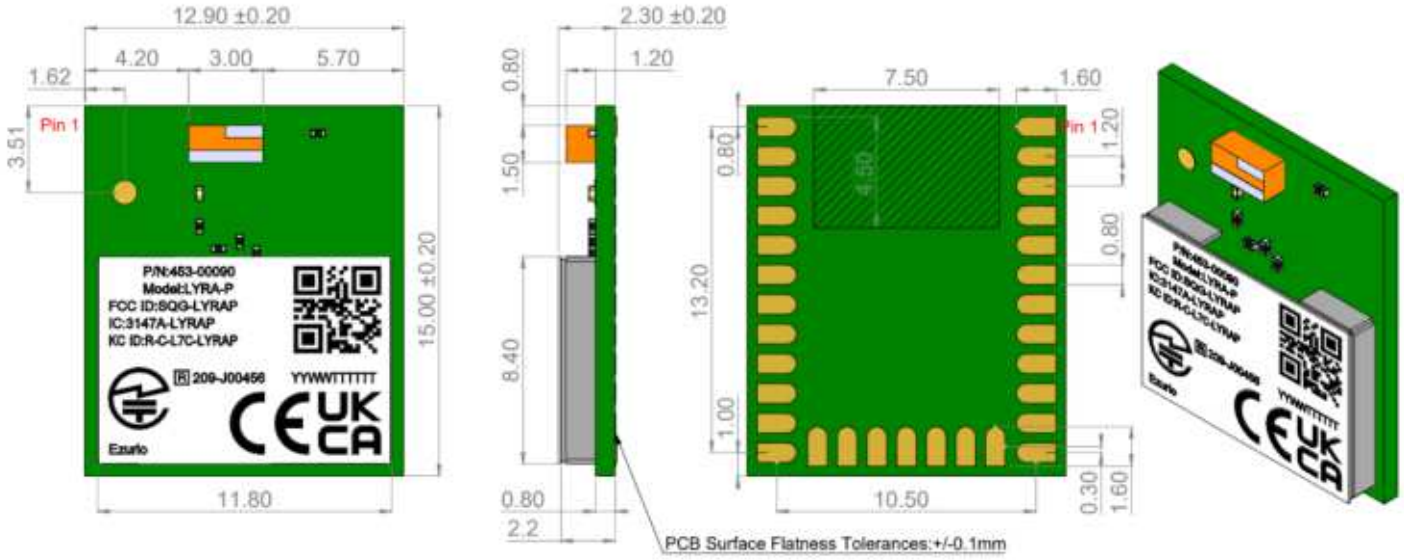


Figure 11: Module dimensions (mm)

8.2 PCB Land Pattern

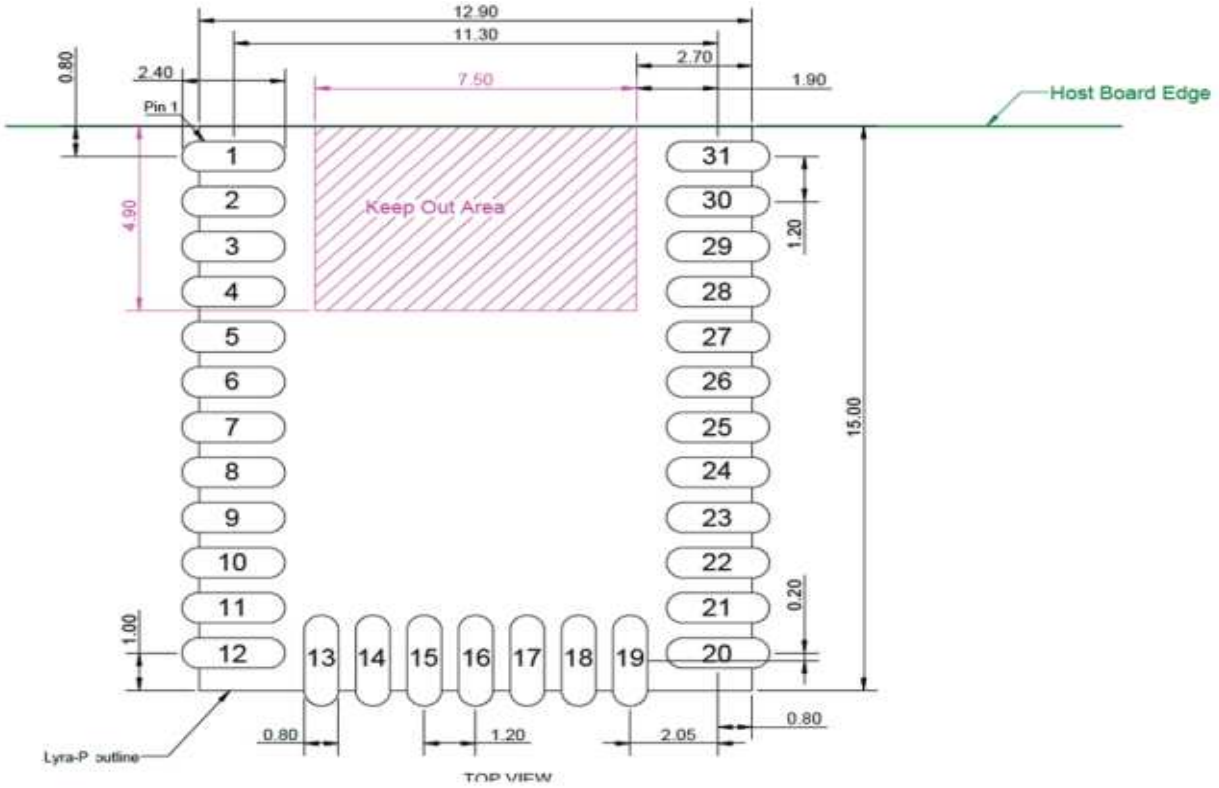


Figure 12: PCB land pattern

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Note: Distance between vertical center of pin 19 and vertical center of pin 20 is 0.2 mm.

8.3 Lyra P Label Marking

The figure below shows the module markings engraved on the RF shield.



Figure 13: Lyra P Top Marking – note part # 453-00147 is identical, except for the PN: is updated

Mark Description

The package marking consists of:

- P/N - Part number designation
- Model: Lyra Model number designation
- QR Code: YYWWMMABCDE
  - YY – Last two digits of the assembly year.
  - WW – Two-digit workweek when the device was assembled.
  - MMABCDE – Silicon Labs unit code
- YYWWTTTTTT
  - YY – Last two digits of the assembly year.
  - WW – Two-digit workweek when the device was assembled.
  - TTTTTT – Manufacturing trace code. The first letter is the device revision.
- Certification marks such as the CE logo, FCC and IC IDs, etc as per above image

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9 Soldering Recommendations

9.1 Reflow for lead Free Solder Paste

- Optimal solder reflow profile depends on solder paste properties and should be optimized as part of an overall process development.
- It is important to provide a solder reflow profile that matches the solder paste supplier's recommendations.
- Temperature ranges beyond that of the solder paste supplier's recommendation could result in poor solderability.
- All solder paste suppliers recommend an ideal reflow profile to give the best solderability.

9.2 Recommended Reflow Profile for lead Free Solder Paste

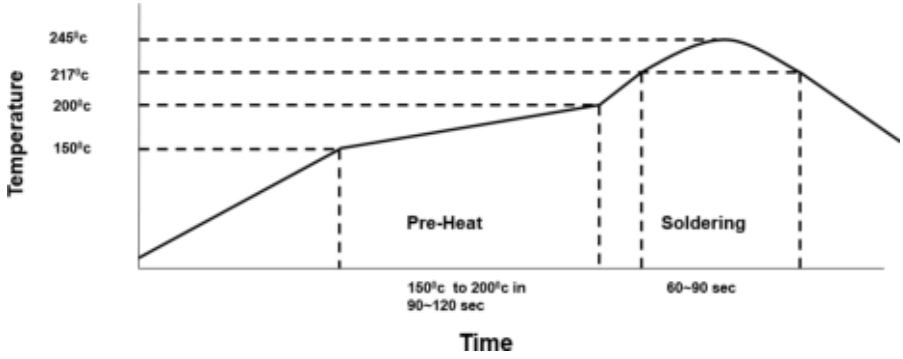


Figure 14: Recommended Reflow Profile

10 Miscellaneous

10.1 Cleaning

In general, cleaning the populated modules is strongly discouraged. Residuals under the module cannot be easily removed with any cleaning process.

- Cleaning with water can lead to capillary effects where water is absorbed into the gap between the host board and the module. The combination of soldering flux residuals and encapsulated water could lead to short circuits between neighboring pads. Water could also damage any stickers or labels.
- Cleaning with alcohol or a similar organic solvent will likely flood soldering flux residuals into the RF shield, which is not accessible for post-washing inspection. The solvent could also damage any stickers or labels.
- Ultrasonic cleaning could damage the module permanently

10.2 Rework

The Lyra P module can be unsoldered from the host board if the Moisture Sensitivity Level (MSL) requirements are met as described in this datasheet.

Never attempt a rework on the module itself, e.g. replacing individual components. Such actions terminate warranty coverage.

10.3 Handling and Storage

10.3.1 Handling

The Lyra P module contain a highly sensitive electronic circuitry. Handling without proper ESD protection may damage the module permanently

10.3.2 Moisture Sensitivity Level (MSL)

Per J-STD-020, devices rated as MSL 3 and not stored in a sealed bag with desiccant pack should be baked prior to use.

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Devices are packaged in a Moisture Barrier Bag with a desiccant pack and Humidity Indicator Card (HIC). Devices that will be subjected to reflow should reference the HIC and J-STD-033 to determine if baking is required.

If baking is required, refer to J-STD-033 for bake procedure.

10.3.3 Storage

Per J-STD-033, the shelf life of devices in a Moisture Barrier Bag is 12 months at <40C and <90% room humidity (RH).

Do not store in salty air or in an environment with a high concentration of corrosive gas, such as Cl2, H2S, NH3, SO2, or NOX. Do not store in direct sunlight.

The product should not be subject to excessive mechanical shock.

10.3.4 Repeated Reflow Soldering

Only a single reflow soldering process is encouraged for host boards.

11 Tape and Reel

Lyra P modules are delivered to the customer in cut tape (250 pcs) or reel (1000 pcs) packaging with the dimensions below. All dimensions are given in mm unless otherwise indicated.

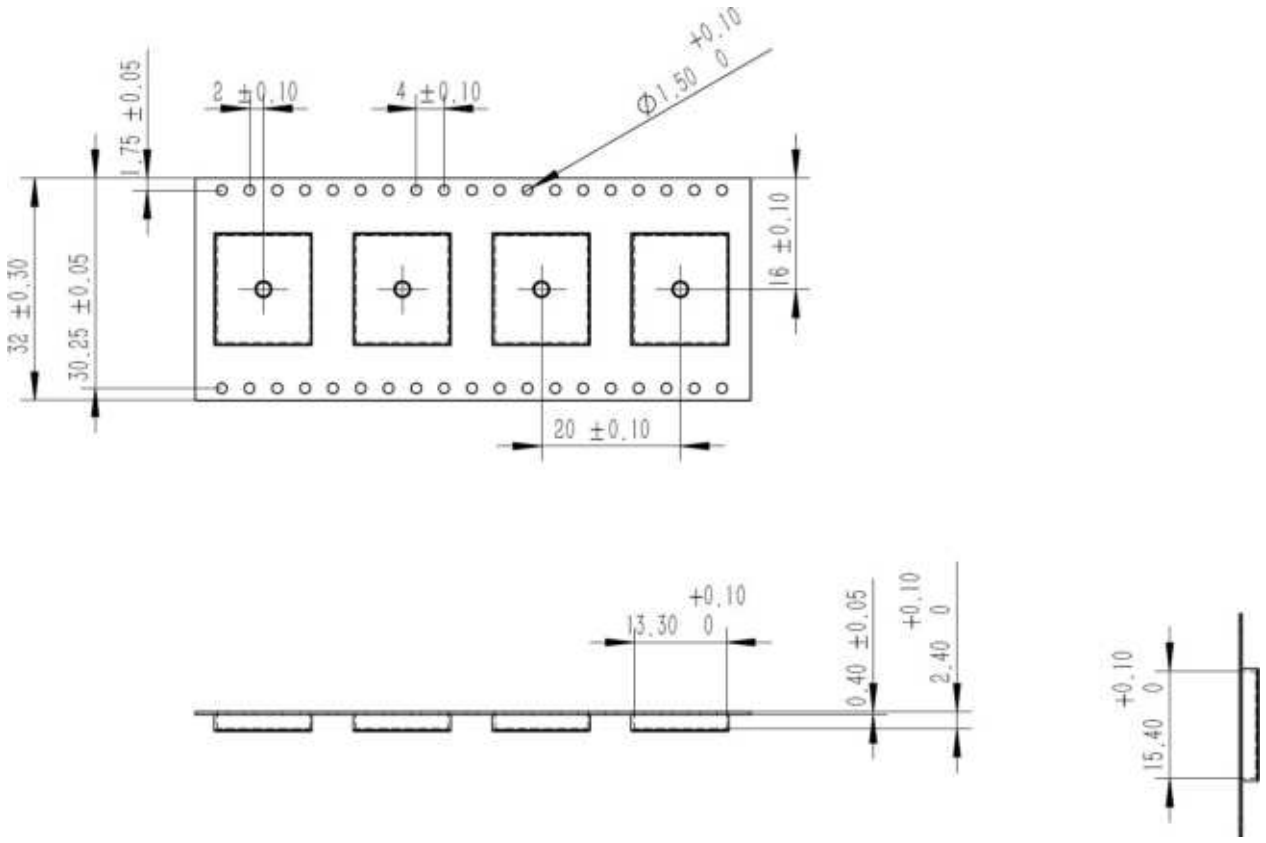


Figure 15: Carrier Tape Dimensions

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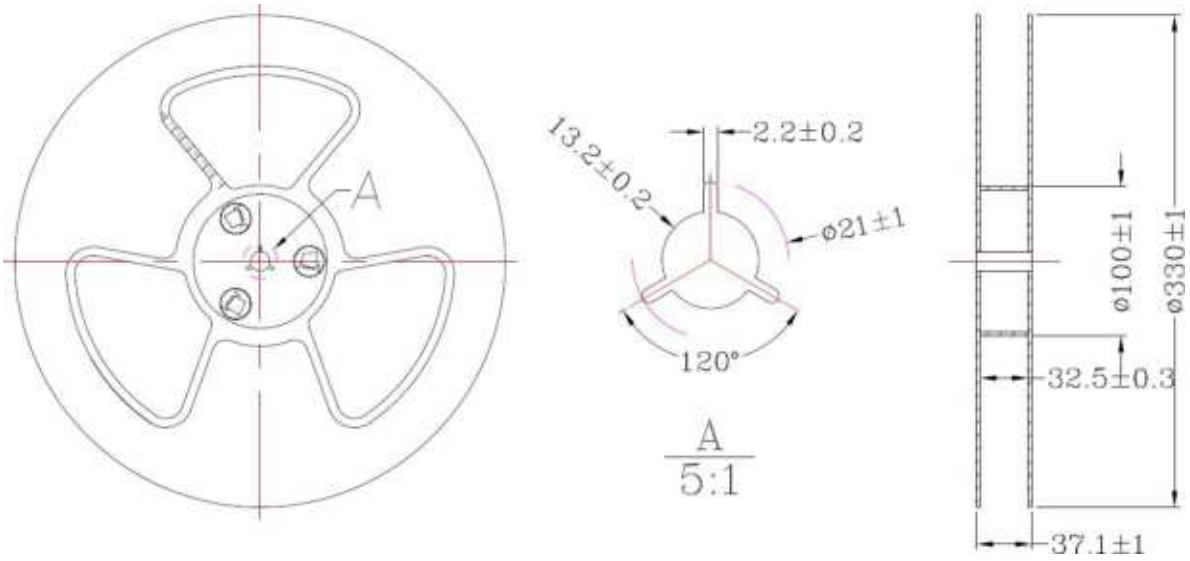


Figure 16: Reel Dimensions

12 Regulatory

Note: For complete regulatory information, refer to the Lyra P Regulatory Information document which is also available from the Lyra Series product page.

The Lyra P holds current certifications in the following countries:

Country/Region	Regulatory ID
USA (FCC)	SQG-LyraP
Canada (ISED)	3147A-LyraP
UK (UKCA)	N/A
EU	N/A
Japan (MIC)	209-J00456
Korea (KC)	R-C-L7C-LyraP

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13 Bluetooth SIG Qualification

13.1 Overview

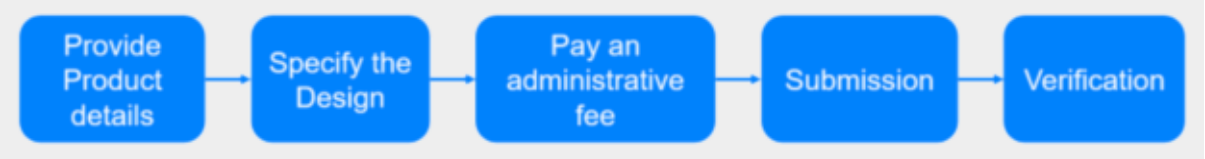
The Bluetooth Qualification Process promotes global product interoperability and reinforces the strength of the Bluetooth® brand and ecosystem to the benefit of all Bluetooth SIG members. The Bluetooth Qualification Process helps member companies ensure their products that incorporate Bluetooth technology comply with the Bluetooth Patent & Copyright License Agreement and the Bluetooth Trademark License Agreement (collectively, the Bluetooth License Agreement) and Bluetooth Specifications.

The Bluetooth Qualification Process is defined by the Qualification Program Reference Document (QPRD) v3.

To demonstrate that a product complies with the Bluetooth Specification(s), each member must for each of its products:

- Identify the product, the design included in the product, the Bluetooth Specifications that the design implements, and the features of each implemented specification
- Complete the Bluetooth Qualification Process by submitting the required documentation for the product under a user account belonging to your company

The Bluetooth Qualification Process consists of the phases shown below:



To complete the Qualification Process the company developing a Bluetooth End Product shall be a member of the Bluetooth SIG. To start the application please use the following link: Apply for Adopter Membership

13.2 Scope

This guide is intended to provide guidance on the Bluetooth Qualification Process for End Products that reference a single existing design, that has not been modified, (refer to Section 3.2.1 of the Qualification Program Reference Document v3).

This option applies to a Member qualifying a Product that includes an existing Design that has a DN, QDID, or DID and that Design has not been modified (e.g., rebranding a Qualified Product from another Member). The Design identified by the DN, QDID, or DID may only implement Bluetooth Specifications that are active or deprecated at the time of Submission. No modifications may be made to the Design, including changes to the ICS Form.

Changes to the Product outside the Design are allowed, including:

- Enabling technologies
- Changes to the industrial design
- Changes to the communication technology other than Bluetooth
- Changes to the features that are unrelated to Bluetooth, branding, packaging, colour, shape, Product name, or Model number

Members are responsible for assessing that modifications to the Product outside of the Design do not affect compliance with Bluetooth Specifications or result in a change to the ICS Form.

For the purposes of this document, it is assumed that the member is combining a single unmodified Core-Complete Configuration.

13.3 Qualification Steps When Referencing a single existing design, (unmodified) – Option 1 in the QPRDv3

For this qualification, follow these steps:

1. To start a listing, go to: https://qualification.bluetooth.com/
2. Select **Start the Bluetooth Qualification Process**.
3. Product Details to be entered:
    - Project Name (this can be the product name or the Bluetooth Design name).
    - Product Description
    - Model Number

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- Product Publication Date (the product publication date may not be later than 90 days after submission)
- Product Website (optional)
- Internal Visibility (this will define if the product will be visible to other users prior to publication)
- If you have multiple End Products to list then you can select 'Import Multiple Products', firstly downloading and completing the template, then by 'Upload Product List'. This will populate Qualification Workspace with all your products.

4. Specify the Design:
   - Do you include any existing Design(s) in your Product? Answer Yes, I do.
   - Enter the single DN or QDID used in your, (for Option 1 only one DN or QDID can be referenced)
   - Once the DN or QDID is selected it will appear on the left-hand side, indicating the layers covered by the design.
   - Select 'I'm finished entering DN's
   - What do you want to do next? Answer, 'Use this Design without Modification'
   - Save and go to Product Qualification Fee
5. Product Qualification Fee:
   - It's important to make sure a Prepaid Product Qualification fee is available as it is required at this stage to complete the Qualification Process.
   - Prepaid Product Qualification Fee's will appear in the available list so select one for the listing.
   - If one is not available select 'Pay Product Qualification Fee', payment can be done immediately via credit card, or you can pay via Invoice. Payment via credit will release the number immediately, if paying via invoice the number will not be released until the invoice is paid.
   - Once you have selected the Prepaid Qualification Fee, select 'Save and go to Submission'
6. Submission:
   - Some automatic checks occur to ensure all submission requirements are complete.
   - To complete the listing any errors must be corrected
   - Once you have confirmed all design information is correct, tick all of the three check boxes and add your name to the signature page.
   - Now select 'Complete the Submission'.
   - You will be asked a final time to confirm you want to proceed with the submission, select 'Complete the Submission'.
   - Qualification Workspace will confirm the submission has been submitted. The Bluetooth SIG will email confirmation once the submission has been accepted, (normally this takes 1 working day).
7. Download Product and Design Details:
   a. You can now download a copy of the confirmed listing from the design listing page and save a copy in your Compliance Folder

For further information, please refer to the following webpage:
https://www.bluetooth.com/develop-with-bluetooth/qualification-listing/

13.4 Example Designs for reference

The following gives an example of a design possible under option 1:

Ezurio End Product design using Silicon Labs Component based design

Design Name	Owner	Declaration ID	QD ID	Link to listing on the SIG website
Lyra P	Ezurio	D057226	182888	https://qualification.bluetooth.com/ListingDetails/147724

13.5 Qualify More Products

If you develop further products based on the same design in the future, it is possible to add them free of charge. The new product must not modify the existing design i.e add ICS functionality, otherwise a new design listing will be required.

To add more products to your design, select 'Manage Submitted Products' in the Getting Started page, Actions, Qualify More Products. The tool will take you through the updating process.

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14 Additional Information

Please contact your local sales representative or our support team for further assistance:

Headquarters	Ezurio 50 S. Main St. Suite 1100 Akron, OH 44308 USA
Website	http://www.ezurio.com
Technical Support	http://www.ezurio.com/resources/support
Sales Contact	http://www.ezurio.com/contact

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