Data Sheet

ACPL-P346/ACPL-W346

2.5-Amp Output Current Power, GaN and SiC MOSFET Gate Drive Optocoupler with Rail-to-Rail Output

Description

The Broadcom® ACPL-P346/W346 contains an AlGaAs LED, which is optically coupled to an integrated circuit with a power output stage. This optocoupler is ideally suited for driving power, GaN (Gallium Nitride) and SiC(Silicon Carbide) MOSFETs used in inverter or AC-DC/DC-DC converter applications. The high operating voltage range of the output stage provides the drive voltages required by gate controlled devices. The voltage and high peak output current supplied by this optocoupler make it ideally suited for direct driving MOSFETs at high frequency for high efficiency conversion. The ACPL-P346 and ACPL-W346 have the highest insulation voltage of V_{IORM} = 891 V_{peak} and V_{IORM} = 1140Vpeak respectively in the IEC/EN/DIN EN 60747-5-5.

Features

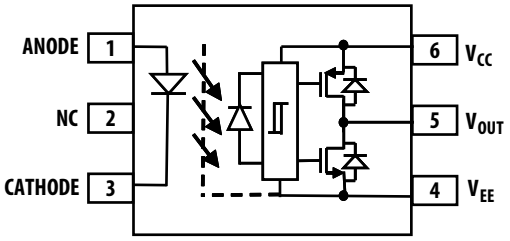
- 2.5A maximum peak output current
- 2.0A minimum peak output current
- Rail-to-rail output voltage
- 120 ns maximum propagation delay
- 50 ns maximum propagation delay difference
- LED current input with hysteresis
- 100 kV/µs minimum Common Mode Rejection (CMR) at V_{CM} = 1500V
- I_{CC} = 4.0 mA maximum supply current
- Under Voltage Lock-Out protection (UVLO) with hysteresis
- Wide operating V_{CC} Range: 10V to 20V
- Industrial temperature range: –40°C to +105°C
- Safety Approval
  - UL Recognized 3750V/5000 V_{RMS} for 1 min.
  - CSA
  - IEC/EN/DIN EN 60747-5-5 V_{IORM} = 891V/ 1140 V_{peak}

Applications

- Power, GaN, and SiC MOSFET gate drive
- AC and brushless DC motor drives
- Switching power supplies

CAUTION! It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD. The components featured in this data sheet are not to be used in military or aerospace applications or environments.

Functional Diagram



NOTE: A 1-µF bypass capacity must be connected between pins V_{CC} and V_{EE}.

Truth Table

LED	$V_{CC} - V_{EE}$ POSITIVE GOING (TURN-ON)	$V_{CC} - V_{EE}$ NEGATIVE GOING (TURN-OFF)	V_O
OFF	0V to 20V	0V to 20V	LOW
ON	0V to 8.1V	0V to 7.1V	LOW
ON	8.1V to 9.1V	7.1V to 8.1V	TRANSITION
ON	9.1V to 20V	8.1V to 20V	HIGH

Ordering information

ACPL-P346 is UL Recognized with 3750 V_{RMS} for 1 minute per UL1577.

ACPL-W346 is UL Recognized with 5000 V_{RMS} for 1 minute per UL1577.

Part Number	Option	Package	Surface Mount	Tape and Reel	IEC/EN/DIN EN 60747-5-5	Quantity
	RoHS Compliant					
ACPL-P346 ACPL-W346	-000E	Stretched SO-6	X			100 per tube
	-500E		X	X		1000 per reel
	-060E		X		X	100 per tube
	-560E		X	X	X	1000 per reel

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

Example 1:

ACPL-P346-560E to order product of Stretched SO-6 Surface Mount package in Tape and Reel packaging with IEC/EN/DIN EN 60747-5-5 Safety Approval in RoHS compliant.

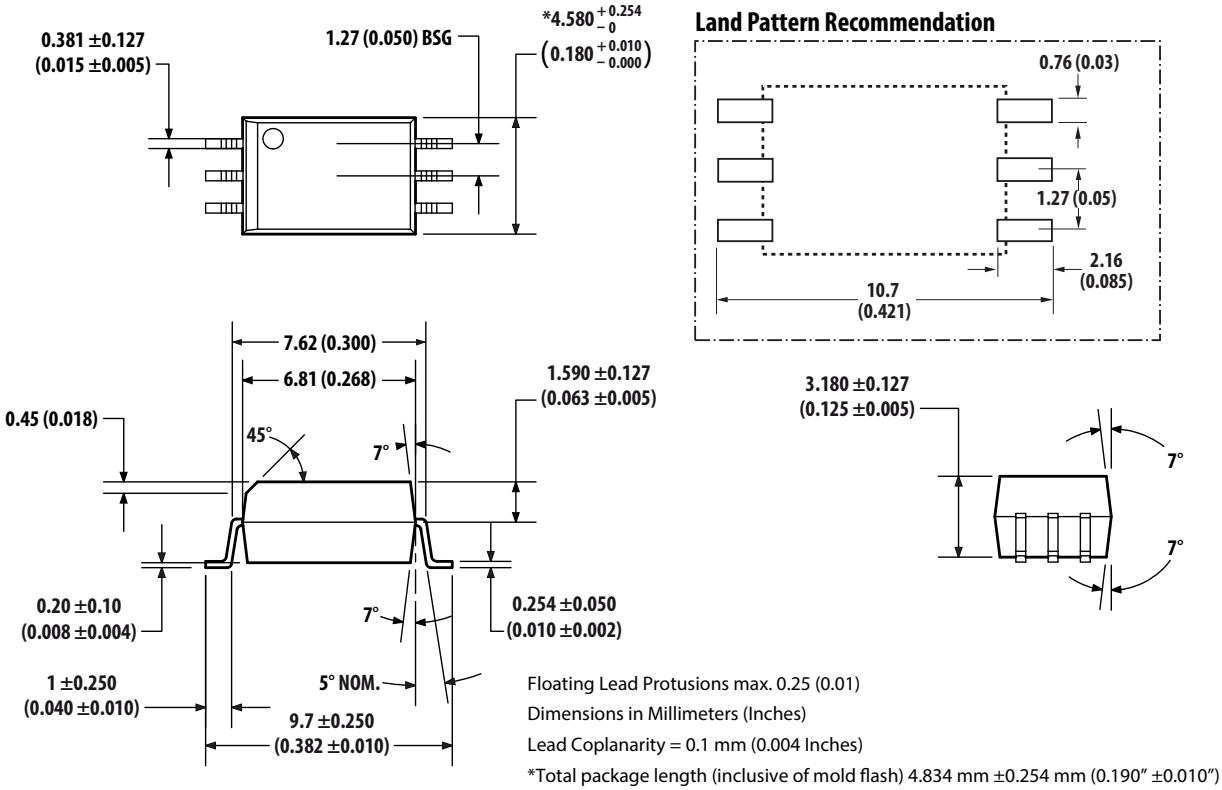
Example 2:

ACPL-W346-000E to order product of Stretched SO-6 Surface Mount package in Tube packaging and RoHS compliant.

Option data sheets are available. Contact your Broadcom sales representative or authorized distributor for information.

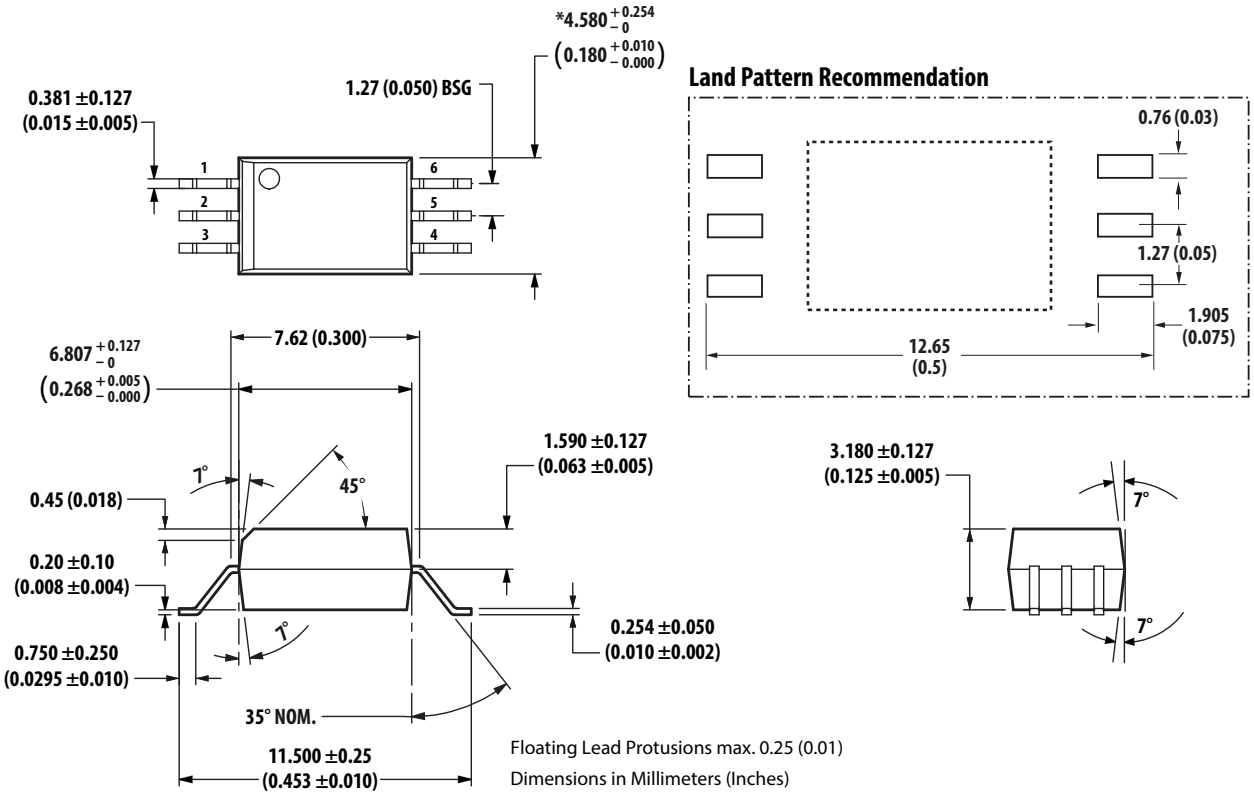
Package Outline Drawing

ACPL-P346 Stretched SO-6 Package (7-mm Clearance)



Floating Lead Protusions max. 0.25 (0.01)
Dimensions in Millimeters (Inches)
Lead Coplanarity = 0.1 mm (0.004 Inches)
*Total package length (inclusive of mold flash) 4.834 mm ±0.254 mm (0.190″ ±0.010″)

ACPL-W346 Stretched SO-6 Package (8-mm Clearance)



Floating Lead Protusions max. 0.25 (0.01)
Dimensions in Millimeters (Inches)
Lead Coplanarity = 0.1 mm (0.004 Inches)
*Total package length (inclusive of mold flash) 4.834 mm ±0.254 mm (0.190″ ±0.010″)

Recommended Pb-Free IR Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision). Non-Halide Flux should be used.

Regulatory Information

The ACPL-P346/W346 is approved by the following organizations.

UL	Recognized under UL 1577, component recognition program up to V_{ISO} = 3750 V_{RMS} (ACPL-P346) and V_{ISO} = 5000 V_{RMS} (ACPL-W346).
CSA	CSA Component Acceptance Notice #5, File CA 88324
IEC/EN/DIN EN 60747-5-5 (Option 060 Only)	Maximum Working Insulation Voltage V_{IORM} = 891 V_{peak} (ACPL-P346) and V_{IORM} = 1140 V_{peak} (ACPL-W346)

IEC/EN/DIN EN 60747-5-5 Insulation Characteristics (Option 060)[a]

Description	Symbol	ACPL-P346 Option 060	ACPL-W346 Option 060	Units
Installation classification per DIN VDE 0110/39, Table 1				
for rated mains voltage ≤ 150 V_{RMS}		I-IV	I-IV	
for rated mains voltage ≤ 300 V_{RMS}		I-IV	I-IV	
for rated mains voltage ≤ 450 V_{RMS}		I-III	I-IV	
for rated mains voltage ≤ 600 V_{RMS}		I-III	I-IV	
for rated mains voltage ≤ 1000 V_{RMS}			I-III	
Climatic Classification		40/105/21	40/105/21	
Pollution Degree (DIN VDE 0110/39)		2	2	
Maximum Working Insulation Voltage	V_{IORM}	891	1,140	V_{peak}
Input to Output Test Voltage, Method b[a] V_{IORM} × 1.875 = V_{PR}, 100% Production Test with t_m =1 second, Partial discharge < 5 pC	V_{PR}	1,671	2,137	V_{peak}
Input to Output Test Voltage, Method a[a] V_{IORM} × 1.6 = V_{PR}, Type and Sample Test, t_m =10 seconds, Partial discharge < 5 pC	V_{PR}	1,426	1,824	V_{peak}
Highest Allowable Overvoltage[a] (Transient Overvoltage t_{ini} = 60 seconds)	V_{IOTM}	6,000	8,000	V_{peak}
Safety-limiting values – maximum values allowed in the event of a failure				
Case Temperature	T_S	175	175	°C
Input Current	$I_{S, INPUT}$	230	230	mA
Output Power	$P_{S, OUTPUT}$	600	600	mW
Insulation Resistance at T_S, V_{IO} = 500V	R_S	$>10^9$	$>10^9$	Ω

a. Refer to IEC/EN/DIN EN 60747-5-5 Optoisolator Safety Standard section of the *Broadcom Regulatory Guide to Isolation Circuits*, AV02-2041EN, for a detailed description of Method a and Method b partial discharge test profiles.

NOTE: These optocouplers are suitable for “safe electrical isolation” only within the safety limit data. Maintenance of the safety data shall be ensured by means of protective circuits. Surface mount classification is Class A in accordance with CECC 00802.

Insulation and Safety-Related Specifications

Parameter	Symbol	ACPL-P346	ACPL-W346	Unit	Conditions
Minimum External Air Gap (Clearance)	L(101)	7.0	8.0	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (Creepage)	L(102)	8.0	8.0	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	0.08	mm	Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and detector.
Tracking Resistance (Comparative Tracking Index)	CTI	>175	>175	V	DIN EN 60112 (2010-05)
Isolation Group		IIIa	IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

NOTE: All Broadcom data sheets report the creepage and clearance inherent to the optocoupler component itself. These dimensions are needed as a starting point for the equipment designer when determining the circuit insulation requirements. However, once mounted on a printed circuit board, minimum creepage and clearance requirements must be met as specified for individual equipment standards. For creepage, the shortest distance path along the surface of a printed circuit board between the solder fillets of the input and output leads must be considered (the recommended land pattern does not necessarily meet the minimum creepage of the device). There are recommended techniques, such as grooves and ribs, that may be used on a printed circuit board to achieve desired creepage and clearances. Creepage and clearance distances will also change depending on factors, such as pollution degree and insulation level.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Notes
Storage Temperature	T_S	–55	+125	°C	
Operating Temperature	T_A	–40	+105	°C	
Output IC Junction Temperature	T_J	—	125	°C	
Average Input Current	$I_{F(AVG)}$	—	25	mA	a
Peak Transient Input Current (<1 second pulse width, 300 pps)	$I_{F(TRAN)}$	—	1	A	
Reverse Input Voltage	V_R	—	5	V	
“High” Peak Output Current	$I_{OH(PEAK)}$	—	2.5	A	b
“Low” Peak Output Current	$I_{OL(PEAK)}$	—	2.5	A	b
Total Output Supply Voltage	$(V_{CC} – V_{EE})$	0	25	V	
Output Voltage	$V_{O(PEAK)}$	–0.5	V_{CC}	V	
Output IC Power Dissipation	P_O	—	500	mW	c
Total Power Dissipation	P_T	—	550	mW	d

a. Derate linearly above 85°C free-air temperature at a rate of 0.3 mA/°C.

b. Maximum pulse width = 10 µs. This value is intended to allow for component tolerances for designs with I_O peak minimum = 2.0A. See applications section for additional details on limiting I_{OH} peak.

c. Derate linearly above 85°C free-air temperature at a rate of 12.5 mW/°C.

d. Derate linearly above 85°C free-air temperature at a rate of 13.75 mW/°C. The maximum LED junction temperature should not exceed 125°C.

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Notes
Operating Temperature	T_A	–40	+105	°C	
Output Supply Voltage	$(V_{CC} – V_{EE})$	10	20	V	
Input Current (ON)	$I_{F(ON)}$	7	11	mA	
Input Voltage (OFF)	$V_{F(OFF)}$	–3.6	+0.8	V	

Electrical Specifications (DC)

All typical values are at T_A = 25°C, $V_{CC} – V_{EE}$ = 10V, V_{EE} = Ground. All minimum and maximum specifications are at recommended operating conditions (T_A = –40°C to +105°C, $I_{F(ON)}$ = 7 mA to +11 mA, $V_{F(OFF)}$ = –3.6V to +0.8V, V_{EE} = Ground, V_{CC} = 10V to 20V), unless otherwise noted.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure	Notes
High Level Peak Output Current	I_{OH}	–2.0	–3.4	—	A	$V_{CC} – V_O$ = 10V	3, 4	a
Low Level Peak Output Current	I_{OL}	2.0	4.4	—	A	$V_O – V_{EE}$ = 10V	6, 7	a
High Output Transistor RDS(ON)	$R_{DS,OH}$	0.3	1.7	3.5	Ω	I_{OH} = –2.0A	8	b
Low Output Transistor RDS(ON)	$R_{DS,OL}$	0.3	0.7	2.0	Ω	I_{OL} = 2.0A	9	b
High Level Output Voltage	V_{OH}	V_{CC} – 0.3	V_{CC} – 0.2	—	V	I_O = –100 mA, I_F = 9 mA	2, 4	c, d
High Level Output Voltage	V_{OH}	—	V_{CC}	—	V	I_O = 0 mA, I_F = 9 mA	1	
Low Level Output Voltage	V_{OL}	—	0.1	0.25	V	I_O = 100 mA	5, 7	
High Level Supply Current	I_{CCH}	—	2.6	4.0	mA	I_F = 9 mA	10, 11	
Low Level Supply Current	I_{CCL}	—	2.6	4.0	mA	V_F = 0V		
Threshold Input Current Low to High	I_{FLH}	0.5	1.5	4.0	mA	V_O > 5V	12, 13	
Threshold Input Voltage High to Low	V_{FHL}	0.8	—	—	V			
Input Forward Voltage	V_F	1.2	1.55	1.95	V	I_F = 9 mA	19	
Temperature Coefficient of Input Forward Voltage	$\Delta V_F/\Delta T_A$	—	–1.7	—	mV/°C			
Input Reverse Breakdown Voltage	BV_R	5	—	—	V	IR = 100 A		
Input Capacitance	C_{IN}	—	70	—	pF	f = 1 MHz, V_F = 0V		
UVLO Threshold	V_{UVLO+}	8.1	8.6	9.1	V	V_O > 5V, I_F = 9 mA		
	V_{UVLO-}	7.1	7.6	8.1				
UVLO Hysteresis	$UVLO_{HYS}$	0.5	1.0	—	V			

a. Maximum pulse width = 10 µs.

b. Output is sourced at –2.0A/+2.0A with a maximum pulse width = 10 µs.

c. In this test, V_{OH} is measured with a DC load current. When driving capacitive loads, V_{OH} will approach V_{CC} as I_{OH} approaches zero amps.

d. Maximum pulse width = 1 ms.

Switching Specifications (AC)

All typical values are at T_A = 25°C, V_{CC} – V_{EE} = 10V, V_{EE} = Ground. All minimum and maximum specifications are at recommended operating conditions (T_A = –40°C to +105°C, $I_{F(ON)}$ = 7 mA to 11 mA, $V_{F(OFF)}$ = –3.6V to +0.8V, V_{EE} = Ground), unless otherwise noted.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure	Notes
Propagation Delay Time to High Output Level	t_{PLH}	30	55	120	ns	Rg = 10Ω, Cg = 10 nF, f = 200 kHz, Duty Cycle = 50%, V_{CC} = 10V	14, 15, 16, 17	
Propagation Delay Time to Low Output Level	t_{PHL}	30	55	120	ns			
Pulse Width Distortion	PWD		0	50	ns			a
Propagation Delay Difference Between Any Two Parts	PDD (t_{PHL} – t_{PLH})	–50	—	+50	ns		24, 25	b
Propagation Delay Skew	t_{PSK}	—	—	40	ns			c
Rise Time	t_R	—	8	30	ns	Cg = 1 nF, f = 200 kHz, Duty Cycle = 50%, V_{CC} = 10V	18, 20	
Fall Time	t_F	—	8	30	ns			
Output High Level Common Mode Transient Immunity	$\|CM_H\|$	100	—	—	kV/µs	T_A = 25°C, I_F = 9 mA, V_{CC} = 20V, V_{CM} = 1500V with split resistors	21	d, e
Output Low Level Common Mode Transient Immunity	$\|CM_L\|$	100	—	—	kV/µs	T_A = 25°C, V_F = 0V, V_{CC} = 20V, V_{CM} = 1500V with split resistors		f

a. Pulse Width Distortion (PWD) is defined as $|t_{PHL} – t_{PLH}|$ for any given device.

b. The difference between t_{PHL} and t_{PLH} between any two ACPL-P346 parts under the same test condition.

c. t_{PSK} is equal to the worst case diff erence in t_{PHL} and/or t_{PLH} that will be seen between units at any given temperature and specified test conditions.

d. Pin 2 must be connected to LED common. Split resistor network in the ratio 1.5:1 with 232Ω at the anode and 154Ω at the cathode.

e. Common mode transient immunity in the high state is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM}, to assure that the output will remain in the high state (meaning V_O > 10.0V).

f. Common mode transient immunity in a low state is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM}, to assure that the output will remain in a low state (meaning V_O < 1.0V).

Package Characteristics

All typical values are at T_A = 25°C. All minimum/maximum specifications are at recommended operating conditions, unless otherwise noted.

Parameter	Symbol	Device	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Input-Output Momentary Withstand Voltage[a]	V_{ISO}	ACPL-P346	3750	—	—	V_{RMS}	RH < 50%, t = 1 min., T_A = 25°C		b, c
		ACPL-W346	5000	—	—	V_{RMS}	RH < 50%, t = 1 min., T_A = 25°C		c, d
Input-Output Resistance	R_{I-O}		—	$>50^{12}$	—	Ω	V_{I-O} = 500 V_{DC}		c
Input-Output Capacitance	C_{I-O}		—	0.6	—	pF	f =1 MHz		
LED-to-Ambient Thermal Resistance	R_{11}		—	135	—	°C/W			e
LED-to-Detector Thermal Resistance	R_{12}		—	27	—				
Detector-to-LED Thermal Resistance	R_{21}		—	39	—				
Detector-to-Ambient Thermal Resistance	R_{22}		—	47	—				

a. The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating, refer to your equipment level safety specification or Broadcom Application Note 1074, *Optocoupler Input-Output Endurance Voltage*.

b. In accordance with UL1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 4500 V_{RMS} for 1 second (leakage detection current limit, I_{I-O} ≤ 5 μA).

c. Device considered a two-terminal device: pins 1, 2, and 3 shorted together and pins 4, 5, and 6 shorted together.

d. In accordance with UL1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 6000 V_{RMS} for 1 second (leakage detection current limit, I_{I-O} ≤ 5 μA).

e. The device was mounted on a high conductivity test board as per JEDEC 51-7.

Typical Performance Plots

Figure 1: High Ouput Rail Voltage vs. Temperature

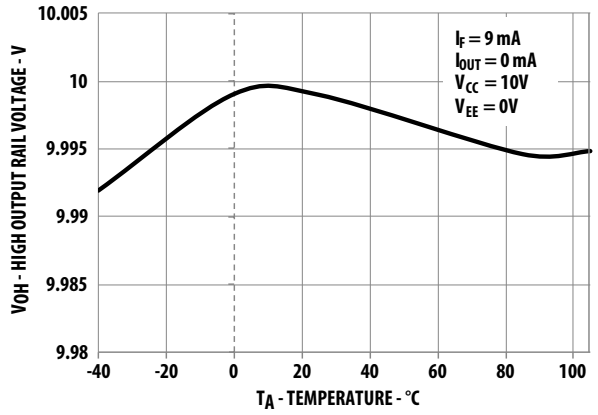


Figure 2: V_{OH} vs. Temperature

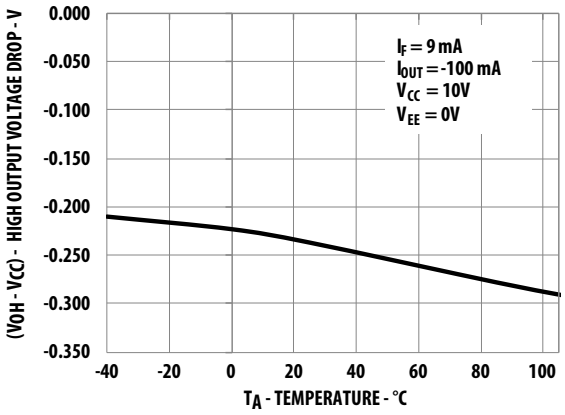


Figure 3: I_{OH} vs. Temperature

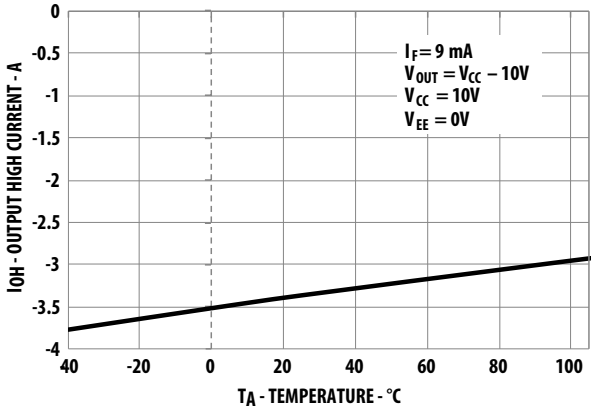


Figure 4: I_{OH} vs. V_{OH}

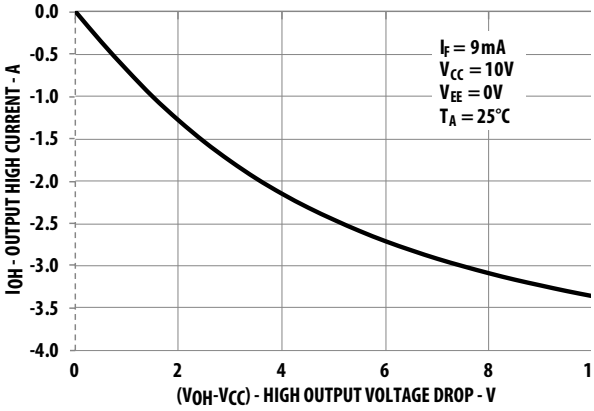


Figure 5: V_{OL} vs. Temperature

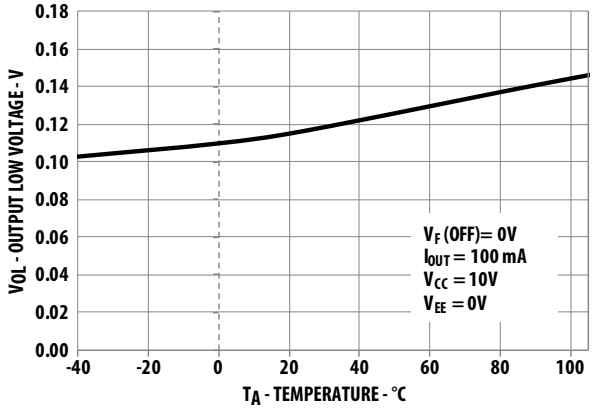


Figure 6: I_{OL} vs. Temperature

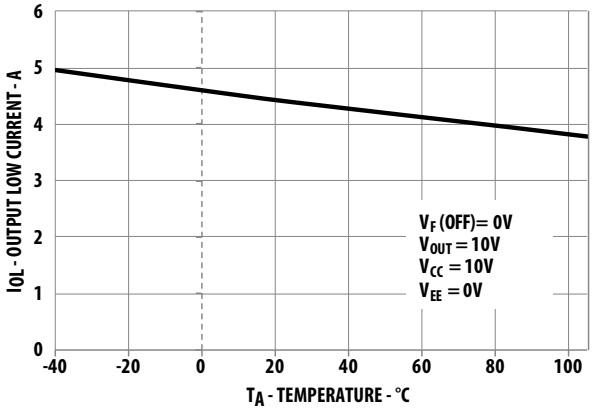


Figure 7: I_{OL} vs. V_{OL}

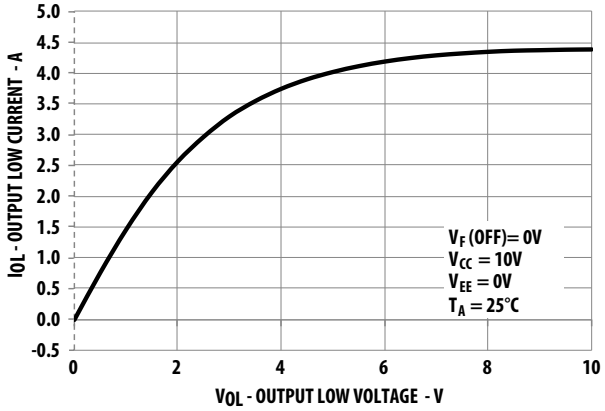


Figure 8: $R_{DS,OH}$ vs. Temperature

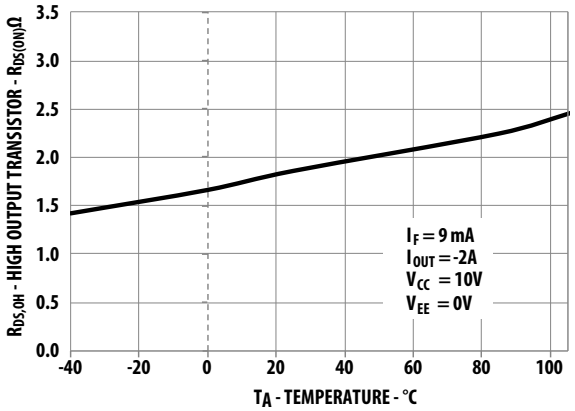


Figure 9: $R_{DS,OL}$ vs. Temperaure

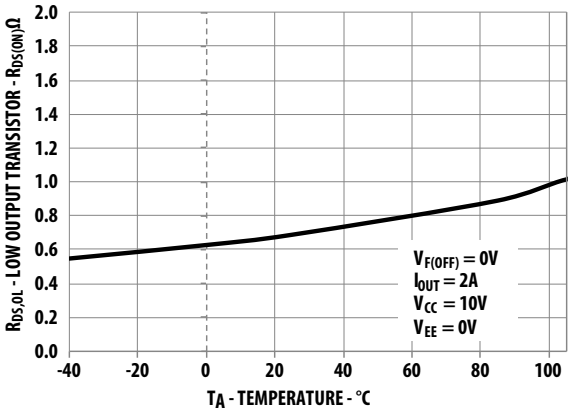


Figure 10: I_{CC} vs. Temperature

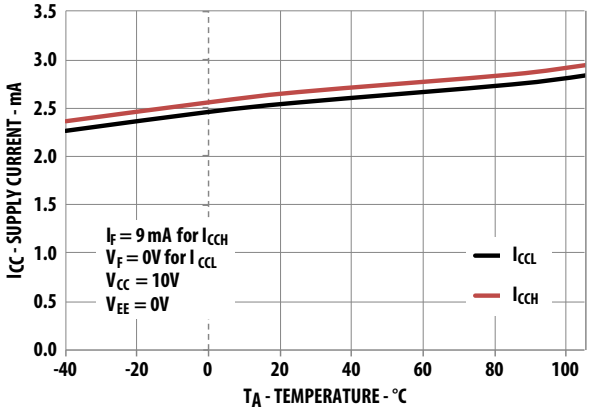


Figure 11: I_{CC} vs. V_{CC}

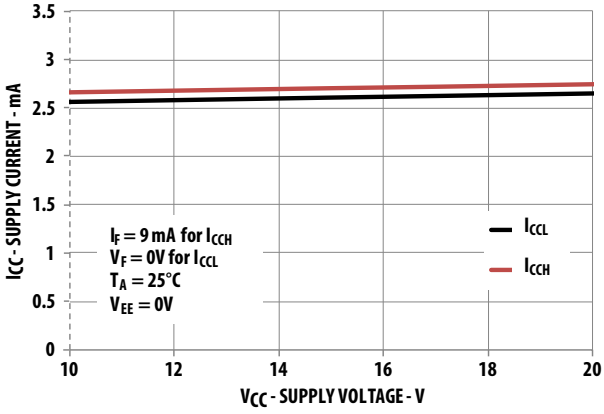


Figure 12: I_{FLH} Hysteresis

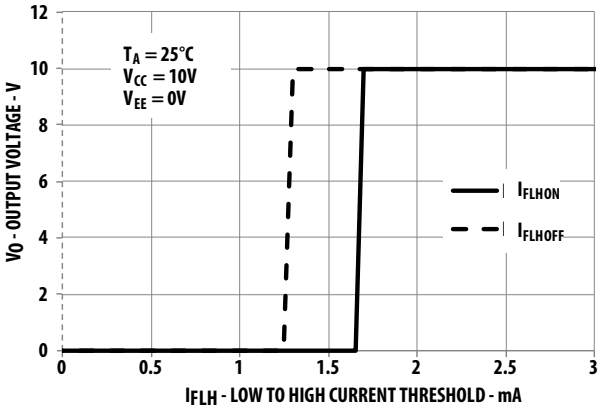


Figure 13: I_{FLH} vs. Temperature

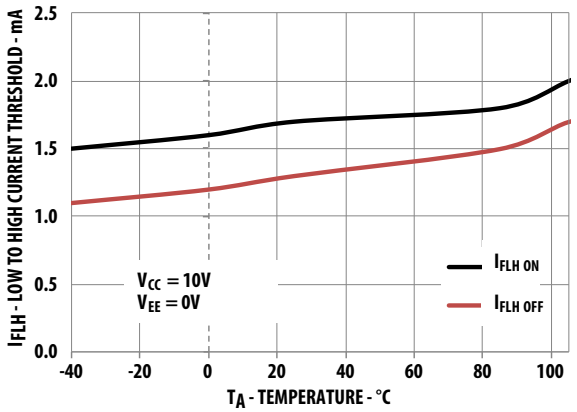


Figure 14: Propagation Delay vs. I_F

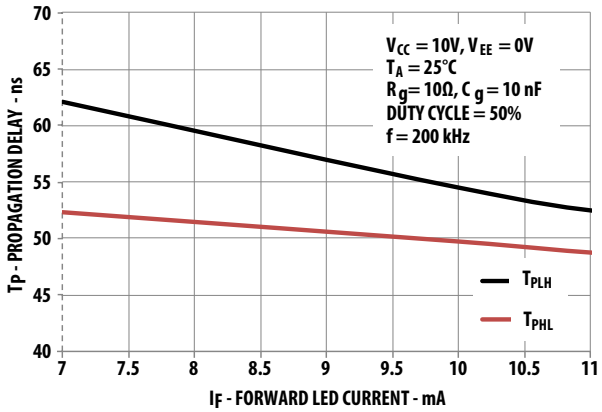


Figure 15: Propagation Delay vs. Temperature

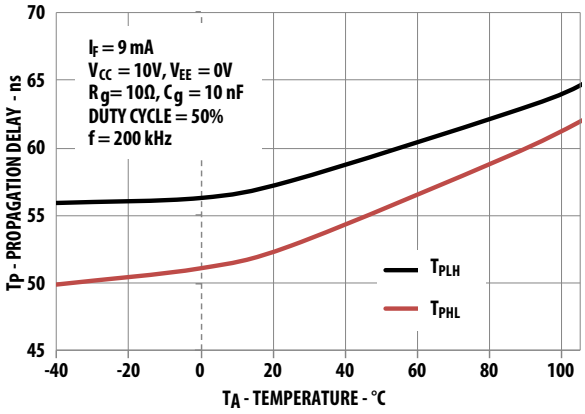


Figure 16: Propagation Delay vs. Rg

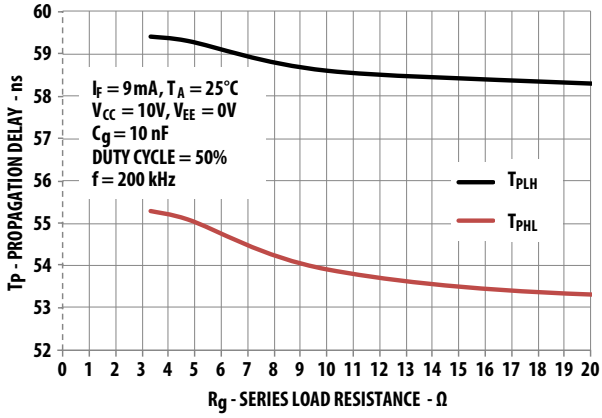


Figure 17: Propagaton Delay vs. Cg

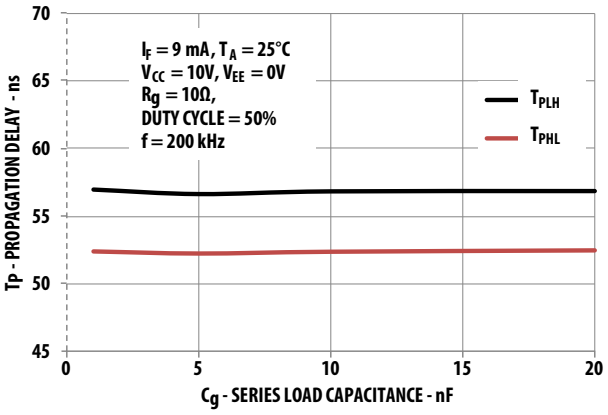


Figure 18: Rise and Fall Times vs. Cg

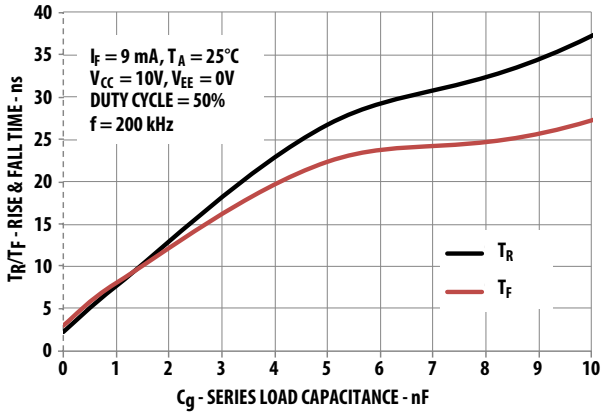


Figure 19: Input Current vs. Forward Voltage

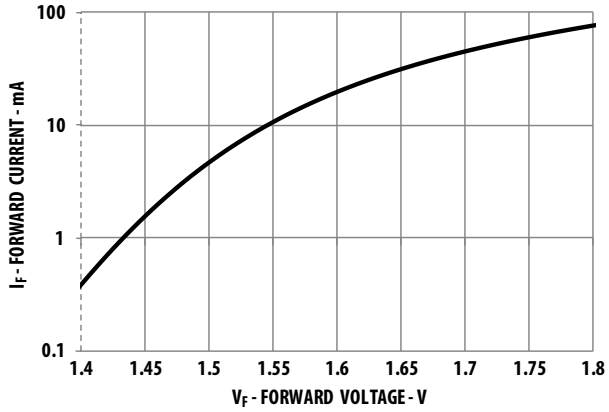


Figure 20: t_r and t_f Test Circuit and Waveforms

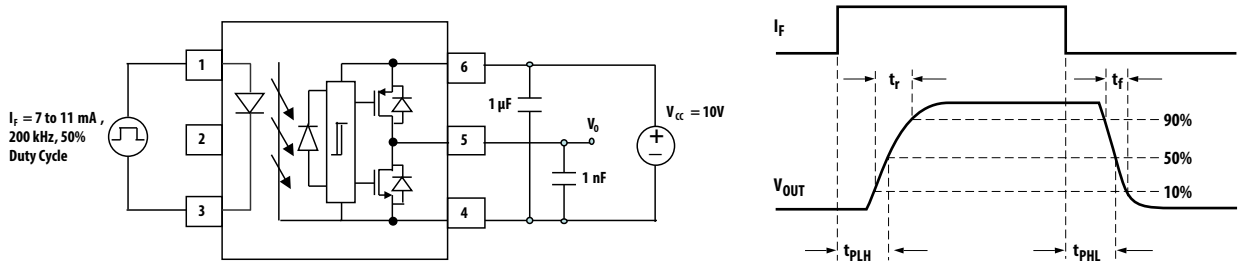
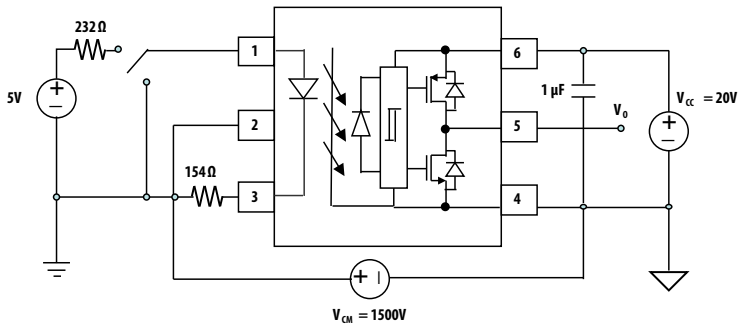


Figure 21: CMR Test Circuit wiht Split Resistors Network



Application Information

Product Overview Description

The ACPL-P346/W346 is an optically isolated power output stage capable of driving power, GaN or SiC MOSFET. Based on BCDMOS technology, this gate drive optocoupler delivers higher peak output current, better rail-to-rail output voltage performance and two times faster speed than the previous generation products.

The high peak output current and short propagation delay are needed for fast MOSFET switching to reduce dead time and improve system overall efficiency. Rail-to-rail output voltage ensures that the MOSFET's gate voltage is driven to the optimum intended level with no power loss across the MOSFET. This helps the designer lower the system power which is suitable for bootstrap power supply operation.

It has very high CMR (common mode rejection) rating which allows the microcontroller and the MOSFET to operate at very large common mode noise found in industrial motor drives and other power switching applications. The input is driven by direct LED current and has a hysteresis that prevents output oscillation if insufficient LED driving current is applied. This will eliminates the need of additional Schmitt trigger circuit at the input LED.

The stretched SO6 package, which is up to 50% smaller than a conventional DIP package, facilitates a smaller and more compact design. These stretched packages are compliant to many industrial safety standards, such as IEC/EN/DIN EN 60747-5-5, UL 1577 and CSA.

Recommended Application Circuit

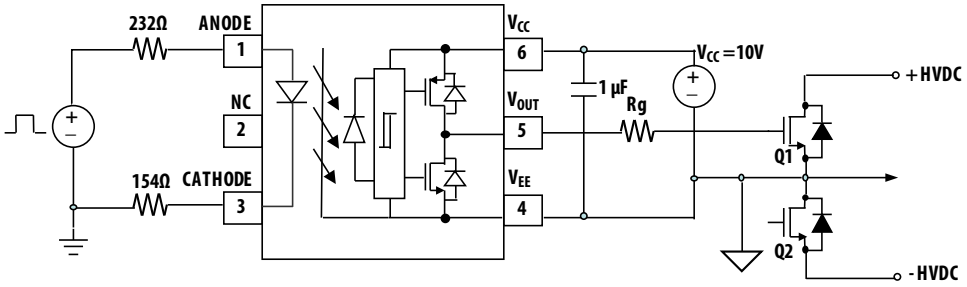
The recommended application circuit shown in Figure 22 illustrates a typical gate drive implementation using the ACPL-P346.

The supply bypass capacitors (1 µF) provide the large transient currents necessary during a switching transition. Because of the transient nature of the charging currents, a low current (4.0 mA) power supply will be enough to power the device. The split resistors (in the ratio of 1.5:1) across the LED will provide a high CMR response by providing a balanced resistance network across the LED.

The gate resistor R_G serves to limit gate charge current and controls the MOSFET switching times.

In PC board design, care should be taken to avoid routing the MOSFET drain or source traces close to the ACPL-P346 input as this can result in unwanted coupling of transient signals into ACPL-P346 and degrade performance.

Figure 22: Recommended Application Circuit with Split Resistors LED



Selecting the Gate Resistor (Rg)

Step 1: Calculate Rg minimum from the I_{OL} peak specification. The MOSFET and Rg in Figure 22 can be analyzed as a simple RC circuit with a voltage supplied by ACPL-P346/W346.

$Rg \geq ((V_{CC} - V_{EE}) / I_{OLPEAK}) - R_{DSON(MIN)}$

$= ((10 - 0V) / 25A) - 0.3\Omega$

$= 3.7\Omega$

The external gate resistor, Rg and internal minimum turn-on resistance, R_{DSON} will ensure the output current will not exceed the device absolute maximum rating of 2.5A.

Step 2: Check the ACPL-P346/W346 power dissipation and increase Rg if necessary. The ACPL-P346/W346 total power dissipation (P_T) is equal to the sum of the emitter power (P_E) and the output power (P_O).

$P_T = P_E + P_O$

$P_E = I_F \times V_F \times \text{Duty Cycle}$

$P_O = P_{O(BIAS)} + P_{O(SWITCHING)}$
$= I_{CC} \times (V_{CC} - V_{EE}) + P_{HS} + P_{LS}$

$P_{HS} = (V_{CC} \times Q_G \times f) \times R_{DS,OH(MAX)} / (R_{DS,OH(MAX)} + Rg) / 2$

$P_{LS} = (V_{CC} \times Q_G \times f) \times R_{DS,OL(MAX)} / (R_{DS,OL(MAX)} + Rg) / 2$

Using I_F (worst case) = 11 mA, Rg = 3.7Ω, Max Duty Cycle = 80%, Q_G = 100 nC (650V 20A MOSFET), f = 200 kHz, and T_A max. = 85°C:

$P_E = 11\text{ mA} \times 1.95V \times 0.8 = 17\text{ mW}$

$P_{HS} = (10V \times 100\text{ nC} \times 200\text{ kHz}) \times 3.5 / (3.5 + 3.7) / 2$
$= 48.6\text{ mW}$

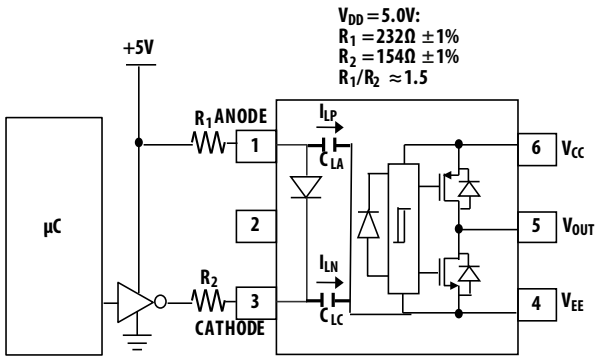
$P_{LS} = (10V \times 100\text{ nC} \times 200\text{ kHz}) \times 2.0/(2.0 + 3.7)/2$
$= 35.1\text{ mW}$

$P_O = 4\text{ mA} \times 10V + 48.6\text{ mW} + 35.1\text{ mW}$
$= 123.7\text{ mW} < 500\text{ mW}$ ($P_{O(MAX)}$ at 85°C)

The value of 4 mA for I_{CC} in the previous equation is the maximum I_{CC} over the entire operating temperature range.

Since P_O is less than $P_{O(MAX)}$, Rg = 3.7Ω is alright for the power dissipation.

Figure 23: Recommended High-CMR Drive Circuit



LED Drive Circuit Considerations for High CMR Performance

Figure 23 shows the recommended drive circuit for the ACPL-P346/W346 that gives optimum common-mode rejection. The two current setting resistors balance the common mode impedances at the LED's anode and cathode. Common-mode transients can be capacitive coupled from the LED anode, through C_{LA} (or cathode through C_{LC}) to the output-side ground causing current to be shunted away from the LED (which is not wanted when the LED should be on) or conversely cause current to be injected into the LED (which is not wanted when the LED should be off).

Table 1 shows the directions of I_{LP} and I_{LN} depend on the polarity of the common-mode transient. For transients occurring when the LED is on, common-mode rejection (CM_H, since the output is at "high" state) depends on LED current (I_F). For conditions where IF is close to the switching threshold (I_{FLH}), CM_H also depends on the extent to which I_{LP} and I_{LN} balance each other. In other words, any condition where a common-mode transient causes a momentary decrease in I_F (meaning when $dV_{CM}/dt > 0$ and $|I_{LP}| > |I_{LN}|$, referring to Table 1) will cause a common-mode failure for transients which are fast enough.

Likewise for a common-mode transient that occurs when the LED is off (that is, CM_L, since the output is at "low" state), if an imbalance between I_{LP} and I_{LN} results in a transient I_F equal to or greater than the switching threshold of the optocoupler, the transient "signal" may cause the output to spike above 1V, which constitutes a CM_L failure. The balanced I_{LED}-setting resistors help equalize the common mode voltage change at the anode and cathode. The shunt drive input circuit will also help to achieve high CML performance by shunting the LED in the off state.

Table 1: Common Mode Pulse Polarity and LED Current Transients

dVCM/dt	I_{LP} Direction	I_{LP} Direction	If $\|I_{LP}\| < \|I_{LN}\|$, I_F Is Momentarily	If $\|I_{LP}\| > \|I_{LN}\|$, I_F Is Momentarily
Positive (>0)	Away from LED anode through C_{LA}	Away from LED cathode through C_{LC}	Increase	Decrease
Negative(<0)	Toward LED anode through C_{LA}	Toward LED cathode through C_{LC}	Decrease	Increase

Dead Time and Propagation Delay Specifications

The ACPL-P346/W346 includes a Propagation Delay Difference (PDD) specification intended to help designers minimize “dead time” in their power inverter designs. Dead time is the time period during which both the high and low side power transistors (Q1 and Q2 in Figure 22) are off. Any overlap in Q1 and Q2 conduction will result in large currents flowing through the power devices between the high and low voltage motor rails.

To minimize dead time in a given design, the turn on of LED2 should be delayed (relative to the turn off of LED1) so that under worst-case conditions, transistor Q1 has just turned off when transistor Q2 turns on, as shown in Figure 24. The amount of delay necessary to achieve this condition is equal to the maximum value of the propagation delay difference specification, PDD_{MAX}, which is specified to be 100 ns over the operating temperature range of –40°C to 105°C.

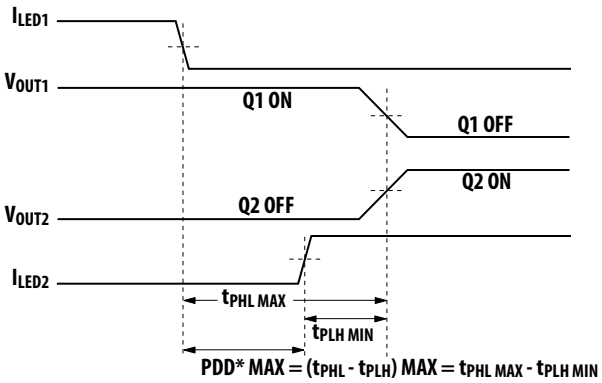
Delaying the LED signal by the maximum propagation delay difference ensures that the minimum dead time is zero, but it does not tell a designer what the maximum dead time will be. The maximum dead time is equivalent to the difference between the maximum and minimum propagation delay difference specifications as shown in Figure 25. The maximum dead time for the ACPL-P346/W346 is 100 ns (= 50 ns – (–50 ns)) over an operating temperature range of –40°C to 105°C.

Note that the propagation delays used to calculate PDD and dead time are taken at equal temperatures and test conditions because the optocouplers under consideration are typically mounted in close proximity to each other and are switching identical MOSFETs.

LED Current Input with Hysteresis

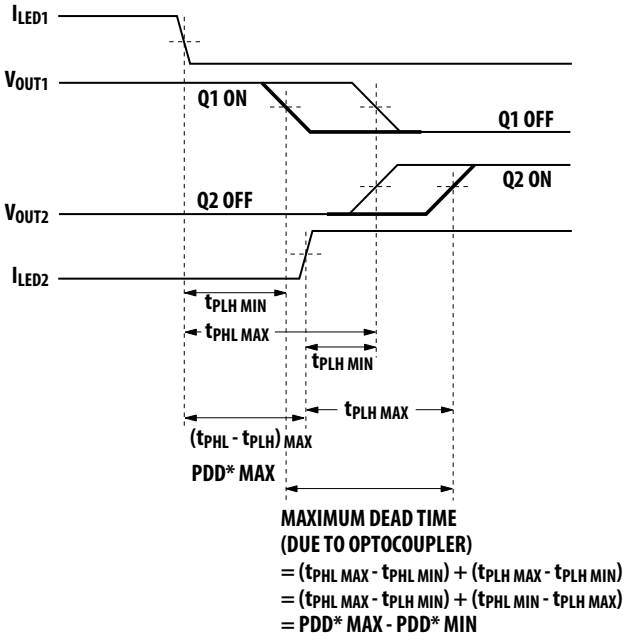
The detector has optical receiver input stage with built-in Schmitt trigger to provide logic compatible waveforms, eliminating the need for additional wave shaping. The hysteresis (Figure 12) provides differential mode noise immunity and minimizes the potential for output signal chatter.

Figure 24: Minimum LED Skew for Zero Dead Time



*PDD = Propagation Delay Difference
Note: For PDD calculations, the propagation delays are taken at the same temperature and test conditions.

Figure 25: Waveforms for Dead Time



*PDD = Propagation Delay Difference
Note: For Dead Time and PDD calculations, all propagation delays are taken at the same temperature and test conditions.

Thermal Model for ACPL-P346/W346 Stretched SO6 Package Optocoupler

Definitions

R_{11}: Junction to Ambient Thermal Resistance of LED due to heating of LED

R_{12}: Junction to Ambient Thermal Resistance of LED due to heating of Detector (Output IC)

R_{21}: Junction to Ambient Thermal Resistance of Detector (Output IC) due to heating of LED.

R_{22}: Junction to Ambient Thermal Resistance of Detector (Output IC) due to heating of Detector (Output IC).

P_1: Power dissipation of LED (W).

P_2: Power dissipation of Detector / Output IC (W).

T_1: Junction temperature of LED (°C).

T_2: Junction temperature of Detector (°C).

Ta: Ambient temperature.

Ambient Temperature: Junction to Ambient Thermal Resistances were measured approximately 1.25 cm above optocoupler at ~23°C in still air.

Thermal Resistance	°C/W
R_{11}	135
R_{12}	27
R_{21}	39
R_{22}	47

This thermal model assumes that an 6-pin single-channel plastic package optocoupler is soldered into a 7.62-cm × 7.62-cm printed circuit board (PCB) per JEDEC standards. The temperature at the LED and Detector junctions of the optocoupler can be calculated using the following equations.

Equation 1:

$$T_1 = (R_{11} \times P_1 + R_{12} \times P_2) + Ta$$

Equation 2:

$$T_2 = (R_{21} \times P_1 + R_{22} \times P_2) + Ta$$

Using the given thermal resistances and thermal model formula in this data sheet, we can calculate the junction temperature for both LED and the output detector. Both junction temperatures should be within the absolute maximum rating.

For example, given P_1 = 17 mW, P_2 = 124 mW, Ta = 85°C:

LED junction temperature,

$$\begin{aligned} T_1 &= (R_{11} \times P_1 + R_{12} \times P_2) + Ta \\ &= (135 \times 0.017 + 27 \times 0.124) + 85 \\ &= 90.7°C \end{aligned}$$

Output IC junction temperature,

$$\begin{aligned} T_2 &= (R_{21} \text{ x } P_1 + R_{22} \text{ x } P_2) + Ta \\ &= (39 \times 0.017 + 47 \times 0.124) + 85 \\ &= 91.5°C \end{aligned}$$

T_1 and T_2 should be limited to 125°C based on the board layout and part placement.

Related Documents

AV02-0421EN	Application Note 5336	*Gate Drive Optocoupler Basic Design for IGBT/MOSFET*
AV02-3698EN	Application Note 1043	*Common-Mode Noise: Sources and Solutions*
AV02-0310EN	Reliability Data	*Plastics Optocouplers Product ESD and Moisture Sensitivity*

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