DATA SHEET

SC Series: MIS Chip Capacitors

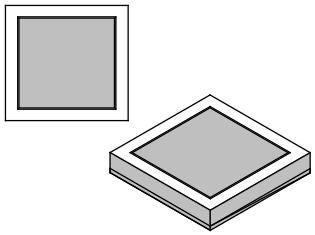
Applications

- Systems requiring DC blocking or RF bypassing
- Fixed capacitance tuning element in filters, oscillators, and matching networks

Features

- Readily available from stock
- High reliability silicon oxide-nitride dielectric
- Low loss: typically 0.04 dB in a 50 Ω system
- Operation through 26 GHz
- Wide temperature operation

Skyworks Green™ products are compliant with all applicable legislation and are halogen-free. For additional information, refer to *Skyworks Definition of Green™*, document number SQ04-0074.



Description

Skyworks Metal Insulator Silicon (MIS) chip capacitors are available in a wide range of sizes and capacitance values. The devices have a dielectric composed of thermally grown silicon dioxide over which a layer of silicon nitride is deposited. This dielectric has a low temperature coefficient of capacitance and very high insulation resistance.

The MIS chip capacitors also exhibit excellent long-term stability, which makes them suitable for high-reliability applications. The capacitors have a high dielectric breakdown, which permits the use of thin dielectrics resulting in large capacitance per unit area.

The temperature coefficient is less than 50 ppm/°C, allowing the capacitors to operate from –65 °C up to 200 °C. Compared to ceramic capacitors, Skyworks MIS chip capacitors offer higher Q and an insertion loss of 0.04 dB in a 50 Ω system. Insulation resistance is greater than 10^5 MΩ.

To accommodate high volume, automated assembly methods, wafers can be supplied on expanded film frames. To reduce cost, chips can be supplied packaged in vials with sample testing only. Packaging in waffle packs with 100 percent electrical testing and visual inspection is also available.

Table 1. MIS Capacitors Absolute Maximum Ratings

Parameter	Symbol	Minimum	Typical	Maximum	Units
Dielectric withstand voltage			100		V
Operating temperature	T_{OP}	–65		+200	°C
Storage temperature	T_{STG}	–65		+200	°C

Note: Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value.

***CAUTION**: Although this device is designed to be as robust as possible, Electrostatic Discharge (ESD) can damage this device. This device must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions should be used at all times.*

Table 2. MIS Chip Capacitors Electrical Specifications (Note 1)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
Capacitance			0.8		1000	pF
Temperature coefficient				50		ppm/°C
Capacitance tolerance			–20		+20	%
Operating temperature	T_{OP}		–65		+200	°C
Dielectric withstand voltage				100		V
Insulation resistance				10^5		MΩ
Leakage current				<1		nA

Note 1: Performance is guaranteed only under the conditions listed in this Table.

Electrical and Mechanical Specifications

The absolute maximum ratings of the MIS chip capacitors are provided in Table 1. Electrical specifications are provided in Table 2.

A graph of typical insertion loss versus frequency is shown in Figure 1. This data is taken from an actual test circuit with series mounted beam-lead or chip capacitors on a 50 Ω microstrip transmission line. The apparent higher loss at lower frequencies on the lower capacitance units is strictly due to the capacitive reactance of the capacitor.

Table 3 provides a list of the available MIS chip capacitors (by part number) and the capacitance and chip dimensions for each one.

Performance

Tests on typical MIS capacitors at the L and S bands show insertion loss to be 1/2 to 1/3 that of equivalent ceramic type capacitors, without any of the associated resonance problems. Power tests indicate that the only limitation is the actual breakdown voltage of the device.

Figure 2 illustrates the use of MIS capacitors in a typical Single-Pole, Double-Throw (SPDT) circuit.

Package Dimensions

Figure 3 provides a visual representation of the capacitor chip sizes and part markings.

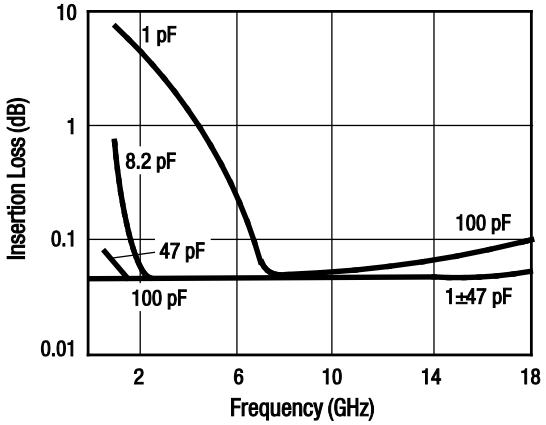


Figure 1. Typical Insertion Loss vs Frequency (50 Ω System)

Table 3. MIS Capacitor Part Numbers

Part Number	Capacitance, ±20% (pF)	Pad/Chip Dimensions (Mils ±1 Mil)	Part Number	Capacitance, ±20% (pF)	Pad/Chip Dimensions (Mils ±1 Mil)
SC00080912	0.8	9/12	SC01001518	10	15/18
SC00120912	1.2	9/12	SC01500912	15	9/12
SC00180912	1.8	9/12	SC01501518	15	15/18
SC00260912	2.6	9/12	SC02201518	22	15/18
SC00380912	3.8	9/12	SC03301518	33	15/18
SC00560912	5.6	9/12	SC04701518	47	15/18
SC00680912	6.8	9/12	SC06801518	68	15/18
SC00820710	8.2	7/10	SC10002430	100	24/30
SC00821518	8.2	15/18	SC33303440	333	34/40
SC01000710	10.0	7/10	SC50004450	500	44/50
SC01000912	10.0	9/12	SC99906068	1000	60/68

Note: Part # structure: SCXXXXYYZZ:
SC = Silicon Conductor
XXXX = Capacitance (pF)
YY = Square contact size (mils), also see Figure 3
ZZ = Square chip size (mils), also see Figure 3

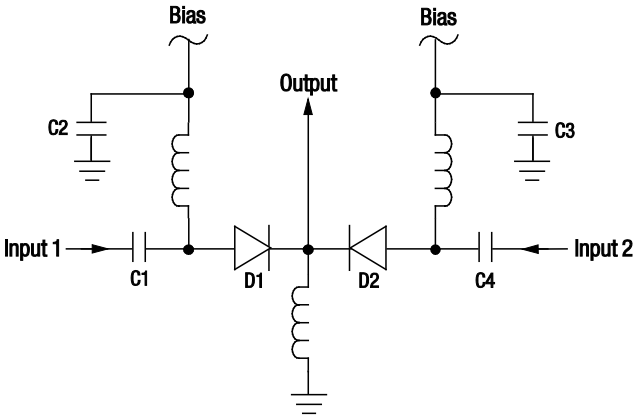


Figure 2. Typical MIS Capacitor Application Circuit

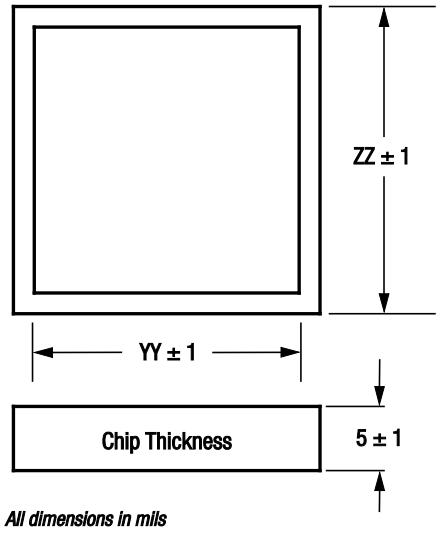


Figure 3. MIS Capacitor Chip Dimensions

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