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The document following this cover page is marked as “Cypress” document as this is the company that originally developed the product. Please note that Infineon will continue to offer the product to new and existing customers as part of the Infineon product portfolio.

Continuity of document content

The fact that Infineon offers the following product as part of the Infineon product portfolio does not lead to any changes to this document. Future revisions will occur when appropriate, and any changes will be set out on the document history page.

Continuity of ordering part numbers

Infineon continues to support existing part numbers. Please continue to use the ordering part numbers listed in the datasheet for ordering.

CY9B100A Series

32-bit Arm® Cortex®-M3 FM3 Microcontroller

The CY9B100A Series are a highly integrated 32-bit microcontroller that target for high-performance and cost-sensitive embedded control applications.
The CY9B100A Series are based on the Arm® Cortex®-M3 Processor and on-chip Flash memory and SRAM, and peripheral functions, including Motor Control Timers, ADCs and Communication Interfaces (UART, CSIO, I²C, LIN).

The products which are described in this data sheet are placed into TYPE0 product categories in “FM3 Family PERIPHERAL MANUAL”.

Features

32-bit Arm® Cortex®-M3 Core

- Processor version: r2p0
- Up to 80 MHz Frequency Operation
- Memory Protection Unit (MPU): improve the reliability of an embedded system
- Integrated Nested Vectored Interrupt Controller (NVIC): 1 NMI (non-maskable interrupt) and 48 peripheral interrupts and 16 priority levels
- 24-bit System timer (Sys Tick): System timer for OS task management

On-chip Memories

[Flash memory]

- Up to 512 Kbyte
- Read cycle: 0 wait-cycle @ up to 60 MHz, 2 wait-cycle* above
  *: Instruction pre-fetch buffer is included. So when CPU access continuously, it becomes 0wait-cycle
- Security function for code protection

[SRAM]

This series contain a total of up to 64 Kbyte on-chip SRAM. This is composed of two independent SRAM(SRAM0, SRAM1). SRAM0 is connected to I-code bus and D-code bus of Cortex-M3 core. SRAM1 is connected to System bus.

- SRAM0: Up to 32 Kbyte
- SRAM1: Up to 32 Kbyte

Multi-function Serial Interface (Max. 8 channels)

- 4 channels with 16 steps × 9bit FIFO (ch.4-ch.7), 4 channels without FIFO (ch.0-ch.3)
- Operation mode is selectable from the followings for each channel.
  - UART
  - CSIO
  - LIN
  - I²C

[UART]

- Full-duplex double buffer
- Selection with or without parity supported
- Built-in dedicated baud rate generator
- External clock available as a serial clock
- Hardware Flow control: Automatically control the transmission by CTS/RTS (only ch.4)
- Various error detect functions available (parity errors, framing errors, and overrun errors)

[CSIO]

- Full-duplex double buffer
- Built-in dedicated baud rate generator
- Overrun error detect function available

[LIN]

- LIN protocol Rev.2.1 supported
- Full-duplex double buffer
- Master/Slave mode supported
- LIN break field generate (can be changed 13-16bit length)
- LIN break delimiter generate (can be changed 1-4bit length)
- Various error detect functions available (parity errors, framing errors, and overrun errors)

[I²C]

- Standard-mode (Max.100 kbps) / Fast-mode (Max.400 kbps) supported

External Bus Interface

- Supports SRAM, NOR& NAND Flash device
- Up to 8 chip selects
- 8-/16-bit Data width
- Up to 25-bit Address bit
- Maximum area size : Up to 256 Mbytes

DMA Controller (8 channels)

DMA Controller has an independent bus for CPU, so CPU and DMA Controller can process simultaneously.

- 8 independently configured and operated channels
- Transfer can be started by software or request from the built-in peripherals
- Transfer address area: 32bit(4Gbyte)
- Transfer mode: Block transfer/Burst transfer/Demand transfer
- Transfer data type: byte/half-word/word
- Transfer block count: 1 to 16
- Number of transfers: 1 to 65536

A/D Converter (Max. 16 channels)

[12-bit A/D Converter]

- Successive Approximation Register type
- Built-in 3unit
- Conversion time: 1.0 µs@5 V
- Priority conversion available (priority at 2 levels)
- Scanning conversion mode
- Built-in FIFO for conversion data storage (for SCAN conversion: 16 steps, for Priority conversion: 4 steps)

Base Timer (Max. 8 channels)

Operation mode is selectable from the followings for each channel.

- 16-bit PWM timer
- 16-bit PPG timer
- 16-/32-bit reload timer
- 16-/32-bit PWC timer

Multi-function Timer (Max. 2 units)

The Multi-function timer is composed of the following blocks.

- 16-bit free-run timer × 3 ch/unit
- Input capture × 4 ch/unit
- Output compare × 6 ch/unit
- A/D activation compare × 3 ch/unit
- Waveform generator × 3 ch/unit
- 16-bit PPG timer × 3 ch/unit

The following function can be used to achieve the motor control.

- PWM signal output function
- DC chopper waveform output function
- Dead time function
- Input capture function
- A/D convertor activate function
- DTIF (Motor emergency stop) interrupt function

Quadrature Position/Revolution Counter (QPRC) (Max. 2 units)

The Quadrature Position/Revolution Counter (QPRC) is used to measure the position of the position encoder. Moreover, it is possible to use up/down counter.

- The detection edge of the three external event input pins AIN, BIN and ZIN is configurable.
- 16-bit position counter
- 16-bit revolution counter
- Two 16-bit compare registers

Dual Timer (Two 32-/16bit Down Counter)

The Dual Timer consists of two programmable 32-/16-bit down counters.
Operation mode is selectable from the followings for each channel.

- Free-running
- Periodic (=Reload)
- One-shot

Watch Counter

The Watch counter is used for wake up from sleep mode.

- Interval timer: up to 64 s (Max.)@ Sub Clock: 32.768 kHz

Watch dog Timer (2 channels)
A watchdog timer can generate interrupts or a reset when a time-out value is reached.

This series consists of two different watchdogs, a “Hardware” watchdog and a “Software” watchdog.

"Hardware" watchdog timer is clocked by the built-in low-speed CR oscillator. Therefore, ”Hardware" watchdog is active in any low-power consumption modes except STOP mode.

External Interrupt Controller Unit

- Up to 16 external vectors
- Include one non-maskable interrupt (NMI)

General Purpose I/O Port
This series can use its pins as general-purpose I/O ports when they are not used for external bus or peripherals. Moreover, the port relocate function is built in. It can set which I/O port the peripheral function can be allocated.

- Capable of pull-up control per pin
- Capable of reading pin level directly
- Built-in the port relocate function
- Up to 100 high-speed general-purpose I/O Ports@120pin Package

CRC (Cyclic Redundancy Check) Accelerator
The CRC accelerator helps a verify data transmission or storage integrity.

CCITT CRC16 and IEEE-802.3 CRC32 are supported.

- CCITT CRC16 Generator Polynomial: 0x1021
- IEEE-802.3 CRC32 Generator Polynomial: 0x04C11DB7

Clock and Reset

[Clocks]
Five clock sources (2 ext. osc, 2 CR osc, and Main PLL) that are dynamically selectable.

- Main Clock: 4 MHz to 48 MHz
- Sub Clock: 32.768 kHz
- Built-in high-speed CR Clock: 4 MHz
- Built-in low-speed CR Clock: 100 kHz
- Main PLL Clock

[Resets]
- Reset requests from INITX pins
- Power-on reset
- Software reset
- Watchdog timers reset
- Low-voltage detector reset
- Clock supervisor reset

Clock Super Visor (CSV)
Clocks generated by CR oscillators are used to supervise abnormality of the external clocks.

- External OSC clock failure (clock stop) is detected, reset is asserted.
- External OSC frequency anomaly is detected, interrupt or reset is asserted.

Low Voltage Detector (LVD)
This series include 2-stage monitoring of voltage on the VCC. When the voltage falls below the voltage has been set, Low Voltage Detector generates an interrupt or reset.

- LVD1: error reporting via interrupt
- LVD2: auto-reset operation

Low-Power Consumption Mode
Three low-power consumption modes supported.

- SLEEP
- TIMER
- STOP

Debug
- Serial Wire JTAG Debug Port (SWJ-DP)
- Embedded Trace Macrocells (ETM) provide comprehensive debug and trace facilities.

Power Supply
- VCC = 2.7 V to 5.5 V: Correspond to the wide range voltage.

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1. Product Lineup

Memory size

Product device	CY9BF102NA/RA	CY9BF104NA/RA	CY9BF105NA/RA	CY9BF106NA/RA
On-chip Flash memory	128 Kbyte	256 Kbyte	384 Kbyte	512 Kbyte
On-chip SRAM	16 Kbyte	32 Kbyte	48 Kbyte	64 Kbyte

Function

Product device			CY9BF102NA CY9BF104NA CY9BF105NA CY9BF106NA	CY9BF102RA CY9BF104RA CY9BF105RA CY9BF106RA
Pin count			100	120
CPU			Cortex-M3	
	Freq.		80 MHz	
Power supply voltage range			2.7 V to 5.5 V	
DMAC			8 ch	
External Bus Interface			Addr:25-bit (Max.) Data:8-/16-bit CS:5(Max.) Support: SRAM, NOR Flash	Addr:25-bit (Max.) Data:8-/16-bit CS:8(Max.) Support: SRAM, NOR & NAND Flash
Multi-function Serial Interface (UART/CSIO/LIN/I^{2}C)			8 ch (Max.)	
Base Timer (PWC/ Reload timer/PWM/PPG)			8 ch (Max.)	
MF-Timer	A/D activation compare	3ch.	2 units (Max.)	
	Input capture	4ch.		
	Free-run timer	3ch.		
	Output compare	6ch.		
	Waveform generator	3ch.		
	PPG	3ch.		
QPRC			2 ch (Max.)	
Dual Timer			1 unit	
Watch Counter			1 unit	
CRC Accelerator			Yes	
Watchdog timer			1 ch(SW) + 1ch(HW)	
External Interrupts			16 pins (Max.)+ NMI × 1	
I/O ports			80 pins (Max.)	100 pins (Max.)
12-bit A/D converter			16 ch (3 units)	
CSV (Clock Super Visor)			Yes	
LVD (Low Voltage Detector)			2 ch	
Built-in CR	High-speed		4 MHz	
	Low-speed		100 kHz	
Debug Function			SWJ-DP/ETM	

Note:

- *All signals of the peripheral function in each product cannot be allocated by limiting the pins of package. It is necessary to use the port relocate function of the General I/O port according to your function use. See "Electrical Characteristics 12.4 AC Characteristics (12.4.3) Built-in CR Oscillation Characteristics" for accuracy of built-in CR.*

2. Packages

Package \ Product name	CY9BF102NA CY9BF104NA CY9BF105NA CY9BF106NA	CY9BF102RA CY9BF104RA CY9BF105RA CY9BF106RA
LQFP: LQI100 (0.5 mm pitch)	❍	-
LQFP: LQM120 (0.5 mm pitch)	-	❍
BGA: LBC112 (0.8 mm pitch)	❍	-

❍: Supported

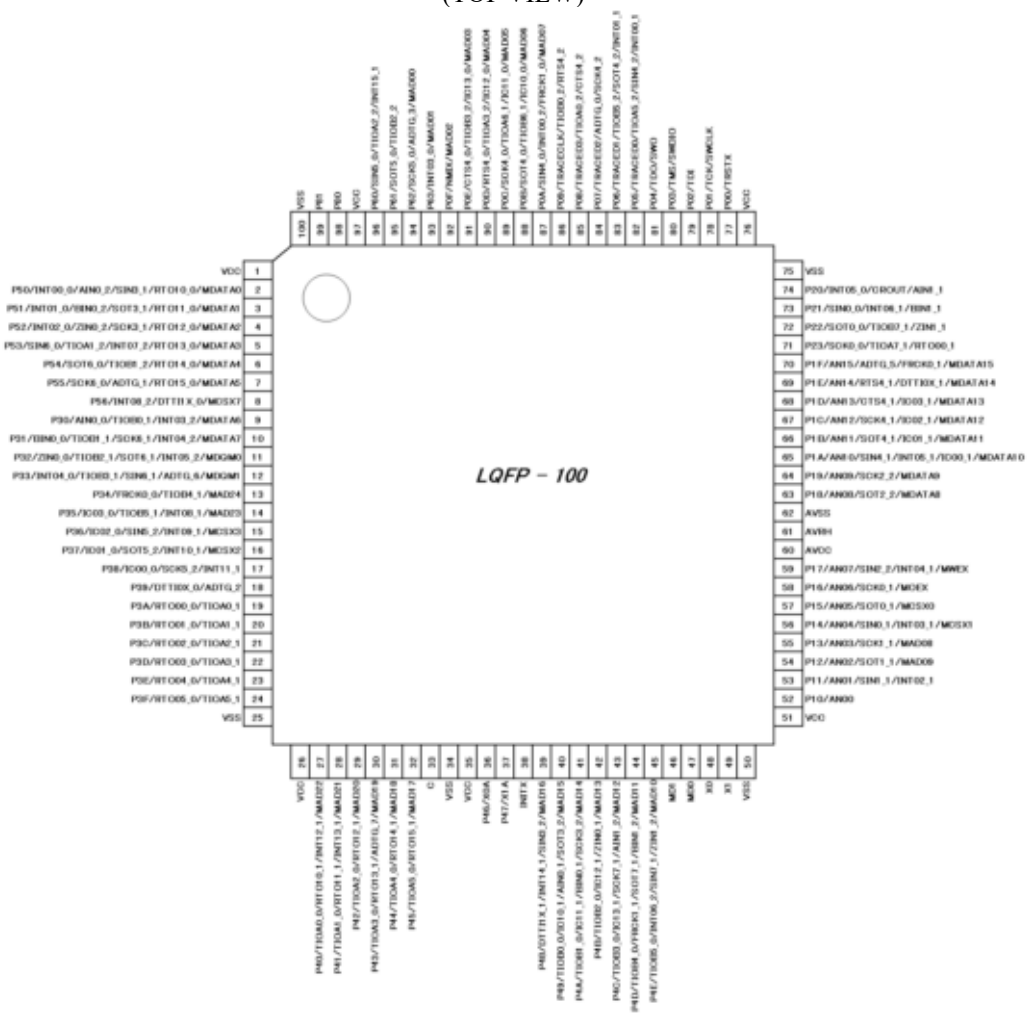
Note:

- *Refer to "Package Dimensions" for detailed information on each package.*

3. Pin Assignment

LQI100

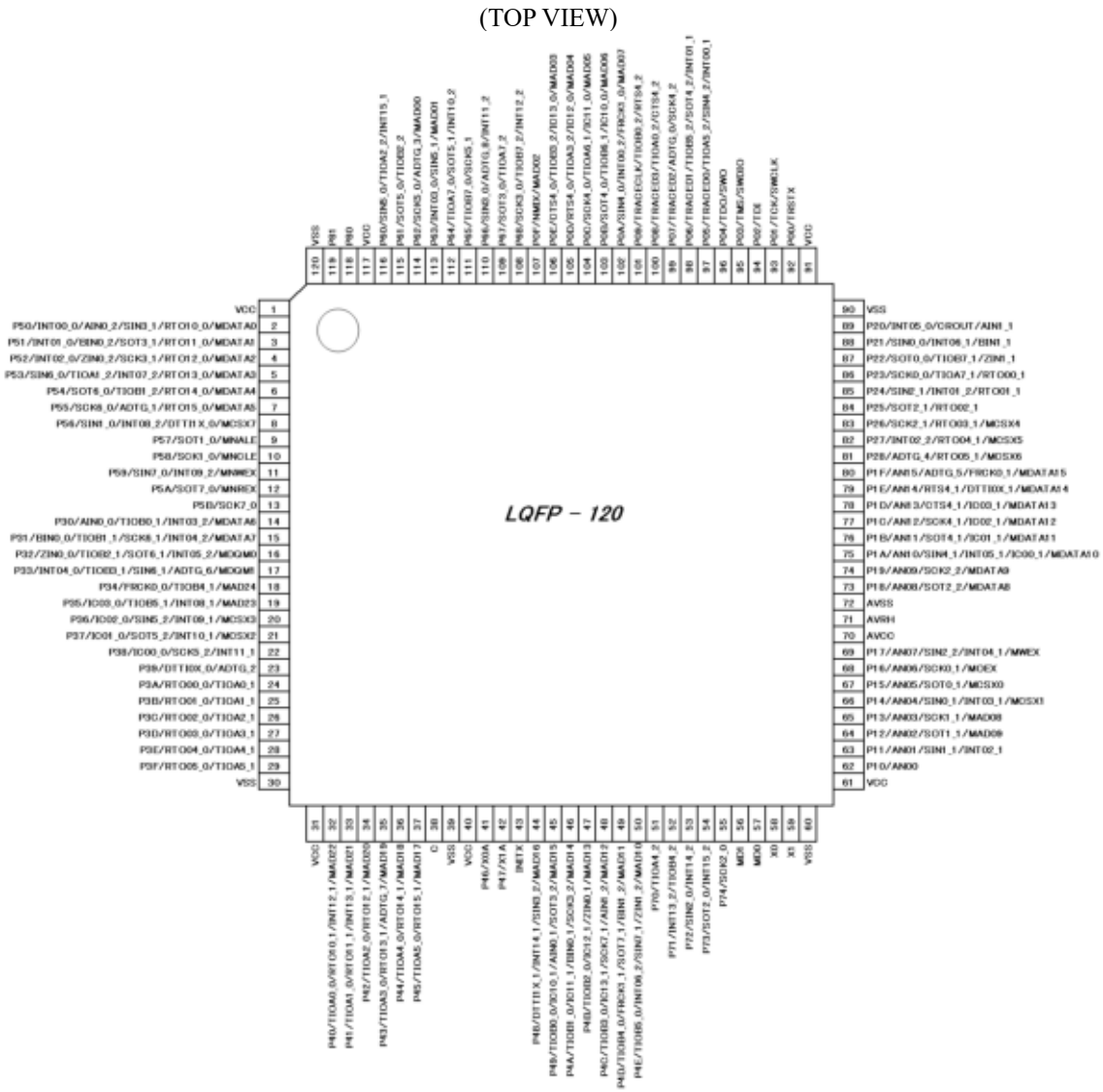
(TOP VIEW)



Note:

- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.*

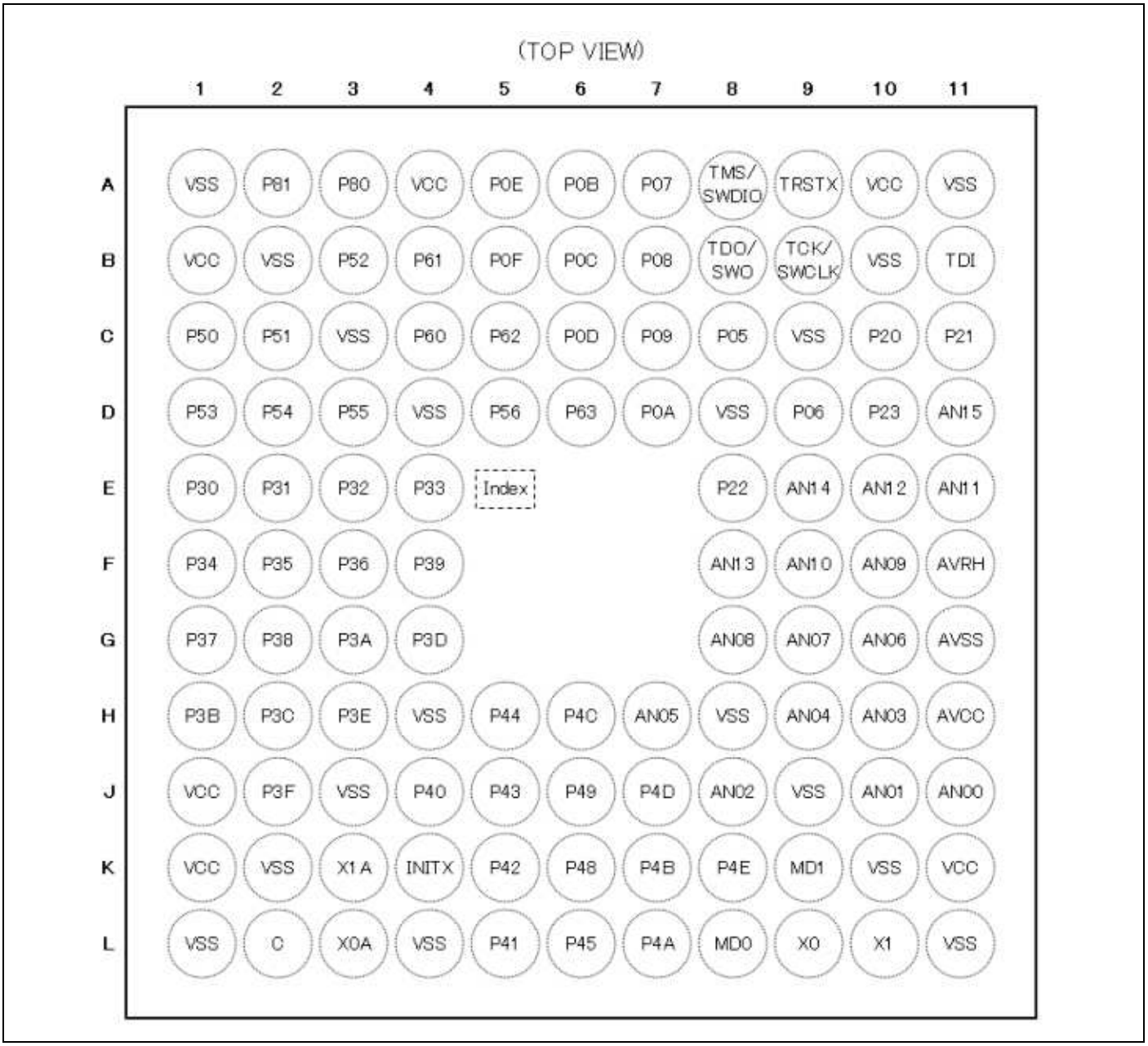
LQM120



Note:

- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.*

LBC112



Note:

- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.*

4. List of Pin Functions

List of pin numbers

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Pin No.			Pin name	I/O circuit type	Pin state type
LQFP-100	BGA-112	LQFP-120			
1	B1	1	VCC	-	
2	C1	2	P50 INT00_0 AIN0_2 SIN3_1 RTO10_0 (PPG10_0) MDATA0	E	H
3	C2	3	P51 INT01_0 BIN0_2 SOT3_1 (SDA3_1) RTO11_0 (PPG10_0) MDATA1	E	H
4	B3	4	P52 INT02_0 ZIN0_2 SCK3_1 (SCL3_1) RTO12_0 (PPG12_0) MDATA2	E	H
5	D1	5	P53 SIN6_0 TIOA1_2 INT07_2 RTO13_0 (PPG12_0) MDATA3	E	H
6	D2	6	P54 SOT6_0 (SDA6_0) TIOB1_2 RTO14_0 (PPG14_0) MDATA4	E	I

Pin No.			Pin name	I/O circuit type	Pin state type
LQFP-100	BGA-112	LQFP-120			
7	D3	7	P55 SCK6_0 (SCL6_0) ADTG_1 RTO15_0 (PPG14_0) MDATA5	E	I
8	D5	8	P56 SIN1_0 (120pin only) INT08_2 DTTI1X_0 MCSX7	E	H
-	-	9	P57 SOT1_0 (SDA1_0) MNALE	E	I
-	-	10	P58 SCK1_0 (SCL1_0) MNCLE	E	I
-	-	11	P59 SIN7_0 INT09_2 MNWEX	E	H
-	-	12	P5A SOT7_0 (SDA7_0) MNREX	E	I
-	-	13	P5B SCK7_0 (SCL7_0)	E	I
9	E1	14	P30 AIN0_0 TIOB0_1 INT03_2 MDATA6	E	H

Pin No.			Pin name	I/O circuit type	Pin state type
LQFP-100	BGA-112	LQFP-120			
10	E2	15	P31 BIN0_0 TIOB1_1 SCK6_1 (SCL6_1) INT04_2 MDATA7	E	H
11	E3	16	P32 ZIN0_0 TIOB2_1 SOT6_1 (SDA6_1) INT05_2 MDQM0	E	H
12	E4	17	P33 INT04_0 TIOB3_1 SIN6_1 ADTG_6 MDQM1	E	H
13	F1	18	P34 FRCK0_0 TIOB4_1 MAD24	E	I
14	F2	19	P35 IC03_0 TIOB5_1 INT08_1 MAD23	E	H
15	F3	20	P36 IC02_0 SIN5_2 INT09_1 MCSX3	E	H
16	G1	21	P37 IC01_0 SOT5_2 (SDA5_2) INT10_1 MCSX2	E	H
17	G2	22	P38 IC00_0 SCK5_2 (SCL5_2) INT11_1	E	H

Pin No.			Pin name	I/O circuit type	Pin state type
LQFP-100	BGA-112	LQFP-120			
18	F4	23	P39 DTTI0X_0 ADTG_2	E	I
19	G3	24	P3A RTO00_0 (PPG00_0) TIOA0_1	G	I
-	B2	-	VSS	-	
20	H1	25	P3B RTO01_0 (PPG00_0) TIOA1_1	G	I
21	H2	26	P3C RTO02_0 (PPG02_0) TIOA2_1	G	I
22	G4	27	P3D RTO03_0 (PPG02_0) TIOA3_1	G	I
23	H3	28	P3E RTO04_0 (PPG04_0) TIOA4_1	G	I
24	J2	29	P3F RTO05_0 (PPG04_0) TIOA5_1	G	I
25	L1	30	VSS	-	
26	J1	31	VCC	-	
27	J4	32	P40 TIOA0_0 RTO10_1 (PPG10_1) INT12_1 MAD22	G	H
28	L5	33	P41 TIOA1_0 RTO11_1 (PPG10_1) INT13_1 MAD21	G	H

Pin No.			Pin name	I/O circuit type	Pin state type
LQFP-100	BGA-112	LQFP-120			
29	K5	34	P42 TIOA2_0 RTO12_1 (PPG12_1) MAD20	G	I
30	J5	35	P43 TIOA3_0 RTO13_1 (PPG12_1) ADTG_7 MAD19	G	I
-	K2	-	VSS	-	
-	J3	-	VSS	-	
-	H4	-	VSS	-	
31	H5	36	P44 TIOA4_0 RTO14_1 (PPG14_1) MAD18	G	I
32	L6	37	P45 TIOA5_0 RTO15_1 (PPG14_1) MAD17	G	I
33	L2	38	C	-	
34	L4	39	VSS	-	
35	K1	40	VCC	-	
36	L3	41	P46 X0A	D	M
37	K3	42	P47 X1A	D	N
38	K4	43	INITX	B	C
39	K6	44	P48 DTTI1X_1 INT14_1 SIN3_2 MAD16	E	H
40	J6	45	P49 TIOB0_0 IC10_1 AIN0_1 SOT3_2 (SDA3_2) MAD15	E	I

Pin No.			Pin name	I/O circuit type	Pin state type
LQFP-100	BGA-112	LQFP-120			
41	L7	46	P4A TIOB1_0 IC11_1 BIN0_1 SCK3_2 (SCL3_2) MAD14	E	I
42	K7	47	P4B TIOB2_0 IC12_1 ZIN0_1 MAD13	E	I
43	H6	48	P4C TIOB3_0 IC13_1 SCK7_1 (SCL7_1) AIN1_2 MAD12	E	I
44	J7	49	P4D TIOB4_0 FRCK1_1 SOT7_1 (SDA7_1) BIN1_2 MAD11	E	I
45	K8	50	P4E TIOB5_0 INT06_2 SIN7_1 ZIN1_2 MAD10	E	H
-	-	51	P70 TIOA4_2	E	I
-	-	52	P71 INT13_2 TIOB4_2	E	H
-	-	53	P72 SIN2_0 INT14_2	E	H

Pin No.			Pin name	I/O circuit type	Pin state type
LQFP-100	BGA-112	LQFP-120			
-	-	54	P73 SOT2_0 (SDA2_0) INT15_2	E	H
-	-	55	P74 SCK2_0 (SCL2_0)	E	I
46	K9	56	MD1	C	D
47	L8	57	MD0	C	D
48	L9	58	X0	A	A
49	L10	59	X1	A	B
50	L11	60	VSS	-	
51	K11	61	VCC	-	
52	J11	62	P10 AN00	F	K
53	J10	63	P11 AN01 SIN1_1 INT02_1	F	L
-	K10	-	VSS	-	
-	J9	-	VSS	-	
54	J8	64	P12 AN02 SOT1_1 (SDA1_1) MAD09	F	K
55	H10	65	P13 AN03 SCK1_1 (SCL1_1) MAD08	F	K
56	H9	66	P14 AN04 SIN0_1 INT03_1 MCSX1	F	L
57	H7	67	P15 AN05 SOT0_1 (SDA0_1) MCSX0	F	K

Pin No.			Pin name	I/O circuit type	Pin state type
LQFP-100	BGA-112	LQFP-120			
58	G10	68	P16	F	K
			AN06		
			SCK0_1 (SCL0_1)		
			MOEX		
59	G9	69	P17	F	L
			AN07		
			SIN2_2		
			INT04_1		
			MWEX		
60	H11	70	AVCC	-	
61	F11	71	AVRH	-	
62	G11	72	AVSS	-	
63	G8	73	P18	F	K
			AN08		
			SOT2_2 (SDA2_2)		
			MDATA8		
64	F10	74	P19	F	K
			AN09		
			SCK2_2 (SCL2_2)		
			MDATA9		
65	F9	75	P1A	F	L
			AN10		
			SIN4_1		
			INT05_1		
			IC00_1		
			MDATA10		
-	H8	-	VSS	-	
66	E11	76	P1B	F	K
			AN11		
			SOT4_1 (SDA4_1)		
			IC01_1		
			MDATA11		
67	E10	77	P1C	F	K
			AN12		
			SCK4_1 (SCL4_1)		
			IC02_1		
			MDATA12		

Pin No.			Pin name	I/O circuit type	Pin state type
LQFP-100	BGA-112	LQFP-120			
68	F8	78	P1D AN13 CTS4_1 IC03_1 MDATA13	F	K
69	E9	79	P1E AN14 RTS4_1 DTTI0X_1 MDATA14	F	K
70	D11	80	P1F AN15 ADTG_5 FRCK0_1 MDATA15	F	K
-	-	81	P28 ADTG_4 RTO05_1 (PPG04_1) MCSX6	E	I
-	-	82	P27 INT02_2 RTO04_1 (PPG04_1) MCSX5	E	H
-	-	83	P26 SCK2_1 (SCL2_1) RTO03_1 (PPG02_1) MCSX4	E	I
-	-	84	P25 SOT2_1 (SDA2_1) RTO02_1 (PPG02_1)	E	I
-	B10	-	VSS	-	
-	C9	-	VSS	-	
-	-	85	P24 SIN2_1 INT01_2 RTO01_1 (PPG00_1)	E	H

Pin No.			Pin name	I/O circuit type	Pin state type
LQFP-100	BGA-112	LQFP-120			
71	D10	86	P23 SCK0_0 (SCL0_0) TIOA7_1 RTO00_1 (PPG00_1)	E	I
72	E8	87	P22 SOT0_0 (SDA0_0) TIOB7_1 ZIN1_1	E	I
73	C11	88	P21 SIN0_0 INT06_1 BIN1_1	E	H
74	C10	89	P20 INT05_0 CROUT AIN1_1	E	H
75	A11	90	VSS	-	
76	A10	91	VCC	-	
77	A9	92	P00 TRSTX	E	E
78	B9	93	P01 TCK SWCLK	E	E
79	B11	94	P02 TDI	E	E
80	A8	95	P03 TMS SWDIO	E	E
81	B8	96	P04 TDO SWO	E	E
82	C8	97	P05 TRACED0 TIOA5_2 SIN4_2 INT00_1	E	F
-	D8	-	VSS	-	

Pin No.			Pin name	I/O circuit type	Pin state type
LQFP-100	BGA-112	LQFP-120			
83	D9	98	P06 TRACED1 TIOB5_2 SOT4_2 (SDA4_2) INT01_1	E	F
84	A7	99	P07 TRACED2 ADTG_0 SCK4_2 (SCL4_2)	E	G
85	B7	100	P08 TRACED3 TIOA0_2 CTS4_2	E	G
86	C7	101	P09 TRACECLK TIOB0_2 RTS4_2	E	G
87	D7	102	P0A SIN4_0 INT00_2 FRCK1_0 MAD07	E	H
88	A6	103	P0B SOT4_0 (SDA4_0) TIOB6_1 IC10_0 MAD06	E	I
89	B6	104	P0C SCK4_0 (SCL4_0) TIOA6_1 IC11_0 MAD05	E	I
90	C6	105	P0D RTS4_0 TIOA3_2 IC12_0 MAD04	E	I

Pin No.			Pin name	I/O circuit type	Pin state type
LQFP-100	BGA-112	LQFP-120			
91	A5	106	P0E CTS4_0 TIOB3_2 IC13_0 MAD03	E	I
-	D4	-	VSS	-	
-	C3	-	VSS	-	
92	B5	107	P0F NMIX MAD02	E	J
-	-	108	P68 SCK3_0 (SCL3_0) TIOB7_2 INT12_2	E	H
-	-	109	P67 SOT3_0 (SDA3_0) TIOA7_2	E	I
-	-	110	P66 SIN3_0 ADTG_8 INT11_2	E	H
-	-	111	P65 TIOB7_0 SCK5_1 (SCL5_1)	E	I
-	-	112	P64 TIOA7_0 SOT5_1 (SDA5_1) INT10_2	E	H
93	D6	113	P63 INT03_0 MAD01	E	H
-	-		SIN5_1		
94	C5	114	P62 SCK5_0 (SCL5_0) ADTG_3 MAD00	E	I
95	B4	115	P61 SOT5_0 (SDA5_0) TIOB2_2	E	I

Pin No.			Pin name	I/O circuit type	Pin state type
LQFP-100	BGA-112	LQFP-120			
96	C4	116	P60	E	H
			SIN5_0		
			TIOA2_2		
			INT15_1		
97	A4	117	VCC	-	
98	A3	118	P80	H	O
99	A2	119	P81	H	O
100	A1	120	VSS	-	

List of pin functions

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Module	Pin Name	Function	Pin No.		
			LQFP-100	BGA-112	LQFP-120
ADC	ADTG_0	A/D converter external trigger input pin.	84	A7	99
	ADTG_1		7	D3	7
	ADTG_2		18	F4	23
	ADTG_3		94	C5	114
	ADTG_4		-	-	81
	ADTG_5		70	D11	80
	ADTG_6		12	E4	17
	ADTG_7		30	J5	35
	ADTG_8		-	-	110
	AN00	A/D converter analog input pin. ANxx describes ADC ch.xx.	52	J11	62
	AN01		53	J10	63
	AN02		54	J8	64
	AN03		55	H10	65
	AN04		56	H9	66
	AN05		57	H7	67
	AN06		58	G10	68
	AN07		59	G9	69
	AN08		63	G8	73
	AN09		64	F10	74
	AN10		65	F9	75
	AN11		66	E11	76
	AN12		67	E10	77
	AN13		68	F8	78
	AN14		69	E9	79
	AN15		70	D11	80
Base Timer 0	TIOA0_0	Base timer ch.0 TIOA pin.	27	J4	32
	TIOA0_1		19	G3	24
	TIOA0_2		85	B7	100
	TIOB0_0	Base timer ch.0 TIOB pin.	40	J6	45
	TIOB0_1		9	E1	14
	TIOB0_2		86	C7	101
Base Timer 1	TIOA1_0	Base timer ch.1 TIOA pin.	28	L5	33
	TIOA1_1		20	H1	25
	TIOA1_2		5	D1	5
	TIOB1_0	Base timer ch.1 TIOB pin.	41	L7	46
	TIOB1_1		10	E2	15
	TIOB1_2		6	D2	6
Base Timer 2	TIOA2_0	Base timer ch.2 TIOA pin.	29	K5	34
	TIOA2_1		21	H2	26
	TIOA2_2		96	C4	116
	TIOB2_0	Base timer ch.2 TIOB pin.	42	K7	47
	TIOB2_1		11	E3	16
	TIOB2_2		95	B4	115

Module	Pin Name	Function	Pin No.		
			LQFP-100	BGA-112	LQFP-120
Base Timer 3	TIOA3_0	Base timer ch.3 TIOA pin.	30	J5	35
	TIOA3_1		22	G4	27
	TIOA3_2		90	C6	105
	TIOB3_0	Base timer ch.3 TIOB pin.	43	H6	48
	TIOB3_1		12	E4	17
	TIOB3_2		91	A5	106
Base Timer 4	TIOA4_0	Base timer ch.4 TIOA pin.	31	H5	36
	TIOA4_1		23	H3	28
	TIOA4_2		-	-	51
	TIOB4_0	Base timer ch.4 TIOB pin.	44	J7	49
	TIOB4_1		13	F1	18
	TIOB4_2		-	-	52
Base Timer 5	TIOA5_0	Base timer ch.5 TIOA pin.	32	L6	37
	TIOA5_1		24	J2	29
	TIOA5_2		82	C8	97
	TIOB5_0	Base timer ch.5 TIOB pin.	45	K8	50
	TIOB5_1		14	F2	19
	TIOB5_2		83	D9	98
Base Timer 6	TIOA6_1	Base timer ch.6 TIOA pin.	89	B6	104
	TIOB6_1	Base timer ch.6 TIOB pin.	88	A6	103
Base Timer 7	TIOA7_0	Base timer ch.7 TIOA pin.	-	-	112
	TIOA7_1		71	D10	86
	TIOA7_2		-	-	109
	TIOB7_0	Base timer ch.7 TIOB pin.	-	-	111
	TIOB7_1		72	E8	87
	TIOB7_2		-	-	108

Module	Pin Name	Function	Pin No.		
			LQFP-100	BGA-112	LQFP-120
Debugger	SWCLK	Serial wire debug interface clock input.	78	B9	93
	SWDIO	Serial wire debug interface data input / output.	80	A8	95
	SWO	Serial wire viewer output.	81	B8	96
	TCK	JTAG test clock input.	78	B9	93
	TDI	JTAG test data input.	79	B11	94
	TDO	JTAG debug data output.	81	B8	96
	TMS	JTAG test mode state input/output.	80	A8	95
	TRACECLK	Trace CLK output of ETM.	86	C7	101
	TRACED0	Trace data output of ETM.	82	C8	97
	TRACED1		83	D9	98
	TRACED2		84	A7	99
	TRACED3		85	B7	100
	TRSTX	JTAG test reset Input.	77	A9	92
External Bus	MAD00	External bus interface address bus.	94	C5	114
	MAD01		93	D6	113
	MAD02		92	B5	107
	MAD03		91	A5	106
	MAD04		90	C6	105
	MAD05		89	B6	104
	MAD06		88	A6	103
	MAD07		87	D7	102
	MAD08		55	H10	65
	MAD09		54	J8	64
	MAD10		45	K8	50
	MAD11		44	J7	49
	MAD12		43	H6	48
	MAD13		42	K7	47
	MAD14		41	L7	46
	MAD15		40	J6	45
	MAD16		39	K6	44
	MAD17		32	L6	37
	MAD18		31	H5	36
	MAD19		30	J5	35
	MAD20		29	K5	34
	MAD21		28	L5	33
	MAD22		27	J4	32
	MAD23		14	F2	19
	MAD24		13	F1	18
	MCSX0	External bus interface chip select output pin.	57	H7	67
	MCSX1		56	H9	66
	MCSX2		16	G1	21
	MCSX3		15	F3	20
	MCSX4		-	-	83
	MCSX5		-	-	82
	MCSX6		-	-	81
	MCSX7		8	D5	8

Module	Pin Name	Function	Pin No.		
			LQFP-100	BGA-112	LQFP-120
External Bus	MDATA0	External bus interface data bus.	2	C1	2
	MDATA1		3	C2	3
	MDATA2		4	B3	4
	MDATA3		5	D1	5
	MDATA4		6	D2	6
	MDATA5		7	D3	7
	MDATA6		9	E1	14
	MDATA7		10	E2	15
	MDATA8		63	G8	73
	MDATA9		64	F10	74
	MDATA10		65	F9	75
	MDATA11		66	E11	76
	MDATA12		67	E10	77
	MDATA13		68	F8	78
	MDATA14		69	E9	79
	MDATA15		70	D11	80
	MDQM0	External bus interface byte mask signal output.	11	E3	16
	MDQM1		12	E4	17
	MNALE	External bus interface ALE signal to control NAND Flash output pin.	-	-	9
	MNCLE	External bus interface CLE signal to control NAND Flash output pin.	-	-	10
	MNREX	External bus interface read enable signal to control NAND Flash.	-	-	12
	MNWEX	External bus interface write enable signal to control NAND Flash.	-	-	11
	MOEX	External bus interface read enable signal for SRAM.	58	G10	68
	MWEX	External bus interface write enable signal for SRAM.	59	G9	69

Module	Pin Name	Function	Pin No.		
			LQFP-100	BGA-112	LQFP-120
External Interrupt	INT00_0	External interrupt request 00 input pin.	2	C1	2
	INT00_1		82	C8	97
	INT00_2		87	D7	102
	INT01_0	External interrupt request 01 input pin.	3	C2	3
	INT01_1		83	D9	98
	INT01_2		-	-	85
	INT02_0	External interrupt request 02 input pin.	4	B3	4
	INT02_1		53	J10	63
	INT02_2		-	-	82
	INT03_0	External interrupt request 03 input pin.	93	D6	113
	INT03_1		56	H9	66
	INT03_2		9	E1	14
	INT04_0	External interrupt request 04 input pin.	12	E4	17
	INT04_1		59	G9	69
	INT04_2		10	E2	15
	INT05_0	External interrupt request 05 input pin.	74	C10	89
	INT05_1		65	F9	75
	INT05_2		11	E3	16
	INT06_1	External interrupt request 06 input pin.	73	C11	88
	INT06_2		45	K8	50
	INT07_2	External interrupt request 07 input pin.	5	D1	5
	INT08_1	External interrupt request 08 input pin.	14	F2	19
	INT08_2		8	D5	8
	INT09_1	External interrupt request 09 input pin.	15	F3	20
	INT09_2		-	-	11
	INT10_1	External interrupt request 10 input pin.	16	G1	21
	INT10_2		-	-	112
	INT11_1	External interrupt request 11 input pin.	17	G2	22
	INT11_2		-	-	110
	INT12_1	External interrupt request 12 input pin.	27	J4	32
	INT12_2		-	-	108
	INT13_1	External interrupt request 13 input pin.	28	L5	33
	INT13_2		-	-	52
	INT14_1	External interrupt request 14 input pin.	39	K6	44
	INT14_2		-	-	53
	INT15_1	External interrupt request 15 input pin.	96	C4	116
	INT15_2		-	-	54
	NMIX	Non-Maskable Interrupt input.	92	B5	107

Module	Pin Name	Function	Pin No.		
			LQFP-100	BGA-112	LQFP-120
GPIO	P00	General-purpose I/O port 0.	77	A9	92
	P01		78	B9	93
	P02		79	B11	94
	P03		80	A8	95
	P04		81	B8	96
	P05		82	C8	97
	P06		83	D9	98
	P07		84	A7	99
	P08		85	B7	100
	P09		86	C7	101
	P0A		87	D7	102
	P0B		88	A6	103
	P0C		89	B6	104
	P0D		90	C6	105
	P0E		91	A5	106
	P0F		92	B5	107
	P10	General-purpose I/O port 1.	52	J11	62
	P11		53	J10	63
	P12		54	J8	64
	P13		55	H10	65
	P14		56	H9	66
	P15		57	H7	67
	P16		58	G10	68
	P17		59	G9	69
	P18		63	G8	73
	P19		64	F10	74
	P1A		65	F9	75
	P1B		66	E11	76
	P1C		67	E10	77
	P1D		68	F8	78
	P1E		69	E9	79
	P1F		70	D11	80
	P20	General-purpose I/O port 2.	74	C10	89
	P21		73	C11	88
	P22		72	E8	87
	P23		71	D10	86
	P24		-	-	85
	P25		-	-	84
	P26		-	-	83
	P27		-	-	82
	P28		-	-	81

Module	Pin Name	Function	Pin No.		
			LQFP-100	BGA-112	LQFP-120
GPIO	P30	General-purpose I/O port 3.	9	E1	14
	P31		10	E2	15
	P32		11	E3	16
	P33		12	E4	17
	P34		13	F1	18
	P35		14	F2	19
	P36		15	F3	20
	P37		16	G1	21
	P38		17	G2	22
	P39		18	F4	23
	P3A		19	G3	24
	P3B		20	H1	25
	P3C		21	H2	26
	P3D		22	G4	27
	P3E		23	H3	28
	P3F		24	J2	29
	P40	General-purpose I/O port 4.	27	J4	32
	P41		28	L5	33
	P42		29	K5	34
	P43		30	J5	35
	P44		31	H5	36
	P45		32	L6	37
	P46		36	L3	41
	P47		37	K3	42
	P48		39	K6	44
	P49		40	J6	45
	P4A		41	L7	46
	P4B		42	K7	47
	P4C		43	H6	48
	P4D		44	J7	49
	P4E		45	K8	50
	P50	General-purpose I/O port 5.	2	C1	2
	P51		3	C2	3
	P52		4	B3	4
	P53		5	D1	5
	P54		6	D2	6
	P55		7	D3	7
	P56		8	D5	8
	P57		-	-	9
	P58		-	-	10
	P59		-	-	11
	P5A		-	-	12
	P5B		-	-	13

Module	Pin Name	Function	Pin No.		
			LQFP-100	BGA-112	LQFP-120
GPIO	P60	General-purpose I/O port 6.	96	C4	116
	P61		95	B4	115
	P62		94	C5	114
	P63		93	D6	113
	P64		-	-	112
	P65		-	-	111
	P66		-	-	110
	P67		-	-	109
	P68		-	-	108
	P70	General-purpose I/O port 7.	-	-	51
	P71		-	-	52
	P72		-	-	53
	P73		-	-	54
	P74		-	-	55
	P80	General-purpose I/O port 8.	98	A3	118
	P81		99	A2	119
Multi Function Serial 0	SIN0_0	Multifunction serial interface ch.0 input pin.	73	C11	88
	SIN0_1		56	H9	66
	SOT0_0 (SDA0_0)	Multifunction serial interface ch.0 output pin. This pin operates as SOT0 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA0 when it is used in an I^2C (operation mode 4).	72	E8	87
	SOT0_1 (SDA0_1)		57	H7	67
	SCK0_0 (SCL0_0)	Multifunction serial interface ch.0 clock I/O pin. This pin operates as SCK0 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL0 when it is used in an I^2C (operation mode 4).	71	D10	86
	SCK0_1 (SCL0_1)		58	G10	68
Multi Function Serial 1	SIN1_0	Multifunction serial interface ch.1 input pin.	-	-	8
	SIN1_1		53	J10	63
	SOT1_0 (SDA1_0)	Multifunction serial interface ch.1 output pin. This pin operates as SOT1 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA1 when it is used in an I^2C (operation mode 4).	-	-	9
	SOT1_1 (SDA1_1)		54	J8	64
	SCK1_0 (SCL1_0)	Multifunction serial interface ch.1 clock I/O pin. This pin operates as SCK1 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL1 when it is used in an I^2C (operation mode 4).	-	-	10
	SCK1_1 (SCL1_1)		55	H10	65

Module	Pin Name	Function	Pin No.		
			LQFP-100	BGA-112	LQFP-120
Multi Function Serial 2	SIN2_0	Multifunction serial interface ch.2 input pin.	-	-	53
	SIN2_1		-	-	85
	SIN2_2		59	G9	69
	SOT2_0 (SDA2_0)	Multifunction serial interface ch.2 output pin. This pin operates as SOT2 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA2 when it is used in an I^2C (operation mode 4).	-	-	54
	SOT2_1 (SDA2_1)		-	-	84
	SOT2_2 (SDA2_2)		63	G8	73
	SCK2_0 (SCL2_0)	Multifunction serial interface ch.2 clock I/O pin. This pin operates as SCK2 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL2 when it is used in an I^2C (operation mode 4).	-	-	55
	SCK2_1 (SCL2_1)		-	-	83
	SCK2_2 (SCL2_2)		64	F10	74
Multi Function Serial 3	SIN3_0	Multifunction serial interface ch.3 input pin.	-	-	110
	SIN3_1		2	C1	2
	SIN3_2		39	K6	44
	SOT3_0 (SDA3_0)	Multifunction serial interface ch.3 output pin. This pin operates as SOT3 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA3 when it is used in an I^2C (operation mode 4).	-	-	109
	SOT3_1 (SDA3_1)		3	C2	3
	SOT3_2 (SDA3_2)		40	J6	45
	SCK3_0 (SCL3_0)	Multifunction serial interface ch.3 clock I/O pin. This pin operates as SCK3 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL3 when it is used in an I^2C (operation mode 4).	-	-	108
	SCK3_1 (SCL3_1)		4	B3	4
	SCK3_2 (SCL3_2)		41	L7	46

Module	Pin Name	Function	Pin No.		
			LQFP-100	BGA-112	LQFP-120
Multi Function Serial 4	SIN4_0	Multifunction serial interface ch.4 input pin.	87	D7	102
	SIN4_1		65	F9	75
	SIN4_2		82	C8	97
	SOT4_0 (SDA4_0)	Multifunction serial interface ch.4 output pin. This pin operates as SOT4 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA4 when it is used in an I^2C (operation mode 4).	88	A6	103
	SOT4_1 (SDA4_1)		66	E11	76
	SOT4_2 (SDA4_2)		83	D9	98
	SCK4_0 (SCL4_0)	Multifunction serial interface ch.4 clock I/O pin. This pin operates as SCK4 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL4 when it is used in an I^2C (operation mode 4).	89	B6	104
	SCK4_1 (SCL4_1)		67	E10	77
	SCK4_2 (SCL4_2)		84	A7	99
	RTS4_0	Multifunction serial interface ch.4 RTS output pin.	90	C6	105
	RTS4_1		69	E9	79
	RTS4_2		86	C7	101
	CTS4_0	Multifunction serial interface ch.4 CTS input pin.	91	A5	106
	CTS4_1		68	F8	78
	CTS4_2		85	B7	100
Multi Function Serial 5	SIN5_0	Multifunction serial interface ch.5 input pin.	96	C4	116
	SIN5_1		-	-	113
	SIN5_2		15	F3	20
	SOT5_0 (SDA5_0)	Multifunction serial interface ch.5 output pin. This pin operates as SOT5 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA5 when it is used in an I^2C (operation mode 4).	95	B4	115
	SOT5_1 (SDA5_1)		-	-	112
	SOT5_2 (SDA5_2)		16	G1	21
	SCK5_0 (SCL5_0)	Multifunction serial interface ch.5 clock I/O pin. This pin operates as SCK5 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL5 when it is used in an I^2C (operation mode 4).	94	C5	114
	SCK5_1 (SCL5_1)		-	-	111
	SCK5_2 (SCL5_2)		17	G2	22

Module	Pin Name	Function	Pin No.		
			LQFP-100	BGA-112	LQFP-120
Multi Function Serial 6	SIN6_0	Multifunction serial interface ch.6 input pin.	5	D1	5
	SIN6_1		12	E4	17
	SOT6_0 (SDA6_0)	Multifunction serial interface ch.6 output pin. This pin operates as SOT6 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA6 when it is used in an I^2C (operation mode 4).	6	D2	6
	SOT6_1 (SDA6_1)		11	E3	16
	SCK6_0 (SCL6_0)	Multifunction serial interface ch.6 clock I/O pin. This pin operates as SCK6 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL6 when it is used in an I^2C (operation mode 4).	7	D3	7
	SCK6_1 (SCL6_1)		10	E2	15
Multi Function Serial 7	SIN7_0	Multifunction serial interface ch.7 input pin.	-	-	11
	SIN7_1		45	K8	50
	SOT7_0 (SDA7_0)	Multifunction serial interface ch.7 output pin. This pin operates as SOT7 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA7 when it is used in an I^2C (operation mode 4).	-	-	12
	SOT7_1 (SDA7_1)		44	J7	49
	SCK7_0 (SCL7_0)	Multifunction serial interface ch.7 clock I/O pin. This pin operates as SCK7 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL7 when it is used in an I^2C (operation mode 4).	-	-	13
	SCK7_1 (SCL7_1)		43	H6	48

Module	Pin Name	Function	Pin No.		
			LQFP-100	BGA-112	LQFP-120
Multi Function Timer 0	DTTI0X_0	Input signal controlling wave form generator outputs RTO00 to RTO05 of multi-function timer 0.	18	F4	23
	DTTI0X_1		69	E9	79
	FRCK0_0	16-bit free-run timer ch.0 external clock input pin.	13	F1	18
	FRCK0_1		70	D11	80
	IC00_0	16-bit input capture ch.0 input pin of multi-function timer 0. ICxx describes channel number.	17	G2	22
	IC00_1		65	F9	75
	IC01_0		16	G1	21
	IC01_1		66	E11	76
	IC02_0		15	F3	20
	IC02_1		67	E10	77
	IC03_0		14	F2	19
	IC03_1		68	F8	78
	RTO00_0 (PPG00_0)	Wave form generator output of multi-function timer 0. This pin operates as PPG00 when it is used in PPG 0 output modes.	19	G3	24
	RTO00_1 (PPG00_1)		71	D10	86
	RTO01_0 (PPG00_0)	Wave form generator output of multi-function timer 0. This pin operates as PPG00 when it is used in PPG 0 output modes.	20	H1	25
	RTO01_1 (PPG00_1)		-	-	85
	RTO02_0 (PPG02_0)	Wave form generator output of multi-function timer 0. This pin operates as PPG02 when it is used in PPG 0 output modes.	21	H2	26
	RTO02_1 (PPG02_1)		-	-	84
	RTO03_0 (PPG02_0)	Wave form generator output of multi-function timer 0. This pin operates as PPG02 when it is used in PPG 0 output modes.	22	G4	27
	RTO03_1 (PPG02_1)		-	-	83
	RTO04_0 (PPG04_0)	Wave form generator output of multi-function timer 0. This pin operates as PPG04 when it is used in PPG 0 output modes.	23	H3	28
	RTO04_1 (PPG04_1)		-	-	82
	RTO05_0 (PPG04_0)	Wave form generator output of multi-function timer 0. This pin operates as PPG04 when it is used in PPG 0 output modes.	24	J2	29
	RTO05_1 (PPG04_1)		-	-	81

Module	Pin Name	Function	Pin No.		
			LQFP-100	BGA-112	LQFP-120
Multi Function Timer 1	DTTI1X_0	Input signal controlling wave form generator outputs RTO10 to RTO15 of multi-function timer 1.	8	D5	8
	DTTI1X_1		39	K6	44
	FRCK1_0	16-bit free-run timer ch.1 external clock input pin.	87	D7	102
	FRCK1_1		44	J7	49
	IC10_0	16-bit input capture ch.0 input pin of multi-function timer 1. ICxx describes channel number.	88	A6	103
	IC10_1		40	J6	45
	IC11_0		89	B6	104
	IC11_1		41	L7	46
	IC12_0		90	C6	105
	IC12_1		42	K7	47
	IC13_0		91	A5	106
	IC13_1		43	H6	48
	RTO10_0 (PPG10_0)	Wave form generator output of multi-function timer 1. This pin operates as PPG10 when it is used in PPG 1 output modes.	2	C1	2
	RTO10_1 (PPG10_1)		27	J4	32
	RTO11_0 (PPG10_0)	Wave form generator output of multi-function timer 1. This pin operates as PPG10 when it is used in PPG 1 output modes.	3	C2	3
	RTO11_1 (PPG10_1)		28	L5	33
	RTO12_0 (PPG12_0)	Wave form generator output of multi-function timer 1. This pin operates as PPG12 when it is used in PPG 1 output modes.	4	B3	4
	RTO12_1 (PPG12_1)		29	K5	34
	RTO13_0 (PPG12_0)	Wave form generator output of multi-function timer 1. This pin operates as PPG12 when it is used in PPG 1 output modes.	5	D1	5
	RTO13_1 (PPG12_1)		30	J5	35
	RTO14_0 (PPG14_0)	Wave form generator output of multi-function timer 1. This pin operates as PPG14 when it is used in PPG 1 output modes.	6	D2	6
	RTO14_1 (PPG14_1)		31	H5	36
	RTO15_0 (PPG14_0)	Wave form generator output of multi-function timer 1. This pin operates as PPG14 when it is used in PPG 1 output modes.	7	D3	7
	RTO15_1 (PPG14_1)		32	L6	37

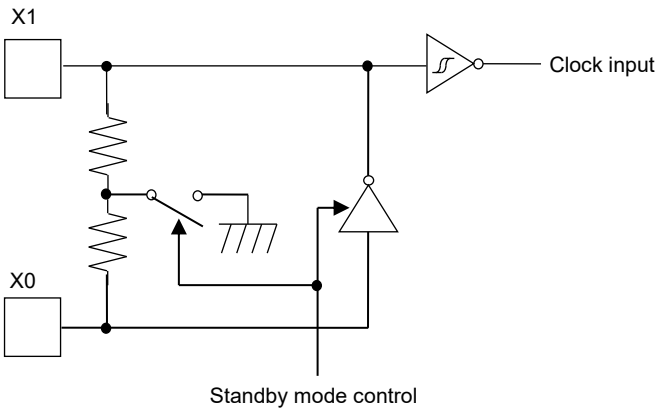
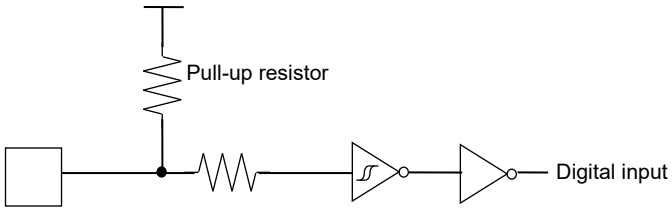
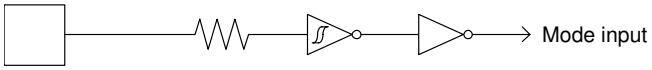
Module	Pin Name	Function	Pin No.		
			LQFP-100	BGA-112	LQFP-120
Quadrature Position/ Revolution Counter 0	AIN0_0	QPRC ch.0 AIN input pin.	9	E1	14
	AIN0_1		40	J6	45
	AIN0_2		2	C1	2
	BIN0_0	QPRC ch.0 BIN input pin.	10	E2	15
	BIN0_1		41	L7	46
	BIN0_2		3	C2	3
	ZIN0_0	QPRC ch.0 ZIN input pin.	11	E3	16
	ZIN0_1		42	K7	47
	ZIN0_2		4	B3	4
Quadrature Position/ Revolution Counter 1	AIN1_1	QPRC ch.1 AIN input pin.	74	C10	89
	AIN1_2		43	H6	48
	BIN1_1	QPRC ch.1 BIN input pin.	73	C11	88
	BIN1_2		44	J7	49
	ZIN1_1	QPRC ch.1 ZIN input pin.	72	E8	87
	ZIN1_2		45	K8	50

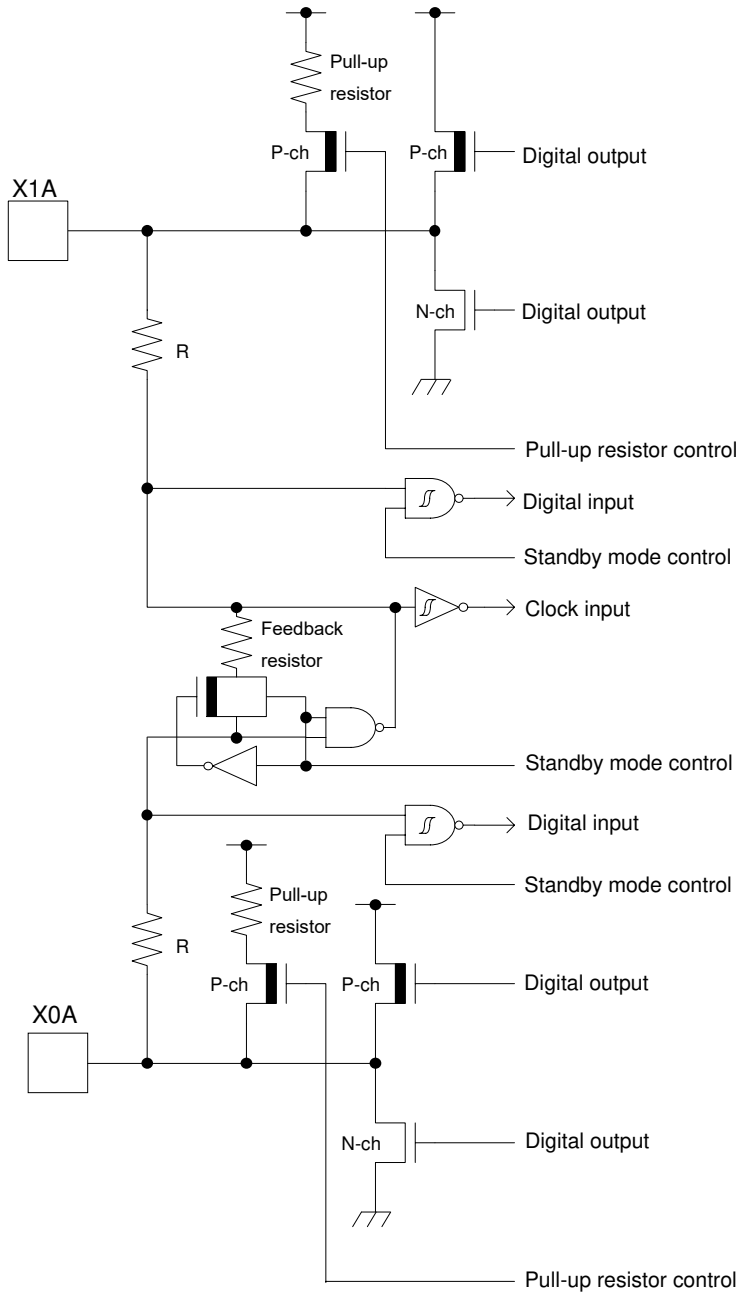
Module	Pin Name	Function	Pin No.		
			LQFP-100	BGA-112	LQFP-120
Reset	INITX	External Reset Input. A reset is valid when INITX=L.	38	K4	43
Mode	MD0	Mode 0 pin. During normal operation, MD0=L must be input. During serial programming to flash memory, MD0=H must be input.	47	L8	57
	MD1	Mode 1 pin. Input must always be at the "L" level.	46	K9	56
Power	VCC	Power Pin.	1	B1	1
	VCC		26	J1	31
	VCC		35	K1	40
	VCC		51	K11	61
	VCC		76	A10	91
	VCC		97	A4	117
GND	VSS	GND Pin.	-	B2	-
	VSS		25	L1	30
	VSS		-	K2	-
	VSS		-	J3	-
	VSS		-	H4	-
	VSS		34	L4	39
	VSS		50	L11	60
	VSS		-	K10	-
	VSS		-	J9	-
	VSS		-	H8	-
	VSS		-	B10	-
	VSS		-	C9	-
	VSS		75	A11	90
	VSS		-	D8	-
	VSS		-	D4	-
	VSS		-	C3	-
	VSS		100	A1	120
Clock	X0	Main clock (oscillation) input pin.	48	L9	58
	X0A	Sub clock (oscillation) input pin.	36	L3	41
	X1	Main clock (oscillation) I/O pin.	49	L10	59
	X1A	Sub clock (oscillation) I/O pin.	37	K3	42
	CROUT	Built-in High-speed CR-osc clock output port.	74	C10	89
Analog Power	AVCC	A/D converter analog power pin.	60	H11	70
	AVRH	A/D converter analog reference voltage input pin.	61	F11	71
Analog GND	AVSS	A/D converter GND pin.	62	G11	72
C-pin	C	Power stabilization capacity pin.	33	L2	38

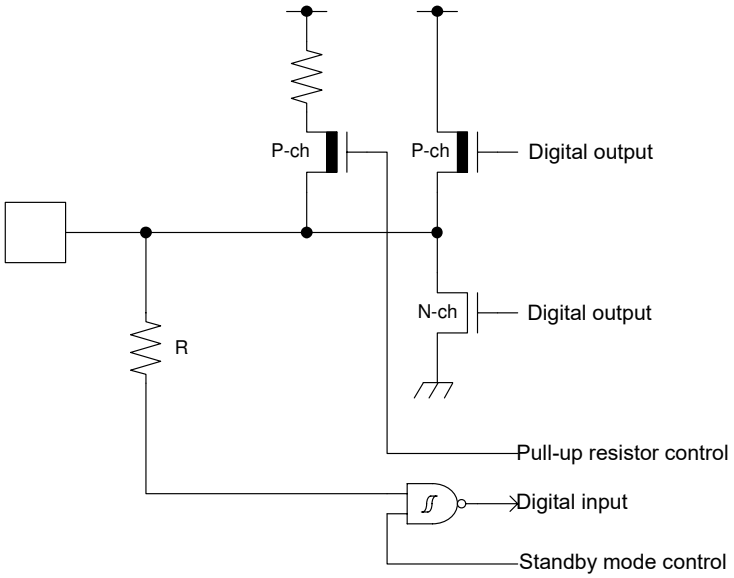
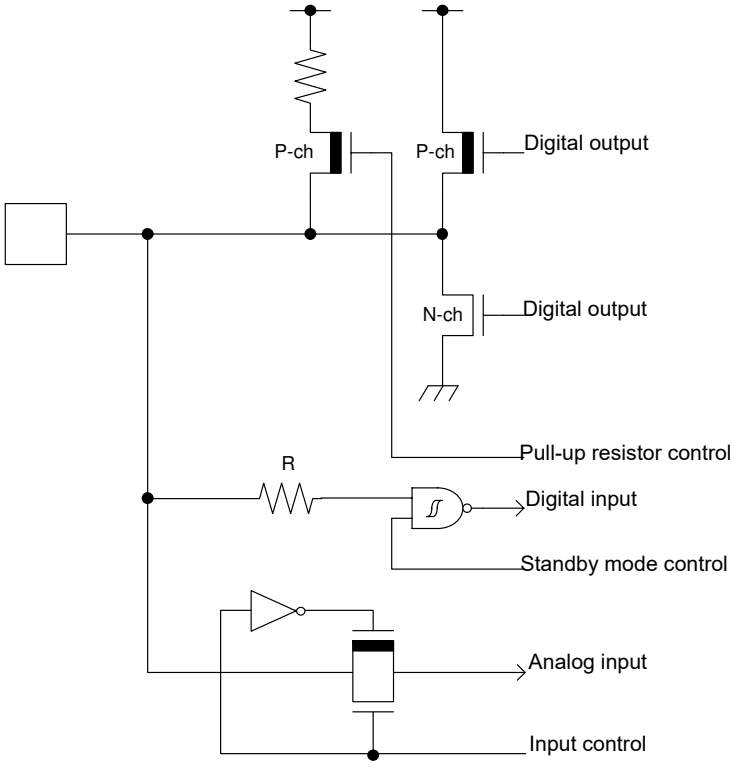
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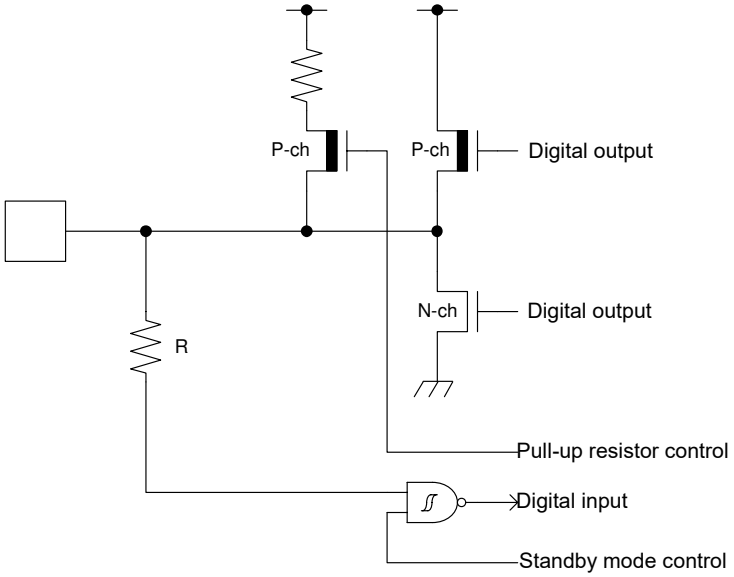
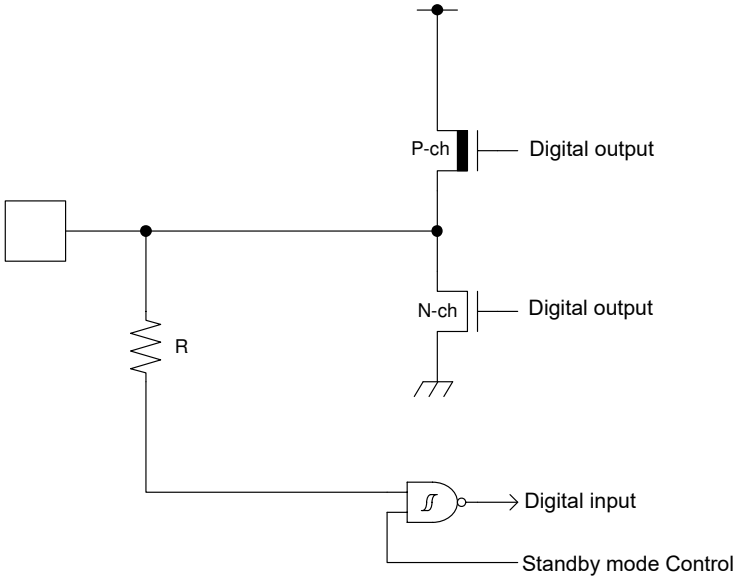
- *While this device contains a Test Access Port (TAP) based on the IEEE 1149.1-2001 JTAG standard, it is not fully compliant to all requirements of that standard. This device may contain a 32-bit device ID that is the same as the 32-bit device ID in other devices with different functionality. The TAP pins may also be configurable for purposes other than access to the TAP controller.*

5. I/O Circuit Type

Type	Circuit	Remarks
A		• Oscillation feedback resistor : Approximately 1 MΩ • With Standby mode control
B		• CMOS level hysteresis input • pull-up resistor : Approximately 50 kΩ
C		• CMOS level hysteresis input

Type	Circuit	Remarks
D		• It is possible to select the sub oscillation / GPIO function When the sub oscillation is selected. • Oscillation feedback resistor : Approximately 20 MΩ • With Standby mode control When the GPIO is selected. • CMOS level output. • CMOS level hysteresis input • With pull-up resistor control • With standby mode control • pull-up resistor : Approximately 50 kΩ • I_{OH} = -4 mA, I_{OL} = 4 mA

Type	Circuit	Remarks
E		• CMOS level output • CMOS level hysteresis input • With pull-up resistor control • With standby mode control • pull-up resistor : Approximately 50 kΩ • I_{OH} = -4 mA, I_{OL} = 4 mA • When this pin is used as an I^2C pin, the digital output P-ch transistor is always off • +B input is available
F		• CMOS level output • CMOS level hysteresis input • With input control • Analog input • With pull-up resistor control • With standby mode control • pull-up resistor : Approximately 50 kΩ • I_{OH} = -4 mA, I_{OL} = 4 mA • When this pin is used as an I^2C pin, the digital output P-ch transistor is always off • +B input is available

Type	Circuit	Remarks
G		• CMOS level output • CMOS level hysteresis input • With pull-up resistor control • With standby mode control • pull-up resistor : Approximately 50 kΩ • I_{OH} = -12 mA, I_{OL} = 12 mA • +B input is available
H		• CMOS level output • CMOS level hysteresis input • With standby mode control • I_{OH} = -25.3 mA, I_{OL} = 19.7 mA

6. Handling Precautions

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your Cypress semiconductor devices.

6.1 Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

Recommended Operating Conditions

Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

Processing and Protection of Pins

These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

1. Preventing Over-Voltage and Over-Current Conditions

   Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.
2. Protection of Output Pins

   Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device.
   Therefore, avoid this type of connection.
3. Handling of Unused Input Pins

   Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

Latch-up

Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNPN junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

1. Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.
2. Be sure that abnormal current flows do not occur during the power-on sequence.

Observance of Safety Regulations and Standards

Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

Fail-Safe Design

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

Precautions Related to Usage of Devices

Cypress semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

6.2 Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Cypress' recommended conditions. For detailed information about mount conditions, contact your sales representative.

Lead Insertion Type

Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Cypress recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

Surface Mount Type

Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. Cypress recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Cypress ranking of recommended conditions.

Lead-Free Packaging

CAUTION: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

Storage of Semiconductor Devices

Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

1. Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product. Store products in locations where temperature changes are slight.
2. Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5°C and 30°C.
   When you open Dry Package that recommends humidity 40% to 70% relative humidity.
3. When necessary, Cypress packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.
4. Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

Baking

Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Cypress recommended conditions for baking.

Condition: 125°C/24 h

Static Electricity

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

1. Maintain relative humidity in the working environment between 40% and 70%. Use of an apparatus for ion generation may be needed to remove electricity.
2. Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.
3. Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ).
   Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.
4. Ground all fixtures and instruments, or protect with anti-static measures.
5. Avoid the use of styrofoam or other highly static-prone materials for storage of completed board assemblies.

6.3 Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

1. Humidity

   Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.
2. Discharge of Static Electricity

   When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.
3. Corrosive Gases, Dust, or Oil

   Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.
4. Radiation, Including Cosmic Radiation

   Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.
5. Smoke, Flame

   CAUTION: Plastic molded devices are flammable, and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of Cypress products in other special environmental conditions should consult with sales representatives.

7. Handling Devices

Power supply pins

In products with multiple VCC and VSS pins, respective pins at the same potential are interconnected within the device in order to prevent malfunctions such as latch-up. However, all of these pins should be connected externally to the power supply or ground lines in order to reduce electromagnetic emission levels, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating.

Moreover, connect the current supply source with each Power supply pin and GND pin of this device at low impedance. It is also advisable that a ceramic capacitor of approximately 0.1 µF be connected as a bypass capacitor between each Power supply pin and GND pin, between AVCC pin and AVSS pin near this device.

Stabilizing power supply voltage

A malfunction may occur when the power supply voltage fluctuates rapidly even though the fluctuation is within the recommended operating conditions of the VCC power supply voltage. As a rule, with voltage stabilization, suppress the voltage fluctuation so that the fluctuation in VCC ripple (peak-to-peak value) at the commercial frequency (50 Hz/60 Hz) does not exceed 10% of the VCC value in the recommended operating conditions, and the transient fluctuation rate does not exceed 0.1 V/µs when there is a momentary fluctuation on switching the power supply.

Crystal oscillator circuit

Noise near the X0/X1 and X0A/X1A pins may cause the device to malfunction. Design the printed circuit board so that X0/X1, X0A/X1A pins, the crystal oscillator (or ceramic oscillator), and the bypass capacitor to ground are located as close to the device as possible.

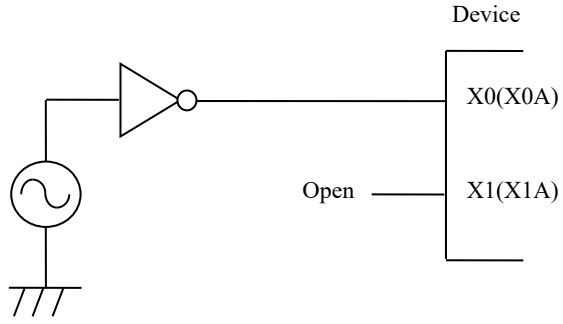
It is strongly recommended that the PC board artwork be designed such that the X0/X1 and X0A/X1A pins are surrounded by ground plane as this is expected to produce stable operation.

Evaluate oscillation of your using crystal oscillator by your mount board.

Using an external clock

When using an external clock, the clock signal should be input to the X0,X0A pin only and the X1,X1A pin should be kept open.

▪ **Example of Using an External Clock**

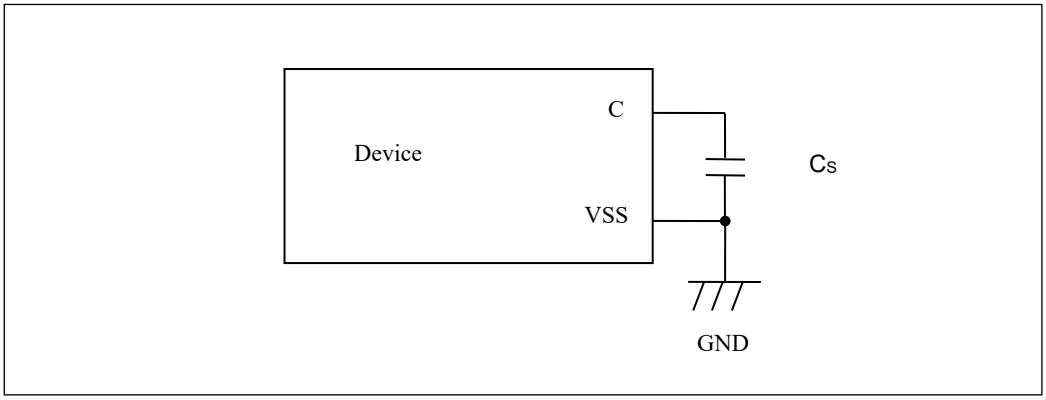


Handling when using Multi function serial pin as I²C pin

If it is using multi function serial pin as I²C pins, P-ch transistor of digital output is always disable. However, I²C pins need to keep the electrical characteristic like other pins and not to connect to external I²C bus system with power OFF.

C Pin

This series contains the regulator. Be sure to connect a smoothing capacitor (C_S) for the regulator between the C pin and the GND pin. Please use a ceramic capacitor or a capacitor of equivalent frequency characteristics as a smoothing capacitor.
However, some laminated ceramic capacitors have the characteristics of capacitance variation due to thermal fluctuation (F characteristics and Y5V characteristics). Please select the capacitor that meets the specifications in the operating conditions to use by evaluating the temperature characteristics of a capacitor.
A smoothing capacitor of about 4.7µF would be recommended for this series.



Mode pins (MD0, MD1)

Connect the MD pin (MD0, MD1) directly to VCC or VSS pins. Design the printed circuit board such that the pull-up/down resistance stays low, as well as the distance between the mode pins and VCC pins or VSS pins is as short as possible and the connection impedance is low, when the pins are pulled-up/down such as for switching the pin level and rewriting the Flash memory data. It is because of preventing the device erroneously switching to test mode due to noise.

Notes on power-on

Turn power on/off in the following order or at the same time.
If not using the A/D converter, connect AVCC =VCC and AVSS = VSS.

Turning on : VCC → AVCC → AVRH

Turning off : AVRH → AVCC → VCC

Serial Communication

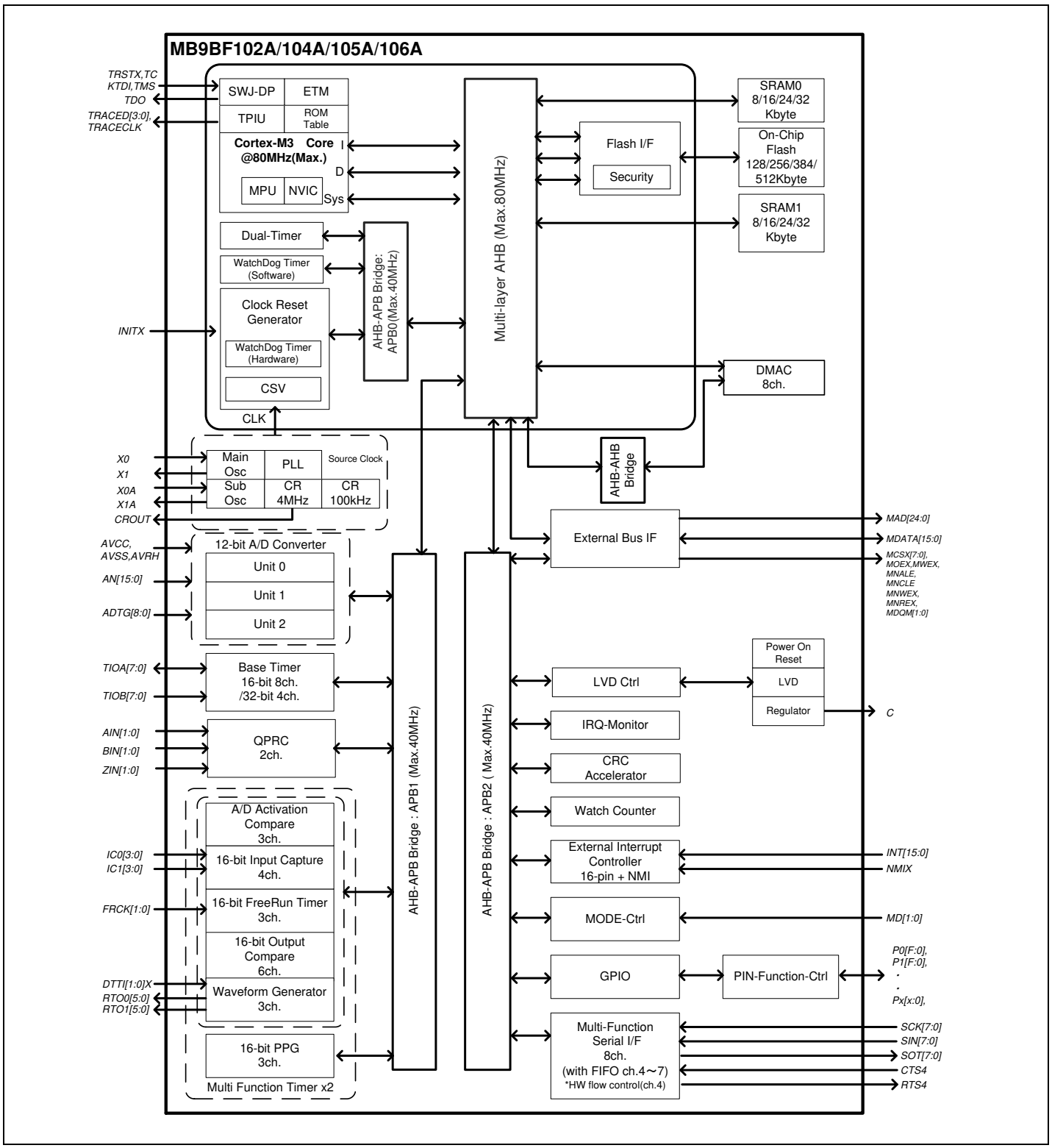
There is a possibility to receive wrong data due to the noise or other causes on the serial communication.
Therefore, design a printed circuit board so as to avoid noise.
Consider the case of receiving wrong data due to noise, perform error detection such as by applying a checksum of data at the end. If an error is detected, retransmit the data.

Differences in features among the products with different memory sizes and between FLASH products and MASK products

The electric characteristics including power consumption, ESD, latch-up, noise characteristics, and oscillation characteristics among the products with different memory sizes and between FLASH products and MASK products are different because chip layout and memory structures are different.

If you are switching to use a different product of the same series, please make sure to evaluate the electric characteristics.

8. Block Diagram

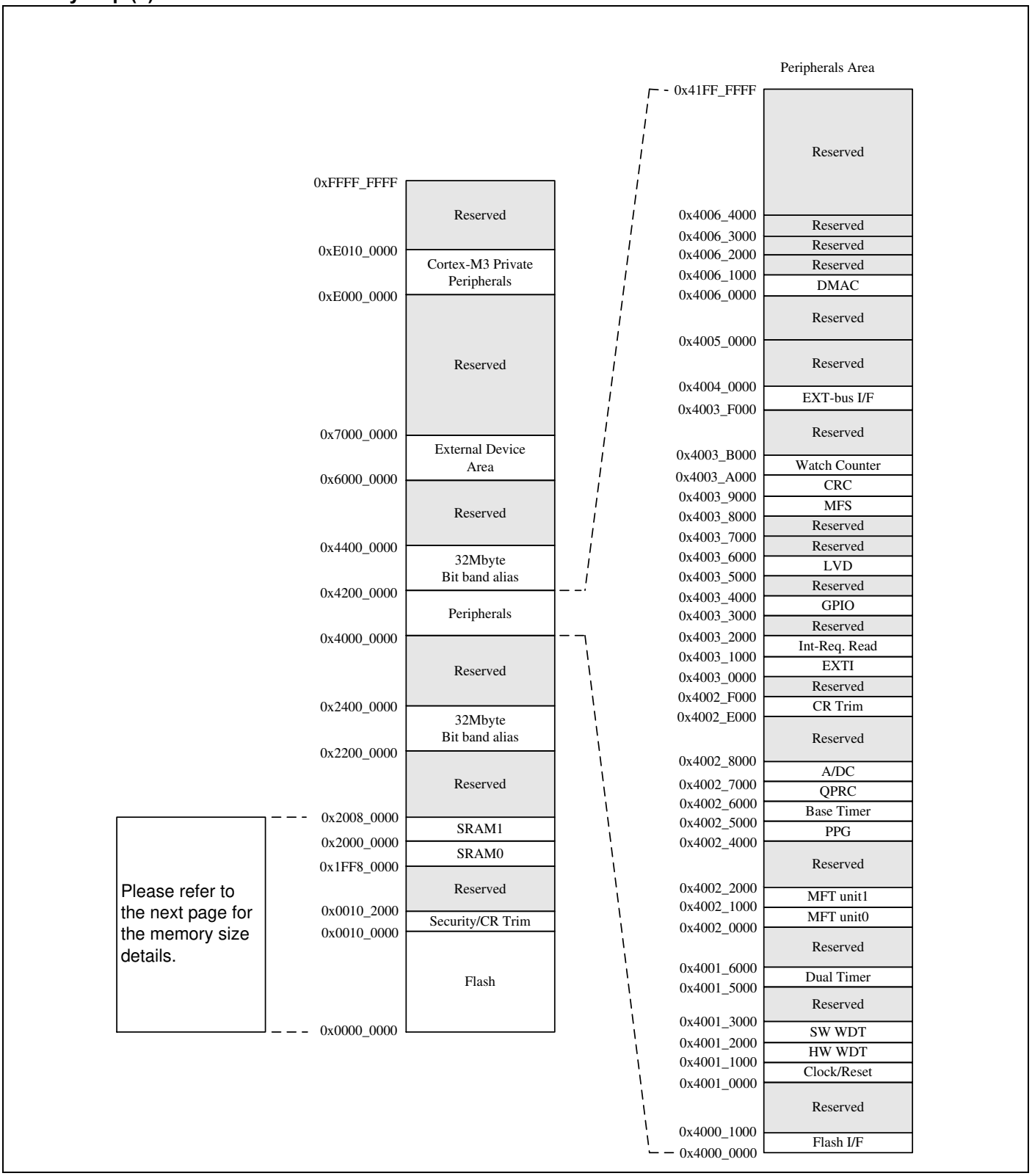


9. Memory Size

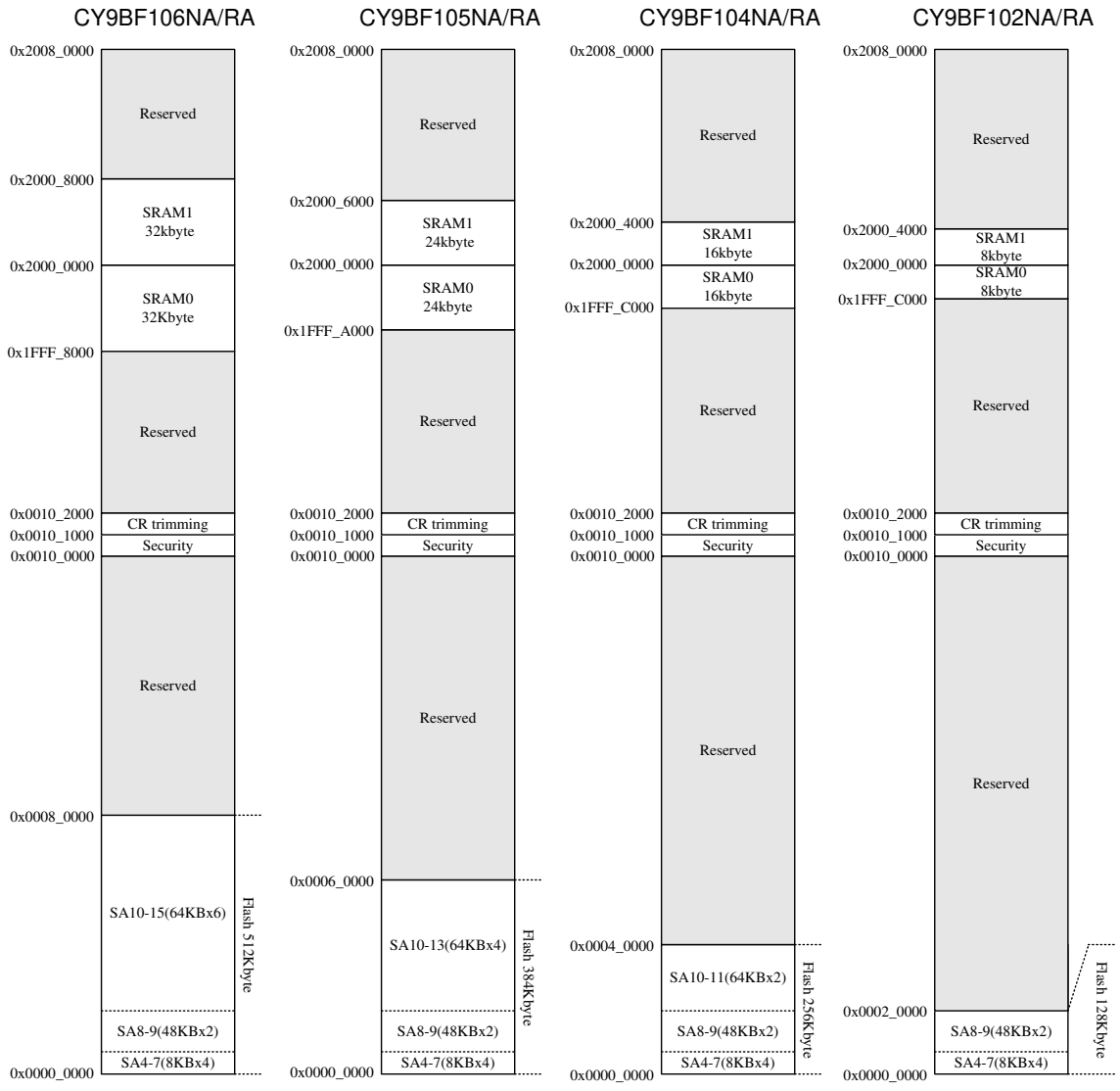
See "Memory size" in "PRODUCT LINEUP" to confirm the memory size.

10. Memory Map

Memory Map (1)



Memory Map (2)



*: See "CY9B500/400/300/100/CY9A100 Series Flash programming Manual" for sector structure of Flash.

Peripheral Address Map

Start address	End address	Bus	Peripherals
0x4000_0000	0x4000_0FFF	AHB	Flash Memory I/F register
0x4000_1000	0x4000_FFFF		Reserved
0x4001_0000	0x4001_0FFF	APB0	Clock/Reset Control
0x4001_1000	0x4001_1FFF		Hardware Watchdog timer
0x4001_2000	0x4001_2FFF		Software Watchdog timer
0x4001_3000	0x4001_4FFF		Reserved
0x4001_5000	0x4001_5FFF		Dual-Timer
0x4001_6000	0x4001_FFFF		Reserved
0x4002_0000	0x4002_0FFF	APB1	Multi-function timer unit0
0x4002_1000	0x4002_1FFF		Multi-function timer unit1
0x4002_2000	0x4002_3FFF		Reserved
0x4002_4000	0x4002_4FFF		PPG
0x4002_5000	0x4002_5FFF		Base Timer
0x4002_6000	0x4002_6FFF		Quadrature Position/Revolution Counter
0x4002_7000	0x4002_7FFF		A/D Converter
0x4002_8000	0x4002_DFFF		Reserved
0x4002_E000	0x4002_EFFF		Internal CR trimming
0x4002_F000	0x4002_FFFF		Reserved
0x4003_0000	0x4003_0FFF	APB2	External Interrupt Controller
0x4003_1000	0x4003_1FFF		Interrupt Request Batch-Read Function
0x4003_2000	0x4003_2FFF		Reserved
0x4003_3000	0x4003_3FFF		GPIO
0x4003_4000	0x4003_4FFF		Reserved
0x4003_5000	0x4003_5FFF		Low Voltage Detector
0x4003_6000	0x4003_6FFF		Reserved
0x4003_7000	0x4003_7FFF		Reserved
0x4003_8000	0x4003_8FFF		Multi-function serial Interface
0x4003_9000	0x4003_9FFF		CRC
0x4003_A000	0x4003_AFFF		Watch Counter
0x4003_B000	0x4003_EFFF		Reserved
0x4003_F000	0x4003_FFFF		External Memory interface
0x4004_0000	0x4004_FFFF	AHB	Reserved
0x4005_0000	0x4005_FFFF		Reserved
0x4006_0000	0x4006_0FFF		DMAC register
0x4006_1000	0x4006_1FFF		Reserved
0x4006_2000	0x4006_2FFF		Reserved
0x4006_3000	0x4006_3FFF		Reserved
0x4006_4000	0x41FF_FFFF		Reserved

11. Pin Status in Each CPU State

The terms used for pin status have the following meanings.

■INITX=0

This is the period when the INITX pin is the "L" level.

■INITX=1

This is the period when the INITX pin is the "H" level.

■SPL=0

This is the status that standby pin level setting bit (SPL) in standby mode control register (STB_CTL) is set to "0".

■SPL=1

This is the status that standby pin level setting bit (SPL) in standby mode control register (STB_CTL) is set to "1".

■Input enabled

Indicates that the input function can be used.

■Internal input fixed at "0"

This is the status that the input function cannot be used. Internal input is fixed at "L".

■Hi-Z

Indicates that the output drive transistor is disabled and the pin is put in the Hi-Z state.

■Setting disabled

Indicates that the setting is disabled.

■Maintain previous state

Maintains the state that was immediately prior to entering the current mode.
If a built-in peripheral function is operating, the output follows the peripheral function.
If the pin is being used as a port, that output is maintained.

■Analog input is enabled

Indicates that the analog input is enabled.

■Trace output

Indicates that the trace function can be used.

List of Pin Status

Pin status type	Function group	Power-on reset or low voltage detection state	INITX input state	Device internal reset state	Run mode or sleep mode state	Timer mode or sleep mode state	
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable	
		-	INITX=0	INITX=1	INITX=1	INITX=1	
		-	-	-	-	SPL=0	SPL=1
A	Main crystal oscillator input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
B	Main crystal oscillator output pin	H output/ Internal input fixed at "0"/ or Input enabled	H output/ Internal input fixed at "0"	H output/ Internal input fixed at "0"	Maintain previous state/ H output at oscillation stop (*1)/ Internal input fixed at "0"	Maintain previous state/ H output at oscillation stop (*1)/ Internal input fixed at "0"	Maintain previous state/ H output at oscillation stop (*1)/ Internal input fixed at "0"
C	INITX input pin	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled
D	Mode input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
E	JTAG selected	Hi-Z	Pull-up/ Input enabled	Pull-up/ Input enabled	Maintain previous state	Maintain previous state	Maintain previous state
	GPIO selected	Setting disabled	Setting disabled	Setting disabled			Hi-Z/ Internal input fixed at "0"
F	Trace selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Trace output
	External interrupt enabled selected						Maintain previous state
	GPIO selected, or other than above resource selected	Hi-Z	Hi-Z/ Input enabled	Hi-Z/ Input enabled			Hi-Z/ Internal input fixed at "0"

Pin status type	Function group	Power-on reset or low voltage detection state	INITX input state	Device internal reset state	Run mode or sleep mode state	Timer mode or sleep mode state	
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable	
		-	INITX=0	INITX=1	INITX=1	INITX=1	
		-	-	-	-	SPL=0	SPL=1
G	Trace selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Trace output
	GPIO selected, or other than above resource selected	Hi-Z	Hi-Z/ Input enabled	Hi-Z/ Input enabled			Hi-Z/ Internal input fixed at "0"
H	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state
	GPIO selected, or other than above resource selected	Hi-Z	Hi-Z/ Input enabled	Hi-Z/ Input enabled			Hi-Z/ Internal input fixed at "0"
I	GPIO selected, resource selected	Hi-Z	Hi-Z/ Input enabled	Hi-Z/ Input enabled	Maintain previous state	Maintain previous state	Hi-Z/ Internal input fixed at "0"
J	NMIX selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state
	GPIO selected, or other than above resource selected	Hi-Z	Hi-Z/ Input enabled	Hi-Z/ Input enabled			Hi-Z/ Internal input fixed at "0"

Pin status type	Function group	Power-on reset or low voltage detection state	INITX input state	Device internal reset state	Run mode or sleep mode state	Timer mode or sleep mode state	
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable	
		-	INITX=0	INITX=1	INITX=1	INITX=1	
		-	-	-	-	SPL=0	SPL=1
K	Analog input selected	Hi-Z	Hi-Z/ Internal input fixed at "0"/ Analog input enabled	Hi-Z/ Internal input fixed at "0"/ Analog input enabled	Hi-Z/ Internal input fixed at "0"/ Analog input enabled	Hi-Z/ Internal input fixed at "0"/ Analog input enabled	Hi-Z/ Internal input fixed at "0"/ Analog input enabled
	GPIO selected, or other than above resource selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/ Internal input fixed at "0"
L	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state
	Analog input selected	Hi-Z	Hi-Z/ Internal input fixed at "0"/ Analog input enabled	Hi-Z/ Internal input fixed at "0"/ Analog input enabled	Hi-Z/ Internal input fixed at "0"/ Analog input enabled	Hi-Z/ Internal input fixed at "0"/ Analog input enabled	Hi-Z/ Internal input fixed at "0"/ Analog input enabled
	GPIO selected, or other than above resource selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/ Internal input fixed at "0"
M	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/ Internal input fixed at "0"
	Sub crystal oscillator input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled

Pin status type	Function group	Power-on reset or low voltage detection state	INITX input state	Device internal reset state	Run mode or sleep mode state	Timer mode or sleep mode state	
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable	
		-	INITX=0	INITX=1	INITX=1	INITX=1	
		-	-	-	-	SPL=0	SPL=1
N	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/ Internal input fixed at "0"
	Sub crystal oscillator output pin	Hi-Z/ Internal input fixed at "0"	Hi-Z/ Internal input fixed at "0"	Hi-Z/ Internal input fixed at "0"	Maintain previous state	Maintain previous state/ Hi-Z at oscillation stop (*2)/ Internal input fixed at "0"	Maintain previous state/ Hi-Z at oscillation stop (*2)/ Internal input fixed at "0"
O	GPIO selected	Hi-Z	Hi-Z/ Input enabled	Hi-Z/ Input enabled	Maintain previous state	Maintain previous state	Hi-Z/ Internal input fixed at "0"

*1: Oscillation is stopped at sub timer mode, Low speed CR timer mode, and stop mode.

*2: Oscillation is stopped at stop mode.

12. Electrical Characteristics

12.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1,*2	Vcc	Vss - 0.5	Vss + 6.5	V	
Analog power supply voltage*1,*3	AVcc	Vss - 0.5	Vss + 6.5	V	
Analog reference voltage*1,*3	AVRH	Vss - 0.5	Vss + 6.5	V	
Input voltage*1	V_I	Vss - 0.5	Vcc + 0.5 (≤ 6.5 V)	V	
Analog pin input voltage*1	V_{IA}	Vss - 0.5	AVcc + 0.5 (≤ 6.5 V)	V	
Output voltage*1	V_O	Vss - 0.5	Vcc + 0.5 (≤ 6.5 V)	V	
Clamp maximum current	I_{CLAMP}	-2	+2	mA	*7
Clamp total maximum current	$\Sigma [I_{CLAMP}]$		+20	mA	*7
"L" level maximum output current*4	I_{OL}	-	10	mA	4mA type
			20	mA	12mA type
			39	mA	P80, P81
"L" level average output current*5	I_{OLAV}	-	4	mA	4mA type
			12	mA	12mA type
			19.7	mA	P80, P81
"L" level total maximum output current	$\sum I_{OL}$	-	100	mA	
"L" level total average output current*6	$\sum I_{OLAV}$	-	50	mA	
"H" level maximum output current*4	I_{OH}	-	- 10	mA	4mA type
			- 20	mA	12mA type
			- 39	mA	P80, P81
"H" level average output current*5	I_{OHAV}	-	- 4	mA	4mA type
			- 12	mA	12mA type
			- 25.3	mA	P80, P81
"H" level total maximum output current	$\sum I_{OH}$	-	- 100	mA	
"H" level total average output current*6	$\sum I_{OHAV}$	-	- 50	mA	
Power consumption	P_D	-	800	mW	
Storage temperature	T_{STG}	- 55	+ 150	°C	

*1: These parameters are based on the condition that Vss = AVss = 0.0 V.

*2: Vcc must not drop below Vss - 0.5 V.

*3: Be careful not to exceed Vcc + 0.5 V, for example, when the power is turned on.

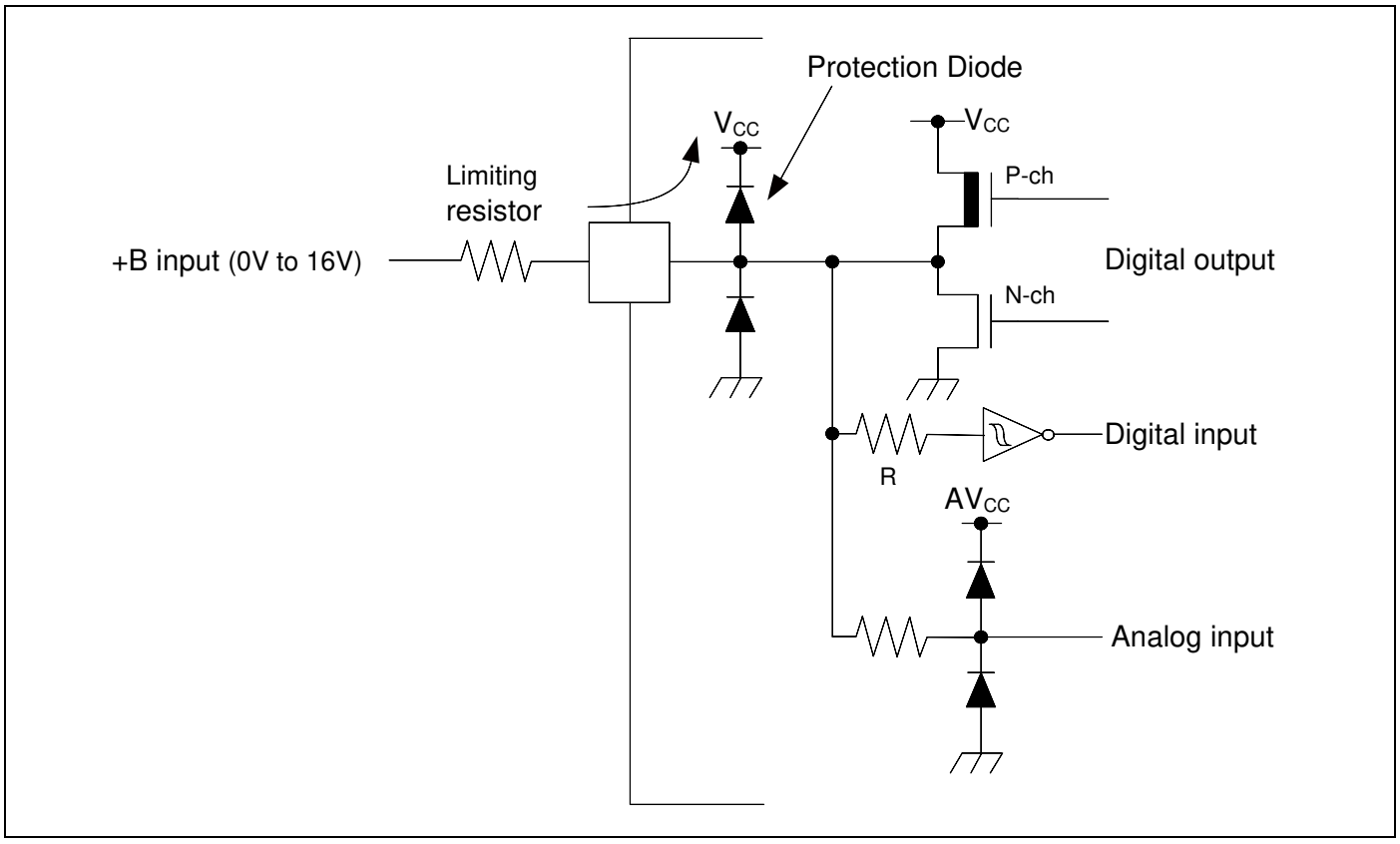
*4: The maximum output current is the peak value for a single pin.

*5: The average output is the average current for a single pin over a period of 100 ms.

*6: The total average output current is the average current for all pins over a period of 100 ms.

*7:

- See "List of Pin Functions" and "I/O Circuit Type" about +B input available pin.
- Use within recommended operating conditions.
- Use at DC voltage (current) the +B input.
- The +B signal should always be applied a limiting resistance placed between the +B signal and the device.
- The value of the limiting resistance should be set so that when the +B signal is applied the input current to the device pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the device drive current is low, such as in the low-power consumption modes, the +B input potential may pass through the protective diode and increase the potential at the VCC and AVCC pin, and this may affect other devices.
- Note that if a +B signal is input when the device power supply is off (not fixed at 0 V), the power supply is provided from the pins, so that incomplete operation may result.
- The following is a recommended circuit example (I/O equivalent circuit).



WARNING:

– *Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.*

12.2 Recommended Operating Conditions

(Vss = AVss = 0.0V)

Parameter		Symbol	Conditions	Value		Unit	Remarks
				Min	Max		
Power supply voltage		Vcc	-	2.7*2	5.5	V	
Analog power supply voltage		AVcc	-	2.7	5.5	V	AVcc = Vcc
Analog reference voltage		AVRH	-	2.7	AVcc	V	
Smoothing capacitor		C_S	-	1	10	µF	For built-in regulator*1
Operating Temperature	LQM120 LQI100 LBC112	T_A	When mounted on four-layer PCB	- 40	+ 85	°C	
			When mounted on double-sided single-layer PCB	- 40	+ 85	°C	Icc ≤ 100 mA
				- 40	+ 70	°C	Icc > 100 mA

*1: See "C Pin" in "HANDLING DEVICES" for the connection of the smoothing capacitor.

*2: In between less than the minimum power supply voltage and low voltage reset/interrupt detection voltage or more, instruction execution and low voltage detection function by built-in High-speed CR(including Main PLL is used) or built-in Low-speed CR is possible to operate only.

WARNING:

– *The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.*
Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure. No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

12.3 DC Characteristics

12.3.1 Current rating

(Vcc = AVcc =2.7V to 5.5V, Vss = AVss = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions		Value		Unit	Remarks
					Typ*3	Max*4		
RUN mode current	Icc	VCC	PLL RUN mode	CPU: 80 MHz, Peripheral: 40 MHz, FLASH 2 Wait FRWTR.RWT = 10 FSYNDN.SD = 000	96	118	mA	*1, *5
				CPU: 60 MHz, Peripheral: 30 MHz, FLASH 0 Wait FRWTR.RWT = 00 FSYNDN.SD = 000	76	94	mA	*1, *5
				CPU: 80 MHz, Peripheral: 40 MHz, FLASH 5 Wait FRWTR.RWT = 10 FSYNDN.SD = 011	66	82	mA	*1, *5
				CPU: 60 MHz, Peripheral: 30 MHz, FLASH 3 Wait FRWTR.RWT = 00 FSYNDN.SD = 011	52	65	mA	*1, *5
			High-speed CR RUN mode	CPU/Peripheral: 4 MHz*2 FLASH 0 Wait FRWTR.RWT = 00 FSYNDN.SD = 000	6.0	9.2	mA	*1
			Sub RUN mode	CPU/Peripheral: 32 kHz FLASH 0 Wait FRWTR.RWT = 00 FSYNDN.SD = 000	0.2	2.24	mA	*1, *6
			Low-speed CR RUN mode	CPU/Peripheral: 100 kHz FLASH 0 Wait FRWTR.RWT = 00 FSYNDN.SD = 000	0.3	2.36	mA	*1
SLEEP mode current	Iccs		PLL SLEEP mode	Peripheral: 40 MHz	43	54	mA	*1, *5
			High-speed CR SLEEP mode	Peripheral: 4 MHz*2	3.5	6.2	mA	*1
			Sub SLEEP mode	Peripheral: 32 kHz	0.15	2.18	mA	*1, *6
			Low-speed CR SLEEP mode	Peripheral: 100 kHz	0.22	2.27	mA	*1

*1: When all ports are fixed.

*2: When setting it to 4 MHz by trimming.

*3: T_A = +25°C, V_{CC} = 3.3 V

*4: T_A = +85°C, V_{CC} = 5.5 V

*5: When using the crystal oscillator of 4 MHz (Including the current consumption of the oscillation circuit)

*6: When using the crystal oscillator of 32 kHz (Including the current consumption of the oscillation circuit)

(Vcc = AVcc =2.7V to 5.5V, Vss = AVss = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions		Value		Unit	Remarks
					Typ*2	Max*3		
TIMER mode current	I_{CCT}	VCC	Main TIMER mode	T_A = + 25°C, When LVD is off	2.4	2.5	mA	*1, *4
				T_A = + 85°C, When LVD is off	-	5.4	mA	*1, *4
			Sub TIMER mode	T_A = + 25°C, When LVD is off	110	300	µA	*1, *5
				T_A = + 85°C, When LVD is off	-	2.2	mA	*1, *5
STOP mode current	I_{CCH}		STOP mode	T_A = + 25°C, When LVD is off	50	200	µA	*1
				T_A = + 85°C, When LVD is off	-	2	mA	*1

*1: When all ports are fixed.

*2: V_{CC}=3.3 V

*3: V_{CC}=5.5 V

*4: When using the crystal oscillator of 4 MHz(Including the current consumption of the oscillation circuit)

*5: When using the crystal oscillator of 32 kHz(Including the current consumption of the oscillation circuit)

Low-Voltage Detection Current

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Typ	Max		
Low-Voltage detection circuit (LVD) power supply current	I_{CCLVD}	VCC	At operation for interrupt	2	10	µA	At not detect

Flash Memory Current

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Typ	Max		
Flash memory write/erase current	$I_{CCFLASH}$	VCC	At Write/Erase	13	24	mA	

A/D Converter Current

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = AVRL = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Typ	Max		
Power supply current	I_{CCAD}	AVCC	At 1unit operation	2.3	3.6	mA	
			At stop	0.1	2	µA	
Reference power supply current	I_{CCAVRH}	AVRH	At 1unit operation AVRH=5.5 V	2.2	3.0	mA	
			At stop	0.03	0.6	µA	

12.3.2 Pin Characteristics

(Vcc = AVcc = 2.7V to 5.5V, Vss = AVss = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage (hysteresis input)	V_{IHS}	CMOS hysteresis input pin, MD0,1	-	Vcc × 0.8	-	Vcc + 0.3	V	
"L" level input voltage (hysteresis input)	V_{ILS}	CMOS hysteresis input pin, MD0,1	-	Vss - 0.3	-	Vcc × 0.2	V	
"H" level output voltage	V_{OH}	4mA type	Vcc ≥ 4.5 V I_{OH} = - 4 mA	Vcc - 0.5	-	Vcc	V	
			Vcc < 4.5 V I_{OH} = - 2 mA					
		12mA type	Vcc ≥ 4.5 V I_{OH} = - 12 mA	Vcc - 0.5	-	Vcc	V	
			Vcc < 4.5 V I_{OH} = - 8 mA					
		P80, P81	Vcc ≥ 4.5 V I_{OH} = - 25.3 mA	Vcc - 0.4	-	Vcc	V	
			Vcc < 4.5 V I_{OH} = - 13.4 mA					
"L" level output voltage	V_{OL}	4mA type	Vcc ≥ 4.5 V I_{OL} = 4 mA	Vss	-	0.4	V	
			Vcc < 4.5 V I_{OL} = 2 mA					
		12mA type	Vcc ≥ 4.5 V I_{OL} = 12 mA	Vss	-	0.4	V	
			Vcc < 4.5 V I_{OL} = 8 mA					
		P80, P81	Vcc ≥ 4.5 V I_{OL} = 19.7 mA	Vss	-	0.4	V	
			Vcc < 4.5 V I_{OL} = 11.9 mA					
Input leak current	I_{IL}	-	-	- 5	-	5	µA	
Pull-up resistance value	R_{PU}	Pull-up pin	Vcc ≥ 4.5 V	25	50	100	kΩ	
			Vcc < 4.5 V	30	80	200		
Input capacitance	C_{IN}	Other than Vcc, Vss, AVcc, AVss, AVRH	-	-	5	15	pF	

12.4 AC Characteristics

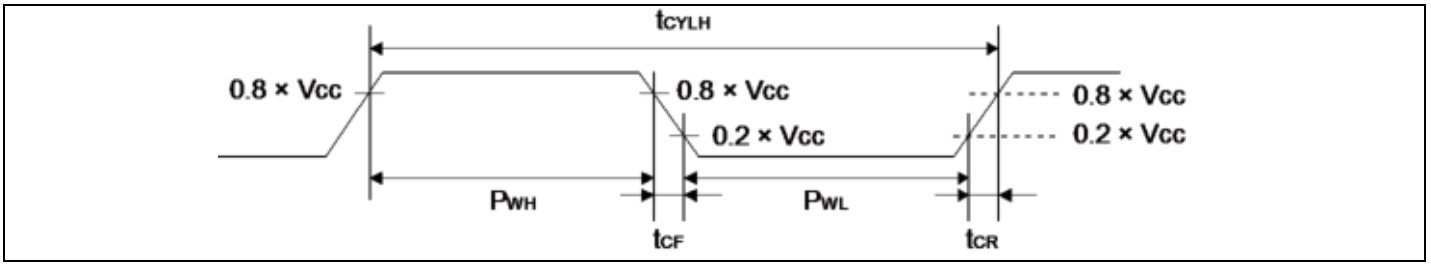
12.4.1 Main Clock Input Characteristics

(Vcc = 2.7V to 5.5V, Vss = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input frequency	F_{CH}	X0 X1	Vcc ≥ 4.5 V	4	48	MHz	When crystal oscillator is connected
			Vcc < 4.5 V	4	20		
			Vcc ≥ 4.5 V	4	48	MHz	When using external clock
			Vcc < 4.5 V	4	20		
Input clock cycle	t_{CYLH}		Vcc ≥ 4.5 V	20.83	250	ns	When using external clock
			Vcc < 4.5 V	50	250		
Input clock pulse width	-		P_{WH}/t_{CYLH} P_{WL}/t_{CYLH}	45	55	%	When using external clock
Input clock rise time and fall time	t_{CF} t_{CR}		-	-	5	ns	When using external clock
Internal operating clock*1 frequency	F_{CM}	-	-	-	80	MHz	Master clock
	F_{CC}	-	-	-	80	MHz	Base clock (HCLK/FCLK)
	F_{CP0}	-	-	-	40	MHz	APB0 bus clock*2
	F_{CP1}	-	-	-	40	MHz	APB1 bus clock*2
	F_{CP2}	-	-	-	40	MHz	APB2 bus clock*2
Internal operating clock*1 cycle time	t_{CYCC}	-	-	12.5	-	ns	Base clock (HCLK/FCLK)
	t_{CYCP0}	-	-	25	-	ns	APB0 bus clock*2
	t_{CYCP1}	-	-	25	-	ns	APB1 bus clock*2
	t_{CYCP2}	-	-	25	-	ns	APB2 bus clock*2

*1: For more information about each internal operating clock, see "CHAPTER 2-1: Clock" in "FM3 Family PERIPHERAL MANUAL".

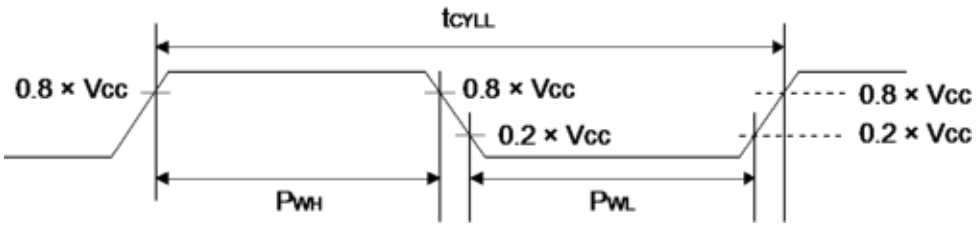
*2: For about each APB bus which each peripheral is connected to, see "Block Diagram" in this data sheet.



12.4.2 Sub Clock Input Characteristics

(Vcc = 2.7V to 5.5V, Vss = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input frequency	F_{CL}	X0A X1A	-	-	32.768	-	kHz	When crystal oscillator is connected
			-	32	-	100	kHz	When using external clock
Input clock cycle	t_{CYLL}		-	10	-	31.25	µs	When using external clock
Input clock pulse width	-		P_{WH}/t_{CYLL} P_{WL}/t_{CYLL}	45	-	55	%	When using external clock



12.4.3 Built-in CR Oscillation Characteristics

Built-in high-speed CR

(Vcc = 2.7V to 5.5V, Vss = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	F_{CRH}	T_A = + 25°C	3.92	4	4.08	MHz	When trimming*1
		T_A = 0°C to + 70°C	3.84	4	4.16		
		T_A = - 40°C to + 85°C	3.8	4	4.2		
		T_A = - 40°C to + 85°C	3	4	6		When not trimming
Frequency stability time	t_{CRWT}	-	-	-	50	µs	*2

*1: In the case of using the values in CR trimming area of Flash memory at shipment for frequency trimming.

*2: Frequency stable time is time to stable of the frequency of the High-speed CR clock after the trim value is set. After setting the trim value, the period when the frequency stability time passes can use the High-speed CR clock as a source clock.

Built-in low-speed CR

(Vcc = 2.7V to 5.5V, Vss = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	F_{CRL}	-	50	100	150	kHz	

12.4.4 Operating Conditions of Main PLL (In the case of using main clock for input of PLL)

(Vcc = 2.7V to 5.5V, Vss = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time (LOCK UP time)*1	t_{LOCK}	100	-	-	µs	
PLL input clock frequency	f_{PLLI}	4	-	30	MHz	
PLL multiple rate	-	4	-	30	multiple	
PLL macro oscillation clock frequency	f_{PLLO}	60	-	120	MHz	
Main PLL clock frequency*2	F_{CLKPLL}	-	-	80	MHz	

*1: Time from when the PLL starts operating until the oscillation stabilizes.

*2: For more information about Main PLL clock (CLKPLL), see "CHAPTER 2-1: Clock" in "FM3 Family PERIPHERAL MANUAL".

12.4.5 Operating Conditions of Main PLL (In the case of using built-in high speed CR)

(Vcc = 2.7V to 5.5V, Vss = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time (LOCK UP time)*1	t_{LOCK}	100	-	-	µs	
PLL input clock frequency	f_{PLLI}	3.8	4	4.2	MHz	
PLL multiple rate	-	15	-	28	multiple	
PLL macro oscillation clock frequency	f_{PLLO}	57	-	120	MHz	
Main PLL clock frequency*2	F_{CLKPLL}	-	-	80	MHz	

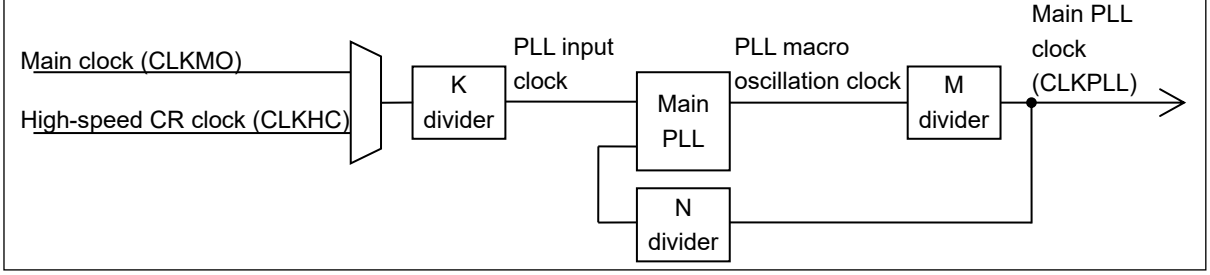
*1: Time from when the PLL starts operating until the oscillation stabilizes.

*2: For more information about Main PLL clock (CLKPLL), see "CHAPTER 2-1: Clock" in "FM3 Family PERIPHERAL MANUAL".

Note:

− *Make sure to input to the main PLL source clock, the high-speed CR clock (CLKHC) that the frequency has been trimmed.*

Main PLL connection



12.4.6 Reset Input Characteristics

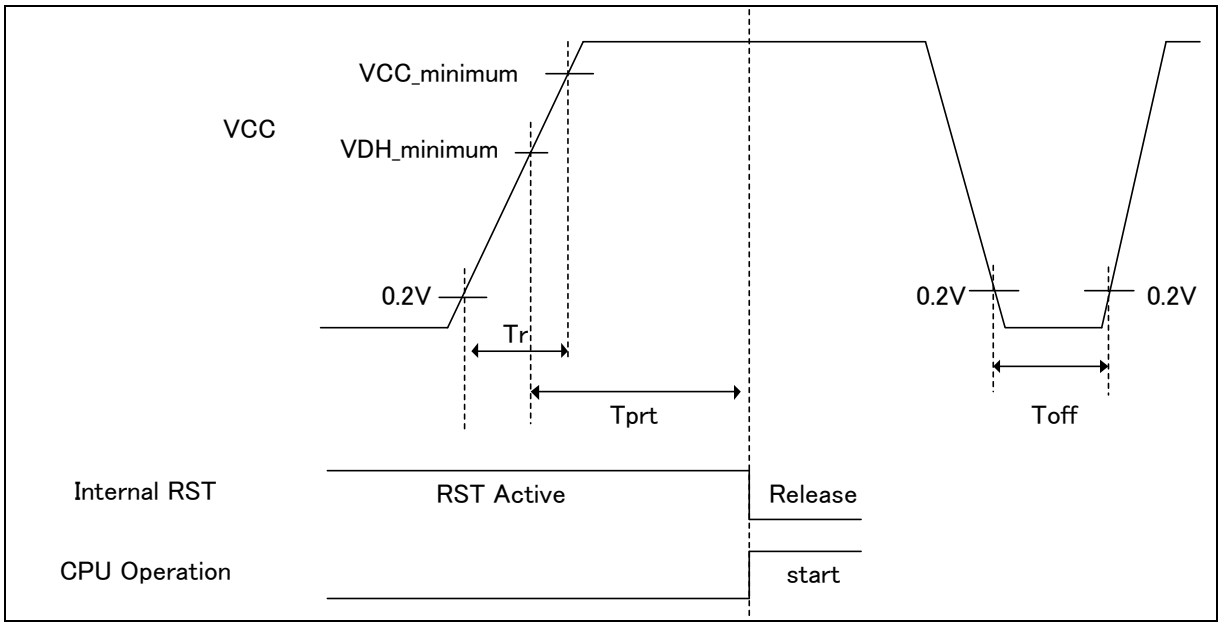
(Vcc = 2.7V to 5.5V, Vss = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Reset input time	t_{INITX}	INITX	-	500	-	ns	

12.4.7 Power-on Reset Timing

(Vcc = 2.7V to 5.5V, Vss = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
Power supply rising time	Tr	Vcc	0	-	ms	
Power supply shut down time	Toff		1	-	ms	
Time until releasing Power-on reset	Tprt		0.422	0.704	ms	



Glossary

- VCC_minimum: Minimum V_{CC} of recommended operating conditions
- VDH_minimum: Minimum release voltage of Low-Voltage detection reset.
  See "12.6 Low-Voltage Detection Characteristics"

12.4.8 External Bus Timing

Asynchronous SRAM Mode

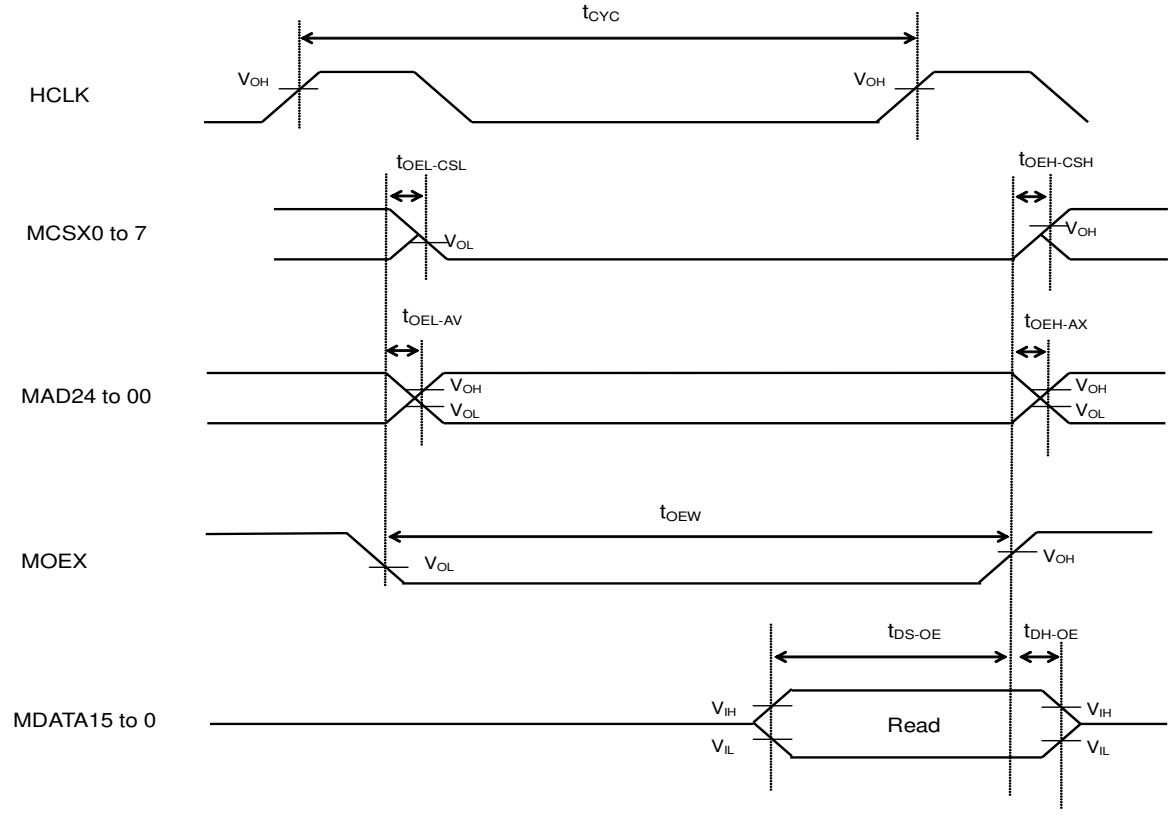
(Vcc = 2.7V to 5.5V, Vss = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
MOEX Min pulse width	t_{OEW}	MOEX	Vcc ≥ 4.5 V	T_{HCLK}×1 - 3	-	ns	
			Vcc < 4.5 V				
MOEX ↓ ⇒ Address delay time	$t_{OEL - AV}$	MOEX MAD24 to 00	Vcc ≥ 4.5 V	0	10	ns	
			Vcc < 4.5 V	0	20		
MOEX ↑ ⇒ Address delay time	$t_{OEH - AX}$	MOEX MAD24 to 00	Vcc ≥ 4.5 V	0	10	ns	
			Vcc < 4.5 V	0	20		
MOEX ↓ ⇒ MCSX ↓ delay time	$t_{OEL - CSL}$	MOEX MCSX	Vcc ≥ 4.5 V	0	10	ns	
			Vcc < 4.5 V				
MOEX ↑ ⇒ MCSX ↑ delay time	$t_{OEH - CSH}$	MOEX MCSX	Vcc ≥ 4.5 V	0	10	ns	
			Vcc < 4.5 V				
Data set up ⇒MOEX ↑ time	$t_{DS - OE}$	MOEX MDATA15 to 0	Vcc ≥ 4.5 V	20	-	ns	
			Vcc < 4.5 V	38	-		
MOEX ↑ ⇒ Data hold time	$t_{DH - OE}$	MOEX MDATA15 to 0	Vcc ≥ 4.5 V	0	-	ns	
			Vcc < 4.5 V				
MCSX ↓ ⇒ MWEX ↓ delay time	$t_{CSL - WEL}$	MCSX MWEX	Vcc ≥ 4.5 V	T_{HCLK}×1 - 5	-	ns	
			Vcc < 4.5 V	T_{HCLK}×1 - 10	-		
MWEX ↑ ⇒ MCSX ↑ delay time	$t_{WEH - CSH}$	MCSX MWEX	Vcc ≥ 4.5 V	T_{HCLK}×1 - 5	-	ns	
			Vcc < 4.5 V	T_{HCLK}×1 - 10	-		
Address ⇒ MWEX ↓ delay time	$t_{AV - WEL}$	MWEX MAD24 to 00	Vcc ≥ 4.5 V	T_{HCLK}×1 - 5	-	ns	
			Vcc < 4.5 V	T_{HCLK}×1 - 15	-		
MWEX ↑ ⇒ Address delay time	$t_{WEH - AX}$	MWEX MAD24 to 00	Vcc ≥ 4.5 V	T_{HCLK}×1 - 5	-	ns	
			Vcc < 4.5 V	T_{HCLK}×1 - 15	-		
MWEX ↓ ⇒ MDQM ↓ delay time	$t_{WEL - DQML}$	MWEX MDQM0 to 1	Vcc ≥ 4.5 V	0	5	ns	
			Vcc < 4.5 V	0	10		
MWEX ↑ ⇒ MDQM ↑ delay time	$t_{WEH - DQMH}$	MWEX MDQM0 to 1	Vcc ≥ 4.5 V	0	5	ns	
			Vcc < 4.5 V	0	10		
MWEX Min pulse width	t_{WEW}	MWEX	Vcc ≥ 4.5 V	T_{HCLK}×1 - 3	-	ns	
			Vcc < 4.5 V				
MWEX ↓ ⇒ Data delay time	$t_{WEL - DV}$	MWEX MDATA15 to 0	Vcc ≥ 4.5 V	- 5	5	ns	
			Vcc < 4.5 V	-15	15		
MWEX ↑ ⇒ Data delay time	$t_{WEH - DX}$	MWEX MDATA15 to 0	Vcc ≥ 4.5 V	T_{HCLK}×1 - 5	-	ns	
			Vcc < 4.5 V	T_{HCLK}×1 - 15	-		

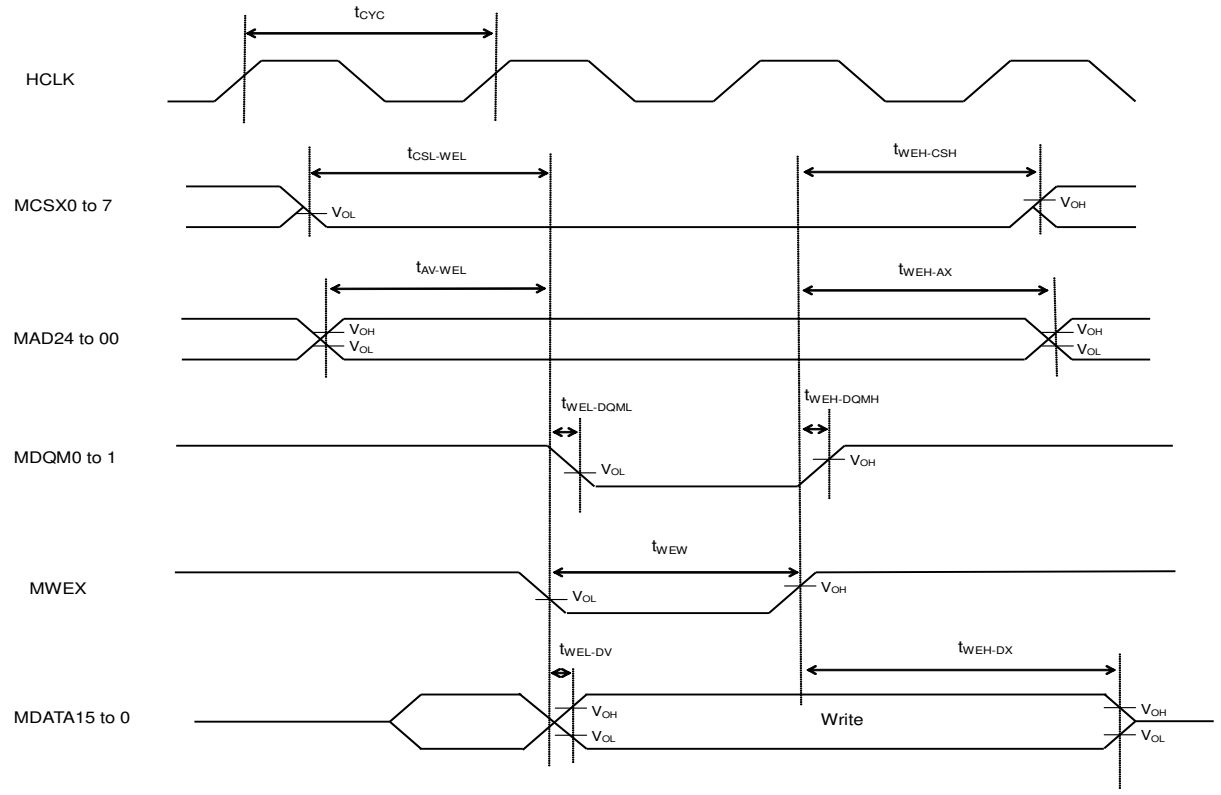
Note:

- *When the external load capacitance C_L = 50 pF.*

SRAM read


tCYC
HCLK
VOH
VOH
tOEL-CSL
tOEH-CSH
MCSX0 to 7
VOL
VOH
tOEL-AV
tOEH-AX
MAD24 to 00
VOH
VOL
VOH
VOL
tOEW
MOEX
VOL
VOH
tDS-OE
tDH-OE
MDATA15 to 0
VIH
VIL
Read
VIH
VIL

SRAM write


tCYC
HCLK
tCSL-WEL
tWEH-CSH
MCSX0 to 7
VOL
VOH
tAV-WEL
tWEH-AX
MAD24 to 00
VOH
VOL
tWEL-DQML
tWEH-DQMH
MDQM0 to 1
tWEW
MWEX
tWEL-DV
tWEH-DX
MDATA15 to 0
Write

NAND FLASH mode

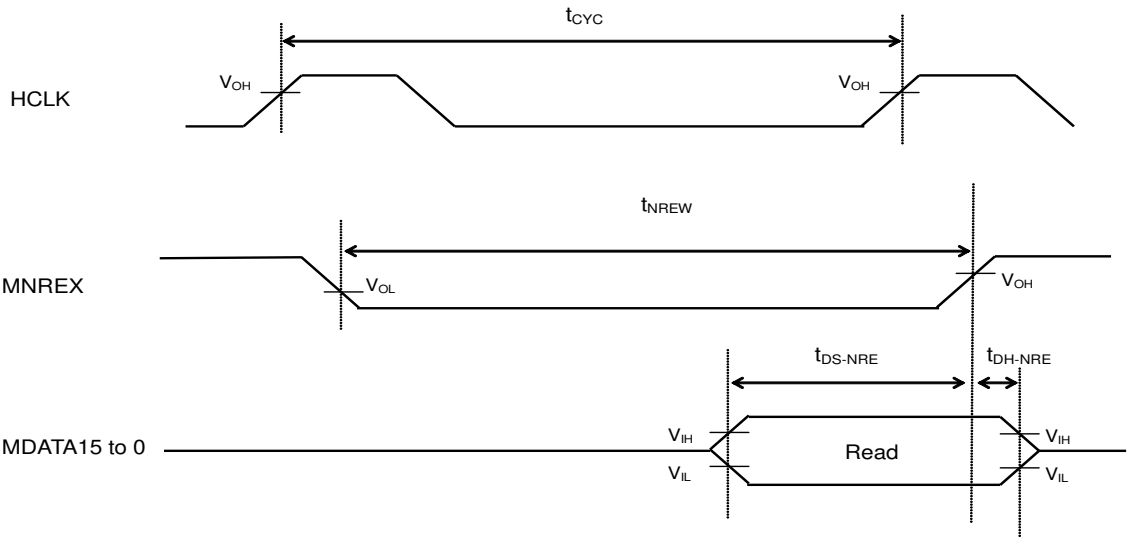
(Vcc = 2.7V to 5.5V, Vss = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
MNREX Min pulse width	t_{NREW}	MNREX	Vcc ≥ 4.5 V	T_{HCLK}×1 - 3	-	ns	
			Vcc < 4.5 V				
Data set up ⇒ MNREX ↑ time	$t_{DS - NRE}$	MNREX MDATA15 to 0	Vcc ≥ 4.5 V	20	-	ns	
			Vcc < 4.5 V	38	-		
MNREX ↑ ⇒ Data hold time	$t_{DH - NRE}$	MNREX MDATA15 to 0	Vcc ≥ 4.5 V	0	-	ns	
			Vcc < 4.5 V	0	-		
MNALE ↑ ⇒ MNWEX delay time	$t_{ALEH - NWEL}$	MNALE MNWEX	Vcc ≥ 4.5 V	T_{HCLK}×1 - 5	-	ns	
			Vcc < 4.5 V	T_{HCLK}×1 - 15	-		
MNWEX ↑ ⇒ MNALE delay time	$t_{NWEH - ALEL}$	MNALE MNWEX	Vcc ≥ 4.5 V	T_{HCLK}×1 - 5	-	ns	
			Vcc < 4.5 V	T_{HCLK}×1 - 15	-		
MNCLE ↑ ⇒ MNWEX delay time	$t_{CLEH - NWEL}$	MNCLE MNWEX	Vcc ≥ 4.5 V	T_{HCLK}×1 - 5	-	ns	
			Vcc < 4.5 V	T_{HCLK}×1 - 15	-		
MNWEX ↑ ⇒ MNCLE delay time	$t_{NWEH - CLEL}$	MNCLE MNWEX	Vcc ≥ 4.5 V	T_{HCLK}×1 - 5	-	ns	
			Vcc < 4.5 V	T_{HCLK}×1 - 15	-		
MNWEX Min pulse width	t_{NWEW}	MNWEX	Vcc ≥ 4.5 V	T_{HCLK}×1 - 3	-	ns	
			Vcc < 4.5 V				
MNWEX ↓ ⇒ Data delay time	$t_{NWEL - DV}$	MNWEX MDATA15 to 0	Vcc ≥ 4.5 V	- 5	+ 5	ns	
			Vcc < 4.5 V	-15	+15		
MNWEX ↑ ⇒ Data delay time	$t_{NWEH - DX}$	MNWEX MDATA15 to 0	Vcc ≥ 4.5 V	T_{HCLK}×1 - 5	-	ns	
			Vcc < 4.5 V	T_{HCLK}×1 - 15	-		

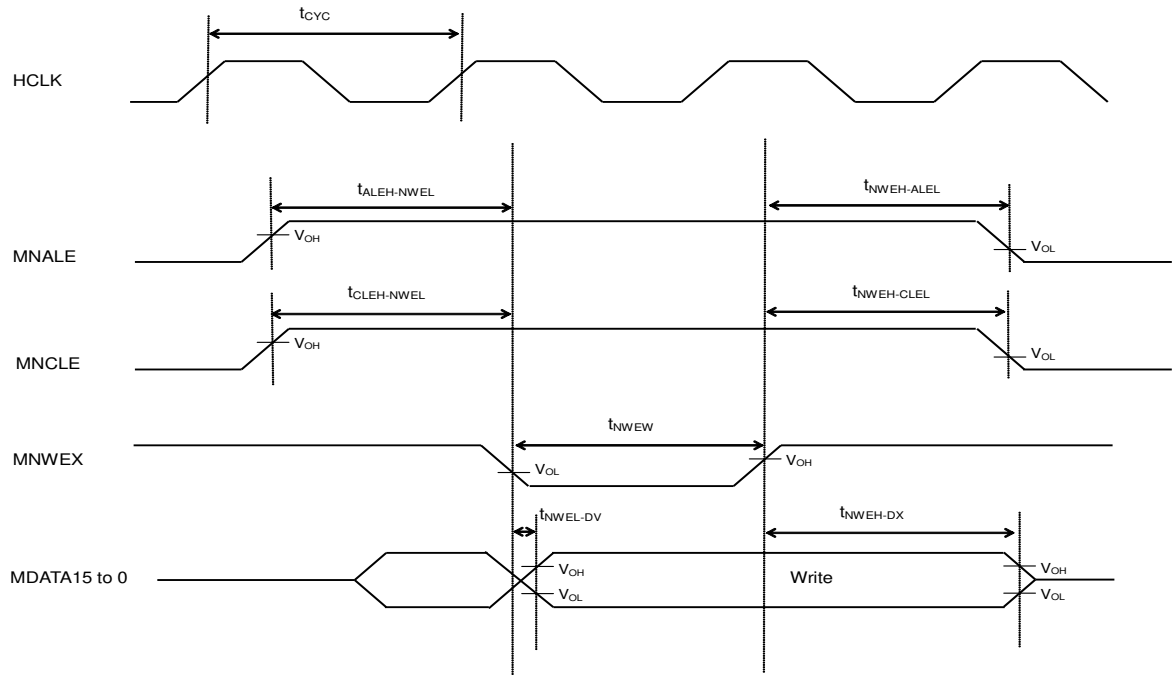
Note:

- *When the external load capacitance C_L = 50 pF.*

NAND FLASH read



NAND FLASH write

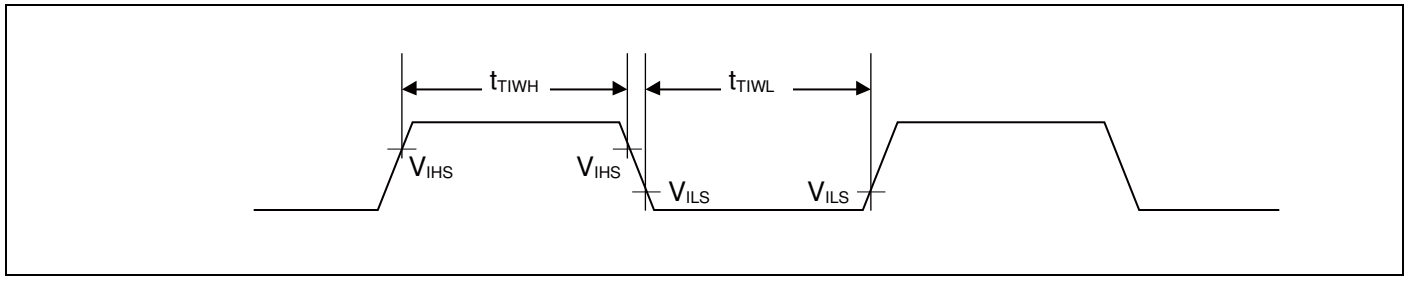


12.4.9 Base Timer Input Timing

Timer input timing

(Vcc = 2.7V to 5.5V, Vss = 0V, T_A = - 40°C to + 85°C)

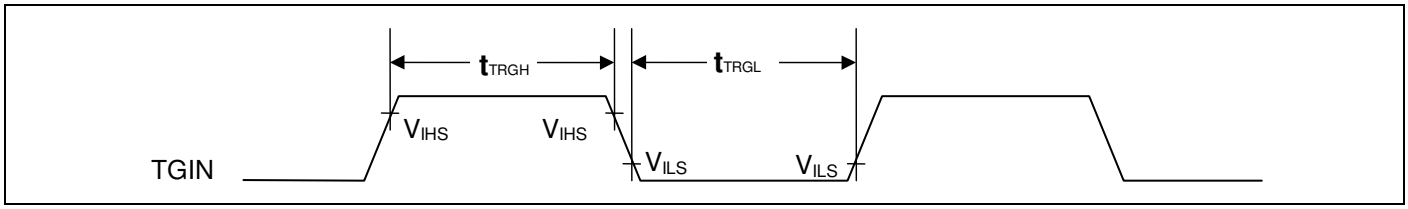
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TIWH} t_{TIWL}	TIOAn/TIOBn (when using as ECK,TIN)	-	$2t_{CYCP}$	-	ns	



Trigger input timing

(Vcc = 2.7V to 5.5V, Vss = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH} t_{TRGL}	TIOAn/TIOBn (when using as TGIN)	-	$2t_{CYCP}$	-	ns	



Note:

- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which the Base Timer is connected to, see "Block Diagram" in this data sheet.

12.4.10 CSIO/UART Timing

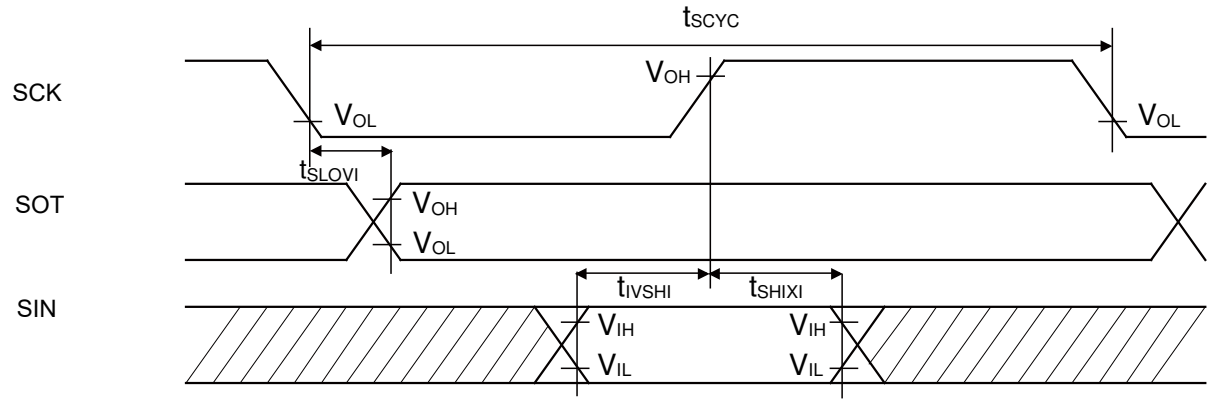
CSIO (SPI = 0, SCINV = 0)

(Vcc = 2.7V to 5.5V, Vss = 0V, T_A = - 40°C to + 85°C)

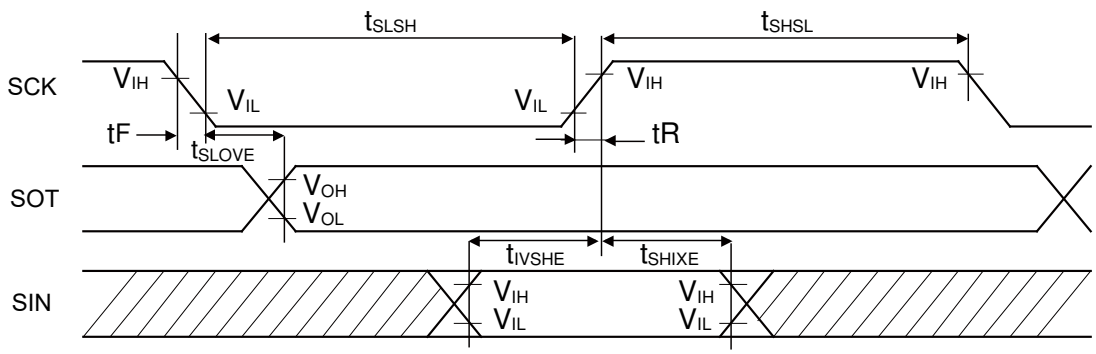
Parameter	Symbol	Pin name	Conditions	Vcc < 4.5 V		Vcc ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Baud Rate	-	-	-	-	8	-	8	Mbps
Serial clock cycle time	t_{SCYC}	SCKx	Master mode	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCKx SOTx		-30	+30	- 20	+ 20	ns
SIN → SCK ↑ setup time	t_{IVSHI}	SCKx SINx		50	-	30	-	ns
SCK ↑ → SIN hold time	t_{SHIXI}	SCKx SINx		0	-	0	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKx	Slave mode	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCKx SOTx		-	50	-	30	ns
SIN → SCK ↑ setup time	t_{IVSHE}	SCKx SINx		10	-	10	-	ns
SCK ↑ → SIN hold time	t_{SHIXE}	SCKx SINx		20	-	20	-	ns
SCK fall time	tF	SCKx		-	5	-	5	ns
SCK rise time	tR	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which Multi-function Serial is connected to, see "Block Diagram" in this data sheet.
- *These characteristics only guarantee the same relocate port number.*
  For example, the combination of SCKx_0 and SOTx_1 is not guaranteed.
- *When the external load capacitance C_L = 50 pF.*



Master mode



Slave mode

CSIO (SPI = 0, SCINV = 1)

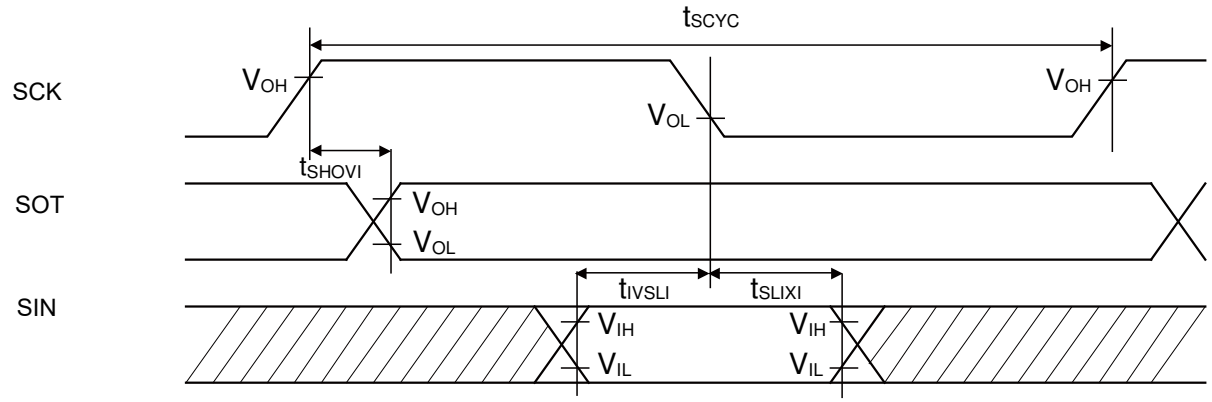
(Vcc = 2.7V to 5.5V, Vss = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Vcc < 4.5 V		Vcc ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Baud Rate	-	-	-	-	8	-	8	Mbps
Serial clock cycle time	t_{SCYC}	SCKx	Master mode	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCKx SOTx		-30	+30	- 20	+ 20	ns
SIN → SCK ↓ setup time	t_{IVSLI}	SCKx SINx		50	-	30	-	ns
SCK ↓ → SIN hold time	t_{SLIXI}	SCKx SINx		0	-	0	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKx	Slave mode	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↑ → SOT delay time	t_{SHOVE}	SCKx SOTx		-	50	-	30	ns
SIN → SCK ↓ setup time	t_{IVSLE}	SCKx SINx		10	-	10	-	ns
SCK ↓ → SIN hold time	t_{SLIXE}	SCKx SINx		20	-	20	-	ns
SCK fall time	tF	SCKx		-	5	-	5	ns
SCK rise time	tR	SCKx		-	5	-	5	ns

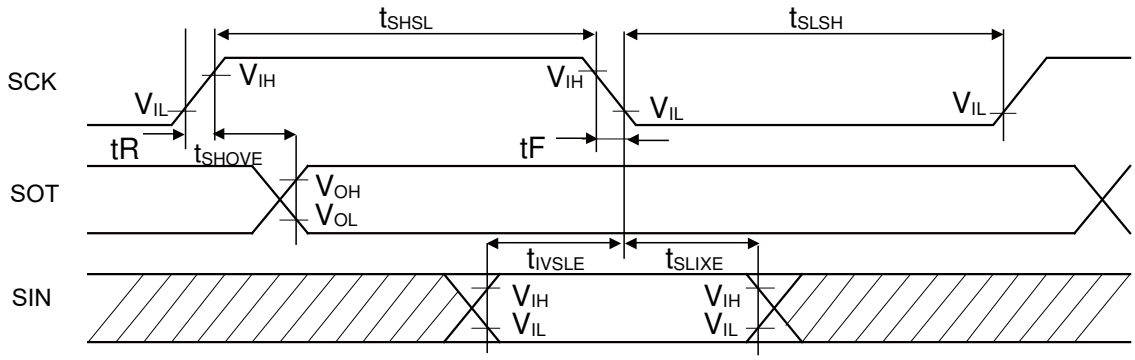
Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
- *About the APB bus number which Multi-function Serial is connected to, see "Block Diagram" in this data sheet.*
- *These characteristics only guarantee the same relocate port number.*
  For example, the combination of SCKx_0 and SOTx_1 is not guaranteed.
- *When the external load capacitance C_L = 50 pF.*

•



Master mode



Slave mode

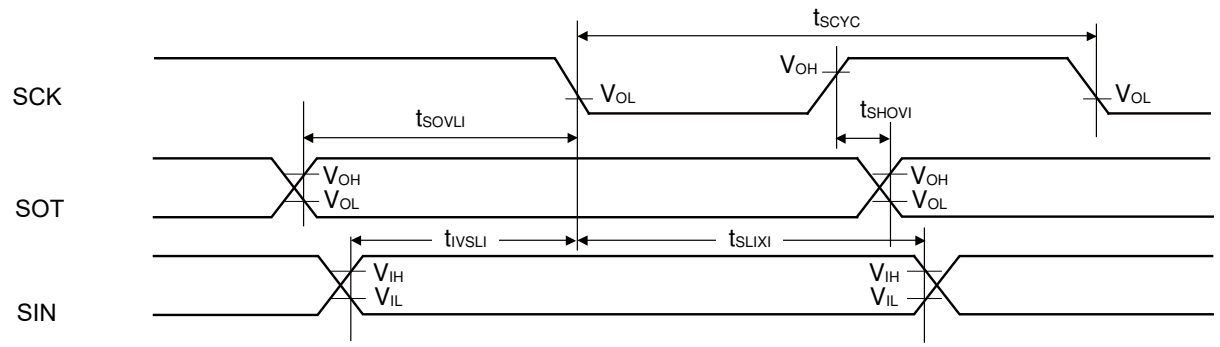
CSIO (SPI = 1, SCINV = 0)

(Vcc = 2.7V to 5.5V, Vss = 0V, T_A = - 40°C to + 85°C)

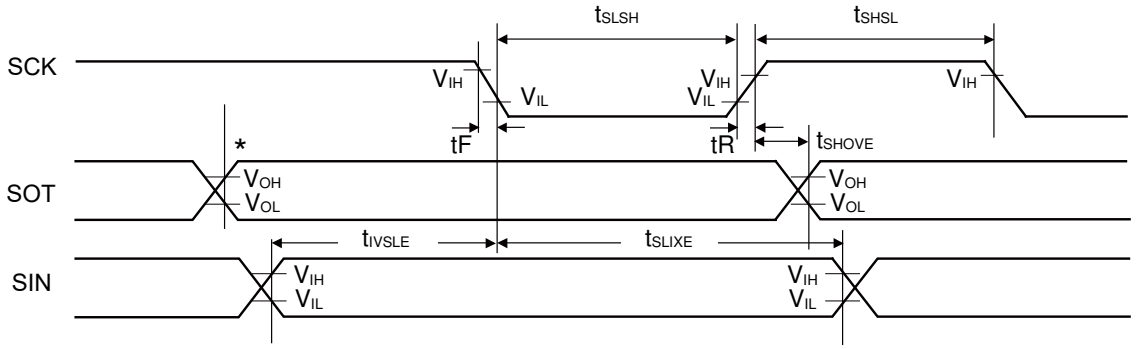
Parameter	Symbol	Pin name	Conditions	Vcc < 4.5 V		Vcc ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Baud Rate	-	-	-	-	8	-	8	Mbps
Serial clock cycle time	t_{SCYC}	SCKx	Master mode	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCKx SOTx		-30	+30	- 20	+ 20	ns
SIN → SCK ↓ setup time	t_{IVSLI}	SCKx SINx		50	-	30	-	ns
SCK ↓ → SIN hold time	t_{SLIXI}	SCKx SINx		0	-	0	-	ns
SOT → SCK ↓ delay time	t_{SOVLI}	SCKx SOTx		$2t_{CYCP}$ - 30	-	$2t_{CYCP}$ - 30	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKx	Slave mode	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↑ → SOT delay time	t_{SHOVE}	SCKx SOTx		-	50	-	30	ns
SIN → SCK ↓ setup time	t_{IVSLE}	SCKx SINx		10	-	10	-	ns
SCK ↓ → SIN hold time	t_{SLIXE}	SCKx SINx		20	-	20	-	ns
SCK fall time	tF	SCKx		-	5	-	5	ns
SCK rise time	tR	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
- *About the APB bus number which Multi-function Serial is connected to, see "Block Diagram" in this data sheet.*
- *These characteristics only guarantees the same relocate port number.*
  For example, the combination of SCKx_0 and SOTx_1 is not guaranteed.
- *When the external load capacitance C_L= 50 pF.*



Master mode



Slave mode

*: Changes when writing to TDR register

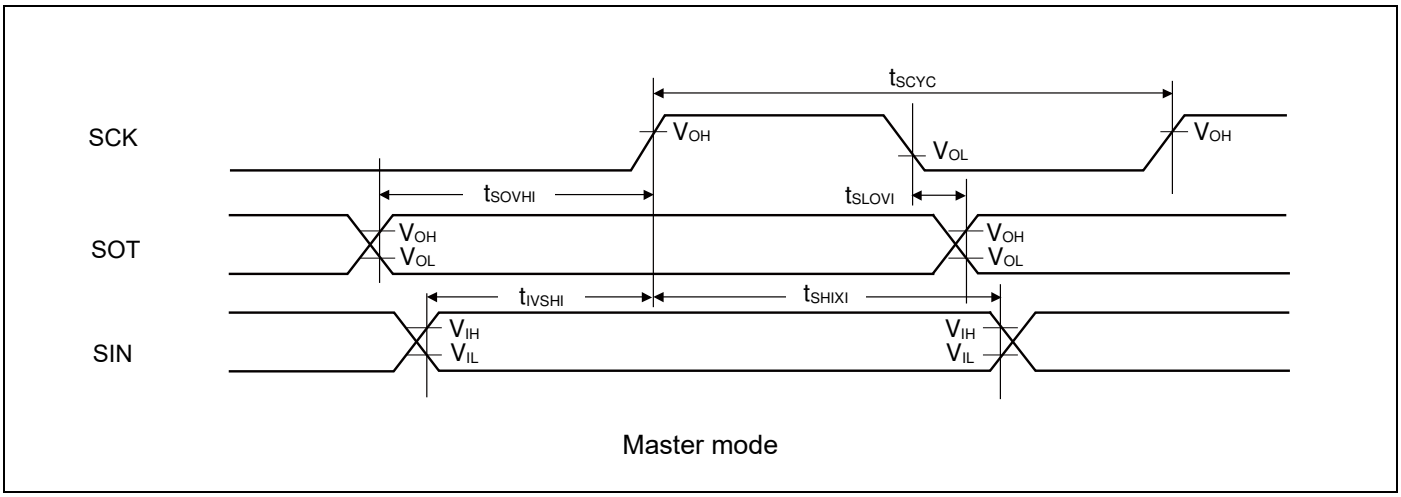
CSIO (SPI = 1, SCINV = 1)

(Vcc = 2.7V to 5.5V, Vss = 0V, T_A = - 40°C to + 85°C)

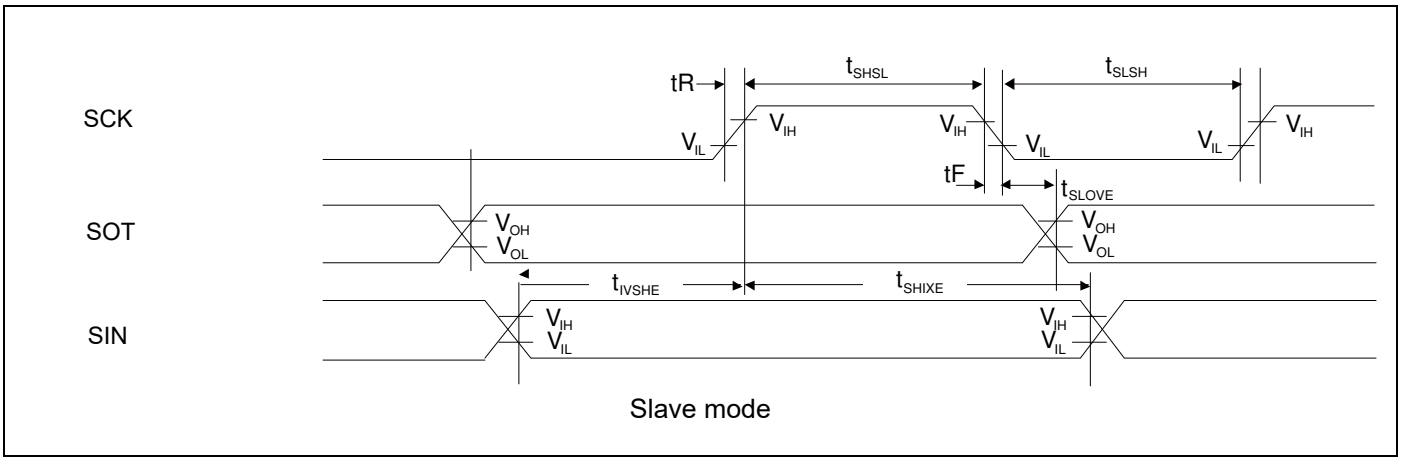
Parameter	Symbol	Pin name	Conditions	Vcc < 4.5 V		Vcc ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Baud Rate	-	-	-	-	8	-	8	Mbps
Serial clock cycle time	t_{SCYC}	SCKx	Master mode	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCKx SOTx		-30	+30	- 20	+ 20	ns
SIN → SCK ↑ setup time	t_{IVSHI}	SCKx SINx		50	-	30	-	ns
SCK ↑ → SIN hold time	t_{SHIXI}	SCKx SINx		0	-	0	-	ns
SOT → SCK ↑ delay time	t_{SOVHI}	SCKx SOTx		$2t_{CYCP}$ - 30	-	$2t_{CYCP}$ - 30	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKx	Slave mode	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCKx SOTx		-	50	-	30	ns
SIN → SCK ↑ setup time	t_{IVSHE}	SCKx SINx		10	-	10	-	ns
SCK ↑ → SIN hold time	t_{SHIXE}	SCKx SINx		20	-	20	-	ns
SCK fall time	tF	SCKx		-	5	-	5	ns
SCK rise time	tR	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
- *About the APB bus number which Multi-function Serial is connected to, see "Block Diagram" in this data sheet.*
- *These characteristics only guarantee the same relocate port number.*
  For example, the combination of SCKx_0 and SOTx_1 is not guaranteed.
- *When the external load capacitance C_L = 50 pF.*



Master mode

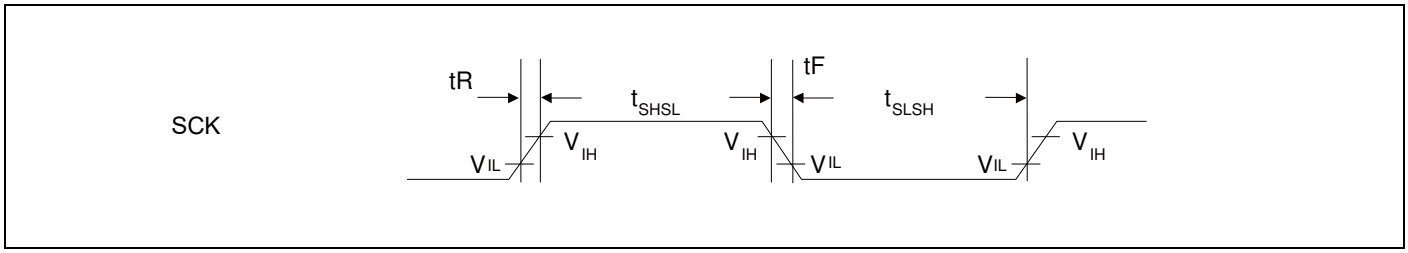


Slave mode

UART external clock input (EXT = 1)

(Vcc = 2.7V to 5.5V, Vss = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Conditions	Min	Max	Unit	Remarks
Serial clock "L" pulse width	t_{SLSH}	C_L = 50 pF	t_{CYCP} + 10	-	ns	
Serial clock "H" pulse width	t_{SHSL}		t_{CYCP} + 10	-	ns	
SCK fall time	tF		-	5	ns	
SCK rise time	tR		-	5	ns	

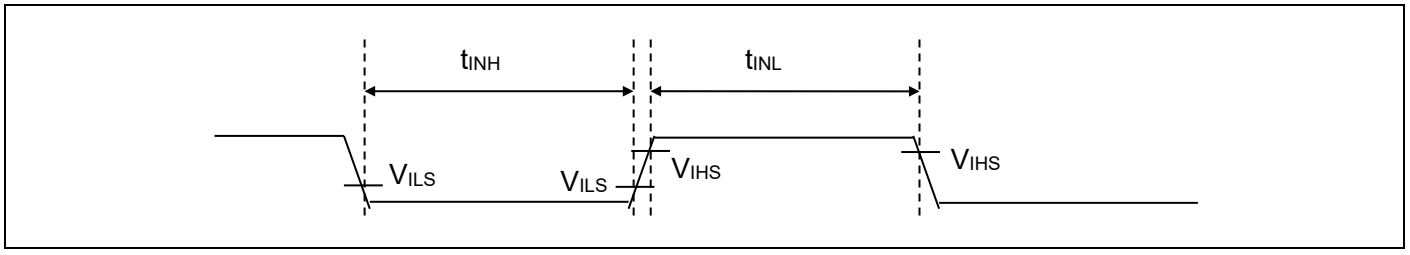


12.4.11 External input timing

(Vcc = 2.7V to 5.5V, Vss = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{INH} t_{INL}	ADTG	-	$2t_{CYCP}$ *	-	ns	A/D converter trigger input
		FRCKx					Free-run timer input clock
		ICxx					Input capture
		DTTIxX	-	$2t_{CYCP}$ *	-	ns	Wave form generator
		INTxx, NMIX	Except Timer mode, Stop mode	$2t_{CYCP}$ + 100 *	-	ns	External interrupt NMI
			Timer mode, Stop mode	500	-	ns	

*: t_{CYCP} indicates the APB bus clock cycle time.
About the APB bus number which the A/D converter, Multi-function Timer, External interrupt are connected to, see "Block Diagram" in this data sheet.

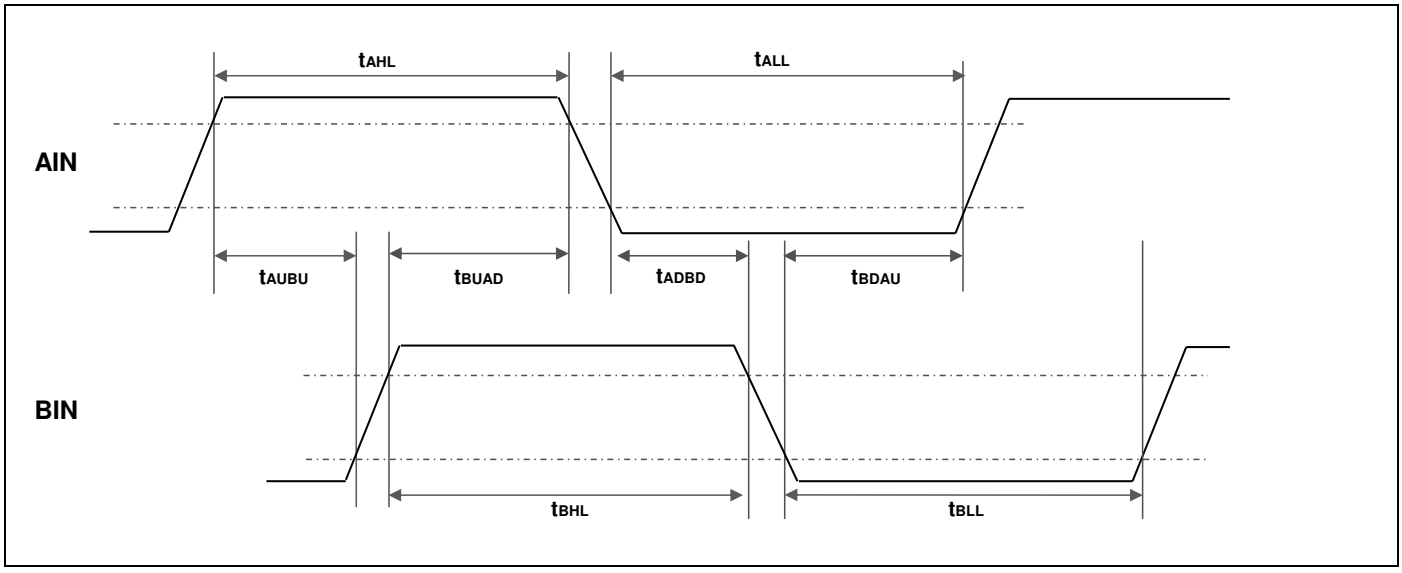


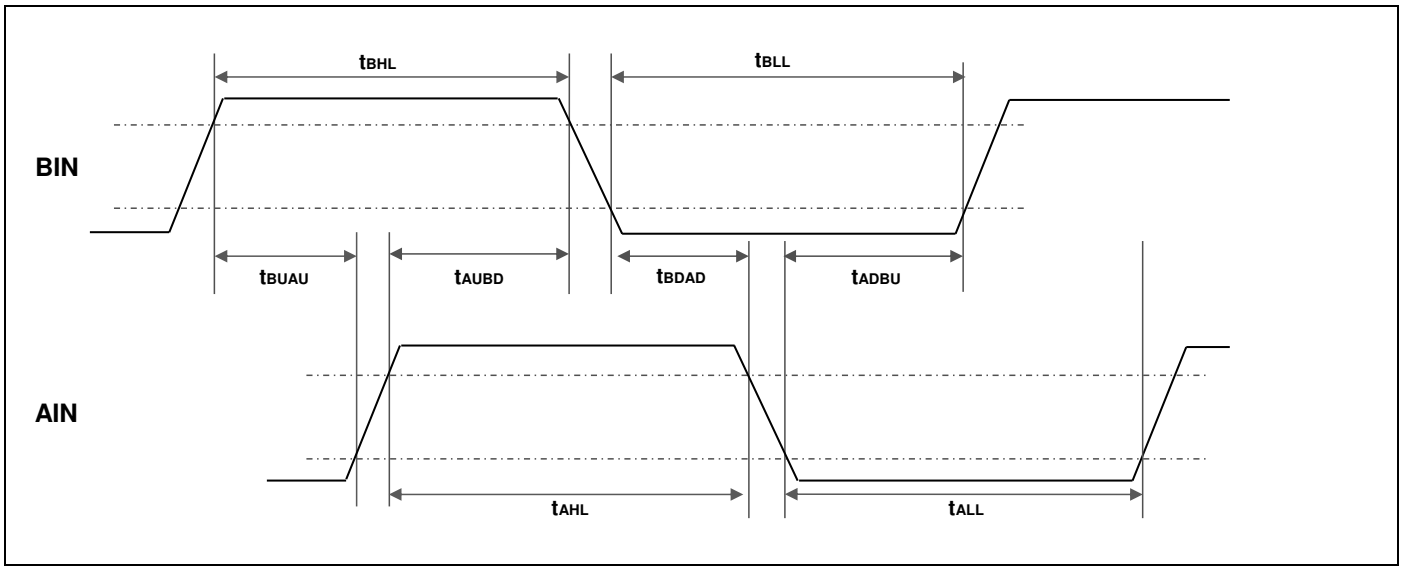
12.4.12 Quadrature Position/Revolution Counter timing

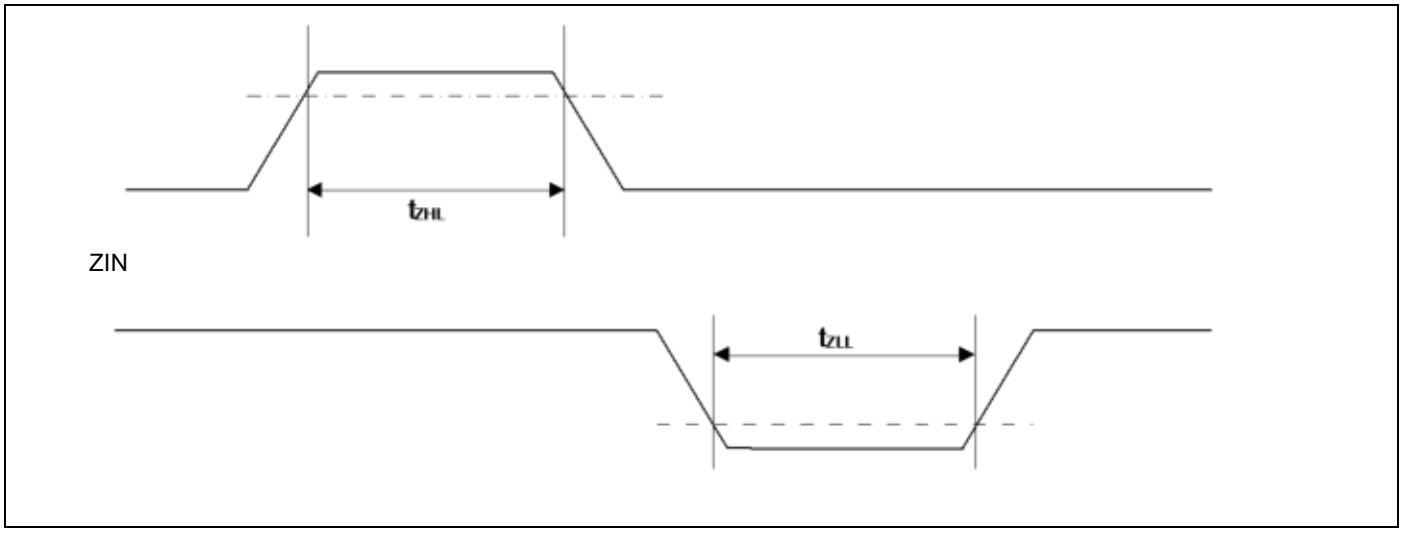
(Vcc = 2.7V to 5.5V, Vss = 0V, T_A = - 40°C to + 85°C)

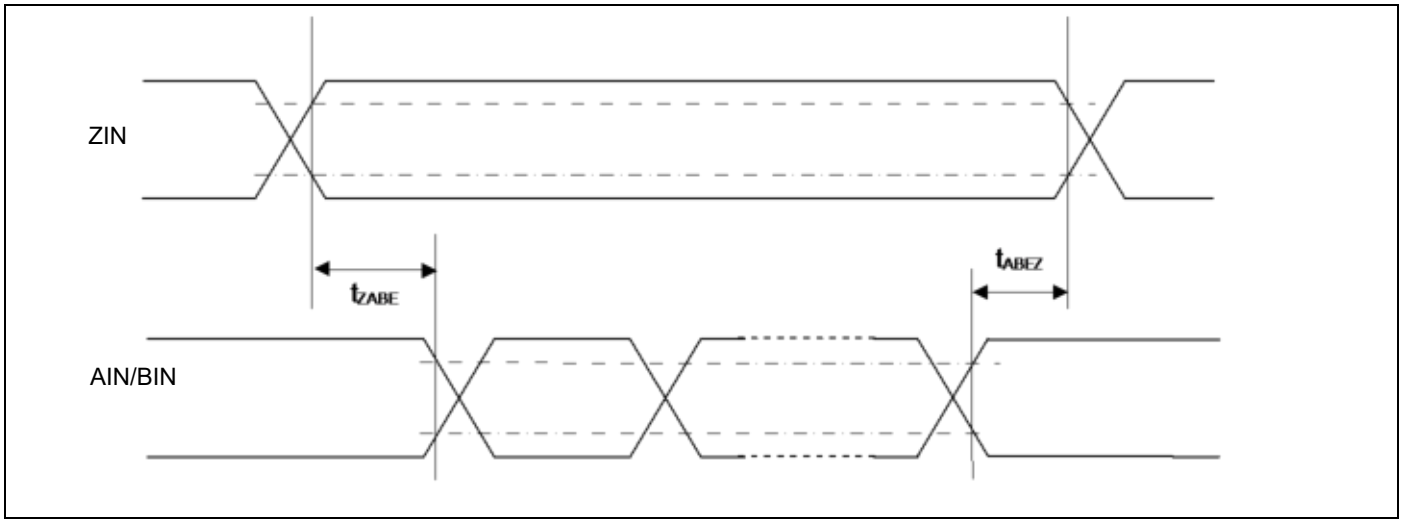
Parameter	Symbol	Conditions	Value		Unit
			Min	Max	
AIN pin "H" width	t_{AHL}	-	$2t_{CYCP}$ *	-	ns
AIN pin "L" width	t_{ALL}	-			
BIN pin "H" width	t_{BHL}	-			
BIN pin "L" width	t_{BLL}	-			
BIN rise time from AIN pin "H" level	t_{AUBU}	PC_Mode2 or PC_Mode3			
AIN fall time from BIN pin "H" level	t_{BUAD}	PC_Mode2 or PC_Mode3			
BIN fall time from AIN pin "L" level	t_{ADBD}	PC_Mode2 or PC_Mode3			
AIN rise time from BIN pin "L" level	t_{BDAU}	PC_Mode2 or PC_Mode3			
AIN rise time from BIN pin "H" level	t_{BUAU}	PC_Mode2 or PC_Mode3			
BIN fall time from AIN pin "H" level	t_{AUBD}	PC_Mode2 or PC_Mode3			
AIN fall time from BIN pin "L" level	t_{BDAD}	PC_Mode2 or PC_Mode3			
BIN rise time from AIN pin "L" level	t_{ADBU}	PC_Mode2 or PC_Mode3			
ZIN pin "H" width	t_{ZHL}	QCR:CGSC="0"			
ZIN pin "L" width	t_{ZLL}	QCR:CGSC="0"			
AIN/BIN rise and fall time from determined ZIN level	t_{ZABE}	QCR:CGSC="1"			
Determined ZIN level from AIN/BIN rise and fall time	t_{ABEZ}	QCR:CGSC="1"			

*: t_{CYCP} indicates the APB bus clock cycle time. About the APB bus number which the Quadrature Position/Revolution Counter is connected to, see "Block Diagram" in this data sheet.




BIN
AIN
tBHL
tBLL
tBUAU
tAUBD
tBDAD
tADBU
tAHL
tALL


ZIN
tZHL
tZLL


ZIN
AIN/BIN
tZABE
tABEZ

12.4.13 I²C timing

(Vcc = 2.7V to 5.5V, Vss = 0V, T_A = - 40°C to + 85°C)

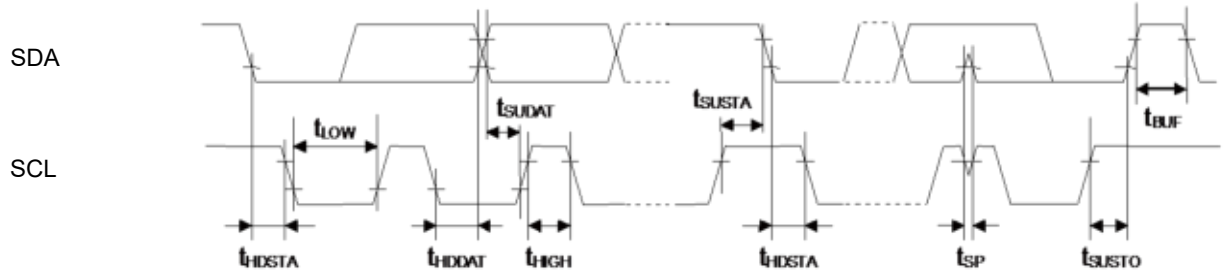
Parameter	Symbol	Conditions	Standard-mode		Fast-mode		Unit	Remarks
			Min	Max	Min	Max		
SCL clock frequency	F_{SCL}	C_L = 50 pF, R = (Vp/I_{OL})*1	0	100	0	400	kHz	
(Repeated) START condition hold time SDA ↓ → SCL ↓	t_{HDSTA}		4.0	-	0.6	-	µs	
SCLclock "L" width	t_{LOW}		4.7	-	1.3	-	µs	
SCLclock "H" width	t_{HIGH}		4.0	-	0.6	-	µs	
(Repeated) START setup time SCL ↑ → SDA ↓	t_{SUSTA}		4.7	-	0.6	-	µs	
Data hold time SCL ↓ → SDA ↓ ↑	t_{HDDAT}		0	3.45*2	0	0.9*3	µs	
Data setup time SDA ↓ ↑ → SCL ↑	t_{SUDAT}		250	-	100	-	ns	
STOP condition setup time SCL ↑ → SDA ↑	t_{SUSTO}		4.0	-	0.6	-	µs	
Bus free time between "STOP condition" and "START condition"	t_{BUF}		4.7	-	1.3	-	µs	
Noise filter	t_{SP}	-	2 t_{CYCP}*4	-	2 t_{CYCP}*4	-	ns	

*1: R and C represent the pull-up resistance and load capacitance of the SCL and SDA lines, respectively.
Vp indicates the power supply voltage of the pull-up resistance and I_{OL} indicates V_{OL} guaranteed current.

*2: The maximum t_{HDDAT} must satisfy that it doesn't extend at least "L" period (t_{LOW}) of device's SCL signal.

*3: Fast-mode I²C bus device can be used on Standard-mode I²C bus system as long as the device satisfies the requirement of "t_{SUDAT} ≥ 250 ns".

*4: t_{CYCP} is the APB bus clock cycle time.
About the APB bus number that I²C is connected to, see "Block Diagram" in this data sheet.
To use Standard-mode, set the APB bus clock at 2 MHz or more.
To use Fast-mode, set the APB bus clock at 8 MHz or more.



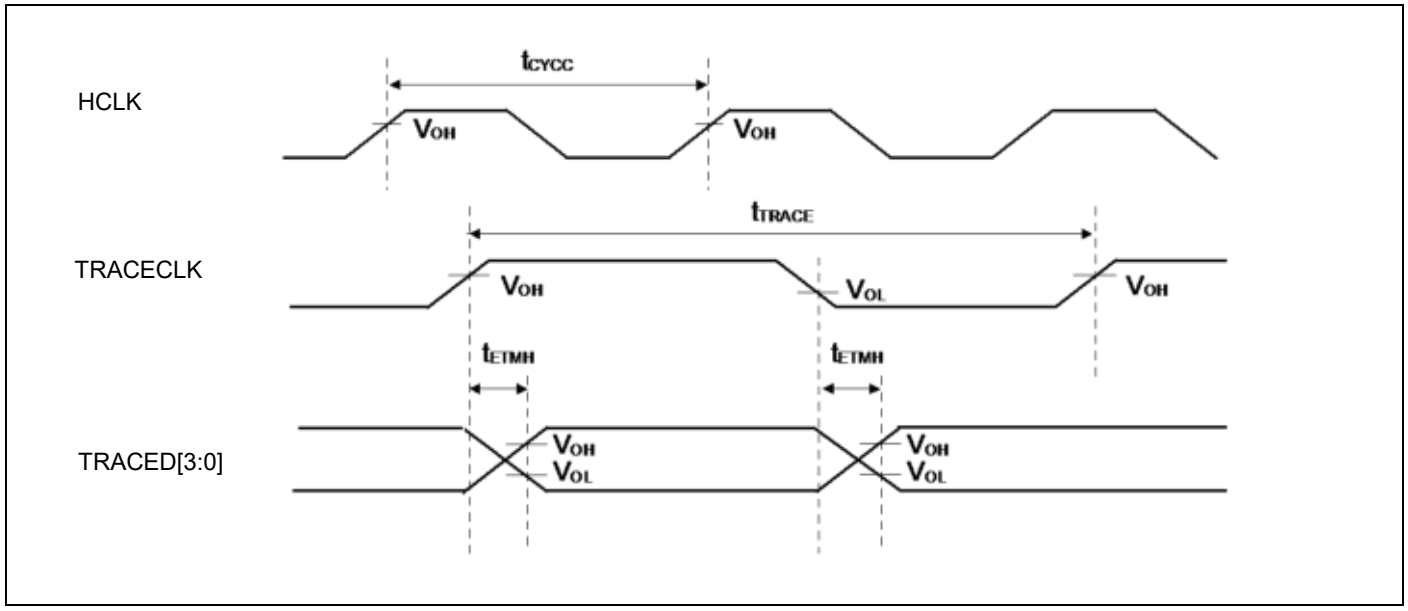
12.4.14 ETM timing

(Vcc = 2.7V to 5.5V, Vss = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Data hold	t_{ETMH}	TRACECLK TRACED3 - 0	Vcc ≥ 4.5 V	2	9	ns	
			Vcc < 4.5 V	2	15		
TRACECLK Frequency	$1/t_{TRACE}$	TRACECLK	Vcc ≥ 4.5 V	-	50	MHz	
			Vcc < 4.5 V	-	32	MHz	
TRACECLK clock cycle time	t_{TRACE}		Vcc ≥ 4.5 V	20	-	ns	
			Vcc < 4.5 V	31.25	-	ns	

Note:

– *When the external load capacitance C_L = 50 pF.*



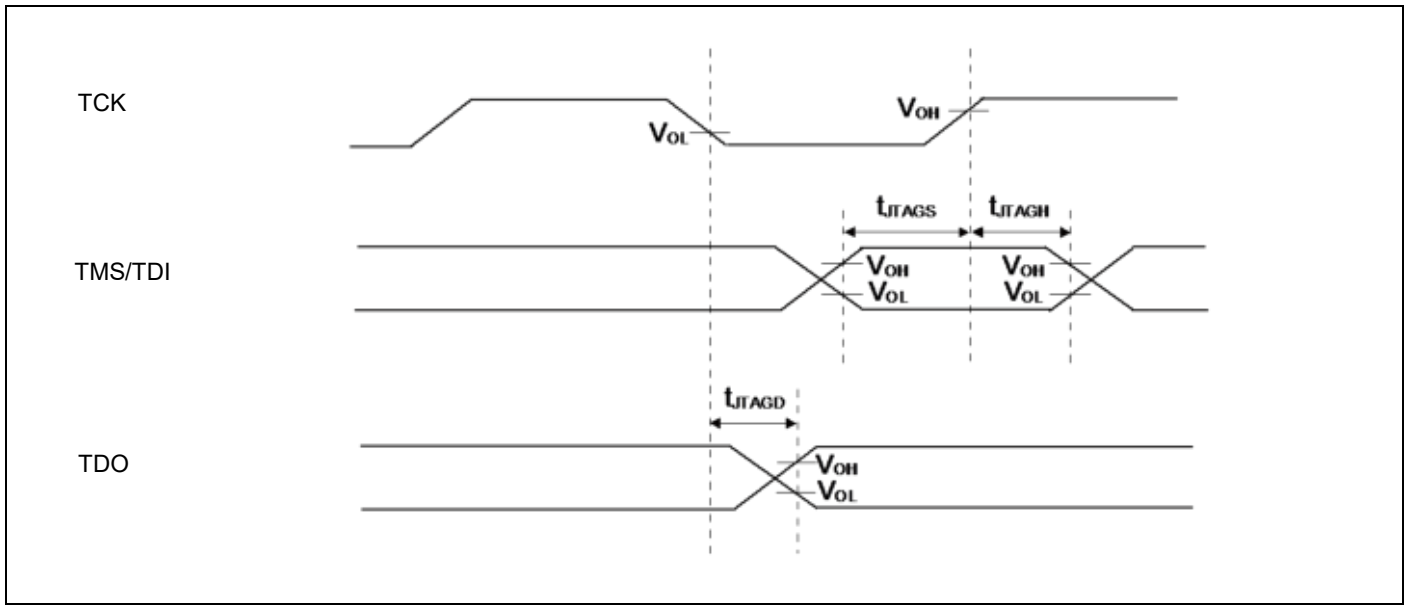
12.4.15 JTAG timing

(Vcc = 2.7V to 5.5V, Vss = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
TMS,TDI setup time	t_{JTAGS}	TCK TMS,TDI	Vcc ≥ 4.5 V	15	-	ns	
			Vcc < 4.5 V				
TMS,TDI hold time	t_{JTAGH}	TCK TMS,TDI	Vcc ≥ 4.5 V	15	-	ns	
			Vcc < 4.5 V				
TDO delay time	t_{JTAGD}	TCK TDO	Vcc ≥ 4.5 V	-	25	ns	
			Vcc < 4.5 V	-	45		

Note:

- *When the external load capacitance C_L = 50 pF.*



12.5 12-bit A/D Converter

Electrical characteristics for the A/D converter.

(Vcc = AVcc = 2.7V to 5.5V, Vss = AVss = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	12	bit	
Integral Nonlinearity	-	-	-	± 2	± 4.5	LSB	AVRH = 2.7 V to 5.5 V
Differential Nonlinearity	-	-	-	± 2	± 2.5	LSB	
Zero transition voltage	V_{ZT}	ANxx	-	± 5	± 20	mV	
Full-scale transition voltage	V_{FST}	ANxx	-	AVRH ± 10	AVRH ± 20	mV	
Conversion time	-	-	1.0*1	-	-	µs	AVcc ≥ 4.5 V
			2.666*1	-	-		AVcc < 4.5 V
Sampling time	Ts	-	*2	-	-	ns	AVcc ≥ 4.5 V
			*2	-	-		AVcc < 4.5 V
Compare clock cycle *3	Tcck	-	55.5	-	10000	ns	AVcc ≥ 4.5 V
			166.6*4				AVcc < 4.5 V
State transition time to operation permission	Tstt	-	-	-	2.5	µs	
Analog input capacity	C_{AIN}	-	-	-	14.5	pF	
Analog input resistance	R_{AIN}	-	-	-	0.93	kΩ	AVcc ≥ 4.5 V
					2.04		AVcc < 4.5 V
Interchannel disparity	-	-	-	-	4	LSB	
Analog port input leak current	-	ANxx	-	-	5	µA	
Analog input voltage	-	ANxx	AV_{SS}	-	AVRH	V	
Reference voltage	-	AVRH	2.7	-	AV_{CC}	V	

*1: The Conversion time is the value of sampling time (Ts) + compare time (Tc).

The condition of the minimum conversion time is the following.

AVcc ≥ 4.5 V, HCLK = 72 MHz sampling time: 0.222 µs compare time: 0.778 µs
AVcc < 4.5 V, HCLK = 54 MHz sampling time: 0.333 µs compare time: 2.333 µs

Ensure that it satisfies the value of the sampling time (Ts) and compare clock cycle (Tcck).
For setting of the sampling time and compare clock cycle, see "CHAPTER 1-1: A/D Converter" in "FM3 Family PERIPHERAL MANUAL Analog Macro Part".

The registers setting of the A/D Converter are reflected in the operation according to the APB bus clock timing.

The sampling clock and compare clock is generated from the Base clock (HCLK).

About the APB bus number which the A/D Converter is connected to, see "Block Diagram" in this data sheet.

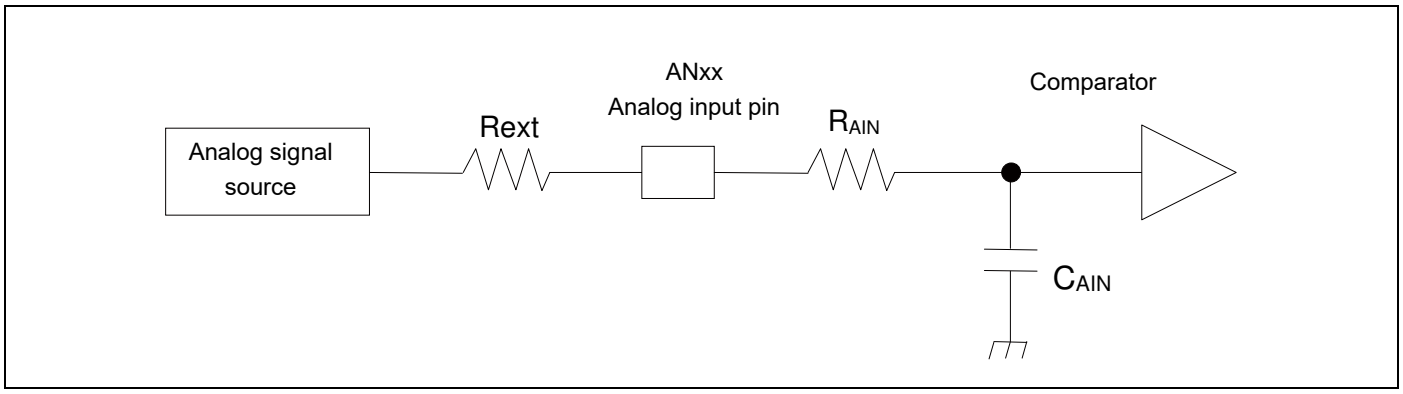
*2: A necessary sampling time changes by external impedance.

Ensure that it set the sampling time to satisfy (Equation 1)

*3: The Compare time (Tc) is the value of (Equation 2)

*4: When 12-bit A/D converter is used at AVcc<4.5 V, there is a limitation as follows.

Please set the HCLK frequency under 54 MHz.



(Equation 1) Ts ≥ (R_{AIN} + Rext) × C_{AIN} × 9

Ts: Sampling time

R_{AIN}: Input resistance of A/D = 0.93kΩ 4.5 V ≤ AV_{CC} ≤ 5.5 V

Input resistance of A/D = 2.04kΩ 2.7 V ≤ AV_{CC} < 4.5 V

C_{AIN}: Input capacity of A/D = 14.5pF 2.7 V ≤ AV_{CC} ≤ 5.5 V

Rext: Output impedance of external circuit

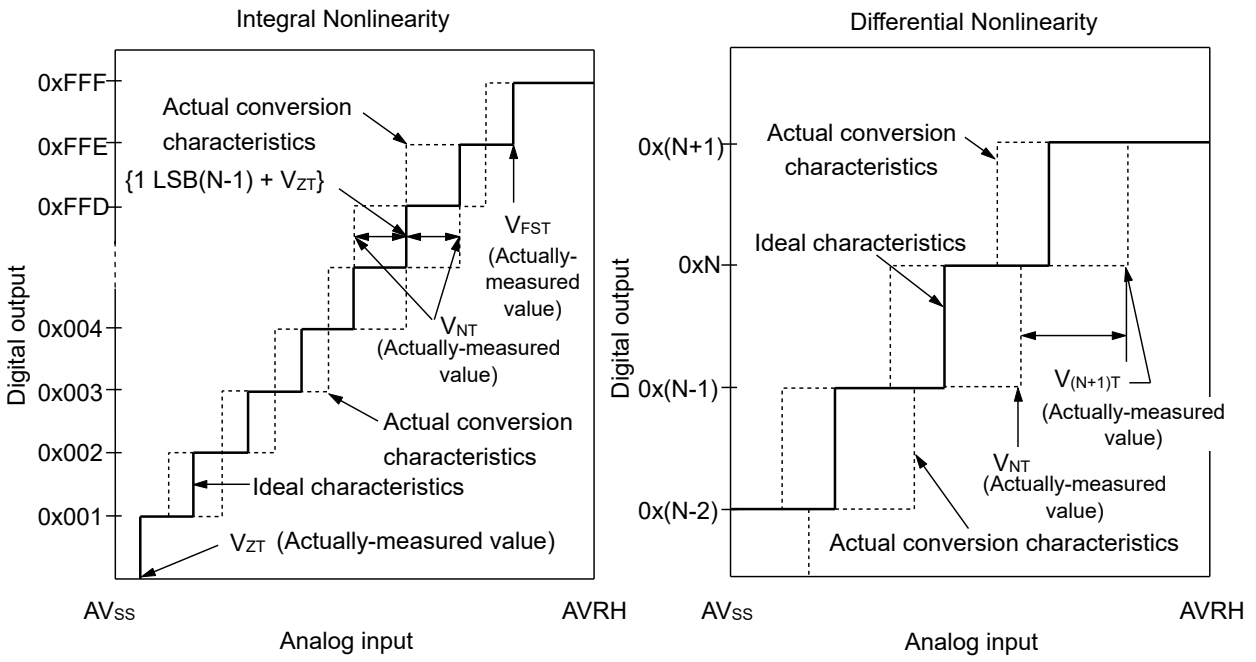
(Equation 2) Tc = Tcck × 14

Tc: Compare time

Tcck: Compare clock cycle

Definition of 12-bit A/D Converter Terms

- Resolution: Analog variation that is recognized by an A/D converter.
- Integral Nonlinearity: Deviation of the line between the zero-transition point (0b000000000000 ⟷ 0b000000000001) and the full-scale transition point (0b111111111110 ⟷ 0b111111111111) from the actual conversion characteristics.
- Differential Nonlinearity: Deviation from the ideal value of the input voltage that is required to change the output code by 1 LSB.



$$\text{Integral Nonlinearity of digital output N} = \frac{V_{NT} - \{1LSB \times (N - 1) + V_{ZT}\}}{1LSB} \text{ [LSB]}$$

$$\text{Differential Nonlinearity of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1LSB} - 1 \text{ [LSB]}$$

$$1LSB = \frac{V_{FST} - V_{ZT}}{4094}$$

N: A/D converter digital output value.
V_{ZT}: Voltage at which the digital output changes from 0x000 to 0x001.
V_{FST}: Voltage at which the digital output changes from 0xFFE to 0xFFF.
V_{NT}: Voltage at which the digital output changes from 0x(N − 1) to 0xN.

12.6 Low-Voltage Detection Characteristics

12.6.1 Low-Voltage Detection Reset

(T_A = - 40°C to + 85°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	-	2.20	2.40	2.60	V	When voltage drops
Released voltage	VDH	-	2.30	2.50	2.70	V	When voltage rises

12.6.2 Interrupt of Low-Voltage Detection

(T_A = - 40°C to + 85°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	SVHI = 0000	2.58	2.8	3.02	V	When voltage drops
Released voltage	VDH		2.67	2.9	3.13	V	When voltage rises
Detected voltage	VDL	SVHI = 0001	2.76	3.0	3.24	V	When voltage drops
Released voltage	VDH		2.85	3.1	3.34	V	When voltage rises
Detected voltage	VDL	SVHI = 0010	2.94	3.2	3.45	V	When voltage drops
Released voltage	VDH		3.04	3.3	3.56	V	When voltage rises
Detected voltage	VDL	SVHI = 0011	3.31	3.6	3.88	V	When voltage drops
Released voltage	VDH		3.40	3.7	3.99	V	When voltage rises
Detected voltage	VDL	SVHI = 0100	3.40	3.7	3.99	V	When voltage drops
Released voltage	VDH		3.50	3.8	4.10	V	When voltage rises
Detected voltage	VDL	SVHI = 0111	3.68	4.0	4.32	V	When voltage drops
Released voltage	VDH		3.77	4.1	4.42	V	When voltage rises
Detected voltage	VDL	SVHI = 1000	3.77	4.1	4.42	V	When voltage drops
Released voltage	VDH		3.86	4.2	4.53	V	When voltage rises
Detected voltage	VDL	SVHI = 1001	3.86	4.2	4.53	V	When voltage drops
Released voltage	VDH		3.96	4.3	4.64	V	When voltage rises
LVD stabilization wait time	T_{LVDW}	-	-	-	2040 × t_{CYCP} *	µs	

*: t_{CYCP} indicates the APB2 bus clock cycle time.

12.7 Flash Memory Write/Erase Characteristics

12.7.1 Write / Erase time

(Vcc = 2.7V to 5.5V, T_A = - 40°C to + 85°C)

Parameter		Value		Unit	Remarks
		Typ*	Max*		
Sector erase time	Large Sector	1.6	7.5	s	Includes write time prior to internal erase
	Small Sector	0.4	2.1		
Half word (16 bit) write time		25	400	µs	Not including system-level overhead time.
Chip erase time		16	76.8	s	Includes write time prior to internal erase

*: The typical value is immediately after shipment, the maximum value is guarantee value under 100,000 cycle of erase/write.

12.7.2 Erase/write cycles and data hold time

Erase/write cycles (cycle)	Data hold time (year)	Remarks
1,000	20 *	
10,000	10 *	
100,000	5 *	

*: At average + 85°C

12.8 Return Time from Low-Power Consumption Mode

12.8.1 Return Factor: Interrupt

The return time from Low-Power consumption mode is indicated as follows. It is from receiving the return factor to starting the program operation.

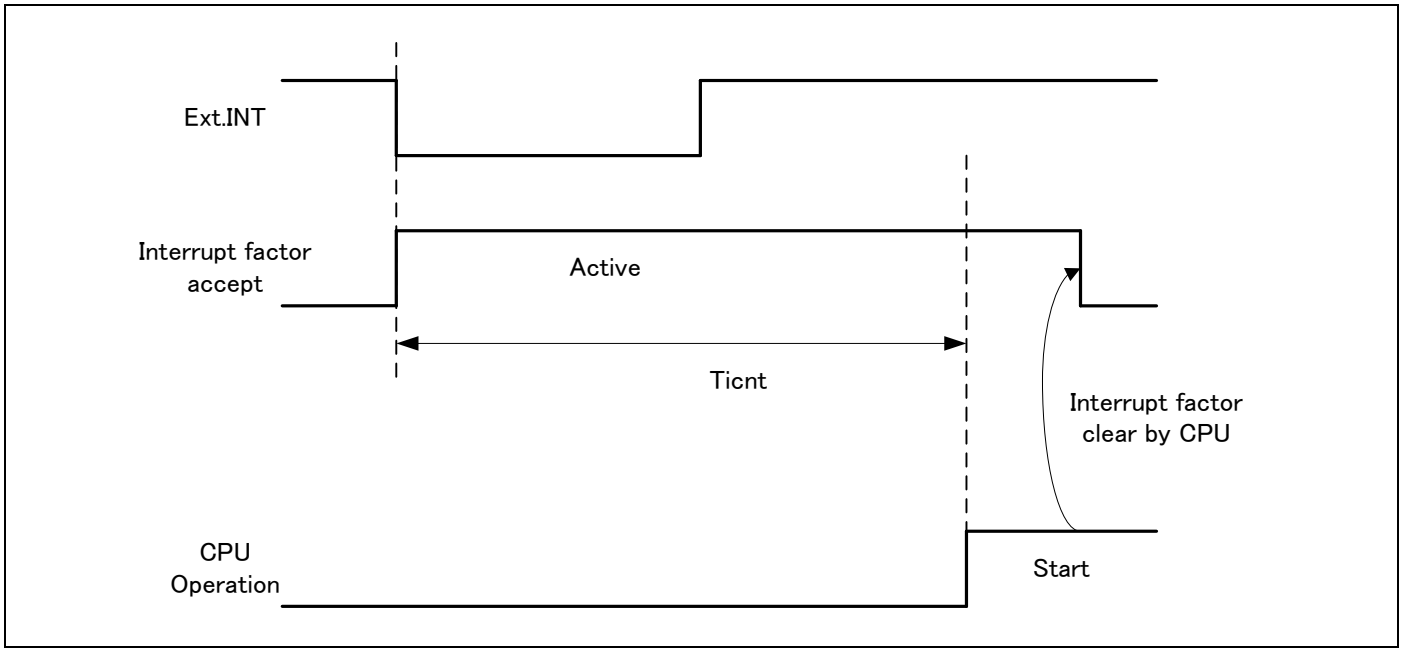
Return Count Time

(V_{CC} = 2.7V to 5.5V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Value		Unit	Remarks
		Typ	Max*		
SLEEP mode	Ticnt	t_{CYCC}		ns	
High-speed CR TIMER mode, Main TIMER mode, PLL TIMER mode		33	100	µs	
Low-speed CR TIMER mode		445	1061	µs	
Sub TIMER mode		445	1061	µs	
STOP mode		445	1061	µs	

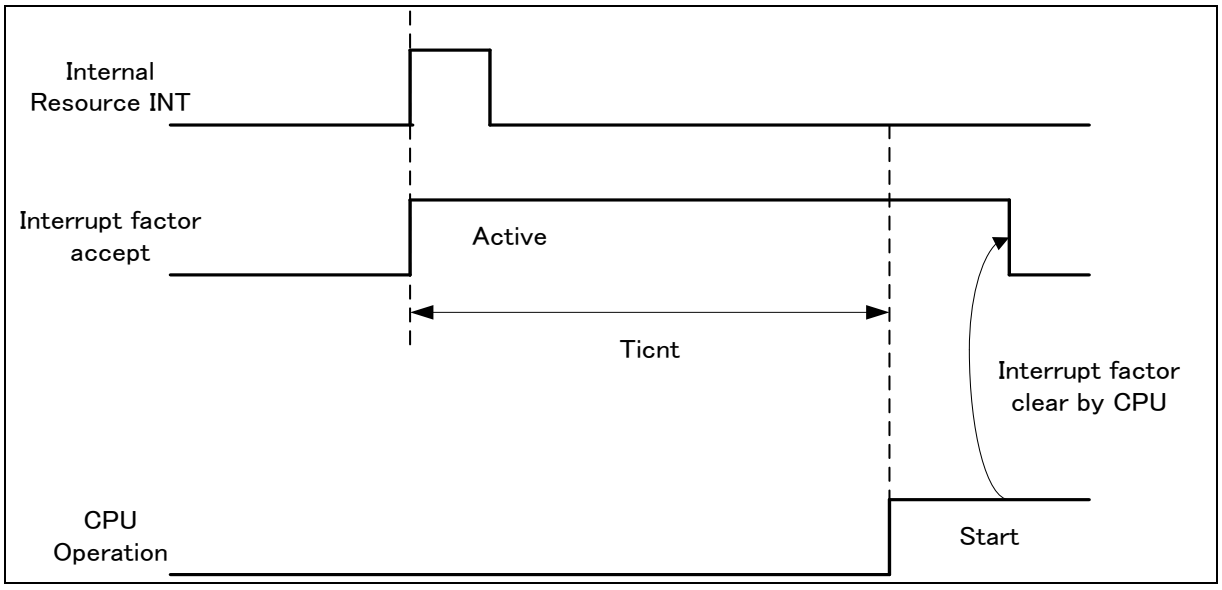
*: The maximum value depends on the accuracy of built-in CR.

Operation example of return from Low-Power consumption mode (by external interrupt*)



*: External interrupt is set to detecting fall edge.

Operation example of return from Low-Power consumption mode (by internal resource interrupt*)



*: Internal resource interrupt is not included in return factor by the kind of Low-Power consumption mode.

Notes:

- *The return factor is different in each Low-Power consumption modes. See "CHAPTER 6: Low Power Consumption Mode" and "Operations of Standby Modes" in FM3 Family PERIPHERAL MANUAL about the return factor from Low-Power consumption mode.*
- *When interrupt recoveries, the operation mode that CPU recoveries depends on the state before the Low-Power consumption mode transition. See "CHAPTER 6: Low Power Consumption Mode" in "FM3 Family PERIPHERAL MANUAL".*

12.8.2 Return Factor: Reset

The return time from Low-Power consumption mode is indicated as follows. It is from releasing reset to starting the program operation.

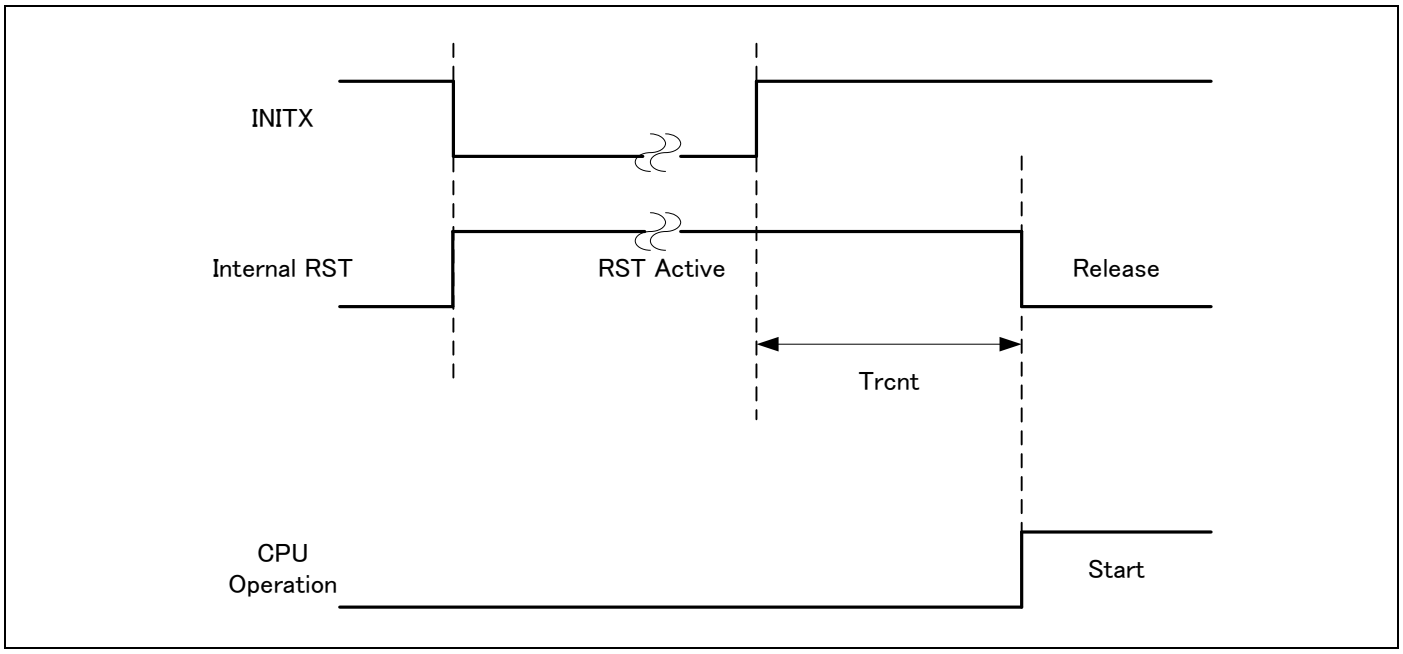
Return Count Time

(V_{CC} = 2.7V to 5.5V, T_A = - 40°C to + 85°C)

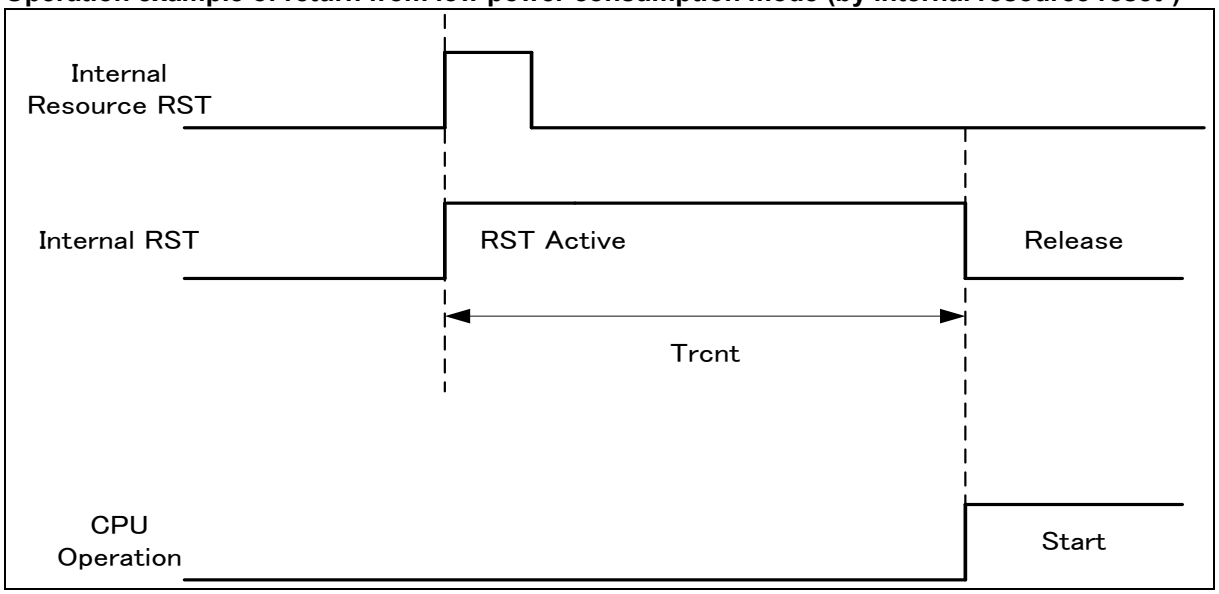
Parameter	Symbol	Value		Unit	Remarks
		Typ	Max*		
SLEEP mode	Trcnt	82	181	µs	
High-speed CR TIMER mode, Main TIMER mode, PLL TIMER mode		82	181	µs	
Low-speed CR TIMER mode		431	1003	µs	
Sub TIMER mode		431	1003	µs	
STOP mode		431	1003	µs	

*: The maximum value depends on the accuracy of built-in CR.

Operation example of return from Low-Power consumption mode (by INITX)



Operation example of return from low power consumption mode (by internal resource reset*)



*: Internal resource reset is not included in return factor by the kind of Low-Power consumption mode.

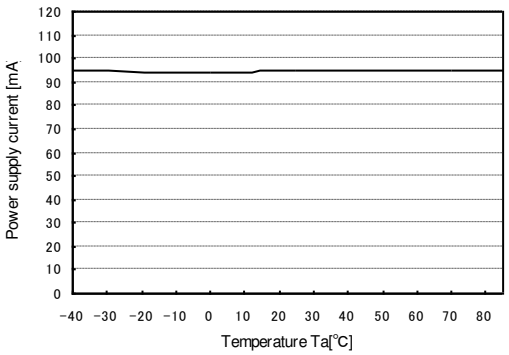
Notes:

- *The return factor is different in each Low-Power consumption modes. See "CHAPTER 6: Low Power Consumption Mode" and "Operations of Standby Modes" in FM3 Family PERIPHERAL MANUAL.*
- *When interrupt recoveries, the operation mode that CPU recoveries depends on the state before the Low-Power consumption mode transition. See "CHAPTER 6: Low Power Consumption Mode" in "FM3 Family PERIPHERAL MANUAL".*
- *The time during the power-on reset/low-voltage detection reset is excluded. See "(6) Power-on Reset Timing in 4. AC Characteristics in ELECTRICAL CHARACTERISTICS" for the detail on the time during the power-on reset/low -voltage detection reset.*
- *When in recovery from reset, CPU changes to the high-speed CR run mode. When using the main clock or the PLL clock, it is necessary to add the main clock oscillation stabilization wait time or the main PLL clock stabilization wait time.*
- *The internal resource reset means the watchdog reset and the CSV reset.*

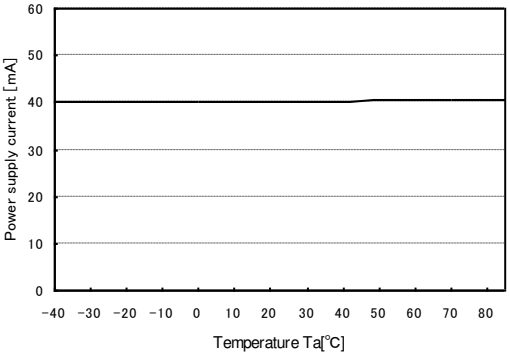
13. Example of Characteristic

Power supply current (PLL run mode, PLL sleep mode)

Icc normal operation(PLL) temperature characteristics
Vcc:5.5V, CPU:80MHz, Peripheral:40MHz,FLASH 2Wait

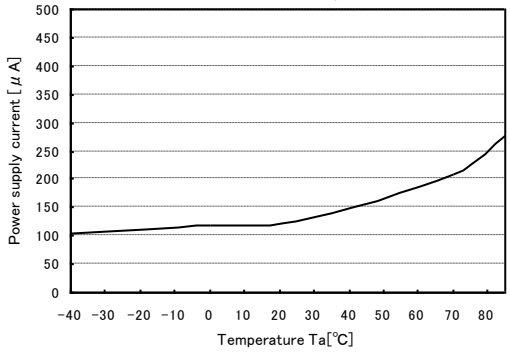


Iccs sleep operation(PLL) temperature characteristics
Vcc:5.5V, Peripheral:40MHz

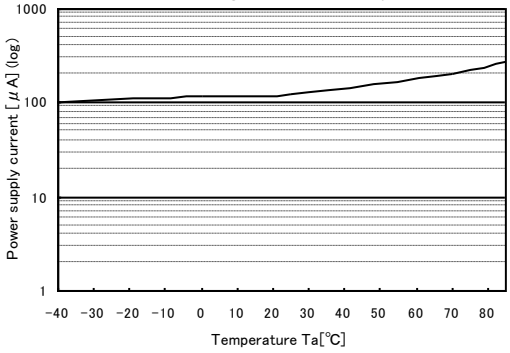


Power supply current (Sub run mode)

Icc normal operation(sub oscillation) temperature
characteristics Vcc:5.5V, CPU/Peripheral:32KHz

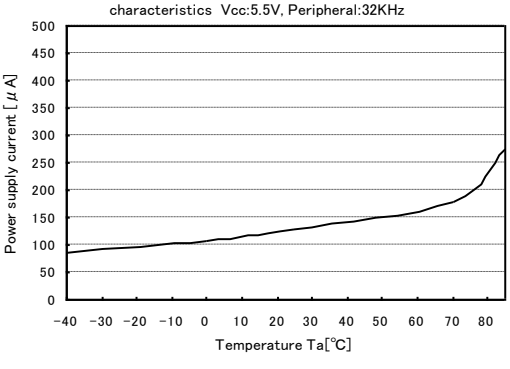


Icc normal operation(sub oscillation) temperature
characteristics(semi-log) Vcc:5.5V, CPU/Peripheral:32KHz

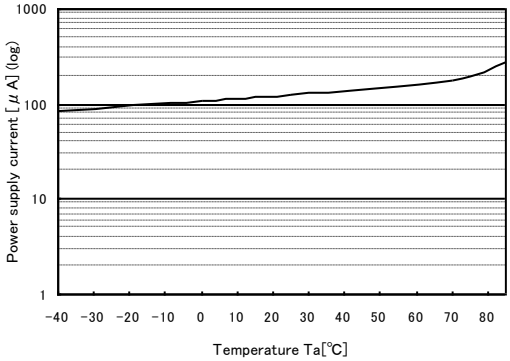


Power supply current (Sub sleep mode)

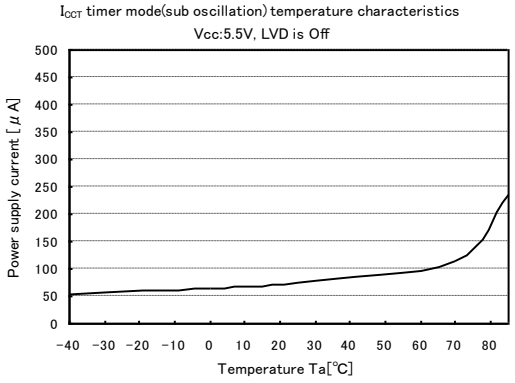
Iccs sleep operation(sub oscillation) temperature
characteristics Vcc:5.5V, Peripheral:32KHz

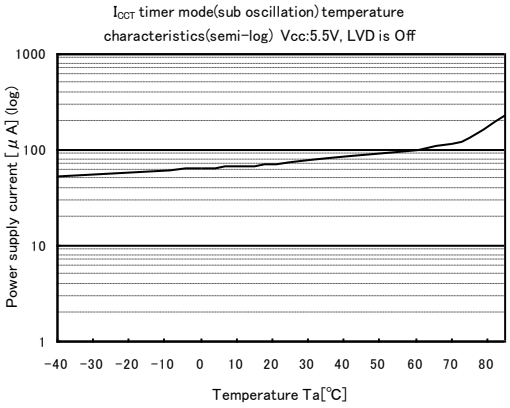


Iccs sleep operation(sub oscillation) temperature
characteristics(semi-log) Vcc:5.5V, Peripheral:32KHz

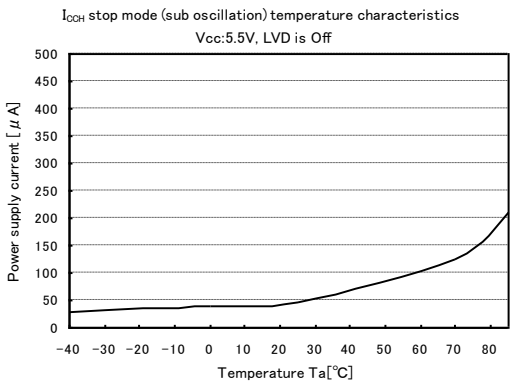


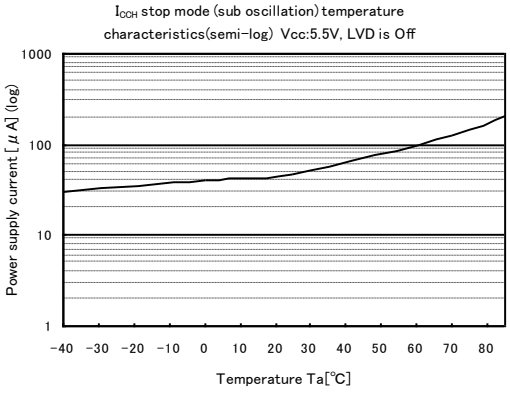
Power supply current (Sub timer mode)





Power supply current (Stop mode)



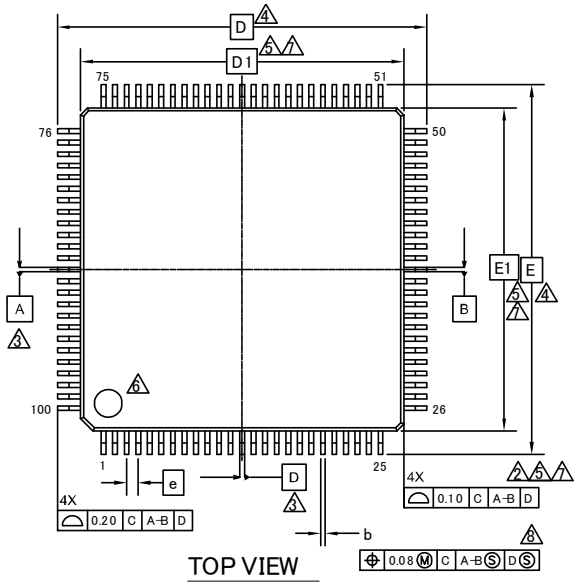


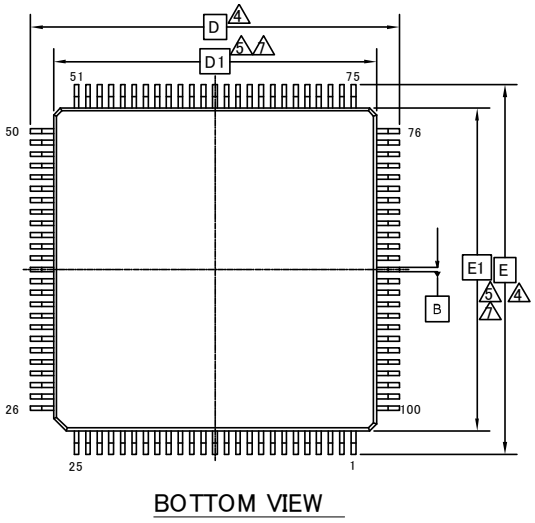
14. Ordering Information

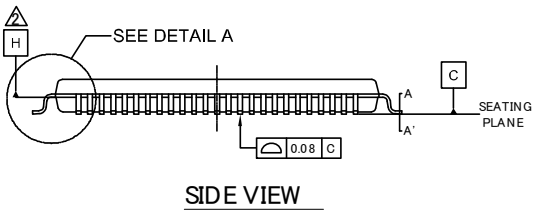
Part Number	On-chip Flash Memory	On-chip SRAM	Package	Packing
CY9BF102NAPMC-G-JNE2	128 Kbyte	16 Kbyte	Plastic・LQFP(0.5mm pitch),100-pin (LQI100)	Tray
CY9BF104NAPMC-G-JNE2	256 Kbyte	32 Kbyte		
CY9BF104NAPMC-G-UNE1				
CY9BF105NAPMC-G-JNE2	384 Kbyte	48 Kbyte		
CY9BF106NAPMC-G-UNE1	512 Kbyte	64 Kbyte		
CY9BF106NAPMC-G-UNE2				
CY9BF102RAPMC-G-JNE2	128 Kbyte	16 Kbyte	Plastic・LQFP(0.5mm pitch),120-pin (LQM120)	
CY9BF104RAPMC-G-JNE2	256 Kbyte	32 Kbyte		
CY9BF105RAPMC-G-JNE2	384 Kbyte	48 Kbyte		
CY9BF106RAPMC-G-UNE1	512 Kbyte	64 Kbyte		
CY9BF106RAPMC-G-UNE2				
CY9BF102NABGL-GK6E1	128 Kbyte	16 Kbyte	Plastic・PFBGA(0.8mm pitch),112-pin (LBC112)	
CY9BF104NABGL-GK6E1	256 Kbyte	32 Kbyte		
CY9BF105NABGL-GK6E1	384 Kbyte	48 Kbyte		
CY9BF106NABGL-GK6E1	512 Kbyte	64 Kbyte		

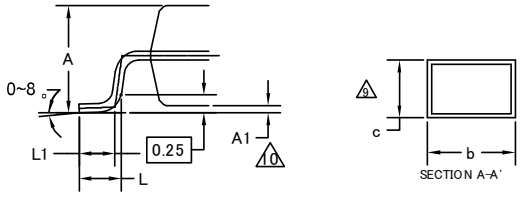
15. Package Dimensions

Package Type	Package Code
LQFP 100	LQI100









SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.05	—	0.15
b	0.15	—	0.27
c	0.09	—	0.20
D	16.00 BSC		
D1	14.00 BSC		
e	0.50 BSC		
E	16.00 BSC		
E1	14.00 BSC		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70

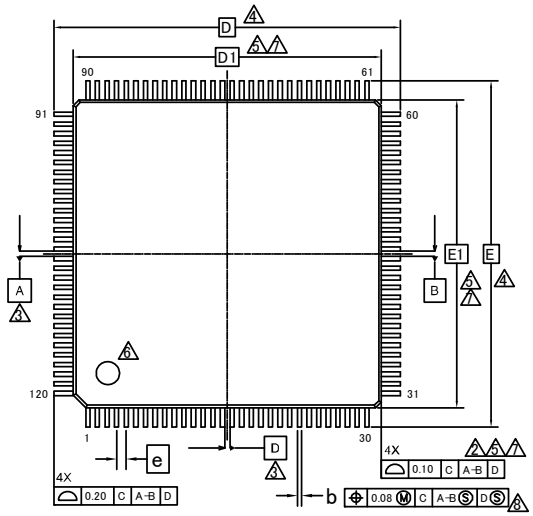
NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

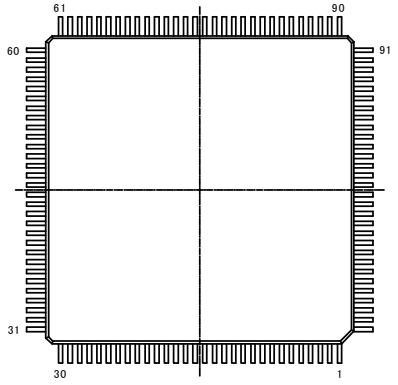
PACKAGE OUTLINE, 100 LEAD LQFP
14.0X14.0X1.7 MM LQI100 REV*A

002-11500 *A

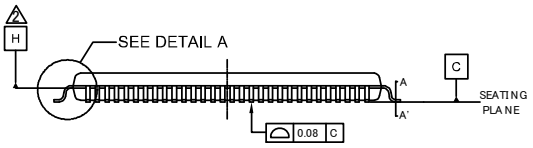
Package Type	Package Code
LQFP 120	LQM120



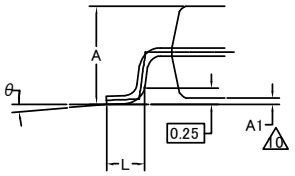
TOP VIEW



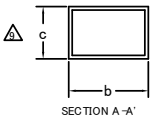
BOTTOM VIEW



SIDE VIEW



DETAIL A



SECTION A-A'

SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.05	—	0.15
b	0.17	0.22	0.27
c	0.115	—	0.195
D		18.00 BSC	
D1		16.00 BSC	
e		0.50 BSC	
E		18.00 BSC	
E1		16.00 BSC	
L	0.45	0.60	0.75
θ	0°	—	8°

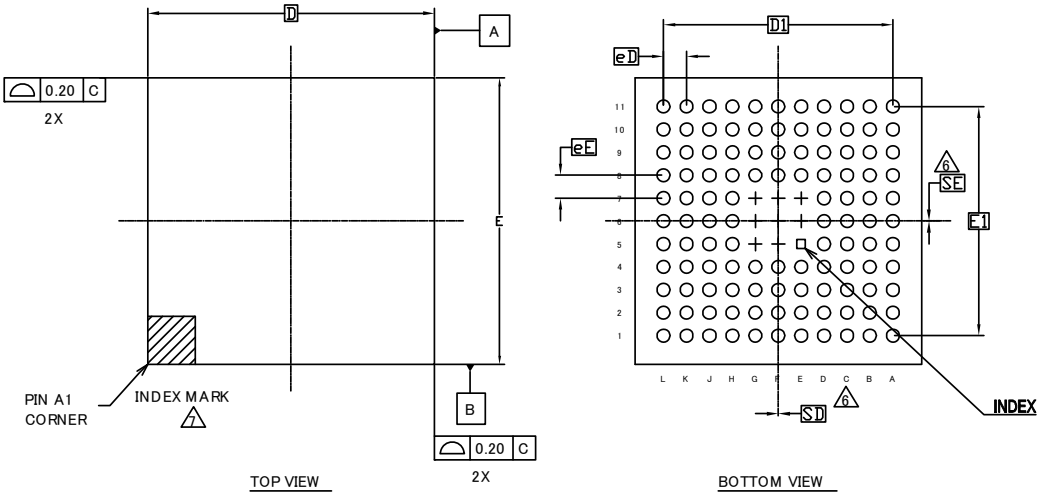
NOTES

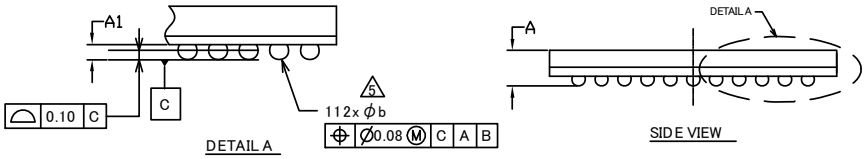
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
11. JEDEC SPECIFICATION NO. REF: N/A.

PACKAGE OUTLINE, 120 LEAD LQFP
18.0X18.0X1.7 MM LQM120 REV**

002-16172 **

Package Type	Package Code
PFBGA 112	LBC112





SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	–	–	1.45
A1	0.25	0.35	0.45
D	10.00 BSC		
E	10.00 BSC		
D1	8.00 BSC		
E1	8.00 BSC		
MD	11		
ME	11		
N	112		
Ø b	0.35	0.45	0.55
eD	0.80 BSC		
eE	0.80 BSC		
SD	0.00		
SE	0.00		

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. SOLDER BALL POSITION DESIGNATIO N PER JEP95, SECTION 3, SPP-020.
3. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
4. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
5. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
6. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
7. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK METALIZED MARK, INDENTATION OR OTHER MEANS.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED SOLDER BALLS.

002-13225 **

PACKAGE OUTLINE, 112 BALL FBGA
10.00X10.00X1.45 MM LBC112 REV**

16. Errata

This chapter describes the errata for CY9B100R series. Details include errata trigger conditions, scope of impact, available workaround, and silicon revision applicability.

Contact your local Cypress Sales Representative if you have questions.

16.1 Part Numbers Affected

Part Number
Initial Revision
CY9BF102RPMC-G-JNE2, CY9BF104RPMC-G-JNE2, CY9BF105RPMC-G-JNE2, CY9BF106RPMC-G-JNE2, CY9BF102NPMC-G-JNE2, CY9BF104NPMC-G-JNE2, CY9BF105NPMC-G-JNE2, CY9BF106NPMC-G-JNE2, CY9BF102NBGL-GE1, CY9BF104NBGL-GE1, CY9BF105NBGL-GE1, CY9BF106NBGL-GE1

16.2 Qualification Status

Product Status: In Production − Qual.

16.3 Errata Summary

This table defines the errata applicability to available devices.

Items	Part Number	Silicon Revision	Fix Status
[1] Timer and Stop Mode Issue	Refer to 16.1	Rev. initial rev.	Fixed in Rev. A
[2] Gap Between Watch Counter Value and Real Time at Return in Timer Mode	Refer to 16.1	Rev. initial rev.	Fixed in Rev. A

16.4 Errata Detail

16.4.1 Timer and Stop Mode Issue

■PROBLEM DEFINITION
MCU does not return form timer or stop mode.

■PARAMETERS AFFECTED
N/A

■TRIGGER CONDITION(S)
The condition is that the timing of entering timer or stop mode and an interruption occurrence meet.

■SCOPE OF IMPACT
MCU does not return from time or stop mode.

■WORKAROUND
This error cannot be avoided by any software, except not using timer and stop mode.

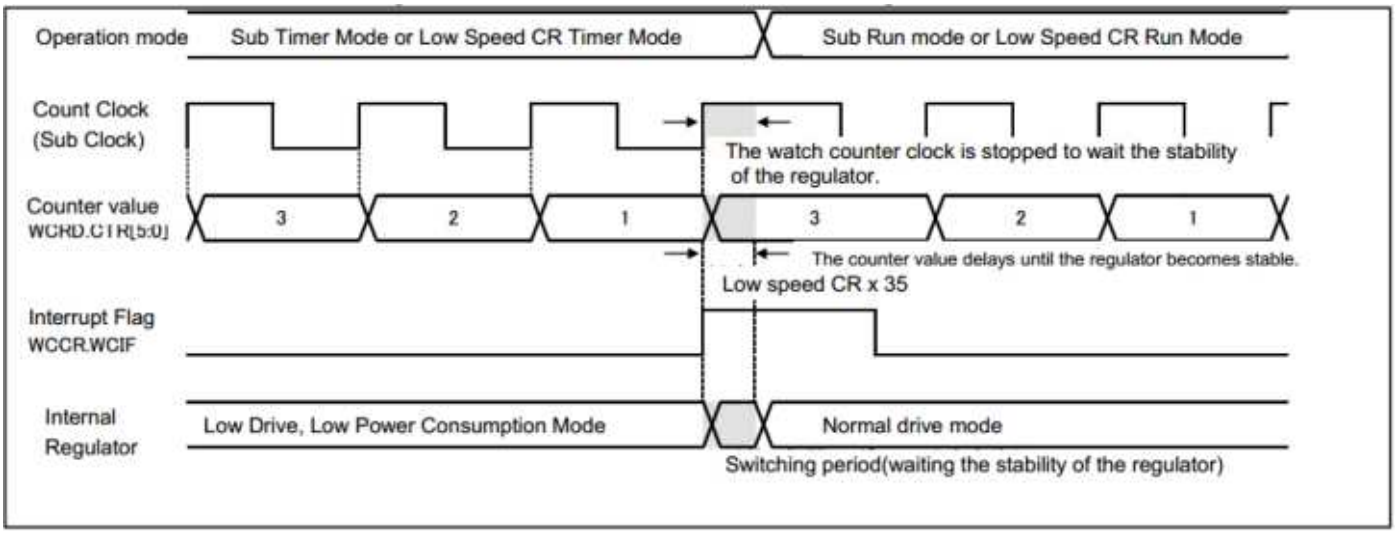
■FIX STATUS
This issue was fixed in Rev. A.

16.4.2 Gap Between Watch Counter Value and Real Time at Return in Timer Mode

■ PROBLEM DEFINITION

There is a gap between the value of the counter and the real time at the return by the interrupt in the sub-timer mode or the low speed CR timer mode. When the watch counter using the sub-crystal oscillator is used in the sub timer mode or the low speed CR timer mode, the value of the watch counter has a “Low speed CR x 35 clock” delay (about 350µs at waiting for the stability of the regulator) at the return by the interrupt. As a result, a gap occurs between the value of the counter and the real time.

The following figure shows the timing waveform.



■ ROOT CAUSE

The internal regulator operates with low drive and low power consumption in the sub timer mode or the low speed CR timer mode.

When the interrupt is requested, the mode of the internal regulator is switched to the normal drive mode. At this time, a switching time for the stability of the regulator is required.

This MCU is designed for keeping down the voltage variation of the regulator by reducing the current. To achieve it, the clock to the watch counter is stopped in the period.

At a result, the value of the watch counter delay until the time for the stability of the regulator is shown in the Figure. Therefore, a gap occurs between the value of the counter and the real time.

■ TRIGGER CONDITION(S)

When both of (1) and (2) described below is applicable, the gap occurs.

(1) CPU Operation Mode

The gap occurs in the sub timer mode or the low speed CR mode.

It does not occur in the following modes:

- Run modes (PLL, main, high speed CR, sub, and low speed CR)
- Sleep modes (PLL, main, high speed CR, sub, low speed CR)
- PLL timer mode
- Main timer mode
- High speed CR timer mode
- Stop mode

(2) Return Factor

The gap occurs when any of the following interrupt is requested for the return in the sub timer mode or the low speed CR timer mode.

- NMI interrupt

- External interrupt
- Hardware Watchdog Timer interrupt
- USB Wakeup interrupt
- Watch Counter interrupt
- Low-voltage detection interrupt
- The gap does not occur in the standby return by the reset because the value of the counter is cleared

■ WORKAROUND

When the extremely accuracy is required for the count time of the watch counter, use the sub sleep mode or the low speed CR sleep mode.

■FIX STATUS

This issue was fixed in Rev. A.

17. Major Changes

Spansion Publication Number: DS706-00020

Page	Section	Change Results
Revision 1.0		
-	-	Initial release
Revision 1.1		
-	-	Company name and layout design change
Revision 2.0		
3	FEATURES External Bus Interface	Added the description of Maximum area size
8	PACKAGES	Deleted the description of ES
17	LIST OF PIN FUNCTIONS · List of pin numbers	Modified the Pin state type of P4E from I to H
32-35	LIST OF PIN FUNCTIONS · List of pin functions	Added LIN to the description of SOTxx
42	I/O CIRCUIT TYPE	Added the description of I^2C to the type of E and F
42, 43	I/O CIRCUIT TYPE	Added about +B input
48	HANDLING DEVICES	Added "Stabilizing power supply voltage"
48	HANDLING DEVICES Crystal oscillator circuit	Added the following description "Evaluate oscillation of your using crystal oscillator by your mount board."
49	HANDLING DEVICES C Pin	Changed the description
50	BLOCK DIAGRAM	Modified the block diagram
50	MEMORY SIZE	Changed to the following description See "Memory size" in "PRODUCT LINEUP" to confirm the memory size.
51	MEMORY MAP · Memory map(1)	Modified the area of "External Device Area"
52	MEMORY MAP · Memory map(2)	Added the summary of Flash memory sector and the note
59, 60	ELECTRICAL CHARACTERISTICS 1. Absolute Maximum Ratings	· Added the Clamp maximum current · Added the output current of P80 and P81 · Added about +B input
61	ELECTRICAL CHARACTERISTICS 2. Recommended Operation Conditions	· Modified the minimum value of Analog reference voltage · Added Smoothing capacitor · Added the note about less than the minimum power supply voltage
62, 63	ELECTRICAL CHARACTERISTICS 3. DC Characteristics (1) Current rating	· Changed the table format · Added Main TIMER mode current · Added Flash Memory Current · Moved A/D Converter Current
65	ELECTRICAL CHARACTERISTICS 4. AC Characteristics (1) Main Clock Input Characteristics	Added Master clock at Internal operating clock frequency
66	ELECTRICAL CHARACTERISTICS 4. AC Characteristics (3) Built-in CR Oscillation Characteristics	Added Frequency stability time at Built-in high-speed CR
67	ELECTRICAL CHARACTERISTICS 4. AC Characteristics (4-1)(4-2) Operating Conditions of Main PLL	· Added Main PLL clock frequency · Added the figure of Main PLL connection
68	ELECTRICAL CHARACTERISTICS 4. AC Characteristics (6) Power-on Reset Timing	· Added Time until releasing Power-on reset · Changed the figure of timing

Page	Section	Change Results
74-81	ELECTRICAL CHARACTERISTICS 4. AC Characteristics (7) CSIO/UART Timing	· Modified from UART Timing to CSIO/UART Timing · Changed from Internal shift clock operation to Master mode · Changed from External shift clock operation to Slave mode
88	ELECTRICAL CHARACTERISTICS 5. 12bit A/D Converter	· Added the typical value of Integral Nonlinearity, Differential Nonlinearity, Zero transition voltage and Full-scale transition voltage · Added Conversion time at AVcc < 4.5V · Modified Stage transition time to operation permission · Modified the minimum value of Reference voltage
92	ELECTRICAL CHARACTERISTICS 7. Flash Memory Write/Erase Characteristics	Change to the erase time of include write time prior to internal erase
93-96	ELECTRICAL CHARACTERISTICS 8. Return Time from Low-Power Consumption Mode	Added Return Time from Low-Power Consumption Mode
99	ORDERING INFORMATION	Change to full part number
100	PACKAGE DIMENSIONS	Deleted FPT-100P-M20 and FPT-120P-M21

Document History

Document Title: CY9B100A Series 32-bit Arm® Cortex®-M3 FM3 Microcontroller
Document Number: 002-05605

<table>
<tr><th>Revision</th><th>ECN</th><th>Orig. of Change</th><th>Submission Date</th><th>Description of Change</th></tr>
<tr><td>**</td><td>-</td><td>AKIH</td><td>12/15/2014</td><td>Migrated to Cypress and assigned document number 002-05605.
No change to document contents.</td></tr>
<tr><td>*A</td><td>5213577</td><td>AKIH</td><td>04/14/2016</td><td>Updated to Cypress template.</td></tr>
<tr><td>*B</td><td>5486354</td><td>NOSU</td><td>03/02/2017</td><td>Changed the package codes in the following chapters as the table below.
2. Packages
3. Pin Assignment
12.2. Recommended Operating Conditions
14. Ordering Information
15. Package Dimensions.
<table><tr><th>Before</th><th>After</th></tr><tr><td>FPT-100P-M23</td><td>LQI100</td></tr><tr><td>FPT-120P-M37</td><td>LQM120</td></tr><tr><td>BGA-112P-M04</td><td>LBC112</td></tr></table>Changed a word “J-TAG” to “JTAG” in 4. List of Pin Functions (Page 26).
Added a note of “TAP Controller” in 4. List of Pin Functions (Page 38).
Changed a word “Ta” to “T_A” in the following chapters.
12.2. Recommended Operating Conditions (Page 59)
12.3. DC Characteristics (Page 60 to 62)
12.4. AC Characteristics (Page 63 to 86)
12.5. 12bit A/D Converter (Page 87)
12.6. Low-Voltage Detection Characteristics (Page 90)
12.7. Flash Memory Write/Erase Characteristics (Page 91)
12.8 Return Time from Low-Power Consumption Mode (Page 92 to 94)
Added the Baud rate spec in 12.4.10 CSIO Timing (Page 73, 75, 77, 79)
Corrected the following statement
Analog port input current → Analog port input leak current
in chapter 12.5 12-bit A/D Converter (Page 87).
Corrected the following statement
Comrare clock cycle → Compare clock cycle
in chapter 12.5 12-bit A/D Converter (Page 88).
Corrected the Part numbers in chapter 14. Ordering Information.
- MB9BF102NABGL-G-YE1 → MB9BF102NABGL-GK6E1
- MB9BF104NABGL-G-YE1 → MB9BF104NABGL-GK6E1
- MB9BF105NABGL-G-YE1 → MB9BF105NABGL-GK6E1
- MB9BF106NABGL-G-YE1 → MB9BF106NABGL-GK6E1
Updated 15. Package Dimensions
Added 16. Errata</td></tr>
</table>

Revision	ECN	Orig. of Change	Submission Date	Description of Change
*C	5811604	YSAT	07/13/2017	Updated Cypress Logo and Copyright.
*D	5942095	HUAL	12/15/2017	Corrected the following Clock frequency MAX value (When not trimming) 5MHz → 6MHz in chapter 12.4.3 Built-in CR Oscillation Characteristics. Added the Part numbers in chapter 14. Ordering Information. - MB9BF104NAPMC-G-UNE1 - MB9BF106NAPMC-G-UNE1 - MB9BF106RAPMC-G-UNE1 Corrected the Part numbers in chapter 14. Ordering Information. - MB9BF106NAPMC-G-JNE2 → MB9BF106NAPMC-G-UNE2 - MB9BF106RAPMC-G-JNE2 → MB9BF106RAPMC-G-UNE2 Added the errata 002-06782 contents in chapter 16. Errata. Completing Sunset Review.
*E	6517784	HUAL	05/07/2019	Updated Document Title to read as “CY9B100A Series 32-bit Arm® Cortex®-M3 FM3 Microcontroller”. Replaced “MB9B100A Series” with “CY9B100A Series” in all instances across the document. Updated Ordering Information: Updated part numbers. Updated to new template.

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PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP | PSoC 6 MCU

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