MMA043PP4

Datasheet

0.5 GHz–12 GHz GaAs pHEMT MMIC Wideband Low-Noise Amplifier

Preliminary

May 2017

Microsemi

Power Matters.™

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.0

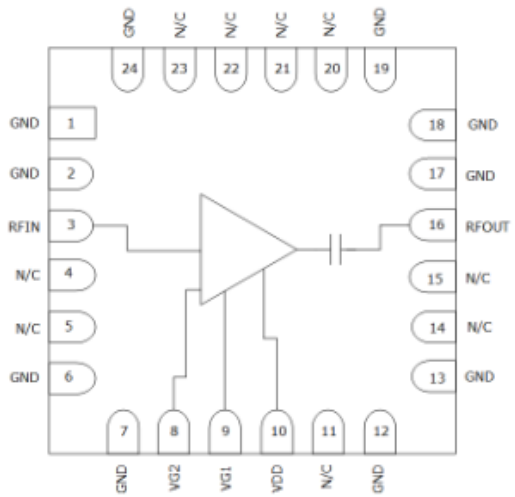
Revision 1.0 was published in May 2017. It was the first publication of this document.

2 Product Overview

The MMA043PP4 is a gallium arsenide (GaAs) pseudomorphic high-electron-mobility transistor (pHEMT) low-noise wideband amplifier in a leadless 4 mm × 4 mm surface-mount package that operates between 0.5 GHz and 12 GHz. The MMA043PP4 amplifier provides 16 dB of gain, 2.0 dB noise figure, and 28 dBm output IP3 and 17 dBm output P1dB while drawing only 55 mA of current from a 5 V supply. P1dB output power of +17 dBm enables the LNA to function as an LO driver for balanced, I/Q, or image reject mixers. The RF ports are internally matched to 50 Ω. This product is also available in die format as the MMA043AA.

The following image shows the primary functional diagram of the MMA043PP4 device.

Figure 1 • MMA043PP4 Functional Block Diagram



2.1 Applications

The MMA043PP4 device is designed for the following applications:

- Test instrumentation
- Wideband communications
- Military and space systems
- Wireless infrastructure
- Wideband microwave radios

2.2 Key Features

The following are key features of the MMA043PP4 device:

- GaAs pHEMT LNA monolithic microwave integrated circuit (MMIC)
- Low-noise figure: 1.5 dB from 0.5 GHz to 6 GHz
- High gain: 16 dB
- Broadband performance: 0.5 GHz–12 GHz
- Excellent P1dB output power: 17 dBm
- High OIP3: 28 dBm
- 50 Ω matched input/output
- Compact 24-lead 4 mm × 4 mm × 1.2 mm QFN package: 16 mm^2

3 Electrical Specifications

This section details the electrical specifications of the MMA043PP4 device.

3.1 Absolute Maximum Ratings

The following table lists the absolute maximum ratings of the MMA043PP4 device.

Table 1 • Absolute Maximum Ratings

Parameter	Rating
Storage temperature	–65 °C to 150 °C
Operating temperature	–40 °C to 85 °C
Drain bias voltage (V_{DD})	6.5 V
Gate bias voltage (V_{G1})	–2.0 V to 0 V
Channel temperature	150 °C
ESD sensitivity (HBM)	TBD
Thermal impedance	TBD

3.2 Specified Electrical Performance

The following table lists the specified electrical performance of the MMA043PP4 device at 25 °C, where V_{DD} is 5 +V, V_{G2} = +1.7 V, I_{DD} = 55 mA (set by V_{G1}).

Table 2 • Specified Electrical Performance

Parameter	Frequency Range	Min	Typ	Max	Units
Operational frequency range		0.5		12	GHz
Gain	0.5 GHz–12 GHz	14	16		dB
Gain flatness	0.5 GHz–12 GHz		±1.3		dB
Noise figure	0.5 GHz–7 GHz		1.5	2.0	dB
Noise figure	7 GHz–10 GHz		1.8	2.2	dB
Noise figure	10 GHz–12 GHz		2.5	2.7	dB
Input return loss	0.5 GHz–5 GHz		–10		dB
Input return loss	5 GHz–12 GHz		–7		dB
Output return loss	0.5 GHz–12 GHz		–10		dB
P1dB	0.5 GHz–10 GHz		17		dBm
P1dB	10 GHz–12 GHz		16		dBm
Psat (3 dB compression point)	0.5 GHz–10 GHz		18		dBm
Psat (3 dB compression point)	10 GHz–12 GHz		17		dBm
OIP3	0.5 GHz–12 GHz		28		dBm
V_{G2} (gate 2 bias voltage)			1.7		V
V_{G1} (gate 1 bias voltage) to set I_{DD}		–0.5	–0.3	0	V
V_{DD} (drain voltage supply)			5		V
I_{DD} (drain current)			55		mA

3.3 Typical Performance Curves

The following graphs show the typical performance curves of the MMA043PP4 device where V_{DD} is 5 V and I_{DD} is 55 mA, unless otherwise indicated. V_{G2} = 1.7 V and V_{G1} = –0.3 V.

Figure 2 • Forward Gain vs. Temperature

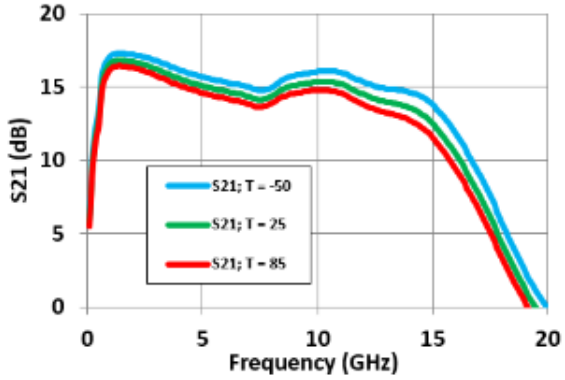


Figure 3 • Noise Figure vs. Temperature

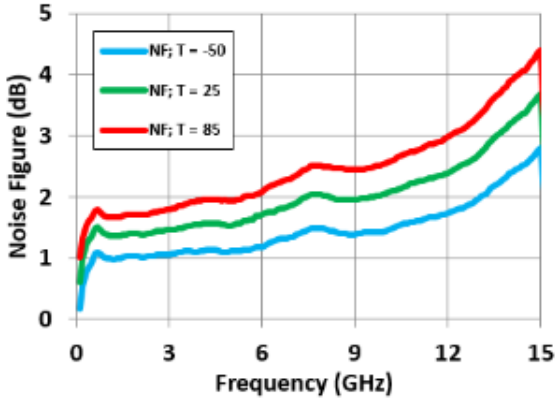


Figure 4 • Input Return Loss vs. Temperature

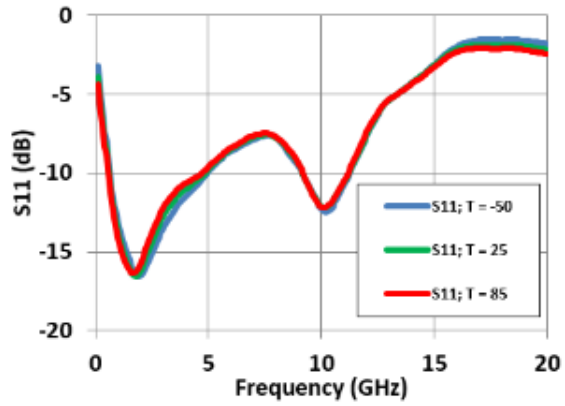


Figure 5 • Output Return Loss vs. Temperature

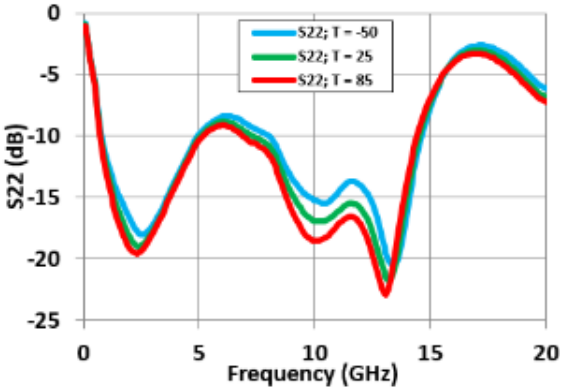


Figure 6 • Output IP3 vs. Temperature

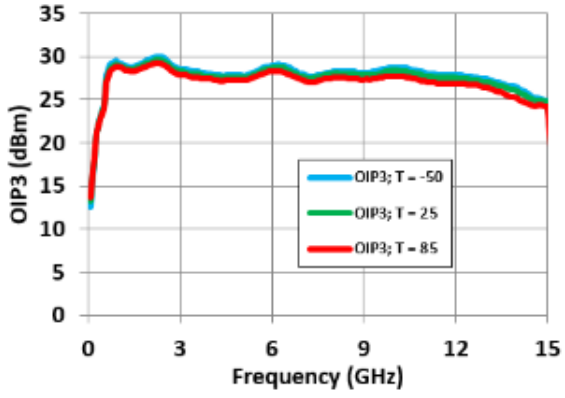
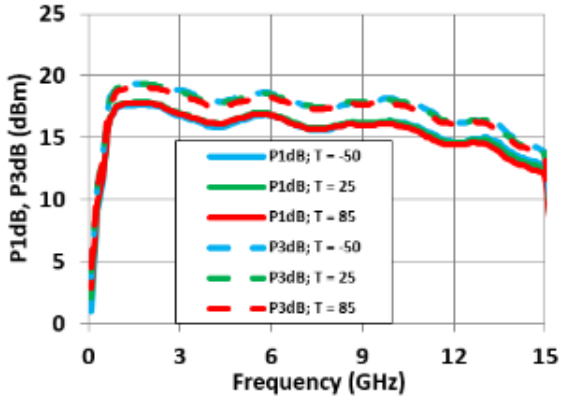


Figure 7 • P1dB and P3dB vs. Temperature



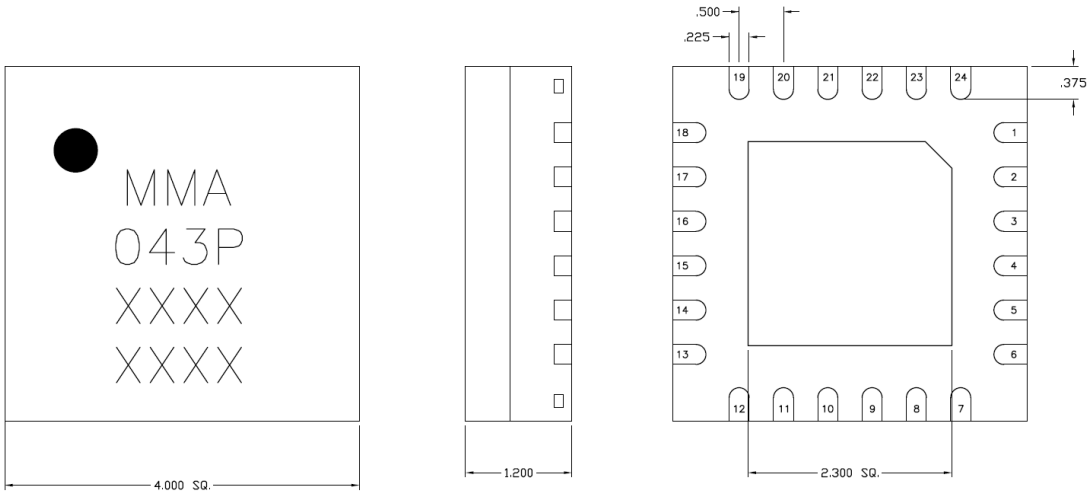
4 Package Specification

This section details the package specifications of the MMA043PP4 device.

4.1 Package Outline Drawing

The following illustration shows the package outline of the MMA043PP4 device. Dimensions are shown in millimeters [inches].

Figure 8 • Package Outline



4.2 Package Information

The following table lists the chip outline of the MMA043PP4 device. Contact your Microsemi sales representative for additional packaging information.

Table 3 • Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking
MMA043PP4	Low-stress injection molded plastic	100% matte Sn	TBD	MMA 043P wwyy

4.3 Pin Descriptions

The following table provides pin description information for the MMA043PP4 device.

Table 4 • Pin Description Information

Pin Number	Pin Name	Description
4, 5, 11, 14, 15, 20, 21, 22, 23	N/C	These pins are not connected internally. May be connected to external RF/DC ground on PCB.
1, 2, 6, 7, 12, 13, 17, 18, 19, 24	GND	GND pins and package bottom must be connected to external RF/DC ground on PCB.
3	RFIN	This pin is DC-coupled and matched to 50 Ω. External >300 pF DC blocking capacitor is required.
8	VG2	Positive Gate 2 control for the amplifier. Please follow the MMIC Amplifier Biasing Procedure application note. See assembly for required external components.
9	VG1	Negative Gate 1 control for the amplifier. Please follow the MMIC Amplifier Biasing Procedure application note. See assembly for required external components.
10	VDD	Power supply voltage for the amplifier. See assembly for required external components.
16	RFOUT	This pin is AC-coupled and matched to 50 Ω.

4.4 Bias Sequence Procedure

The following lists show the bias sequence procedures for the MMA043PP4 device.

Turn on:

1. Set V_{G1} (–ve) to –1 V.
2. Set V_{DD} to 5 V.
3. Set V_{G2} to 1.7 V.
4. Increase V_{G1} to achieve Idq of 55 mA.
5. Apply RF input.

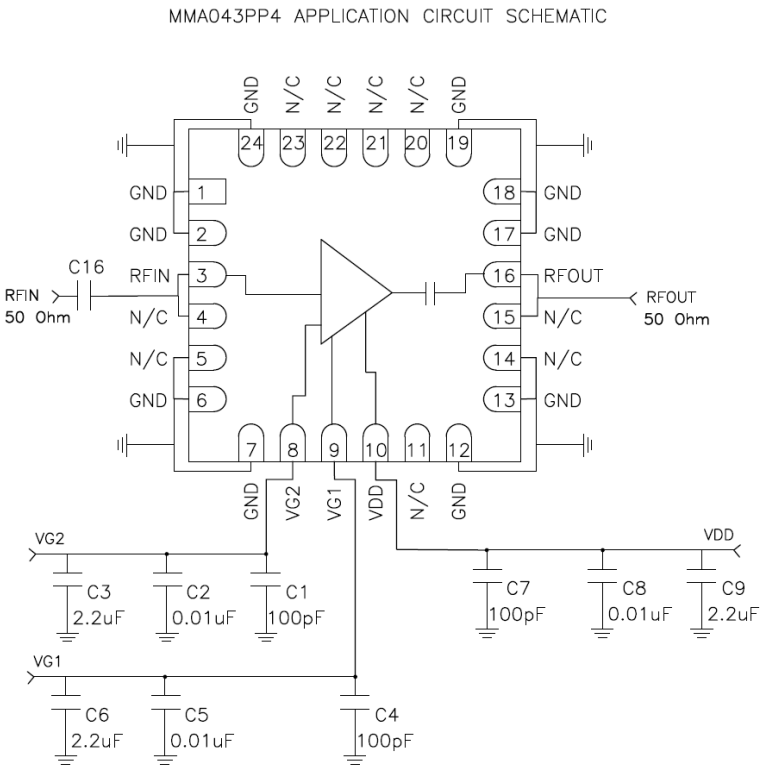
Turn off:

1. Turn off RF input.
2. Reduce V_{G1} to –1 V to achieve Idq of 0 mA.
3. Decrease V_{G2} to 0 V.
4. Decrease V_{DD} to 0 V.

4.5 Application Circuit

The following illustration shows the application circuit of the MMA043PP4 device.

Figure 9 • Application Circuit



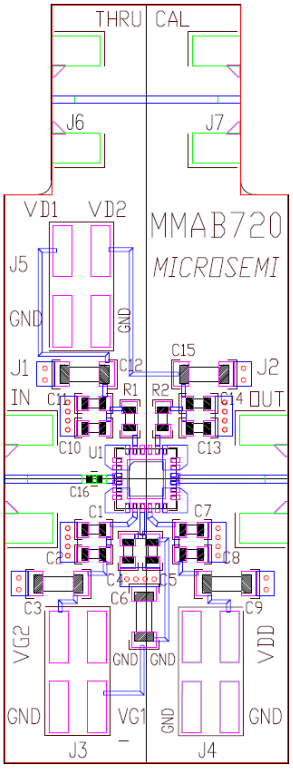
5 Handling Recommendations

Gallium arsenide integrated circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. It is recommended to follow all procedures and guidelines outlined in Microsemi application note AN01 GaAs MMIC Handling and Die Attach Recommendations.

6 Evaluation Board Information

The following illustration shows the evaluation board of the MMA043PP4 device.

Figure 10 • Evaluation Board



The circuit board used in the application should be generated with proper RF circuit design techniques. Signal lines at the RF port should have 50 Ω impedance, and the package ground leads and backside ground paddle should be connected directly to the ground plane similar to the previous image.

Only the components shown in the following table should be assembled.

Table 5 • Materials for Evaluation PCB MMA043PP4E

Item	Description
C1, C4, C7	0603, 100 pF, ±5%, 100 V, AVX, NPO
C2, C5, C8	0603, 10000 pF, ±10%, 100 V, AVX, X7R
C3,C6,C9	1206, 2.2 µF, ±10%, 50 V, AVX, X7R
C16	0402, 330 pF, ±10%, 25 V, AVX, NPO
J1,J2, J6, J7	SRI RF connector 2.9 mm
J3, J4	4-pin DC header Molex
U1	MMA043PP4 QFN 4X4, 24L
PCB	MMAB720
Base plate	749-MM-0198_Rev02 (modified)

7 Ordering Information

The following table lists the ordering information for the MMA043PP4 device.

Table 6 • Ordering Information

Part Number	Package
MMA043PP4	4 mm × 4 mm plastic QFN package
MMA043PP4E	Evaluation board for MMA043PP4

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