Features

- High Performance RF-CMOS 2.4 GHz Radio Transceiver Targeted for IEEE 802.15.4™, ZigBee®, 6LoWPAN, RF4CE, SP100, WirelessHART™ and ISM Applications
- Industry Leading Link Budget (104 dB):
  - Programmable Output Power from -17 dBm up to 3 dBm
  - Receiver Sensitivity -101 dBm
- Ultra-Low Power Consumption:
  - SLEEP: 20 nA
  - RX: 15.5 mA
  - TX: 16.5 mA (at max Transmit Power of 3 dBm)
- Ultra-Low Supply Voltage (1.8V to 3.6V) with Internal Regulator
- Optimized for Low BoM Cost and Ease of Production:
  - Few External Components Necessary (Crystal, Capacitors and Antenna)
- Excellent ESD Robustness
- Easy to Use Interface:
  - Registers and Frame Buffer Accessible through Fast SPI
  - Only Two Microcontroller GPIO Lines Necessary
  - One Interrupt Pin from Radio Transceiver
  - Clock Output with Prescaler from Radio Transceiver
- Radio Transceiver Features:
  - 128-byte SRAM for Data Buffering
  - Programmable Clock Output to Clock the Host Microcontroller or as Timer Reference
  - Integrated TX/RX Switch
  - Fully Integrated PLL with on-chip Loop Filter
  - Fast PLL Settling Time
  - Battery Monitor
  - Fast Power-Up Time < 1 ms
- Special IEEE 802.15.4-2003 Hardware Support:
  - FCS Computation
  - Clear Channel Assessment
  - Energy Detection / RSSI Computation
  - Automatic CSMA-CA
  - Automatic Frame Retransmission
  - Automatic Frame Acknowledgement
  - Automatic Address Filtering
- Industrial Temperature Range:
  - -40° C to 85° C
- I/O and Packages:
  - 32-pin Low-Profile QFN
  - RoHS/Fully Green
- Compliant to EN 300 328/440, FCC-CFR-47 Part 15, ARIB STD-66, RSS-210
- Compliant to IEEE 802.15.4-2003

AVR®

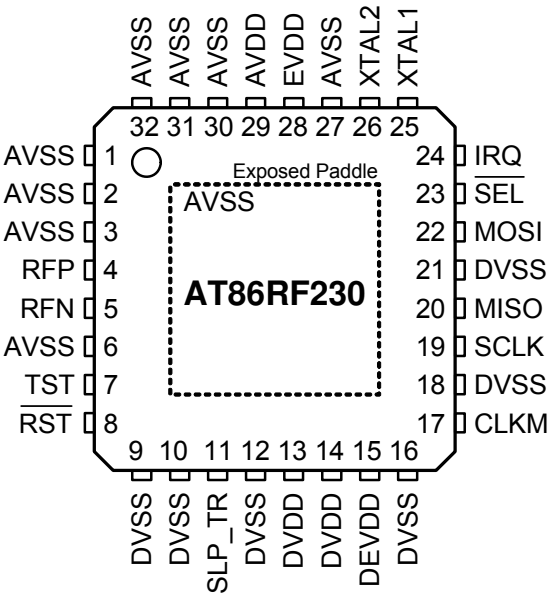
Low Power 2.4 GHz Transceiver for ZigBee, IEEE 802.15.4, 6LoWPAN, RF4CE and ISM Applications

AT86RF230

5131E-MCU Wireless-02/09

1 Pin-out Diagram

Figure 1-1. AT86RF230 Pin-Out Diagram



Note: The exposed paddle is electrically connected to the die inside the package. It shall be soldered to the board to ensure electrical and thermal contact and good mechanical stability.

Disclaimer

Typical values contained in this datasheet are based on simulations and testing. Min and Max values will be available when the radio transceiver has been fully characterized.

2 Overview

The AT86RF230 is a low-power 2.4 GHz radio transceiver especially designed for ZigBee/IEEE 802.15.4 applications. The AT86RF230 is a true SPI-to-antenna solution. All RF-critical components except the antenna, crystal and de-coupling capacitors are integrated on-chip. Therefore, the AT86RF230 is particularly suitable for applications like:

- 2.4 GHz IEEE 802.15.4 and ZigBee systems
- 6LoWPAN and RF4CE systems
- Wireless sensor networks
- Industrial control, sensing and automation (SP100, WirelessHART)
- Home and building automation
- Consumer electronics
- PC peripherals

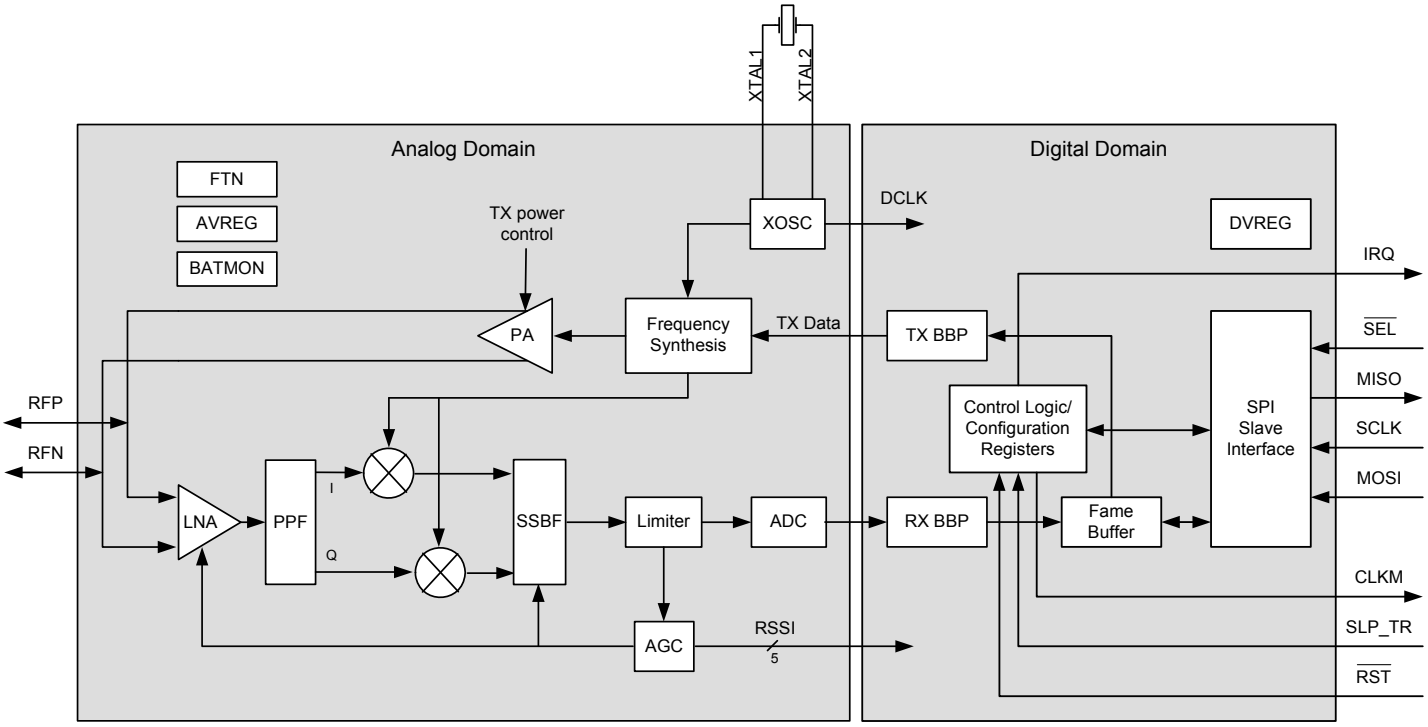
The AT86RF230 can be operated by using an external microcontroller like ATMEL's AVR microcontrollers. A comprehensive software programming description can be found in the application note AVR2009 "AT86RF230 – Software Programming Model".

3 General Circuit Description

This single-chip radio transceiver provides a complete radio transceiver interface between the antenna and the microcontroller. It comprises the analog radio transceiver and the digital demodulation including time and frequency synchronization, and data buffering. The number of external components is minimized such that only an antenna, a crystal and four decoupling capacitors are required. The bidirectional differential antenna pins are used for transmission and reception, so that no external antenna switch is needed.

The AT86RF230 block diagram is shown in Figure 3-1.

Figure 3-1. Block Diagram of the AT86RF230



The received RF signal at pins RFN and RFP is differentially fed through the low-noise amplifier (LNA) to the RF filter (PPF) to generate a complex signal. This signal is converted down by mixers to an intermediate frequency and fed to the integrated channel filter (SSBF). The limiting amplifier provides sufficient gain to drive the succeeding analog-to-digital converter (ADC) and generates a digital RSSI signal with 3 dB granularity. The ADC output signal is sampled by the digital base band receiver (RX BBP).

The transmit modulation scheme is offset-QPSK (O-QPSK) with half-sine pulse shaping and 32-length block coding (spreading) according to [1]. The modulation signal is generated in the digital transmitter (TX BBP) and applied to the fractional-N frequency synthesis (PLL) generating a coherent phase modulation required for demodulation of O-QPSK signals. The frequency-modulated RF signal is fed to the power amplifier (PA).

An internal 128 byte RAM for RX and TX (Frame Buffer) buffers the data to be transmitted or the received data. Two on chip low dropout (LDO) voltage regulators provide the internal analog and digital 1.8V supply.

4 Pin Description

Table 4-1. AT86RF230 Pin List

Number	Name	Type	Description
1	AVSS	Ground	Analog ground
2	AVSS	Ground	Analog ground
3	AVSS	Ground	Ground for RF signals
4	RFP	RF I/O	Differential RF signal
5	RFN	RF I/O	Differential RF signal
6	AVSS	Ground	Ground for RF signals
7	TST	Digital input	Enables Continuous Transmission Test Mode; active high
8	$\overline{\text{RST}}$	Digital input	Chip reset; active low
9	DVSS	Ground	Digital ground
10	DVSS	Ground	Digital ground
11	SLP_TR	Digital input	Controls sleep, transmit start and receive states; active high
12	DVSS	Ground	Digital ground
13	DVDD	Supply	Regulated 1.8V supply voltage; digital domain
14	DVDD	Supply	Regulated 1.8V supply voltage; digital domain
15	DEVDD	Supply	External supply voltage; digital domain
16	DVSS	Ground	Digital ground
17	CLKM	Digital output	Master clock signal output
18	DVSS	Ground	Digital ground
19	SCLK	Digital input	SPI clock
20	MISO	Digital output	SPI data output (master input slave output)
21	DVSS	Ground	Digital ground
22	MOSI	Digital input	SPI data input (master output slave input)
23	$\overline{\text{SEL}}$	Digital input	SPI select; active low
24	IRQ	Digital output	Interrupt request signal; active high
25	XTAL1	Analog input	Crystal pin or external clock supply
26	XTAL2	Analog input	Crystal pin
27	AVSS	Ground	Analog ground
28	EVDD	Supply	External supply voltage; analog domain
29	AVDD	Supply	Regulated 1.8V supply voltage; analog domain
30	AVSS	Ground	Analog ground
31	AVSS	Ground	Analog ground
32	AVSS	Ground	Analog ground
Paddle	AVSS	Ground	Analog ground; Exposed Paddle of QFN package

4.1 Supply and Ground Pins

EVDD, DEVDD

EVDD and DEVDD are analog and digital supply voltage pins of the AT86RF230 radio transceiver.

AVDD, DVDD

AVDD and DVDD are outputs of the internal 1.8V voltage regulators. The voltage regulators are controlled independently by the radio transceivers state machine and are activated depending on the current radio transceiver state. The voltage regulators can be configured for external supply. For details refer to section 9.4.

AVSS, DVSS

AVSS and DVSS are analog and digital ground pins respectively.

The analog and digital power domains should be separated on the PCB, for further details see application note AVR2005 "Design Considerations for the AT86RF230".

4.2 Analog and RF Pins

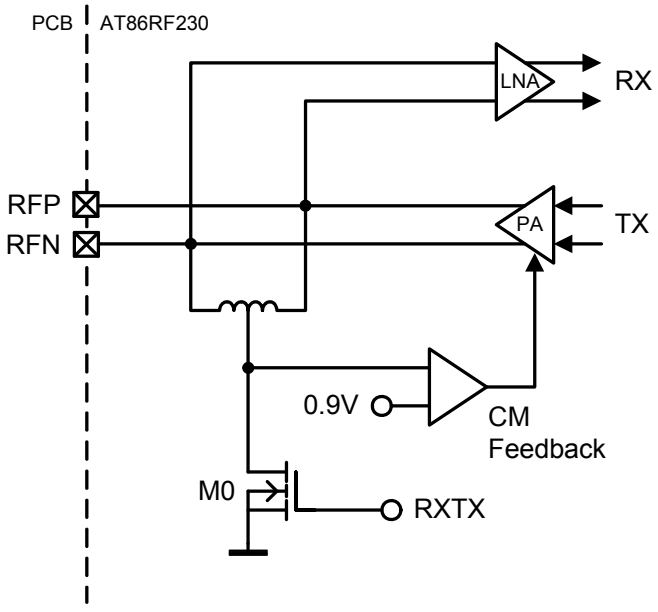
RFP, RFN

A differential RF port (RFP/RFN) provides common-mode rejection to suppress the switching noise of the internal digital signal processing blocks. At the board-level, the differential RF layout ensures high receiver sensitivity by rejecting any spurious interspersions originating from other digital ICs such as a microcontroller.

The RF port is designed for a 100Ω differential load. A DC path between the RF pins is allowed. A DC path to ground or supply voltage is not allowed. Therefore, when connecting a RF-load providing a DC path to the power supply or to ground, capacitive coupling is required as indicated in Table 4-2.

A simplified schematic of the RF front end is shown in Figure 4-1.

Figure 4-1. Simplified RF Front-End Schematic



RF port DC values depend on the operating mode. In TRX_OFF state (see section 7.1.2), when the analog front end is disabled, the RF pins are pulled to ground, preventing a floating voltage.

In receive mode, the RF input provides a low-impedance path to ground when transistor M0 (see Figure 4-1) pulls the inductor center tap to ground. A DC voltage drop of 20 mV across the on-chip inductor can be measured at the RF pins.

In transmit mode, a control loop provides a common-mode voltage of 0.9V. Transistor M0 is off, allowing the PA to set the common-mode voltage. The common-mode capacitance at each pin to ground shall be < 30 pF to ensure the stability of this common-mode feedback loop.

XTAL1, XTAL2

The pin XTAL1 is the input of the reference oscillator amplifier (XOSC), XTAL2 is the output. A detailed description of the crystal oscillator setup and the related XTAL1/XTAL2 pin configuration can be found in section 9.6.

When using an external clock reference signal, XTAL1 shall be used as input pin. For further details refer to section 9.6.3.

Table 4-2. Comments on Analog and RF Pins

Pin	Condition	Recommendation/Comment
RFP/RFN	VDC = 0.9V (TX) VDC = 20 mV (RX) at both pins	AC-coupling is required if an antenna with a DC path to ground is used. Serial capacitance must be < 30 pF.
XTAL1/XTAL2	CPAR = 3 pF VDC = 0.9V at both pins	Parasitic capacitance (CPAR) of the pins must be considered as additional load capacitance to the crystal.

4.3 Digital Pins

The digital interface of the AT86RF230 compromises pins $\overline{\text{SEL}}$, SCLK, MOSI and MISO forming the serial peripheral interface (SPI) and pins CLKM, IRQ, SLP_TR and $\overline{\text{RST}}$ used as additional control signal between radio transceiver and microcontroller. The digital radio transceiver interface is described in detail in section 6.

4.3.1 Driver Strength Settings of Digital Output Pins

The driver strength of the digital output pins (MISO, IRQ) and CLKM pin can be configured by register 0x03 (TRX_CTRL_0) as described in Table 4-3.

The capacitive load should be as small as possible and not larger than 50 pF when using the 2 mA minimum driver strength setting. Generally, the output driver strength should be adjusted to the lowest possible value in order to keep the current consumption and the emission of digital signal harmonics low.

Table 4-3. Digital Output Driver Configuration

Pin	Default Driver Strength	Comment
MISO, IRQ	2 mA	Adjustable to 2 mA, 4 mA, 6 mA and 8 mA
CLKM	4 mA	Adjustable to 2 mA, 4 mA, 6 mA and 8 mA

4.3.2 Pull-up and Pull-down Configuration of Digital Input Pins

Pulling resistors are internally connected to all digital input pins in radio transceiver state P_ON (see section 7.1.2). Table 4-4 summarizes the pull-up and pull-down configuration.

Table 4-4 Pull-Up/Pull-Down Configuration of Digital Input Pins in P_ON State

Pin	H ≙ pull-up, L ≙ pull-down
$\overline{\text{RST}}$	H
$\overline{\text{SEL}}$	H
SCLK	L
MOSI	L
SLP_TR	L

In all other radio transceiver states, no pull-up or pull-down resistors are connected to any of the digital input pins.

4.3.3 Register Description

Register 0x03 (TRX_CTRL_0)

The TRX_CTRL_0 register controls the drive current of the digital output pads and the CLKM clock rate.

Bit	7	6	5	4	
0x03	PAD_IO		PAD_IO_CLKM		TRX_CTRL_0
Read/Write	R/W	R/W	R/W	R/W	
Reset value	0	0	0	1	

Bit	3	2	1	0	
0x03	CLKM_SHA_SEL	CLKM_CTRL			TRX_CTRL_0
Read/Write	R/W	R/W	R/W	R/W	
Reset value	1	0	0	1	

- **Bit [7:6] – PAD_IO**

The register bits PAD_IO set the output driver current of digital output pads MISO and IRQ.

Table 4-5. Digital Output Driver Strength

Register Bit	Value	Description
PAD_IO	0[1]	2 mA
	1	4 mA
	2	6 mA
	3	8 mA
Notes:	1. Reset values of register bits are underlined characterized in the document.	

- **Bit [5:6] – PAD_IO_CLKM**

The register bits PAD_IO_CLKM set the output driver current of pin CLKM.

Table 4-6. CLKM Driver Strength

Register Bit	Value	Description
PAD_IO_CLKM	0	2 mA
	1	4 mA
	2	6 mA
	3	8 mA

- **Bit 3 – CLKM_SHA_SEL**

Refer to section 9.6.5.

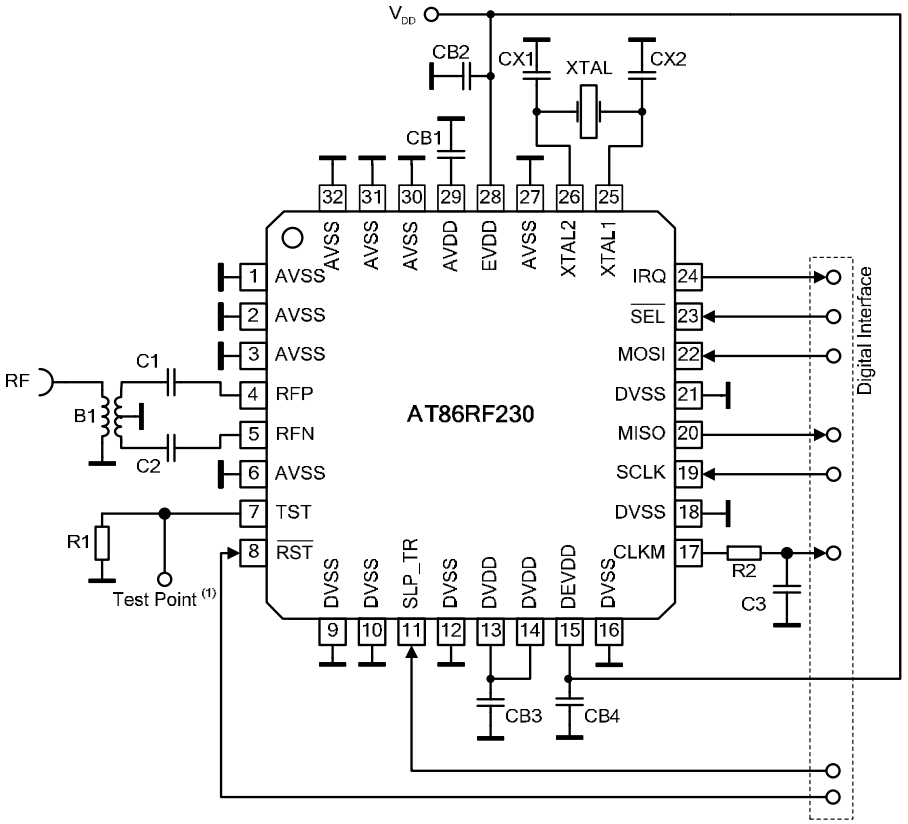
- **Bit [2:0] – CLKM_CTRL**

Refer to section 9.6.5.

5 Application Circuit

An application circuit of the AT86RF230 radio transceiver with a single-ended RF connector is shown in Figure 5-1. The balun B1 transforms the 100Ω differential RF port (RFP/RFN) to a 50Ω single-ended RF port. The capacitors C1 and C2 provide AC coupling of the RF signals to the RF pins.

Figure 5-1. Application Circuit Schematic



Note: (1) For further details refer to „Appendix A – Continuous Transmission Test Mode“

The power supply decoupling capacitors (CB2, CB4) are connected to the external analog supply pin (EVDD, pin 28) and the external digital supply pin (DEVDD, pin 15).

Capacitors CB1 and CB3 are bypass capacitors for the integrated analog and digital voltage regulators to ensure stable operation (1 µF recommended value). All decoupling and bypass capacitors should be placed as close as possible to the AT86RF230 pins and should have a low-resistance and low-inductance connection to ground to achieve the best performance.

The crystal (XTAL), the two load capacitors (CX1, CX2), and the internal circuitry connected to pins XTAL1 and XTAL2 form the crystal oscillator. To achieve the best accuracy and stability of the reference frequency, large parasitic capacitances should be avoided. Crystal lines should be routed as short as possible and not in proximity of digital I/O signals.

Crosstalk from digital signals on the crystal pins or the RF pins can degrade the system performance. Therefore, a low-pass filter (C3, R2) is placed close to the CLKM output pin to reduce the radiation of signal harmonics. This is not needed if the CLKM pin is not used. Then the output should be turned off during device initialization.

The application board ground plane should be separated into four independent fragments, the analog, the digital, the antenna and the XTAL ground plane. The exposed paddle shall act as reference of the individual grounds.

For further details see application note AVR2005 "Design Considerations for the AT86RF230".

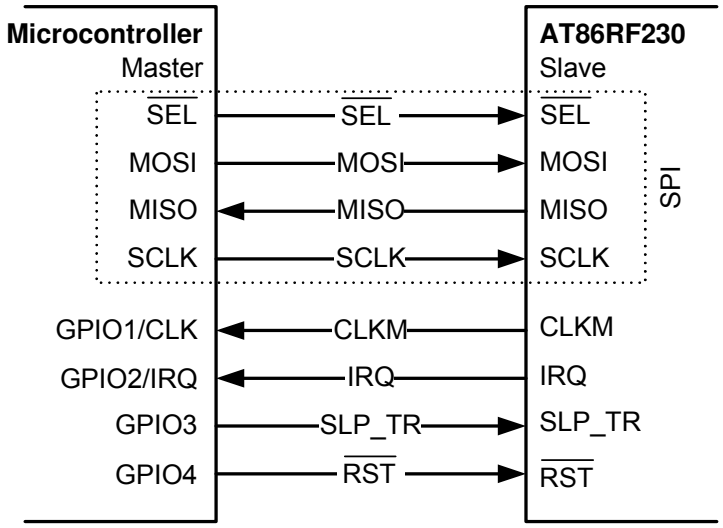
Table 5-1. Example Bill of Materials

Designator	Description	Value	Manufacturer	Part Number	Comment
B1	SMD balun	2.45 GHz	Wuerth	748421245	2.45 GHz Balun
B1 (alternatively)	SMD balun / filter	2.45 GHz	Johanson Technology	2450FB15L0001	2.45 GHz Balun / Filter
CB1	LDO VREG bypass capacitor	1 µF	AVX Murata	0603YD105KAT2A GRM188R61C105KA12D	X5R 10% 16V (0603)
CB2	Power supply decoupling	1 µF			
CB3	LDO VREG bypass capacitor	1 µF			
CB4	Power supply decoupling	1 µF			
CX1	Crystal load capacitor	12 pF	AVX Murata	06035A120JA GRP1886C1H120JA01	COG 5% 50V (0603)
CX2	Crystal load capacitor	12 pF			
C1	RF coupling capacitor	22 pF	Epcos Epcos AVX	B37930 B37920 06035A220JAT2A	C0G 5% 50V (0402 or 0603)
C2	RF coupling capacitor	22 pF			
C3	CLKM low-pass filter capacitor	2.2 pF	AVX Murata	06035A229DA GRP1886C1H2R0DA01	COG ±0.5 pF 50V (0603) Designed for f_{CLKM} = 1 MHz
R1	Pull-down resistor	10 kΩ			Recommended 0Ω, if continuous transmission is not required
R2	CLKM low-pass filter resistor	680Ω			Designed for f_{CLKM} = 1 MHz
XTAL	Crystal	CX-4025 16 MHz SX-4025 16 MHz	ACAL Taitjen Siward	XWBBPL-F-1 A207-011	

6 Microcontroller Interface

This section describes the AT86RF230 to microcontroller interface. The interface comprises a slave SPI and additional control signals, see Figure 6-1. The SPI timing and protocol are described.

Figure 6-1. Microcontroller to AT86RF230 Interface



Microcontrollers with a master SPI, such as Atmel's AVR family, interface directly to the AT86RF230. The SPI is used for Frame Buffer and register access. The additional control signals are connected to the GPIO/IRQ interface of the microcontroller. Table 6-1 introduces the radio transceiver I/O signals and their functionality.

Table 6-1. Signal Description of Microcontroller Interface

Signal	Description
$\overline{\text{SEL}}$	SPI select signal, active low
MOSI	SPI data (master output slave input) signal
MISO	SPI data (master input slave output) signal
SCLK	SPI clock signal
CLKM	AT86RF230 clock output, usable as: - Microcontroller clock source - High precision timing reference
IRQ	AT86RF230 interrupt request signal
SLP_TR	AT86RF230 multi purpose control signal (functionality is state-depended): - Sleep/Wakeup - TX start - Controls CLKM output
$\overline{\text{RST}}$	AT86RF230 reset signal, active low

6.1 SPI Timing Description

The SPI is designed to work in synchronous or asynchronous mode.

In synchronous mode, the CLKM output of the radio transceiver is used as the master clock of the microcontroller. In this case the maximum SPI clock frequency is 8 MHz.

In asynchronous mode, the SPI master clock (SCLK) is generated by the microcontroller itself. The maximum SPI clock rate is limited to 7.5 MHz using this operating mode. If the clock signal from the radio transceiver pin CLKM is not required, it may be disabled.

Figure 6-2 and Figure 6-3 illustrate the SPI timing and introduce its parameters. The corresponding timing parameter definition is given in Table 11-4.

Figure 6-2. SPI Timing, Global Map and Definition of Timing Parameters t_5, t_6, t_8 and t_9

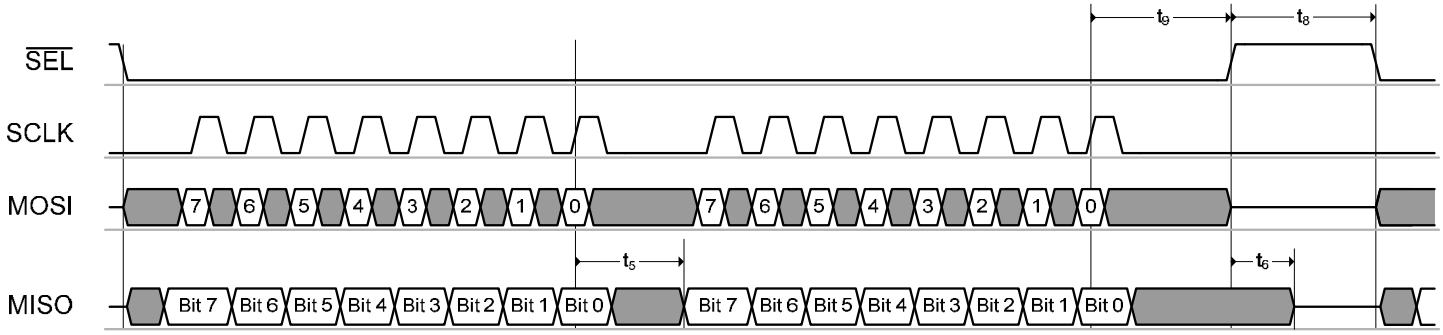
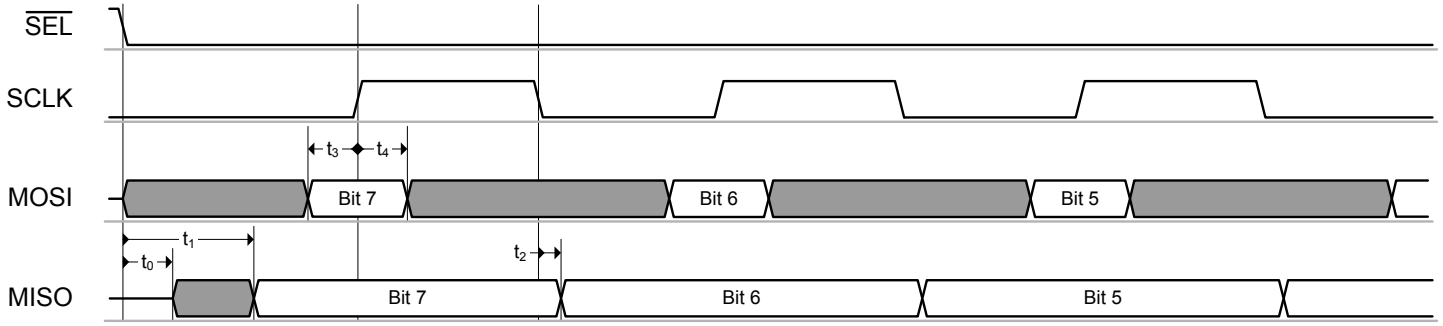


Figure 6-3. SPI Timing, Detailed View and Definition of Timing Parameters t_0 to t_4



The SPI is based on a byte-oriented protocol and is always a bidirectional communication between master and slave. The SPI master starts the transfer by asserting $\overline{SEL}$ = L. Then the master generates eight SPI clock cycles to transfer a byte to the radio transceiver (via MOSI). At the same time the slave transmits one byte to the master (via MISO). When the master wants to receive one byte of data from the slave it must also transmit one byte to the slave. All bytes are transferred MSB first. An SPI transaction is finished by releasing $\overline{SEL}$ = H.

A SPI register access consists of two bytes, a Frame Buffer or SRAM access of two or more bytes, as described in section 6.2.

$\overline{SEL}$ = L enables the MISO output driver of the radio transceiver. The MSB of MISO is valid after t_1 (see section 11.4 parameter 11.4.3) and is updated at each falling edge of SCLK. If the MISO output driver is disabled, there is no internal pull-up resistor connected to the output. Driving the appropriate signal level must be ensured by the

master device or an external pull-up resistor. Note, when both $\overline{SEL}$ and $\overline{RST}$ are active, the MISO output driver is also enabled.

The MOSI line is sampled by the radio transceiver at the rising edge of SCLK. The signal must be stable before and after the rising edge of SCLK as specified by t_3 and t_4, refer to section 11.4 parameters 11.4.5 and 11.4.6.

This mode of SPI operation is commonly called “SPI Mode 0”.

6.2 SPI Protocol

Each transfer sequence starts with transferring a command byte from SPI master via MOSI (see Table 6-2) with MSB first. This command byte defines the access mode and additional mode-dependent information.

Table 6-2. SPI Command Byte Definition

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Mode
1	0	Register address [5:0]						Register Access Mode – Read Access
1	1	Register address [5:0]						Register Access Mode – Write Access
0	0	1	Reserved					Frame Buffer Access Mode – Read Access
0	1	1	Reserved					Frame Buffer Access Mode – Write Access
0	0	0	Reserved					SRAM Access Mode – Read Access
0	1	0	Reserved					SRAM Access Mode – Write Access

The different access modes are described within the following sections.

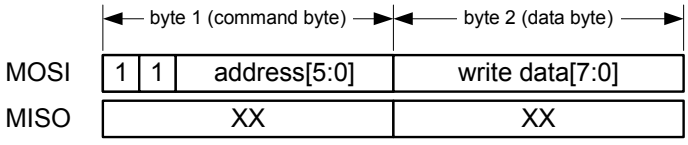
In Figure 6-4 to Figure 6-14 logic values stated with X on MOSI are ignored by the radio transceiver, but need to have a valid level. Return values on MISO stated as X shall be ignored by the microcontroller.

6.2.1 Register Access Mode

The Register access mode is a two-byte read/write operation and is initiated by setting $\overline{SEL}$ = L. The first transferred byte on MOSI is the command byte and must indicate a register access (see Table 6-2) and a register address (see Table 12-1).

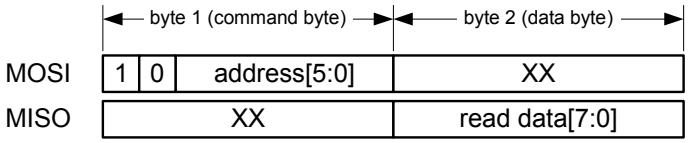
On write access the second byte transferred on MOSI contains the write data to the selected address (see Figure 6-4).

Figure 6-4. Packet Structure – Register Write Access



On read access the content of the selected register address is returned in the second byte on MISO (see Figure 6-5).

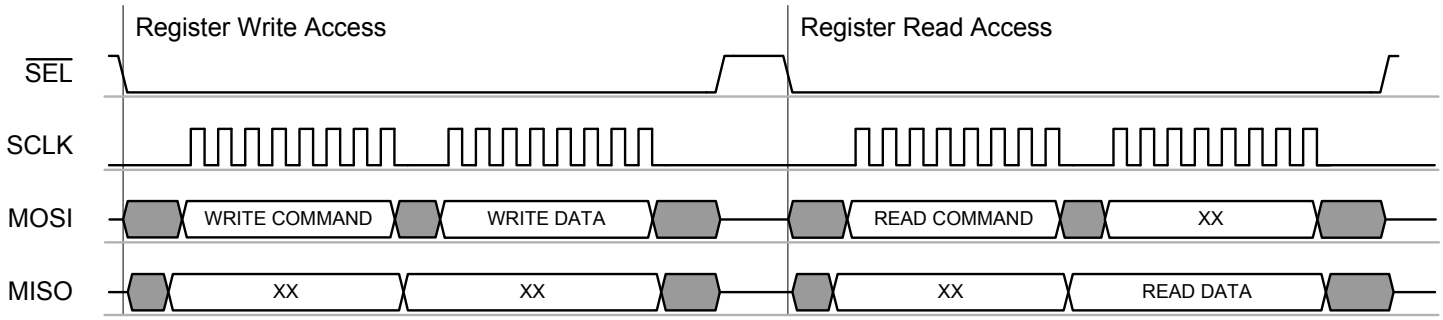
Figure 6-5. Packet Structure – Register Read Access



Each register access must be terminated by setting $\overline{SEL}$ = H.

Figure 6-6 illustrates a typical SPI sequence for a register access sequence for write and read respectively.

Figure 6-6. Example SPI Sequence - Register Access Mode



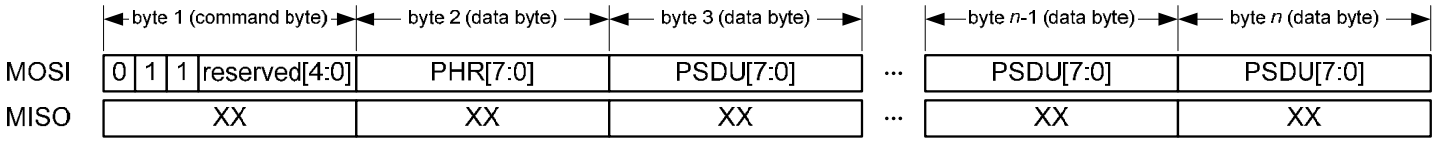
6.2.2 Frame Buffer Access Modes

The Frame Buffer read access and the Frame Buffer write access are used to upload or download frames to the microcontroller.

Each access starts by setting $\overline{SEL}$ = L. The first byte transferred on MOSI is the command byte and must indicate a Frame Buffer access mode according to the definition in Table 6-2.

On Frame Buffer write access the second byte transferred on MOSI contains the frame length (PHR field) followed by the payload data (PSDU) as shown by Figure 6-7.

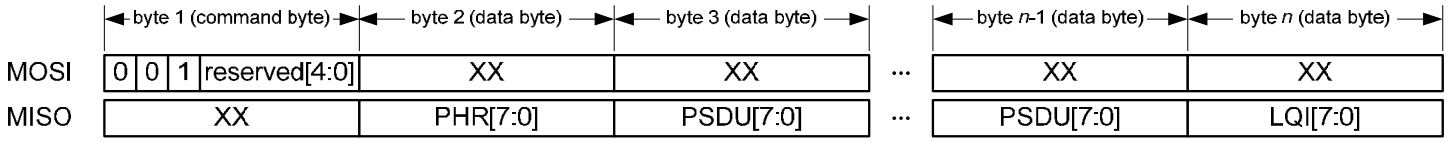
Figure 6-7. Packet Structure - Frame Buffer Write Access



On Frame Buffer read access PHR and PSDU are transferred via MISO starting with the second byte. After the PSDU data bytes one more byte can be transferred containing the link quality indication (LQI) value of the received frame, for details refer to section 8.5. Figure 6-8 illustrates the packet structure of a Frame Buffer read access.

Note, the Frame Buffer read access can be terminated at any time without any consequences by setting $\overline{SEL}$ = H, e.g. after reading the frame length byte only.

Figure 6-8. Packet Structure - Frame Buffer Read Access



The number of bytes *n* for one Frame Buffer access is calculated as follow:

Receive: *n* = 3 + *frame_length*

[command byte, frame length byte, PSDU data, LQI byte]

Transmit: *n* = 2 + *frame_length*

[command byte, frame length byte, PSDU data]

The maximum value of *frame_length* is 127 bytes. That means that *n* ≤ 130 for Frame Buffer read access and *n* ≤ 129 for Frame Buffer write access. Each read or write of a data byte increments automatically the address counter of the Frame Buffer until the access is terminated by setting SEL = H.

Figure 6-9 and Figure 6-10 illustrate an example SPI sequence of a Frame Buffer access to write and read a frame with 4-byte PSDU respectively.

Figure 6-9. Example SPI Sequence - Frame Buffer Write Sequence of a Frame with 4-byte PSDU

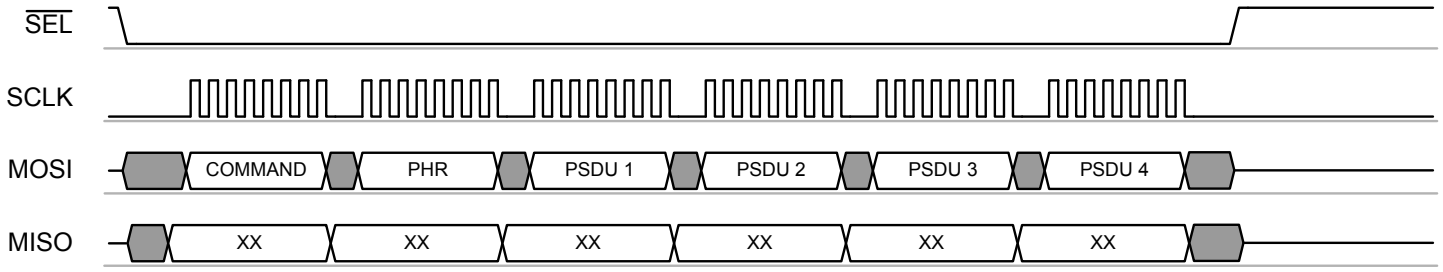
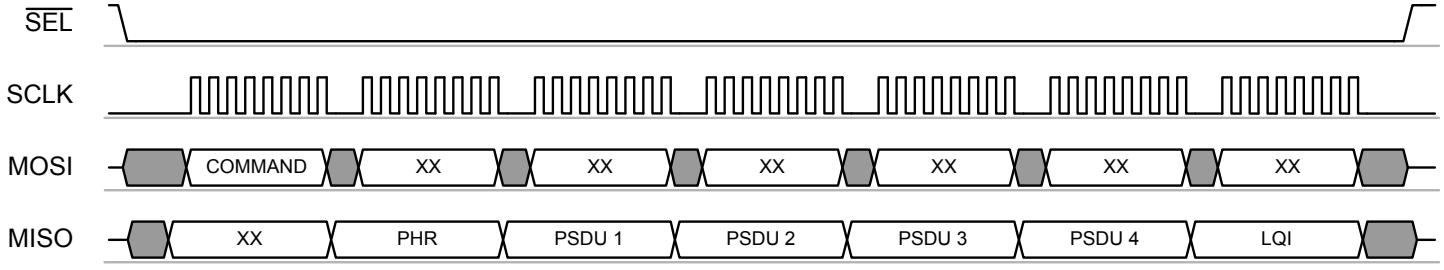


Figure 6-10. Example SPI Sequence - Frame Buffer Read Sequence of a Frame with 4-byte PSDU



Access violations during a Frame Buffer write or read access are indicated by a TRX_UR interrupt. For further details refer to section 9.3.3.

6.2.3 SRAM Access Mode

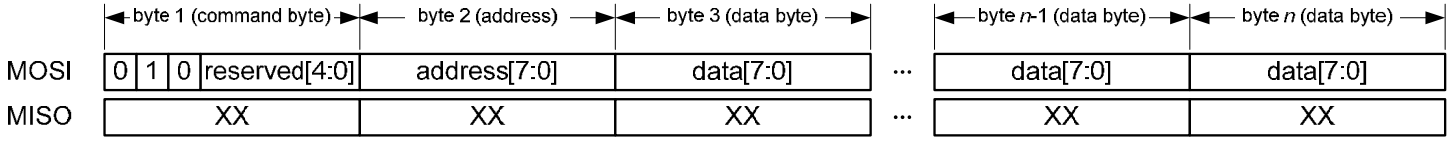
The SRAM access mode allows access to certain bytes within the Frame Buffer. This may reduce SPI traffic.

The SRAM access mode is useful, for instance, if a transmit frame is already stored in the Frame Buffer and certain bytes (e.g. sequence number or address field) need to be replaced before retransmitting the frame. Furthermore, it can be used to access only the LQI value after frame reception. A detailed description of the user accessible frame content can be found in section 9.3.2.

Each access starts by setting $\overline{SEL}$ = L. The first transferred byte on MOSI shall be the command byte and must indicate a SRAM access mode according to the definition in Table 6-2. The following byte indicates the start address of the write or read access. The address space is 0x00 to 0x7F. The microcontroller software has to ensure to access only to the valid address space.

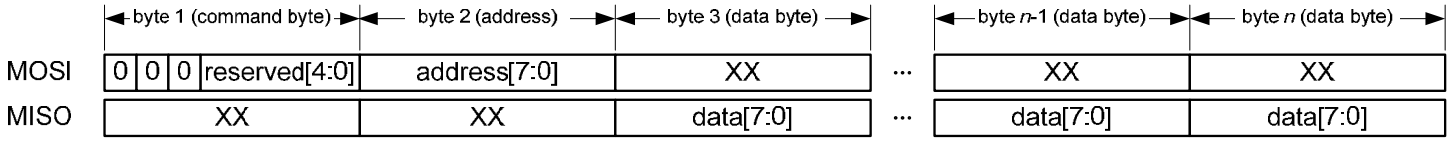
On SRAM write access, one or more bytes of write data are transferred on MOSI starting with the third byte of the access sequence (see Figure 6-11).

Figure 6-11. Packet Structure - SRAM Write Access



On SRAM read access, one or more bytes of read data are transferred on MISO starting with the third byte of the access sequence (see Figure 6-12).

Figure 6-12. Packet Structure - SRAM Read Access



As long as $\overline{SEL}$ is logic low, every subsequent byte read or write increments the address counter of the Frame Buffer until the SRAM access is terminated by setting $\overline{SEL}$ = H.

Figure 6-13 and Figure 6-14 illustrate an example SPI sequence of a SRAM access to write and read a data package of 5 byte length respectively.

Figure 6-13. Example SPI Sequence – SRAM Write Access Sequence of a 5 byte Data Package

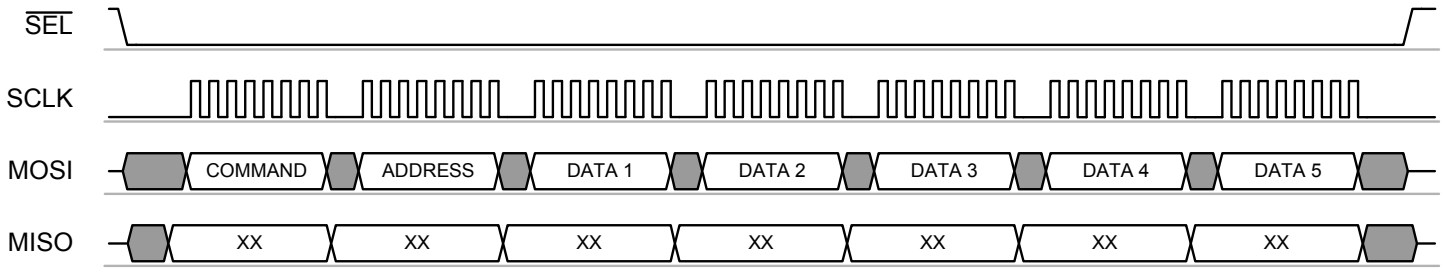
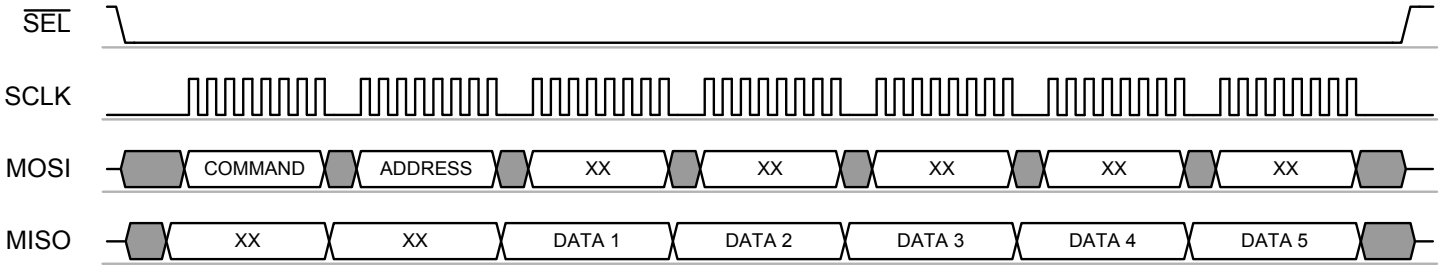


Figure 6-14. Example SPI Sequence – SRAM Read Access Sequence of a 5 byte Data Package



Notes:

- Because the Frame Buffer is shared between TX and RX, the frame data are overwritten by new incoming frames. If the TX frame data is to be retransmitted, it must be ensured that no frame was received meanwhile.
- If the SRAM access mode is used to upload received frames, the Frame Buffer contains all frame data except the frame length byte. The frame length information can be accessed only using the Frame Buffer read access.
- It is not possible to transmit received frames without a Frame Buffer read and write operation by the microcontroller.
- Frame Buffer access violations are not indicated by a TXR_UR interrupt when using the SRAM access mode (see section 9.3.3)

6.3 Radio Transceiver Identification

The AT86RF230 can be identified by four registers. One register contains an unique part number and one register the corresponding version number. Additional two registers contain the JEDEC manufacturer ID.

6.3.1 Register Description

Register 0x1C (PART_NUM)

Bit	7	6	5	4	3	2	1	0	
0x1C	PART_NUM								PART_NUM
Read/Write	R	R	R	R	R	R	R	R	
Reset value	0	0	0	0	0	0	1	0	

- **Bit [7:0] – PART_NUM**

This register bits PART_NUM contain the radio transceiver part number.

Table 6-3. Radio Transceiver Part Number

Register Bits	Value[7:0]	Description
PART_NUM	2	AT86RF230 part number

Register 0x1D (VERSION_NUM)

Bit	7	6	5	4	3	2	1	0	
0x1D	VERSION_NUM								VERSION_NUM
Read/Write	R	R	R	R	R	R	R	R	
Reset value	0	0	0	0	0	0	1	0	

- **Bit [7:0] – VERSION_NUM**

This register bits VERSION_NUM contain the radio transceiver version number.

Table 6-4. Radio Transceiver Version Number

Register Bits	Value[7:0]	Description
VERSION_NUM	1	AT86RF230 Revision A
	2	AT86RF230 Revision B

Register 0x1E (MAN_ID_0)

Bit	7	6	5	4	3	2	1	0	
0x1E	MAN_ID_0								MAN_ID_0
Read/Write	R	R	R	R	R	R	R	R	
Reset value	0	0	0	1	1	1	1	1	

- **Bit [7:0] – MAN_ID_0**

Bits [7:0] of the 32 bit JEDEC manufacturer ID are stored in register bits MAN_ID_0. Bits [15:8] are stored in register 0x1F (MAN_ID_1). The highest 16 bits of the ID are not stored in registers.

Table 6-5. JEDEC Manufacturer ID – Bits [7:0]

Register Bits	Value[7:0]	Description
MAN_ID_0	0x1F	Atmel JEDEC manufacturer ID Bits [7:0] of 32 bit manufacturer ID: 00 00 00 1F

Register 0x1F (MAN_ID_1)

Bit	7	6	5	4	3	2	1	0	
0x1F	MAN_ID_1								MAN_ID_1
Read/Write	R	R	R	R	R	R	R	R	
Reset value	0	0	0	0	0	0	0	0	

- **Bit [7:0] – MAN_ID_1**

Bits [15:8] of the 32 bit JEDEC manufacturer ID are stored in register bits MAN_ID_1. Bits [7:0] are stored in register 0x1E (MAN_ID_0). The upper 16 bits of the ID are not stored in registers.

Table 6-6. JEDEC Manufacturer ID – Bits [15:8]

Register Bits	Value[7:0]	Description
MAN_ID_1	0x00	Atmel JEDEC manufacturer ID Bits [15:8] of 32 bit manufacturer ID: 00 00 00 1F

6.4 Sleep/Wake-up and Transmit Signal (SLP_TR)

The SLP_TR signal is a multi-functional pin. Its function relates to the current state of the AT86RF230 and is summarized in Table 6-7. The radio transceiver states are explained in detail in section 7.

Table 6-7. SLP_TR Multi-Functional Pin

Radio Transceiver Status	Function	Transition	Description
TRX_OFF	Sleep	L → H	Takes the radio transceiver into SLEEP state
SLEEP	Wakeup	H → L	Takes the radio transceiver into TRX_OFF state
RX_ON	Disable CLKM	L → H	Takes the radio transceiver into RX_ON_NOCLK state and disables CLKM
RX_ON_NOCLK	Enables CLKM	H → L	Takes the radio transceiver into RX_ON state and enables CLKM
RX_AACK_ON	Disable CLKM	L → H	Takes the radio transceiver into RX_AACK_ON_NOCLK state and disables CLKM
RX_AACK_ON_NOCLK	Enables CLKM	H → L	Takes the radio transceiver into RX_AACK_ON state and enables CLKM
PLL_ON	TX start	L → H	Starts frame transmission
TX_ARET_ON	TX start	L → H	Starts TX_ARET transaction

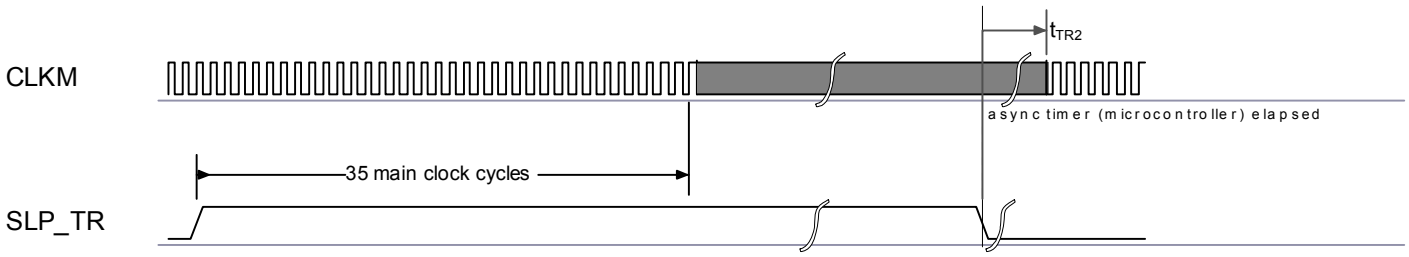
In states PLL_ON and TX_ARET_ON, the SLP_TR pin is used as trigger input to initiate a TX transaction. Here pin SLP_TR is sensitive on rising edge only.

After initiating a state change by a rising edge at pin SLP_TR in radio transceiver states TRX_OFF, RX_ON or RX_AACK_ON the radio transceiver remains in the new state as long as the pin is logical high and returns to the preceding state with the falling edge.

The SLEEP state is used when radio transceiver functionality is not required, and thus the AT86RF230 can be powered down to reduce the overall power consumption.

A power-down scenario is shown in Figure 6-15. When the radio transceiver is in TRX_OFF state the microcontroller force the AT86RF230 to SLEEP by setting SLP_TR = H. If the CLKM output provides a clock to the microcontroller this clock is switched off after 35 clock cycles. This enables a microcontroller in a synchronous system to complete its power-down routine and prevent dead-lock situations. The AT86RF230 awakes when the microcontroller releases pin SLP_TR. This concept provides the lowest possible power consumption.

Figure 6-15. Sleep and Wake-up Initiated by Asynchronous Microcontroller Timer Output (for Timing Information see Table 7-1)



For synchronous systems, where CLKM is used as a microcontroller clock source and the SPI master clock (SCLK) is directly derived from CLKM, the AT86RF230 supports an additional power-down mode for receive operating states RX_ON and RX_AACK_ON.

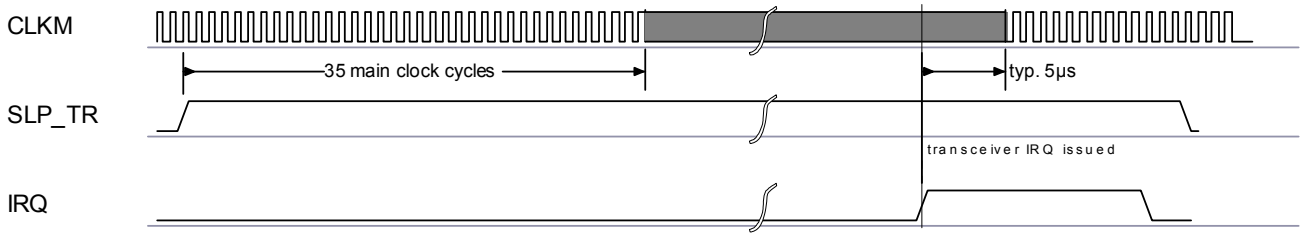
If an incoming frame is expected and no other applications are running on the microcontroller, it can be powered down without missing incoming frames.

This can be achieved by a rising edge on pin SLP_TR which turns off the CLKM output 35 clock cycles afterwards. The radio transceiver state changes from RX_ON or RX_AACK_ON to RX_ON_NOCLK or RX_AACK_ON_NOCLK respectively.

In case that a frame is received the radio transceiver enters the state BUSY_RX/BUSY_RX_AACK and the clock output CLKM is automatically switched on again. This scenario is shown in Figure 6-16.

The power consumption of the radio transceiver is similar in state RX_ON_NOCLK/RX_AACK_ON_NOCLK and state RX_ON, because only the CLKM output is switched off.

Figure 6-16. Wake-Up Initiated by Radio Transceiver Interrupt



6.5 Interrupt Logic

6.5.1 Overview

The AT86RF230 differentiates between six interrupt events. Each interrupt is enabled or disabled by writing the corresponding bit to the interrupt mask register 0x0E (IRQ_MASK). Internally, each interrupt is stored as a separate bit of the interrupt status register. All interrupt lines are combined via logical “OR” to one external interrupt line (IRQ). If the IRQ pin issues, the microcontroller shall read the interrupt status register 0x0F (IRQ_STATUS) to determine the reason for the interrupt. A read access to this register clears the interrupt status register and the IRQ pin, too. Interrupts are not cleared automatically when the event that caused them is not valid anymore. Exception: the PLL_LOCK IRQ clears the PLL_UNLOCK IRQ and vice versa. The supported interrupts for the Basic Operating Mode (see section 7.1) are summarized in Table 6-8.

Table 6-8. Interrupt Description in Basic Operating Mode

IRQ Name	Comments	Details
IRQ_7: BAT_LOW	Indicates a supply voltage below the programmed threshold.	Section 9.5.3
IRQ_6: TRX_UR	Indicates a Frame Buffer access violation (under run).	Section 9.3.3
IRQ_3: TRX_END	RX: Indicates the completion of a frame reception. TX: Indicates the completion of a frame transmission.	Section 7.1.3 Section 7.1.3
IRQ_2: RX_START	Indicates a SFD detection. The TRX_STATE changes to BUSY_RX.	Section 7.1.3
IRQ_1: PLL_UNLOCK	Indicates PLL unlock. The PA is turned off immediately, if the radio transceiver is in BUSY_TX/BUSY_TX_ARET state.	Section 9.7.4
IRQ_0: PLL_LOCK	Indicates PLL lock	Section 9.7.4

Using the Extended Operating Mode, the interrupts are handled in a slightly different way. A detailed description can be found in section 7.2.4.

6.5.2 Register Description

Register 0x0E (IRQ_MASK)

The IRQ_MASK register is used to enable (set register bit to 1) or disable (set register bit to 0) interrupt events by writing the corresponding bit to the interrupt mask register.

Bit	7	6	5	4	
0x0E	MASK_BAT_LOW	MASK_TRX_UR	Reserved		IRQ_MASK
Read/Write	R/W	R/W	R/W	R/W	
Reset value	1	1	1	1	

Bit	3	2	1	0	
0x0E	MASK_TRX_END	MASK_RX_START	MASK_PLL_UNLOCK	MASK_PLL_LOCK	IRQ_MASK
Read/Write	R/W	R/W	R/W	R/W	
Reset value	1	1	1	1	

If an interrupt will be enabled or disabled, it is recommended to read the interrupt status register 0x0F (IRQ_STATUS) first to clear the history.

Register 0x0F (IRQ_STATUS)

The IRQ_STATUS register contains the status of the individual interrupts. A read access to this register resets all interrupt bits.

Bit	7	6	5	4	
0x0F	BAT_LOW	TRX_UR	Reserved		IRQ_STATUS
Read/Write	R	R	R	R	
Reset value	0	0	0	0	

Bit	3	2	1	0	
0x0F	TRX_END	RX_START	PLL_UNLOCK	PLL_LOCK	IRQ_STATUS
Read/Write	R	R	R	R	
Reset value	0	0	0	0	

By reading the register after an interrupt is signaled at IRQ pin, the reason for the interrupt can be identified.

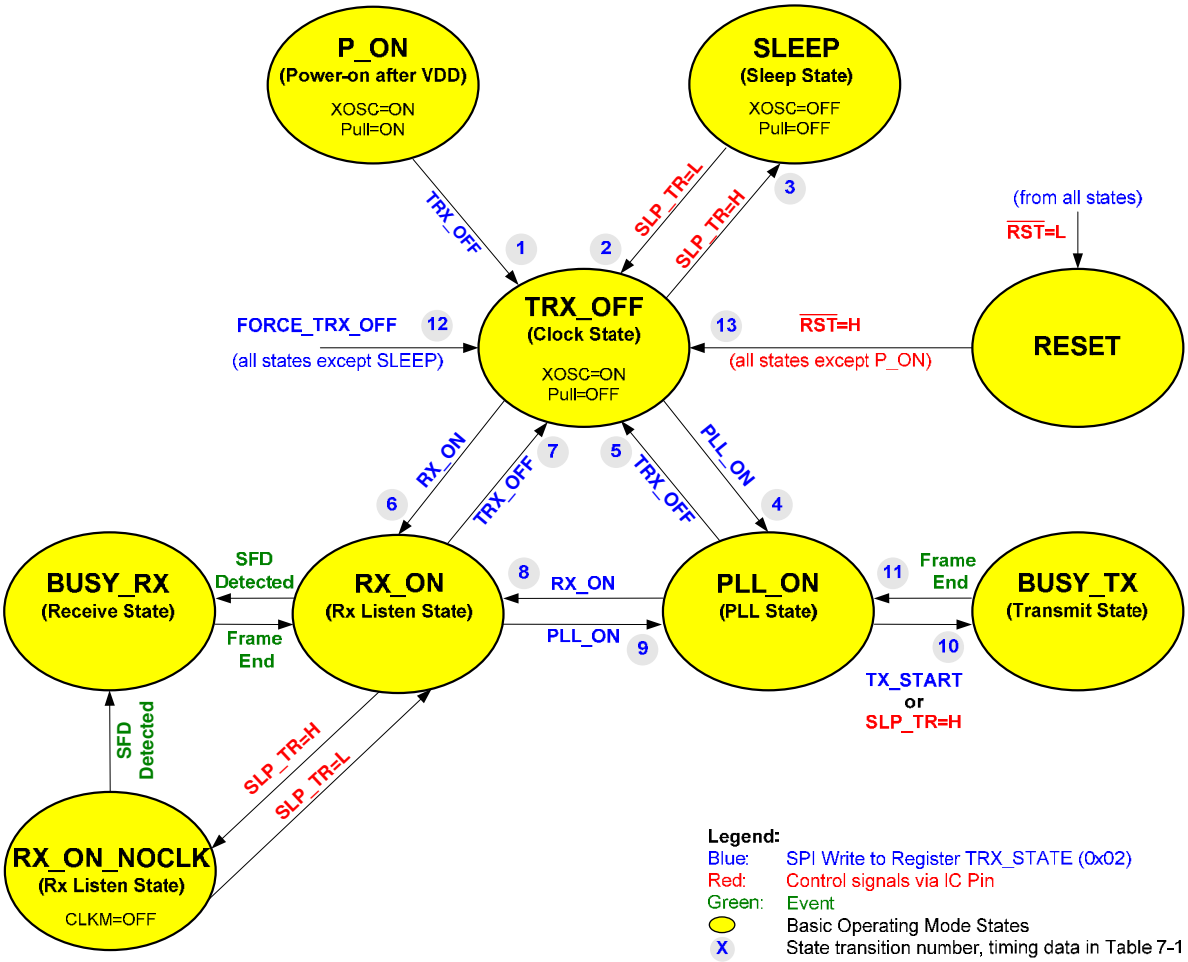
A detailed description of the individual interrupts can be found in Table 6-8.

7 Operating Modes

7.1 Basic Operating Mode

This section summarizes all states to provide the basic functionality of the AT86RF230, such as receiving and transmitting frames, and powering up and down. The Basic Operating Mode is designed for IEEE 802.15.4 applications; the corresponding radio transceiver states are shown in Figure 7-1.

Figure 7-1. Basic Operating Mode State Diagram (for State Transition Timing Data Refer to Table 7-1)



7.1.1 State Control

The radio transceiver state is controlled by two signal pins (SLP_TR, $\overline{\text{RST}}$) and the register 0x02 (TRX_STATE). A successful state change shall be confirmed by reading the radio transceiver status from register 0x01 (TRX_STATUS).

If TRX_STATUS = 0x1F (STATE_TRANSITION_IN_PROGRESS) the AT86RF230 is on a state transition. Do not try to initiate a further state change while the radio transceiver is in STATE_TRANSITION_IN_PROGRESS.

The pin SLP_TR is a multifunctional pin. Depending on radio transceiver state the rising edge of SLP_TR causes the following state transitions:

- TRX_OFF → SLEEP
- RX_ON → RX_ON_NOCLK
- PLL_ON → BUSY_TX

For further details to the functionality of pin SLP_TR refer to section 6.4.

The pin $\overline{\text{RST}}$ causes a reset of all registers (register bits CLKM_SHA_SEL and CLKM_CTRL are shadowed, for details refer to section 9.6.4) and forces the radio transceiver into TRX_OFF state. However, if the device is in the P_ON state it remains in the P_ON state.

For all states, the state change commands FORCE_TRX_OFF or TRX_OFF lead to a transition into TRX_OFF state. If the radio transceiver is in the BUSY_RX or BUSY_TX state, the command FORCE_TRX_OFF interrupts the active receiving or transmitting process, and forces an immediate transition. In contrast to that the TRX_OFF command is stored until a currently ongoing frame reception or transmission has finished. After the end of the frame, the transition to TRX_OFF is performed.

The completion of each requested state change shall always be confirmed by reading the register 0x01 (TRX_STATUS).

7.1.2 Basic Operating Mode Description

7.1.2.1 P_ON - Power-on after V_{DD}

When the external supply voltage (V_{DD}) is firstly applied to the radio transceiver, the system goes into the P_ON state. An on-chip reset is performed. The crystal oscillator gets activated and the master clock is provided to the CLKM pin after the crystal oscillator has stabilized. CLKM can be used as a clock source to the microcontroller.

The on-chip power-on-reset sets all registers to their default values. A dedicated reset signal from the microcontroller at the pin $\overline{\text{RST}}$ is not necessary, but recommended for hardware/software synchronization reasons. The reset impulse should have a minimum length as specified in section 11.4, see parameter 11.4.12.

All digital inputs have pull-up or pull-down resistors (see Table 4-4). This is necessary to support microcontrollers where GPIO signals are floating after reset. The input pull-up and pull-down resistors are disabled when the radio transceiver leaves the P_ON state.

Prior to leaving P_ON, the microcontroller must set all digital input pins (MOSI, $\overline{\text{RST}}$, SCLK, $\overline{\text{SEL}}$, SLP_TR) to their default operating values.

Once the supply voltage has stabilized and the crystal oscillator has settled (see section 11.5, parameter 11.5.5), a SPI write access to the register 0x02 (TRX_STATE) with the command TRX_OFF or FORCE_TRX_OFF initiates a state change from P_ON to TRX_OFF.

7.1.2.2 SLEEP – Sleep State

In SLEEP state, the entire radio transceiver is disabled. No circuitry is operating. The AT86RF230 current consumption is reduced to leakage current only.

This state can only be entered from state TRX_OFF by setting the pin SLP_TR = H. If CLKM is enabled, the SLEEP state is entered 35 CLKM cycles after the rising edge. At that time CLKM is turned off. If the CLKM output is turned off (bits CLKM_CTRL = 0 in register 0x03), the SLEEP state is entered immediately.

Setting SLP_TR = L returns the radio transceiver to the TRX_OFF state. It is recommended that pin SLP_TR should be active for a minimum of 40 CLKM cycles to completely power down the radio transceiver.

During SLEEP state, the register contents remain valid while the content of the Frame Buffer is cleared.

7.1.2.3 TRX_OFF – Clock State

In TRX_OFF state the SPI interface and the crystal oscillator are enabled. The digital voltage regulator (DVREG) is enabled and provides 1.8V to the digital core to make the Frame Buffer available (see section 9.1). The microcontroller can access all digital functions and if enabled, the CLKM output supplies a clock. The pin SLP_TR is enabled for state control.

7.1.2.4 PLL_ON – PLL State

Entering the PLL_ON state from TRX_OFF state enables the analog voltage regulator (AVREG) first. After the voltage regulator has been settled, the PLL frequency synthesizer is enabled. When the PLL has been settled at the receive frequency, a successful PLL lock is indicated by issuing a PLL_LOCK interrupt.

If an RX_ON command is issued in PLL_ON state, the receiver is immediately enabled. If the PLL has not been settled before, actual frame reception can only happen once the PLL has locked.

The PLL_ON state corresponds to the TX_ON state in IEEE 802.15.4.

7.1.2.5 RX_ON and BUSY_RX – RX Listen and Receive State

In RX_ON state the receiver blocks and the PLL frequency synthesizer are enabled.

The AT86RF230 receive mode is internally divided into RX_ON state and BUSY_RX state. There is no difference between these states with respect to the analog radio transceiver circuitry, which is always turned on. During RX_ON state, only the preamble detection of the digital signal processing is running. When a preamble and a valid SFD are detected, also the digital receiver is turned on. The radio transceiver enters the BUSY_RX state and a RX_START interrupt is generated.

During the frame reception frame data are stored continuously in the Frame Buffer until the last byte was received. The completion of the frame reception is indicated by a TRX_END interrupt and the radio transceiver reenters the state RX_ON. At the same time the register bit RX_CRC_VALID (register 0x06) is updated with the result of the FCS check (see section 8.2).

Note, settings of address registers 0x20 to 0x2B do not affect the frame reception in Basic Operating Mode. Frame address filtering is only applied when using the Extended Operating Mode (see section 7.2).

7.1.2.6 RX_ON_NOCLK – RX Listen State without CLKM

If the radio transceiver is listening for an incoming frame and the microcontroller is not running an application, the microcontroller can be powered down to decrease the total system power consumption. This special power-down scenario for systems running in clock synchronous mode (see section 6.4) is supported by the AT86RF230 using the state RX_ON_NOCLK.

This state can only be entered by setting SLP_TR = H while the AT86RF230 is in the RX_ON state. The CLKM pin is disabled 35 clock cycles after the rising edge at the SLP_TR pin. This allows the microcontroller to complete its power-down sequence. The

reception of a frame is indicated to the microcontroller by a RX_START interrupt. CLKM is turned on again, and the radio transceiver enters the BUSY_RX state (see section 6.4, Figure 6-16).

The end of the transaction is indicated to the microcontroller by a TRX_END interrupt. After the transaction has been completed, the radio transceiver enters the RX_ON state. The radio transceiver only reenters the RX_ON_NOCLK state, when the next rising edge at pin SLP_TR occurs.

If the radio transceiver is in the RX_ON_NOCLK state, and the SLP_TR pin is reset to logic low, it enters the RX_ON state, and it starts to supply clock on the CLKM pin again.

In states RX_ON_NOCLK and RX_ON, the current consumption is about the same, because only the CLKM output is switched off in state RX_ON_NOCLK.

7.1.2.7 BUSY_TX – Transmit State

A transmission can only be started in state PLL_ON. There are two ways to start a transmission:

- Rising edge of SLP_TR
- TX_START command to register 0x02 (TRX_STATE).

Either of these causes the AT86RF230 to enter the BUSY_TX state.

During the transition to BUSY_TX state, the PLL frequency shifts to the transmit frequency. Transmission of the first data chip of the preamble starts after 16 µs to allow PLL settling and PA ramping, see Figure 7-2. After transmission of the preamble and the SFD, the Frame Buffer content is transmitted.

The last two bytes to be transmitted are the FCS (see Figure 8-2). The radio transceiver can be configured to autonomously compute the FCS bytes and append it to the transmit data. The register bit TX_AUTO_CRC_ON in register 0x05 (PHY_TX_PWR) needs to be set to 1 to enable this feature. For further details refer to section 8.2.When the frame transmission is completed, the radio transceiver automatically turns off the power amplifier, generates a TRX_END interrupt and returns to PLL_ON state.

Note that in case the PHR indicates a frame length of zero, the transmission is aborted.

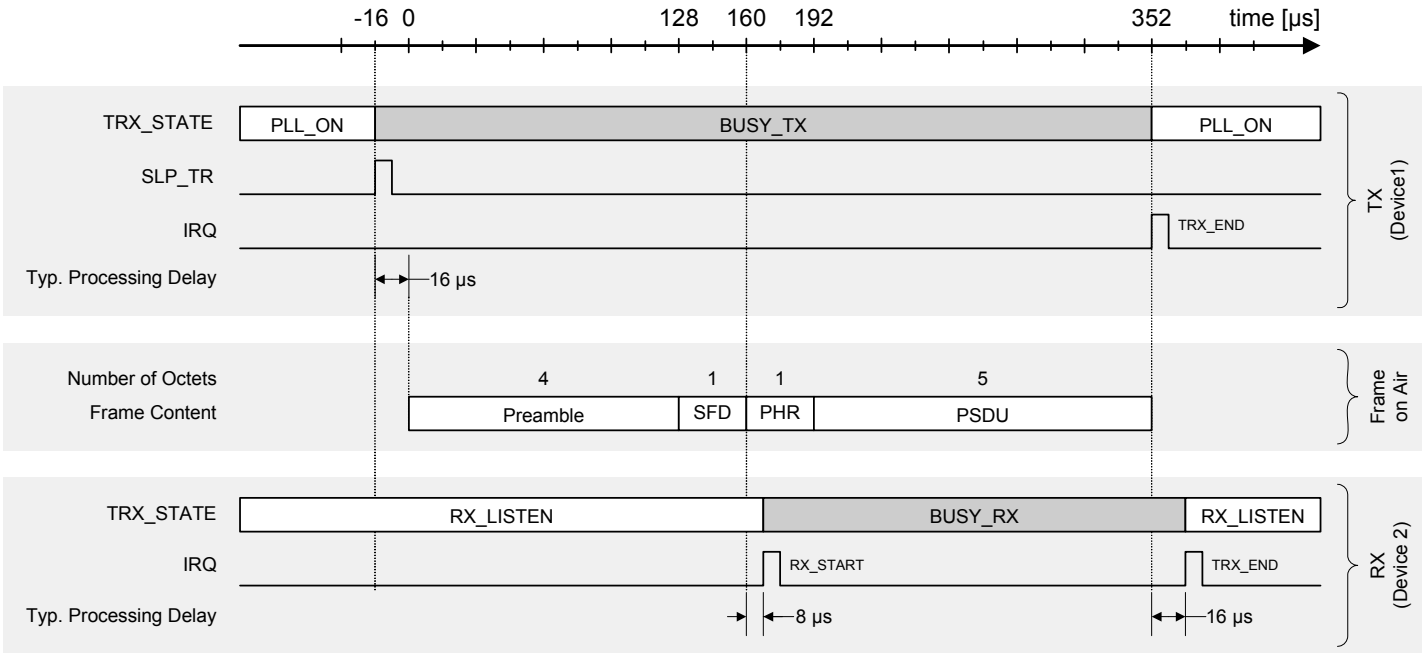
7.1.3 Interrupt Handling in Basic Operating Mode

All interrupts of the AT86RF230 (see Table 6-8) are supported during operation in Basic Operating Mode.

Two interrupts are used to support RX and TX operation of the radio transceiver. On receive the RX_START interrupt indicates the detection of a valid SFD. The TRX_END interrupt indicates the completion of the frame reception or frame transmission.

Figure 7-2 shows a receive/transmit transaction and the related interrupt events in Basic Operating Mode. One device is assumed to operate as transmitter (device 1), the second one as receiver (device 2). Processing delays are typical values.

Figure 7-2. Timing of RX_START and TRX_END Interrupts in Basic Operating Mode (see register 0x0F)



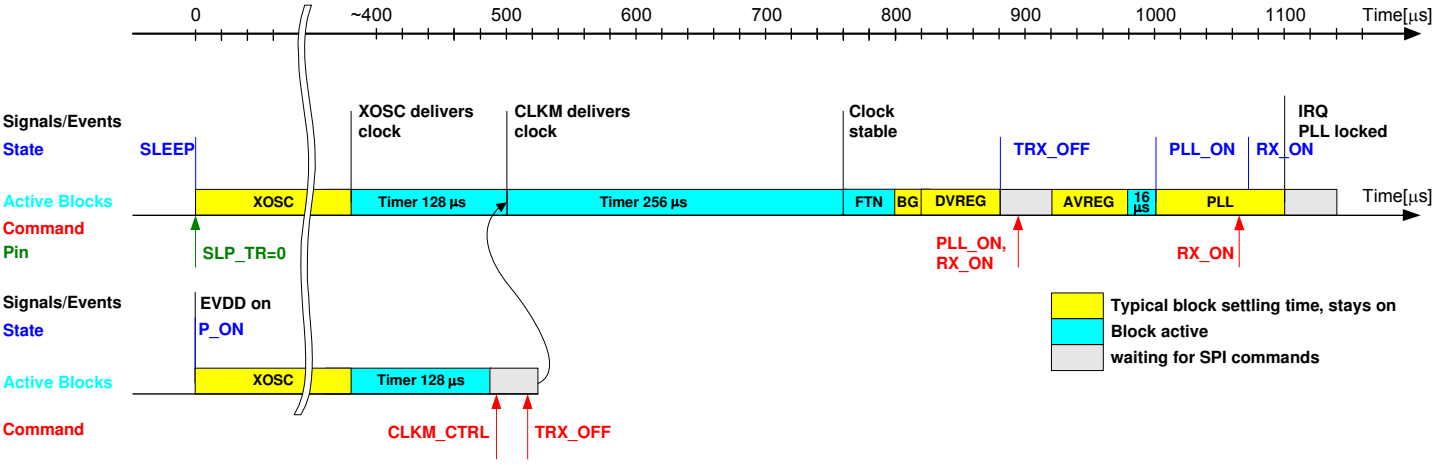
7.1.4 Basic Mode Timing

The following paragraphs depict the transitions between states and their timing.

7.1.4.1 Power-on and Wake-up Procedure

The power-on sequence and the wake-up procedure is shown in Figure 7-3.

Figure 7-3. Wake-Up Procedure from SLEEP and P_ON to RX_ON (PLL Locked)



Setting pin SLP_TR = L in SLEEP state enables the crystal oscillator. After 0.4 ms (typ.), the internal clock signal is available. After another 128 µs the clock signal is provided at the CLKM pin if enabled. An additional 256 µs timer ensures that frequency stability is sufficient to drive filter tuning (FTN) and the PLL. After the digital voltage regulator has been settled, the radio transceiver enters the TRX_OFF state and waits for further commands.

In TRX_OFF state, entering the commands PLL_ON or RX_ON initiates a ramp-up sequence of the analog voltage regulator. RX_ON state can be entered any time during PLL_ON state regardless whether the PLL has already locked.

When the wake-up sequence is started from P_ON state (V_{DD} first applied to the radio transceiver) the state machine stops after the 128 µs timer expires to wait for a valid TRX_OFF command from the microcontroller. The default CLKM frequency in P_ON state is 1 MHz.

7.1.4.2 Reset Procedure

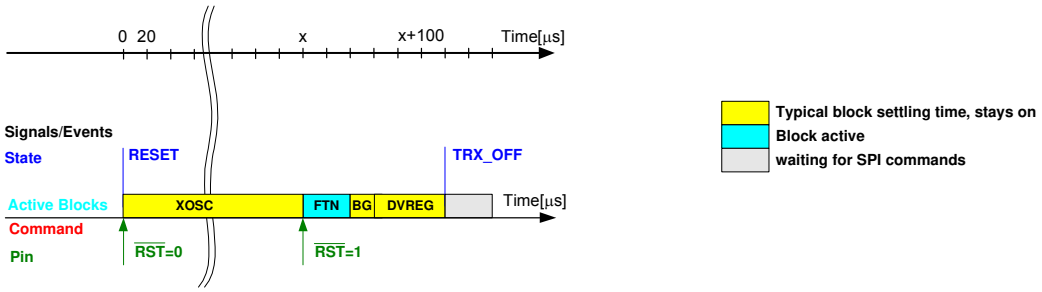
$\overline{RST}$ = L sets all registers to their default values (see Table 12-2). Exception, register bits CLKM_CTRL of register 0x03 (TRX_CTRL_0) are shadowed at reset. For details refer to section 9.6.4.

After releasing the reset pin ($\overline{RST}$ = H) a calibration cycle of the FTN is started and the digital voltage regulator is turned on. The state TRX_OFF is entered and the status of the main state machine changes from STATE_TRANSITION_IN_PROGRESS to TRX_OFF.

This sequence is identical for all radio transceiver states except in state P_ON. The state machine does not leave the state P_ON after a reset in this state. Instead, the procedure described in section 7.1.2.1 must be followed to enter the TRX_OFF state for the very first time. Figure 7-4 describes the reset procedure once the P_ON state was left.

Note that the access to the device should not occur earlier than 625 ns after releasing the reset pin. During the reset procedure the SPI interface shall be inactive ($\overline{SEL}$ = H; SCLK = L).

Figure 7-4. Reset Procedure



7.1.4.3 State Transition Timing

The transition numbers (first column) in Table 7-1 correspond to Figure 7-1 and do not include SPI access time if not otherwise stated. See measurement setup in Figure 5-1.

Table 7-1. State Transition Timing

No	Symbol	Transition	Time [µs] (tppical)	Comments
1	t_{TR1}	P_ON → TRX_OFF	880	Depends on external bypass capacitor at DVDD (1 µF nom) and crystal oscillator setup (CL = 10 pF)
2	t_{TR2}	SLEEP → TRX_OFF	880	Depends on external bypass capacitor at DVDD (1 µF nom) and crystal oscillator setup (CL = 10 pF)
3	t_{TR3}	TRX_OFF → SLEEP	35	f_{CLKM} = 1 MHz
4	t_{TR4}	TRX_OFF → PLL_ON	180	Depends on external bypass capacitor at AVDD (1 µF nom).

No	Symbol	Transition	Time [µs] (tppical)	Comments
5	t_{TR5}	PLL_ON → TRX_OFF	1	
6	t_{TR6}	TRX_OFF → RX_ON	180	Depends on external bypass capacitor at AVDD (1 µF nom).
7	t_{TR7}	RX_ON → TRX_OFF	1	
8	t_{TR8}	PLL_ON → RX_ON	1	
9	t_{TR9}	RX_ON → PLL_ON	1	
10	t_{TR10}	PLL_ON → BUSY_TX	16	When asserting SLP_TR pin first symbol transmission is delayed by 16 µs (PLL settling and PA ramp up).
11	t_{TR11}	BUSY_TX → PLL_ON	32	32 µs PLL settling time
12	t_{TR12}	All states → TRX_OFF	1	Using TRX_CMD FORCE_TRX_OFF (see register 0x02), not valid for SLEEP mode
13	t_{TR13}	$\overline{RST}$ = L → TRX_OFF	120	Depends on external bypass capacitor at DVDD (1 µF nom), not valid for P_ON mode

The state transition timing is calculated based on the timing of the individual blocks as shown in Figure 7-3. The worst case values include maximum operating temperature, minimum supply voltage, and device parameter variations.

Table 7-2. Block Settling Time

Block	Time [µs] (typical)	Time [µs] (worst case)	Comments
XOSC	500	1000	Until clock signal is provided at CLKM pin. Depends on crystal Q factor and load capacitor
DVREG	60	1000	Depends on external bypass capacitor at DVDD (CB3 = 1 µF nom., 10 µF worst case)
AVREG	60	1000	Depends on external bypass capacitor at AVDD (CB1 = 1 µF nom., 10 µF worst case)
PLL, initial	100	150	
PLL, RX → TX	16		PLL settling time
PLL, TX → RX	32		PLL settling time

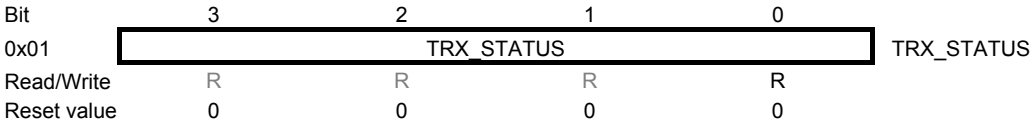
7.1.5 Register Description

Register 0x01 (TRX_STATUS)

The TRX_STATUS register signals the current state of the radio transceiver as well as the status of the CCA measurement. Note, a read access to the register clears bits CCA_DONE and CCA_STATUS.

This register is used for Extended and Basic Operating Mode. The Extended Operating Mode functionality is described in section 7.2.

Bit	7	6	5	4	
0x01	CCA_DONE	CCA_STATUS	Reserved	TRX_STATUS	TRX_STATUS
Read/Write	R	R	R	R	
Reset value	0	0	0	0	



- **Bit 7 – CCA_DONE**

Refer to section 8.6.

- **Bit 6 – CCA_STATUS**

Refer to section 8.6.

- **Bit 5 – Reserved**
- **Bit [4:0] – TRX_STATUS**

The register bits TRX_STATUS signal the current radio transceiver status. If the requested state transition is not completed yet, the TRX_STATUS returns STATE_TRANSITION_IN_PROGRESS. State transition timings are defined in Table 7-1.

Table 7-3. Radio Transceiver Status, Register Bits TRX_STATUS

Register Bits	Value[4:0]	State Description
TRX_STATUS	0x00	P_ON
	0x01	BUSY_RX
	0x02	BUSY_TX
	0x06	RX_ON
	0x08	TRX_OFF (Clock State)
	0x09	PLL_ON (TX_ON)
	0x0F	SLEEP
	0x11(1)	BUSY_RX_AACK
	0x12(1)	BUSY_TX_ARET
	0x16(1)	RX_AACK_ON
	0x19(1)	TX_ARET_ON
	0x1C	RX_ON_NOCLK
	0x1D(1)	RX_AACK_ON_NOCLK
	0x1E(1)	BUSY_RX_AACK_NOCLK
	0x1F	STATE_TRANSITION_IN_PROGRESS
		All other values are reserved
Notes:	1. Extended Operating Mode only, refer to section 7.2.	

Register 0x02 (TRX_STATE)

The register TRX_STATE controls the radio transceiver states via register bits TRX_CMD. The status and the result of a TX_ARET/RX_AACK transaction is indicated by register bits TRAC_STATUS.

A successful state transition shall be confirmed by reading register bits TRX_STATUS in register 0x01 (TRX_STATUS).

This register is used for Basic and Extended Operating Mode. The Extended Operating Mode functionality is described in section 7.2.

Bit	7	6	5	4	
0x02	TRAC_STATUS			TRX_CMD	TRX_STATE
Read/Write	R	R	R	R/W	
Reset value	0	0	0	0	

Bit	3	2	1	0	
0x02	TRX_CMD				TRX_STATE
Read/Write	R/W	R/W	R/W	R/W	
Reset value	0	0	0	0	

- **Bit [7:5] – TRAC_STATUS**

Refer to section 7.2.6.

- **Bit [4:0] – TRX_CMD**

A write access to register bits TRX_CMD initiates a radio transceiver state transition towards the new state.

Table 7-4. State Control Commands, Register Bits TRX_CMD

Register Bits	Value[4:0]	State Transition towards
TRX_CMD	0x00(1)	NOP
	0x02(2)	TX_START
	0x03	FORCE_TRX_OFF
	0x06	RX_ON
	0x08	TRX_OFF (Clock State)
	0x09	PLL_ON (TX_ON)
	0x16(3)	RX_AACK_ON
	0x19(3)	TX_ARET_ON
		All other values are reserved

Notes:
1. TRX_CMD = 0 after power-on reset (POR) only
2. Frame transmission starts 16 µs (1 symbol) after TX_START
3. Extended Operating Mode only, refer to section 7.2

7.2 Extended Operating Mode

The Extended Operating Mode goes beyond the basic radio transceiver functionality provided by the Basic Operating Mode. Specific functionality requested by the IEEE 802.15.4-2003 standard is supported such as automatic acknowledgement and automatic frame retransmission. This results in a more efficient IEEE 802.15.4-2003 software MAC implementation including reduced code size, the possible use of a smaller microcontroller or the ability to simplify the handling of time-critical tasks.

The Extended Operating Mode is designed to support IEEE 802.15.4-2003 standard compliant frames. While using the Extended Operating Mode, the AT86RF230 radio transceiver supports:

- Automatic address filtering
- Automatic acknowledgement (RX_AACK) and
- Automatic CSMA-CA with optional frame retransmission (TX_ARET)

Note, the Extended Operating Mode does not support slotted CSMA-CA.

The RX_AACK transaction consists of:

- Frame reception
- Address filtering and automatic FCS check
- Interrupt indicating frame reception, if it passes address filtering and FCS check
- Automatic ACK frame transmission, if necessary

For details on RX_AACK transaction see section 7.2.3.1.

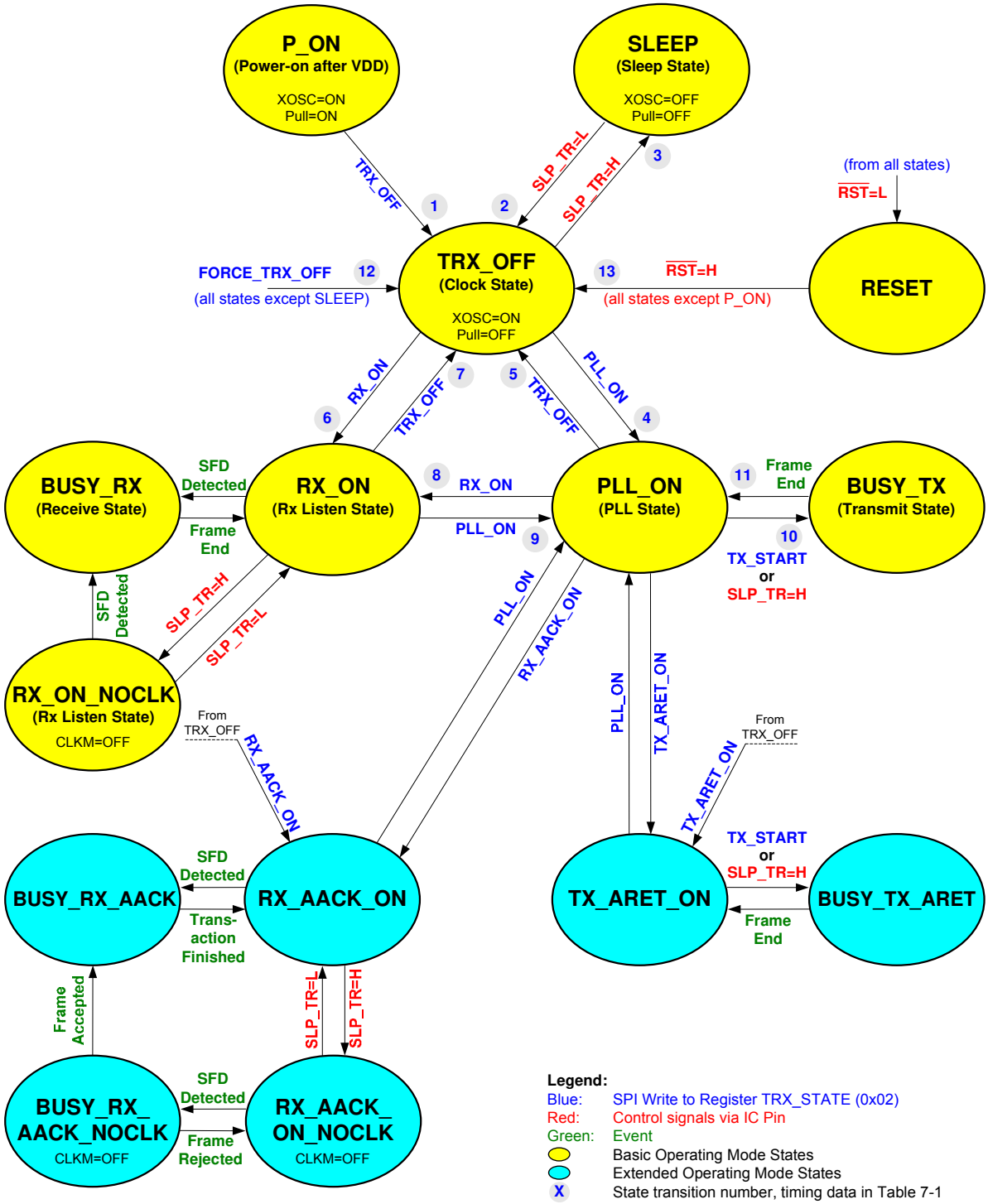
The TX_ARET transaction consists of:

- CSMA-CA including automatic retry
- Frame transmission and automatic FCS field generation
- Reception of ACK frame, if requested
- Automatic retry of transmissions if ACK was expected but not received
- Interrupt and transaction return code generation

For details on TX_ARET transaction see section 7.2.3.2.

The AT86RF230 state diagram including the Extended Operating Mode states is shown in Figure 7-5. Yellow marked states represent the Basic Operating Mode, blue marked states represent the Extended Operating Mode.

Figure 7-5. Extended Operating Mode State Diagram



7.2.1 State Control

The Extended Operating Mode states can be entered from states TRX_OFF or PLL_ON as described by the state diagram in Figure 7-5. The completion of each requested state change shall always be confirmed by reading the register 0x01 (TRX_STATUS).

RX_AACK:

The state RX_AACK_ON is entered by writing the command RX_AACK_ON to the register bits TRX_CMD in register 0x02 (TRX_STATE). The state change shall be confirmed by reading register 0x01 (TRX_STATUS) that changes to RX_AACK_ON or BUSY_RX_AACK on success.

TX_ARET:

Similarly, TX_ARET_ON state is activated by setting register bits TRX_CMD (register 0x02) to TX_ARET_ON. The radio transceiver is in the TX_ARET_ON state after TRX_STATUS (register 0x01) has changed to TX_ARET_ON.

Notes:

1. It is not recommended to use the FORCE_TRX_OFF command while being in state BUSY_TX_ARET without appending a SLEEP cycle by activating SLP_TR for at least 2 µs.
2. After state transition from state RX_AACK_ON to state PLL_ON, start of frame transmission shall be confirmed by reading register 0x01 (TRX_STATUS). If register bits TRX_STATUS do not return BUSY_TX during frame transmission, the frame transmission needs to be initiated again. If the frame has been downloaded before initiating the frame transmission, it has to be downloaded again.

7.2.2 Configuration

The use of the Extended Operating Mode is based on Basic Operating Mode functionality. Only features beyond the basic radio transceiver functionality are described in the following sections. For details to the Basic Operating Mode refer to section 7.1.

When using the RX_AACK or TX_ARET modes, the following registers needs to be configured.

RX_AACK:

- Setup registers 0x20 – 0x2B for PAN-ID and IEEE addresses
- Set register bit AACK_SET_PD (register 0x2E)
- Configure register bit I_AM_COORD (register 0x2E)

TX_ARET:

- Configure CSMA-CA
  - MAX_FRAME_RETRIES (register 0x2C)
  - MAX_CSMA_RETRIES (register 0x2C)
  - CSMA_SEED (registers 0x2D, 0x2E)
  - MIN_BE (register 0x2E)
- Configure CCA (see section 8.7)

The MIN_BE register bits (register 0x2E) sets the minimum back-off exponent (refer to IEEE 802.15.4-2003 section 7.5.1.3), and the CSMA_SEED_0 and CSMA_SEED_1 register bits (registers 0x2D, 0x2E) define a random seed for the back-off-time random-number generator in the AT86RF230. The register bits MAX_CSMA_RETRIES (register 0x2C) configures how often the radio transceiver retries the CSMA-CA algorithm after a busy channel is detected. MAX_FRAME_RETRIES (register 0x2C) defines the maximum number of frame retransmissions.

7.2.3 Extended Operating Mode Description

7.2.3.1 RX_AACK_ON – Receive with Automatic ACK

In the RX_AACK_ON state, the radio transceiver listens for incoming frames. After detecting a frame start (SFD), the radio transceiver state changes to BUSY_RX_AACK (register 0x01) and the TRAC_STATUS bits (register 0x02) are set to INVALID. The AT86RF230 starts to parse the MAC header (MHR) and a filtering procedure as described in IEEE 802.15.4-2003 section 7.5.6.2. (third level filter rules) is applied accordingly. It accepts only frames that satisfy all of the following requirements (quote from IEEE 802.15.4 2003):

- The frame type subfield of the frame control field shall not contain an illegal frame type.
- If the frame type indicates that the frame is a beacon frame, the source PAN identifier shall match macPANId unless macPANId is equal to 0xFFFF, in which case the beacon frame shall be accepted regardless of the source PAN identifier.
- If a destination PAN identifier is included in the frame, it shall match macPANId or shall be the broadcast PAN identifier (0xFFFF).
- If a short destination address is included in the frame, it shall match either macShortAddress or the broadcast address (0xFFFF). Otherwise, if an extended destination address is included in the frame, it shall match an ExtendedAddress.
- If only source addressing fields are included in a data or MAC command frame, the frame shall be accepted only if the device is a PAN coordinator and the source PAN identifier matches macPANId. Any frames rejected by these rules are discarded.

The AT86RF230 requires to satisfy two additional rules:

- The frame type indicates that the frame is not an ACK frame (refer to Table 8-1)
- At least one address field must be present (refer to Table 8-2)

A frame is also discarded if the FCS is invalid. Otherwise, the TRX_END interrupt is issued and the register bits TRAC_STATUS are set to SUCCESS after the reception of the frame was completed. The microcontroller can then upload the frame.

The AT86RF230 detects whether an ACK frame needs to be sent. In that case, the radio transceiver automatically generates an ACK frame which is transmitted 12 symbol periods after the end of the received frame. If the frame that needs to be acknowledged is a valid MAC command data request frame, the content of register bit AACK_SET_PD in register 0x2E (CSMA_SEED_1) is copied to the frame pending subfield of the ACK and the frame sequence number is copied likewise. During these operations the radio transceiver remains in BUSY_RX_AACK state.

After the completion of the RX_AACK transaction the radio transceiver reenters the state RX_AACK_ON.

The flow diagram of the RX_AACK algorithm is shown in Figure 7-6.

The timing of an RX_AACK transaction is shown in Figure 7-7. It shows a reception of a data frame of length 10 with the ACK request bit set to one. A state change to BUSY_RX_AACK is performed after SFD detection. The completion of the frame reception is indicated by a TRX_END interrupt. The ACK frame is transmitted after a wait period of 12 symbols (192 µs).

Figure 7-6. Flow Diagram of RX_AACK

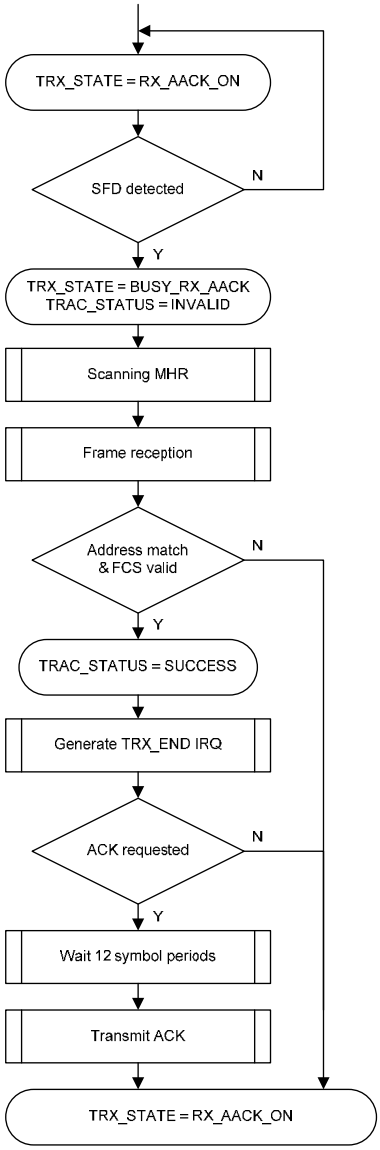
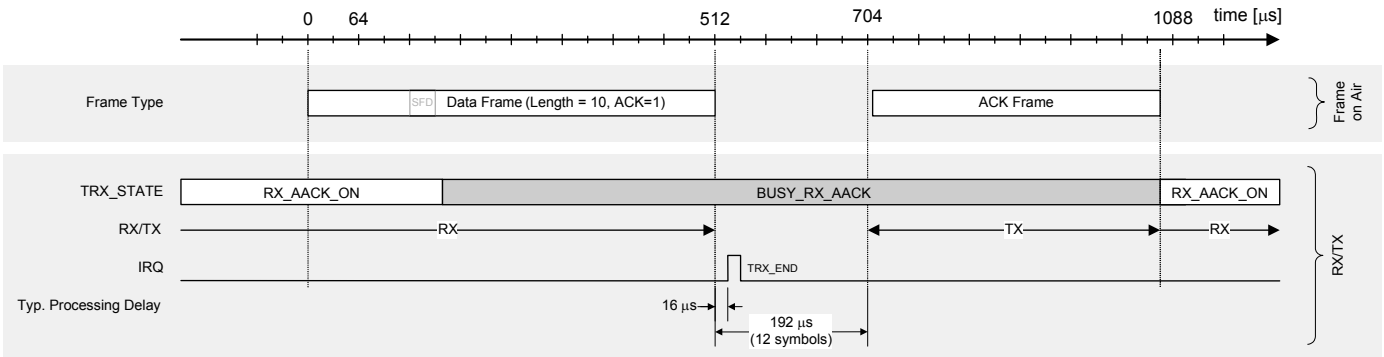


Figure 7-7. Example Timing of an RX_AACK Transaction



7.2.3.2 TX_ARET_ON – Transmit with Automatic CSMA-CA Retry

The implemented TX_ARET algorithm is shown in Figure 7-8.

The TX_ARET transaction is started by either a rising edge on SLP_TR pin or by writing a TX_START command to register 0x02 (TRX_STATE). The radio transceiver sets the TRAC_STATUS bits to INVALID and executes the CSMA-CA algorithm as defined by IEEE 802.15.4-2003 section 7.5.1.4. If a clear channel is detected during CSMA-CA execution, the radio transceiver proceeds to transmit the frame.

During frame transmission the AT86RF230 parses the frame control field of the downloaded frame to check if an ACK reply is expected. If an ACK is expected, the radio transceiver switches into receive mode to wait for valid ACK reply. An ACK is considered as valid if its FCS is correct, and if the sequence number of the ACK matches the sequence number of the previously transmitted frame.

If no valid ACK is received or a timeout (after 864 µs) occurred, the radio transceiver retries the entire transaction, including CSMA-CA execution. This repeats until the frame has been acknowledged or the maximum number of retransmissions (as set by the register bits MAX_FRAME_RETRIES in register 0x2C) has been reached. In this case, the TRX_END interrupt is issued and the value of TRAC_STATUS is set to NO_ACK.

If a valid ACK is found, the TRX_END interrupt is issued. The Frame Pending subfield of the ACK frame is parsed and the register bits TRAC_STATUS are updated. If the frame pending subfield of the ACK frame is set, TRAC_STATUS is updated with SUCCESS_DATA_PENDING, otherwise TRAC_STATUS is updated with SUCCESS.

While in receive mode for ACK reception, incoming data do not overwrite the Frame Buffer content. Transmit data in the Frame Buffer are not changed during the TX_ARET transaction.

If no ACK is expected, the radio transceiver issues a TRX_END interrupt after the frame transmission has been completed. The value of register bits TRAC_STATUS (register 0x02) is set to SUCCESS.

If the CSMA-CA did not detect a clear channel, the channel access is retried as often as specified by the register bits MAX_CSMA_RETRIES (register 0x2C). In case that CSMA-CA does not detect a clear channel after MAX_CSMA_RETRIES, the transaction is aborted and the TRX_END interrupt is issued. The TRAC_STATUS register bits are updated with CHANNEL_ACCESS_FAILURE.

Note that it is recommended to download the transmit data before starting a TX_ARET transaction.

Figure 7-8 Flow Diagram of TX_ARET

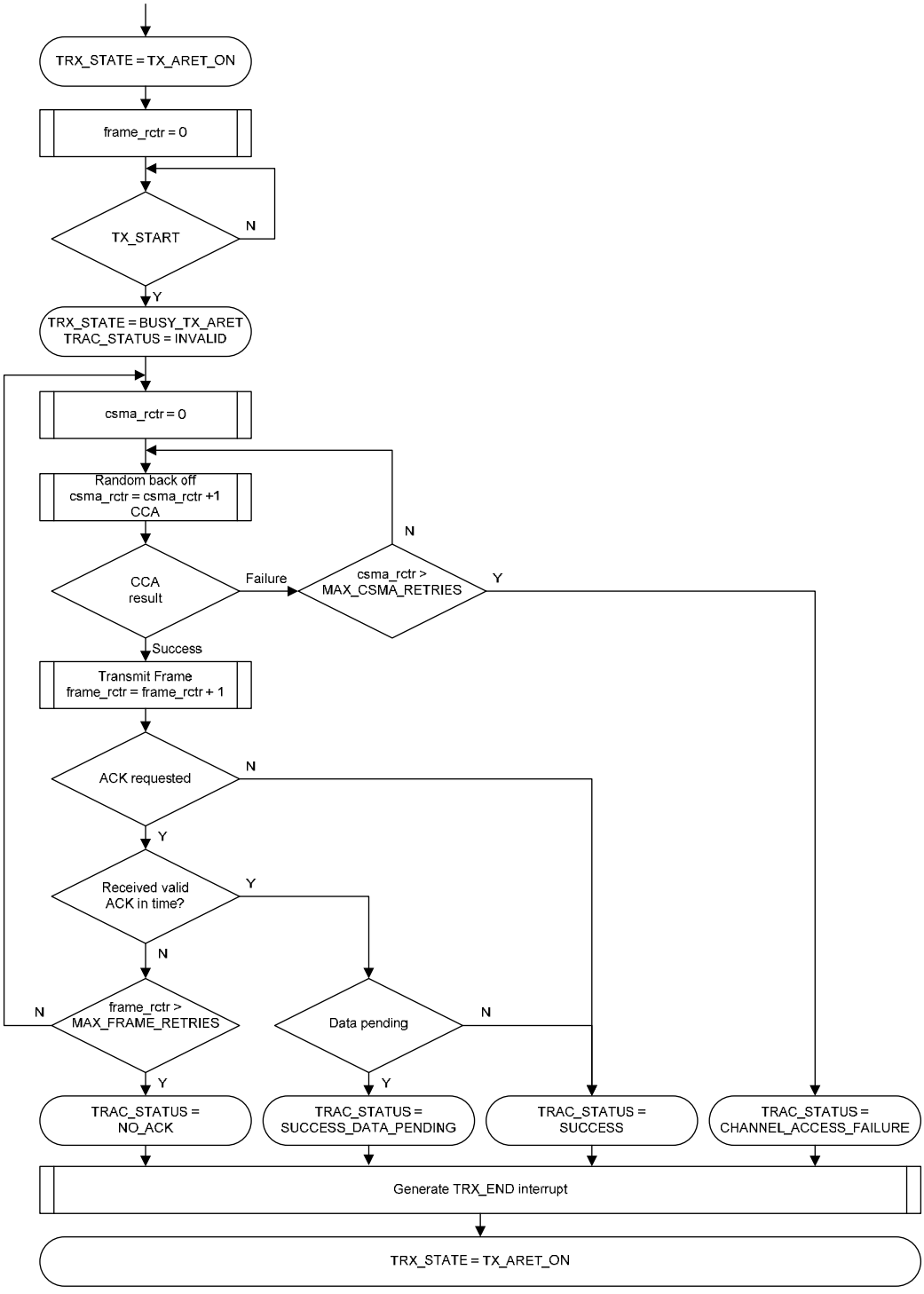
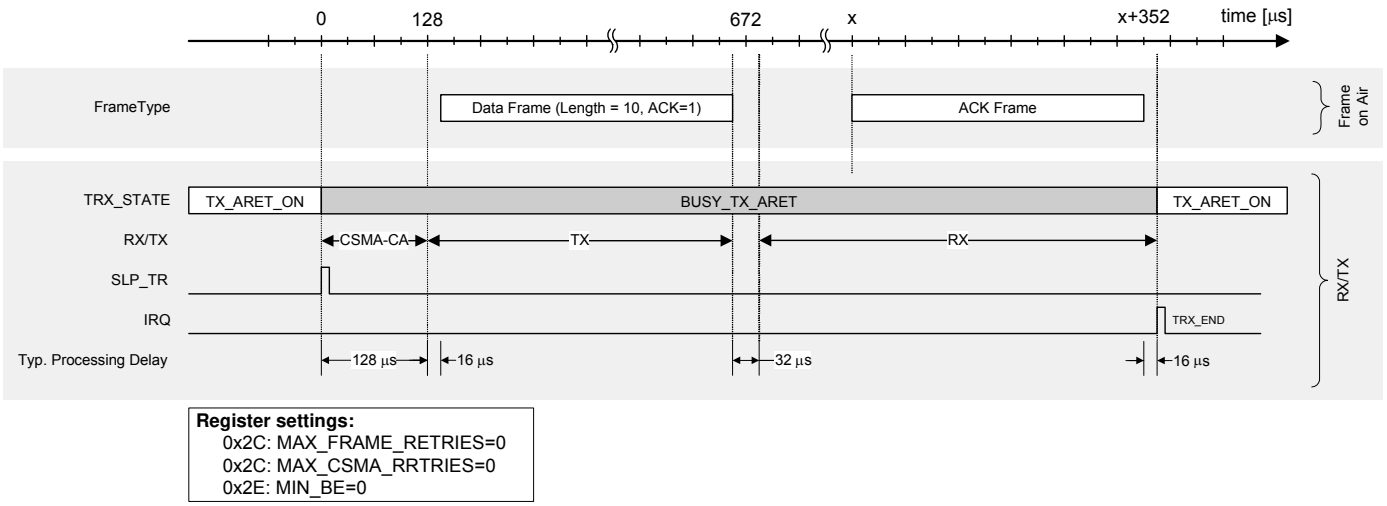


Figure 7-9 shows a TX_ARET transaction with the related timing. In this example a data frame of length 10 with ACK request is transmitted. Furthermore the following constrains are assumed:

- Register bits MIN_BE (register 0x2E) are set to 0 to not delay the execution of the CCA algorithm after the rising edge at pin SLP_TR
- A clear channel is assumed (no CSMA-CA retry, no frame retransmission).

Figure 7-9 Timing Example of a TX_ARET Transaction



7.2.3.3 RX_AACK_ON_NOCLK – RX_AACK_ON without CLKM

If the AT86RF230 is listening for an incoming frame and the microcontroller is not running an application, the microcontroller can be powered down to decrease the total system power consumption. This special power-down scenario for systems running in clock synchronous mode (see section 6.4) is supported by the AT86RF230 using the state RX_AACK_ON_NOCLK. The radio transceiver functionality in this state is based on that in state RX_AACK_ON (see section 7.2.3.1), only the clock on pin CLKM is disabled.

The RX_AACK_ON_NOCLK state is entered from RX_AACK_ON by a rising edge at SLP_TR pin. The return to RX_AACK_ON state results either from a successful frame reception or a falling edge on pin SLP_TR.

The CLKM pin is disabled 35 clock cycles after the rising edge at SLP_TR pin. This allows the microcontroller to complete its power-down sequence.

In case of frame reception, the radio transceiver enters the BUSY_RX_AACK_ON state and parses the address field and the FCS of the incoming frame. If it passes address filtering and has a correct FCS the frame is accepted and the radio transceiver state changes to BUSY_RX_AACK, the TRX_END interrupt is issued and CLKM is turned on. If an ACK was requested the radio transceiver follows the procedure described in section 7.2.3.1.

After the transaction has been completed, the radio transceiver enters the RX_AACK_ON state. Note, the radio transceiver reenters the RX_AACK_ON_NOCLK state only, when the next rising edge at SLP_TR pin occurs.

7.2.4 Interrupt Handling in Extended Operating Mode

The interrupts in the Extended Operating Mode are handled slightly different compared to the Basic Operating Mode (see section 7.1.3). The number of possible interrupts is reduced to a necessary minimum of events. This minimizes the interaction between microcontroller and AT86RF230 to reduce the overall power consumption. The differences in the interrupt handling are described in Table 7-5.

Table 7-5. Interrupt Description for Extended Operating Mode

IRQ	Handling in Extended Operating Mode
IRQ_7: BAT_LOW	No special handling (see section 6.5)
IRQ_6: TRX_UR	No special handling (see section 6.5)
IRQ_3: TRX_END	TX_ARET: Indicates the completion of TX_ARET algorithm. RX_AACK: Indicates the successful frame reception. Frame data can be uploaded to the microcontroller.
IRQ_2: RX_START	Not used
IRQ_1: PLL_UNLOCK	Disabled for regular operation. In case of occurrence, the device status needs to be examined (refer to AVR2009 “AT86RF230 – Software Programming Model”).
IRQ_0: PLL_LOCK	Disabled for regular operation. In case of occurrence, the device status needs to be examined (refer to AVR2009 “AT86RF230 – Software Programming Model”).

7.2.5 Register Summary

Table 7-6. Register Summary

Reg.-Address	Register Name	Description
0x01	TRX_STATUS	Radio transceiver status, CCA result
0x02	TRX_STATE	State control
0x20 - 0x2B		Address filter configuration
0x2C	XAH_CTRL	Retries value control
0x2D	CSMA_SEED_0	CSMA-CA seed value
0x2E	CSMA_SEED_1	CSMA-CA seed value, MIN_BE, AACK_SET_PD, I_AM_COORD

7.2.6 Register Description – Control Registers

Register 0x01 (TRX_STATUS)

The TRX_STATUS register signals the current state of the radio transceiver as well as the status of the CCA measurement. Note, a read access to the register clears bits CCA_DONE and CCA_STATUS. This register is also used for Basic Operating Mode, refer to section 7.1.

Bit	7	6	5	4	
0x01	CCA_DONE	CCA_STATUS	Reserved	TRX_STATUS	TRX_STATUS
Read/Write	R	R	R	R	
Reset value	0	0	0	0	

Bit	3	2	1	0	
0x01	TRX_STATUS				TRX_STATUS
Read/Write	R	R	R	R	
Reset value	0	0	0	0	

- **Bit 7 – CCA_DONE**

Refer to section 8.6.

- **Bit 6 – CCA_STATUS**

Refer to section 8.6.

- **Bit 5 – Reserved**
- **Bit [4:0] – TRX_STATUS**

The register bits TRX_STATUS signal the current radio transceiver status. If the requested state transition is not completed yet, the TRX_STATUS returns STATE_TRANSITION_IN_PROGRESS. State transition timings are defined in Table 7-1.

Table 7-7. Radio Transceiver Status, Register Bits TRX_STATUS

Register Bits	Value[4:0]	State Description
TRX_STATUS	0x00	P_ON
	0x01	BUSY_RX
	0x02	BUSY_TX
	0x06	RX_ON
	0x08	TRX_OFF (Clock State)
	0x09	PLL_ON (TX_ON)
	0x0F	SLEEP
	0x11	BUSY_RX_AACK
	0x12	BUSY_TX_ARET
	0x16	RX_AACK_ON
	0x19	TX_ARET_ON
	0x1C	RX_ON_NOCLK
	0x1D	RX_AACK_ON_NOCLK
	0x1E	BUSY_RX_AACK_NOCLK
	0x1F	STATE_TRANSITION_IN_PROGRESS
		All other values are reserved

Register 0x02 (TRX_STATE)

The register TRX_STATE controls the radio transceiver states via register bits TRX_CMD. The status and the result of a TX_ARET/RX_AACK transaction is indicated by register bits TRAC_STATUS.

A successful state transition shall be confirmed by reading register bits TRX_STATUS in register 0x01 (TRX_STATUS).

Bit	7	6	5	4	
0x02	TRAC_STATUS			TRX_CMD	TRX_STATE
Read/Write	R	R	R	R/W	
Reset value	0	0	0	0	

Bit	3	2	1	0	
0x02	TRX_CMD				TRX_STATE
Read/Write	R/W	R/W	R/W	R/W	
Reset value	0	0	0	0	

- **Bit [7:5] – TRAC_STATUS**

The status of the TX_ARET algorithm is indicated by register bits TRAC_STATUS.

Details of the algorithm and a description of the status information are given in section 7.2.3.2.

Table 7-8. State Control Register, Register Bits TRAC_STATUS TX_ARET

Register Bits	Value[7:5]	Description
TRAC_STATUS	0	SUCCESS
	1	SUCCESS_DATA_PENDING
	3	CHANNEL_ACCESS_FAILURE
	5	NO_ACK
	7	INVALID
		All other values are reserved

- **Bit [4:0] – TRX_CMD**

A write access to register bits TRX_CMD initiates a radio transceiver state transition towards the new state.

Table 7-9. State Control Register, Register Bits TRX_CMD

Register Bits	Value[4:0]	State Description
TRX_CMD	0x00(1)	NOP
	0x02(2)	TX_START
	0x03	FORCE_TRX_OFF
	0x06	RX_ON
	0x08	TRX_OFF (Clock State)
	0x09	PLL_ON (TX_ON)
	0x16	RX_AACK_ON
	0x19	TX_ARET_ON
		All other values are reserved
Notes:	1. TRX_CMD = 0 after power-on reset (POR) 2. Frame transmission starts 16 µs (1 symbol) after TX_START	

Register 0x2C (XAH_CTRL)

The XAH_CTRL register controls the TX_ARET transaction in the Extended Operating Mode of the radio transceiver.

Bit	7	6	5	4	
0x2C	MAX_FRAME_RETRIES				XAH_CTRL
Read/Write	R/W	R/W	R/W	R/W	
Reset value	0	0	1	1	

Bit	3	2	1	0	
0x2C	MAX_CSMA_RETRIES			Reserved	XAH_CTRL
Read/Write	R/W	R/W	R/W	R/W	
Reset value	1	0	0	0	

- **Bit [7:4] – MAX_FRAME_RETRIES**

MAX_FRAME_RETRIES specifies the maximum number of frame retransmission in TX_ARET transaction.

- **Bit [3:1] – MAX_CSMA_RETRIES**

MAX_CSMA_RETRIES specifies the maximum number of retries in TX_ARET transaction to repeat the random back-off/CCA procedure before the transaction gets cancelled. Even though the valid range of MAX_CSMA_RETRIES is [0, 1 … 5] according to IEEE 802.15.4-2003, the AT86RF230 can be configured up to a maximum value of 7 retries.

- **Bit 0 – Reserved**

Register 0x2D (CSMA_SEED_0)

The CSMA_SEED_0 register contains a fraction of the CSMA_SEED value for the CSMA-CA algorithm.

Bit	7	6	5	4	3	2	1	0	
0x2D	CSMA_SEED_0								CSMA_SEED_0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset value	1	1	1	0	1	0	1	0	

- **Bit [7:0] – CSMA_SEED_0**

The register bits CSMA_SEED_0 contain the lower 8 bits of the CSMA_SEED. The upper 3 bits are stored in register bits CSMA_SEED_1 of register 0x2E (CSMA_SEED_1). CSMA_SEED is the seed of the random number generator for the CSMA-CA algorithm.

Register 0x2E (CSMA_SEED_1)

The CSMA_SEED_1 register contains a fraction of the CSMA_SEED value, the back-off exponent for the CSMA-CA algorithm and configuration bits for address filtering in RX_AACK operation.

Bit	7	6	5	4	
0x2C	MIN_BE		AACK_SET_PD	Reserved	CSMA_SEED_1
Read/Write	R/W	R/W	R/W	R	
Reset value	1	1	0	0	

Bit	3	2	1	0	
0x2C	I_AM_COORD	CSMA_SEED_1			CSMA_SEED_1
Read/Write	R/W	R/W	R/W	R/W	
Reset value	0	0	1	0	

- **Bit [7:6] – MIN_BE**

The register bit MIN_BE defines the minimal back-off exponent used in the CSMA-CA algorithm to generate a pseudo random number for back-off the CCA. For details refer to IEEE 802.15.4-2003 section 7.5.1.3. If set to zero, the start of the CCA algorithm is not delayed.

- **Bit 5 – AACK_SET_PD**

This register bit defines the content of the frame pending subfield for acknowledgement frames in RX_AACK mode. If this bit is enabled the frame pending subfield of the

acknowledgment frame is set in response to a MAC command data request frame, otherwise not. The register bit has to be set before finishing the SHR transmission of the acknowledgment frame. This is 352 µs (192 µs ACK wait time + 160 µs SHR transmission) after the TRX_END interrupt issued by the frame to be acknowledged.

- **Bit 4 – Reserved**
- **Bit 3 – I_AM_COORD**

This register bit has to be set if the node is a PAN coordinator. This register bit is used for address filtering in RX_AACK. If I_AM_COORD = 1 and if only source addressing fields are included in a data or MAC command frame, the frame shall be accepted only if the device is the PAN coordinator and the source PAN identifier matches macPANId, for details refer to IEEE 802.15.4-2003, section 7.5.6.2 (third-level filter rules).

- **Bit [2:0] – CSMA_SEED_1**

The register bits CSMA_SEED_1 contain the upper 3 bits of the CSMA_SEED. The lower part is defined in register 0x2D (CSMA_SEED_0).

7.2.7 Register Description – Address Registers

Register 0x20 (SHORT_ADDR_0)

This register contains bits [7:0] of the 16 bit short address for address filtering.

Bit	7	6	5	4	3	2	1	0	
0x20	SHORT_ADDRESS_0								SHORT_ADDR_0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset value	0	0	0	0	0	0	0	0	

Register 0x21 (SHORT_ADDR_1)

This register contains bits [15:8] of the 16 bit short address for address filtering.

Bit	7	6	5	4	3	2	1	0	
0x21	SHORT_ADDRESS_1								SHORT_ADDR_1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset value	0	0	0	0	0	0	0	0	

Register 0x22 (PAN_ID_0)

This register contains bits [7:0] of the 16 bit PAN ID for address filtering.

Bit	7	6	5	4	3	2	1	0	
0x22	PAN_ID_0								PAN_ID_0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset value	0	0	0	0	0	0	0	0	

Register 0x23 (PAN_ID_1)

This register contains bits [15:8] of the 16 bit PAN ID for address filtering.

Bit	7	6	5	4	3	2	1	0	
0x23	PAN_ID_1								PAN_ID_1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset value	0	0	0	0	0	0	0	0	

Register 0x24 (IEEE_ADDR_0)

This register contains bits [7:0] of the 64 bit IEEE address for address filtering.

Bit	7	6	5	4	3	2	1	0	
0x24	IEEE_ADDR_0								IEEE_ADDR_0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset value	0	0	0	0	0	0	0	0	

Register 0x25 (IEEE_ADDR_1)

This register contains bits [15:8] of the 64 bit IEEE address for address filtering.

Bit	7	6	5	4	3	2	1	0	
0x25	IEEE_ADDR_1								IEEE_ADDR_1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset value	0	0	0	0	0	0	0	0	

Register 0x26 (IEEE_ADDR_2)

This register contains bits [23:16] of the 64 bit IEEE address for address filtering.

Bit	7	6	5	4	3	2	1	0	
0x26	IEEE_ADDR_2								IEEE_ADDR_2
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset value	0	0	0	0	0	0	0	0	

Register 0x27 (IEEE_ADDR_3)

This register contains bits [31:24] of the 64 bit IEEE address for address filtering.

Bit	7	6	5	4	3	2	1	0	
0x27	IEEE_ADDR_3								IEEE_ADDR_3
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset value	0	0	0	0	0	0	0	0	

Register 0x28 (IEEE_ADDR_4)

This register contains bits [39:32] of the 64 bit IEEE address for address filtering.

Bit	7	6	5	4	3	2	1	0	
0x28	IEEE_ADDR_4								IEEE_ADDR_4
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset value	0	0	0	0	0	0	0	0	

Register 0x29 (IEEE_ADDR_5)

This register contains bits [47:40] of the 64 bit IEEE address for address filtering.

Bit	7	6	5	4	3	2	1	0	
0x29	IEEE_ADDR_5								IEEE_ADDR_5
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset value	0	0	0	0	0	0	0	0	

Register 0x2A (IEEE_ADDR_6)

This register contains bits [55:48] of the 64 bit IEEE address for address filtering.

Bit	7	6	5	4	3	2	1	0	
0x2A	IEEE_ADDR_6								IEEE_ADDR_6
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset value	0	0	0	0	0	0	0	0	

Register 0x2B (IEEE_ADDR_7)

This register contains bits [63:56] of the 64 bit IEEE address for address filtering.

Bit	7	6	5	4	3	2	1	0	
0x2B	IEEE_ADDR_7								IEEE_ADDR_7
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset value	0	0	0	0	0	0	0	0	

8 Functional Description

8.1 Introduction - Frame Format

Figure 8-1 provides an overview of the physical layer frame structure as defined by the IEEE 802.15.4-2003 standard. Figure 8-2 shows details of the defined MAC layer frame structure.

Figure 8-1 IEEE 802.15.4-2003 Frame Format – PHY Layer Frame Structure

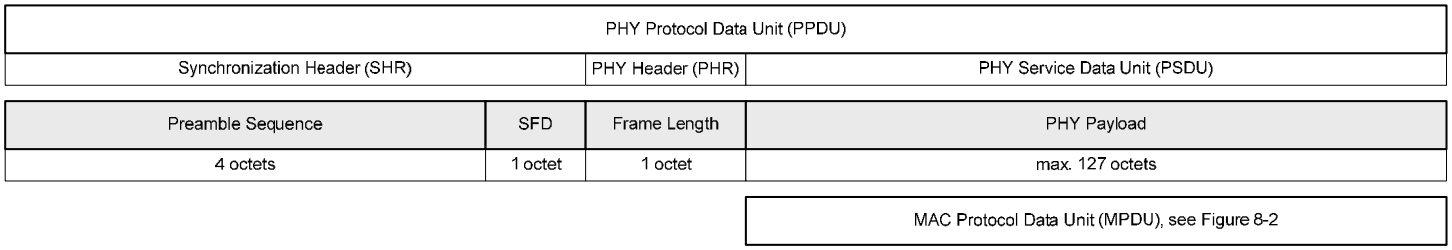
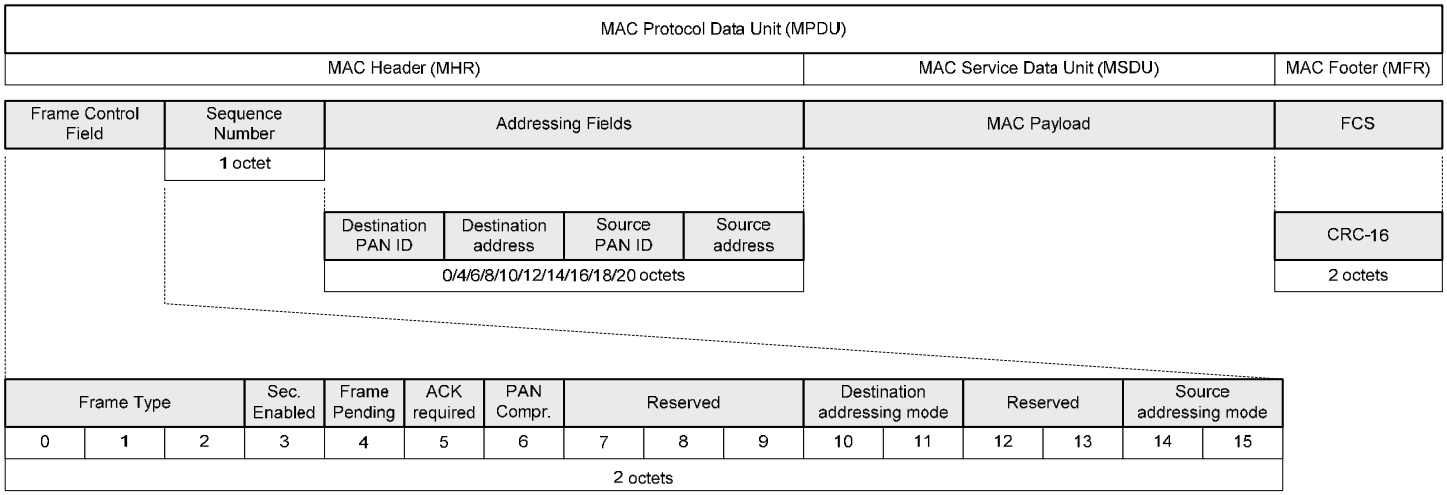


Figure 8-2 IEEE 802.15.4-2003 Frame Format – MAC Layer Frame Structure



8.1.1 PHY Protocol Layer Data Unit (PPDU)

8.1.1.1 Synchronization Header (SHR)

The SHR consists of a four-octet preamble field (all zero), followed by a single SFD octet which has the predefined value 0xA7. When transmitting, the SHR is automatically generated by the AT86RF230, and prefixed to the frame that has been read from the Frame Buffer. The transmission of the SHR requires 160 µs (10 symbols). This allows the microcontroller to initiate a transmission and to start downloading the frame contents subsequently. Note, that in this case the SPI transfer rate must be equal or faster than the PHY data rate.

During frame reception, the SHR is used for PHY synchronization purposes. In Basic Operating Mode an RX_START interrupt is issued 8 µs after detection of the SFD field.

8.1.1.2 PHY Header (PHR)

The PHY header consists of a single octet following the SHR. The least significant 7 bits of that octet denote the frame length of the following PSDU, while the most significant bit of that octet is reserved.

During transmission, the PHR field has to be supplied by the microcontroller during Frame Buffer write access.

On receive, the radio transceiver does not write the PHR field into the Frame Buffer. Instead it is prefixed to the PSDU during Frame Buffer read access. Note, that the reserved MSB of the PHR octet is always set to 0.

8.1.1.3 PHY Payload (PHY Service Data Unit, PSDU)

The PSDU has a variable length between one and 127 octets.

8.1.2 MAC Protocol Layer Data Unit (MPDU)

8.1.2.1 MAC Header (MHR) Fields

The MAC header consists of the Frame Control Field (FCF), a sequence number, and the variable length addressing fields.

8.1.2.2 Frame Control Field (FCF)

The FCF consists of 16 bits, and occupies the first two octets of the MPDU.

Bit [2:0] describe the frame type. Table 8-1 summarizes frame types defined by IEEE 802.15.4-2003, section 7.2.1.1.1.

Table 8-1. IEEE 802.15.4-2003 Frame Types

Frame Control field bit assignments		Description
Bit [2:0]	value	
000	0	Beacon
001	1	Data
010	2	Acknowledge
011	3	MAC command
100 – 111	4 – 7	Reserved

These bits are used for address filtering by applying the IEEE 802.15.4-2003 third level filter rules. Only frame types 0 – 3 pass the third level filter rules. Automatic address filtering by the AT86RF230 is enabled when using the RX_AACK operation (see section 7.2.3.1).

Bit 3: indicates whether security processing applies to this frame. This field is not evaluated by the AT86RF230.

Bit 4 is the “frame pending” subfield. This field can be set in an acknowledgement frame. It indicates that the transmitter of the acknowledgement frame has more data to send for the recipient of the acknowledgement frame. For acknowledgment frames automatically generated by the AT86RF230, this bit is set according to the content of register bit AACK_SET_PD in register 0x2E (CSMA_SEED_1).

Bit 5 forms the “acknowledgment request” subfield. If this bit is set within a data or MAC command frame that is not broadcast, the recipient shall acknowledge the reception of the frame within the time specified by IEEE 802.15.4-2003 (i.e. within 192 µs for

nonbeacon-enabled networks). The AT86RF230 parses this bit during RX_AACK operation and transmits an acknowledgment frame if necessary.

Bit 6 the “Intra-PAN” subfield indicates that in a frame, where both, the destination and source addresses are present, the PAN ID is omitted from the source address field. This bit is evaluated by the AT86RF230 address filter logic when using RX_AACK operation.

Bit [11:10] the “Destination address mode” subfield describes the format of the destination address of the frame. The values of the address modes are summarized in Table 8-2, according to IEEE 802.15.4-2003:

Table 8-2. IEEE 802.15.4-2003 Address Modes

Addressing Mode Value		Description
Bit [11:10] Bit [15:14]	**value**	
00	0	Address not present
01	1	Reserved, must not be used
10	2	Address is 16-bit short
11	3	Address is 64-bit extended address

If the destination address mode is either 2 or 3 (i.e. if the destination address is present at all), it always consists of a 16-bit PAN ID first, followed by either the 16-bit or 64-bit address as described by the mode.

Bit [15:14] form the “Source address mode” subfield, with a similar meaning as “Destination address mode”.

The address field description bits of the FCF (Bits 6, 10, 11, 14, 15) affect the address filter logic of the AT86RF230 while operating in RX_AACK states (see section 7.2.3.1).

8.1.2.3 Sequence number

The one-octet sequence number following the FCF identifies a particular frame, so that duplicated frame transmissions can be detected. While operating in RX_AACK states, the content of this field is copied from the frame to be acknowledged into the acknowledgment frame.

8.1.2.4 Addressing fields

The addressing fields terminate the MHR. The destination address (if present) is always transmitted first, followed by the source address (if present). Each address consists of the PAN ID and a device address. If both addresses are present, and the “Intra PAN” subfield in the FCF is set to 1, the source PAN ID is omitted.

Note that in addition to these general rules, IEEE 802.15.4-2003 further restricts the valid address combinations for the individual possible MAC frame types. For example, the situation where both addresses are omitted (source addressing mode = 0 and destination addressing mode = 0) is only allowed for acknowledgment frames. The address filter in the AT86RF230 has been designed to apply to IEEE 802.15.4-2003 compliant frames only.

8.1.2.5 MAC Service Data Unit (MSDU)

This is the actual MAC payload. It is usually structured according to the individual frame type descriptions in IEEE 802.15.4-2003.

8.1.2.6 MAC Footer (MFR) Fields

The MAC footer consists of a two-octet frame checksum (FCS). The AT86RF230 can generate and evaluate this FCS automatically, for details refer to section 8.2.

8.2 Frame Check Sequence (FCS)

The frame check sequence main features are:

- Indicates bit errors, based on a cyclic redundancy check (CRC) of length 16 bit
- Uses International Telecommunication Union (ITU) CRC polynomial
- Automatically evaluated during reception
- Can be automatically generated during transmission

8.2.1.1 Overview

The FCS is intended for use at the MAC level to detect corrupted frames. It is computed by applying an ITU CRC polynomial to all transferred bytes following the length field (MHR and MSDU fields). The frame check sequence has a length of 16 bit and is located in the last two bytes of a frame (MAC footer, see Figure 8-2).

The AT86RF230 applies an FCS check on each received frame. The FCS check result is stored to register bit RX_CRC_VALID in register 0x06 (PHY_RSSI). On transmit the radio transceiver can be configured to autonomously compute and append the FCS bytes.

8.2.2 CRC calculation

The CRC polynomial used in IEEE 802.15.4-2003 networks is defined by

$$G_{16}(x) = x^{16} + x^{12} + x^5 + 1 .$$

The FCS shall be calculated for transmission using the following algorithm:

Let

$$M(x) = b_0 x^{k-1} + b_1 x^{k-2} + \ldots + b_{k-2} x + b_{k-1}$$

be the polynomial representing the sequence of bits for which the checksum is to be computed. Multiply *M(x)* by x^{16}, giving the polynomial

$$N(x) = M(x) \cdot x^{16} .$$

Divide *N(x)* modulo 2 by the generator polynomial, $G_{16}(x)$, to obtain the remainder polynomial,

$$R(x) = r_0 x^{15} + r_1 x^{14} + \ldots + r_{14} x + r_{15}$$

The FCS field is given by the coefficients of the remainder polynomial, *R(x)*.

Example:

Considering a 5 octet ACK frame. The MHR field consists of

0100 0000 0000 0000 0101 0110.

The leftmost bit (b_0) is transmitted first in time. The FCS would be following

0010 0111 1001 1110.

The leftmost bit (r_0) is transmitted first in time.

8.2.3 Automatic FCS generation

The AT86RF230 automatic FCS generation and insertion is enabled by setting register bit TX_AUTO_CRC_ON to 1.

For a frame with a frame length field (PHR) specified as N ($3 \le N \le 127$), the FCS is calculated on the first N-2 PSDU octets in the Frame Buffer, and the resulting 16 bit FCS field is appended during transmission. Note, if the AT86RF230 automatic FCS generation is enabled, the frame download to the Frame Buffer can be stopped right after MAC payload. There is no need to download FCS dummy bytes.

In RX_AACK states, when a received frame needs to be acknowledged, the FCS of the ACK frame is always automatically generated by the AT86RF230.

Example:

A frame transmission of length five with the register bit TX_AUTO_CRC_ON set, is started with a frame download of five bytes (the last two bytes can be omitted). The first three bytes are used for FCS generation, the last two bytes are replaced by the internally calculated FCS.

8.2.4 Automatic FCS check

An FCS check is applied on each incoming frame with a frame length $N \ge 2$. The result of the FCS check is stored to register bit RX_CRC_VALID in register 0x06 (PHY_RSSI). The register bit is updated at the event of the TRX_END interrupt and remains valid until the next TRX_END interrupt caused by a new frame reception.

In RX_AACK states, if FCS of the received frame is not valid, the radio transceiver rejects the frame and the TRX_END interrupt will not be generated.

In TX_ARET states, the FCS of an ACK is automatically checked. If it is not correct, the ACK is not accepted.

8.2.5 Register Description

Register 0x05 (PHY_TX_PWR)

The PHY_TX_PWR register sets the transmit power and controls the FCS algorithm for TX operation.

Bit	7	6	5	4	
0x05	TX_AUTO_CRC_ON	Reserved			PHY_TX_PWR
Read/Write	R/W	R	R	R	
Reset value	0	0	0	0	

Bit	3	2	1	0	
0x05	TX_PWR				PHY_TX_PWR
Read/Write	R/W	R/W	R/W	R/W	
Reset value	0	0	0	0	

- **Bit 7 – TX_AUTO_CRC_ON**

Register bit TX_AUTO_CRC_ON controls the automatic FCS generation for TX operation. The automatic FCS algorithm is performed autonomously by the radio transceiver if register bit TX_AUTO_CRC_ON = 1.

- **Bit [6:4] – Reserved**
- **Bit [3:0] – TX_PWR**

Refer to section 9.2.3.

Register 0x06 (PHY_RSSI)

The PHY_RSSI register is a multi purpose register to indicate the current received signal strength (RSSI) and the FCS validity of a received frame.

Bit	7	6	5	4	
0x06	RX_CRC_VALID	Reserved		RSSI	PHY_RSSI
Read/Write	R	R	R	R	
Reset value	0	0	0	0	

Bit	3	2	1	0	
0x06	RSSI				PHY_RSSI
Read/Write	R	R	R	R	
Reset value	0	0	0	0	

- **Bit 7 – RX_CRC_VALID**

This register bit indicates whether a received frame has a valid FCS. The register bit is updated when issuing the TRX_END interrupt remains valid until the next TRX_END interrupt caused by a new frame reception.

Table 8-3. RX FCS Result

Register Bit	Value	Description
RX_CRC_VALID	0	FCS is not valid.
	1	FCS is valid.

- **Bit [6:5] – Reserved**
- **Bit [4:0] – RSSI**

Refer to section 8.4.4.

8.3 Energy Detection (ED)

The main features for the Energy Detection module are:

- 85 unique energy levels defined
- 1 dB resolution

8.3.1 Overview

The receiver Energy Detection measurement is used by a network layer as part of a channel selection algorithm. It is an estimation of the received signal power within the bandwidth of an IEEE 802.15.4-2003 channel. No attempt is made to identify or decode signals on the channel. The ED value is calculated by averaging RSSI values over eight symbols (128 µs).

8.3.2 Request an ED Measurement

There are two ways implemented in the AT86RF230 to initiate an ED measurement:

- Manually, by a write access to register 0x07 (PHY_ED_LEVEL), or
- Automatically, by detecting a valid SFD of an incoming frame.

For manually initiated ED measurement the radio transceiver needs to be in one of the states RX_ON or BUSY_RX. An automated ED measurement is started, if a SFD field is detected. A valid SFD detection is signalized by an RX_START interrupt in Basic Operating Mode.

The measurement result is stored to register 0x07 (PHY_ED_LEVEL) 140 µs after its initialization. The value is always 0 if the AT86RF230 is not in any of the RX states.

Thus by using Basic Operating Mode, a valid ED value from the currently received frame is accessible 140 µs after the RX_START interrupt and remains valid until a new RX_START interrupt is generated by the next incoming frame or until another ED measurement is initiated manually.

By using the Extended Operating Mode, the RX_START interrupt is always masked and cannot be used as timing reference. Here successful frame reception is only signalized by the TRX_END interrupt. The minimum time between a TRX_END interrupt and a following SFD detection is 96 µs. Including the ED measurement time, the ED value needs to be read within 224 µs after the TRX_END interrupt; otherwise, it could be overwritten by the result of the next measurement cycle.

Note, it is not recommended to initiate manually an ED measurement when using the Extended Operating Mode.

8.3.3 Data Interpretation

The PHY_ED_LEVEL is an 8 bit register. The ED value of the AT86RF230 radio transceiver has a valid range from 0 to 84 with a resolution of 1 dB. All other values do not occur. If zero is read from the PHY_ED_LEVEL register, this indicates that the measured energy is less than -91 dBm (see parameter 11.7.16). Due to environmental conditions (temperature, voltage, semiconductor parameters, etc.) the computed energy value has an accuracy of ±5 dBm, this is to be considered as constant offset over the measurement range.

8.3.4 Register Description

Register 0x07 (PHY_ED_LEVEL)

The ED_LEVEL register contains the result after an ED measurement.

Bit	7	6	5	4	3	2	1	0	
0x07	ED_LEVEL[7:0]								ED_LEVEL
Read/Write	R	R	R	R	R	R	R	R	
Reset value	0	0	0	0	0	0	0	0	

- **Bit [7:0] – ED_LEVEL**

The minimum ED value (ED_LEVEL = 0) indicates receiver power less than RSSI_BASE_VAL. The range is 84 dB with a resolution of 1 dB and an absolute accuracy of ±5 dB. The measurement period is 8 symbol periods.

A manual ED measurement can be initiated by a write access to the register.

8.4 Received Signal Strength Indicator (RSSI)

The Received Signal Strength Indicator main features are:

- Minimum RSSI sensitivity is -91 dBm (RSSI_BASE_VAL, see parameter 11.7.16)
- Dynamic range is 81 dB
- Minimum RSSI value is 0
- Maximum RSSI value is 28

8.4.1 Overview

The RSSI is a 5-bit value indicating the receive power in the selected channel, in steps of 3 dB. No attempt is made to distinguish between IEEE 802.15.4 signal and other signal source, only the received signal power is evaluated. The RSSI provides the basis for ED measurement.

8.4.2 Reading RSSI

Using the Basic Operating Mode, the RSSI value is valid at any RX state, and is updated every 2 µs. The current RSSI value is stored to the PHY_RSSI register.

Note, it is not recommended to read the RSSI value when using the Extended Operating Mode. The automatically generated ED value should be used alternatively (see section 8.3).

8.4.3 Data Interpretation

The PHY_RSSI is an 8-bit register, however, the value is represented in the lowest five bits [4:0] and the range is 0 – 28.

An RSSI value of 0 indicates an RF input power of < -91 dBm. For an RSSI value in the range of 1 to 28, the RF input power can be calculated as follows:

$$P_{RF} = RSSI_BASE_VAL + 3 \bullet (RSSI - 1)$$

8.4.4 Register Description

Register 0x06 (PHY_RSSI)

The PHY_RSSI register is a multi purpose register to indicate the current received signal strength (RSSI) and the FCS validity of a received frame.

Bit	7	6	5	4	
0x06	RX_CRC_VALID	Reserved		RSSI	PHY_RSSI
Read/Write	R	R	R	R	
Reset value	0	0	0	0	

Bit	3	2	1	0	
0x06	RSSI				PHY_RSSI
Read/Write	R	R	R	R	
Reset value	0	0	0	0	

- **Bit 7 – RX_CRC_VALID**

Refer to section 8.2.5.

- **Bit [6:5] – Reserved**
- **Bit [4:0] – RSSI**

The register bits RSSI contain the result of the automated RSSI measurement. The value is updated every 2 µs in receive states.

The read value is a number between 0 and 28 indicating the received signal strength as a linear curve on a logarithmic input power scale (dBm) with a resolution of 3 dB. An RSSI value of 0 indicates an RF input power of < -91 dBm (see parameter 11.7.17), a value of 28 a power of ≥ -10 dBm (see parameter 11.7.18).

8.5 Link Quality Indication (LQI)

The IEEE 802.15.4 standard defines the LQI measurement as a characterization of the strength and/or quality of a received packet. The use of the LQI result by the network or application layer is not specified in this standard. LQI values shall be an integer ranging from 0 to 255. The minimum and maximum LQI values (0 and 255) should be associated with the lowest and highest quality compliant signals, respectively, and LQI values in between should be uniformly distributed between these two limits.

8.5.1 Overview

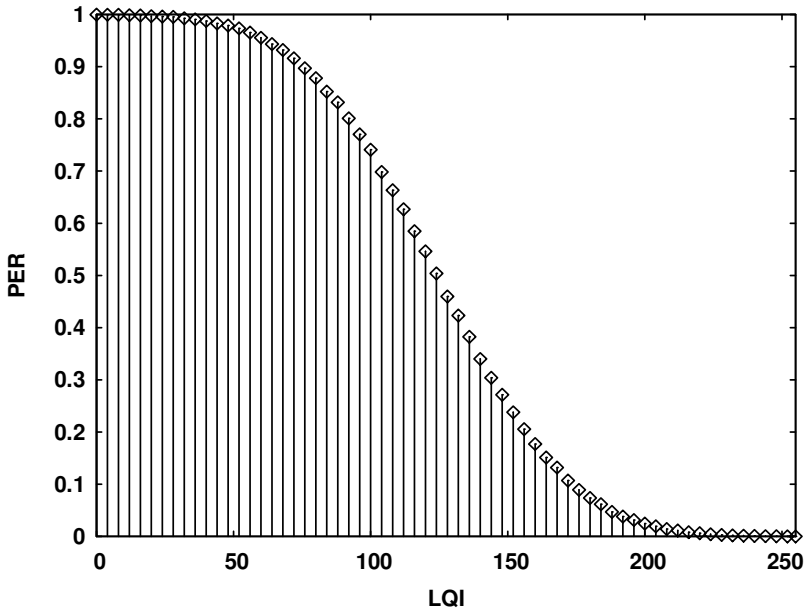
The AT86RF230 determines the link quality of a radio link. The radio transceiver uses correlation results of multiple symbols within a frame to determine the LQI value. This is done for each received frame. The minimum frame length for a valid LQI value is two octets PSDU. LQI values are integers ranging from 0 to 255.

The LQI values can be associated with an expected packet error rate (PER). The PER is the ratio of erroneous received frames to the total number of received frames. A PER of zero indicates no frame error, whereas at a PER of one no frame was received correctly.

As an example, Figure 8-3 shows the conditional packet error rate with associated LQI values. The values are taken from received frames of length 20 octets PSDU on transmission channels with low multipath delay spreads. Even if the transmission channel characteristic has higher multipath delay spread than assumed for this example, the dependency of PER to LQI values is not affected.

Since the packet error rate is a statistical value, the PER shown in Figure 8-3 is based on a huge number of receptions.

Figure 8-3. Conditional Packet Error Rate versus LQI



8.5.2 Request an LQI Measurement

The LQI byte can be obtained after a frame has been received by the radio transceiver. One additional byte is attached to the received frame containing the LQI value. This

information can be read as an extra byte from the Frame Buffer (see section 9.1). The LQI byte can be uploaded after the TRX_END interrupt.

8.5.3 Data Interpretation

A low LQI value is associated with low signal strength and/or high signal distortions. Signal distortions are mainly caused by interference signals and/or multipath propagation. High LQI values indicate a sufficient high signal power and low signal distortions.

Note, the received signal power as indicated by received signal strength indication (RSSI) value or energy detection (ED) value do not characterize the signal quality and the ability to decode a signal. As an example, a received signal with an input power of about 6 dB above the receiver sensitivity likely results in a LQI value close to 255 for radio channels with very low signal distortions. For higher signal power levels the LQI value becomes independent of the actual signal strength. This is because the packet error rate for these scenarios tends towards zero and further increase of the signal strength, i.e. by increasing the transmission power, does not decrease the error rate any further. In this case RSSI or ED can be used to evaluate the signal strength and the link margin.

ZigBee networks require to determine the “best” route between two nodes. Both, the LQI and the RSSI/ED can be used for this, depending on the optimization criteria. As a rule of thumb RSSI/ED is useful to differentiate between links with high LQI values. Transmission links with low LQI values should be discarded for routing decisions even if the RSSI/ED values are high.

8.6 Clear Channel Assessment (CCA)

The main features of the Clear Channel Assessment (CCA) module are:

- All 3 modes available as defined by IEEE 802.15.4-2003 in section 6.7.9
- Adjustable threshold of the energy detection algorithm

8.6.1 Overview

The CCA is used to detect a clear channel. There are three modes available as defined in Table 8-4.

Table 8-4. Available CCA Modes

CCA Mode	Description
1	Energy above threshold. CCA shall report a busy medium upon detecting any energy above the ED threshold.
2	Carrier sense only. CCA shall report a busy medium only upon the detection of a signal with the modulation and spreading characteristics of IEEE 802.15.4. This signal may be above or below the ED threshold.
3	Carrier sense with energy above threshold. CCA shall report a busy medium only upon the detection of a signal with the modulation and spreading characteristics of IEEE 802.15.4 with energy above the ED threshold.

8.6.2 CCA Configuration and Request

The CCA modes are configurable via register 0x08 (PHY_CC_CCA).

The 4 bit value CCA_ED_THRES of register 0x09 (CCA_THRES) defines the received power threshold of the “energy above threshold” algorithm. The threshold is calculated by RSSI_BASE_VAL+2•CCA_ED_THRES [dBm].

Using the Basic Operating Mode, a CCA request can be initiated manually by setting CCA_REQUEST = 1 in register 0x08 (PHY_CC_CCA), if the AT86RF230 is in any RX state. The CCA computation is done over eight symbol periodes and the result is accessible 140 µs after the request.

Note, it is not recommended to initiate manually a CCA measurement when using the Extended Operating Mode.

8.6.3 Data Interpretation

The current channel status (CCA_STATUS) and the CCA completion status (CCA_DONE) are accessible in register 0x01 (TRX_STATUS). Note, a read access to this register clears register bits CCA_DONE and CCA_STATUS.

The completion of a measurement cycle is indicated by CCA_DONE = 1. If the radio transceiver detected no signal (idle channel) during the measurement cycle, the CCA_STATUS bit is set to 1.

When using the “energy above threshold” algorithm (mode 1 and mode 3) any received power above CCA_ED_THRES level is interpreted as a busy channel. The “carrier sense” algorithm (mode 2 and mode 3) reports a busy channel when detecting a IEEE 802.15.4 signal above the RSSI_BASE_VAL (see parameter 11.7.16). The radio transceiver is also able to detect signals below this value, but the detection probability decreases with the signal power. It is almost zero at the radio transceivers sensitivity level (see parameter 11.7.1).

8.6.4 Register Description

Register 0x01 (TRX_STATUS)

The TRX_STATUS register signals the current state of the radio transceiver as well as the status of the CCA measurement. Note, a read access to the register clears bits CCA_DONE and CCA_STATUS.

Bit	7	6	5	4	
0x01	CCA_DONE	CCA_STATUS	Reserved	TRX_STATUS	TRX_STATUS
Read/Write	R	R	R	R	
Reset value	0	0	0	0	

Bit	3	2	1	0	
0x01	TRX_STATUS				TRX_STATUS
Read/Write	R	R	R	R	
Reset value	0	0	0	0	

- **Bit 7 – CCA_DONE**

This register indicates if a CCA request is completed. Each read access to register 0x01 resets the CCA_DONE bit.

Table 8-5. Status CCA Algorithm

Register Bit	Value	Description
CCA_DONE	0	CCA calculation in progress
	1	CCA calculation finished

- **Bit 6 – CCA_STATUS**

CCA_STATUS register bit indicates the result of a CCA request. Each read access to register 0x01 resets the CCA_STATUS bit.

Table 8-6. Status CCA Result

Register Bit	Value	Description
CCA_STATUS	0	Channel is busy
	1	Channel is idle

- **Bit 5 – Reserved**
- **Bit [4:0] – TRX_STATUS**

Refer to section 7.1.5.

Register 0x08 (PHY_CC_CCA)

The PHY_CC_CCA register contains register bits to initiate and control the CCA measurement as well as to set the channel center frequency.

Bit	7	6	5	4	
0x08	CCA_REQUEST	CCA_MODE		CHANNEL	PHY_CC_CCA
Read/Write	R/W	R/W	R/W	R/W	
Reset value	0	0	1	0	

Bit	3	2	1	0	
0x08	CHANNEL				PHY_CC_CCA
Read/Write	R/W	R/W	R/W	R/W	
Reset value	1	0	1	1	

- **Bit 7 – CCA_REQUEST**

A manual CCA measurement is initiated with setting CCA_REQUEST = 1.

- **Bit [6:5] – CCA_MODE**

The CCA mode can be selected using register bits CCA_MODE.

Table 8-7. CCA Modes

Register Bit	Value	Description
CCA_MODE	0	Reserved
	1	Mode 1, Energy above threshold
	2	Mode 2, Carrier sense only
	3	Mode 3, Carrier sense with energy above threshold

- **Bit [4:0] – CHANNEL**

Refer to section 9.7.5.

Register 0x09 (CCA_THRES)

This register contains the threshold level for CCA-ED measurement.

Bit	7	6	5	4	
0x09	Reserved				CCA_THRES
Read/Write	R/W	R/W	R/W	R/W	
Reset value	1	1	0	0	

Bit	3	2	1	0	
0x09	CCA_ED_THRES				CCA_THRES
Read/Write	R/W	R/W	R/W	R/W	
Reset value	0	1	1	1	

- **Bit [7:4] – Reserved**
- **Bit [3:0] – CCA_ED_THRES**

The register bits CCA_ED_THRES define the threshold value of the CCA-ED measurement. A cannel is indicated as busy when the received signal power is above RSSI_BASE_VAL + 2 • CCA_ED_THRES [dBm].

9 Module Description

9.1 Receiver (RX)

9.1.1 Overview

The AT86RF230 receiver is spitted into an analog radio front end and a digital base band processor (RX BBP), see Figure 3-1.

The RF signal is amplified by a low noise amplifier (LNA) and converted down to an intermediate frequency by a mixer. Channel selectivity is performed using an integrated band pass filter. A limiting amplifier (Limiter) provides sufficient gain to overcome the DC offset of the succeeding analog-to-digital converter (ADC) and generates a digital RSSI signal with 3 dB granularity. The IF signal is sampled and processed further by the digital base band receiver.

The RX BBP performs additional signal filtering and signal synchronization. The frequency offset of each frame is calculated by the synchronization unit and is used during the remaining receive process to correct the offset. The receiver is designed to handle frequency and symbol rate deviations up to ±120 ppm, caused by combined receiver and transmitter deviations. For details refer to section 11.5 parameter 11.5.6. Finally the signal is demodulated and the data are stored to the Frame Buffer.

In Basic Operating Mode the start of an IEEE 802.15.4 compliant frame is indicated by a RX_START interrupt. Accordingly it's end is signalized by an TRX_END interrupt. Based on the quality of the received signal a link quality indicator (LQI) is calculated and appended to the frame, refer to section 8.5. Additional signal processing is applied to the frame data to provide further status information like ED value (register 0x07) and FCS correctness (register 0x06).

Beyond these features the Extended Operating Mode of the AT86RF230 supports address filtering and pending data indication. For details refer to section 7.2.

9.1.2 Configuration

The receiver is enabled by writing the command RX_ON for the Basic Operating Mode or RX_AACK_ON for the Extended Operating Mode to register bits TRX_CMD in register 0x02 (TRX_STATE).

The receiver does not need any additional configuration to receive IEEE 802.15.4 compliant frames on the current selected channel when using the Basic Operating Mode. However the frame reception in the Extended Operating Mode requires further register configurations, for details refer to section 7.2.

9.2 Transmitter (TX)

9.2.1 Overview

The AT86RF230 transmitter consists of a digital base band processor (TX BBP) and an analog radio front end, see Figure 3-1.

The TX BBP reads the frame data from the Frame Buffer and performs the bit-to-symbol and symbol-to-chip mapping as specified by IEEE 802.15.4 in section 6.5.2. The O-QPSK modulation signal is generated and fed into the analog radio front end.

The fractional-N frequency synthesizer (PLL) converts the baseband transmit signal to the RF signal, which is amplified by the power amplifier (PA). The PA output is internally

connected to bidirectional differential antenna pins (RFP, RFN), so that no external antenna switch is needed.

9.2.2 Configuration

In Basic Operating Mode a transmission is started from PLL_ON state by either writing TX_START to register bits TRX_CMD (register 0x02, TRX_STATE) or by raising edge of SLP_TR.

In Extended Operating Modes a transmission is started automatically dependent on the transaction phase of either RX_AACK or TX_ARET, refer to section 7.2.

The RF output power can be set via register bits TX_PWR in register 0x05 (PHY_TX_PWR). The maximum output power of the transmitter is typical +3 dBm. The selectable output power range of the transmitter is 20 dB.

9.2.3 Register Description

Register 0x05 (PHY_TX_PWR)

The PHY_TX_PWR register sets the transmit power and controls the FCS algorithm for TX operation.

Bit	7	6	5	4	
0x05	TX_AUTO_CRC_ON	Reserved			PHY_TX_PWR
Read/Write	R/W	R	R	R	
Reset value	0	0	0	0	

Bit	3	2	1	0	
0x05	TX_PWR				PHY_TX_PWR
Read/Write	R/W	R/W	R/W	R/W	
Reset value	0	0	0	0	

- **Bit 7 – TX_AUTO_CRC_ON**

Refer to sections 7.2.6 and 8.2.

- **Bit [6:4] – Reserved**
- **Bit [3:0] – TX_PWR**

The register bits TX_PWR sets the TX output power of the AT86RF230. The available power settings are summarized in Table 9-1.

Table 9-1. PA Output Power Setting

Register Bits	Value [3:0]	Output Power [dBm]
TX_PWR	0x0	+3.0
	0x1	+2.6
	0x2	+2.1
	0x3	+1.6
	0x4	+1.1
	0x5	+0.5
	0x6	-0.2
	0x7	-1.2
	0x8	-2.2
	0x9	-3.2
	0xA	-4.2

Register Bits	Value [3:0]	Output Power [dBm]
	0xB	-5.2
	0xC	-7.2
	0xD	-9.2
	0xE	-12.2
	0xF	-17.2

9.3 Frame Buffer

The AT86RF230 contains a 128 byte dual port SRAM. One port is connected to the SPI interface, the other to the internal TX/RX BBP port. For data communication both ports are independent and simultaneously accessible. Access conflicts are indicated by a TRX under run (TRX_UR) interrupt.

The Frame Buffer is used for the TX and RX operation of the device and can keep one IEEE 802.15.4-2003 TX or one RX frame of maximum length at a time.

Note, a Frame Buffer access is only possible if the digital voltage regulator is turned on. This is the case in all device states except in SLEEP and P_ON.

9.3.1 Frame Buffer Data Management

Data stored in Frame Buffer (received data or data to be transmitted) remains valid as long as

- No new frame is written into the buffer via SPI
- No new frame is received (in any BUSY_RX state)
- No state change into SLEEP state is made

If the radio transceiver is in any RX state an incoming frame with valid SFD field overwrites the Frame Buffer content 32 µs after the RX_START interrupt occurs, even if the RX_START interrupt is disabled. Thus the Frame Buffer content should be uploaded to the microcontroller before the next SFD is received. To avoid an unintended Frame Buffer overwrite a state change to PLL_ON immediately after the frame reception (TRX_END interrupt) is recommended.

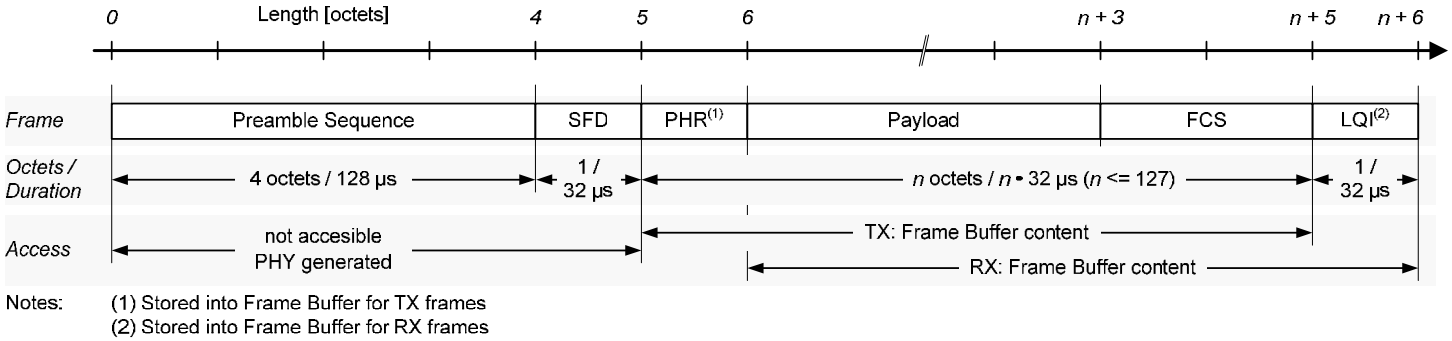
Using the Extended Operating Mode states TX_ARET_ON or TX_ARET_ON_NOCLK, the radio transceiver switches to RX (after successful frame transmission), if an acknowledgement was requested in FCF. Received frames are evaluated but not stored in the Frame Buffer in these states. This allows the radio transceiver to wait for an acknowledgement frame and retry the data frame transmission without downloading them again.

A radio transceiver state change, except a transition to SLEEP, does not affect the Frame Buffer contents. If the radio transceiver is forced into SLEEP, the Frame Buffer is powered off and the stored data gets lost.

9.3.2 User accessible Frame Content

The AT86RF230 supports an IEEE 802.15.4-2003 compliant frame format as shown in Figure 9-1.

Figure 9-1. Frame Structure



A frame comprises two sections, the fixed internally generated SHR field and the user accessible part stored in the Frame Buffer. The first fixed part of the frame consists of the preamble and the SFD field. The variable frame section contains the frame length field and the frame payload followed by the FCS field. The Frame Buffer content differs depending on the direction of the communication (RX or TX). To access the data follow the procedures described in sections 6.2.2 and 6.2.3.

In any of the receive states, the payload and the link quality indicator (LQI) value of a successfully received frame are stored to the Frame Buffer. The radio transceiver appends the LQI value to the PSDU data. The frame length information is not stored to the Frame Buffer. When using the Frame Buffer access mode to read the Frame Buffer content, the PHR octet is automatically prefixed to the payload during the upload process. If the SRAM access mode is used, the frame length information cannot be accessed. The preamble or the SFD value cannot be read.

For frame transmission, the PHR octet and the PSDU data shall be stored to the Frame Buffer. If the TX_AUTO_CRC_ON bit is set in register 0x05 (PHY_TX_PWR), the FCS field is replaced by the automatically calculated FCS during frame transmission. There is no need to download the FCS field when using the automatic FCS generation.

For non IEEE 802.15.4-2003 frames, the minimum PSDU length supported by the AT86RF230 is one byte.

9.3.3 Frame Buffer Interrupt Handling

Access conflicts may occur when reading or writing data simultaneously at the two independent ports of the Frame Buffer, BBP and SPI. Both of these ports have its own address counter that points to the Frame Buffer's current address.

During Frame Buffer read access, if the SPI port's address counter value is more than or equal to that of TX/RX BBP port then an access violation occurs. This indicates that the SPI transfer rate is higher than the PHY data rate.

Similar on Frame Buffer write access, an access violation occurs if the SPI port's address counter value is less than or equal to that of TX/RX BBP port. This access violation can occur if the SPI transfer rate during a frame download is slower than the PHY data rate, while having started the frame transmission already.

Both these access violations may cause data corruption and are indicated by TRX_UR interrupt when using the Frame Buffer access mode. Access violations are not indicated when using the SRAM access mode.

While receiving a frame, primarily the data needs to be stored to the Frame Buffer before reading it. This can be ensured by starting the Frame Buffer read access 32 µs after the RX_START interrupt at the earliest. When reading the frame data continuously

the SPI transfer rate shall be lower than 250 Kbit/s to ensure no TRX_UR interrupt occurs.

Note, during the Frame Buffer read access the TRX_UR interrupt is first valid 64 µs after the RX_START interrupt. The occurrence of the interrupt can be disregarded when reading the first byte of the Frame Buffer between 32 µs and 64 µs after the RX_START interrupt.

If a received frame upload is delayed and during the upload process a new frame is received, a TRX_UR and an RX_START interrupt occurs. Even so, the old frame data can be read, if the SPI data rate is higher than the effective over air data rate. A minimum SPI clock rate of 1 MHz is recommended in this special case. Finally it is required to check the uploaded frame data integrity by a FCS using the microcontroller.

When writing data to the Frame Buffer during frame transmission, the SPI transfer rate shall be higher than 250 Kbit/s to ensure no TRX_UR interrupt occurs. The first byte of the PSDU data must be available in the Frame Buffer before SFD transmission has been completed, which takes 176 µs (16 µs PA ramp up + 128 µs preamble transmission + 32 µs SFD transmission) from the rising edge of SLP_TR pin (see Figure 7-2).

9.4 Voltage Regulators (AVREG, DVREG)

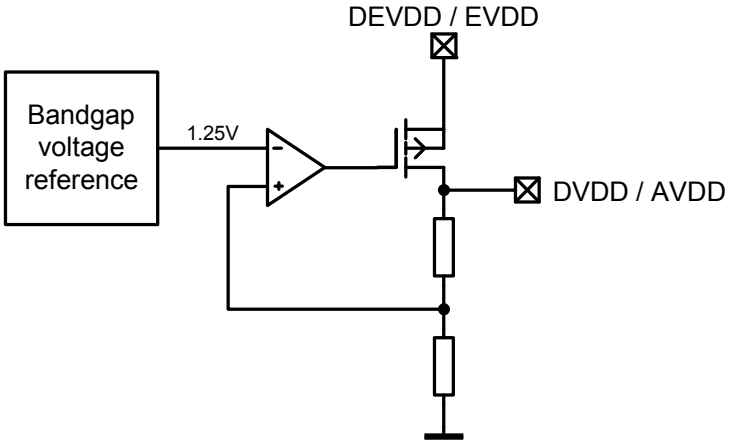
The main features of the Voltage Regulator modules are:

- Bandgap stabilized 1.8V supply for analog and digital domain.
- Low dropout (LDO) voltage regulator
- Configurable for usage of external voltage regulator

9.4.1 Overview

The internal voltage regulators supply the low voltage domains of the AT86RF230. The AVREG provides the regulated 1.8V supply voltage for the analog section and the DVREG supplies the 1.8V supply voltage for the digital section. A simplified schematic of the internal voltage regulator is shown in Figure 9-2.

Figure 9-2. Simplified Schematic of AVREG/DVREG



9.4.2 Configure the Voltage Regulators

The voltage regulators can be configured by the register 0x10 (VREG_CTRL).

It is recommended to use the internal regulators, but it is also possible to supply the low voltage domains by an external voltage source. For this configuration, the internal regulators need to be switched off by setting the register bits to the values AVREG_EXT = 1 and DVREG_EXT = 1. A regulated external supply voltage of 1.8V needs to be connected to the pins DVDD and AVDD. When turning on the external supply, ensure a sufficiently long stabilization time before interacting with the AT86RF230.

9.4.3 Data Interpretation

The status bit values AVDD_OK = 1 and DVDD_OK = 1 indicate an enabled and stable internal supply voltage. Reading 0 indicates a disabled or unstable internal supply voltage.

9.4.4 Register Description

Register 0x10 (VREG_CTRL)

This register VREG_CTRL controls the use of the voltage regulators and indicates the status of these.

Bit	7	6	5	4	
0x10	AVREG_EXT	AVDD_OK	Reserved		VREG_CTRL
Read/Write	R/W	R	R/W	R/W	
Initial value	0	0	0	0	

Bit	3	2	1	0	
0x10	DVREG_EXT	DVDD_OK	Reserved		VREG_CTRL
Read/Write	R/W	R	R/W	R/W	
Initial value	0	0	0	0	

- **Bit 7 – AVREG_EXT**

The register bit AVREG_EXT defines whether the internal analog voltage regulator or an external regulator is used to supply the analog low voltage building blocks of the radio transceiver.

Table 9-2. Regulated Voltage Supply Control for Analog Building Blocks

Register Bit	Value	Description
AVREG_EXT	0	Use internal voltage regulator
	1	Use external voltage regulator, internal voltage regulator is disabled

- **Bit 6 – AVDD_OK**

This register bit AVDD_OK indicates if the internal 1.8V regulated supply voltage AVDD has settled. The bit is set to logic high, if AVREG_EXT = 1.

Table 9-3 Regulated Voltage Supply Control for Analog Building Blocks

Register Bit	Value	Description
AVDD_OK	0	Analog voltage regulator disabled or supply voltage not stable
	1	Analog supply voltage has settled

- **Bit [5:4] – Reserved**
- **Bit 7 – DVREG_EXT**

The register bit DVREG_EXT defines whether the internal digital voltage regulator or an external regulator is used to supply the digital low voltage building blocks of the radio transceiver.

Table 9-4. Regulated Voltage Supply Control for Digital Building Blocks

Register Bit	Value	Description
DVREG_EXT	0	Use internal voltage regulator
	1	Use external voltage regulator, internal voltage regulator is disabled

- **Bit 6 – DVDD_OK**

This register bit DVDD_OK indicates if the internal 1.8V regulated supply voltage DVDD has settled. The bit is set to logic high, if DVREG_EXT = 1.

Table 9-5 Regulated Voltage Supply Control for Digital Building Blocks

Register Bit	Value	Description
DVDD_OK	0	Digital voltage regulator disabled or supply voltage not stable
	1	Digital supply voltage has settled

- **Bit [1:0] – Reserved**

9.5 Battery Monitor (BATMON)

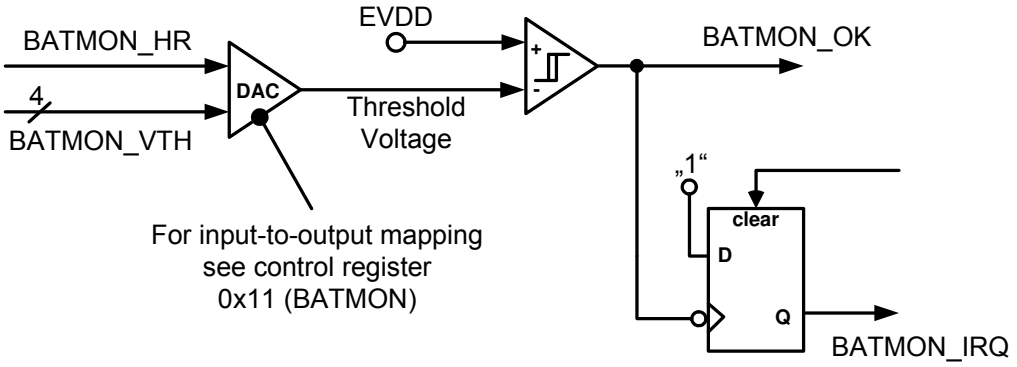
The main features of the battery monitor are:

- Programmable voltage threshold range: 1.7V to 3.675V
- Battery low voltage interrupt

9.5.1 Overview

The battery monitor (BATMON) detects and indicates a low supply voltage. This is done by comparing the voltage on the external supply pin (EVDD) with a programmable internal threshold voltage. A simplified schematic of the BATMON with the most important input and output signals is shown in Figure 9-3.

Figure 9-3. Simplified Schematic of BATMON



9.5.2 Data Interpretation

The signal bit BATMON_OK of register 0x11 (BATMON) indicates the current value of the battery voltage:

- If BATMON_OK = 0, the battery voltage is lower than the threshold voltage
- If BATMON_OK = 1, the battery voltage is higher than the threshold voltage

After setting a new threshold, the value BATMON_OK should be read out to verify the current supply voltage value.

Note, the battery monitor is inactive during P_ON and SLEEP states, see control register 0x01 (TRX_STATUS).

9.5.3 BATMON Interrupt Handling

A supply voltage drop below the programmed threshold value is indicated by the BAT_LOW interrupt, see control register 0x0E and 0x0F. The interrupt is issued only if BATMON_OK changes from 1 to 0.

No interrupt is generated when:

- The battery voltage is under the default 1.8V threshold at power up (BATMON_OK was never 1), or
- A new threshold is set, which is still above the current supply voltage (BATMON_OK remains 0).

Noise or temporary voltage drops may generate unwanted interrupts when the battery voltage is close to the programmed threshold voltage. To avoid this:

- Disable the IRQ_7 (BAT_LOW) in register 0x0E (IRQ_MASK) and treat the battery as empty, or
- Set a lower threshold value.

9.5.4 Register Description

Register 0x11 (BATMON)

The register BATMON configures the battery monitor. Additionally the supply voltage status at pin 28 (EVDD) is accessible by reading register bit BATMON_OK according to the actual BATMON settings.

Bit	7	6	5	4	
0x11	Reserved		BATMON_OK	BATMON_HR	BATMON
Read/Write	R	R	R	R/W	
Reset value	0	0	0	0	

Bit	3	2	1	0	
0x11	BATMON_VTH				BATMON
Read/Write	R/W	R/W	R/W	R/W	
Reset value	0	0	1	0	

- **Bit [7:6] – Reserved**
- **Bit 5 – BATMON_OK**

The register bit BATMON_OK indicates the level of the external supply voltage with respect to the programmed threshold BATMON_VTH.

Table 9-6. Battery Monitor Status

Register Bit	Value	Description
BATMON_OK	0	V_{DD} < BATMON_VTH
	1	V_{DD} > BATMON_VTH

- **Bit 4 – BATMON_HR**

The register bit BATMON_HR selects the range and resolution of the battery monitor.

Table 9-7. Battery Monitor Voltage Range Settings

Register Bit	Value	Description
BATMON_HR	0	Enables the low range, see BATMON_VTH
	1	Enables the high range, see BATMON_VTH

- **Bit [3:0] – BATMON_VTH**

The threshold value for the battery monitor is set with register bits BATMON_VTH.

Table 9-8. Battery Monitor Threshold Voltages

Value BATMON_VTH [3:0]	Threshold Voltage [V] BATMON_HR = 1	Threshold Voltage [V] BATMON_HR = 0
0x0	2.550	1.70
0x1	2.625	1.75
0x2	2.700	1.80
0x3	2.775	1.85
0x4	2.850	1.90
0x5	2.925	1.95
0x6	3.000	2.00
0x7	3.075	2.05
0x8	3.150	2.10
0x9	3.225	2.15
0xA	3.300	2.20
0xB	3.375	2.25
0xC	3.450	2.30
0xD	3.525	2.35
0xE	3.600	2.40
0xF	3.675	2.45

9.6 Crystal Oscillator (XOSC)

The main crystal oscillator features are:

- 16 MHz amplitude controlled crystal oscillator
- 500 µs typical settling time
- Integrated trimming capacitance array
- Programmable clock output (CLKM)

9.6.1 Overview

The crystal oscillator generates the reference frequency for the AT86RF230. All other internally generated frequencies of the radio transceiver are derived from this unique frequency. Therefore, the overall system performance is mainly based on the accuracy of this reference frequency. The external components of the crystal oscillator should be selected carefully and the related board layout should be done meticulously (refer to section 5).

The register 0x12 (XOSC_CTRL) provides access to the control signals of the oscillator. Two operating modes are supported. It is recommended to use the integrated oscillator setup as described in Figure 9-4, nevertheless a reference frequency can be fed to the internal circuitry by using an external clock reference as shown in Figure 9-5.

9.6.2 Integrated Oscillator Setup

Using the internal oscillator, the oscillation frequency strongly depends on the load capacitance between the crystal pins XTAL1 and XTAL2. The total load capacitance CL must be equal to the specified load capacitance of the crystal itself. It consists of the external capacitors CX and parasitic capacitances connected to the XTAL nodes. In Figure 9-4, all parasitic capacitances, such as PCB stray capacitances and the pin input capacitance, are summarized to C_{PAR}. Additional internal trimming capacitors C_{TRIM} are available. Any value in the range from 0 pF to 4.5 pF with a 0.3 pF resolution is selectable using XTAL_TRIM of register 0x12 (XOSC_CTRL). To calculate the total load capacitance, the following formula can be used

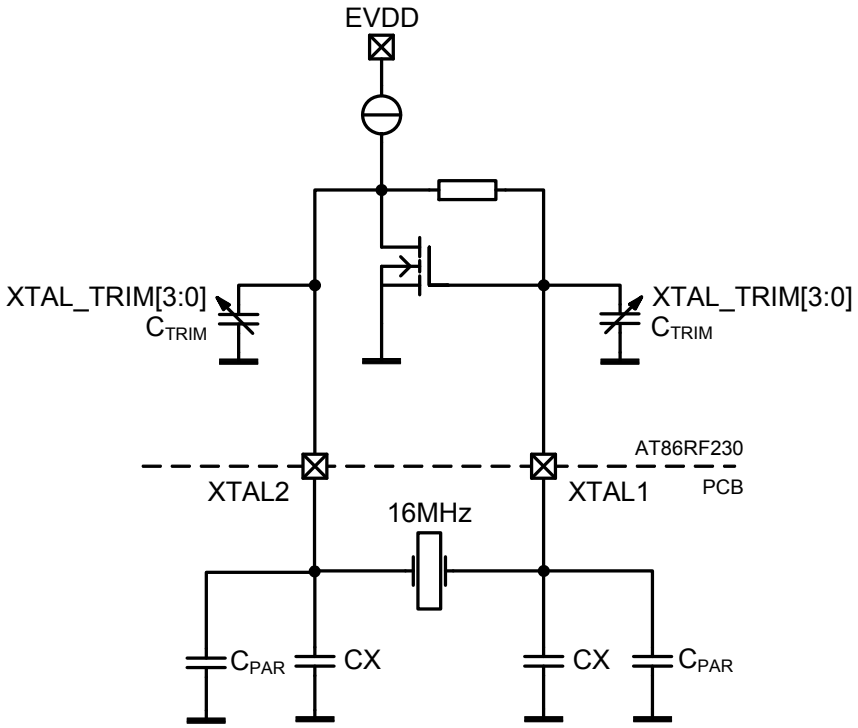
$$CL = 0.5 \bullet (CX + C_{TRIM} + C_{PAR}).$$

The trimming capacitors provide the possibility of reducing frequency deviations caused by production process variations or by external components tolerances. Note that the oscillation frequency can be reduced only by increasing the trimming capacitance. The frequency deviation caused by one step of C_{TRIM} decreases with increasing crystal load capacitor values.

A magnitude control circuit is included to ensure stable operation under different operating conditions and for different crystal types. A high current during the amplitude build-up phase guarantees a low start-up time. At stable operation, the current is reduced to the amount necessary for a robust operation. This also keeps the drive level of the crystal low.

Generally, crystals with a higher load capacitance are less sensitive to parasitic pulling effects caused by external component variations or by variations of board and circuit parasitics. On the other hand, a larger crystal load capacitance results in a longer start-up time and a higher steady state current consumption.

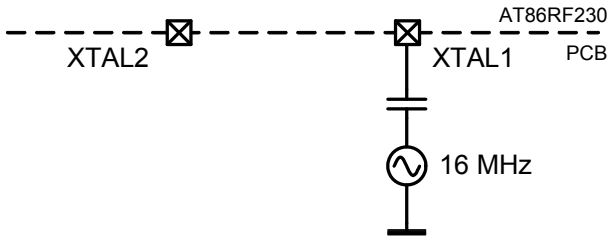
Figure 9-4. Simplified XOSC Schematic with External Components



9.6.3 External Reference Frequency Setup

When using an external reference frequency, the signal needs to be connected to pin XTAL1 as indicated in Figure 9-5 and the register XTAL_MODE of register 0x12 (XOSC_CTRL) need to be set to the external oscillator mode. The oscillation peak-to-peak amplitude shall be 400 mV, but not larger than 500 mV.

Figure 9-5. Setup for Using an External Frequency Reference



9.6.4 Master Clock Signal Output (CLKM)

The generated reference clock signal can be fed to a microcontroller using pin 17 (CLKM). The internal 16 MHz raw clock can be divided by an internal prescaler. Thus, clock frequencies of 16 MHz, 8 MHz, 4 MHz, 2 MHz or 1 MHz can be supplied by pin CLKM.

The CLKM frequency and pin driver strength is configurable using register 0x03 (TRX_CTRL_0). There are two possibilities to change the CLKM frequency. If CLKM_SHA_SEL = 0, changing the register bits CLKM_CTRL (register 0x03, TRX_CTRL_0) immediately affects the CLKM clock rate. Otherwise (CLKM_SHA_SEL = 1) the new clock rate is supplied when leaving the SLEEP state the next time.

To reduce power consumption and spurious emissions, it is recommended to turn off the CLKM clock when not in use or to reduce its driver strength to a minimum, refer to section 4.3.

Note:

During reset procedure, see section 7.1.4.2, register bits CLKM_CTRL are shadowed. Although the clock setting of CLKM remains after reset, a read access to register bits CLKM_CTRL delivers the reset value 1. For that reason it is recommended to write the previous configuration (before reset) to the CLKM_CTRL to align the radio transceiver behavior and register configuration. Otherwise the CLKM clock rate is set back to the reset value (1 MHz) after the next SLEEP cycle.

For example if the CLKM clock rate is configured to 16 MHz the CLKM rate remains at 16 MHz after a reset, however the register bits CLKM_CTRL are set back to 1. Since CLKM_SHA_SEL reset value is 1, the CLKM clock rate would change to 1 MHz after the next SLEEP cycle if the CLKM_CTRL setting is not updated.

9.6.5 Register Description

Register 0x03 (TRX_CTRL_0)

The TRX_CTRL_0 register controls the drive current of the digital output pads and the CLKM clock rate.

Bit	7	6	5	4	
0x03	PAD_IO		PAD_IO_CLKM		TRX_CTRL_0
Read/Write	R/W	R/W	R/W	R/W	
Reset value	0	0	0	1	

Bit	3	2	1	0	
0x03	CLKM_SHA_SEL	CLKM_CTRL			TRX_CTRL_0
Read/Write	R/W	R/W	R/W	R/W	
Reset value	1	0	0	1	

- **Bit [7:6] – PAD_IO**

Refer to in section 4.3.3.

- **Bit [5:6] – PAD_IO_CLKM**

The register bits PAD_IO_CLKM set the output driver current of pin CLKM.

Table 9-9. CLKM Driver Strength

Register Bit	Value	Description
PAD_IO_CLKM	0	2 mA
	1	4 mA
	2	6 mA
	3	8 mA

- **Bit 3 – CLKM_SHA_SEL**

The register bit CLKM_SHA_SEL defines the commencement of the CLKM clock rate modifications when changing register bits CLKM_CTRL.

Table 9-10. Commencement of CLKM Clock Rate Modification

Register Bit	Value	Description
CLKM_SHA_SEL	0	CLKM clock rate changes immediately

Register Bit	Value	Description
	1	CLKM clock rate changes after SLEEP cycle

- **Bit [2:0] – CLKM_CTRL**

The register bits CLKM_CTRL set clock rate of pin CLKM.

Table 9-11. Clock Rate at Pin CLKM

Register Bit	Value	Description
CLKM_CTRL	0	No clock, pin set to logic low
	1	1 MHz
	2	2 MHz
	3	4 MHz
	4	8 MHz
	5	16 MHz
	6	Reserved
	7	Reserved

Register 0x12 (XOSC_CTRL)

The register XOSC_CTRL controls the operation of the crystal oscillator.

Bit	7	6	5	4	
0x12	XTAL_MODE				XOSC_CTRL
Read/Write	R/W	R/W	R/W	R/W	
Initial value	1	1	1	1	

Bit	3	2	1	0	
0x12	XTAL_TRIM				XOSC_CTRL
Read/Write	R/W	R/W	R/W	R/W	
Initial value	0	0	0	0	

- **Bit [7:4] – XTAL_MODE**

The register bit XTAL_MODE sets the operating mode of the crystal oscillator.

Table 9-12. Crystal Oscillator Operating Mode

Register Bit	Value	Description
XTAL_MODE	0x0	Crystal oscillator disabled, no clock signal is fed to the internal circuitry.
	0x4	Internal crystal oscillator disabled, use external reference frequency
	0xF	Internal crystal oscillator enabled

- **Bit [3:0] – XTAL_TRIM**

The register bits XTAL_TRIM control two internal capacitance arrays connected to pins XTAL1 and XTAL2. A capacitance value in the range from 0 pF to 4.5 pF is selectable with a resolution of 0.3 pF.

Table 9-13. Crystal Oscillator Trimming Capacitors

Register Bit	Value	Description
XTAL_TRIM	0x0	0.0 pF, trimming capacitors disconnected

Register Bit	Value	Description
	0x1	0.3 pF, trimming capacitor switched on
	…	
	0xF	4.5 pF, trimming capacitor switched on

9.7 Frequency Synthesizer (PLL)

The main PLL features are:

- Generate RX/TX frequencies for all IEEE 802.15.4 - 2.4 GHz channels
- Fully integrated fractional-N synthesizer
- Autonomous calibration loops for stable operation within the operating range
- Two PLL-interrupts for status indication

9.7.1 Overview

The synthesizer of the AT86RF230 is implemented as a fractional-N PLL. The PLL is fully integrated and configurable by registers 0x08 (PHY_CC_CCA), 0x1A (PLL_CF) and 0x1B (PLL_DCU).

The PLL is turned on when entering the state PLL_ON and stays on in all receive and transmit states. The PLL settles to the correct frequency needed for RX or TX operation according to the adjusted channel center frequency in register 0x08 (PHY_CC_CCA).

Two calibration loops ensure correct PLL functionality within the specified operating limits.

9.7.2 RF Channel Selection

The PLL is designed to support 16 channels in the IEEE 802.15.4 – 2.4 GHz band with a channel spacing of 5 MHz. The center frequency F_{CH} of these channels is defined as follows:

$F_{CH} = 2405 + 5\ (k - 11)$ [MHz], for k = 11, 12, ..., 26

where k is the channel number.

The channel k is selected by register bits CHANNEL (register 0x08, PHY_CC_CA).

9.7.3 Calibration Loops

The center frequency control loop ensures a correct center frequency of the VCO for the currently programmed channel.

The delay calibration unit compensates the phase errors inherent in fractional-N PLLs. Using this technique, unwanted spurious frequency components beside the RF carrier are suppressed, and the PLL behaves similar to an integer-N PLL.

Both calibration routines are initiated automatically when the PLL is turned on. Additionally, the center frequency calibration is running when the PLL is programmed to a different channel (register bits CHANNEL in register 0x08).

If the PLL operates for a long time on the same channel or the operating temperature changes significantly, the control loops should be initiated manually. The recommended calibration interval is 5 min.

Both calibration loops can be initiated manually by setting PLL_CF_START = 1 of register 0x1A (PLL_CF) and register bit PLL_DCU_START = 1 of register 0x1B

(PLL_DCU). To start the calibrations routines the device should be in state PLL_ON. The center frequency tuning takes a maximum of 80 µs. The completion is indicated by a PLL_LOCK interrupt. The delay cell calibration loop is completed after 6 µs. This is typically not indicated by a PLL_LOCK interrupt.

9.7.4 PLL Interrupt Handling

There are two different interrupts indicating the PLL status (see register 0x0F). The PLL_LOCK interrupt indicates that the PLL has locked. The PLL_UNLOCK interrupt indicates an unexpected unlock condition. A PLL_LOCK interrupt clears any preceding PLL_UNLOCK interrupt automatically and vice versa.

A PLL_LOCK interrupt occurs in the following situations:

- State change from TRX_OFF to PLL_ON/RX_ON
- Channel change in states PLL_ON/RX_ON
- Initiating a center frequency tuning manually

The state transition from BUSY_TX to PLL_ON can also initiate a PLL_LOCK interrupt, due to the PLL settling back to the RX frequency.

Any other occurrences of PLL interrupts indicate erroneous behavior and require checking of the actual device status.

9.7.5 Register Description

Register 0x08 (PHY_CC_CCA)

The PHY_CC_CCA register contains register bits to initiate and control the CCA measurement as well as to set the channel center frequency.

Bit	7	6	5	4	
0x08	CCA_REQUEST	CCA_MODE		CHANNEL	PHY_CC_CCA
Read/Write	R/W	R/W	R/W	R/W	
Reset value	0	0	1	0	

Bit	3	2	1	0	
0x08	CHANNEL				PHY_CC_CCA
Read/Write	R/W	R/W	R/W	R/W	
Reset value	1	0	1	1	

- **Bit 7 – CCA_REQUEST**

Refer to section 8.6.4.

- **Bit [6:5] – CCA_MODE**

Refer to section 8.6.4.

- **Bit [4:0] – CHANNEL**

The register bits CHANNEL define the RX/TX channel. The channel assignment is according to IEEE 802.15.4.

Table 9-14. Channel Assignment for IEEE 802.15.4 – 2.4 GHz Band

Register Bit	Value	Channel Number	Center Frequency [MHz]
CHANNEL	0x0B	11	2405
	0x0C	12	2410
	0x0D	13	2415
	0x0E	14	2420

Register Bit	Value	Channel Number	Center Frequency [MHz]
	0x0F	15	2425
	0x10	16	2430
	0x11	17	2435
	0x12	18	2440
	0x13	19	2445
	0x14	20	2450
	0x15	21	2455
	0x16	22	2460
	0x17	23	2465
	0x18	24	2470
	0x19	25	2475
	0x1A	26	2480

Register 0x1A (PLL_CF)

The register PLL_CF controls the operation of the center frequency calibration loop.

Bit	7	6	5	4	
0x1A	PLL_CF_START	Reserved			PLL_CF
Read/Write	R/W	R/W	R/W	R/W	
Reset value	0	1	0	1	

Bit	3	2	1	0	
0x1A	Reserved				PLL_CF
Read/Write	R/W	R/W	R/W	R/W	
Reset value	0	1	1	1	

- **Bit 7 – PLL_CF_START**

PLL_CF_START = 1 initiates the center frequency calibration. The calibration cycle has finished after a maximum of 80 µs. The register bit is cleared immediately after the register write operation.

- **Bit [6:0] – Reserved**

Register 0x1B (PLL_DCU)

The register PLL_DCU controls the operation of the delay cell calibration loop.

Bit	7	6	5	4	
0x1B	PLL_DCU_START	Reserved			PLL_DCU
Read/Write	R/W	R	R/W	R/W	
Reset value	0	0	1	0	

Bit	3	2	1	0	
0x1B	Reserved				PLL_DCU
Read/Write	R/W	R/W	R/W	R/W	
Reset value	0	0	0	0	

- **Bit 7 – PLL_DCU_START**

PLL_DCU_START = 1 initiates the delay cell calibration. The calibration cycle has finished after maximum of 6 µs. The register bit is cleared immediately after the register write operation.

- **Bit [6:0] – Reserved**

9.8 Automatic Filter Tuning (FTN)

The filter-tuning unit is a separate block within the AT86RF230. The filter-tuning result is used to provide a correct SSBF transfer function and PLL loop-filter time constant independent of temperature effects and part-to-part variations.

A calibration cycle is initiated automatically when entering the TRX_OFF state from the SLEEP, RESET or P_ON states.

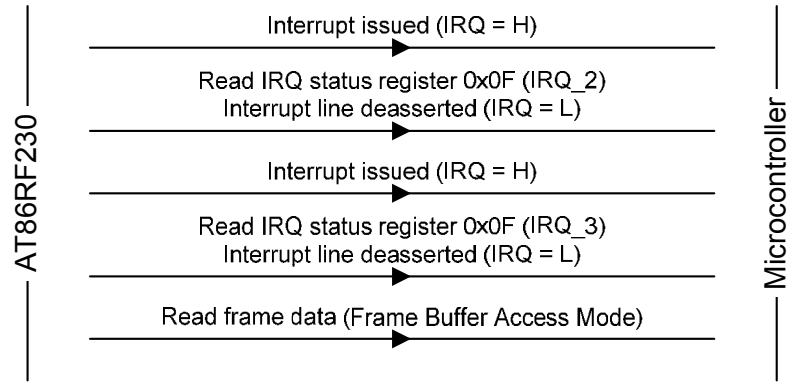
10 Radio Transceiver Usage

This section describes basic procedures to receive and transmit frames using the AT86RF230. For a detailed programming description refer to application note AVR2009 “AT86RF230 – Software Programming Model”.

10.1 Frame Receive Procedure

While in state RX_ON the radio transceiver searches for incoming frames on the selected channel. A detection of a valid IEEE 802.15.4 frame is indicated by an IRQ_2 (RX_START) interrupt. The frame reception is completed when issuing the IRQ_3 (TRX_END) interrupt. Waiting for IRQ_3 (TRX_END) interrupt before uploading the frame to the microcontroller is recommended for operations considered to be non time critical. Figure 9-6 illustrates the frame receive procedure.

Figure 9-6. Frame Receive Procedure - Transactions between AT86RF230 and Microcontroller



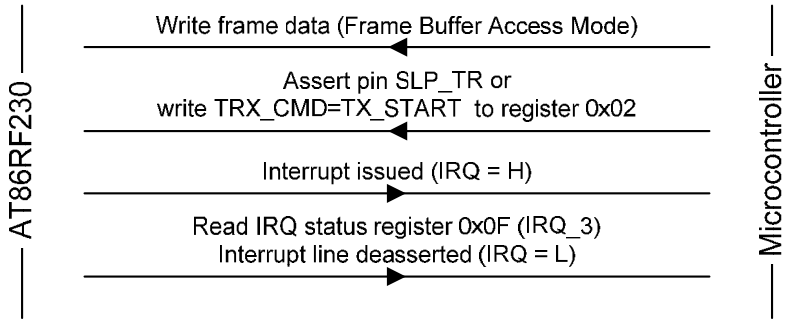
Critical protocol timing could require starting the frame upload as soon as possible. The first byte of the frame data can be read 32 µs after the IRQ_2 (RX_START) interrupt. The microcontroller must ensure to read slower than the frame is received. Otherwise, the Frame Buffer wills under run, IRQ_6 (TRX_UR) interrupt is issued. The frame data are not valid anymore and need to read again. The LQI byte can be uploaded to the microcontroller after the IRQ_3 (TRX_END) interrupt was issued.

10.2 Frame Transmit Procedure

A frame transmission comprises two actions, a frame download to the Frame Buffer and the transmission of the Frame Buffer content. Both actions can be run in parallel if required by critical protocol timing.

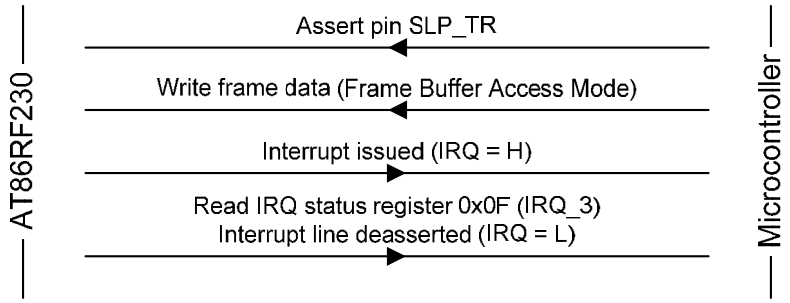
Figure 9-7 illustrates the frame transmit procedure, when downloading and transmitting the frame consecutively. After a frame download by a Frame Buffer write access, the frame transmission is initiated by asserting pin SLP_TR or writing the TRX command TX_START to register 0x02 (TRX_STATE), while the radio transceiver is in state PLL_ON. The completion of the transmission is indicated by an IRQ_3 (TRX_END) interrupt.

Figure 9-7. Frame Transmit Procedure - Transactions between AT86RF230 and Microcontroller



Alternatively, the frame transmission can be started before the frame data download as described in Figure 9-8. This is useful for time critical applications. At the rising edge of SPL_TR, the radio transceiver starts transmitting the preamble and the SFD field, which takes about 176 µs (see Figure 7-2). The first byte of the PSDU must be available in the Frame Buffer before this time. The SPI data rate must be higher than 250 kBit/s to ensure that no Frame Buffer under run occurs (IRQ_6, TRX_UR).

Figure 9-8. Time Optimized Frame Transmit Procedure - Transactions between AT86RF230 and Microcontroller



11 Technical Parameters

11.1 Absolute Maximum Ratings

Note: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 11-1. Absolute Maximum Ratings

No	Parameter	Symbol	Min	Typ	Max	Unit	Conditions/Notes
11.1.1	Storage temperature	T_{stor}	-50		150	°C	
11.1.2	Lead temperature	T_{lead}			260	°C	
11.1.3	ESD robustness	V_{ESD}	4 750			kV V	Compl. to [2] Compl. to [3]
11.1.4	Input RF level	P_{RF}			+14	dBm	
11.1.5	Voltage on all pins (except pins 4, 5, 13, 14, 29)		-0.3		V_{DD}+0.3		
11.1.6	Voltage on pins 4, 5, 13, 14, 29		-0.3		2.0		

11.2 Recommended Operating Range

Table 11-2. Operating Range

No	Parameter	Symbol	Min	Typ	Max	Unit	Conditions/Notes
11.2.1	Operating temperature range	T_{op}	-40		+85	°C	
11.2.2	Supply voltage	V_{DD}	1.8	3.0	3.6	V	
11.2.3	Supply voltage (on pins 13, 14, 29)	$V_{DD1.8}$	1.65	1.8	1.95	V	When using external voltage regulators (see section 9.4).

11.3 Digital Pin Specifications

Test Conditions (unless otherwise stated):

T_{op} = 25°C

Table 11-3. Digital Pin Specifications

No	Parameter	Symbol	Min	Typ	Max	Unit	Conditions/Notes
11.3.1	High level input voltage	V_{IH}	V_{DD} – 0.4			V	
11.3.2	Low level input voltage	V_{IL}			0.4	V	
11.3.3	High level output voltage	V_{OH}	V_{DD} – 0.4			V	For all output driver strengths defined in TRX_CTRL_0
11.3.4	Low level output voltage	V_{OL}			0.4	V	For all output driver strengths defined in TRX_CTRL_0

11.4 Digital Interface Timing Specifications

Test Conditions (unless otherwise stated):

V_{DD} = 3V, T_{op} = 25°C

Table 11-4. Digital Interface Timing Parameters

No	Parameter	Symbol	Min	Typ	Max	Unit	Conditions/Notes
11.4.1	SCLK frequency (synchronous mode)				8	MHz	
11.4.2	SCLK frequency (asynchronous mode)				7.5	MHz	
11.4.3	$\overline{SEL}$ low to MISO active	t_1			180	ns	
11.4.4	SCLK to MISO out	t_2	10			ns	data hold time
11.4.5	MOSI setup time	t_3	10			ns	
11.4.6	MOSI hold time	t_4	10			ns	
11.4.7	LSB last byte to MSB next byte	t_5	250			ns	
11.4.8	$\overline{SEL}$ high to MISO tristate	t_6			10	ns	
11.4.9	SLP_TR pulse width	t_7	65			ns	TX start trigger
11.4.10	SPI idle time	t_8	250			ns	Idle time between consecutive SPI accesses
11.4.11	Last SCLK to $\overline{SEL}$ high	t_9	250			ns	
11.4.12	Reset pulse width		625			ns	≥ 10 clock cycles at 16 MHz
11.4.13	Output clock frequency (CLKM)			0 1 2 4 8 16		MHz MHz MHz MHz MHz MHz	Programmable in register TRX_CTRL_0

11.5 General RF Specifications

Test Conditions (unless otherwise stated):

V_{DD} = 3V, f = 2.45 GHz, T_{op} = 25°C, Measurement setup see Figure 5-1

Table 11-5. General RF Parameters

No	Parameter	Symbol	Min	Typ	Max	Unit	Conditions/Notes
11.5.1	Frequency range	f	2405		2480	MHz	As specified in [1]
11.5.2	Bit rate	f_{bit}		250		kbit/s	As specified in [1]
11.5.3	Chip rate	f_{chip}		2000		kchip/s	As specified in [1]
11.5.4	Reference oscillator frequency	f_{clk}		16		MHz	
11.5.5	Reference oscillator settling time			0.5	1	ms	Leaving SLEEP state to clock available at pin CLKM
11.5.6	Reference frequency accuracy for proper functionality		-60		+60	ppm	±40 ppm is required by [1]
11.5.7	TX signal 20 dB bandwidth	B_{20dB}		2.8		MHz	RBW 100 kHz VBW 300 kHz

11.6 Transmitter Specifications

Test Conditions (unless otherwise stated):

V_{DD} = 3V, f = 2.45 GHz, T_{op} = 25°C, Measurement setup see Figure 5-1

Table 11-6. TX Parameters

No	Parameter	Symbol	Min	Typ	Max	Unit	Conditions/Notes
11.6.1	Output power	P_{TX}	0	3	6	dBm	Maximum configurable value
11.6.2	Output power range			20		dB	Configurable in register PHY_TX_PWR
11.6.3	Output power tolerance				±3	dB	
11.6.4	TX Return loss			10		dB	
11.6.5	EVM			8		%rms	
11.6.6	Harmonics 2nd harmonic 3rd harmonic			 -38 -45		 dBm dBm	
11.6.7	Spurious emissions 30 – ≤ 1000 MHz >1 – 12.75 GHz 1.8 – 1.9 GHz 5.15 – 5.3 GHz				 -36 -30 -47 -47	 dBm dBm dBm dBm	Complies with EN 300 328/440, FCC-CFR-47 part 15, ARIB STD-66, RSS-210

11.7 Receiver Specifications

Test Conditions (unless otherwise stated):

V_{DD} = 3V, f = 2.45 GHz, T_{op} = 25°C, Measurement setup see Figure 5-1

Table 11-7. RX Parameters

No	Parameter	Symbol	Min	Typ	Max	Unit	Conditions/Notes
11.7.1	Receiver sensitivity			-101		dBm	AWGN channel, PER ≤ 1%, PSDU length of 20 octets
11.7.2	RX Return loss			10		dB	100Ω differential impedance
11.7.3	Noise figure	NF		6		dB	
11.7.4	Maximum RX input level			10		dBm	PER ≤ 1%, PSDU length of 20 octets
11.7.5	Adjacent channel rejection -5 MHz			34		dBm	PER ≤ 1%, PSDU length of 20 octets, P_{RF} = -82 dBm
11.7.6	Adjacent channel rejection +5 MHz			36		dBm	PER ≤ 1%, PSDU length of 20 octets, P_{RF} = -82 dBm
11.7.7	Alternate adjacent channel rejection -10 MHz			52		dBm	PER ≤ 1%, PSDU length of 20 octets, P_{RF} = -82 dBm
11.7.8	Alternate adjacent channel rejection +10 MHz			53		dBm	PER ≤ 1%, PSDU length of 20 octets, P_{RF} = -82 dBm
11.7.9	Spurious emissions LO leakage 30 – ≤ 1000 MHz >1 – 12.75 GHz			 -75	 -57 -47	 dBm dBm dBm	

No	Parameter	Symbol	Min	Typ	Max	Unit	Conditions/Notes
11.7.10	TX/RX carrier frequency offset tolerance		-300		300	kHz	Sensitivity loss < 2 dB; equals 120 ppm ([1] requires 80 ppm)
11.7.11	3rd-order intercept point	IIP3		-9		dB	At maximum gain Offset freq. interf. 1 = 5 MHz Offset freq. interf. 2 = 10 MHz
11.7.12	2nd-order intercept point	IIP2		24		dB	At maximum gain Offset freq. interf. 1 = 60 MHz Offset freq. interf. 2 = 62 MHz
11.7.13	RSSI tolerance				±5	dB	
11.7.14	RSSI dynamic range			81		dB	
11.7.15	RSSI resolution			3		dB	
11.7.16	RSSI sensitivity			-91		dBm	Defined as RSSI_BASE_VAL
11.7.17	Minimum RSSI value			0			P_{RF} < RSSI_BASE_VAL
11.7.18	Maximum RSSI value			28			P_{RF} ≥ RSSI_BASE_VAL + 81 dB

11.8 Current Consumption Specifications

Test Conditions (unless otherwise stated):

V_{DD} = 3V, f = 2.45 GHz, T_{op} = 25°C, Measurement setup see Figure 5-1

Table 11-8. Current Consumption

No	Parameter	Symbol	Min	Typ	Max	Unit	Conditions/Notes
11.8.1	Supply current transmit state	I_{BUSY_TX}		16.5 14.5 12.5 9.5		mA mA mA mA	P_{TX} = 3 dBm P_{TX} = 1 dBm P_{TX} = -3 dBm P_{TX} = -17 dBm (At each output power level, the supply current consumption can be decreased by approx. 2 mA if reducing V_{DD} to 1.8V.)
11.8.2	Supply current receive state	I_{RX_ON}		15.5		mA	State: RX_ON
11.8.3	Supply current TRX_OFF state	I_{TRX_OFF}		1.5		mA	State: TRX_OFF
11.8.4	Supply current SLEEP state	I_{SLEEP}		0.02		µA	State: SLEEP
11.8.5	Supply current PLL_ON state	I_{PLL_ON}		7.8		mA	State: PLL_ON

11.9 Crystal Parameter Requirements

Table 11-9. Crystal Parameter Requirements

No	Parameter	Symbol	Min	Typ	Max	Unit	Conditions/Notes
11.9.1	Crystal frequency	f_0		16		MHz	
11.9.2	Load capacitance	C_L	8		14	pF	
11.9.3	Static capacitance	C_0			7	pF	
11.9.4	Series resistance	R_1			100	Ω	

12 Register Reference

The AT86RF230 provides a register space of 64 8-bit registers, which is used to configure, control and monitor the radio transceiver. The registers can be accessed in any order.

Note: All registers not mentioned within the following table are reserved for internal use and must not be overwritten. When writing to a register, any reserved bits shall be overwritten only with their reset value (see Table 12-2).

Table 12-1. Register Summary – Non Reserved Registers

Addr.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
0x01	TRX_STATUS	CCA_DONE	CCA_STATUS	Reserved	TRX_STATUS					pg. 27, 38, 55
0x02	TRX_STATE	TRAC_STATUS			TRX_CMD					pg. 28, 39
0x03	TRX_CTRL_0	PAD_IO		PAD_IO_CLKM		CLKM_SHA_SEL	CLKM_CTRL			pg. 7, 69
0x05	PHY_TX_PWR	TX_AUTO_CRC_ON	Reserved			TX_PWR				pg. 49, 59
0x06	PHY_RSSI	RX_CRC_VALID	Reserved		RSSI					pg. 50, 52
0x07	PHY_ED_LEVEL	ED_LEVEL								pg. 51
0x08	PHY_CC_CCA	CCA_REQUEST	CCA_MODE		CHANNEL					pg. 56, 72
0x09	CCA_THRES	Reserved				CCA_ED_THRES				pg. 57
0x0E	IRQ_MASK	MASK_BAT_LOW	MASK_TRX_UR	Reserved		MASK_TRX_END	MASK_RX_START	MASK_PLL_UNLOCK	MASK_PLL_LOCK	pg. 20
0x0F	IRQ_STATUS	BAT_LOW	TRX_UR	Reserved		TRX_END	RX_START	PLL_UNLOCK	PLL_LOCK	pg. 20
0x10	VREG_CTRL	AVREG_EXT	AVDD_OK	Reserved		DVREG_EXT	DVDD_OK	Reserved		pg. 63
0x11	BATMON	Reserved		BATMON_OK	BATMON_HR	BATMON_VTH				pg. 65
0x12	XOSC_CTRL	XTAL_MODE				XTAL_TRIM				pg. 70
0x1A	PLL_CF	PLL_CF_START	Reserved							pg. 73
0x1B	PLL_DCU	PLL_DCU_START	Reserved							pg. 73
0x1C	PART_NUM	PART_NUM								pg. 16
0x1D	VERSION_NUM	VERSION_NUM								pg. 16
0x1E	MAN_ID_0	MAN_ID_0								pg. 17
0x1F	MAN_ID_1	MAN_ID_1								pg. 17
0x20	SHORT_ADDR_0	SHORT_ADDR_0								pg. 42
0x21	SHORT_ADDR_1	SHORT_ADDR_1								pg. 42
0x22	PAN_ID_0	PAN_ID_0								pg. 42
0x23	PAN_ID_1	PAN_ID_1								pg. 42
0x24	IEEE_ADDR_0	IEEE_ADDR_0								pg. 43
0x25	IEEE_ADDR_1	IEEE_ADDR_1								pg. 43
0x26	IEEE_ADDR_2	IEEE_ADDR_2								pg. 43
0x27	IEEE_ADDR_3	IEEE_ADDR_3								pg. 43
0x28	IEEE_ADDR_4	IEEE_ADDR_4								pg. 43
0x29	IEEE_ADDR_5	IEEE_ADDR_5								pg. 43
0x2A	IEEE_ADDR_6	IEEE_ADDR_6								pg. 44
0x2B	IEEE_ADDR_7	IEEE_ADDR_7								pg. 44
0x2C	XAH_CTRL	MAX_FRAME_RETRIES				MAX_CSMA_RETRIES			Reserved	pg. 40
0x2D	CSMA_SEED_0	CSMA_SEED_0								pg. 41
0x2E	CSMA_SEED_1	MIN_BE		AACK_SET_PD	Reserved	I_AM_COORD	CSMA_SEED_1			pg. 41

Notes:

- Reset values in Table 12-2 are only valid after a power on reset. After a reset procedure ($\overline{RST}$ = L) as described in section 7.1.4.2 the reset values of selected registers (e.g. registers 0x01, 0x10, 0x11) can differ from that in Table 12-2.
- Read value of register 0x30 after a reset in state:

  P_ON 0x11
  Any other state 0x07

Table 12-2. Register Summary – Reset values

Address	Reset Value	Address	Reset Value	Address	Reset Value	Address	Reset Value
0x00	0x00	0x10	0x00	0x20	0x00	0x30	0x00
0x01	0x00	0x11	0x02	0x21	0x00	0x31	0x00
0x02	0x00	0x12	0xF0	0x22	0x00	032	0x00
0x03	0x19	0x13	0x00	0x23	0x00	0x33	0x00
0x04	0x00	0x14	0x00	0x24	0x00	0x34	0x00
0x05	0x00	0x15	0x00	0x25	0x00	0x35	0x00
0x06	0x00	0x16	0x00	0x26	0x00	0x36	0x00
0x07	0x00	0x17	0x00	0x27	0x00	0x37	0x00
0x08	0x2B	0x18	0x58	0x28	0x00	0x38	0x00
0x09	0xC7	0x19	0x55	0x29	0x00	0x39	0x40
0x0A	0xBC	0x1A	0x5F	0x2A	0x00	0x3A	0x00
0x0B	0xA7	0x1B	0x20	0x2B	0x00	0x3B	0x00
0x0C	0x04	0x1C	0x02	0x2C	0x38	0x3C	0x00
0x0D	0x00	0x1D	0x02	0x2D	0xEA	0x3D	0x00
0x0E	0xFF	0x1E	0x1F	0x2E	0xC2	0x3E	0x00
0x0F	0x00	0x1F	0x00	0x2F	0x00	0x3F	0x00

Abbreviations

AACK	—	Auto acknowledge
ACK	—	Acknowledge
ADC	—	Analog-to-digital converter
AGC	—	Automatic gain control
ARET	—	Auto retry
AVREG	—	Analog voltage regulator
AWGN	—	Additive White Gaussian Noise
BATMON	—	Battery monitor
BBP	—	Base-band processor
BG	—	Band gap reference
BoM	—	Bill of material
CCA	—	Clear channel assessment
CRC	—	Cyclic redundancy check
CSMA	—	Carrier sense multiple access
CW	—	Continuous wave
DCLK	—	Digital clock
DCU	—	Delay calibration unit
DVREG	—	Digital voltage regulator
ED	—	Energy detection
ESD	—	Electro static discharge
EVM	—	Error vector magnitude
FCS	—	Frame Check Sequence
FCF	—	Frame Control Field
FIFO	—	First in first out
FTN	—	Automatic filter tuning
GPIO	—	General purpose input output
ISM	—	Industrial, scientific, and medical
LDO	—	Low-drop output
LNA	—	Low-noise amplifier
LO	—	Local oscillator
LQI	—	Link-quality indication
LSB	—	Least significant bit
MAC	—	Medium access control
MFR	—	MAC Footer
MHR	—	MAC header
MSB	—	Most significant bit
MSDU	—	MAC service data unit
MSK	—	Minimum shift keying
NOP	—	No operation
O-QPSK	—	Offset-quadrature phase shift keying
PA	—	Power amplifier

PAN	—	Personal area network
PCB	—	Printed circuit board
PER	—	Packet error rate
PHY	—	Physical layer
PHR	—	PHY Header
PLL	—	Phase-locked loop
POR	—	Power-on reset
PPF	—	Poly-phase filter
PRBS	—	Pseudo random binary sequence
PSDU	—	PHY service data unit
QFN	—	Quad flat no-lead package
RAM	—	Random access memory
RBW	—	Resolution band width
RSSI	—	Received signal strength indicator
RX	—	Receiver
SFD	—	Start-of-frame delimiter
SHR	—	Synchronization Header
SPI	—	Serial peripheral interface
SRAM	—	Static random access memory
SSBF	—	Single side band filter
TX	—	Transmitter
VBW	—	Video band width
VCO	—	Voltage controlled oscillator
VREG	—	Voltage regulator
XOSC	—	Crystal stabilized oscillator

13 Ordering Information

Ordering Code	Package	Voltage Range	Temperature Range
AT86RF230-ZU	QN	1.8V – 3.6V	Industrial (-40° C to +85° C) Lead-free/Halogen-free

Package Type	Description
QN	32QN1, 32-lead 5.0x5.0 mm Body, 0.50 mm Pitch, Quad Flat No-lead Package (QFN) Sawn

Note: T&R quantity 5,000.

Please contact your local Atmel sales office for more detailed ordering information and minimum quantities.

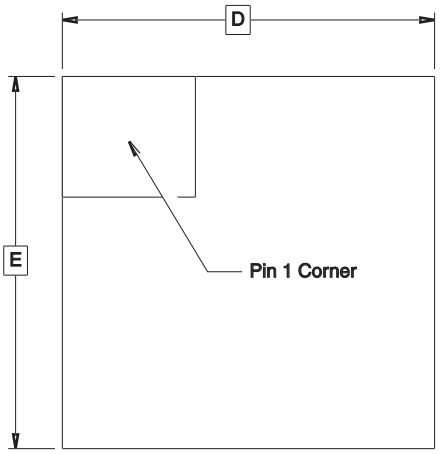
14 Soldering Information

Recommended soldering profile is specified in IPC/JEDEC J-STD-.020C.

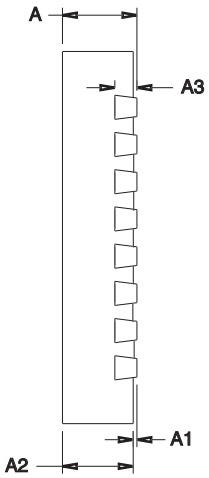
15 Package Thermal Properties

Thermal Resistance	
Velocity [m/s]	Theta ja [K/W]
0	40.9
1	35.7
2.5	32.0

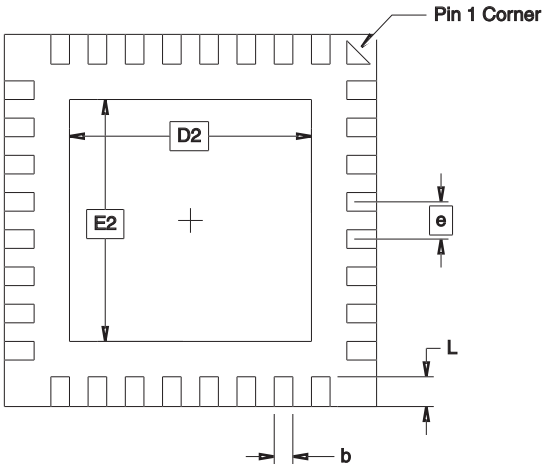
16 Package Drawing – 32QN1



Top View



Side View



Bottom View

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
D		5.00 BSC		
E		5.00 BSC		
D2	3.20	3.30	3.40	
E2	3.20	3.30	3.40	
A	0.80	0.90	1.00	
A1	0.0	0.02	0.05	
A2	0.0	0.65	1.00	
A3		0.20 REF		
L	0.30	0.40	0.50	
e		0.50 BSC		
b	0.18	0.23	0.30	2

Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MO-220, Variation VHHD-6, for proper dimensions, tolerances, datums, etc.
2. Dimension b applies to metallized terminal and is measured between 0.15 mm and 0.30 mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension should not be measured in that radius area.

11/26/07

	TITLE	GPC	DRAWING NO.	REV.
Package Drawing Contact: packagedrawings@atmel.com	**32QN2**, 32-lead 5.0 x 5.0 mm Body, 0.50 mm Pitch, Quad Flat No Lead Package (QFN) Sawn	ZJZ	32QN2	A

Appendix A - Continuous Transmission Test Mode

The Continuous Transmission Test Mode offers the following features:

- Continuous frame transmission
- Continuous wave signal transmission

A.1 - Overview

The AT86RF230 offers a Continuous Transmission Test Mode to support final application/production tests as well as certification tests. Using this test mode the radio transceiver transmits continuously a previously downloaded frame data (PRBS mode) or a continuous wave signal (CW mode).

In CW mode three different signal frequencies can be transmitted:

$f_1 = f_{CH} – 2$ MHz

$f_2 = f_{CH} + 0.5$ MHz

$f_3 = f_{CH} - 0.5$ MHz

where f_{CH} is the center frequency of the current programmed cannel in register 0x08 (PHY_CC_CCA). Note that it is not possible to transmit a CW signal on the channel center frequency. Before starting a CW signal transmission valid data needs to be downloaded to the Frame Buffer (refer to section 6.2.2), e.g a PHR field denotes a frame length of 1 and one octet PSDU data.

In PRBS mode the transmission center frequency is f_{CH}. Data downloaded to the Frame Buffer must contain at least a valid Frame Length Field (see sections 8.1 and 9.1). It is recommended to use a frame of maximum length (127 bytes) and arbitrary PSDU data. In contrast to normal frame transmission here the SHR and the PHR are not transmitted. The transmission starts with the PSDU data and is repeated continuously.

A.2 - Configuration

Before enabling the Continuous Transmission Test Mode (TST = 1) all register configurations shall be done as follows:

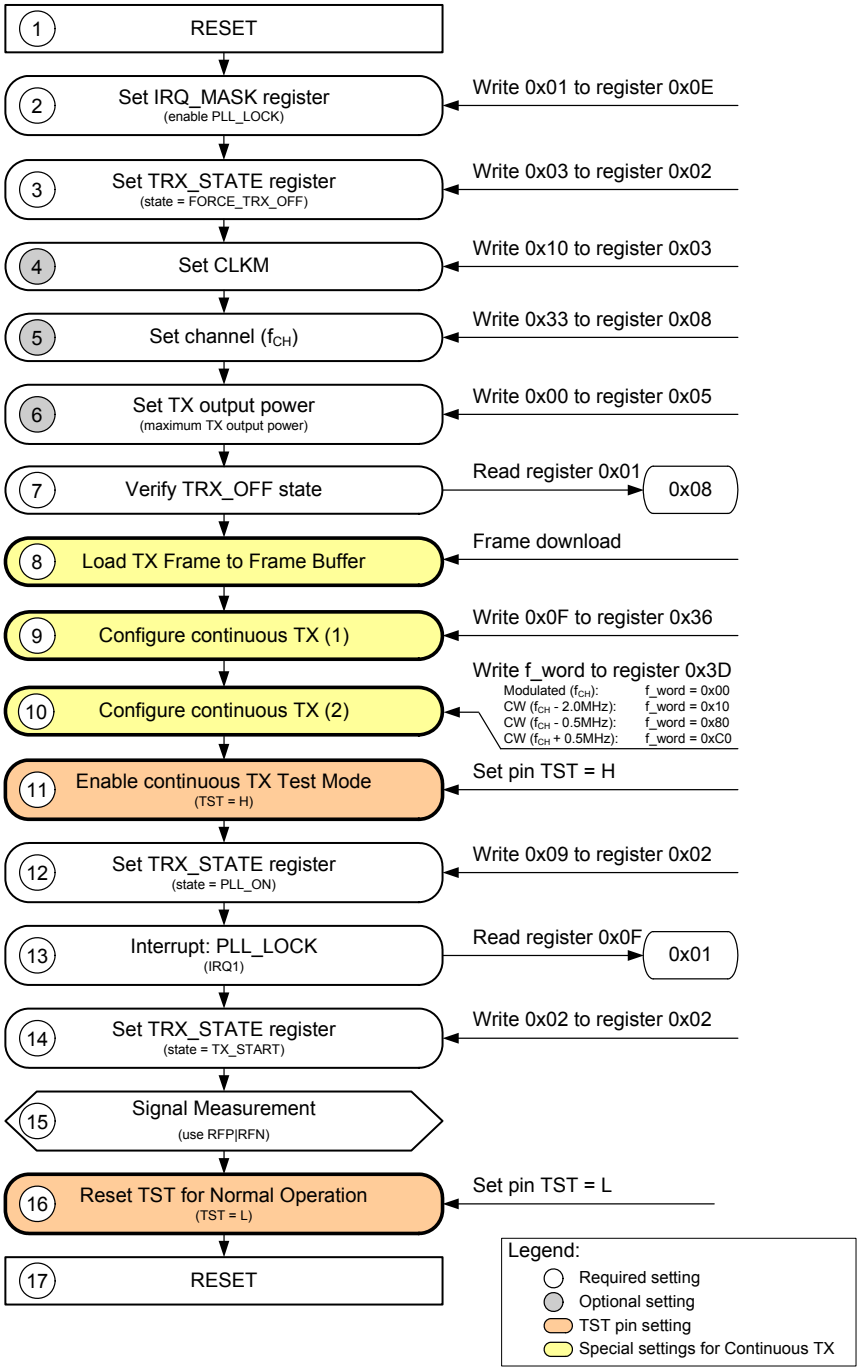
- Radio transceiver initialization (TRX_STATUS = TRX_OFF)
- TX channel selection (optional)
- TX output power setting (optional)
- Frame data download (random sequence of max. length)
- Mode selection (PRBS/CW)

Setting TST = 1 enables the Continuous Transmission Test Mode. The test system or a microcontroller has to overwrite the pull down resistor R1 connected to the TST pin (see Figure 5-1). The pull down resistor ensures a disabled test functionality during normal operation (TST = 0).

The transmission is started after enabling the PLL (TRX_CMD = PLL_ON) and writing the TX_START command to register 0x02.

The detailed programming sequence is shown in Figure A-1.

Figure A-1. Programming Sequence - Continuous Transmission



A.3 - Disclaimer

The functionality of the Continuous Transmit Mode is not characterized by Atmel and therefore not guaranteed.

The normal operation of the AT86RF230 is only guaranteed if pin TST is always logic low.

Appendix B - Errata

AT86RF230 Rev. B

No known errata.

AT86RF230 Rev. A

1. Data frames with destination address=0xFFFF is acknowledged in RX_AACK

According to IEEE 802.15.4-2003 data frames with destination address=0xFFFF (broadcast) should not have the acknowledgment request subfield set in the frame control field. If such a non-standard compliant data frame arrives, a device in RX_AACK state acknowledges that frame.

Fix/Workaround

Use only standard compliant frames, i.e. do not initiate frames with destination address=0xFFFF (broadcast) and the acknowledgment request subfield set.

2. Frame upload in RX_AACK

The following frames are not uploaded:

(1) Data frames and command frames with destination PAN ID=0xFFFF and extended destination addressing mode

(2) Beacon frames, when the PAN ID of the receiving node is set to 0xFFFF.

Fix/Workaround

(1) Use Basic Operating Mode for orphan scanning

(2) Use Basic Operating Mode for network scanning

3. TX_ARET returns TRAC_STATUS=SUCCESS even though transaction failed

It might happen that under very special conditions (e.g. noisy network environment) the status bit TRAC_STATUS (register 0x02) after transmission of a frame is SUCCESS even though the transaction failed.

Example

A node transmits a frame with the acknowledgment request subfield set to logic high and waits for an incoming ACK. If no frame is received at the end of the ACK wait period (54 symbols), but a valid preamble is detected (e.g. jammer/interferer signal), the TX_ARET procedure is finished immediately. A TRX_END interrupt is generated. The TRAC_STATUS is not updated and thus shows the default value SUCCESS.

Fix/Workaround

The workaround comprises two changes:

1. Set register bits MAX_FRAME_RETRIES to 0. This prevents any retransmissions in the TX_ARET procedure. The frame retransmission has to be implemented in S/W. A retransmission does not require a frame download again, only TX_START command is necessary.
2. Control of the TX_ARET procedure should follow these steps:
    - TRX_STATUS == TX_ARET_ON
    - set TRX_CMD = TX_START and download frame
    - poll for TRX_STATUS == BUSY_TX_ARET

- set TRX_CMD = RX_ON
- wait for TRX_END IRQ
- read TRAC_STATUS
- set TRX_CMD = TX_ARET_ON
- poll for TRX_STATUS == TX_ARET_ON

Switching to RX_ON is not executed during BUSY_TX_ARET but immediately after BUSY_TX_ARET has completed. This enables the receiver to receive a frame which arrives shortly before the end of the ACK wait period. In this case TRAC_STATUS is not accidentally set to SUCCESS and is still correct (NO_ACK), as long as the frame is received. That means the software has additional time to read the TRAC_STATUS.

Using the workaround mentioned above, the failure occurrence is considerably reduced. A wrong TRAC_STATUS can still be observed, but very seldom (one of million transmissions).

4. **Sensitivity to continuous wave interferers**

   Due to the high receiver sensitivity continuous wave interferers may cause RX_START interrupts. This may result in missed frames since the receiver is kept busy detecting preambles and SFD. One cause of continuous wave interferers may be due to crosstalk from clock.

   Fix/Workaround

   For further details see application note AVR2005 "Design Considerations for the AT86RF230".

5. **TRX_END_IRQ occurs sometimes too late in TX_ARET_ON state**

   This behavior can be observed, if the procedure TX_ARET performs frame retransmissions.

   Fix/Workaround

   Set register bit MAX_FRAME_RETRIES = 0 (register 0x2C) and implement frame retries by software. A frame retransmission does not require downloading the frame again, only TX_START command is necessary.

6. **TX_ARET ACK wait time too short**

   The maximum number of symbols waiting for an acknowledgment frame should be 54 symbols as defined in IEEE 802.15.4-2003. The implemented waiting time is 46 symbols.

   Fix/Workaround

   None

7. **CCA Request is not executed**

   A requested CCA may be rejected without execution. In this case the CCA_DONE bit indicates “CCA calculation in progress” even though the calculation must be finished already.

   Fix/Workaround

   The TRX_STATUS is RX_ON. To initiate a CCA request, switch to PLL_ON state and back to RX_ON state. Immediately after the state change initiate a CCA request. It is not necessary to confirm the state changes.

References

[1] IEEE Std 802.15.4-2003: Wireless Medium Access Control (MAC) and Physical Layer (PHY) Specifications for Low-Rate Wireless Personal Area Networks (LR-WPANs)

[2] ANSI / ESD-STM5.1-2001: ESD Association Standard Test Method for electrostatic discharge sensitivity testing – Human Body Model (HBM)

[3] ESD-STM5.3.1-1999: ESD Association Standard Test Method for electrostatic discharge sensitivity testing – Charged Device Model (CDM)

Data Sheet Revision History

Rev. 5131E-ZIGB-02/04/09

1. Removed PRELIMINARY statement
2. Updated parameter 11.4.4
3. Minor editorial changes

Rev. 5131D-ZIGB-12/03/07

The AT86RF230 data sheet was fully revised and modifications of silicon revision AT86RF230 Rev. B were incorporated. A migration note of silicon revision A to revision B is available on www.atmel.com.

The most important modifications are:

4. Device version number in register 0x1D (VERSION_NUM) changed to 2 (section 6.3)
5. SPI Interface: MISO pin is updated on falling edge at pin SCLK (section 6.1)
6. Extended Operating Mode state diagram: State changes towards RX_AACK_ON and TX_ARET_ON (Figure 7-5)
7. Enhanced return code of TX_ARET transaction in register bits TRAC_STATUS of register 0x02 (section 7.2.3.2)
8. FCS check of received frames in Basic Operating Mode (section 8.2)
9. Support of pending data indication in Extended Operating Mode (sections 7.2.3.1, 7.2.3.2)
10. Update package drawing (section 16)

Rev. 5131C-ZIGB-05/22/07

1. Major revise of sections 1 to 10
2. Added “Appendix A - Continuous Transmission Test Mode”
3. Added “Appendix B - Errata”

Rev. 5131A-ZIGB-06/14/06

1. Initial release

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