Features

- Fully Integrated 700/800/900 MHz-Band Transceiver
  - Chinese WPAN Band from 779 to 787 MHz
  - European SRD Band from 863 to 870 MHz
  - North American ISM Band from 902 to 928 MHz
- Direct Sequence Spread Spectrum with Different Modulation Schemes and Data Rates
  - BPSK with 20 and 40 kbit/s, compliant to IEEE 802.15.4-2003/2006
  - O-QPSK with 100 and 250 kbit/s, compliant to IEEE 802.15.4-2006
  - O-QPSK with 250 kbit/s, compliant to IEEE 802.15.4c-2009
  - O-QPSK with 200, 400, 500, and 1000 kbit/s PSDU Data Rate
- Flexible Combination of Frequency Bands and Data Rates
- Industry Leading Link Budget
  - Receiver Sensitivity up to -110 dBm
  - Programmable TX Output Power up to +10 dBm
- Low Power Supply Voltage from 1.8 V to 3.6 V
  - Internal Voltage Regulators and Battery Monitor
- Low Current Consumption
  - SLEEP = 0.2 µA
  - TRX_OFF = 0.4 mA
  - RX_ON = 9.2 mA
  - BUSY_TX = 17 mA at P_{TX} = 5 dBm
- Digital Interface
  - Registers, Frame Buffer, and AES Accessible through SPI
  - Clock Output with Configurable Rate
- Radio Transceiver Features
  - Adjustable Receiver Sensitivity
  - Integrated TX/RX Switch, LNA, and PLL Loop Filter
  - Fast Settling PLL Supporting Frequency Hopping
  - Automatic VCO and Filter Calibration
  - Integrated 16 MHz Crystal Oscillator
  - 128 byte FIFO for Transmit/Receive
- IEEE 802.15.4-2006 Hardware Support
  - FCS Computation and Check
  - Clear Channel Assessment
  - Received Signal Strength Indicator, Energy Detection, and Link Quality Indication
- MAC Hardware Accelerator
  - Automatic Acknowledgement and Retransmission
  - CSMA-CA and Listen before Talk
  - Automatic Frame Filtering
- AES 128 bit Hardware Accelerator (ECB and CBC modes)
- Extended Feature Set Hardware Support
  - True Random Number Generation for Security Applications
  - TX/RX Indication for External RF Front End Control
  - Configurable SFD
- Optimized for Low BoM Cost and Ease of Production
  - Low External Component Count: Antenna, Reference Crystal, and Bypass Capacitors
  - Excellent ESD Robustness
- Industrial Temperature Range from -40 °C to +85 °C
- 32-pin Low-profile Lead-free Plastic QFN Package, 5.0 x 5.0 x 0.9 mm^3
- Compliant to IEEE 802.15.4-2003, IEEE 802.15.4-2006, IEEE 802.15.4c-2009, ETSI EN 300 220-1, and FCC 47 CFR Section 15.247

AVR®

Low Power 700/800/900 MHz Transceiver for IEEE 802.15.4-2006, IEEE 802.15.4c-2009, Zigbee, 6LoWPAN, and ISM Applications

AT86RF212

8168C-MCU Wireless-02/10

1 Overview

The AT86RF212 is a low-power, low-voltage 700/800/900 MHz transceiver specially designed for the IEEE Standard 802.15.4, ZigBee, 6LoWPAN, and high data rate ISM applications. For the sub-1 GHz bands, it supports low data rates (20 and 40 kbit/s) of the IEEE Standard 802.15.4-2003/2006 [1, 2] and provides optional data rates (100 and 250 kbit/s) using O-QPSK, according to the IEEE Standard 802.15.4-2006 [1] and the respective IEEE 802.15.4c-2009 Amendment [3]. Furthermore, proprietary High Data Rate Modes up to 1000 kbit/s can be employed.

The AT86RF212 is a true SPI-to-antenna solution. RF-critical components except the antenna, crystal, and de-coupling capacitors are integrated on-chip. MAC and AES hardware accelerators improve overall system power efficiency and timing.

1.1 General Circuit Description

The AT86RF212 single-chip RF transceiver provides a complete radio interface between the antenna and the microcontroller. It comprises the analog radio part, digital modulation and demodulation, including time and frequency synchronization, as well as data buffering. A single 128 byte TRX buffer stores receive or transmit data. Communication between transmitter and receiver is based on direct sequence spread spectrum with different modulation schemes and spreading codes.

The number of external components is minimized so that only the antenna, a filter (at high output power levels), the crystal, and four bypass capacitors are required. The bidirectional differential antenna pins are used in common for RX and TX, i.e. no external antenna switch is needed. Control of an external power amplifier is supported by two digital control signals (differential operation).

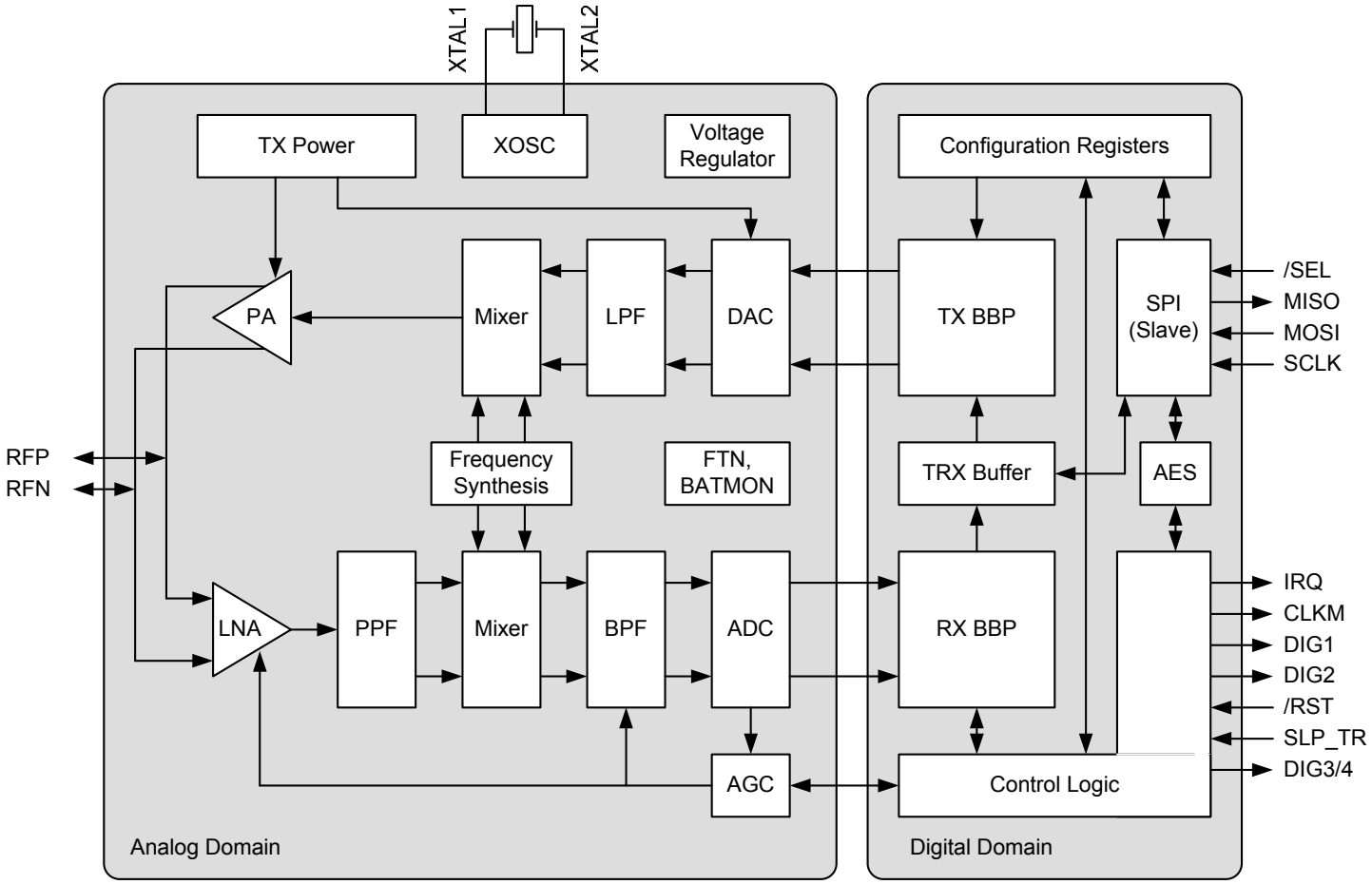
The AT86RF212 supports the IEEE 802.15.4-2006 standard mandatory BPSK modulation and optional O-QPSK modulation in the 868.3 MHz and 915 MHz bands. In addition, it supports the O-QPSK modulation defined in IEEE 802.15.4c-2009 for the Chinese 780 MHz band. For applications not necessarily targeting IEEE compliant networks, the radio transceiver supports proprietary High Data Rate Modes based on O-QPSK.

The AT86RF212 features hardware supported 128 bit security operation. The standalone AES encryption/decryption engine can be accessed in parallel to all PHY operational modes. Configuration of the AT86RF212, reading and writing of data memory, as well as the AES hardware engine are controlled by the SPI interface and additional control signals.

On-chip low-dropout voltage regulators provide the analog and digital 1.8 V power supply. Control registers retain their settings in sleep mode when the regulators are turned off. The RX and TX signal processing paths are highly integrated and optimized for low power consumption.

The transceiver block diagram is shown in Figure 1-1.

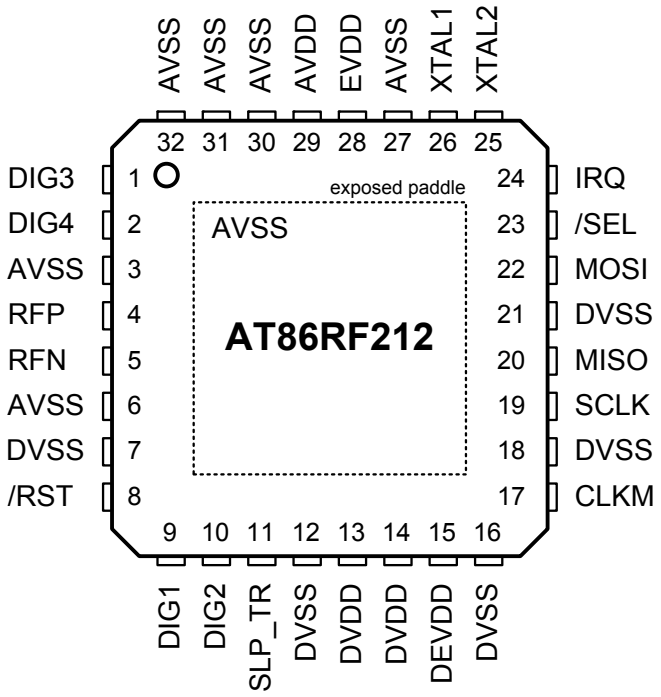
Figure 1-1. AT86RF212 Block Diagram



2 Pin Configuration

2.1 Pin-out Diagram

Figure 2-1. AT86RF212 Pin-out Diagram



Note: The exposed paddle is electrically connected to the die inside the package. It shall be soldered to the board to ensure electrical and thermal contact and good mechanical stability.

2.2 Pin Description

Table 2-1. Pin Description

Pin	Name	Type	Description
1	DIG3	Digital output	RX/TX Indication, see section 9.4; if disabled, internally pulled to AVSS
2	DIG4	Digital output	RX/TX Indication (inverted DIG3), see section 9.4; if disabled, internally pulled to AVSS
3	AVSS	Ground	Ground for RF signals
4	RFP	RF I/O	Differential RF signal
5	RFN	RF I/O	Differential RF signal
6	AVSS	Ground	Ground for RF signals
7	DVSS	Ground	Digital ground
8	/RST	Digital input	Chip reset; active low
9	DIG1	Digital output	General purpose signal, see section 9.3; if disabled, internally pulled to DVSS

Pin	Name	Type	Description
10	DIG2	Digital output	1. General purpose signal (inverted DIG1), see section 9.3 2. Signal IRQ_2 (RX_START) for RX Frame Time Stamping, see section 9.5 If disabled, internally pulled to DVSS
11	SLP_TR	Digital input	Controls sleep, transmit start, and receive states; active high; see section 4.6
12	DVSS	Ground	Digital ground
13	DVDD	Analog	Regulated 1.8 V internal supply voltage; digital domain; see section 7.5
14	DVDD	Analog	Regulated 1.8 V internal supply voltage; digital domain; see section 7.5
15	DEVDD	Supply	External supply voltage; digital domain
16	DVSS	Ground	Digital ground
17	CLKM	Digital output	Master clock signal output; low if disabled; see section 7.7
18	DVSS	Ground	Digital ground
19	SCLK	Digital input	SPI clock
20	MISO	Digital output	SPI data output (master input slave output)
21	DVSS	Ground	Digital ground
22	MOSI	Digital input	SPI data input (master output slave input)
23	/SEL	Digital input	SPI select; active low
24	IRQ	Digital output	1. Interrupt request signal; active high or active low; see section 4.7 2. Buffer-level mode indicator; active high
25	XTAL2	Analog	Crystal pin, see sections 2.2.1.3 and 7.7
26	XTAL1	Analog	Crystal pin or external clock supply, see sections 2.2.1.3 and 7.7
27	AVSS	Ground	Analog ground
28	EVDD	Supply	External supply voltage; analog domain
29	AVDD	Analog	Regulated 1.8 V internal supply voltage; analog domain; see section 7.5
30	AVSS	Ground	Analog ground
31	AVSS	Ground	Analog ground
32	AVSS	Ground	Analog ground
Paddle	AVSS	Ground	Analog ground; exposed paddle of QFN package

2.2.1 Analog and RF Pins

2.2.1.1 Supply and Ground Pins

EVDD, DEVDD

EVDD and DEVDD are analog and digital supply voltage pins of the AT86RF212 radio transceiver.

AVDD, DVDD

AVDD and DVDD are outputs of the internal voltage regulators and require bypass capacitors for stable operation. The voltage regulators are controlled independently by the radio transceivers state machine and are activated depending on the current radio transceiver state. The voltage regulators can be configured for external supply; for details, refer to section 7.5.

AVSS, DVSS

AVSS and DVSS are analog and digital ground pins respectively.

2.2.1.2 RF Pins

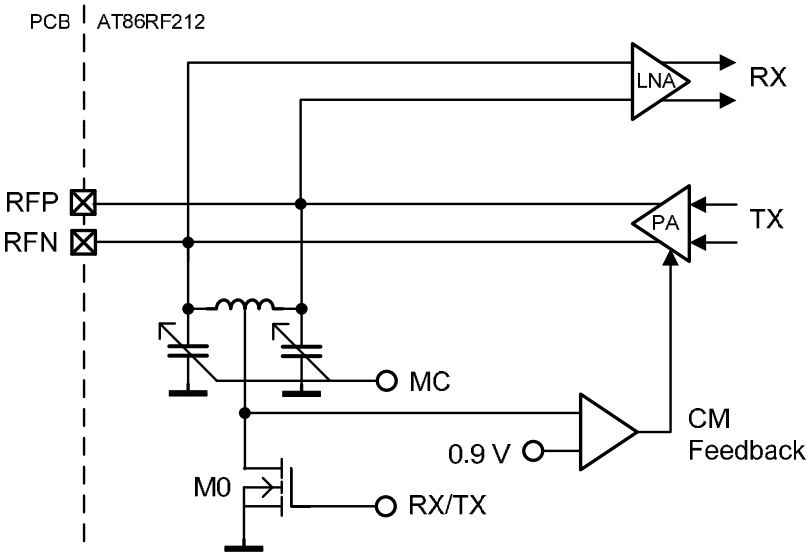
RFN, RFP

A differential RF port (RFP/RFN) provides common-mode rejection to suppress the switching noise of the internal digital signal processing blocks. At board-level, the differential RF layout ensures high receiver sensitivity by reducing spurious emissions originated from other digital ICs such as a microcontroller.

The RF port is designed for a 100 Ω differential load. A DC path between the RF pins is allowed. A DC path to ground or supply voltage is not allowed. Therefore, when connecting a RF-load providing a DC path to the power supply or ground, AC-coupling is required as indicated in Table 2-2.

A simplified schematic of the RF front end is shown in Figure 2-2.

Figure 2-2. Simplified RF Front-end Schematic



RF port DC values depend on the operating state; refer to section 5. In TRX_OFF state, when the analog front-end is disabled (see section 5.1.2.3), the RF pins are pulled to ground, preventing a floating voltage larger than 1.8 V which is not allowed for the internal circuitry.

In transmit mode, a control loop provides a common-mode voltage of 0.9 V. Transistor M0 is off, allowing the PA to set the common-mode voltage. The common-mode capacitance at each pin to ground shall be < 100 pF to ensure the stability of this common-mode feedback loop.

In receive mode, the RF port provides a low-impedance path to ground when transistor M0 (see Figure 2-2) pulls the inductor center tap to ground. A DC voltage drop of 20 mV across the on-chip inductor can be measured at the RF pins.

Matching control (MC) is implemented by an adjustable capacitance to ground at each RF pin as shown in Figure 2-2. The input capacitance can be changed within 15 steps by setting a 4-bit control word (register 0x19, RF_CTRL_1); refer to section 7.2.3.

2.2.1.3 Crystal Oscillator Pins

XTAL1, XTAL2

The pin XTAL1 is the input of the reference oscillator amplifier (XOSC), XTAL2 the output. A detailed description of the crystal oscillator setup and the related XTAL1/XTAL2 pin configuration can be found in section 7.7.

When using an external clock reference signal, XTAL1 shall be used as input pin. For further details, refer to section 7.7.3.

2.2.1.4 Analog Pin Summary

Table 2-2. Analog Pin Behavior – DC Values

Pin	Values and Conditions	Comments
RFP/RFN	V_{DC} = 0.9 V (BUSY_TX) V_{DC} = 20 mV (receive states) V_{DC} = 0 mV (otherwise)	DC level at pins RFP/RFN for various transceiver states AC-coupling is required if an antenna with a DC path to ground is used. Serial capacitance and capacitance of each pin to ground must be < 100 pF.
XTAL1/XTAL2	V_{DC} = 0.9 V at both pins C_{PAR} = 3 pF	DC level at pins XTAL1/XTAL2 for various transceiver states Parasitic capacitance (C_{PAR}) of the pins must be considered as additional load capacitance to the crystal.
DVDD	V_{DC} = 1.8 V (all states, except SLEEP) V_{DC} = 0 mV (otherwise)	DC level at pin DVDD for various transceiver states Supply pins (voltage regulator output) for the digital 1.8 V voltage domain. The outputs shall be bypassed by 1 µF.
AVDD	V_{DC} = 1.8 V (all states, except P_ON, SLEEP, RESET, and TRX_OFF) V_{DC} = 0 mV (otherwise)	DC level at pin AVDD for various transceiver states Supply pin (voltage regulator output) for the analog 1.8 V voltage domain. The outputs shall be bypassed by 1 µF.

2.2.2 Digital Pins

The AT86RF212 provides a digital microcontroller interface. The interface comprises a slave SPI (/SEL, SCLK, MOSI, and MISO) and additional control signals (CLKM, IRQ, SLP_TR, /RST, and DIG2). The microcontroller interface is described in detail in section 4.

Additional digital output signals DIG1 … DIG4 are provided to control external blocks, i.e. for Antenna Diversity RF switch control or as an RX/TX Indicator; see sections 9.3 and 9.4 respectively. After reset, these pins are connected to digital ground (DIG1/DIG2) or analog ground (DIG3/DIG4).

2.2.2.1 Driver Strength Settings

The driver strength of all digital output pins (MISO, IRQ, DIG1, … , DIG4) and CLKM pin can be configured using register 0x03 (TRX_CTRL_0); see Table 2-3.

Table 2-3. Digital Output Driver Configuration

Pin	Default Driver Strength	Comment
MISO, IRQ, DIG1, … , DIG4	2 mA	Adjustable to 2 mA, 4 mA, 6 mA, and 8 mA
CLKM	4 mA	Adjustable to 2 mA, 4 mA, 6 mA, and 8 mA

The capacitive load should be as small as possible and not larger than 50 pF when using the 2 mA minimum driver strength setting. Generally, the output driver strength should be adjusted to the lowest possible value in order to keep the current consumption and the emission of digital signal harmonics low.

2.2.2.2 Pull-up and Pull-down Configuration

Pulling resistors are internally connected to all digital input pins in radio transceiver state P_ON; see section 5.1.2.1. Table 2-4 summarizes the pull-up and pull-down configuration.

Table 2-4. Pull-up / Pull-Down Configuration of Digital Input Pins in P_ON State

Pin	H ≙ pull-up, L ≙ pull-down
/RST	H
/SEL	H
SCLK	L
MOSI	L
SLP_TR	L

In all other states, including RESET, no pull-up or pull-down resistors are connected to any of the digital input pins.

2.2.2.3 Register Description

Register 0x03 (TRX_CTRL_0):

The TRX_CTRL_0 register controls the driver current of the digital output pads and the CLKM clock rate.

Table 2-5. Register 0x03 (TRX_CTRL_0)

Bit	7	6	5	4
Name	PAD_IO[1]	PAD_IO[0]	PAD_IO_CLKM[1]	PAD_IO_CLKM[0]
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	0	1
Bit	3	2	1	0
Name	CLKM_SHA_SEL	CLKM_CTRL	CLKM_CTRL	CLKM_CTRL
Read/Write	R/W	R/W	R/W	R/W
Reset Value	1	0	0	1

- **Bit 7:6 – PAD_IO**

These register bits set the output driver current of digital output pads, except CLKM.

Table 2-6. Digital Output Driver Strength

Register Bits	Value	Description
PAD_IO	0 (1)	2 mA
	1	4 mA
	2	6 mA
	3	8 mA

Note: 1. Throughout this data sheet, underlined values indicate reset settings.

- **Bit 5:4 – PAD_IO_CLKM**

These register bits set the output driver current of pin CLKM. Refer also to section 7.7.

Table 2-7. CLKM Driver Strength

Register Bits	Value	Description
PAD_IO_CLKM	0	2 mA
	1	4 mA
	2	6 mA
	3	8 mA

- **Bit 3:0 – CLKM_SHA_SEL, CLKM_CTRL**

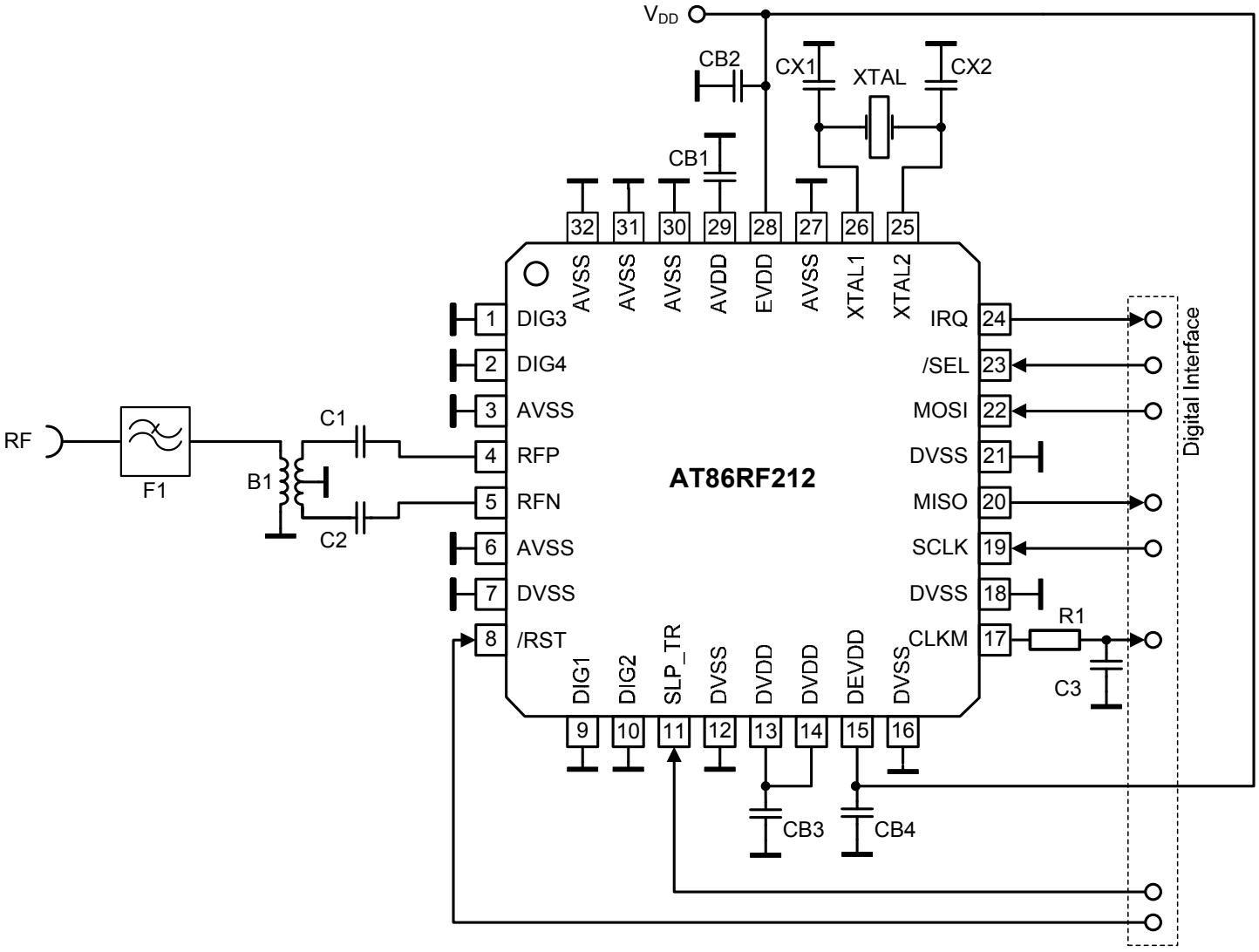
Refer to section 7.7.6.

3 Application Schematic

3.1 Basic Application Schematic

A basic application schematic of the AT86RF212 with a single-ended RF connector is shown in Figure 3-1. The 50 Ω single-ended RF input is transformed to the 100 Ω differential RF port impedance using balun B1. The capacitors C1 and C2 provide AC coupling of the RF input to the RF port. Regulatory rules like FCC 47 CFR section 15.247 [4], ETSI EN 300 220-1 [5], and ERC/REC 70-03 [6] may require an external filter F1, depending on used transmit power levels.

Figure 3-1. Basic Application Schematic



The power supply bypass capacitors (CB2, CB4) are connected to the external analog supply pin (EVDD, pin 28) and external digital supply pin (DEVDD, pin 15). Capacitors CB1 and CB3 are bypass capacitors for the integrated analog and digital voltage regulators to ensure stable operation. All bypass capacitors should be placed as close

as possible to the pins and should have a low-resistance and low-inductance connection to ground to achieve the best performance.

The crystal (XTAL), the two load capacitors (CX1, CX2), and the internal circuitry connected to pins XTAL1 and XTAL2 form the crystal oscillator. To achieve the best accuracy and stability of the reference frequency, large parasitic capacitances should be avoided. Crystal lines should be routed as short as possible and not in proximity of digital I/O signals. This is especially required for the High Data Rate Modes; refer to section 7.1.4.

Crosstalk from digital signals to the crystal pins or the RF pins can degrade the system performance. Therefore, a low-pass filter (C3, R1) is placed close to the CLKM output pin to reduce the emission of CLKM signal harmonics. This is not needed if the CLKM pin is not used as a microcontroller clock source. In that case, the output should be turned off during device initialization.

The ground plane of the application board should be separated into four independent fragments: the analog, the digital, the antenna, and the XTAL ground plane. The exposed paddle shall act as the reference point of the individual grounds.

Please note that pins DIG1, DIG2, DIG3, and DIG4 are connected to ground in the Basic Application Schematic; refer to Figure 3-1. Special programming of these pins requires a different schematic; refer to section 3.2.

Table 3-1. Exemplary Bill of Materials (BoM) for Basic Application Schematic

Symbol	Description	Value	Manufacturer	Part Number	Comment
B1	SMD balun	800 – 1000 MHz	Wuerth JTI	748431090 0900BL18B100	
F1	SMD low pass filter	902 – 928 MHz	Wuerth JTI	748131009 0915LP15A026	
B1 + F1	Balun/Filter combination	863 – 928 MHz	JTI	0896FB15A0100	
		779 – 787 MHz	JTI	0783FB15A0100	
CB1, CB3	LDO VREG bypass capacitor	1 µF	AVX Murata	0603YD105KAT2A GRM188R61C105KA12D	X5R 10% 16 V (0603)
CB2, CB4	Power supply bypass capacitor	1 µF			
CX1, CX2	Crystal load capacitor	12 pF	AVX Murata	06035A120JA GRP1886C1H120JA01	COG 5% 50 V (0603)
C1, C2	RF coupling capacitor	68 pF	Epcos Epcos AVX	B37930 B37920 06035A680JAT2A	COG 5% 50 V (0402 or 0603)
C3	CLKM low-pass filter capacitor	2.2 pF	AVX Murata	06035A229DA GRP1886C1H2R0DA01	COG ±0.5 pF 50 V (0603) Designed for f_{CLKM} = 1 MHz
R1	CLKM low-pass filter resistor	680 Ω			Designed for f_{CLKM} = 1 MHz
XTAL	Crystal	CX-4025 16 MHz SX-4025 16 MHz	ACAL Taitien Siward	XWBBPL-F-1 A207-011	

3.2 Extended Feature Set Application Schematic

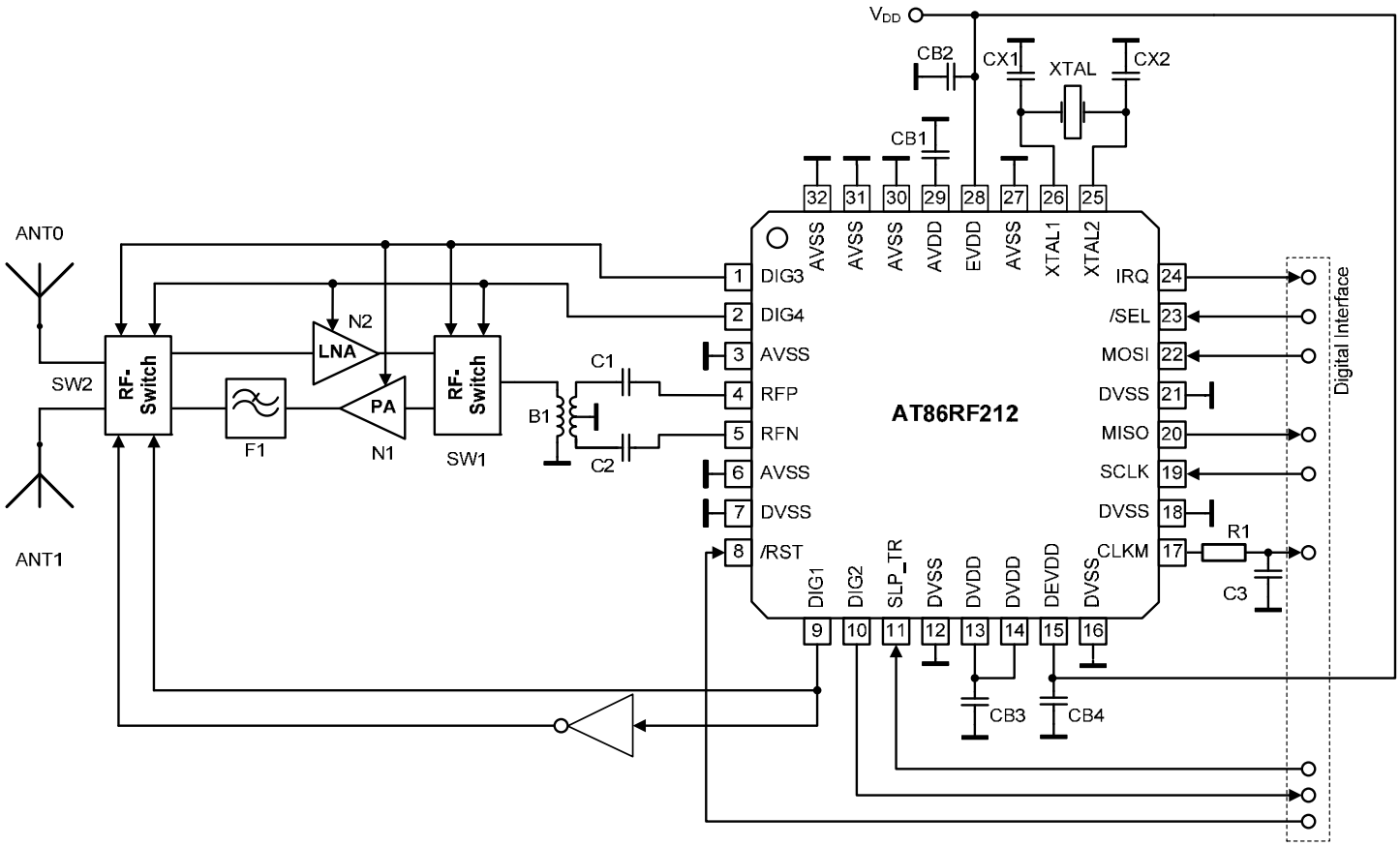
For using the extended features

- Antenna Diversity uses pins DIG1/DIG2 (1) section 9.3
- RX/TX Indicator uses pins DIG3/DIG4 section 9.4
- RX Frame Time Stamping uses pin DIG2 section 9.5

an extended application schematic is required. All other extended features (see section 9) do not need an extended schematic.

An application schematic illustrating the use of the AT86RF212 Extended Feature Set is shown in Figure 3-2. Although this example shows all additional hardware features combined, it is possible to use all features separately or in various combinations.

Figure 3-2. Extended Feature Set Application Schematic



In this example, a balun (B1) transforms the differential radio transceiver RF pins (RFP/RFN) to a single ended RF signal, similar to the Basic Application Schematic; refer to Figure 3-1. The RF switches (SW1, SW2) separate between receive and transmit path in an external RF front-end. These switches are controlled by the RX/TX Indicator, represented by the differential pin pair DIG3/DIG4; refer to section 9.4.

During receive, the corresponding microcontroller may search for the most reliable RF signal path using an Antenna Diversity algorithm or stored statistic data of link signal quality. One antenna is selected by a RF switch (SW2) controlled by pin DIG1 (1). The RF signal is amplified by an optional low-noise amplifier (N2) and fed to the radio transceiver using a RX/TX switch (SW1).

During transmit, the AT86RF212 TX signal is amplified using an external PA (N1), low pass filtered to suppress spurious harmonics emission, and fed to the antennas via a RF switch (SW2). In this example, RF switch SW2 further supports Antenna Diversity controlled by pin DIG1 [1].

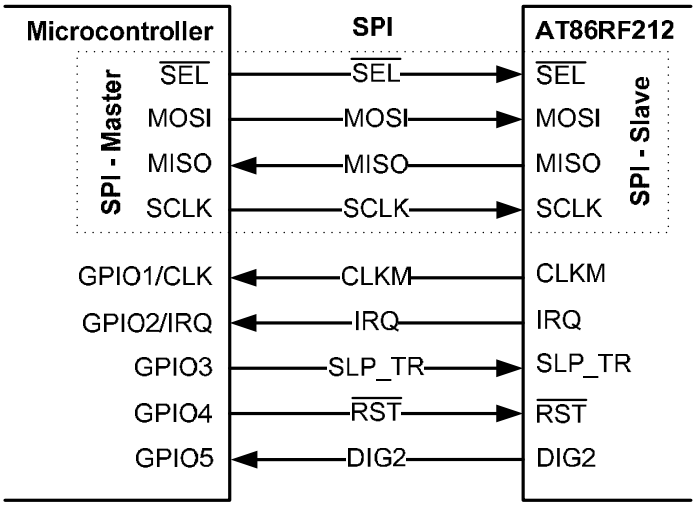
Note: 1. DIG1/DIG2 can be used as a differential pin pair to control a RF switch if RX Frame Time Stamping is not used; refer to sections 9.3 and 9.5.

4 Microcontroller Interface

4.1 Overview

This section describes the AT86RF212 to microcontroller interface. The interface comprises a slave SPI and additional control signals; see Figure 4-1. The SPI timing and protocol are described below.

Figure 4-1. Microcontroller to AT86RF212 Interface



Microcontrollers with a master SPI such as Atmel's AVR family interface directly to the AT86RF212. The SPI is used for register, Frame Buffer, SRAM, and AES access. The additional control signals are connected to the GPIO/IRQ interface of the microcontroller. Table 4-1 introduces the radio transceiver I/O signals.

Table 4-1. Signal Description of Microcontroller Interface

Signal	Description
/SEL	SPI select signal, active low
MOSI	SPI data (Master Output, Slave Input) signal
MISO	SPI data (Master Input, Slave Output) signal
SCLK	SPI clock signal
CLKM	Clock output (refer to section 7.7.4), usable as - microcontroller clock source - high precision timing reference - MAC timer reference.
IRQ	Interrupt request signal, further used as - Frame Buffer Empty indicator; refer to section 9.6.
SLP_TR	Multi purpose control signal (refer to section 4.6): - Sleep/Wakeup - TX start - disable/enable CLKM
/RST	AT86RF212 reset signal; active low
DIG2	Multi purpose control signal, amongst others to signal the reception of a frame; refer to section 9.5.

4.2 SPI Timing Description

Pin 17 (CLKM) can be used as a microcontroller master clock source. If the microcontroller derives the SPI master clock (SCLK) directly from CLKM, the SPI operates in synchronous mode, otherwise in asynchronous mode.

In synchronous mode, the maximum SCLK frequency is 8 MHz.

In asynchronous mode, the maximum SCLK frequency is limited to 7.5 MHz. The signal at pin CLKM is not required to derive SCLK and may be disabled to reduce power consumption and spurious emissions.

Figure 4-2 and Figure 4-3 illustrate the SPI timing and introduces its parameters. The corresponding timing parameter definitions t_1 – t_9 are defined in section 10.4.

Figure 4-2. SPI Timing: Global Map and Definition of Timing Parameters t_5, t_6, t_8, and t_9

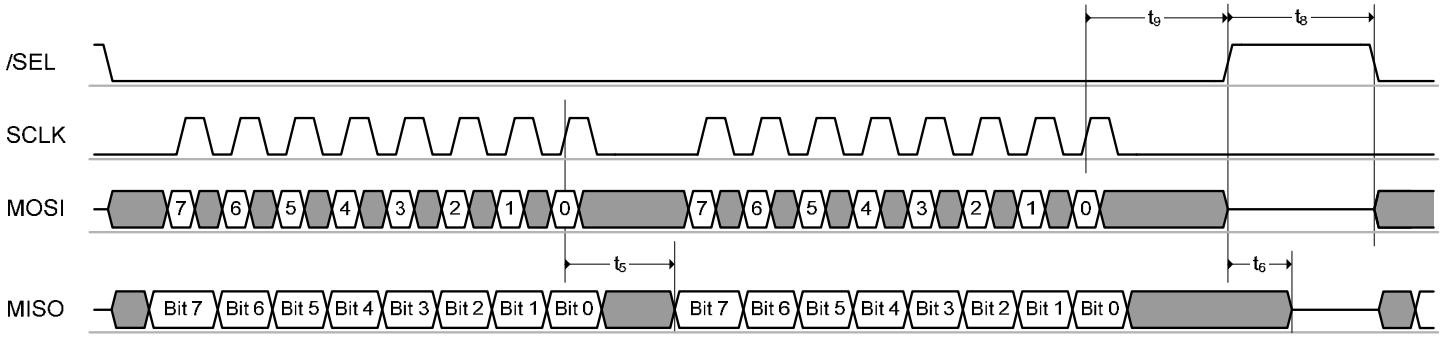
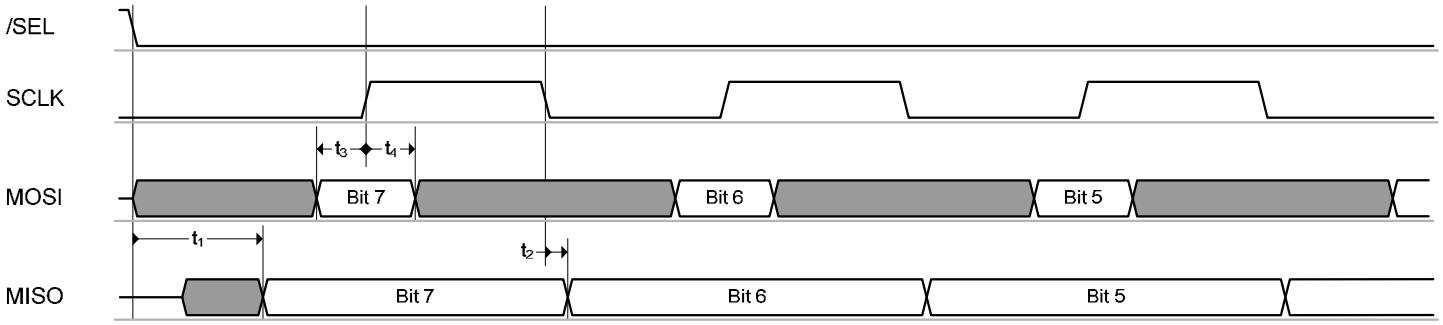


Figure 4-3. SPI Timing: Detailed Drawing of Timing Parameter t_1, t_2, t_3, and t_4



The SPI is based on a byte-oriented protocol and is always a bidirectional communication between master and slave. The SPI master starts the transfer by asserting /SEL = L. Then the master generates eight SPI clock cycles to transfer one byte to the radio transceiver (via MOSI). At the same time, the slave transmits one byte to the master (via MISO). When the master wants to receive one byte of data from the slave, it must also transmit one byte to the slave. All bytes are transferred with MSB first. An SPI transaction is finished by releasing /SEL = H.

/SEL = L enables the MISO output driver of the AT86RF212. The MSB of MISO is valid after t_1 (see section 10.4, parameter 10.4.3) and is updated at each falling edge of SCLK. If the driver is disabled, there is no internal pull-up resistor connected to it. Driving the appropriate signal level must be ensured by the master device or an external pull-up resistor. Note, when both /SEL and /RST are active, the MISO output driver is also enabled.

Referring to Figure 4-2 and Figure 4-3, MOSI is sampled at the rising edge of the SCLK signal and the output is set at the falling edge of SCLK. The signal must be stable before and after the rising edge of SCLK as specified by t_3 and t_4; refer to section 10.4, parameters 10.4.5 and 10.4.6.

This SPI operational mode is commonly known as “SPI mode 0”.

4.3 SPI Protocol

Each SPI sequence starts with transferring a command byte from the SPI master via MOSI (see Table 4-2) with MSB first. This command byte defines the SPI access mode and additional mode-dependent information.

Table 4-2. SPI Command Byte Definition

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access Mode	Access Type
1	0	Register address [5:0]						Register access	Read access
1	1	Register address [5:0]							Write access
0	0	1	Reserved					Frame Buffer access	Read access
0	1	1	Reserved						Write access
0	0	0	Reserved					SRAM access	Read access
0	1	0	Reserved						Write access

Each SPI transfer returns bytes back to the SPI master on MISO. The content of the first byte is the *PHY_STATUS* field, see section 4.4.

In Figure 4-4 to Figure 4-14 and the following sections, logic values stated with XX on MOSI are ignored by the radio transceiver but need to have a valid logic level. Return values on MISO stated as XX shall be ignored by the microcontroller.

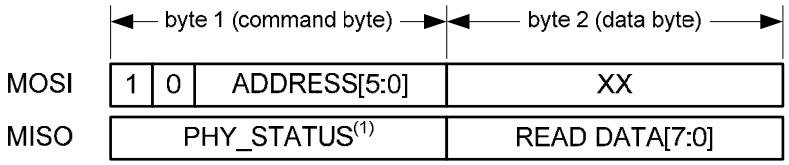
The different access modes are described within the following sections.

4.3.1 Register Access Mode

A register access mode is a two-byte read/write operation initiated by /SEL = L. The first transferred byte on MOSI is the command byte, including an identifier bit (bit7 = 1), a read/write select bit (bit 6), and a 6-bit register address.

On read access, the content of the selected register address is returned in the second byte on MISO (see Figure 4-4).

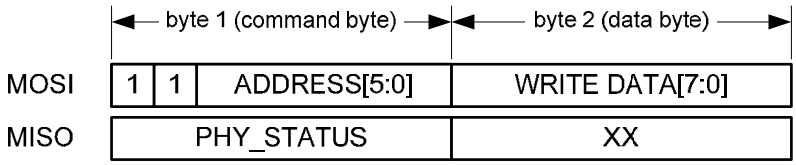
Figure 4-4. Register Access Mode – Read Access



Note: 1. Each SPI access can be configured to return PHY status information (*PHY_STATUS*) on MISO, refer to section 4.4.

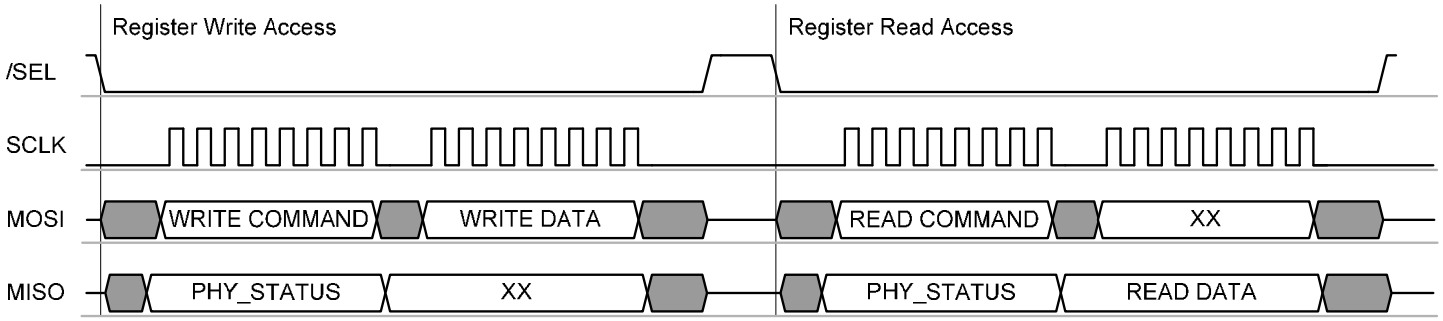
On write access, the second byte transferred on MOSI contains the write data to the selected address (see Figure 4-5).

Figure 4-5. Register Access Mode – Write Access



Each register access must be terminated by setting /SEL = H. Figure 4-6 illustrates a typical SPI sequence for a register write and read access.

Figure 4-6. Exemplary SPI Sequence – Register Access Mode



4.3.2 Frame Buffer Access Mode

The 128 byte Frame Buffer can hold the PHY service data unit (PSDU) data of one IEEE 802.15.4 compliant RX or TX frame of maximum length at a time. A detailed description of the Frame Buffer can be found in section 7.4. An introduction to the IEEE 802.15.4 frame format can be found in section 6.1.

Frame Buffer read and write accesses are used to read or write frame data (PSDU and additional information) from or to the Frame Buffer. Each access starts with /SEL = L followed by a command byte on MOSI. If this byte indicates a frame read or write access, the next byte (PHR) indicates the frame length followed by the PSDU data, see Figure 4-7 and Figure 4-8.

On Frame Buffer read access, PHY header (PHR) and PSDU are transferred via MISO starting with the second byte. After the PSDU data, three more bytes are transferred containing the link quality indication (LQI) value, the energy detection (ED) value, and the status information (RX_STATUS) of the received frame. Figure 4-7 illustrates the packet structure of a Frame Buffer read access. The structure of RX_STATUS is described in Table 4-3.

Figure 4-7. Packet Structure - Frame Read Access

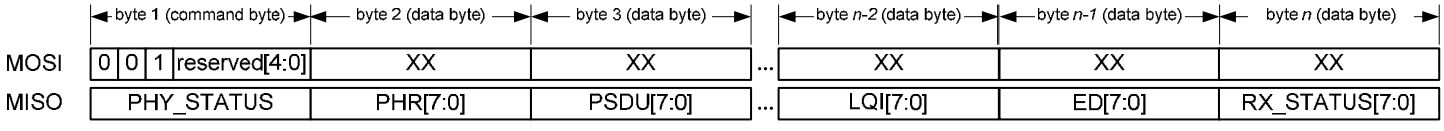


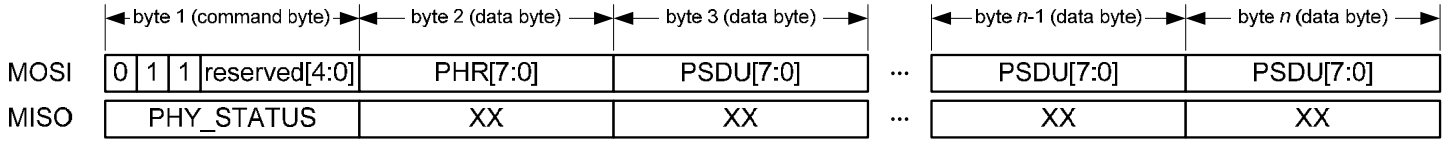
Table 4-3. RX_STATUS

Bit	7	6	5	4	3 … 0
Content	RX_CRC_VALID (register 0x06, PHY_RSSI)	TRAC_STATUS (register 0x02, TRX_STATE)			Reserved
Reference	Section 6.3.5	Section 5.2.6			

Note, the Frame Buffer read access can be terminated at any time without any consequences by setting /SEL = H, e.g. after reading the frame length byte only. A successive Frame Buffer read operation starts again at the PHR field.

On Frame Buffer write access, the second byte transferred on MOSI contains the frame length (PHR field) followed by the payload data (PSDU) as shown in Figure 4-8.

Figure 4-8. Packet Structure - Frame Write Access



The number of bytes *n* for one frame buffer access is calculated as follows:

Read Access: *n* = 5 + *frame_length*

[PHY_STATUS, PHR, PSDU data, LQI, ED, and RX_STATUS]

Write Access: *n* = 2 + *frame_length*

[command byte, PHR, and PSDU data]

The maximum value of *frame_length* is 127 bytes. That means that *n* ≤ 132 for Frame Buffer read and *n* ≤ 129 for Frame Buffer write accesses.

Each read or write of a data byte automatically increments the address counter of the Frame Buffer until the access is terminated by setting /SEL = H.

Figure 4-9 and Figure 4-10 illustrate an exemplary SPI sequence of a Frame Buffer access to read a frame with 2-byte PSDU and write a frame with 4-byte PSDU.

Figure 4-9. Exemplary SPI Sequence - Frame Buffer Read of a Frame with 2-byte PSDU

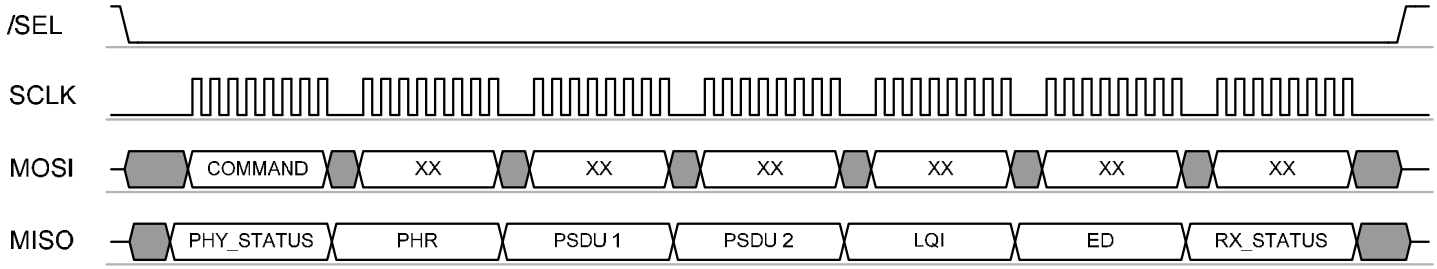
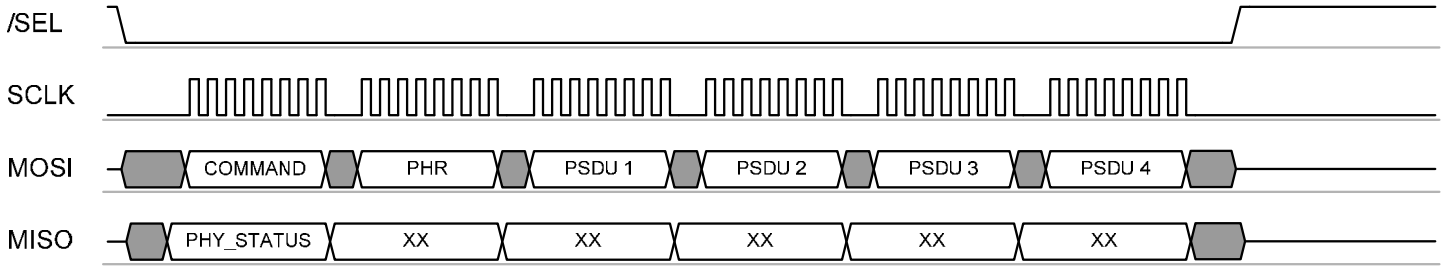


Figure 4-10. Exemplary SPI Sequence - Frame Buffer Write of a Frame with 4-byte PSDU



Access violations during a Frame Buffer read or write access are indicated by interrupt IRQ_6 (TRX_UR). For further details, refer to section 7.4.

Notes

- The Frame Buffer is shared between RX and TX; therefore, the frame data are overwritten by new incoming frames. If the TX frame data are to be retransmitted, it must be ensured that no frame was received in the meanwhile.
- To avoid overwriting during receive, Dynamic Frame Buffer Protection can be enabled; refer to section 9.7.
- For exceptions, e.g. receiving acknowledgement frames in Extended Operating Mode (TX_ARET), refer to section 5.2.4.

4.3.3 SRAM Access Mode

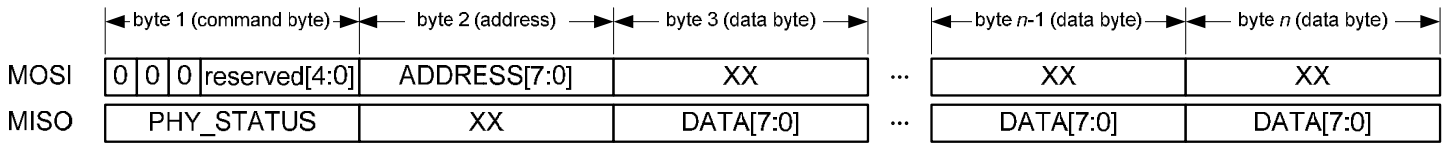
The SRAM access mode allows accessing dedicated bytes within the Frame Buffer. This may reduce the SPI traffic.

During frame receive, after occurrence of IRQ_2 (RX_START), a SRAM access can be used to upload the PHR field while preserving Dynamic Frame Buffer Protection, see section 9.7.

Each SRAM access starts with /SEL = L. The first transferred byte on MOSI shall be the command byte and must indicate an SRAM access mode according to the definition in Table 4-2. The following byte indicates the start address of the write or read access. The address space is 0x00 to 0x7F for radio transceiver receive or transmit operations. The security module (AES) uses an address space from 0x82 to 0x94; refer to section 9.1.

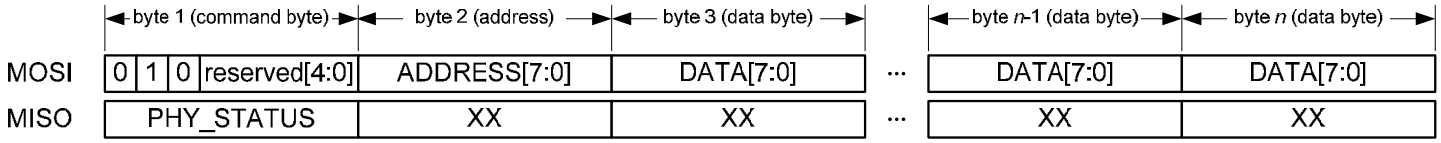
On SRAM read access, one or more bytes of read data are transferred on MISO starting with the third byte of the access sequence; refer to Figure 4-11.

Figure 4-11. Packet Structure – SRAM Read Access



On SRAM write access, one or more bytes of write data are transferred on MOSI starting with the third byte of the access sequence; refer to Figure 4-12. Do not attempt to read or write bytes beyond the SRAM buffer size.

Figure 4-12. Packet Structure – SRAM Write Access



As long as /SEL = L, every subsequent byte read or byte write increments the address counter of the Frame Buffer until the SRAM access is terminated by /SEL = H.

Figure 4-13 and Figure 4-14 illustrate an exemplary SPI sequence of a SRAM access to read and write a data package of 5-byte length, respectively.

Figure 4-13. Exemplary SPI Sequence – SRAM Read Access of a 5-byte Data Package

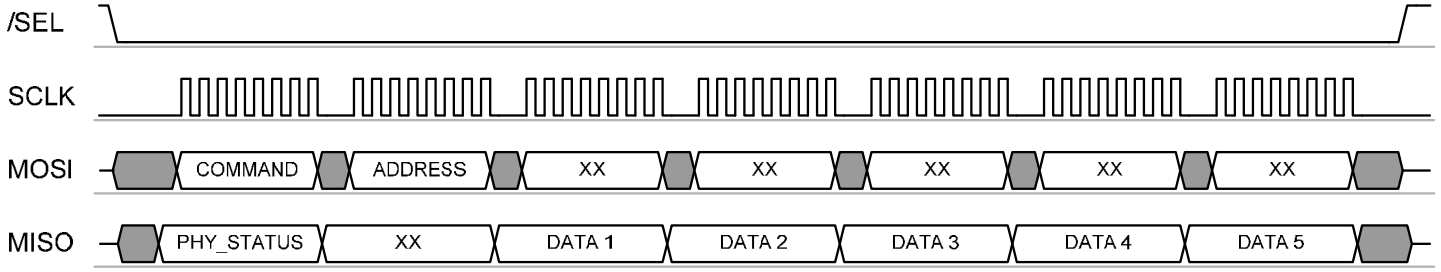
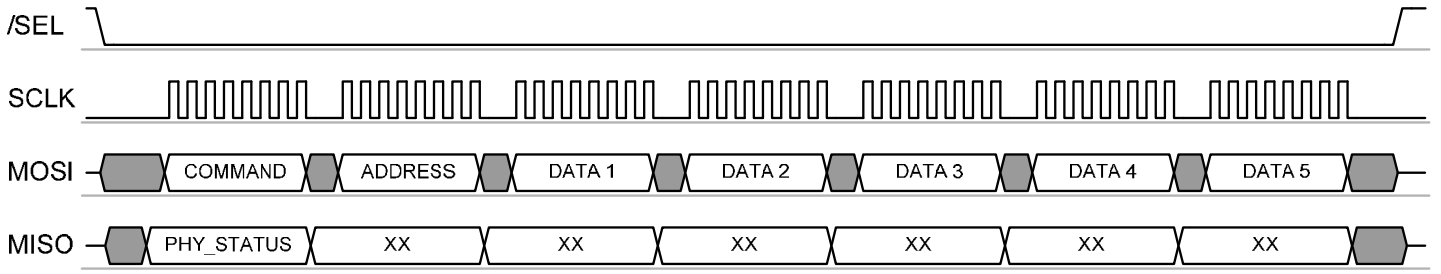


Figure 4-14. Exemplary SPI Sequence – SRAM Write Access of a 5-byte Data Package



Notes

- The SRAM access mode is not intended to be used as an alternative to the Frame Buffer access modes; refer to section 4.3.2.
- Frame Buffer access violations are not indicated by a TRX_UR interrupt when using the SRAM access mode; for further details refer to section 7.4.3.

4.4 PHY Status Information

Each SPI access can be configured to return status information of the radio transceiver (PHY_STATUS) to the microcontroller using the first byte of the data transferred via MISO.

The content of the radio transceiver status information can be configured using register bits SPI_CMD_MODE (register 0x04, TRX_CTRL_1). After reset, the content on the first byte send on MISO to the microcontroller is set to 0x00.

4.4.1 Register Description – SPI Control

Register 0x04 (TRX_CTRL_1):

The TRX_CTRL_1 register is a multi purpose register to control various operating modes and settings of the radio transceiver.

Table 4-4. Register 0x04 (TRX_CTRL_1)

Bit	7	6	5	4
Name	PA_EXT_EN	IRQ_2_EXT_EN	TX_AUTO_CRC_ON	RX_BL_CTRL
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	1	0
Bit	3	2	1	0
Name	SPI_CMD_MODE	SPI_CMD_MODE	IRQ_MASK_MODE	IRQ_POLARITY
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0

- **Bit 7 – PA_EXT_EN**

Refer to section 9.4.3.

- **Bit 6 – IRQ_2_EXT_EN**

Refer to section 9.5.2.

- **Bit 5 – TX_AUTO_CRC_ON**

Refer to section 6.3.5.

- **Bit 4 – RX_BL_CTRL**

Refer to section 9.6.2.

- **Bit 3:2 – SPI_CMD_MODE**

Each SPI transfer returns bytes back to the SPI master. The content of the first byte can be configured using register bits SPI_CMD_MODE.

Table 4-5. PHY Status Information

Register Bits	Value	Description
SPI_CMD_MODE	0	First byte = 0x00
	1	Monitor TRX_STATUS register, see section 5.1.5
	2	Monitor PHY_RSSI register, see section 6.4.4
	3	Monitor IRQ_STATUS register, see section 4.7.2 Interrupts are not cleared.

- **Bit 1:0 – IRQ_MASK_MODE, IRQ_POLARITY**

Refer to section 4.7.2.

4.5 Radio Transceiver Identification

The AT86RF212 can be identified by four registers. One register contains a unique part number and one register the corresponding version number. Additional two registers contain the JEDEC manufacture ID.

4.5.1 Register Description

Register 0x1C (PART_NUM):

Table 4-6. Register 0x1C (PART_NUM)

Bit	7	6	5	4	3	2	1	0
Name	PART_NUM[7:0]							
Read/Write	R							
Reset Value	0	0	0	0	0	1	1	1

- **Bit 7:0 – PART_NUM**

This register contains the radio transceiver part number.

Table 4-7. Radio Transceiver Part Number

Register Bits	Value	Description
PART_NUM	7	AT86RF212 part number

Register 0x1D (VERSION_NUM):

Table 4-8. Register 0x1D (VERSION_NUM)

Bit	7	6	5	4	3	2	1	0
Name	VERSION_NUM[7:0]							
Read/Write	R							

- **Bit 7:0 – VERSION_NUM**

This register contains the radio transceiver version number.

Table 4-9. Radio Transceiver Version Number

Register Bits	Value	Description
VERSION_NUM	1	Revision A

Register 0x1E (MAN_ID_0):

Table 4-10. Register 0x1E (MAN_ID_0)

Bit	7	6	5	4	3	2	1	0
Name	MAN_ID_0[7:0]							
Read/Write	R							
Reset Value	0	0	0	1	1	1	1	1

- **Bit 7:0 – MAN_ID_0**

Bits [7:0] of the 32-bit JEDEC manufacturer ID are stored in register bits MAN_ID_0. Bits [15:8] are stored in register 0x1F (MAN_ID_1). The highest 16 bits of the ID are not stored in registers.

Table 4-11. JEDEC Manufacturer ID – Bits [7:0]

Register Bits	Value	Description
MAN_ID_0	0x1F	Atmel JEDEC manufacturer ID, Bits [7:0] of 32-bit manufacturer ID: 00 00 00 1F

Register 0x1F (MAN_ID_1):

Table 4-12. Register 0x1F (MAN_ID_1)

Bit	7	6	5	4	3	2	1	0
Name	MAN_ID_1[7:0]							
Read/Write	R							
Reset Value	0	0	0	0	0	0	0	0

- **Bit 7:0 – MAN_ID_1**

Bits [15:8] of the 32-bit JEDEC manufacturer ID are stored in register bits MAN_ID_1. Bits [7:0] are stored in register 0x1E (MAN_ID_0). The higher 16 bits of the ID are not stored in registers.

Table 4-13. JEDEC Manufacturer ID – Bits [15:8]

Register Bits	Value	Description
MAN_ID_1	0x00	Atmel JEDEC manufacturer ID Bits [15:8] of 32-bit manufacturer ID: 00 00 00 1F

4.6 Sleep/Wake-up and Transmit Signal (SLP_TR)

Pin 11 (SLP_TR) is a multi-functional pin. Its function relates to the current state of the AT86RF212 and is summarized in Table 4-14. The radio transceiver states are explained in detail in section 5.

In states PLL_ON and TX_ARET_ON, pin SLP_TR is used as trigger input to initiate a TX transaction. Here pin SLP_TR is sensitive on rising edge only.

After initiating a state change by a rising edge at pin SLP_TR in radio transceiver states TRX_OFF, RX_ON or RX_AACK_ON, the radio transceiver remains in the new state as long as the pin is logical high and returns to the preceding state with the falling edge.

Table 4-14. SLP_TR Multi-functional Pin

Transceiver Status	Function	Transition	Description
PLL_ON	TX start	L → H	Starts frame transmission
TX_ARET_ON	TX start	L → H	Starts TX_ARET transaction
BUSY_RX_AACK	TX start	L → H	Starts ACK transmission during RX_AACK slotted operation, see section 5.2.3.5.
TRX_OFF	Sleep	L → H	Takes the radio transceiver into SLEEP state; CLKM disabled
SLEEP	Wakeup	H → L	Takes the radio transceiver back into TRX_OFF state; level sensitive
RX_ON	Disable CLKM	L → H	Takes the radio transceiver into RX_ON_NOCLK state and disables CLKM
RX_ON_NOCLK	Enable CLKM	H → L	Takes the radio transceiver into RX_ON state and enables CLKM
RX_AACK_ON	Disable CLKM	L → H	Takes the radio transceiver into RX_AACK_ON_NOCLK state and disables CLKM
RX_AACK_ON_NOCLK	Enable CLKM	H → L	Takes the radio transceiver into RX_AACK_ON state and enables CLKM

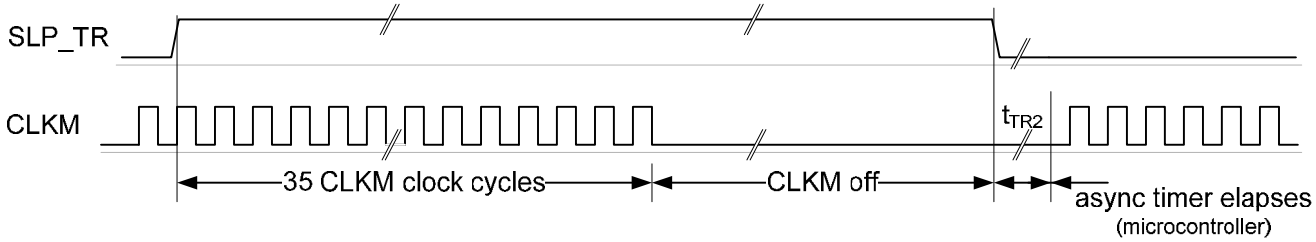
SLEEP state

The SLEEP state is used when radio transceiver functionality is not required, and thus the AT86RF212 can be powered down to reduce the overall power consumption.

A power-down scenario is shown in Figure 4-15. When the radio transceiver is in TRX_OFF state, the microcontroller forces the AT86RF212 to SLEEP by setting SLP_TR = H. If pin 17 (CLKM) provides a clock to the microcontroller, this clock is switched off after 35 clock cycles. This enables a microcontroller in a synchronous system to complete its power-down routine and prevent deadlock situations. The AT86RF212 awakes when the microcontroller releases pin SLP_TR. This concept provides the lowest possible power consumption.

The CLKM clock frequency settings for CLKM_CTRL values 6 and 7 are not intended to directly clock the microcontroller. When using these clock rates, CLKM is turned off immediately when entering SLEEP state.

Figure 4-15. Sleep and Wake-up Initiated by Asynchronous Microcontroller Timer



Note: Timing figure t_{TR2} refers to Table 5-1.

RX_ON and RX_AACK_ON states

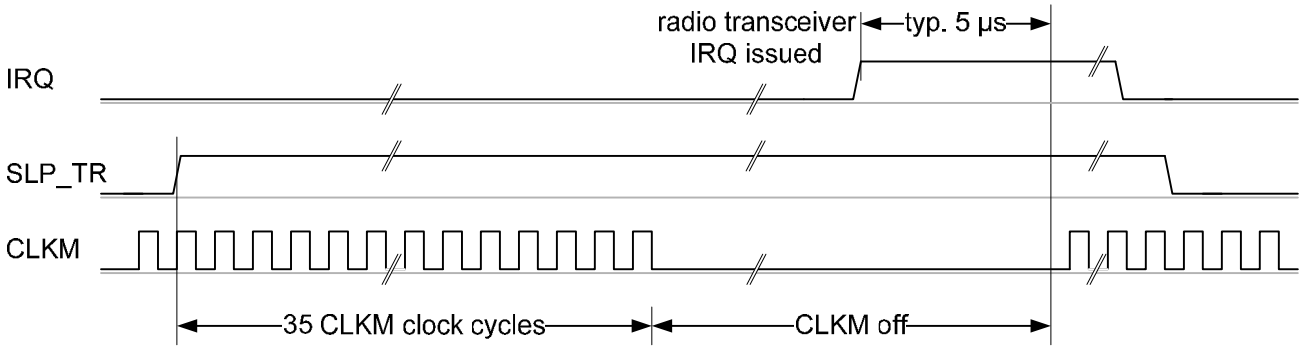
For synchronous systems where CLKM is used as a microcontroller clock source and the SPI master clock (SCLK) is directly derived from CLKM, the AT86RF212 supports an additional power-down mode for receive operating states (RX_ON and RX_AACK_ON).

If an incoming frame is expected and no other applications are running on the microcontroller, it can be powered down without missing incoming frames. This can be achieved by a rising edge on pin SLP_TR that turns CLKM off. Then the radio transceiver state changes from RX_ON or RX_AACK_ON (Extended Operating Mode) to RX_ON_NOCLK or RX_AACK_ON_NOCLK, respectively. In case that a frame is received (e.g. indicated by an IRQ_2 (RX_START) interrupt), the clock output CLKM is automatically switched on again. This scenario is shown in Figure 4-16. In RX_ON state, the clock at pin 17 (CLKM) is switched off after 35 clock cycles when setting the pin SLP_TR = H.

The CLKM clock frequency settings for CLKM_CTRL values 6 and 7 are not intended to directly clock the microcontroller. When using these clock rates, CLKM is turned off immediately when entering RX_ON_NOCLK or RX_AACK_ON_NOCLK.

In states RX_(AACK)_ON_NOCLK and RX_(AACK)_ON, the radio transceiver current consumptions are equivalent. However, the RX_(AACK)_ON_NOCLK current consumption is reduced by the current required for driving pin 17 (CLKM).

Figure 4-16. Wake-Up Initiated by Radio Transceiver Interrupt



4.7 Interrupt Logic

4.7.1 Overview

The AT86RF212 supports 8 interrupt requests as listed in Table 4-15. Each interrupt is enabled by setting the corresponding bit in the interrupt mask register 0x0E (IRQ_MASK). Internally, each pending interrupt is stored in a separate bit of the interrupt status register. All interrupt events are OR-combined to a single external interrupt signal (IRQ, pin 24). If an interrupt is issued (pin IRQ = H), the microcontroller shall read the interrupt status register 0x0F (IRQ_STATUS) to determine the source of the interrupt. A read access to this register clears the interrupt status register and thus the IRQ pin, too.

Interrupts are not cleared automatically when the event that caused them vanishes. Exceptions are IRQ_0 (PLL_LOCK) and IRQ_1 (PLL_UNLOCK) because the occurrence of one clears the other.

The supported interrupts for the Basic Operating Mode are summarized in Table 4-15.

Table 4-15. Interrupt Description in Basic Operating Mode

IRQ Name	Description	Section
IRQ_7 (BAT_LOW)	Indicates a supply voltage below the programmed threshold	7.6.4
IRQ_6 (TRX_UR)	Indicates a Frame Buffer access violation	7.4.3
IRQ_5 (AMI)	Indicates address matching	6.2
IRQ_4 (CCA_ED_DONE)	Multi-functional interrupt: 1. AWAKE_END: • Indicates radio transceiver reached TRX_OFF state at the end of P_ON ⇨ TRX_OFF and SLEEP ⇨ TRX_OFF state transition 2. CCA_ED_DONE: • Indicates the end of a CCA or ED measurement	5.1.2.3 6.6.4
IRQ_3 (TRX_END)	RX: Indicates the completion of a frame reception TX: Indicates the completion of a frame transmission	5.1.3
IRQ_2 (RX_START)	Indicates the start of a PSDU reception; the TRX state changes to BUSY_RX; the PHR is valid to be read from Frame Buffer.	5.1.3
IRQ_1 (PLL_UNLOCK)	Indicates PLL unlock; if the radio transceiver is in BUSY_TX / BUSY_TX_ARET state, the PA is turned off immediately.	7.8.5
IRQ_0 (PLL_LOCK)	Indicates PLL lock	7.8.5

The interrupt IRQ_4 has two meanings, depending on the current radio transceiver state; refer to register 0x01 (TRX_STATUS). After P_ON, SLEEP, or RESET, the radio transceiver issues an interrupt IRQ_4 (AWAKE_END) when it enters state TRX_OFF. The second meaning is only valid for receive states. If the microcontroller initiates an ED or CCA measurement, the completion of the measurement is indicated by interrupt IRQ_4 (CCA_ED_DONE); refer to sections 6.5.4 and 6.6.4 for details.

After P_ON or RESET, all interrupts are disabled. During radio transceiver initialization, it is recommended to enable IRQ_4 (AWAKE_END) to be notified once the TRX_OFF state is entered. Note that AWAKE_END interrupt can usually not be seen when the transceiver enters TRX_OFF state after RESET, because register 0x0E (IRQ_MASK) is reset to mask all interrupts. In this case, state TRX_OFF is normally entered before the microcontroller could modify the register.

The interrupt handling in Extended Operating Mode is described in section 5.2.5.

If register bit IRQ_MASK_MODE (register 0x04, TRX_CTRL_1) is set, an interrupt event can be read from IRQ_STATUS register, even if the interrupt itself is masked; refer to Figure 4-18. However, in that case no timing information for this interrupt is provided.

The IRQ pin polarity can be configured with register bit IRQ_POLARITY (register 0x04, TRX_CTRL_1). The default behavior is active high, which means that pin IRQ = H issues an interrupt request.

If the Frame Buffer Empty Indicator is enabled during Frame Buffer read access, the IRQ pin has an alternative functionality; refer to section 9.6 for details.

A solution to monitor the IRQ_STATUS register (without clearing it) is described in section 4.4.

4.7.2 Register Description

Register 0x0E (IRQ_MASK):

The IRQ_MASK register is used to enable or disable individual interrupts. An interrupt is enabled if the corresponding bit is set to 1. All interrupts are disabled after power up sequence (P_ON state) or reset (RESET state).

Table 4-16. Register 0x0E (IRQ_MASK)

Bit	7	6	5	4
Name	MASK_BAT_LOW	MASK_TRX_UR	MASK_AMI	MASK_ CCA_ED_DONE
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0
Bit	3	2	1	0
Name	MASK_TRX_END	MASK_RX_START	MASK_ PLL_UNLOCK	MASK_PLL_LOCK
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0

If an interrupt is enabled, it is recommended to read the interrupt status register 0x0F (IRQ_STATUS) first to clear the history.

Register 0x0F (IRQ_STATUS):

The IRQ_STATUS register contains the status of the pending interrupt requests.

Table 4-17. Register 0x0F (IRQ_STATUS)

Bit	7	6	5	4
Name	BAT_LOW	TRX_UR	AMI	CCA_ED_DONE
Read/Write	R	R	R	R
Reset Value	0	0	0	0
Bit	3	2	1	0
Name	TRX_END	RX_START	PLL_UNLOCK	PLL_LOCK
Read/Write	R	R	R	R
Reset Value	0	0	0	0

By reading the register after an interrupt is signaled at pin 24 (IRQ), the source of the issued interrupt can be identified. A read access to this register resets all interrupt bits, and so clears the IRQ_STATUS register.

If register bit IRQ_MASK_MODE (register 0x04, TRX_CTRL_1) is set, an interrupt event can be read from IRQ_STATUS register, even if the interrupt itself is masked; refer to Figure 4-18. However, in that case no timing information for this interrupt is provided. It is recommended to read the interrupt status register 0x0F (IRQ_STATUS) first to clear the history.

Register 0x04 (TRX_CTRL_1):

The TRX_CTRL_1 register is a multi purpose register to control various operating modes and settings of the radio transceiver.

Table 4-18. Register 0x04 (TRX_CTRL_1)

Bit	7	6	5	4
Name	PA_EXT_EN	IRQ_2_EXT_EN	TX_AUTO_CRC_ON	RX_BL_CTRL
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	1	0
Bit	3	2	1	0
Name	SPI_CMD_MODE	SPI_CMD_MODE	IRQ_MASK_MODE	IRQ_POLARITY
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0

- **Bit 7 – PA_EXT_EN**

RX/TX Indicator, refer to section 9.4.3.

- **Bit 6 – IRQ_2_EXT_EN**

The timing of a received frame can be determined by a separate pin. If register bit IRQ_2_EXT_EN is set to 1, the reception of a PHR field is directly issued on pin 10 (DIG2), similar to interrupt IRQ_2 (RX_START). Note that this pin is also active, even if the corresponding IRQ_2 (RX_START) mask bit in register 0x0E (IRQ_MASK) is set to 0. The pin remains at high level until the end of the frame receive procedure. For further details refer to section 9.5.

- **Bit 5 – TX_AUTO_CRC_ON**

Refer to section 6.3.5.

- **Bit 4 – RX_BL_CTRL**

Refer to section 9.6.2.

- **Bit 3:2 – SPI_CMD_MODE**

Refer to section 4.4.1.

- **Bit 1 – IRQ_MASK_MODE**

The AT86RF212 supports polling of interrupt events. Interrupt polling can be enabled by register bit IRQ_MASK_MODE. Even if an interrupt request is masked by the corresponding bit in register 0x0E (IRQ_MASK), the event is indicated in register 0x0F (IRQ_STATUS). The different options are shown in Table 4-19.

Table 4-19. IRQ Mask Configuration

IRQ_MASK_MODE	IRQ_MASK Value	Description
0	0	IRQ is suppressed entirely and none of interrupt causes are shown in register IRQ_STATUS.
	≠ 0	All enabled interrupts are signaled on pin IRQ and are also shown in register IRQ_STATUS.
1	0	IRQ is suppressed entirely but all interrupt causes are shown in register IRQ_STATUS.
	≠ 0	All enabled interrupts are signaled on pin IRQ and all interrupt causes are shown in register IRQ_STATUS.

Figure 4-17. IRQ_MASK_MODE = 0

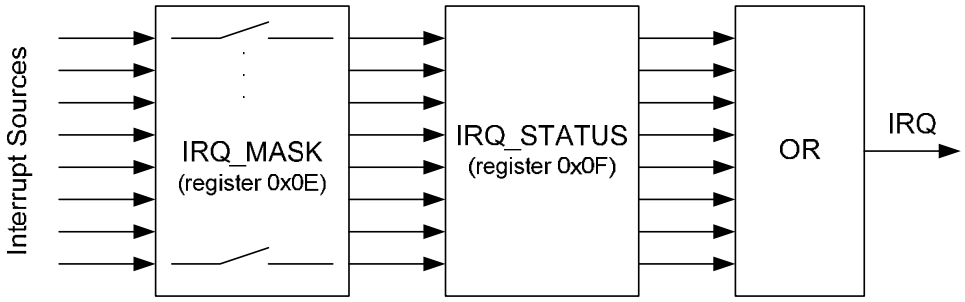
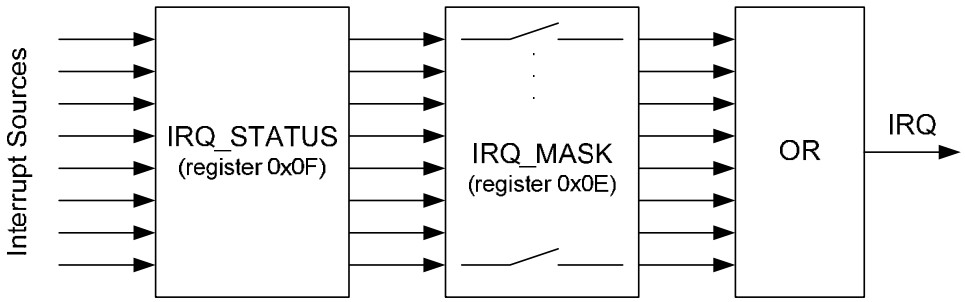


Figure 4-18. IRQ_MASK_MODE = 1



- **Bit 0 – IRQ_POLARITY**

The default polarity of the IRQ pin is active high. The polarity can be configured to active low via register bit IRQ_POLARITY, see Table 4-20.

Table 4-20. Configuration of Pin 24 (IRQ)

Register Bit	Value	Description
IRQ_POLARITY	0	pin IRQ high active
	1	pin IRQ low active

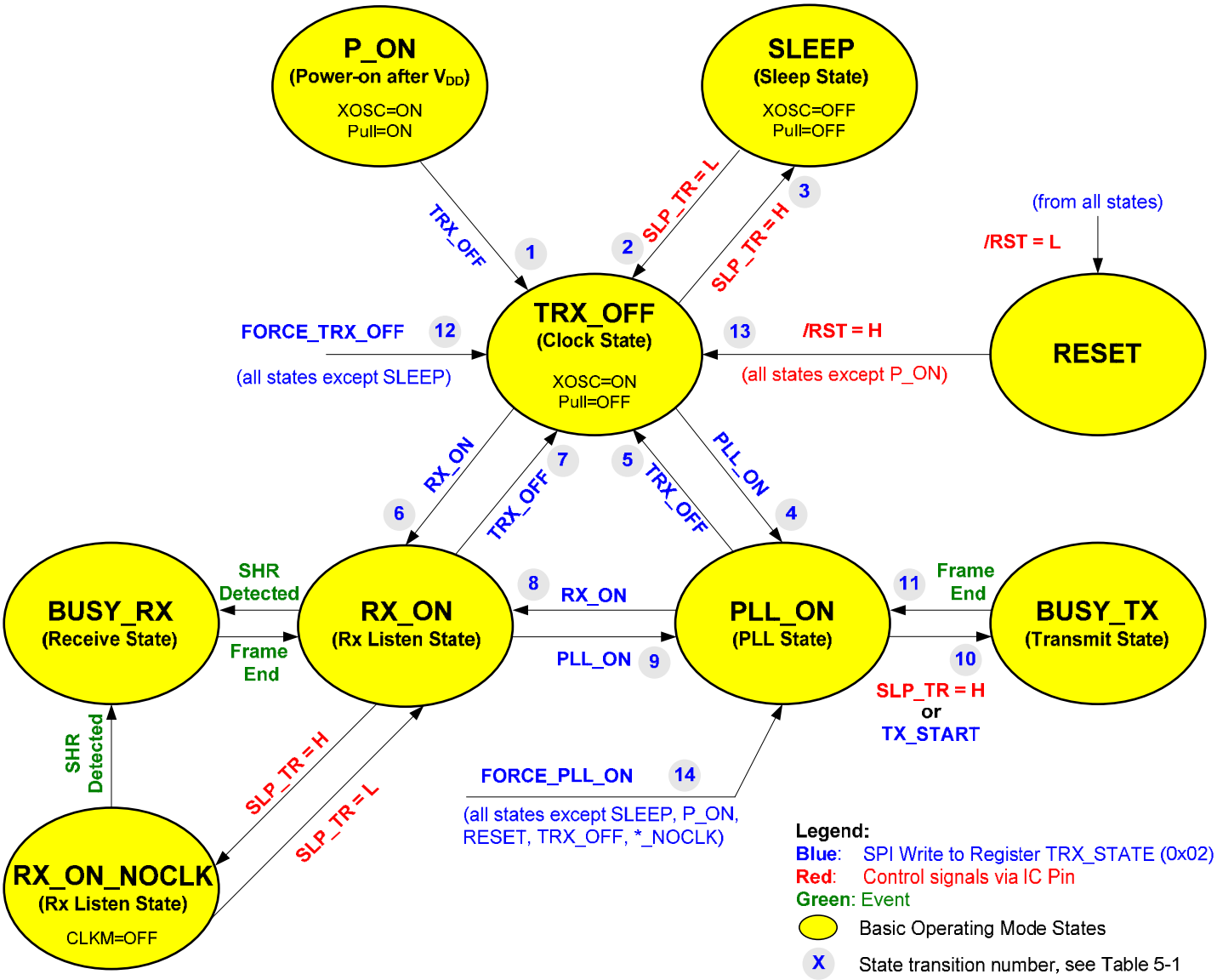
This setting does not affect the polarity of the Frame Buffer Empty Indicator, refer to section 9.6. The Frame Buffer Empty Indicator is always active high.

5 Operating Modes

5.1 Basic Operating Mode

This section summarizes all states to provide the basic functionality of the AT86RF212, such as receiving and transmitting frames, the power up sequence, and sleep. The Basic Operating Mode is designed for IEEE 802.15.4 and ISM applications; the corresponding radio transceiver states are shown in Figure 5-1.

Figure 5-1. Basic Operating Mode State Diagram (for timing refer to Table 5-1)



5.1.1 State Control

The radio transceiver states are controlled either by writing commands to register bits TRX_CMD (register 0x02, TRX_STATE), or directly by two signal pins: pin 11 (SLP_TR) and pin 8 (/RST). A successful state change can be verified by reading the radio transceiver status from register 0x01 (TRX_STATUS).

If TRX_STATUS = 0x1F (STATE_TRANSITION_IN_PROGRESS), the AT86RF212 is in a state transition. Do not try to initiate a further state change while the radio transceiver is in STATE_TRANSITION_IN_PROGRESS.

Pin SLP_TR is a multifunctional pin, refer to section 4.6. Depending on the radio transceiver state, a rising edge of pin SLP_TR causes the following state transitions:

- TRX_OFF → SLEEP
- RX_ON → RX_ON_NOCLK
- PLL_ON → BUSY_TX

whereas the falling edge of pin SLP_TR causes the following state transitions:

- SLEEP → TRX_OFF
- RX_ON_NOCLK → RX_ON

Pin 8 (/RST) causes a reset of all registers (register bits CLKM_CTRL are shadowed; for details, refer to section 7.7.4) and the content of the SRAM is deleted. It forces the radio transceiver into TRX_OFF state. However, if the device was in P_ON state, it remains in P_ON state.

For all states except SLEEP, the state change commands FORCE_TRX_OFF or TRX_OFF lead to a transition into TRX_OFF state. If the radio transceiver is in active receive or transmit states (BUSY_*), the command FORCE_TRX_OFF interrupts these active processes and forces an immediate transition to TRX_OFF. By contrast, a TRX_OFF command is stored until an active state (receiving or transmitting) has been finished. After that the transition to TRX_OFF is performed.

For a fast transition from receive or active transmit states to PLL_ON state, the command FORCE_PLL_ON is provided. Active processes are interrupted. In contrast to FORCE_TRX_OFF, this command does not disable the PLL and the analog voltage regulator AVREG. It is not available in states SLEEP, P_ON, RESET, and all *_NOCLK states.

The completion of each requested state change shall always be confirmed by reading the register bits TRX_STATUS (register 0x01, TRX_STATUS).

5.1.2 Description

5.1.2.1 P_ON – Power-on after V_{DD}

When the external supply voltage (V_{DD}) is applied first to the AT86RF212, the radio transceiver goes into P_ON state performing an on-chip reset. The crystal oscillator is activated and the default 1 MHz master clock is provided at pin 17 (CLKM) after the crystal oscillator has stabilized. CLKM can be used as a clock source to the microcontroller. The SPI interface and digital voltage regulator are enabled.

The on-chip power-on reset sets all registers to their default values. A dedicated reset signal from the microcontroller at pin 8 (/RST) is not necessary but recommended for hardware/software synchronization reasons.

All digital inputs have pull-up or pull-down resistors during P_ON state, refer to section 2.2.2.2. This is necessary to support microcontrollers where GPIO signals are floating

after power-on or reset. The input pull-up and pull-down resistors are disabled when the radio transceiver leaves P_ON state. Leaving P_ON state, outputs pins DIG1/DIG2 are internally connected to digital ground, whereas pins DIG3/DIG4 are internally connected to analog ground, unless their configuration is changed. A reset at pin 8 (/RST) does not enable the pull-up or pull-down resistors.

Prior to leaving P_ON, the microcontroller must set the input pins to the default operating values: SLP_TR = L, /RST = H, and /SEL = H.

All interrupts are disabled by default. Thus, interrupts for state transition control are to be enabled first, e.g. enable IRQ_4 (AWAKE_END) to indicate a state transition to TRX_OFF state. In P_ON state, a first access to the radio transceiver registers is possible after a default 1 MHz master clock is provided at pin 17 (CLKM), refer to t_{TR1} in Table 5-1.

Once the supply voltage has stabilized and the crystal oscillator has settled (see t_{TR15} in Table 5-2), the interrupt mask for the AWAKE_END should be set. A valid SPI write access to register bits TRX_CMD (register 0x02, TRX_STATE) with the command TRX_OFF or FORCE_TRX_OFF initiates a state change from P_ON towards TRX_OFF state, which is then indicated by an AWAKE_END interrupt if enabled.

5.1.2.2 SLEEP – Sleep State

In SLEEP state, the entire radio transceiver is disabled; no circuitry is operating. The radio transceiver current consumption is reduced to leakage current plus the current of a low power voltage regulator (typ. 100 nA). This regulator provides the supply voltage for the registers such that the contents of them remain valid. SLEEP can only be entered from state TRX_OFF by setting SLP_TR = H.

If CLKM is enabled, the SLEEP state is entered 35 CLKM cycles after the rising edge at pin 11 (SLP_TR). At that time CLKM is turned off. If the CLKM output is already turned off (bits CLKM_CTRL = 0 in register 0x03), the SLEEP state is entered immediately.

At clock rates of 250 kHz and symbol clock rate (CLKM_CTRL values 6 and 7; register 0x03, TRX_CTRL_0), the main clock at pin 17 (CLKM) is turned off immediately.

Setting SLP_TR = L returns the radio transceiver back to the TRX_OFF state. During SLEEP, the register contents remains valid while the content of the Frame Buffer and the security engine (AES) are cleared.

/RST = L in SLEEP state returns the radio transceiver to TRX_OFF state and thereby sets all registers to their default values. Exceptions are register bits CLKM_CTRL (register 0x03, TRX_CTRL_0). These register bits require a specific treatment; for details see section 7.7.4.

5.1.2.3 TRX_OFF – Clock State

In TRX_OFF, the crystal oscillator is running and the master clock is available at pin 17 (CLKM). The SPI interface and digital voltage regulator are enabled, thus the radio transceiver registers, the Frame Buffer, and security engine (AES) are accessible (see sections 7.4 and 9.1).

In contrast to P_ON state, pull-up and pull-down resistors are disabled.

Note that the analog front-end is disabled during TRX_OFF. If TRX_OFF_AVDD_EN (register 0x0C, TRX_CTRL_2) is set, the analog voltage regulator is turned on, enabling faster switch to any transmit/receive state.

Entering the TRX_OFF state from P_ON, SLEEP, or RESET state, the state change is indicated by interrupt IRQ_4 (AWAKE_END) if enabled.

5.1.2.4 PLL_ON – PLL State

Entering the PLL_ON state from TRX_OFF state enables the analog voltage regulator (AVREG) first, unless the AVREG is already switched on (register 0x0C, TRX_OFF_AVDD_EN). After the voltage regulator has been settled (see Table 5-2), the PLL frequency synthesizer is enabled. When the PLL has been settled at the receive frequency to a channel defined by register bits CHANNEL (register 0x08, PHY_CC_CCA), CC_NUMBER (register 0x013, CC_CTRL_0), and CC_BAND (register 0x014, CC_CTRL_1), a successful PLL lock is indicated by issuing an interrupt IRQ_0 (PLL_LOCK).

After the RX_ON command is issued in PLL_ON state, register bits TRX_STATUS (register 0x01, TRX_STATUS) immediately indicate the radio being in RX_ON state. However, frame reception can only start, once the PLL has locked.

The PLL_ON state corresponds to the TX_ON state in IEEE 802.15.4.

5.1.2.5 RX_ON and BUSY_RX – RX Listen and Receive State

The AT86RF212 receive mode is internally separated into RX_ON state and BUSY_RX state. There is no difference between these states with respect to the analog radio transceiver circuitry, which is always turned on. In both states the receiver and the PLL frequency synthesizer are enabled.

During RX_ON state, the receiver listens for incoming frames. After detecting a valid synchronization header (SHR), the AT86RF212 automatically enters the BUSY_RX state. The reception of a non-zero PHR field generates an IRQ_2 (RX_START) if enabled.

During PSDU reception, the frame data are stored continuously in the Frame Buffer until the last byte was received. The completion of the frame reception is indicated by an interrupt IRQ_3 (TRX_END) and the radio transceiver returns to state RX_ON. At the same time, the register bit RX_CRC_VALID (register 0x06, PHY_RSSI) is updated with the result of the FCS check (see section 6.3).

Received frames are passed to the address match filter, refer to section 6.2. If the content of the MAC addressing fields (refer to IEEE 802.15.4-2006, section 7.2.1) of a frame matches to the expected addresses, which is further dependent on the addressing mode, an address match interrupt IRQ_5 (AMI) is issued. The expected address values are to be stored in registers 0x20 – 0x2B (Short address, PAN ID, and IEEE address). Frame filtering is available in Basic and Extended Operating Mode, refer to section 6.2.

Leaving state RX_ON is only possible by writing a state change command to register bits TRX_CMD in register 0x02 (TRX_STATE).

5.1.2.6 RX_ON_NOCLK – RX Listen State without CLKM

If the radio transceiver is listening for an incoming frame and the microcontroller is not running an application, the microcontroller may be powered down to decrease the total system power consumption. This specific power-down scenario – for systems running in clock synchronous mode (see section 4) – is supported by the AT86RF212 using the state RX_ON_NOCLK.

This state can only be entered by setting pin 11 (SLP_TR) = H while the radio transceiver is in RX_ON state. Pin 17 (CLKM) is disabled 35 clock cycles after the rising edge at the SLP_TR pin, see Figure 4-16. This allows the microcontroller to complete its power-down sequence.

Note that for CLKM clock rates 250 kHz and symbol clock rates (CLKM_CTRL values 6 and 7; register 0x03, TRX_CTRL_0), the master clock signal CLKM is switched off immediately after the rising edge of SLP_TR.

The reception of a frame shall be indicated to the microcontroller by an interrupt indicating the receive status. CLKM is turned on again, and the radio transceiver enters the BUSY_RX state (see section 4.6 and Figure 4-16). When using RX_ON_NOCLK, it is essential to enable at least one interrupt request indicating the reception status.

After the receive transaction has been completed, the radio transceiver enters the RX_ON state. The radio transceiver only reenters the RX_ON_NOCLK state when the next rising edge of pin SLP_TR pin occurs.

If the AT86RF212 is in the RX_ON_NOCLK state and pin SLP_TR is reset to logic low, it enters the RX_ON state and it starts to supply clock on the CLKM pin again.

A reset in state RX_ON_NOCLK further requires to reset pin SLP_TR to logic low, otherwise the radio transceiver enters directly the SLEEP state.

5.1.2.7 BUSY_TX – Transmit State

A transmission can only be initiated in state PLL_ON. There are two ways to start a transmission:

- Rising edge of pin 11 (SLP_TR)
- TX_START command written to register bits TRX_CMD (register 0x02, TRX_STATE).

Either of these forces the radio transceiver into the BUSY_TX state.

During the transition to BUSY_TX state, the PLL frequency shifts to the transmit frequency, refer to section 7.8.3. The actual transmission of the first data chip of the SHR starts after 1 symbol period (see note) in order to allow PLL settling and PA ramp-up, see Figure 5-6. After transmission of the SHR, the Frame Buffer content is transmitted. In case the PHR indicates a frame length of zero, the transmission is aborted immediately after the PHR field.

After the frame transmission has been completed, the AT86RF212 automatically turns off the power amplifier, generates an IRQ_3 (TRX_END) interrupt, and returns into PLL_ON state.

Note

- Throughout this data sheet, a “symbol period” refers to the definition described in section 7.1.3.

5.1.2.8 RESET State

The RESET state is used to set back the state machine and to reset all registers of the AT86RF212 to their default values; exceptions are register bits CLKM_CTRL (register 0x03, TRX_CTRL_0). These register bits require a specific treatment, for details see section 7.7.4.

A reset forces the radio transceiver into TRX_OFF state. If, however, the device is in P_ON state, it remains in P_ON state.

A reset is initiated with pin /RST = L and the state returns after setting /RST = H. The reset pulse should have a minimum length as specified in sections 5.1.4.5 and 10.4

(parameter 10.4.12). During reset, the microcontroller has to set the radio transceiver control pins SLP_TR and /SEL to their default values.

An overview of the register reset values is provided in Table 11-2.

5.1.3 Interrupt Handling

All interrupts provided by the AT86RF212 (see Table 4-15) are supported in Basic Operating Mode. For example, interrupts are provided to observe the status of radio transceiver RX and TX operations.

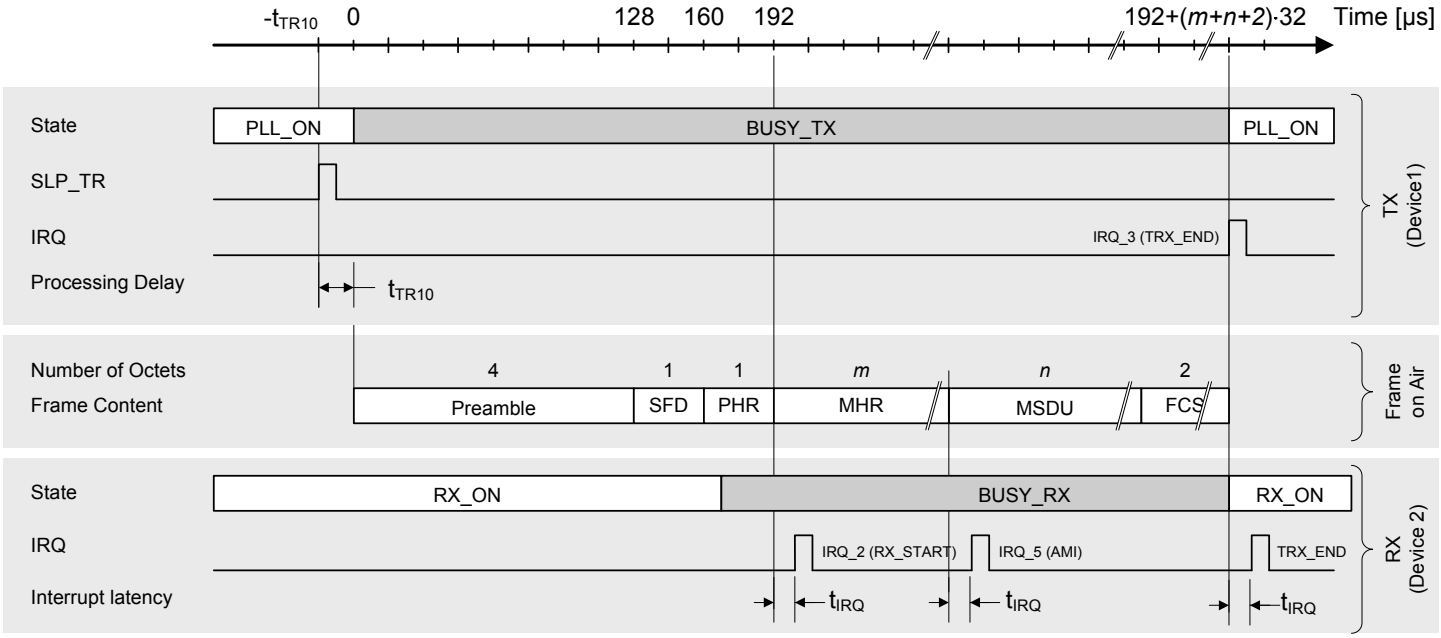
When being in receive mode, IRQ_2 (RX_START) indicates the detection of a non-zero PHR first, IRQ_5 (AMI) an address match, and IRQ_3 (TRX_END) the completion of the frame reception. During transmission, IRQ_3 (TRX_END) indicates the completion of the frame transmission.

Figure 5-2 shows an example for a transmit/receive transaction between two devices and the related interrupt events in Basic Operating Mode. Device 1 transmits a frame containing a MAC header, MAC payload, and a valid FCS. The end of the frame transmission is indicated by IRQ_3 (TRX_END).

The frame is received by Device 2. Interrupt IRQ_2 (RX_START) indicates the detection of a valid PHR field and IRQ_3 (TRX_END) the completion of the frame reception. If the frame passes the Frame Filter (refer to 6.2), an address match interrupt IRQ_5 (AMI) is issued after the reception of the MAC header (MHR).

Processing delay t_{IRQ} is a typical value, refer to section 10.4.

Figure 5-2. Timing of RX_START, AMI, and TRX_END Interrupts in Basic Operating Mode for O-QPSK 250 kbit/s Mode



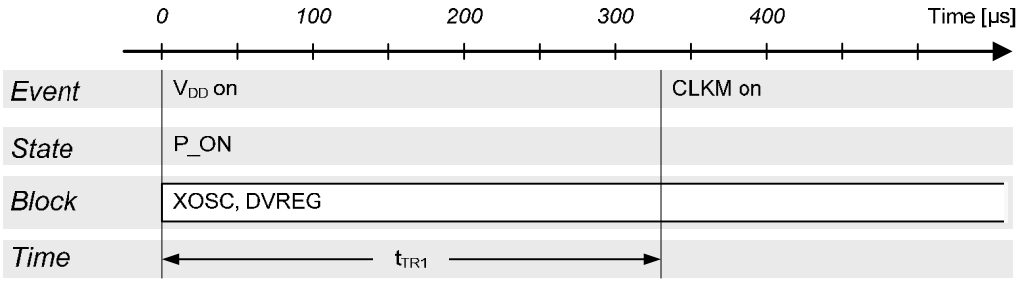
5.1.4 Timing

The following paragraphs depict state transitions and their timing properties. Timings are explained in Table 5-1 and section 10.4.

5.1.4.1 Power-on Procedure

The power-on procedure to P_ON state is shown in Figure 5-3.

Figure 5-3. Power-on Procedure to P_ON State

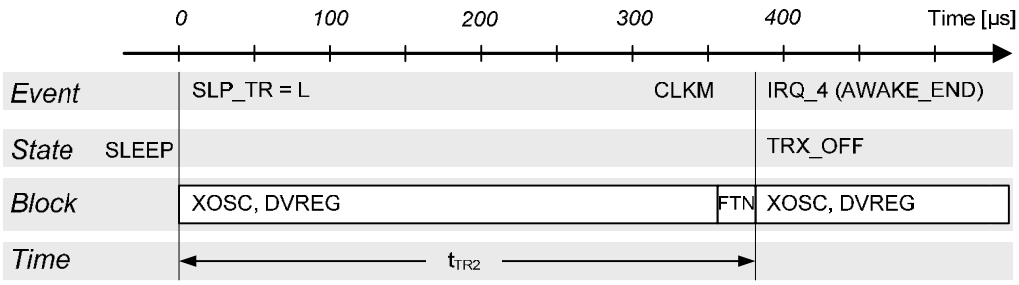


When the external supply voltage (V_{DD}) is supplied to the AT86RF212, the radio transceiver enables the crystal oscillator (XOSC) and the internal 1.8 V voltage regulator for the digital domain (DVREG). After t_{TR1}, the master clock signal is available at pin 17 (CLKM) at a default rate of 1 MHz. If CLKM is available, the SPI has already been enabled and can be used to control the transceiver. As long as no state change towards state TRX_OFF is performed, the radio transceiver remains in P_ON state.

5.1.4.2 Wake-up Procedure

The wake-up procedure from SLEEP state is shown in Figure 5-4.

Figure 5-4. Wake-up Procedure from SLEEP State



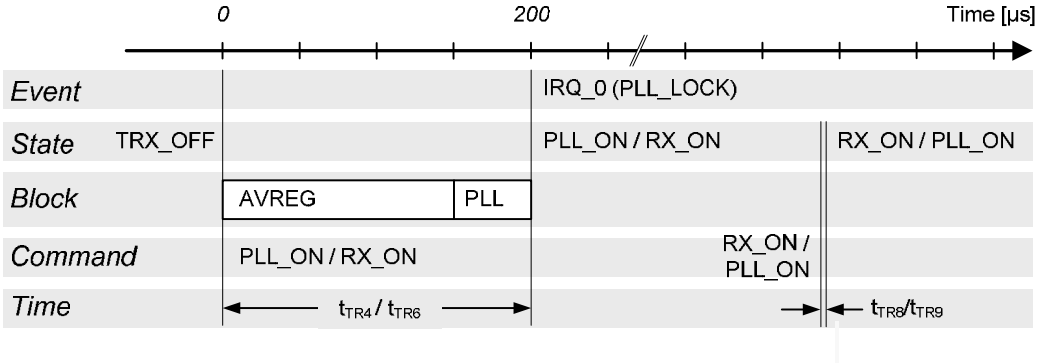
The radio transceiver's SLEEP state is left by releasing pin SLP_TR to logic low. This restarts the XOSC and DVREG. After t_{TR2}, the radio transceiver enters TRX_OFF state. The internal clock signal is available and provided to pin 17 (CLKM) if enabled.

This procedure is similar to power-on, however, the radio transceiver automatically ends in TRX_OFF state. During this, the filter-tuning network (FTN) calibration is performed. Entering TRX_OFF state is signaled by IRQ_4 (AWAKE_END) if this interrupt was enabled by the appropriate mask register bit.

5.1.4.3 State Change from TRX_OFF to PLL_ON / RX_ON

The transition from TRX_OFF to PLL_ON or RX_ON state and further to RX_ON or PLL_ON is shown in Figure 5-5.

Figure 5-5. Transition from TRX_OFF to PLL_ON/RX_ON State and further to RX_ON/PLL_ON



Note: If TRX_CMD = RX_ON in TRX_OFF state, RX_ON state is entered immediately, even if the PLL has not settled.

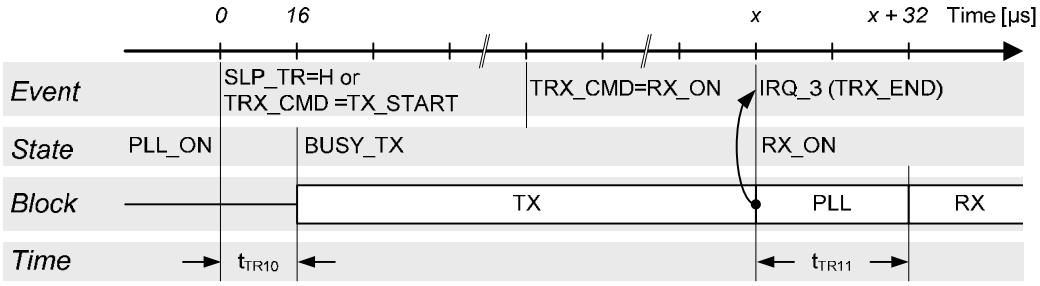
In TRX_OFF state, entering the commands PLL_ON or RX_ON initiates a ramp-up sequence of the internal 1.8 V voltage regulator for the analog domain (AVREG). RX_ON state can be entered any time from PLL_ON state, regardless whether the PLL has already locked, which is indicated by IRQ_0 (PLL_LOCK). Likewise, PLL_ON state can be entered any time from RX_ON state.

When TRX_OFF_AVDD_EN (register 0x0C, TRX_CTRL_2) is already set in TRX_OFF state, the analog voltage regulator is turned on immediately and the ramp up sequence to PLL_ON or RX_ON can be accelerated.

5.1.4.4 State Change from PLL_ON via BUSY_TX to RX_ON States

The transition from PLL_ON to BUSY_TX state and subsequently to RX_ON state is shown in Figure 5-6.

Figure 5-6. PLL_ON to BUSY_TX to RX_ON Timing for O-QPSK 250 kbit/s Mode



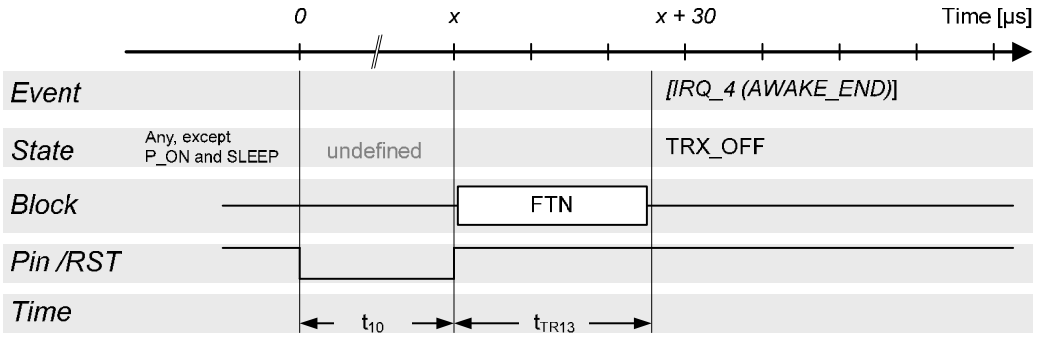
Starting from PLL_ON, it is further assumed that the PLL has already been locked. A transmission is initiated either by a rising edge of pin 11 (SLP_TR) or by command TX_START. The PLL settles to the transmit frequency and the PA is enabled. After the duration of t_{TR10} (1 symbol period), the AT86RF212 changes into BUSY_TX state, transmitting the internally generated SHR and the PSDU data of the Frame Buffer. After completing the frame transmission, indicated by IRQ_3 (TRX_END), the PLL settles back to the receive frequency within t_{TR11} and returns to state PLL_ON.

If during BUSY_TX the radio transmitter is requested to change to a receive state, it automatically proceeds to state RX_ON upon completion of the transmission.

5.1.4.5 Reset Procedure

The radio transceiver reset procedure is shown in Figure 5-7.

Figure 5-7. Reset Procedure



/RST = L sets all registers to their default values. Exceptions are register bits CLKM_CTRL (register 0x03, TRX_CTRL_0), refer to section 7.7.4. After releasing the reset pin (/RST = H), the wake-up sequence including an FTN calibration cycle is performed, refer to section 7.9. After that, the TRX_OFF state is entered.

Figure 5-7 illustrates the reset procedure once P_ON state was left and the radio transceiver was not in SLEEP state.

The reset procedure is identical for all originating radio transceiver states except of states P_ON and SLEEP. Instead, the procedures described in sections 5.1.2.1 and 5.1.2.2 must be followed to enter the TRX_OFF state. If the radio transceiver was in SLEEP state, the XOSC and DVREG are enabled before entering TRX_OFF state.

Notes

- The reset impulse should have a minimum length t_{10} as specified in section 10.4.
- An access to the device should not occur earlier than t_{11} after releasing the pin /RST; refer to section 10.4, parameter 10.4.13.
- A reset overrides an SPI command that might be queued.

5.1.4.6 State Transition Timing Summary

Transition timings are listed in Table 5-1 and do not include SPI access time if not otherwise stated. See measurement setup in Figure 3-1.

Table 5-1. State Transition Timing

No.	Symbol	Transition	Time, typ.	Comments
1	t_{TR1}	P_ON ⇨ until CLKM available	330 µs	Depends on crystal oscillator setup (Siward A207-011, C_L = 10 pF) and external capacitor at DVDD (CB3 = 1 µF nom.)
2	t_{TR2}	SLEEP ⇨ TRX_OFF	380 µs	Depends on crystal oscillator setup (Siward A207-011, C_L = 10 pF) and external capacitor at DVDD (CB3 = 1 µF nom.); TRX_OFF state indicated by IRQ_4 (AWAKE_END)
3	t_{TR3}	TRX_OFF ⇨ SLEEP	35 cycles of CLKM	For f_{CLKM} > 250 kHz
4	t_{TR4}	TRX_OFF ⇨ PLL_ON	200 µs	Depends on external capacitor at AVDD (CB1 = 1 µF nom.); register bit TRX_OFF_AVDD_EN (register 0x0c, TRX_CTRL_2) is not set; for details, refer to section 7.8.3

No.	Symbol	Transition	Time, typ.	Comments
5	t_{TR5}	PLL_ON ⇨ TRX_OFF	1 µs	
6	t_{TR6}	TRX_OFF ⇨ RX_ON	200 µs	Depends on external capacitor at AVDD (CB1 = 1 µF nom.); register bit TRX_OFF_AVDD_EN (register 0x0c, TRX_CTRL_2) is not set; for details, refer to section 7.8.3
7	t_{TR7}	RX_ON ⇨ TRX_OFF	1 µs	
8	t_{TR8}	PLL_ON ⇨ RX_ON	1 µs	
9	t_{TR9}	RX_ON ⇨ PLL_ON	1 µs	Transition time is also valid for TX_ARET_ON / RX_AACK_ON ⇨ PLL_ON
10	t_{TR10}	PLL_ON ⇨ BUSY_TX	1 symbol period	When asserting pin 11 (SLP_TR) or TRX_CMD = TX_START, first symbol transmission is delayed by 1 symbol period (PLL settling and PA ramp up)
11	t_{TR11}	BUSY_TX ⇨ PLL_ON	32 µs	PLL settling time, refer to section 7.8.3
12	t_{TR12}	All states ⇨ TRX_OFF	1 µs	Using TRX_CMD = FORCE_TRX_OFF (see register 0x02, TRX_STATE); not valid for SLEEP ⇨ TRX_OFF (see t_{TR2})
13	t_{TR13}	RESET ⇨ TRX_OFF	26 µs	Not valid for reset in states P_ON or SLEEP
14	t_{TR14}	Various states ⇨ PLL_ON	1 µs	Using TRX_CMD = FORCE_PLL_ON (see register 0x02, TRX_STATE); not valid for states SLEEP, P_ON, RESET, TRX_OFF, and *_NOCLK

The state transition timing is calculated based on the timing of the individual blocks shown in Figure 5-3 to Figure 5-7. The worst case values include maximum operating temperature, minimum supply voltage, and device parameter variations, see Table 5-2.

Table 5-2. Analog Block Initialization and Settling Times

Symbol	Block	Time, typ.	Time, max.	Comments
t_{TR15}	XOSC	330 µs	1000 µs	Leaving SLEEP state; depends on crystal oscillator setup (Siward A207-011, C_L = 10 pF)
t_{TR16}	FTN		25 µs	Filter tuning time
t_{TR17}	DVREG	150 µs	1500 µs	Depends on external bypass capacitor at DVDD (CB3 = 1 µF nom., 10 µF worst case), and on V_{DD}
t_{TR18}	AVREG	150 µs	1500 µs	Depends on external bypass capacitor at AVDD (CB1 = 1 µF nom., 10 µF worst case) , and on V_{DD}
t_{TR19}	PLL, initial	200 µs	370 µs	PLL settling time TRX_OFF ⇨ PLL_ON, including 150 µs AVREG settling time (see t_{TR18})
t_{TR20}	PLL, settling	11 µs	42 µs	Duration of a channel switch within frequency band, refer to section 7.8.3
t_{TR21}	PLL, CF cal.	8 µs	270 µs	PLL center frequency calibration, refer to section 7.8.4
t_{TR22}	PLL, DCU cal.	10 µs		PLL DCU calibration, refer to section 7.8.4
t_{TR23}	PLL, RX ⇨ TX	16 µs		PLL settling time, refer to section 7.8.3
t_{TR24}	PLL, TX ⇨ RX	32 µs		PLL settling time, refer to section 7.8.3
t_{TR25}	RSSI	BPSK-20: 32 µs BPSK-40: 24 µs O-QPSK: 8 µs		RSSI update period in receive states, refer to section 6.4.2
t_{TR26}	ED	8 symbol periods		ED measurement period; different timing with High Data Rate Modes, see sections 6.5.2 and 7.1.4.3
t_{TR28}	CCA	8 symbol periods		CCA measurement period, refer to section 6.6.2

5.1.5 Register Description

Register 0x01 (TRX_STATUS):

A read access to TRX_STATUS register signals the current radio transceiver state. A state change is initiated by writing a state transition command to register bits TRX_CMD (register 0x02, TRX_STATE). Alternatively, a state transition can be initiated by the rising edge of pin 11 (SLP_TR) in the appropriate state. This register is used for Basic and Extended Operating Mode, refer to section 5.2.

Table 5-3. Register 0x01 (TRX_STATUS)

Bit	7	6	5	4
Name	CCA_DONE	CCA_STATUS	Reserved	TRX_STATUS[4]
Read/Write	R	R	R	R
Reset Value	0	0	0	0

Bit	3	2	1	0
Name	TRX_STATUS[3]	TRX_STATUS[2]	TRX_STATUS[1]	TRX_STATUS[0]
Read/Write	R	R	R	R
Reset Value	0	0	0	0

- **Bit 7:6 – CCA_DONE, CCA_STATUS**

Refer to section 6.6.6.

- **Bit 5 – Reserved**
- **Bit 4:0 – TRX_STATUS**

The register bits TRX_STATUS signal the current radio transceiver status. If the requested state transition is not completed yet, the TRX_STATUS returns STATE_TRANSITION_IN_PROGRESS. Do not try to initiate a further state change while the radio transceiver is in STATE_TRANSITION_IN_PROGRESS.

Table 5-4. Radio Transceiver Status, Register Bits TRX_STATUS

Register Bits	Value	State Description
TRX_STATUS	0x00	P_ON
	0x01	BUSY_RX
	0x02	BUSY_TX
	0x06	RX_ON
	0x08	TRX_OFF (CLK Mode)
	0x09	PLL_ON (TX_ON)
	0x0F (3)	SLEEP
	0x11 (1)	BUSY_RX_AACK
	0x12 (1)	BUSY_TX_ARET
	0x16 (1)	RX_AACK_ON
	0x19 (1)	TX_ARET_ON
	0x1C	RX_ON_NOCLK
	0x1D (1)	RX_AACK_ON_NOCLK
	0x1E (1)	BUSY_RX_AACK_NOCLK
	0x1F (2)	STATE_TRANSITION_IN_PROGRESS
		All other values are reserved.

Notes: 1. Extended Operating Mode only, refer to section 5.2.6.
2. Do not try to initiate a further state change while the radio transceiver is in STATE_TRANSITION_IN_PROGRESS state.
3. Register is not accessible in SLEEP state.

Register 0x02 (TRX_STATE):

Radio transceiver state changes can be initiated by writing register bits TRX_CMD. This register is used for Basic and Extended Operating Mode, refer to section 5.2.

Table 5-5. Register 0x02 (TRX_STATE)

Bit	7	6	5	4
Name	TRAC_STATUS	TRAC_STATUS	TRAC_STATUS	TRX_CMD[4]
Read/Write	R	R	R	R/W
Reset Value	0	0	0	0

Bit	3	2	1	0
Name	TRX_CMD[3]	TRX_CMD[2]	TRX_CMD[1]	TRX_CMD[0]
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0

- **Bit 7:5 – TRAC_STATUS**

Refer to section 5.2.6.

- **Bit 4:0 – TRX_CMD**

A write access to register bits TRX_CMD initiates a radio transceiver state transition.

Table 5-6. State Control Command, Register Bits TRX_CMD

Register Bits	Value	State Transition towards
TRX_CMD	0x00	NOP
	0x02	TX_START
	0x03	FORCE_TRX_OFF
	0x04 (1)	FORCE_PLL_ON
	0x06	RX_ON
	0x08	TRX_OFF (CLK Mode)
	0x09	PLL_ON (TX_ON)
	0x16 (2)	RX_AACK_ON
	0x19 (2)	TX_ARET_ON
		All other values are reserved and mapped to NOP.

Notes: 1. FORCE_PLL_ON is not valid for states SLEEP, P_ON, RESET, and all *_NOCLK states, as well as STATE_TRANSITION_IN_PROGRESS towards these states.
2. Extended Operating Mode only, refer to section 5.2.6.

5.2 Extended Operating Mode

The Extended Operating Mode is a hardware MAC accelerator and goes beyond the basic radio transceiver functionality provided by the Basic Operating Mode. It handles time critical MAC tasks requested by the IEEE 802.15.4-2003/2006 standard, such as automatic acknowledgement, automatic CSMA-CA, and retransmission. This results in a more efficient IEEE 802.15.4-2003/2006 software MAC implementation, including reduced code size, and may allow the use of a smaller microcontroller.

The Extended Operating Mode is designed to support IEEE 802.15.4-2003/2006 standard compliant frames and comprises the following procedures:

Receive with Automatic Acknowledgement (RX_AACK) divides into the tasks:

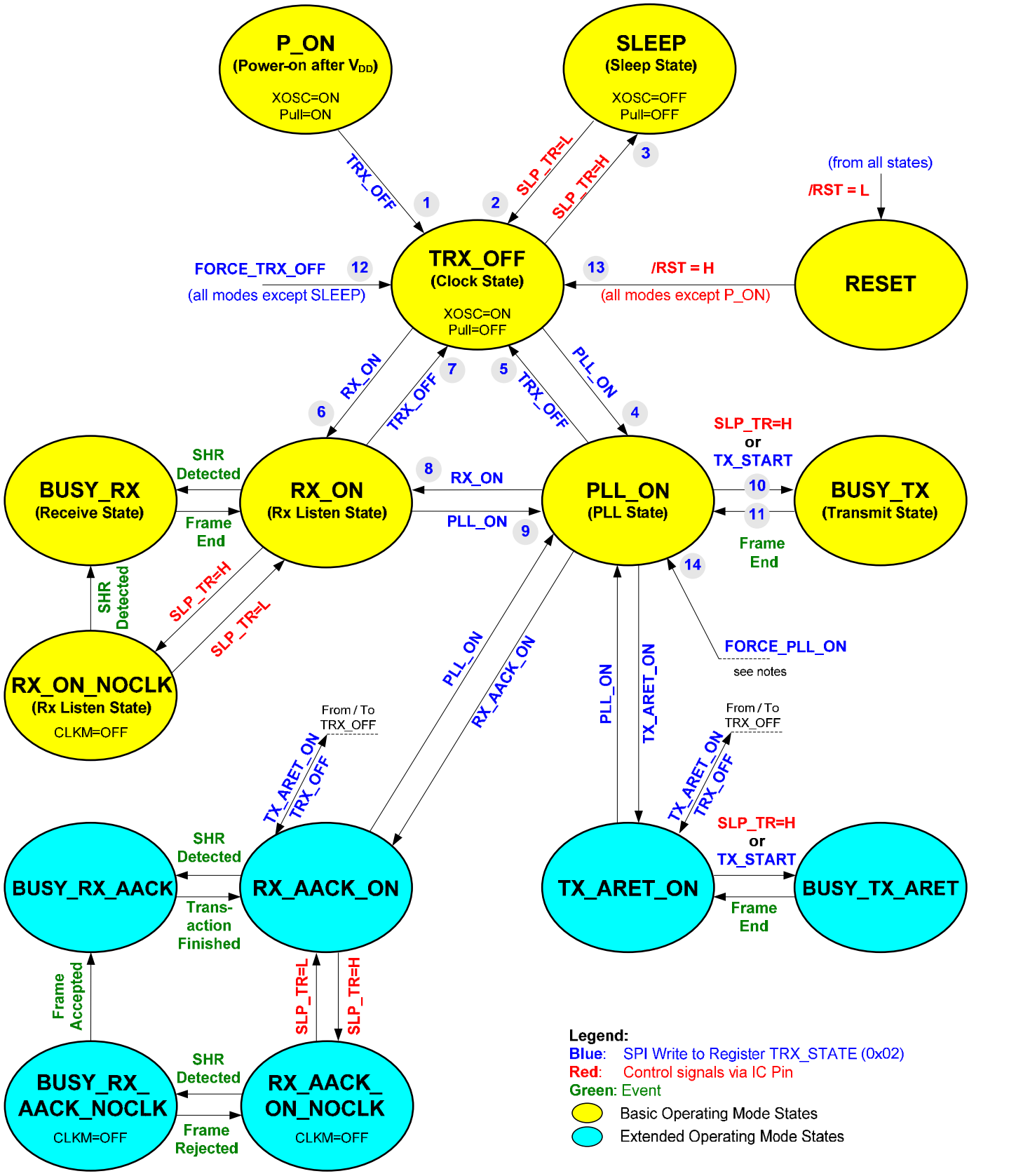
- Frame reception and automatic FCS check
- Configurable addressing fields check
- Interrupt indicating address match
- Interrupt indicating frame reception if it passes frame filtering and FCS check
- Automatic acknowledgment (ACK) frame transmission if applicable
- Support of slotted acknowledgment using SLP_TR pin (used for beacon-enabled operation)

Transmit with Automatic CSMA-CA and Retransmission (TX_ARET) divides into the tasks:

- CSMA-CA, including automatic CCA retry and random backoff
- Frame transmission and automatic FCS field generation
- Reception of ACK frame (if ACK was requested)
- Automatic retry of transmissions if ACK was expected but not received or accepted
- Interrupt signaling with transaction status

An AT86RF212 state diagram, including the Extended Operating Mode states, is shown in Figure 5-8. Yellow marked states represent the Basic Operating Mode; blue marked states represent the Extended Operating Mode.

Figure 5-8. Extended Operating Mode State Diagram



5.2.1 State Control

The Extended Operating Modes RX_AACK and TX_ARET are controlled via register bits TRX_CMD (register 0x02, TRX_STATE), which receives the state transition commands. The corresponding states, RX_AACK_ON and TX_ARET_ON respectively, are to be entered from states TRX_OFF or PLL_ON as illustrated by Figure 5-8. The success of the state change shall be confirmed by reading register 0x01 (TRX_STATUS).

RX_AACK - Receive with Automatic Acknowledgement

A state transition to RX_AACK_ON from PLL_ON or TRX_OFF is initiated by writing the command RX_AACK_ON to register bits TRX_CMD (register 0x02, TRX_STATE). On success, reading register 0x01 (TRX_STATUS) returns RX_AACK_ON or BUSY_RX_AACK. The latter one is returned if a frame is currently about being received.

The RX_AACK Extended Operating Mode is terminated by writing command PLL_ON to the register bits TRX_CMD. If the AT86RF212 is within a frame receive or acknowledgment procedure (BUSY_RX_AACK), the state change is executed after finish. Alternatively, the commands FORCE_TRX_OFF or FORCE_PLL_ON can be used to cancel the RX_AACK transaction and change into transceiver state TRX_OFF or PLL_ON.

TX_ARET - Transmit with Automatic CSMA-CA and Retransmission

Similarly, a state transition to TX_ARET_ON from PLL_ON or TRX_OFF is initiated by writing command TX_ARET_ON to register bits TRX_CMD (register 0x02, TRX_STATE). The radio transceiver is in the TX_ARET_ON state when register 0x01 (TRX_STATUS) returns TX_ARET_ON. The TX_ARET transaction is actually started with a rising edge of pin 11 (SLP_TR) or by writing the command TX_START to register bits TRX_CMD.

The TX_ARET Extended Operating Mode is terminated by writing the command PLL_ON to the register bits TRX_CMD. If the AT86RF212 is within a CSMA-CA, a frame-transmit or an acknowledgment procedure (BUSY_TX_ARET), the state change is executed after finish. Alternatively, the command FORCE_PLL_ON can be used to instantly terminate the TX_ARET transaction and change into transceiver state PLL_ON.

Note

- A state change request from TRX_OFF to RX_AACK_ON or TX_ARET_ON internally passes the state PLL_ON to initiate the radio transceiver front end. Thus, the readiness to receive or transmit data is delayed accordingly (see Table 5-1). In that case, it is recommended to use interrupt IRQ_0 (PLL_LOCK) as an indicator.

5.2.2 Configuration

As the usage of the Extended Operating Mode is based on Basic Operating Mode functionality, only features beyond the basic radio transceiver functionality are described in the following sections. For details of the Basic Operating Mode, refer to section 5.1.

When using the RX_AACK or TX_ARET modes, the following registers need to be configured.

RX_AACK configuration steps:

- Setup Frame Filter: registers 0x20 – 0x2B
  - Short address, PAN ID, and IEEE address
- Configure acknowledgement generation registers 0x2C, 0x2E
  - Handling of Frame Version Subfield
  - Handling of Pending Data
  - Automatic or slotted ACK generation
- Additional Frame Filtering Properties register 0x17
  - Frame Filter Version Control
  - Characterize the device as PAN coordinator if required
  - Promiscuous Mode
  - Handling of reserved frame types

The configuration of the Frame Filter is described in section 6.2.1. The addresses for the address match algorithm are to be stored in the appropriate address registers. Additional control of the RX_AACK mode is done with register 0x17 (XAH_CTRL_1) and register 0x2E (CSMA_SEED_1).

Configuration examples for different device operating modes and handling of various frame types can be found in section 5.2.3.1.

TX_ARET configuration steps:

- Enable automatic FCS handling if necessary register 0x04
- Configure CSMA-CA
  - MAX_FRAME_RETRIES register 0x2C
  - MAX_CSMA_RETRIES register 0x2C
  - CSMA_SEED registers 0x2D, 0x2E
  - MAX_BE, MIN_BE register 0x2F
- Configure CCA (see section 6.6)

MAX_FRAME_RETRIES (register 0x2C, XAH_CTRL_0) defines the maximum number of frame retransmissions.

The register bits MAX_CSMA_RETRIES (register 0x2C) configure the maximum number of CSMA-CA retries after a busy channel is detected.

The CSMA_SEED_0 and CSMA_SEED_1 register bits (registers 0x2D and 0x2E) define a random seed for the backoff time random-number generator in the AT86RF212.

The register bits MAX_BE and MIN_BE (register 0x2F) define the maximum and minimum CSMA backoff exponent, respectively.

5.2.3 RX_AACK_ON – Receive with Automatic ACK

The RX_AACK Extended Operating Mode handles reception and automatic acknowledgement of IEEE 802.15.4 compliant frames.

The general flow of the RX_AACK algorithm is shown in Figure 5-9. Here the gray shaded area is the standard flow of an RX_AACK transaction for IEEE 802.15.4

compliant frames, refer to 5.2.3.2. All other procedures are exceptions for specific operating modes or frame formats, refer to section 5.2.3.3.

In RX_AACK_ON state, the AT86RF212 listens for incoming frames. After detecting a non-zero PHR, the AT86RF212 changes into BUSY_RX_AACK state and parses the frame content of the MAC header (MHR), refer to section 6.1.2. If the content of the MAC addressing fields of the received frame passes the frame filter, an address match interrupt IRQ_5 (AMI) is issued. The reference address values are to be stored in registers 0x20 – 0x2B (Short address, PAN ID, and IEEE address). The Frame Filter operations are described in detail in section 6.2.

Generally, at nodes configured as a normal device or PAN coordinator, a frame is indicated by interrupt IRQ_3 (TRX_END) if the frame passes the Frame Filter and the FCS is valid. The interrupt is issued after the completion of the frame reception. The microcontroller can then read the frame data. An exception applies if promiscuous mode is enabled, see section 5.2.3.2. In that case, an interrupt IRQ_3 is issued for all frames.

During reception, the AT86RF212 parses bit 5 (ACK Request) of the frame control field of the received data or MAC command frame to check if an acknowledgement (ACK) response is expected. In that case and if the frame matches the third level filtering rules (see IEEE 802.15.4-2006, section 7.5.6.2), the radio transceiver automatically generates and transmits an ACK frame and proceeds back to RX_AACK_ON state.

By default, the acknowledgment frame is transmitted *aTurnaroundTime* (12 symbols; see IEEE 802.15.4-2006, section 6.4.1) after the reception of the last symbol of a data or MAC command frame. Optionally, for non-compliant networks, this delay can be reduced to 2 symbols by register bit AACK_ACK_TIME (register 0x2E, XAH_CTRL_1).

The content of the “Frame Pending” subfield of the ACK response is set according to register bit AACK_SET_PD (register 0x2E, CSMA_SEED_1). The sequence number is copied from the received frame accordingly.

If the register bit AACK_DIS_ACK (register 0x2E, CSMA_SEED_1) is set, no acknowledgement frame is sent, even if requested.

For slotted operation, the start of the transmission of acknowledgement frames is controlled by pin 11 (SLP_TR), refer to 5.2.3.5.

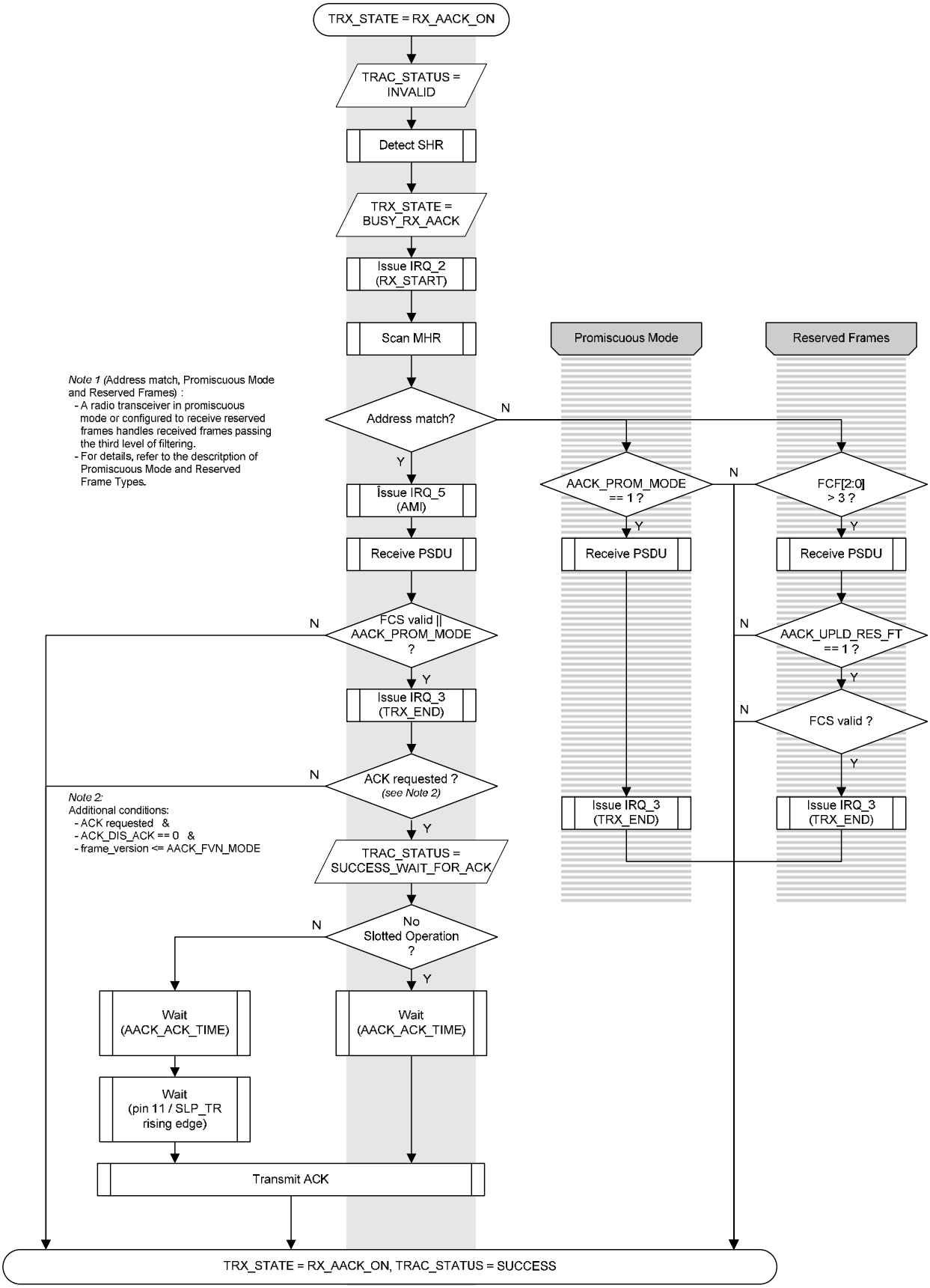
The status of the RX_AACK transaction is indicated by register subfield TRAC_STATUS (register 0x02, TRX_STATE). Table 5-7 lists corresponding values.

Table 5-7. RX_AACK interpretation of TRAC_STATUS Register Bits

Value	Name	Description
0	SUCCESS	The transaction has finished with success
2	SUCCESS_WAIT_FOR_ACK	The transaction either waits *aTurnaroundTime* until the ACK is transmitted or expects the rising edge on pin 11 (SLP_TR) to start the transmission (slotted operation)
7	INVALID	Default value when RX_AACK transaction is invoked

Note that generally the AT86RF212 PHY modes as well as the Extended Feature Set work independent from RX_AACK Extended Operating Mode.

Figure 5-9. Flow Diagram of RX_AACK



5.2.3.1 Configuration Registers

RX_AACK configuration as described below shall be done prior to switching the AT86RF212 into state RX_AACK_ON, refer to section 5.2.1.

Table 5-8 summarizes all register bits which affect the behavior of an RX_AACK transaction. For frame filtering it is further required to setup address registers to match to the expected address.

Table 5-8. Overview of RX_AACK Configuration Bits

Register Address	Register Bit	Name	Description
0x20,0x21 0x22,0x23 0x24 … 0x2B		SHORT_ADDR_0/1 PAN_ADDR_0/1 IEEE_ADDR_0 … IEEE_ADDR_7	Setup Frame Filter, see section 6.2.1
0x0C	7	RX_SAFE_MODE	Dynamic frame buffer protection, see section 9.7
0x17	1	AACK_PROM_MODE	Enable promiscuous mode
0x17	2	AACK_ACK_TIME	Modify auto acknowledge start time
0x17	4	AACK_UPLD_RES_FT	Enable reserved frame type reception, needed to receive non-standard compliant frames, see section 5.2.3.3
0x17	5	AACK_FLTR_RES_FT	Filter reserved frame types like data frame type, needed for filtering of non-standard compliant frames, see section 5.2.3.3
0x2C	0	SLOTTED_OPERATION	If set, acknowledgment transmission has to be triggered by pin 11 (SLP_TR), see section 4.6
0x2E	3	AACK_I_AM_COORD	Define device as PAN coordinator, see section 5.2.3.2
0x2E	4	AACK_DIS_ACK	Disable generation of acknowledgment
0x2E	5	AACK_SET_PD	Signal pending data in Frame Control Field (FCF) of acknowledgement
0x2E	7:6	AACK_FVN_MODE	Control the ACK generation, depending on FCF frame version number

The usage of the RX_AACK configuration bits for various device types or operating modes is explained in the following sections. Configuration bits not mentioned in the following two sections should be set to their reset values according to Table 11-2.

All registers mentioned in Table 5-8 are described in section 5.2.6.

5.2.3.2 Configuration of IEEE Compliant Scenarios

Device not operating as a PAN Coordinator

Table 5-9 shows the RX_AACK configuration registers, required to setup a typical IEEE 802.15.4 compliant device.

Table 5-9. Configuration of IEEE 802.15.4 Devices

Register Address	Register Bit	Name	Description
0x20,0x21 0x22,0x23 0x24 … 0x2B		SHORT_ADDR_0/1 PAN_ADDR_0/1 IEEE_ADDR_0 … IEEE_ADDR_7	Setup Frame Filter, see section 6.2.1
0x0C	7	RX_SAFE_MODE	*0*: Disable frame protection *1*: Enable frame protection
0x2C	0	SLOTTED_OPERATION	*0*: Transceiver operates in unslotted mode. *1*: Transceiver operates in slotted mode, see section 5.2.3.5
0x2E	7:6	AACK_FVN_MODE	Controls the ACK behavior, depending on FCF frame version number *b00*: Acknowledges only frames with version number 0, i.e. according to IEEE 802.15.4-2003 frames *b01*: Acknowledges only frames with version number 0 or 1, i.e. frames according to IEEE 802.15.4-2003/2006 *b10*: Acknowledges only frames with version number 0 or 1 or 2 *b11*: Acknowledges all frames independent of the FCF frame version number

Notes

- The default value of the short address is 0xFFFF. Thus, if no short address has been configured, only frames with either the broadcast address or the IEEE address are accepted by the frame filter.
- In the IEEE 802.15.4-2003 standard the frame version subfield does not yet exist but is marked as reserved. According to this standard, reserved fields have to be set to zero. At the same time, the IEEE 802.15.4-2003 standard requires ignoring reserved bits upon reception. Thus, there is a contradiction in the standard which can be interpreted in two ways:
  1. If a network should only allow access to nodes compliant to IEEE 802.15.4-2003, then AACK_FVN_MODE should be set to 0.
  2. If a device should acknowledge all frames independent of its frame version, AACK_FVN_MODE should be set to 3. However, this may result in conflicts with co-existing IEEE 802.15.4-2006 standard compliant networks.

  The same holds for PAN coordinators, see below.

PAN Coordinator

Table 5-10 shows the RX_AACK configuration registers required to setup a PAN coordinator device.

Table 5-10. Configuration of a PAN Coordinator

Register Address	Register Bit	Name	Description
0x20,0x21 0x22,0x23 0x24 … 0x2B		SHORT_ADDR_0/1 PAN_ADDR_0/1 IEEE_ADDR_0 … IEEE_ADDR_7	Setup Frame Filter, see section 6.2.1
0x0C	7	RX_SAFE_MODE	*0*: Disable frame protection *1*: Enable frame protection
0x2C	0	SLOTTED_OPERATION	*0*: Transceiver operates in unslotted mode. *1*: Transceiver operates in slotted mode, see section 5.2.3.5.
0x2E	3	AACK_I_AM_COORD	*1*: Device is PAN coordinator
0x2E	5	AACK_SET_PD	*0*: “Frame Pending” subfield is 0 in FCF *1*: “Frame Pending” subfield is 1 in FCF
0x2E	7:6	AACK_FVN_MODE	Controls the ACK behavior, depending on FCF frame version number *b00*: Acknowledges only frames with version number 0, i.e. according to IEEE 802.15.4-2003 frames *b01*: Acknowledges only frames with version number 0 or 1, i.e. frames according to IEEE 802.15.4-2003/2006 *b10*: Acknowledges only frames with version number 0 or 1 or 2 *b11*: Acknowledges all frames, independent of the FCF frame version number

Promiscuous Mode or Sniffer

The promiscuous mode is described in IEEE 802.15.4-2006, section 7.5.6.5. This mode is further illustrated in Figure 5-9. According to IEEE 802.15.4-2006, in promiscuous mode the MAC sub layer shall pass received frames with correct FCS to the next higher layer without further processing. This implies that received frames should never be automatically acknowledged.

In order to support sniffer application and promiscuous mode, only second level filter rules as defined by IEEE 802.15.4-2006, section 7.5.6.2, are applied to the received frame.

Table 5-11 shows the RX_AACK configuration registers required to setup a typical IEEE 802.15.4 compliant device which operates in promiscuous mode.

Table 5-11. Configuration of Promiscuous Mode

Register Address	Register Bit	Name	Description
0x20,0x21 0x22,0x23 0x24 … 0x2B		SHORT_ADDR_0/1 PAN_ADDR_0/1 IEEE_ADDR_0 … IEEE_ADDR_7	Each address shall be set to 0x00
0x17	1	AACK_PROM_MODE	*1*: Enable promiscuous mode
0x2E	4	AACK_DIS_ACK	*1*: Disable acknowledgment generation

To signal the availability of frame data, an IRQ_3 (TRX_END) is issued, even if the FCS is invalid. Thus, it is necessary to read register bit RX_CRC_VALID (register 0x06, PHY_RSSI) after IRQ_3 (TRX_END) in order to verify the reception of a frame with a valid FCS. Alternatively, bit 7 of byte RX_STATUS can be evaluated, refer to section 4.3.2.

If a device, operating in promiscuous mode, received a frame with a valid FCS that furthermore passed the third level of filtering (according to IEEE 802.15.4-2006, section 7.5.6.2), an acknowledgement (ACK) frame would be transmitted. But, according to the definition of the promiscuous mode, a received frame shall not be acknowledged, even if requested. Thus, register bit AACK_DIS_ACK (register 0x2E, CSMA_SEED_1) must be set to 1 to disable ACK generation.

In all receive modes, interrupt IRQ_5 (AMI) is issued if the received frame matches the node's address according to the filter rules described in section 6.2.

Promiscuous mode could also be implemented using state RX_ON (Basic Operating Mode), refer to section 5.1. However, the RX_AACK transaction additionally enables extended functionality like automatic acknowledgement and non-destructive frame filtering.

5.2.3.3 Configuration of Non IEEE Compliant Scenarios

Reserved Frame Types

In RX_AACK mode, frames with reserved frame types (refer to section 6.1.2.2, Table 6-2) can also be handled. This might be required when implementing proprietary, non-standard compliant protocols. The reception of reserved frame types is an extension of the AT86RF212 Frame Filter, see section 6.2. Received frames are either handled like data frames, or may be allowed to completely bypass the Frame Filter. The flow chart in Figure 5-9 shows the corresponding state machine.

In addition to Table 5-9 or Table 5-10, the following Table 5-12 shows RX_AACK configuration registers required to setup a node to receive reserved frame types.

Table 5-12. RX_AACK Configuration to Receive Reserved Frame Types

Register Address	Register Bit	Name	Description
0x17	4	AACK_UPLD_RES_FT	*1*: Enable reserved frame type reception
0x17	5	AACK_FLTR_RES_FT	Filter reserved frame types like data frame type *0*: Disable *1*: Enable

There are two different options for handling reserved frame types.

1. AACK_UPLD_RES_FT = 1, AACK_FLTR_RES_FT = 0:

   Any non-corrupted frame with a reserved frame type is indicated by the interrupt IRQ_3 (TRX_END). No further frame filtering is applied on those frames. The interrupt IRQ_5 (AMI) is never generated and no acknowledgment is sent.

2. AACK_UPLD_RES_FT = 1, AACK_FLTR_RES_FT = 1:

   Any frame with a reserved frame type is treated like an IEEE 802.15.4 compliant data frame. This implies the generation of the interrupt IRQ_5 (AMI) upon address matches. The IRQ_3 (TRX_END) interrupt is only generated if the address matches and the frame is correct (FCS valid). Then an acknowledgment is sent if the ACK request subfield of the received frame is set accordingly.

Short Acknowledgment Frame Start Timing

Register bit AACK_ACK_TIME (register 0x17, XAH_CTRL_1) defines the delay between the end of the frame reception and the start of the transmission of an acknowledgment frame.

Table 5-13. ACK Start Timing for Unslotted Operation

Register Address	Register Bit	Name	Description
0x17	2	AACK_ACK_TIME	*0*: Standard compliant acknowledgement delay of 12 symbol periods *1*: Reduced acknowledgment delay of 2 symbol periods (BPSK-20, O-QPSK-{100,200,400}) or 3 symbol periods (BPSK-40, O-QPSK-{250,500,1000}).

Note that this feature can be used in all scenarios, independent of other configurations. However, shorter acknowledgment timing is especially useful when using High Data Rate Modes to increase battery lifetime and to improve the overall data throughput, refer to section 7.1.4.3.

In slotted operation mode, the acknowledgment transmission is actually started by pin 11 (SLP_TR). Table 5-14 shows that the AT86RF212 enables the trigger pin with an appropriate delay. Thus, a transmission cannot be started earlier.

Table 5-14. ACK Start Timing for Slotted Operation

Register Address	Register Bit	Name	Description
0x17	2	AACK_ACK_TIME	*0*: Acknowledgment frame transmission can be triggered after 6 symbol periods. *1*: Acknowledgment frame transmission can be triggered after 3 symbol periods.

5.2.3.4 RX_AACK_NOCLK – RX_AACK_ON without CLKM

If the AT86RF212 is listening for an incoming frame and the microcontroller is not running an application, the microcontroller can be powered down to decrease the total system power consumption. This special power-down scenario for systems running in clock synchronous mode (see section 4.2) is supported by the AT86RF212 using the states RX_AACK_ON_NOCLK and BUSY_RX_AACK_NOCLK, see Figure 5-8. They

achieve the same functionality as the states RX_AACK_ON and BUSY_RX_AACK with pin 17 (CLKM) disabled.

The RX_AACK_NOCLK state is entered from RX_AACK_ON by a rising edge at pin 11 (SLP_TR). The return to RX_AACK_ON state automatically results either from the reception of a valid frame, indicated by interrupt IRQ_3 (TRX_END), or a falling edge on pin SLP_TR.

A received frame is considered valid if it passes frame filtering and has a correct FCS. If an ACK was requested, the radio transceiver enters BUSY_RX_AACK state and follows the procedure described in section 5.2.3.

After the RX_AACK transaction has been completed, the radio transceiver remains in RX_AACK_ON state. The AT86RF212 re-enters the RX_AACK_ON_NOCLK state only by the next rising edge on pin 11 (SLP_TR).

The timing and behavior, when CLKM is disabled or enabled, are described in section 4.6.

Note that RX_AACK_NOCLK is not available for slotted operation mode (see section 5.2.3.5).

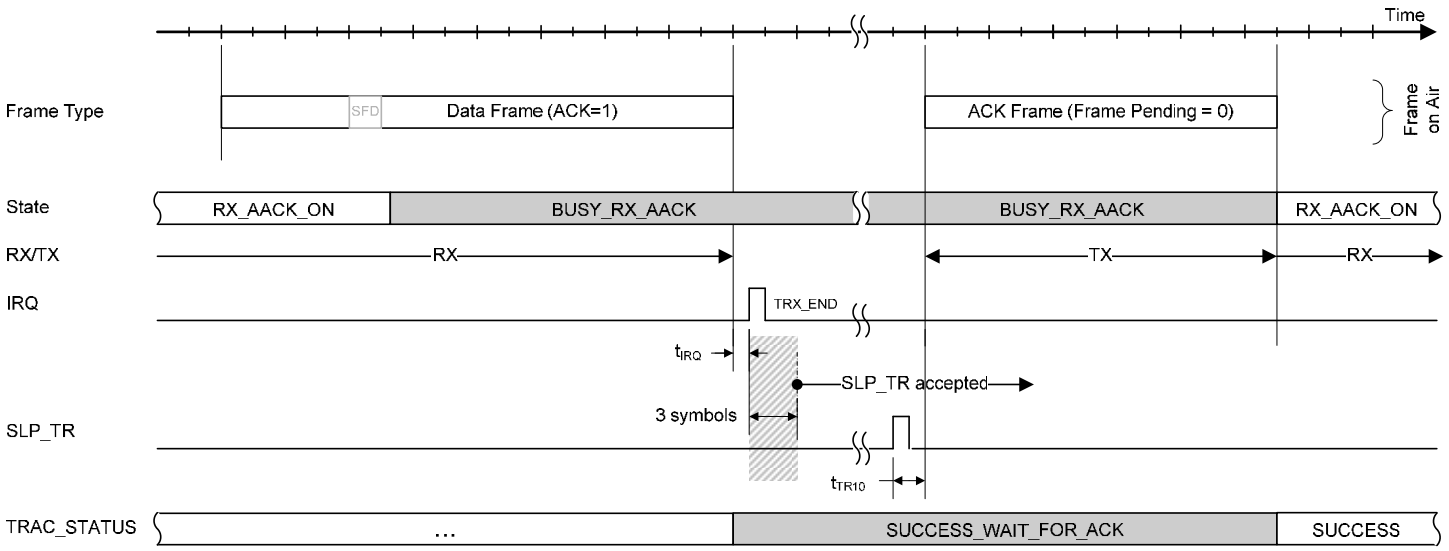
5.2.3.5 Slotted Operation – Slotted Acknowledgement

In networks using slotted operation the start of the acknowledgment frame, and thus the exact timing, must be provided by the microcontroller. Exact timing requirements for the transmission of acknowledgments in beacon-enabled networks are explained in IEEE 802.15.4-2006, section 7.5.6.4.2. In conjunction with the microcontroller the AT86RF212 supports slotted acknowledgement operation. This mode is invoked by setting register bit SLOTTED_OPERATION (register 0x2C, XAH_CTRL_0) to 1.

If an acknowledgment (ACK) frame is to be transmitted in RX_AACK mode, the radio transceiver expects a rising edge on pin 11 (SLP_TR) to actually start the transmission. During this waiting period, the transceiver reports SUCCESS_WAIT_FOR_ACK through register bits TRAC_STATUS (register 0x02, XAH_CTRL_0), see Figure 5-9. The minimum delay between the occurrence of interrupt IRQ_3 (TRX_END) and pin start of the ACK frame in slotted operation is 3 symbol periods.

Figure 5-10 illustrates the timing of an RX_AACK transaction in slotted operation. The acknowledgement frame is ready to transmit 3 symbol times after the reception of the last symbol of a data or MAC command frame indicated by IRQ_3. The transmission of the acknowledgement frame is initiated by the microcontroller with the rising edge of pin 11 (SLP_TR) and starts t_{TR10} later.

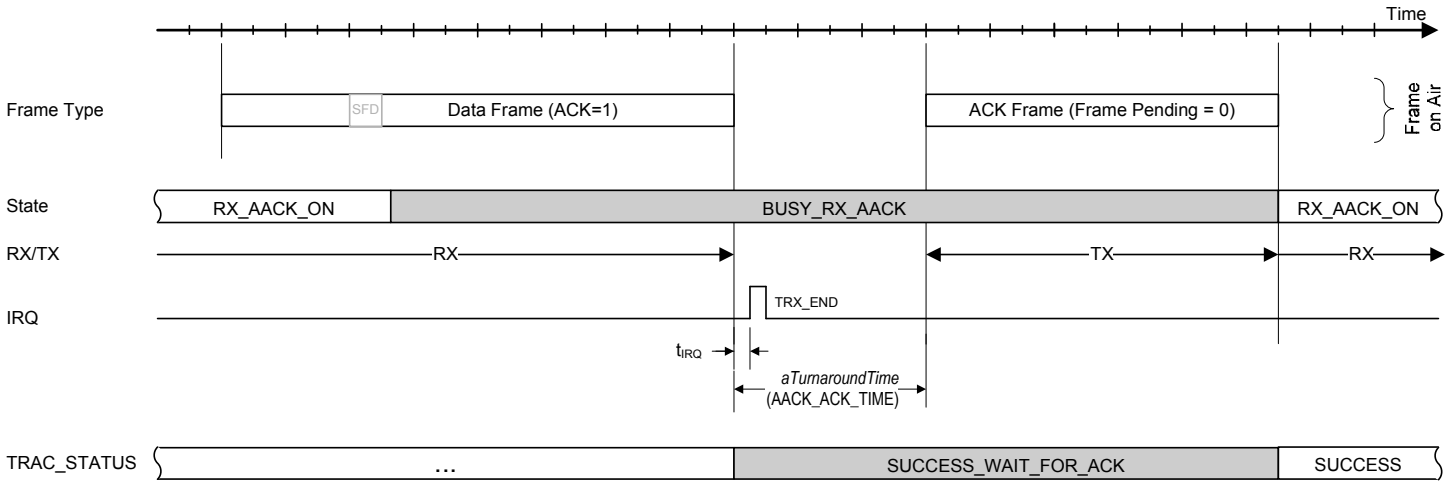
Figure 5-10. Exemplary Timing of an RX_AACK Transaction for Slotted Operation



5.2.3.6 Timing

A general timing example of an RX_AACK transaction is shown in Figure 5-11. In this example, a data frame with an ACK request is received. The AT86RF212 changes to state BUSY_RX_AACK after SFD detection. The completion of the frame reception is indicated by a TRX_END interrupt. The interrupts IRQ_2 (TX_START) and IRQ_5 (AMI) are disabled in this example. The ACK frame is automatically transmitted after *aTurnaroundTime* (12 symbols), assuming default acknowledgment frame start timing. The interrupt latency t_9 is specified in section 10.4.

Figure 5-11. Exemplary Timing of an RX_AACK Transaction



5.2.4 TX_ARET_ON – Transmit with Automatic Retry and CSMA-CA Retry

Overview

The TX_ARET Extended Operating Mode supports the frame transmission process as defined by IEEE 802.15.4-2006. It is invoked as described in section 5.2.1 by writing TX_ARET_ON to register subfield TRX_CMD (register 0x02, TRX_STATE).

If a transmission is initiated in TX_ARET mode, the AT86RF212 executes the CSMA-CA algorithm as defined by IEEE 802.15.4-2006, section 7.5.1.4. If the CCA reports IDLE, the frame is transmitted from the Frame Buffer.

If an acknowledgement frame is requested, the radio transceiver checks for an ACK reply automatically. The CSMA-CA based transmission process is repeated as long as no valid acknowledgement is received or the number of frame retransmissions (MAX_FRAME_RETRIES) is exceeded.

The completion of the TX_ARET transaction is indicated by the IRQ_3 (TRX_END) interrupt, see section 5.2.5.

Description

The implemented TX_ARET algorithm is shown in Figure 5-12.

Prior to invoking TX_ARET mode, the basic configuration steps as described in section 5.2.2 shall be executed. It is further recommended to write the PSDU transmit data to the Frame Buffer in advance.

The transmit start event may either come from a rising edge on pin 11 (SLP_TR) or by writing a TX_START command to register subfield TRX_CMD (register 0x02, TRX_STATE).

If the CSMA-CA algorithm detects a busy channel, this process is repeated up to MAX_CSMA_RETRIES (register 0x2C, XAH_CTRL_0). In case that CSMA-CA does not detect a clear channel after MAX_CSMA_RETRIES, it aborts the TX_ARET transaction, issues interrupt IRQ_3 (TRX_END), and returns CHANNEL_ACCESS_FAILURE in register bits TRAC_STATUS (register 0x02, TRX_STATE).

During transmission of a frame, the radio transceiver parses bit 5 (ACK Request) of the MAC header (MHR) frame to check whether an ACK reply is expected.

If no ACK is expected, the radio transceiver issues IRQ_3 (TRX_END) directly after the frame transmission has been completed. The register bits TRAC_STATUS (register 0x02, TRX_STATE) are set to SUCCESS.

If an ACK is expected, after transmission the radio transceiver automatically switches to receive mode waiting for a valid ACK reply (i.e. matching sequence number and correct FCS). After receiving a valid ACK frame, the “Frame Pending” subfield of this frame is parsed and the status register bits TRAC_STATUS are updated to SUCCESS or SUCCESS_DATA_PENDING accordingly, refer to Table 5-15. At the same time, the entire TX_ARET transaction is terminated and interrupt IRQ_3 (TRX_END) is issued.

If no valid ACK is received within the timeout period (refer to section 5.2.4.1), the radio transceiver retries the entire transaction (CSMA-CA based frame transmission) until the maximum number of frame retransmissions is exceeded, see register bits MAX_FRAME_RETRIES (register 0x2C, XAH_CTRL_0). In that case, the TRAC_STATUS is set to NO_ACK, the TX_ARET transaction is terminated, and interrupt IRQ_3 (TRX_END) is issued.

Table 5-15 summarizes the Extended Operating Mode result codes in register subfield TRAC_STATUS (register 0x02, TRX_STATE) with respect to the TX_ARET transaction.

Figure 5-12. Flow Diagram of TX_ARET

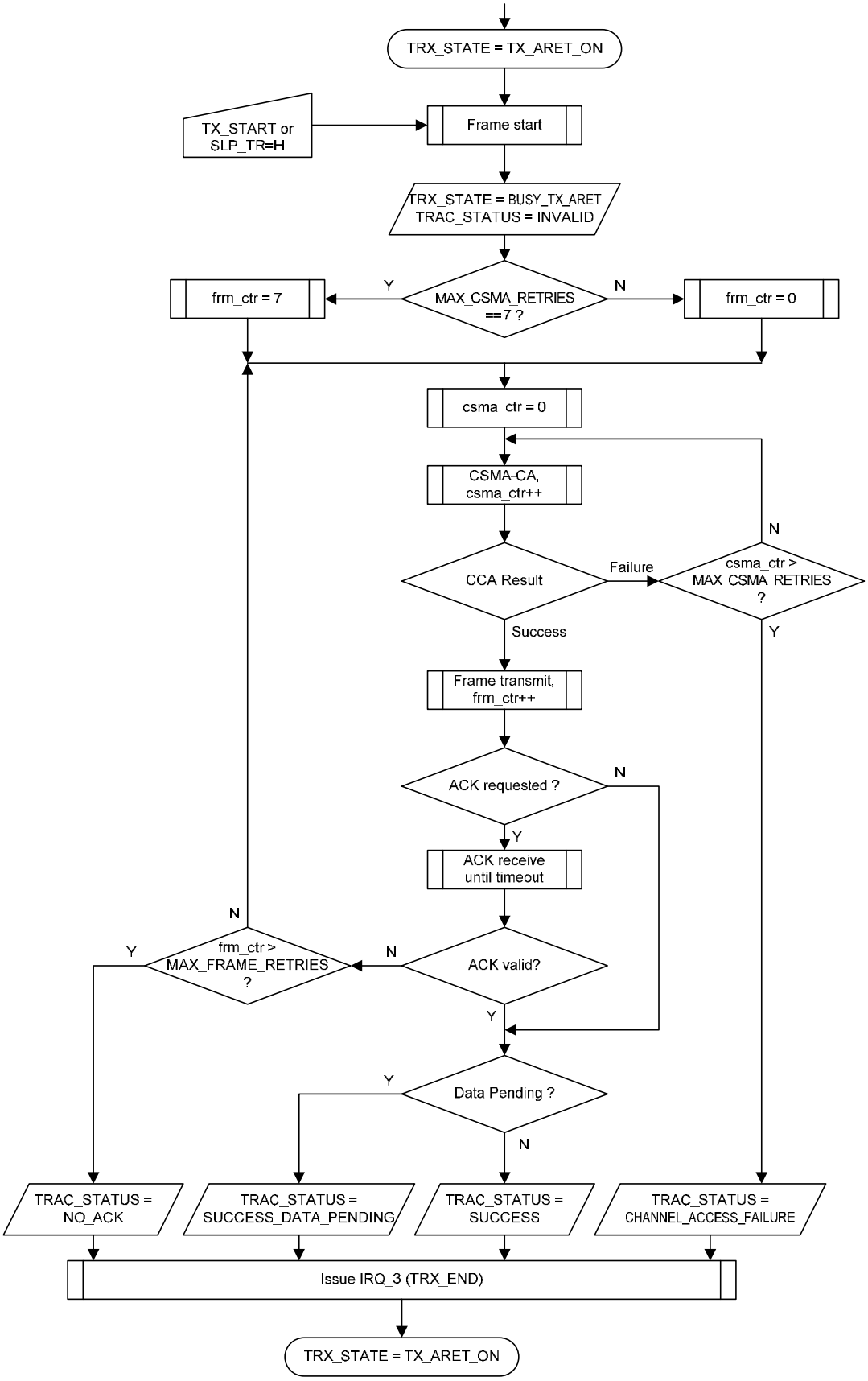


Table 5-15. TX_ARET Interpretation of TRAC_STATUS Register Bits

Value	Name	Description
0	SUCCESS	The transaction was responded by a valid ACK, or, if no ACK is requested, after a successful frame transmission.
1	SUCCESS_DATA_PENDING	Equivalent to SUCCESS and indicating that the “Frame Pending” bit (see section 6.1.2.2) of the received acknowledgment frame was set.
3	CHANNEL_ACCESS_FAILURE	Channel is still busy after MAX_CSMA_RETRIES of CSMA-CA.
5	NO_ACK	No acknowledgement frame was received during all retry attempts.
7	INVALID	Entering TX_ARET mode until IRQ_3 (TRX_END).

A value of MAX_CSMA_RETRIES = 7 initiates an immediate TX_ARET transaction without performing CSMA-CA. This supports beacon-enabled network operation. Furthermore, by ignoring the value of MAX_FRAME_RETRIES, only a single attempt is made to transmit the frame.

Note that the acknowledgment receive procedure does not overwrite the Frame Buffer content. Transmit data in the Frame Buffer is not modified during the entire TX_ARET transaction. Received frames, other than the expected ACK frame, are discarded automatically.

5.2.4.1 Acknowledgment Timeout

If an acknowledgment (ACK) frame is expected after frame transmission, the AT86RF212 sets a timeout until which a valid ACK frame must have been arrived. This timeout *macAckWaitDuration* is defined according to [2] as follows:

macAckWaitDuration [symbol periods] =

aUnitBackoffPeriod + aTurnaroundTime + phySHRDuration + 6 · phySymbolsPerOctet

where *6* represents the number of PHY header octets plus the number of PSDU octets in an acknowledgment frame.

Specifically for the implemented PHY Modes (see section 7.1), this formula results in the following values:

- BPSK: *macAckWaitDuration* = 120 symbol periods
- O-QPSK: *macAckWaitDuration* = 54 symbol periods

Note that for any PHY Mode the unit “symbol period” refers to the symbol duration of the appropriate synchronization header; see section 7.1.3 for further information regarding symbol period.

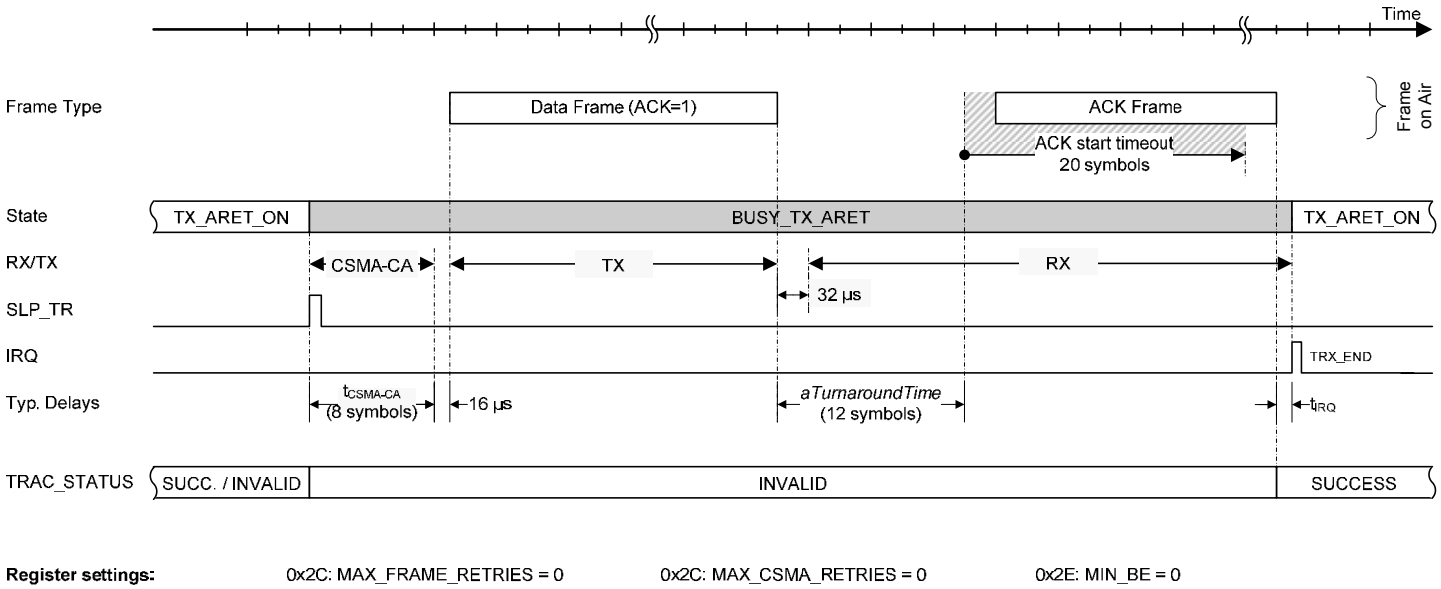
5.2.4.2 Timing

A timing example of a TX_ARET transaction is shown in Figure 5-13. In the example shown, a data frame with an acknowledgment request is to be transmitted. The frame transmission is started by pin 11 (SLP_TR). As MIN_BE is set to zero, the initial CSMA-CA backoff period has length zero too. Thus, the CSMA-CA duration time $t_{CSMA-CA}$ only consists of 8 symbols of CCA measurement period. If CCA returns IDLE (assumed here), the frame is transmitted.

After that, the AT86RF212 switches to receive mode and expects an acknowledgement response, which is indicated by register subfield TRAC_STATUS (register 0x02, TRX_STATE) set to SUCCESS_WAIT_FOR_ACK. After a period of *aTurnaroundTime* + *aUnitBackoff*, the transmission of the ACK frame must have started. During the entire transaction, including frame transmit, wait for ACK, and ACK receive, the radio transceiver status register TRX_STATUS (register 0x01, TRX_STATUS) signals BUSY_TX_ARET.

A successful reception of the acknowledgment frame is indicated by interrupt IRQ_3 (TRX_END). The status register TRX_STATUS (register 0x01, TRX_STATUS) changes back to TX_ARET_ON. At the same time, register TRAC_STATUS changes to SUCCESS or to SUCCESS_DATA_PENDING if the “Frame Pending” subfield of the acknowledgment frame was set to 1.

Figure 5-13. Exemplary Timing of a TX_ARET Transaction (without Pending Data Bit set in ACK Frame)



Register settings: 0x2C: MAX_FRAME_RETRIES = 0 0x2C: MAX_CSMA_RETRIES = 0 0x2E: MIN_BE = 0

5.2.5 Interrupt Handling

The interrupt handling in the Extended Operating Mode is similar to the Basic Operating Mode. Interrupts can be enabled by setting the appropriate bit in register 0x0E (IRQ_MASK).

For RX_AACK and TX_ARET, the following interrupts inform about the status of a frame reception and transmission:

- IRQ_2 (RX_START)
- IRQ_3 (TRX_END)
- IRQ_5 (AMI)

For RX_AACK mode, it is recommended to enable only interrupt IRQ_3 (TRX_END). This interrupt is issued only if the Frame Filter (see section 6.2) reports a matching address and the FCS is valid (see section 6.3). The usage of other interrupts is optional.

On reception of a frame, the RX_START interrupt indicates the detection of a correct synchronization header (SHR) and a non-zero PHY header (PHR). This interrupt is issued after the PHR. AMI indicates address match, refer to filter rules in section 6.2.

The TRX_END interrupt is always generated after completing a TX_ARET transaction. After that, the return code can be read from subfield TRAC_STATUS (register 0x02, TRX_STATE).

Several interrupts are automatically suppressed by the radio transceiver during TX_ARET transaction. In contrast to section 6.6, the CCA algorithm (part of CSMA-CA) does not generate interrupt IRQ_4 (CCA_ED_DONE). Furthermore, the interrupts RX_START and AMI are not generated during the TX_ARET acknowledgment receive process.

5.2.6 Register Description

Register Summary

The following registers control the Extended Operating Mode.

Table 5-16. Extended Operating Mode Register Summary

Reg.-Addr.	Register Name	Description
0x01	TRX_STATUS	Radio transceiver status, CCA result
0x02	TRX_STATE	Radio transceiver state control, TX_ARET status
0x04	TRX_CTRL_1	TX_AUTO_CRC_ON
0x08	PHY_CC_CCA	CCA mode control, see section 6.6.6
0x09	CCA_THRES	CCA ED threshold settings, see section 6.6.6
0x17	XAH_CTRL_1	RX_AACK control
0x20 … 0x2B		Frame Filter configuration – Short address, PAN ID, and IEEE address – See section 6.2.3
0x2C	XAH_CTRL_0	TX_ARET control, retries value control
0x2D	CSMA_SEED_0	CSMA-CA seed value
0x2E	CSMA_SEED_1	CSMA-CA seed value, RX_AACK control
0x2F	CSMA_BE	CSMA-CA backoff exponent control

Register 0x01 (TRX_STATUS):

The read-only register TRX_STATUS provides the current state of the radio transceiver. A state change is initiated by writing a state transition command to register bits TRX_CMD (register 0x02, TRX_STATE).

Table 5-17. Register 0x01 (TRX_STATUS)

Bit	7	6	5	4
Name	CCA_DONE	CCA_STATUS	Reserved	TRX_STATUS[4]
Read/Write	R	R	R	R
Reset Value	0	0	0	0

Bit	3	2	1	0
Name	TRX_STATUS[3]	TRX_STATUS[2]	TRX_STATUS[1]	TRX_STATUS[0]
Read/Write	R	R	R	R
Reset Value	0	0	0	0

- **Bit 7:6 – CCA_DONE, CCA_STATUS**

Refer to section 6.6.6; not updated in Extended Operating Mode.

- **Bit 5 – Reserved**
- **Bit 4:0 – TRX_STATUS**

The register bits TRX_STATUS signal the current radio transceiver status.

Table 5-18. Radio Transceiver Status

Register Bits	Value	State Description
TRX_STATUS	0x00	P_ON
	0x01	BUSY_RX
	0x02	BUSY_TX
	0x06	RX_ON
	0x08	TRX_OFF (CLK Mode)
	0x09	PLL_ON (TX_ON)
	0x0F (1)	SLEEP
	0x11	BUSY_RX_AACK
	0x12	BUSY_TX_ARET
	0x16	RX_AACK_ON
	0x19	TX_ARET_ON
	0x1C	RX_ON_NOCLK
	0x1D	RX_AACK_ON_NOCLK
	0x1E	BUSY_RX_AACK_NOCLK
	0x1F (2)	STATE_TRANSITION_IN_PROGRESS
		All other values are reserved.

Notes: 1. Registers are not accessible in SLEEP state.

2. Do not try to initiate a further state change while the radio transceiver is in STATE_TRANSITION_IN_PROGRESS state.

Register 0x02 (TRX_STATE):

The AT86RF212 radio transceiver states are controlled via register TRX_STATE using register bits TRX_CMD. A successful state transition shall be confirmed by reading register bits TRX_STATUS (register 0x01, TRX_STATUS).

The read-only register bits TRAC_STATUS indicate the status or result of an Extended Operating Mode transaction.

Table 5-19. Register 0x02 (TRX_STATE)

Bit	7	6	5	4
Name	TRAC_STATUS[2]	TRAC_STATUS[1]	TRAC_STATUS[0]	TRX_CMD[4]
Read/Write	R	R	R	R/W
Reset Value	0	0	0	0

Bit	3	2	1	0
Name	TRX_CMD[3]	TRX_CMD[2]	TRX_CMD[1]	TRX_CMD[0]
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0

- **Bit 7:5 – TRAC_STATUS**

The status of the RX_AACK and TX_ARET procedures is indicated by register bits TRAC_STATUS. Details of the algorithms and a description of the status information are given in sections 5.2.3 and 5.2.4.

Table 5-20. TRAC_STATUS Transaction Status

Register Bits	Value	Description	RX_AACK	TX_ARET
TRAC_STATUS	0 (1)	SUCCESS	X	X
	1	SUCCESS_DATA_PENDING		X
	2	SUCCESS_WAIT_FOR_ACK	X	
	3	CHANNEL_ACCESS_FAILURE		X
	5	NO_ACK		X
	7 (1)	INVALID	X	X
		All other values are reserved.		

Note: 1. Even though the reset value for register bits TRAC_STATUS is 0, the RX_AACK and TX_ARET procedures set the register bits to TRAC_STATUS = 7 (INVALID) when it is started.

- **Bit 4:0 – TRX_CMD**

A write access to register bits TRX_CMD initiates a radio transceiver state transition.

Table 5-21. State Control Register

Register Bits	Value	State Description
TRX_CMD	0x00	NOP
	0x02	TX_START
	0x03	FORCE_TRX_OFF
	0x04 (1)	FORCE_PLL_ON
	0x06	RX_ON
	0x08	TRX_OFF (CLK Mode)
	0x09	PLL_ON (TX_ON)
	0x16	RX_AACK_ON
	0x19	TX_ARET_ON
		All other values are reserved and mapped to NOP.

Note: 1. FORCE_PLL_ON is not valid for states SLEEP, P_ON, RESET, and all *_NOCLK states, as well as STATE_TRANSITION_IN_PROGRESS towards these states.

Register 0x04 (TRX_CTRL_1):

The TRX_CTRL_1 register is a multi-purpose register to control various operating modes and settings of the radio transceiver.

Table 5-22. Register 0x04 (TRX_CTRL_1)

Bit	7	6	5	4
Name	PA_EXT_EN	IRQ_2_EXT_EN	TX_AUTO_CRC_ON	RX_BL_CTRL
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	1	0

Bit	3	2	1	0
Name	SPI_CMD_MODE	SPI_CMD_MODE	IRQ_MASK_MODE	IRQ_POLARITY
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0

- **Bit 7 – PA_EXT_EN**

Refer to section 9.4.3.

- **Bit 6 – IRQ_2_EXT_EN**

Refer to section 9.5.2.

- **Bit 5 – TX_AUTO_CRC_ON**

If set, register bit TX_AUTO_CRC_ON enables the automatic FCS generation. For further details refer to section 6.3.

- **Bit 4 – RX_BL_CTRL**

Refer to section 9.6.2.

- **Bit 3:2 – SPI_CMD_MODE**

Refer to section 4.4.1.

- **Bit 1:0 – IRQ_MASK_MODE, IRQ_POLARITY**

Refer to section 4.7.2.

Register 0x17 (XAH_CTRL_1):

The XAH_CTRL_1 register is a control register for Extended Operating Mode.

Table 5-23. Register 0x17 (XAH_CTRL_1)

Bit	7	6	5	4
Name	Reserved	CSMA_LBT_MODE	AACK_FLTR_RES_FT	AACK_UPLD_RES_FT
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0

Bit	3	2	1	0
Name	Reserved	AACK_ACK_TIME	AACK_PROM_MODE	Reserved
Read/Write	R	R/W	R/W	R
Reset Value	0	0	0	0

- **Bit 7 – Reserved**
- **Bit 6 – CSMA_LBT_MODE**

Refer to section 6.7.3.

- **Bit 5 – AACK_FLTR_RES_FT**

This register bit shall only be set if AACK_UPLD_RES_FT = 1.

If AACK_FLTR_RES_FT = 1, reserved frame types are filtered like data frames as specified in IEEE 802.15.4-2006. Reserved frame types are explained in IEEE 802.15.4-2006, section 7.2.1.1.1. Interrupt IRQ_5 (AMI) is issued upon passing the frame filter, see section 6.2.

If AACK_FLTR_RES_FT = 0, the received reserved frame is only checked for a valid FCS.

- **Bit 4 – AACK_UPLD_RES_FT**

If AACK_UPLD_RES_FT = 1, received frames marked as reserved frames are further processed. For these frames, interrupt IRQ_3 (TRX_END) is generated if the FCS is valid.

In conjunction with the configuration bit AACK_FLTR_RES_FT = 1, these frames are handled like IEEE 802.15.4 compliant data frames during RX_AACK transaction.

Otherwise, if AACK_UPLD_RES_FT = 0, frames with a reserved frame type are blocked.

- **Bit 3 – Reserved**
- **Bit 2 – AACK_ACK_TIME**

According to IEEE 802.15.4-2006, section 7.5.6.4.2, the transmission of an acknowledgment frame shall commence 12 symbol periods (*aTurnaroundTime*) after the reception of the last symbol of a data or MAC command frame. This is achieved with the reset value of the register bit AACK_ACK_TIME.

Alternatively, if AACK_ACK_TIME = 1, the acknowledgment response time is reduced according to Table 5-24.

Table 5-24. Short ACK Response Time (AACK_ACK_TIME = 1)

PHY Mode	ACK response time [symbol periods]
BPSK-20, OQPSK-{100,200,400}	2
BPSK-40, OQPSK-{250,500,1000}	3

The reduced ACK response time is particularly useful for the High Data Rate Modes, refer to section 7.1.4.

- **Bit 1 – AACK_PROM_MODE**

Register bit AACK_PROM_MODE enables the promiscuous mode within the RX_AACK mode; refer to IEEE 802.15.4-2006, section 7.5.6.5.

If this bit is set, incoming frames with a valid PHR generate interrupt IRQ_3 (TRX_END), even if the third level filter rules do not match or the FCS is not valid. However, register bit RX_CRC_VALID (register 0x06) is set accordingly.

If a frame passes the third level filter rules, an acknowledgement frame is generated and transmitted unless disabled by register bit AACK_DIS_ACK (register 0x2E, CSMA_SEED_1).

- **Bit 0 – Reserved**

Register 0x2C (XAH_CTRL_0):

Register 0x2C (XAH_CTRL_0) is a control register for Extended Operating Mode.

Table 5-25. Register 0x2C (XAH_CTRL_0)

Bit	7	6	5	4
Name	MAX_FRAME_RETRIES[3:0]			
Read/Write	R/W			
Reset Value	0	0	1	1

Bit	3	2	1	0
Name	MAX_CSMA_RETRIES[2:0]			SLOTTED_OPERATION
Read/Write	R/W			R/W
Reset Value	1	0	0	0

- **Bit 7:4 – MAX_FRAME_RETRIES**

The setting of MAX_FRAME_RETRIES specifies the number of attempts in TX_ARET mode to automatically retransmit a frame when it was not acknowledged by the recipient.

- **Bit 3:1 – MAX_CSMA_RETRIES**

MAX_CSMA_RETRIES specifies the number of retries in TX_ARET mode to repeat the CSMA-CA procedure before the transaction gets cancelled. According to IEEE 802.15.4, the valid range of MAX_CSMA_RETRIES is [0, 1, … , 5].

A value of MAX_CSMA_RETRIES = 7 initiates an immediate frame transmission without performing CSMA-CA. No retry is performed. This may especially be required for slotted acknowledgement operation. MAX_CSMA_RETRIES = 6 is reserved.

- **Bit 0 – SLOTTED_OPERATION**

If set, register bit SLOTTED_OPERATION enables RX_AACK acknowledgment generation in slotted operation mode, refer to section 5.2.3.5.

Using RX_AACK mode in networks operating in beacon or slotted mode (refer to IEEE 802.15.4-2006, section 5.5.1), register bit SLOTTED_OPERATION indicates that acknowledgement frames are to be sent on backoff slot boundaries (slotted acknowledgement).

If this register bit is set, the acknowledgement frame transmission is initiated by the microcontroller using the rising edge of pin 11 (SLP_TR).

Register 0x2D (CSMA_SEED_0):

The CSMA_SEED_0 register is a control register for TX_ARET and contains a part of the CSMA seed for the CSMA-CA algorithm.

Table 5-26. Register 0x2D (CSMA_SEED_0)

Bit	7	6	5	4	3	2	1	0
Name	CSMA_SEED[7:0]							
Read/Write	R/W							
Reset Value	1	1	1	0	1	0	1	0

- **Bit 7:0 – CSMA_SEED**

This register contains the lower 8 bit of the CSMA_SEED, i.e. bits [7:0]. The higher 3 bit are part of register bits CSMA_SEED_1 (register 0x2E, CSMA_SEED_1). CSMA_SEED is the seed for the random number generation that determines the length of the backoff period in the CSMA-CA algorithm.

It is recommended to initialize registers CSMA_SEED with random values. This can be done using register bits RND_VALUE (register 0x06, PHY_RSSI), refer to section 9.2.

The content of register CSMA_SEED_0/1 initializes the TX_ARET random backoff generator after wakeup from SLEEP state. It is recommended to reinitialize both registers before every SLEEP state with a random value.

Register 0x2E (CSMA_SEED_1):

The CSMA_SEED_1 register contains a part of the CSMA seed for the CSMA-CA algorithm, as well as control bits for the Frame Filter and RX_AACK transaction.

Table 5-27. Register 0x2E (CSMA_SEED_1)

Bit	7	6	5	4
Name	AACK_FVN_MODE	AACK_FVN_MODE	AACK_SET_PD	AACK_DIS_ACK
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	1	0	0
Bit	3	2	1	0
Name	AACK_I_AM_COORD	CSMA_SEED[10]	CSMA_SEED[9]	CSMA_SEED[8]
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	1	0

- **Bit 7:6 – AACK_FVN_MODE**

The frame control field of the MAC header (MHR) contains a frame version subfield. The setting of AACK_FVN_MODE specifies the frame filtering and acknowledgement behavior of the AT86RF212. According to the content of these register bits, the radio transceiver passes frames with a specific frame version number, number group, or independent of the frame version number.

Thus, the register bit AACK_FVN_MODE defines the maximum acceptable frame version. Received frames with a higher frame version number than configured do not pass the Frame Filter and thus are not acknowledged.

Table 5-28. Frame Version Subfield dependent Frame Acknowledgment

Register Bits	Value	Description
AACK_FVN_MODE	0	Acknowledge frames with version number 0
	1	Acknowledge frames with version number 0 or 1
	2	Acknowledge frames with version number 0 or 1 or 2
	3	Acknowledge independent of frame version number

Note that the frame version field of the acknowledgment frame is set to 0x00 according to IEEE 802.15.4-2006, section 7.2.2.3.1 “Acknowledgment frame MHR fields”.

- **Bit 5 – AACK_SET_PD**

The content of AACK_SET_PD bit is copied into the “Frame Pending” subfield of the acknowledgment frame if the ACK is the answer to a data request MAC command frame.

In addition, if register bits AACK_FVN_MODE (register 0x2E, CSMA_SEED_1) are configured to accept frames with a frame version other than 0 or 1, the content of register bit AACK_SET_PD is also copied into the “Frame Pending” subfield of the acknowledgment frame for any MAC command frame with a frame version of 2 or 3 that have the security enabled subfield set to 1. This is done in the assumption that a future version of the standard [2] might change the length or structure of the auxiliary security header, so it would not possible to safely detect whether the MAC command frame is actually a data request command or not.

- **Bit 4 – AACK_DIS_ACK**

If this bit is set, no acknowledgment frames are transmitted in RX_AACK Extended Operating Mode, even if requested.

- **Bit 3 – AACK_I_AM_COORD**

This register bit has to be set if the node is a PAN coordinator. It is used for frame filtering in RX_AACK mode.

If I_AM_COORD = 1 and if only source addressing fields are included in a data or MAC command frame, the frame shall be accepted only if the device is the PAN coordinator and the source PAN identifier matches *macPANId*. For details, refer to IEEE 802.15.4-2006, section 7.5.6.2 (third-level filter rule 6).

- **Bit 2:0 – CSMA_SEED**

These register bits are the higher 3 bit of the CSMA_SEED, i.e. bits [10:8]. The lower part is in register 0x2D (CSMA_SEED_0), see register CSMA_SEED_0 for details.

Register 0x2F (CSMA_BE):

Table 5-29. Register 0x2F (CSMA_BE)

Bit	7	6	5	4
Name	MAX_BE[3]	MAX_BE[2]	MAX_BE[1]	MAX_BE[0]
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	1	0	1
Bit	3	2	1	0
Name	MIN_BE[3]	MIN_BE[2]	MIN_BE[1]	MIN_BE[0]
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	1	1

- **Bit 7:4 – MAX_BE**

Register bits MAX_BE define the maximum value of the backoff exponent in the CSMA-CA algorithm. It equals *macMaxBE*; refer to section 7.5.1.4 of [2]. Valid values are [4'd8, 4'd7, … , 4'd3].

- **Bit 3:0 – MIN_BE**

Register bits MIN_BE define the minimum value of the backoff exponent in the CSMA-CA algorithm. It equals to *macMinBE*; refer to section 7.5.1.4 of [2]. Valid values are [MAX_BE, (MAX_BE – 1), … , 4'd0].

Note

- If MIN_BE = 0 and MAX_BE = 0, the CCA backoff period is always set to 0.

6 Functional Description

6.1 Introduction – IEEE 802.15.4-2006 Frame Format

Figure 6-1 provides an overview of the physical layer (PHY) frame structure as defined by the IEEE 802.15.4-2006 standard. Figure 6-2 shows the medium access control layer (MAC) frame structure.

Figure 6-1. IEEE 802.15.4 Frame Format – PHY Layer Frame Structure

<table>
<tr><td colspan="4">PHY Protocol Data Unit (PPDU)</td></tr>
<tr><td>Preamble Sequence</td><td>SFD</td><td>Frame Length</td><td>PHY Payload</td></tr>
<tr><td colspan="2">5 octets
Synchronization Header (SHR)</td><td>1 octet
(PHR)</td><td>max. 127 octets PHY Payload
PHY Service Data Unit (PSDU)</td></tr>
<tr><td colspan="3"></td><td>MAC Protocol Data Unit (MPDU)</td></tr>
</table>

6.1.1 PHY Protocol Data Unit (PPDU)

6.1.1.1 Synchronization Header (SHR)

The SHR consists of a four-octet preamble field (all zero), followed by a single octet start-of-frame delimiter (SFD). During transmit, the SHR is automatically generated by the AT86RF212, thus the Frame Buffer shall contain PHR and PSDU only, see section 4.3.2.

The transmission of the SHR requires 40 symbols for a transmission with BPSK modulation and 10 symbols for a transmission with O-QPSK modulation. Table 6-1 illustrates the SHR duration depending on the selected data rate, see also section 10.5.

As the SPI data rate is usually higher than the over-the-air data rate, this allows the microcontroller to initiate a transmission before the frame buffer write access is completed.

During frame reception, the SHR is used for synchronization purposes. The matching SFD determines the beginning of the PHR and the following PSDU payload data.

6.1.1.2 PHY Header (PHR)

The PHY header is a single octet following the SHR. The least significant 7 bits denote the frame length of the following PSDU, while the most significant bit of that octet is reserved and shall be set to 0 for IEEE 802.15.4 compliant frames. Even though the MSB is reserved, AT86RF212 is able to transmit and receive this bit.

In transmit mode, the PHR needs to be supplied as the first octet during Frame Buffer write access, see section 4.3.2.

In receive mode, the PHR is returned as the first octet during Frame Buffer read access, see section 4.3.2.

6.1.1.3 PHY Payload (PHY Service Data Unit, PSDU)

The PSDU has a variable length between one and 127 octets. The PSDU contains the MAC protocol data unit (MPDU), where the last two octets are used for the Frame Check Sequence (FCS), see section 6.3.

6.1.1.4 Timing Summary

Table 6-1 shows timing information for the above mentioned frame structure depending on the selected data rate.

Table 6-1. PPDU Timing

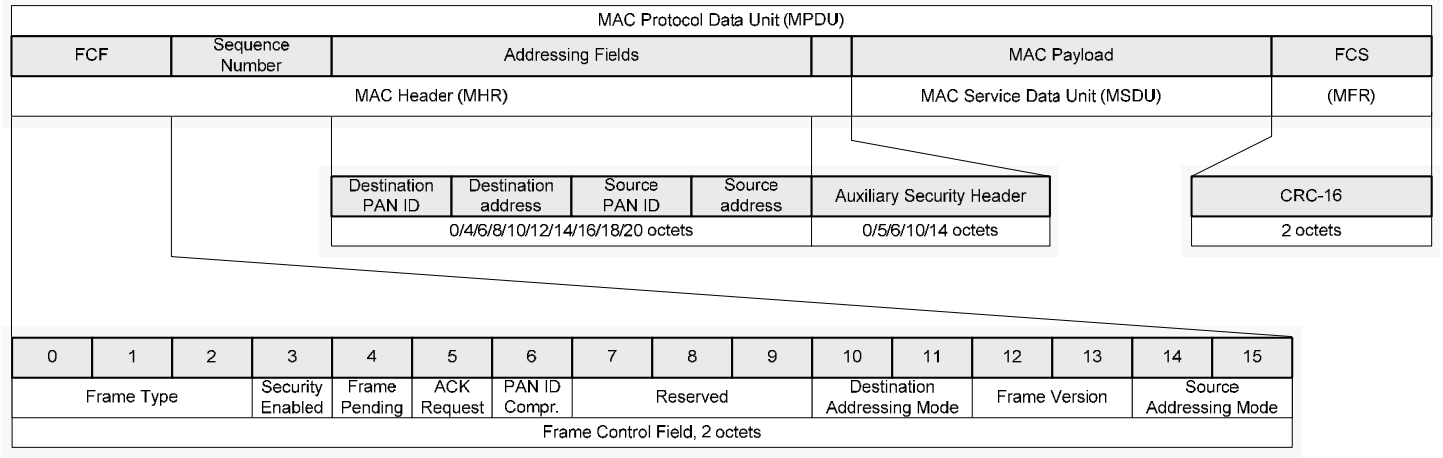
PHY Mode	PSDU Bit Rate [kbit/s]	Header Bit Rate [kbit/s]	Duration		
			SHR [µs]	PHR [µs]	Max. PSDU [ms]
BPSK (1)	20	20	2000	400	50.8
	40	40	1000	200	25.4
O-QPSK (1)	100	100	300	80	10.16
	250	250	160	32	4.064
O-QPSK (2)	200	100	300	80	5.08
	400	100	300	80	2.54
	500	250	160	32	2.032
	1000	250	160	32	1.016

Notes: 1. Compliant to IEEE 802.15.4-2006 [2]
2. High Data Rate Modes, see section 7.1.4

6.1.2 MAC Protocol Data Unit (MPDU)

Figure 6-2 shows the frame structure of the MAC layer.

Figure 6-2. IEEE 802.15.4-2006 Frame Format – MAC Layer Frame Structure



6.1.2.1 MAC Header (MHR)

The MAC header consists of the Frame Control Field (FCF), a sequence number, and the addressing fields of variable length.

6.1.2.2 Frame Control Field (FCF)

The FCF occupies the first two octets of the MPDU.

Bits [2:0] describe the “Frame Type”. Table 6-2 summarizes frame types defined by [2], section 7.2.1.1.1.

Table 6-2. Frame Type Field

Frame Type Value		Description
b_2 b_1 b_0	Value	
000	0	Beacon
001	1	Data
010	2	Acknowledge
011	3	MAC command
100 – 111	4 – 7	Reserved

These bits are used for frame filtering by the third level filter rules, refer to section 6.2.

Bit 3 indicates whether security processing applies to this frame. This field is evaluated by the Frame Filter.

Bit 4 is the “Frame Pending” subfield. This field can be set in an acknowledgment frame to indicate to the node receiving the acknowledgment frame that the node sent the acknowledgment frame has more data to send.

Bit 5 forms the “Acknowledgment Request” subfield. If this bit is set within a data or MAC command frame that is not broadcast, the recipient shall acknowledge the reception of the frame within the time specified by IEEE 802.15.4, i.e. within 12 symbols for nonbeacon-enabled networks.

Bit 6, the “PAN ID Compression” subfield, indicates that in a frame where both the destination and source addresses are present, the PAN ID is omitted from the source addressing field. This bit is evaluated by the Frame Filter of the AT86RF212.

Bits [9:7] are reserved.

Bits [11:10]: The “Destination Addressing Mode” subfield describes the format of the destination address of the frame. The values of the address modes are summarized in Table 6-3 according to IEEE 802.15.4.

Table 6-3. Destination and Source Addressing Mode

Addressing Mode Value		Description
b_{11} b_{10}	Value	
00	0	PAN identifier and address fields are not present
01	1	Reserved
10	2	Address field contains a 16-bit short address
11	3	Address field contains a 64-bit extended address

If the destination address mode is either 2 or 3, i.e. if the destination address is present, the addressing field consists of a 16-bit PAN ID first, followed by either the 16-bit or 64-bit address as defined by the mode.

Bits [13:12]: The “Frame Version” subfield specifies the version number corresponding to the frame, see Table 6-4. These bits are reserved in IEEE-802.15.4-2003.

This subfield shall be set to 0x00 to indicate a frame compatible with IEEE 802.15.4-2003; it shall be set to 0x01 to indicate an IEEE 802.15.4-2006 frame. All other subfield values shall be reserved for future use. See [2], section 7.2.3, for details on frame compatibility.

Table 6-4. Frame Version Field

Frame Version Value		Description
b_{13} b_{12}	Value	
00	0	Frames are compatible with IEEE 802.15.4-2003
01	1	Frames are compatible with IEEE 802.15.4-2006
10	2	Reserved
11	3	Reserved

Bits [15:14] form the “Source Addressing Mode” subfield, with similar meaning as “Destination Addressing Mode”.

The addressing field description bits of the FCF (Bits 0...2, 3, 6, 10…15) affect the AT86RF212 Frame Filter, see section 6.2.

6.1.2.3 Frame Compatibility between IEEE 802.15.4 Rev. 2003 and 2006

All unsecured frames according to IEEE 802.15.4-2006 are compatible with unsecured frames compliant with IEEE 802.15.4-2003, with two exceptions: a coordinator realignment command frame with the Channel Page field present (see [2], section 7.3.8) and any frame with a MAC Payload field larger than *aMaxMACSafePayloadSize* octets.

Compatibility for secured frames is shown in Table 6-5, which identifies the security operating modes for IEEE 802.15.4-2003 and IEEE 802.15.4-2006.

Table 6-5. Frame Compatibility

Frame Control Field Bit Assignments		Description
Security Enabled b_3	Frame Version b_{13} b_{12}	
0	00	No security. Frames are compatible between IEEE 802.15.4-2003 and IEEE 802.15.4-2006.
0	01	No security. Frames are not compatible between IEEE 802.15.4-2003 and IEEE 802.15.4-2006.
1	00	Secured frame formatted according to IEEE 802.15.4-2003. This type of frame is not supported in IEEE 802.15.4-2006.
1	01	Secured frame formatted according to IEEE 802.15.4-2006

6.1.2.4 Sequence Number

The one-octet sequence number following the FCF identifies a particular frame, so that duplicated frame transmissions can be detected. While operating in RX_AACK states, the received frame content of this field is copied into the acknowledgment frame.

6.1.2.5 Addressing Fields

The addressing field carries several addresses used for address matching indication. The destination address (if present) is always first, followed by the source address (if present). Each address field consists of the PAN ID and a device address. If both addresses are present and the “PAN ID compression” subfield in the FCF is set to one, the source PAN ID is omitted.

Note that in addition to these general rules, IEEE 802.15.4 further restricts the valid address combinations for the different MAC frame types. For example, the situation where both addresses are omitted (source addressing mode = 0 and destination addressing mode = 0) is only allowed for acknowledgment frames. The Frame Filter in the AT86RF212 has been designed to apply to IEEE 802.15.4 compliant frames. It can be configured to handle other frame formats and exceptions.

6.1.2.6 Auxiliary Security Header

The Auxiliary Security Header terminates the MHR. This field has a variable length and specifies information required for security processing, including how the frame is actually protected (security level) and which keying material from the MAC security PIB is used (see [2], section 7.6.1). This field shall be present only if the Security Enabled subfield b3 (see section 6.1.2.3) is set to one. For details on formatting, see section 7.6.2 of [2].

6.1.2.7 MAC Service Data Unit (MSDU)

This is the actual MAC payload. It is usually structured according to the individual frame type descriptions in IEEE 802.15.4 standard.

6.1.2.8 MAC Footer (MFR)

The MAC footer consists of a two-octet Frame Checksum (FCS). For details, refer to section 6.3.

6.2 Frame Filter

Frame Filtering is a procedure that evaluates whether or not a received frame matches predefined criteria, like source or destination address or frame types. A filtering procedure as described in IEEE 802.15.4-2006 (section 7.5.6.2, third level of filtering) is applied to the frame to accept a received frame and to generate the address match interrupt IRQ_5 (AMI).

The AT86RF212 Frame Filter passes only frames that satisfy all of the following requirements/rules (quote from IEEE 802.15.4-2006, section 7.5.6.2):

1. The Frame Type subfield shall not contain a reserved frame type.
2. The Frame Version subfield shall not contain a reserved value.
3. If a destination PAN identifier is included in the frame, it shall match *macPANId* or shall be the broadcast PAN identifier (0xFFFF).
4. If a short destination address is included in the frame, it shall match either *macShortAddress* or the broadcast address (0xFFFF). Otherwise, if an extended destination address is included in the frame, it shall match *aExtendedAddress*.
5. If the frame type indicates that the frame is a beacon frame, the source PAN identifier shall match *macPANId* unless *macPANId* is equal to 0xffff, in which case the beacon frame shall be accepted regardless of the source PAN identifier.
6. If only source addressing fields are included in a data or MAC command frame, the frame shall be accepted only if the device is the PAN coordinator and the source PAN identifier matches *macPANId*.

Moreover the AT86RF212 has two additional requirements:

7. The frame type shall indicate that the frame is not an acknowledgment (ACK) frame.
8. At least one address field must be configured.

Address matching, indicated by interrupt IRQ_5 (AMI), is furthermore controlled by the FCF of a received frame according to the following rule: If Destination Addressing Mode is 0/1 and Source Addressing Mode is 0 (see section 6.1.2.2), no interrupt IRQ_5 is generated. This causes that no acknowledgement frame is announced.

For backward compatibility with IEEE 802.15.4-2003, the third level filter rule 2 (Frame Version) can be disabled by register bits AACK_FVN_MODE (register 0x2E, CSMA_SEED_1).

Frame filtering is available in Extended and Basic Operating Modes. A frame that passes the Frame Filter generates the interrupt IRQ_5 (AMI) if not masked.

Notes

- Filter rule 1 is affected by register bits AACK_FLTR_RES_FT and AACK_UPLD_RES_FT, see section 6.2.3.
- Filter rule 2 is affected by register bits AACK_FVN_MODE, see section 6.2.3.

6.2.1 Configuration

The Frame Filter is configured by setting the appropriate address variables and several additional properties as described in Table 6-6.

Table 6-6. Frame Filter Configuration

Register Address	Register Bits	Name	Description
0x20,0x21 0x22,0x23 0x24 … 0x2B	7:0	SHORT_ADDR_0/1 PAN_ADDR_0/1 IEEE_ADDR_0 … IEEE_ADDR_7	Set *macShortAddress*, *macPANId* , and *aExtendedAddress* as described in [2]
0x17	1	AACK_PROM_MODE	*0:* Disable promiscuous mode *1*: Enable promiscuous mode
0x17	4	AACK_UPLD_RES_FT	*0:* Disable reserved frame type reception *1*: Enable reserved frame type reception
0x17	5	AACK_FLTR_RES_FT	Filter reserved frame types like data frame type, see section 6.2.2 *0*: Disable *1*: Enable
0x2E	7:6	AACK_FVN_MODE	Frame acceptance criteria depending on FCF frame version number *b00*: Accept only frames with version number 0, i.e. according to IEEE 802.15.4-2003 frames *b01*: Accept only frames with version number 0 or 1, i.e. frames according to IEEE 802.15.4-2006 *b10*: Accept only frames with version number 0 or 1 or 2 *b11*: Accept all frames, independent of the FCF frame version number

6.2.2 Handling of Reserved Frame Types

Reserved frame types (as described in section 5.2.3.3) are treated according to bits AACK_UPLD_RES_FT and AACK_FLTR_RES_FT of register 0x17 (XAH_CTRL_1) with three options:

1. AACK_UPLD_RES_FT = 1, AACK_FLTR_RES_FT = 0:

   Frames of reserved frame type with correct FCS are indicated by the interrupt IRQ_3 (TRX_END). No further frame filtering is applied on these frames. Interrupt IRQ_5 (AMI) is never generated and no acknowledgment is sent.

2. AACK_UPLD_RES_FT = 1, AACK_FLTR_RES_FT = 1:

   If AACK_FLTR_RES_FT = 1, any frame with a reserved frame type is treated by the RX_AACK Frame Filter as an IEEE 802.15.4 compliant data frame. This implies the generation of the interrupt IRQ_5 (AMI) upon address matches.

3. AACK_UPLD_RES_FT = 0

   Any frame with a reserved frame type is blocked.

6.2.3 Register Description

Register 0x17 (XAH_CTRL_1):

The XAH_CTRL_1 register is a control register for Extended Operating Mode.

Table 6-7. Register 0x17 (XAH_CTRL_1)

Bit	7	6	5	4
Name	Reserved	CSMA_LBT_MODE	AACK_FLTR_RES_FT	AACK_UPLD_RES_FT
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0

Bit	3	2	1	0
Name	Reserved	AACK_ACK_TIME	AACK_PROM_MODE	Reserved
Read/Write	R	R/W	R/W	R
Reset Value	0	0	0	0

- **Bit 7 – Reserved**
- **Bit 6 – CSMA_LBT_MODE**

Refer to section 6.7.3.

- **Bit 5 – AACK_FLTR_RES_FT**

This register bit shall only be set if AACK_UPLD_RES_FT = 1.

If AACK_FLTR_RES_FT = 1, any frame with a reserved frame type is treated by the RX_AACK Frame Filter as an IEEE 802.15.4 compliant data frame. If AACK_FLTR_RES_FT = 0, the received reserved frame is only checked for a valid FCS. See section 6.2.2 for details.

- **Bit 4 – AACK_UPLD_RES_FT**

If AACK_UPLD_RES_FT = 1, received frames which are identified as reserved frames will not be blocked. See section 6.2.2 for details.

- **Bit 3 – Reserved**
- **Bit 2 – AACK_ACK_TIME**

Refer to sections 5.2.3.3 and 5.2.6.

- **Bit 1 – AACK_PROM_MODE**

Refer to section 5.2.6.

- **Bit 0 – Reserved**

Register 0x20 (SHORT_ADDR_0):

This register contains the lower 8 bit of the 16-bit short address for Frame Filter address recognition, i.e. bits [7:0].

Table 6-8. Register 0x20 (SHORT_ADDR_0)

Bit	7	6	5	4	3	2	1	0
Name	SHORT_ADDRESS_0[7:0]							
Read/Write	R/W							
Reset Value	1	1	1	1	1	1	1	1

Register 0x21 (SHORT_ADDR_1):

This register contains the higher 8 bit of the 16-bit short address for Frame Filter address recognition, i.e. bits [15:8].

Table 6-9. Register 0x21 (SHORT_ADDR_1)

Bit	7	6	5	4	3	2	1	0
Name	SHORT_ADDRESS_1[7:0]							
Read/Write	R/W							
Reset Value	1	1	1	1	1	1	1	1

Register 0x22 (PAN_ID_0):

This register contains the lower 8 bit of the MAC PAN ID for Frame Filter address recognition, i.e. bits [7:0].

Table 6-10. Register 0x22 (PAN_ID_0)

Bit	7	6	5	4	3	2	1	0
Name	PAN_ID_0[7:0]							
Read/Write	R/W							
Reset Value	1	1	1	1	1	1	1	1

Register 0x23 (PAN_ID_1):

This register contains the higher 8 bit of the MAC PAN ID for Frame Filter address recognition, i.e. bits [15:8].

Table 6-11. Register 0x23 (PAN_ID_1)

Bit	7	6	5	4	3	2	1	0
Name	PAN_ID_1[7:0]							
Read/Write	R/W							
Reset Value	1	1	1	1	1	1	1	1

Register 0x24 (IEEE_ADDR_0):

This register contains bits [7:0] of the 64-bit IEEE extended address for Frame Filter address recognition.

Table 6-12. Register 0x24 (IEEE_ADDR_0)

Bit	7	6	5	4	3	2	1	0
Name	IEEE_ADDR_0[7:0]							
Read/Write	R/W							
Reset Value	0	0	0	0	0	0	0	0

Register 0x25 (IEEE_ADDR_1):

This register contains bits [15:8] of the 64-bit IEEE extended address for Frame Filter address recognition.

Table 6-13. Register 0x25 (IEEE_ADDR_1)

Bit	7	6	5	4	3	2	1	0
Name	IEEE_ADDR_1[7:0]							
Read/Write	R/W							
Reset Value	0	0	0	0	0	0	0	0

Register 0x26 (IEEE_ADDR_2):

This register contains bits [23:16] of the 64-bit IEEE extended address for Frame Filter address recognition.

Table 6-14. Register 0x26 (IEEE_ADDR_2)

Bit	7	6	5	4	3	2	1	0
Name	IEEE_ADDR_2[7:0]							
Read/Write	R/W							
Reset Value	0	0	0	0	0	0	0	0

Register 0x27 (IEEE_ADDR_3):

This register contains bits [31:24] of the 64-bit IEEE extended address for Frame Filter address recognition.

Table 6-15. Register 0x27 (IEEE_ADDR_3)

Bit	7	6	5	4	3	2	1	0
Name	IEEE_ADDR_3[7:0]							
Read/Write	R/W							
Reset Value	0	0	0	0	0	0	0	0

Register 0x28 (IEEE_ADDR_4):

This register contains bits [39:32] of the 64-bit IEEE extended address for Frame Filter address recognition.

Table 6-16. Register 0x28 (IEEE_ADDR_4)

Bit	7	6	5	4	3	2	1	0
Name	IEEE_ADDR_4[7:0]							
Read/Write	R/W							
Reset Value	0	0	0	0	0	0	0	0

Register 0x29 (IEEE_ADDR_5):

This register contains bits [47:40] of the 64-bit IEEE extended address for Frame Filter address recognition.

Table 6-17. Register 0x29 (IEEE_ADDR_5)

Bit	7	6	5	4	3	2	1	0
Name	IEEE_ADDR_5[7:0]							
Read/Write	R/W							
Reset Value	0	0	0	0	0	0	0	0

Register 0x2A (IEEE_ADDR_6):

This register contains bits [55:48] of the 64-bit IEEE extended address for Frame Filter address recognition.

Table 6-18. Register 0x2A (IEEE_ADDR_6)

Bit	7	6	5	4	3	2	1	0
Name	IEEE_ADDR_6[7:0]							
Read/Write	R/W							
Reset Value	0	0	0	0	0	0	0	0

Register 0x2B (IEEE_ADDR_7):

This register contains bits [63:56] of the 64-bit IEEE extended address for Frame Filter address recognition.

Table 6-19. Register 0x2B (IEEE_ADDR_7)

Bit	7	6	5	4	3	2	1	0
Name	IEEE_ADDR_7[7:0]							
Read/Write	R/W							
Reset Value	0	0	0	0	0	0	0	0

Register 0x2E (CSMA_SEED_1):

The CSMA_SEED_1 register is a control register for RX_AACK and contains a part of the CSMA seed for the CSMA-CA algorithm, as well as control bits for the Frame Filter and RX_AACK transaction.

Table 6-20. Register 0x2E (CSMA_SEED_1)

Bit	7	6	5	4
Name	AACK_FVN_MODE	AACK_FVN_MODE	AACK_SET_PD	AACK_DIS_ACK
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	1	0	0

Bit	3	2	1	0
Name	AACK_I_AM_COORD	CSMA_SEED_1	CSMA_SEED_1	CSMA_SEED_1
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	1	0

- **Bit 7:6 – AACK_FVN_MODE**

The frame control field of the MAC header (MHR) contains a frame version subfield. The setting of AACK_FVN_MODE specifies the frame filtering and acknowledgement behavior of the AT86RF212. According to the content of these register bits, the radio transceiver passes frames with a specific set of frame version numbers.

Thus, the register bit AACK_FVN_MODE defines the maximum acceptable frame version. Received frames with a higher frame version number than configured do not pass the Frame Filter and thus are not acknowledged.

Table 6-21. Frame Version Subfield dependent Frame Acceptance

Register Bits	Value	Description
AACK_FVN_MODE	0	Accept frames with version number 0
	1	Accept frames with version number 0 or 1
	2	Accept frames with version number 0 or 1 or 2
	3	Accept frames independent of frame version number

- **Bit 5:0**

Refer to section 5.2.6.

6.3 Frame Check Sequence (FCS)

A FCS mechanism employing a 16-bit International Telecommunication Union - Telecommunication Standardization Sector (ITU-T) cyclic redundancy check (CRC) can be used to detect errors in frames.

6.3.1 Overview

The FCS is intended for use at the MAC layer in order to detect corrupted frames. It is computed by applying an ITU-T CRC polynomial to all transmitted/received bytes following the length field (MHR and MSDU fields). The FCS has a length of 16 bit and is located in the last two octets of the PSDU.

By default, the AT86RF212 generates and inserts the FCS octets autonomously during transmit process. This behavior can be disabled by setting register bit TX_AUTO_CRC_ON = 0 (register 0x04, TRX_CTRL_1).

An automatic FCS check is always performed during frame reception.

6.3.2 CRC Calculation

The CRC polynomial used in IEEE 802.15.4 networks is defined by

$$G_{16}(x) = x^{16} + x^{12} + x^5 + 1 \ .$$

The FCS shall be calculated for transmission using the following algorithm:

Let

$$M(x) = b_0 x^{k-1} + b_1 x^{k-2} + \ldots + b_{k-2} x + b_{k-1}$$

be the polynomial representing the sequence of bits for which the checksum is to be computed. Multiply M(x) by x^{16}, giving the polynomial

$$N(x) = M(x) \cdot x^{16} .$$

Divide $N(x)$ modulo 2 by the generator polynomial $G_{16}(x)$ to obtain the remainder polynomial

$$R(x) = r_0 x^{15} + r_1 x^{14} + \ldots + r_{14} x + r_{15}$$

The FCS field is given by the coefficients of the remainder polynomial $R(x)$.

Example:

Considering a 5-octet ACK frame, the MHR field consists of

0100 0000 0000 0000 0101 0110 .

The leftmost bit (b_0) is transmitted first in time. The FCS would be

0010 0111 1001 1110 .

The leftmost bit (r_0) is transmitted first in time.

6.3.3 Automatic FCS Generation

The automatic FCS generation is enabled with register bit TX_AUTO_CRC_ON = 1. This allows the AT86RF212 to compute the FCS autonomously. For a frame with a frame length field specified as N (3 ≤ N ≤ 127), the FCS is calculated on the first N-2 octets in the Frame Buffer and the resulting FCS octets are transmitted in place of the last two octets of the Frame Buffer.

6.3.4 Automatic FCS Check

Basic and Extended Operating Modes are provided with an automatic FCS check for received frames. Register bit RX_CRC_VALID (register 0x06, PHY_RSSI) is set to 1 if the FCS of a received frame is valid. In addition, bit 7 of byte RX_STATUS is set accordingly, refer to section 4.3.2.

In Extended Operating Mode, the RX_AACK procedure does not accept a frame if the corresponding FCS is not valid, i.e. no TRX_END interrupt is issued. When operating in TX_ARET mode, the FCS of a received ACK is automatically checked. If it is not correct, the ACK is not accepted; refer to section 5.2.4 for automated retries.

6.3.5 Register Description

Register 0x04 (TRX_CTRL_1):

The TRX_CTRL_1 register is a multi-purpose register to control various operating modes and settings of the radio transceiver, see Table 6-22.

Table 6-22. Register 0x04 (TRX_CTRL_1)

Bit	7	6	5	4
Name	PA_EXT_EN	IRQ_2_EXT_EN	TX_AUTO_CRC_ON	RX_BL_CTRL
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	1	0

Bit	3	2	1	0
Name	SPI_CMD_MODE	SPI_CMD_MODE	IRQ_MASK_MODE	IRQ_POLARITY
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0

- **Bit 7 – PA_EXT_EN**

Refer to section 9.4.3.

- **Bit 6 – IRQ_2_EXT_EN**

Refer to section 9.5.2.

- **Bit 5 – TX_AUTO_CRC_ON**

The automatic FCS generation is performed with register bit TX_AUTO_CRC_ON = 1, which is the reset value.

- **Bit 4 – RX_BL_CTRL**

Refer to section 9.6.2.

- **Bit 3:2 – SPI_CMD_MODE**

Refer to section 4.4.1.

- **Bit 1:0 – IRQ_MASK_MODE, IRQ_POLARITY**

Refer to section 4.7.2.

Register 0x06 (PHY_RSSI):

The PHY_RSSI register is a multi-purpose register to indicate FCS validity, to provide random numbers, and a RSSI value.

Table 6-23. Register 0x06 (PHY_RSSI)

Bit	7	6	5	4
Name	RX_CRC_VALID	RND_VALUE[1]	RND_VALUE[0]	RSSI[4]
Read/Write	R	R	R	R
Reset Value	0	0	0	0

Bit	3	2	1	0
Name	RSSI[3]	RSSI[2]	RSSI[1]	RSSI[0]
Read/Write	R	R	R	R
Reset Value	0	0	0	0

- **Bit 7 – RX_CRC_VALID**

Reading this register bit indicates whether the last received frame has a valid FCS or not. The register bit is updated at the same time the IRQ_3 (TRX_END) is issued and remains valid until the next SHR detection. A value of “1” corresponds to a valid FCS; a value of “0” corresponds to an invalid FCS.

- **Bit 6:5 – RND_VALUE**

Refer to section 9.2.2.

- **Bit 4:0 – RSSI**

Refer to section 6.4.4.

6.4 Received Signal Strength Indicator (RSSI)

The Received Signal Strength Indicator is characterized by:

- a dynamic range of 87 dB
- a resolution of about 3 dB

6.4.1 Overview

The RSSI value indicates the received signal power in the selected channel. No attempt is made to distinguish IEEE 802.15.4 signals from others; only the received signal strength is evaluated. The RSSI provides the basis for an ED measurement, see section 6.5.

6.4.2 Reading RSSI

In Basic Operating Modes, the RSSI value is valid in any receive state and is updated at time intervals according to Table 6-24. The current RSSI value can be accessed by reading register bits RSSI of register 0x06 (PHY_RSSI).

Table 6-24. RSSI Update Interval

PHY Mode	Update Interval [µs]
BPSK-20	32
BPSK-40	24
O-QPSK	8

It is not recommended reading the RSSI value when using the Extended Operating Modes. Instead, the automatically generated ED value should be used, see section 6.5.

6.4.3 Data Interpretation

The RSSI value is a 5-bit value in a range of 0 to 28, indicating the receiver input power in steps of about 3 dB.

A RSSI value of 0 indicates a receiver input power less than or equal to RSSI_BASE_VAL [dBm], a value of 28 an input power equal to or larger than (RSSI_BASE_VAL + 87) [dBm]. The value RSSI_BASE_VAL itself depends on the PHY mode, refer to section 7.1. For typical conditions, it is shown in Table 6-25.

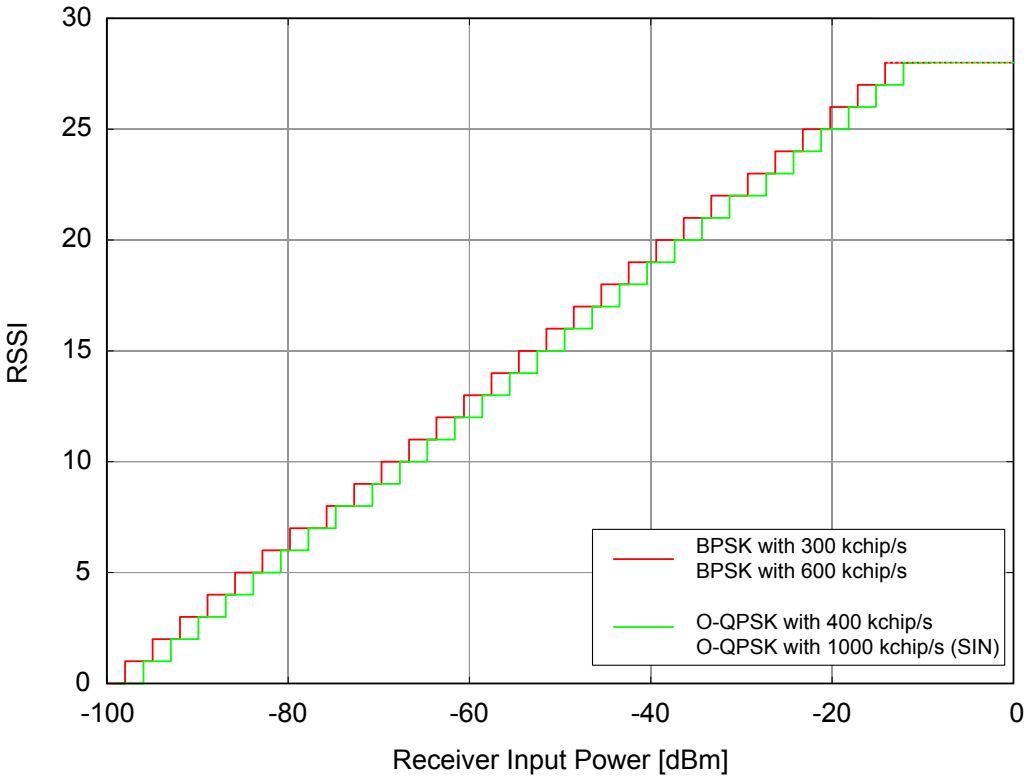
Table 6-25. RSSI_BASE_VAL

PHY Mode	RSSI_BASE_VAL [dBm]
BPSK with 300 kchip/s	-100
BPSK with 600 kchip/s	-100
O-QPSK with 400 kchip/s	-98
O-QPSK with 1000 kchip/s, sine shaping (SIN)	-98
O-QPSK with 1000 kchip/s, raised cosine shaping (RC-0.8)	-97

The receiver input power can be calculated as follows:

$$P_{RF}\ [\text{dBm}] = \text{RSSI_BASE_VAL} + 3.1 \cdot \text{RSSI}$$

Figure 6-3. Mapping between RSSI Value and Receiver Input Power



6.4.4 Register Description

Register 0x06 (PHY_RSSI)

Table 6-26. Register 0x06 (PHY_RSSI)

Bit	7	6	5	4
Name	RX_CRC_VALID	RND_VALUE[1]	RND_VALUE[0]	RSSI[4]
Read/Write	R	R	R	R
Reset Value	0	0	0	0

Bit	3	2	1	0
Name	RSSI[3]	RSSI[2]	RSSI[1]	RSSI[0]
Read/Write	R	R	R	R
Reset Value	0	0	0	0

- **Bit 7 – RX_CRC_VALID**

Refer to section 6.3.5.

- **Bit 6:5 – RND_VALUE**

Refer to section 9.2.2.

- **Bit 4:0 – RSSI**

The result of the automated RSSI measurement is stored in register bits RSSI. The value is updated at time intervals according to Table 6-24 in any receive state. RSSI is a number between 0 and 28, representing the received signal strength with a resolution of about 3 dB.

6.5 Energy Detection (ED)

The Energy Detection (ED) module is characterized by:

- a dynamic range of 87 dB
- a resolution of about 1 dB
- a measurement time of 8 symbol periods for IEEE 802.15.4 compliant data rates

6.5.1 Overview

The receiver ED measurement (ED scan procedure) can be used as a part of a channel selection algorithm. It is an estimation of the received signal power within the bandwidth of an IEEE 802.15.4 channel. No attempt is made to identify or decode signals on the channel. The ED value is calculated by averaging RSSI values over 8 symbol periods, with the exception of the High Data Rate Modes (refer to section 7.1.4).

6.5.2 Measurement Description

There are two ways to initiate an ED measurement,

- manually by writing an arbitrary value to register 0x07 (PHY_ED_LEVEL), or
- automatically after detection of a valid SHR of an incoming frame.

Manually:

For manually initiated ED measurements, the radio transceiver needs to be either in the state RX_ON or BUSY_RX. The end of the ED measurement time (8 symbol periods) is indicated by the interrupt IRQ_4 (CCA_ED_DONE) and the measurement result is stored in register 0x07 (PHY_ED_LEVEL).

In order to avoid interference with an automatically initiated ED measurement, the SHR detection can be disabled by setting register bit RX_PDT_DIS (register 0x15, RX_SYN), refer to section 7.2.

Note that it is not recommended to manually initiate an ED measurement when using the Extended Operating Mode.

Automatically:

An automated ED measurement is started upon SHR detection. The end of the automated measurement is not signaled by an interrupt.

When using the Basic Operating Mode and standard compliant data rates, a valid ED value (register 0x07, PHY_ED_LEVEL) of the currently received frame is accessible not later than 8 symbol periods after IRQ_2 (RX_START) plus a processing time of 12 µs. For High Data Rate Modes (refer to 7.1.4), the measurement duration is reduced to 2 symbol periods plus a processing time of 12 µs. The ED value remains valid until a new RX_START interrupt is generated by the next incoming frame or until another ED measurement is initiated.

When using the Extended Operating Mode, it is useful to mask IRQ_2 (RX_START), thus the interrupt cannot be used as timing reference. A successful frame reception is signalized by interrupt IRQ_3 (TRX_END). In this case, the ED value needs to be read within the time span of a next SHR detection plus the ED measurement time in order to avoid overwrite of the current ED value.

6.5.3 Data Interpretation

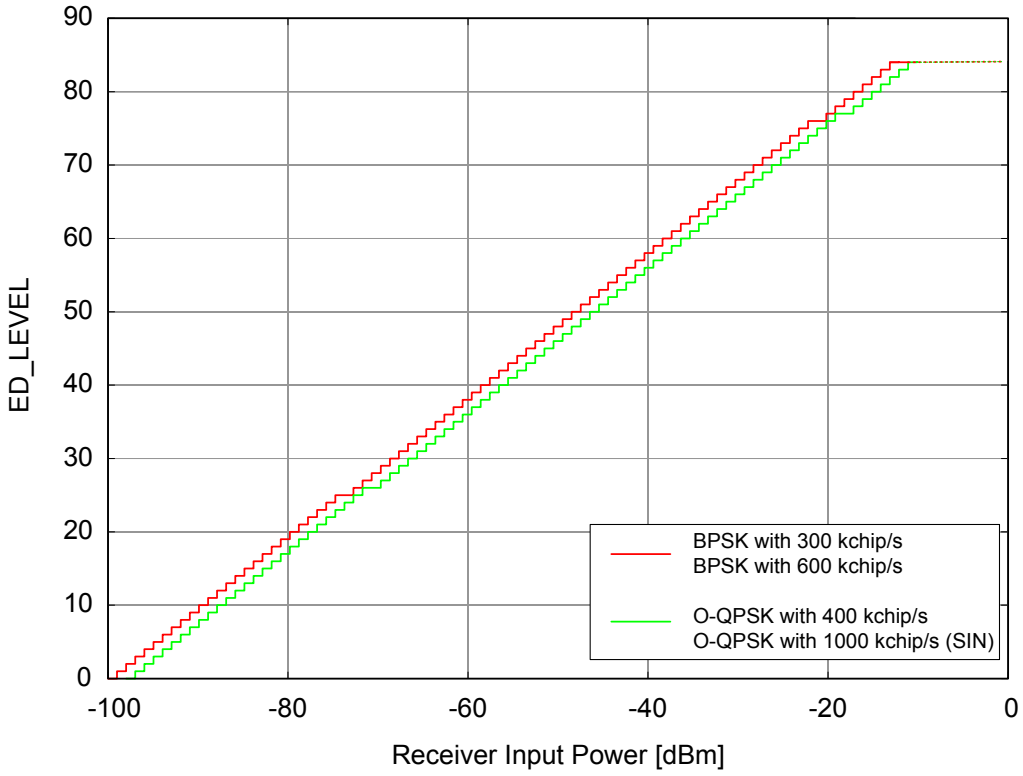
The PHY_ED_LEVEL (ED) is an 8-bit register. The ED value of the AT86RF212 has a valid range from 0x00 to 0x54 (0 to 84) with a resolution of about 1 dB. Values 0x55 to 0xFE do not occur and a value of 0xFF indicates the reset value.

An ED value of 0 indicates a receiver input power less than or equal to RSSI_BASE_VAL [dBm] (refer to Table 6-25); a value of 85 indicates an input power equal to or larger than (RSSI_BASE_VAL + 87) [dBm].

The receiver input power can be calculated as follows:

$$P_{RF}\ [\text{dBm}] = \text{RSSI_BASE_VAL} + 1.03 \cdot \text{ED_LEVEL}$$

Figure 6-4. Mapping between ED Value and Receiver Input Power



6.5.4 Interrupt Handling

Interrupt IRQ_4 (CCA_ED_DONE) is issued at the end of a manually initiated ED measurement.

Note that an ED measurement should only be initiated in RX states but not in RX_AACK states. Otherwise, the radio transceiver generates an IRQ_4 (CCA_ED_DONE) without actually performing an ED measurement.

6.5.5 Register Description

Register 0x07 (PHY_ED_LEVEL)

The PHY_ED_LEVEL register contains the result of an ED measurement.

Table 6-27. Register 0x07 (PHY_ED_LEVEL)

Bit	7	6	5	4	3	2	1	0
Name	ED_LEVEL[7:0]							
Read/Write	R (1)							
Reset Value	1	1	1	1	1	1	1	1

Note: 1. A write access is required for initiation of a manual ED measurement.

Bit 7:0 – ED_LEVEL

The measured ED value has a valid range from 0x00 to 0x54 (0 to 84). The value 0xFF indicates that a measurement has never been started (reset value).

A manual ED measurement can be initiated by a write access to the register.

6.6 Clear Channel Assessment (CCA)

The main features of the Clear Channel Assessment (CCA) module are:

- All four CCA modes are provided as defined in IEEE 802.15.4-2006
- Adjustable threshold for energy detection algorithm

6.6.1 Overview

A CCA measurement is used to detect a clear channel. Four CCA modes are specified by IEEE 802.15.4-2006:

Table 6-28. CCA Mode Overview

CCA Mode	Description
1	*Energy above threshold:* CCA shall report a busy medium upon detecting any energy above the ED threshold.
2	*Carrier sense* only: CCA shall report a busy medium only upon the detection of a signal with the modulation and spreading characteristics of an IEEE 802.15.4 compliant signal. The signal strength may be above or below the ED threshold.
0, 3	*Carrier sense* with *energy above threshold:* CCA shall report a busy medium using a logical combination of – detection of a signal with the modulation and spreading characteristics of this standard and/or – energy above the ED threshold, where the logical operator may be configured as either OR (mode 0) or AND (mode 3).

6.6.2 Configuration and Request

The CCA modes are configurable via register 0x08 (PHY_CC_CCA).

When being in Basic Operating Mode, a CCA request can be initiated manually by setting CCA_REQUEST = 1 (register 0x08, PHY_CC_CCA) if the AT86RF212 is in any RX state. The current channel status (CCA_STATUS) and the CCA completion status (CCA_DONE) are accessible through register 0x01 (TRX_STATUS).

The end of a manually initiated CCA (8 symbol periods plus 12 µs processing delay) is indicated by the interrupt IRQ_4 (CCA_ED_DONE).

The sub-register CCA_ED_THRES of register 0x09 (CCA_THRES) defines the receive power threshold of the “energy above threshold” algorithm. The threshold is calculated by

$$V_THRES\ [dBm] = RSSI_BASE_VAL + 2.07 \cdot CCA_ED_THRES\ .$$

Any received power above this level is interpreted as a busy channel.

Note that it is not recommended to manually initiate a CCA request when using the Extended Operating Mode.

6.6.3 Data Interpretation

The current channel status (CCA_STATUS) and the CCA completion status (CCA_DONE) are accessible through register 0x01 (TRX_STATUS). Note that register bits CCA_DONE and CCA_STATUS are cleared in response to a CCA_REQUEST. The completion of a measurement cycle is indicated by CCA_DONE = 1. If the radio transceiver detects no signal (idle channel) during the CCA evaluation period, the CCA_STATUS bit is set to 1; otherwise, it is set to 0.

When using the “energy above threshold” algorithm, a received power above V_THRES level is interpreted as a busy channel.

When using the “carrier sense” algorithm (i.e. CCA_MODE = 0, 2, and 3), the AT86RF212 reports a busy channel upon detection of a PHY mode specific IEEE 802.15.4 signal above RSSI_BASE_VAL [dBm] (see Table 6-25). The AT86RF212 is also capable of detecting signals below this value, but the detection probability decreases with decreasing signal power. It is almost zero at the radio transceivers sensitivity level (see parameter 10.7.1 on page 154).

6.6.4 Interrupt Handling

Interrupt IRQ_4 (CCA_ED_DONE) is issued at the end of a manually initiated CCA measurement.

Note

- A CCA request should only be initiated in Basic Operating Mode RX states. Otherwise, the radio transceiver generates IRQ_4 (CCA_ED_DONE) and sets the register bit CCA_DONE = 1, without actually performing a CCA measurement.

6.6.5 Measurement Time

The response time of a manually initiated CCA measurement depends on the receiver state.

In RX_ON state, the CCA measurement is done over 8 symbol periods and the result is accessible upon the event IRQ_4 (CCA_ED_DONE) or upon CCA_DONE = 1 (register 0x01, TRX_STATUS).

In BUSY_RX state, the CCA measurement duration depends on the CCA mode and the CCA request relative to the detection of the SHR. The end of the CCA measurement is indicated by IRQ_4 (CCA_ED_DONE). The variation of a CCA measurement period in BUSY_RX state is described in Table 6-29.

Table 6-29. CCA Measurement Period and Access in BUSY_RX State

CCA Mode	Request within ED Measurement (1)	Request after ED Measurement
1	*Energy above threshold*	
	CCA result is available after finishing automated ED measurement period.	CCA result is immediately available after request.
2	*Carrier sense* only	
	CCA result is immediately available after request.	
3	*Carrier sense* with *energy above threshold* (AND)	
	CCA result is available after finishing automated ED measurement period.	CCA result is immediately available after request.
0	*Carrier sense* with *energy above threshold* (OR)	
	CCA result is available after finishing automated ED measurement period.	CCA result is immediately available after request.

Note: 1. After detecting the SHR, an automated ED measurement is started with a length of 8 symbol periods (2 symbol periods for high rate PHY modes). This automated ED measurement must be finished to provide a result for the CCA measurement. Only one automated ED measurement per frame is performed.

It is recommended to perform CCA measurements in RX_ON state only. To avoid switching accidentally to BUSY_RX state, the SHR detection can be disabled by setting register bit RX_PDT_DIS (register 0x15, RX_SYN), refer to section 7.2.3. The receiver remains in RX_ON state to perform a CCA measurement until the register bit RX_PDT_DIS is set back to continue the frame reception. In this case, the CCA measurement duration is 8 symbol periods.

6.6.6 Register Description

Register 0x01 (TRX_STATUS):

Two register bits of register 0x01 (TRX_STATUS) indicate the status of the CCA measurement.

Table 6-30. Register 0x01 (TRX_STATUS)

Bit	7	6	5	4
Name	CCA_DONE	CCA_STATUS	Reserved	TRX_STATUS[4]
Read/Write	R	R	R	R
Reset Value	0	0	0	0
Bit	3	2	1	0
Name	TRX_STATUS[3]	TRX_STATUS[2]	TRX_STATUS[1]	TRX_STATUS[0]
Read/Write	R	R	R	R
Reset Value	0	0	0	0

- **Bit 7 – CCA_DONE**

This register indicates completion a CCA measurement, which is additionally indicated by the interrupt IRQ_4 (CCA_ED_DONE). Note that register bit CCA_DONE is cleared in response to a CCA_REQUEST.

Table 6-31. CCA Algorithm Status

Register Bit	Value	Description
CCA_DONE	0	CCA calculation not finished
	1	CCA calculation finished

- **Bit 6 – CCA_STATUS**

After a CCA request is completed, the result of the CCA measurement is available in register bit CCA_STATUS. Note that register bit CCA_STATUS is cleared in response to a CCA_REQUEST.

Table 6-32. CCA Status Result

Register Bit	Value	Description
CCA_STATUS	0	Channel indicated as busy
	1	Channel indicated as idle

- **Bit 5 – Reserved**
- **Bit 4:0 – TRX_STATUS**

Refer to sections 5.1.5 and 5.2.6.

Register 0x08 (PHY_CC_CCA):

This register is provided to initiate and control a CCA measurement.

Table 6-33. Register 0x08 (PHY_CC_CCA)

Bit	7	6	5	4
Name	CCA_REQUEST	CCA_MODE[1]	CCA_MODE[0]	CHANNEL[4]
Read/Write	W	R/W	R/W	R/W
Reset Value	0	0	1	0
Bit	3	2	1	0
Name	CHANNEL[3]	CHANNEL[2]	CHANNEL[1]	CHANNEL[0]
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	1	0	1

- **Bit 7 – CCA_REQUEST**

A manual CCA measurement is initiated by setting CCA_REQUEST = 1. The register bit is automatically cleared after requesting a CCA measurement with CCA_REQUEST = 1.

- **Bit 6:5 – CCA_MODE**

The CCA mode can be selected using register bits CCA_MODE.

Table 6-34. CCA Mode

Register Bits	Value	Description
CCA_MODE	0	“Carrier sense” OR “energy above threshold”
	1	“Energy above threshold”
	2	“Carrier sense” only
	3	“Carrier sense” AND “energy above threshold”

Note that IEEE 802.15.4–2006 CCA mode 3 defines the logical combination of CCA mode 1 and 2 with the logical operators AND or OR. This can be selected with:

- CCA_MODE = 0 for logical operation OR, and
- CCA_MODE = 3 for logical operation AND.

- **Bit 4:0 – CHANNEL**

Refer to section 7.8.6.

Register 0x09 (CCA_THRES):

This register sets the ED threshold level for CCA.

Table 6-35. Register 0x09 (CCA_THRES)

Bit	7	6	5	4
Name	Reserved	Reserved	Reserved	Reserved
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	1	1	1
Bit	3	2	1	0
Name	CCA_ED_THRES	CCA_ED_THRES	CCA_ED_THRES	CCA_ED_THRES
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	1	1	1

- **Bit 7:4 – Reserved**
- **Bit 3:0 – CCA_ED_THRES**

For CCA_MODE = 1, a busy channel is indicated if the measured received power is above (RSSI_BASE_VAL + 2.07 · CCA_ED_THRES) [dBm]. CCA modes 0 and 3 are logically related to this result.

6.7 Listen Before Talk (LBT)

6.7.1 Overview

Equipment using the AT86RF212 shall conform to the established regulations. With respect to the regulations in Europe, CSMA-CA based transmission according to IEEE 802.15.4 is not appropriate. In principle, transmission is subject to low duty cycles (0.1 to 1 %). However, according to [5], equipment employing listen before talk (LBT) and adaptive frequency agility (AFA) does not have to comply with duty cycle conditions. Hence, LBT can be attractive in order to reduce network latency.

Minimum Listening Time

A device with LBT needs to comply with a minimum listening time, refer to section 9.1.1.2 of [5]. Prior transmission, the device must listen for a receive signal at or above the LBT threshold level to determine whether the intended channel is available for use, unless transmission is pursuing acknowledgement.

A device using LBT needs to listen for a fixed period of 5 ms. If the channel is free after this period, transmission may immediately commence (i.e. no CSMA is required). Otherwise, a new listening period of a randomly selected time span between 5 and 10 ms is required. The time resolution shall be approximately 0.5 ms. The last step needs to be repeated until a free channel is available.

LBT Threshold

According to [5], the maximum LBT threshold for an IEEE 802.15.4 signal is presumably -82 dBm, assuming a channel spacing of 1 MHz.

6.7.2 LBT Mode

The AT86RF212 supports the previously described LBT specific listening mode when operating in the Extended Operating Mode.

In particular, during TX_ARET (see section 5.2.4), the CSMA-CA algorithm can be replaced by the LBT listening mode when setting register bit CSMA_LBT_MODE (register 0x17, XAH_CTRL_1). In this case, however, the register bits MAX_CSMA_RETRIES (register 0x2C, XAH_CTRL_0) as well as MIN_BE and MAX_BE (register 0x2F, CSMA_BE) are ignored, implying that the listening mode will sustain unless a clear channel has been found or the TX_ARET transaction will be canceled. The latter can be achieved by setting TRX_CMD to either FORCE_PLL_ON or FORCE_TRX_OFF (register 0x02, TRX_STATE). All other aspects of TX_ARET remain unchanged, refer to section 5.2.4.

The LBT threshold can be configured in the same way as for CCA, i.e. via register bits CCA_MODE (register 0x08, PHY_CC_CCA) and register bits CCA_ED_THRES (register 0x09, CCA_THRES), refer to section 6.6.

6.7.3 Register Description

Register 0x08 (PHY_CC_CCA):

This register is relevant for the measurement mode when using LBT, i.e. selecting “energy above threshold” or “carrier sense” (CS) or combination of both.

Table 6-36. Register 0x08 (PHY_CC_CCA)

Bit	7	6	5	4
Name	CCA_REQUEST	CCA_MODE[1]	CCA_MODE[0]	CHANNEL[4]
Read/Write	W	R/W	R/W	R/W
Reset Value	0	0	1	0

Bit	3	2	1	0
Name	CHANNEL[3]	CHANNEL[2]	CHANNEL[1]	CHANNEL[0]
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	1	0	1

- **Bit 7 – CCA_REQUEST**

Not applicable for LBT, see section 6.6.6.

- **Bit 6:5 – CCA_MODE**

The CCA mode can be used in order to select the appropriate LBT measurement mode by using register bits CCA_MODE, refer to section 6.6.

- **Bit 4:0 – CHANNEL**

Refer to section 7.8.6.

Register 0x09 (CCA_THRES):

This register is relevant for the ED threshold when using LBT.

Table 6-37. Register 0x09 (CCA_THRES)

Bit	7	6	5	4
Name	Reserved	Reserved	Reserved	Reserved
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	1	1	1
Bit	3	2	1	0
Name	CCA_ED_THRES	CCA_ED_THRES	CCA_ED_THRES	CCA_ED_THRES
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	1	1	1

- **Bit 7:4 – Reserved**
- **Bit 3:0 – CCA_ED_THRES**

For CCA_MODE = 1, a busy channel is indicated if the measured received power is above (RSSI_BASE_VAL + 2.07 · CCA_ED_THRES) [dBm]. CCA_MODE = 0 and 3 are logically related to this result.

Register 0x17 (XAH_CTRL_1):

This register is relevant for enabling or disabling the LBT mode.

Table 6-38. Register 0x17 (XAH_CTRL_1)

Bit	7	6	5	4
Name	Reserved	CSMA_LBT_MODE	AACK_FLTR_RES_FT	AACK_UPLD_RES_FT
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0
Bit	3	2	1	0
Name	Reserved	AACK_ACK_TIME	AACK_PROM_MODE	Reserved
Read/Write	R	R/W	R/W	R
Reset Value	0	0	0	0

- **Bit 7 – Reserved**
- **Bit 6 – CSMA_LBT_MODE**

If set to 0 (default), CSMA-CA algorithm is used during TX_ARET for clear channel assessment. Otherwise, the LBT specific listening mode is applied.

- **Bit 5:4 – AACK_FLTR_RES_FT, AACK_UPLD_RES_FT**

Refer to section 5.2.6.

- **Bit 3 – Reserved**
- **Bit 2:1 – AACK_ACK_TIME, AACK_PROM_MODE**

Refer to sections 5.2.6 and 5.2.3.3.

- **Bit 0 – Reserved**

6.8 Link Quality Indication (LQI)

6.8.1 Requirements

The IEEE 802.15.4 standard defines the LQI as a characterization of the strength and/or quality of a received frame. The use of the LQI result by the network or application layer is not specified in this standard. The LQI value shall be an integer ranging from 0 to 255, with at least 8 unique values. The minimum and maximum LQI values (0 and 255) should be associated with the lowest and highest quality compliant signals, respectively, and LQI values in between should be uniformly distributed between these two limits.

6.8.2 Implementation

During symbol detection within frame reception, the AT86RF212 uses correlation results of multiple symbols in order to compute an estimate of the LQI value. This is motivated by the fact that the mean value of the correlation result is inversely related to the probability of a detection error.

LQI computation is automatically performed for each received frame, once the SHR has been detected. LQI values are integers ranging from 0 to 255 as required by the IEEE 802.15.4 standard.

6.8.3 Obtaining the LQI Value

The LQI value is available, once the corresponding frame has been completely received. This is indicated by the interrupt IRQ_3 (TRX_END). The value can be obtained by means of a frame buffer read access, see section 4.3.2.

6.8.4 Remarks

The reason for a low LQI value can be twofold: a low signal strength and/or high signal distortions, e.g. by interference and/or multipath propagation. High LQI values, however, indicate a sufficient signal strength and low signal distortions.

Note that the LQI value is almost always 255 for scenarios with very low signal distortions and a signal strength much greater than the sensitivity level. In this case, the packet error rate tends towards zero and increase of the signal strength, i.e. by increasing the transmission power, cannot decrease the error rate any further. Received signal strength indication (RSSI) or energy detection (ED) can be used to evaluate the signal strength and the link margin.

ZigBee networks often require identification of the “best” routing between two nodes. LQI and RSSI/ED can be applied, depending on the optimization criteria. If a low frame error rate (corresponding to a high throughput) is the optimization criteria, then the LQI value should be taken into consideration. If, however, the target is a low transmission power, then the RSSI/ED value is also helpful.

Various combinations of LQI and RSSI/ED are possible for routing decisions. As a rule of thumb, information on RSSI/ED is useful in order to differentiate between links with high LQI values. However, transmission links with low LQI values should be discarded for routing decisions, even if the RSSI/ED values are high, since it is merely an information about the received signal strength, whereas the source can be an interferer.

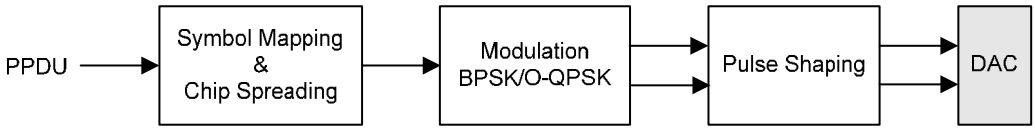
7 Module Description

7.1 Physical Layer Modes

7.1.1 Spreading, Modulation, and Pulse Shaping

The AT86RF212 supports various physical layer (PHY) modes independent of the RF channel selection. Symbol mapping along with chip spreading, modulation, and pulse shaping is part of the digital base band processor, see Figure 7-1.

Figure 7-1. Base Band Transmitter Architecture



The combination of spreading, modulation, and pulse shaping are restricted to several combinations as shown in Table 7-1.

The AT86RF212 is fully compliant to the IEEE 802.15.4 low data rate modes of 20 kbit/s or 40 kbit/s, employing binary phase-shift keying (BPSK) and spreading with a fixed chip rate of 300 kchip/s or 600 kchip/s, respectively. The symbol rate is 20 ksymbol/s or 40 ksymbol/s, respectively. In both cases, pulse shaping is approximating a raised cosine filter with roll-off factor 1.0 (RC-1.0).

For optional data rates according to IEEE 802.15.4-2006, offset quadrature phase-shift keying (O-QPSK) is supported by the AT86RF212 with a fixed chip rate of either 400 kchip/s or 1000 kchip/s.

At a chip rate of 400 kchip/s, pulse shaping is always a combination of both, half-sine shaping (SIN) and raised cosine filtering with roll-off factor 0.2 (RC-0.2) according to IEEE 802.15.4-2006 for the 868.3 MHz band. At a chip rate of 1000 kchip/s, pulse shaping is either half-sine filtering (SIN) as specified in IEEE 802.15.4-2006 [2], or, alternatively, raised cosine filtering with roll-off factor 0.8 (RC-0.8) as specified in IEEE 802.15.4c-2009 [3].

For O-QPSK, the AT86RF212 supports spreading according to IEEE 802.15.4-2006 with data rates of either 100 kbit/s or 250 kbit/s depending on the chip rate, leading to a symbol rate of either 25 ksymbol/s or 62.5 ksymbol/s, respectively.

Additionally, the AT86RF212 supports two more spreading codes for O-QPSK with shortened code lengths. This leads to higher but non IEEE 802.15.4-2006 compliant data rates during the PSDU part of the frame with 200, 400, 500, and 1000 kbit/s. The proprietary High Data Rate Modes are outlined in more detail in section 7.1.4.

Table 7-1. Modulation and Pulse Shaping

Modulation	Chip Rate [kchip/s]	Supported Data Rate for PPDU Header [kbit/s]	Supported Data Rates for PSDU [kbit/s]	Pulse Shaping
BPSK	300	20	20	RC-1.0
	600	40	40	RC-1.0
O-QPSK	400	100	100, 200, 400	SIN and RC-0.2
	1000	250	250, 500, 1000	SIN or RC-0.8

7.1.2 Configuration

The PHY mode can be selected by setting appropriate register bits of register 0x0C (TRX_CTRL_2), refer to section 7.1.5. During configuration, the transceiver needs to be in state TRX_OFF.

7.1.3 Symbol Period

Within IEEE 802.15.4 and, accordingly, within this document, time references are often specified in units of symbol periods, leading to a PHY mode independent description. Table 7-2 shows the duration of the symbol period. Note that for the proprietary High Data Rate Modes, the symbol period is (by definition) the same as the symbol period of the corresponding base mode.

Table 7-2. Duration of the Symbol Period

Modulation	PSDU Data Rate [kbit/s]	Duration of Symbol Period [µs]
BPSK	20	50
	40	25
O-QPSK	100, 200, 400	40
	250, 500, 1000	16

7.1.4 Proprietary High Data Rate Modes

The main features are:

- High data rates up to 1000 kbit/s
- Support of Basic and Extended Operating Mode
- Reduced ACK timing (optional)

7.1.4.1 Overview

The AT86RF212 supports alternative data rates of {200, 400, 500, 1000} kbit/s for applications not necessarily targeting IEEE 802.15.4 compliant networks.

The High Data Rate Modes utilize the same RF channel bandwidth as the IEEE 802.15.4-2006 sub-1 GHz O-QPSK modes. Higher data rates are achieved by modified O-QPSK spreading codes having reduced code lengths. The lengths are reduced by the factor 2 or by the factor 4.

For O-QPSK with 400 kchip/s, this leads to a data rate of 200 kbit/s (2-fold) and 400 kbit/s (4-fold), respectively.

For O-QPSK with 1000 kchip/s, the resulting data rate is 500 kbit/s (2-fold) and 1000 kbit/s (4-fold), respectively.

Due to the decreased spreading factor, the sensitivity of the receiver is reduced. Section 10.7, parameter 10.7.1, shows typical values of the sensitivity for different data rates. Note that the sensitivity values of the High Data Rate Modes are provided for a maximum PSDU length of 127 octets.

7.1.4.2 High Data Rate Frame Structure

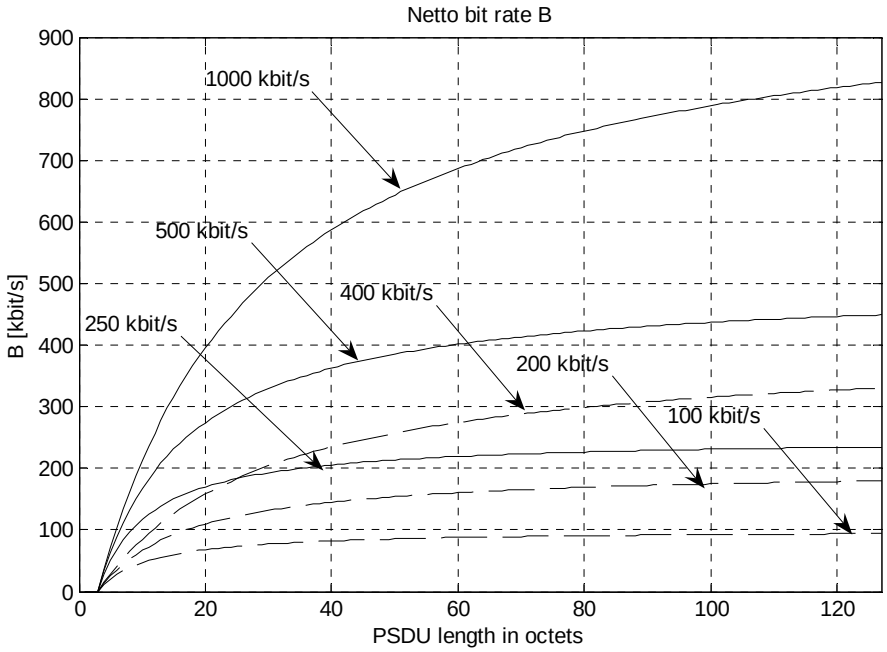
In order to allow robust frame synchronization, high data rate modulation is restricted to the PSDU part only. The PPDU header (the preamble, the SFD, and the PHR field) are transmitted with the IEEE 802.15.4-2006 O-QPSK rate of either 100 kbit/s or 250 kbit/s (basic rates), see Figure 7-2.

Figure 7-2. High Date Rate Frame Structure



Due to the overhead caused by the PPDU header and the FCS, the effective data rate is less than the selected data rate, depending on the length of the PSDU. A graphical representation of the effective data rate is shown in Figure 7-3.

Figure 7-3. Effective Data Rate of the O-QPSK Modes



Consequently, high data rate transmission is useful for large PSDU lengths due to the higher effective data rate, or in order to reduce the power consumption of the system.

7.1.4.3 High Date Rate Mode Options

Reduced Acknowledgment Time

If register bit AACK_ACK_TIME (register 0x17, XAH_CTRL_1) is set, the acknowledgment time is reduced to the duration of 2 symbol periods for 200 and 400 kbit/s, and to 3 symbol periods for 500 and 1000 kbit/s, refer to Table 5-24. Otherwise, it defaults to 12 symbol periods according to IEEE 802.15.4.

Receiver Sensitivity Control

The different data rates between PPDU header (SHR and PHR) and PHY payload (PSDU) cause a different sensitivity between header and payload. This can be adjusted by defining sensitivity threshold levels of the receiver. With a sensitivity threshold level set, the AT86RF212 does not synchronize to frames with an RSSI level below that threshold. Refer to section 7.2.3 for a configuration of the sensitivity threshold with register 0x15 (RX_SYN).

Scrambler

For data rates 1000 kbit/s and 400 kbit/s, additional chip scrambling is applied per default in order to mitigate data dependent spectral properties. Scrambling can be disabled if bit OQPSK_SCRAM_EN (register 0x0C, TRX_CTRL_2) is set to 0.

Energy Detection

The ED measurement time span is 8 symbol periods according to IEEE 802.15.4. For frames operated at a higher data rate, the automated measurement duration (see section 6.5.2) is reduced to 2 symbol periods taking reduced frame durations into account. This means, the ED measurement time is 80 µs for modes 200 kbit/s and 400 kbit/s, and 32 µs for modes 500 kbit/s and 1000 kbit/s. For manually initiated ED measurements in these modes, the measurement time is still 8 symbol periods.

Carrier Sense

For clear channel assessment, IEEE 802.15.4-2006 specifies several modes which may either apply “energy above threshold” or “carrier sense” (CS) or a combination of both. Since signals of the High Data Rate Modes are not compliant to IEEE 802.15.4-2006, CS is not supported when the AT86RF212 is operating in these modes. However, “energy above threshold” is supported.

Link Quality Indicator (LQI)

For the High Data Rate Modes, the link quality value does not contain useful information and should be discarded.

7.1.5 Register Description

Register 0x0C (TRX_CTRL_2):

The TRX_CTRL_2 register controls the PHY mode settings. Note that during configuration, the transceiver needs to be in state TRX_OFF.

Table 7-3. Register 0x0C (TRX_CTRL_2)

Bit	7	6	5	4
Name	RX_SAFE_MODE	TRX_OFF_AVDD_EN	OQPSK_SCRAM_EN	OQPSK_SUB1_RC_EN
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	1	0

Bit	3	2	1	0
Name	BPSK_OQPSK	SUB_MODE	OQPSK_DATA_RATE	OQPSK_DATA_RATE
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	1	0	0

- **Bit 7 – RX_SAFE_MODE**

Refer to section 9.7.2.

- **Bit 6 – TRX_OFF_AVDD_EN**

Refer to sections 5.1.4.3 and 7.5.4.

- **Bit 5 – OQPSK_SCRAM_EN**

If set to 1 (reset value), the scrambler is enabled for OQPSK_DATA_RATE = 2 and BPSK_OQPSK = 1 (O-QPSK is active). Otherwise, the scrambler is disabled.

Note that during reception, this bit is evaluated within the AT86RF212, so it is explicitly required to align different transceivers with OQPSK_SCRAM_EN in order to assure interoperability.

- **Bit 4 – OQPSK_SUB1_RC_EN**

The bit is relevant for SUB_MODE = 1 and BPSK_OQPSK = 1.

If set to 0 (reset value), pulse shaping is half-sine filtering for O-QPSK transmission with 1000 kchip/s.

If set to 1, pulse shaping is RC-0.8 filtering. Compared with half-sine filtering, side-lobes are reduced at the expense of an increased peak to average ratio (~ 1 dB). This mode is particularly suitable for the Chinese 780 MHz band, refer to IEEE 802.15.4c-2009.

Note that during reception, this bit is not evaluated within the AT86RF212, so it is not explicitly required to align different transceivers with OQPSK_SUB1_RC_EN in order to assure interoperability. It is very likely that this also holds for any IEEE 802.15.4-2006 compliant O-QPSK transceiver in the 915 MHz band, since the IEEE 802.15.4-2006 requirements are fulfilled for both types of shaping.

- **Bit 3 – BPSK_OQPSK**

If set to 0 (reset value), BPSK transmission and reception is applied.

If set to 1, O-QPSK transmission and reception is applied.

Note that during reception, this bit is evaluated within the AT86RF212, so it is explicitly required to align different transceivers with BPSK_OQPSK in order to assure interoperability.

- **Bit 2 – SUB_MODE**

If set to 1 (reset value), the chip rate is 1000 kchip/s for BPSK_OQPSK = 1 and 600 kchip/s for BPSK_OQPSK = 0. It permits data rates out of {250, 500, 1000} kbit/s or 40 kbit/s, respectively. This mode is particularly suitable for the 915 MHz band. For O-QPSK transmission, pulse shaping is either half-sine shaping or RC-0.8 shaping, depending on OQPSK_SUB1_RC_EN.

If set to 0, the chip rate is 400 kchip/s for BPSK_OQPSK = 1 and 300 kchip/s for BPSK_OQPSK = 0. It permits data rates out of {100, 200, 400} kbit/s or 20 kbit/s, respectively. This mode is particularly suitable for the 868.3 MHz band. For O-QPSK transmission, pulse shaping is always the combination of half-sine shaping and RC-0.2 shaping.

Note that during reception, this bit is evaluated within the AT86RF212, so it is explicitly required to align different transceivers with SUB_MODE in order to assure interoperability.

- **Bit 1:0 – OQPSK_DATA_RATE**

These register bits control the O-QPSK data rate during the PSDU part of the frame, as depicted by Table 7-4. The reset value is OQPSK_DATA_RATE = 0.

Note that during reception, these bits are evaluated within the AT86RF212, so it is explicitly required to align different transceivers with OQPSK_DATA_RATE in order to assure interoperability.

Table 7-4. O-QPSK Data Rate during PSDU

Register Bits	Value	O-QPSK Data Rate [kbit/s]	
		SUB_MODE = 0	SUB_MODE = 1
OQPSK_DATA_RATE	0	100	250
	1	200	500
	2	400	1000
	3	Reserved	

In Table 7-5 all PHY modes supported by the AT86RF212 are summarized with the relevant setting for each bit of register TRX_CTRL_2. The "-" (minus) character means that the bit entry is not relevant for the particular PHY mode.

Table 7-5. Register 0x0C (TRX_CTRL_2) Bit Alignment

PHY Mode	Bits of Register 0x0C								Compliance
	7	6	5	4	3	2	1	0	
BPSK-20	-	-	-	0	0	0	0	0	IEEE 802.15.4-2003/2006: channel page 0, channel 0
BPSK-40	-	-	-	0	0	1	0	0	IEEE 802.15.4-2003/2006: channel page 0, channel 1 to 10
OQPSK-SIN-RC-100	-	-	-	0	1	0	0	0	IEEE 802.15.4-2006: channel page 2, channel 0
OQPSK-SIN-RC-200	-	-	-	0	1	0	0	1	Proprietary
OQPSK-SIN-RC-400-SCR-ON	-	-	1	0	1	0	1	0	Proprietary, scrambler on
OQPSK-SIN-RC-400-SCR-OFF	-	-	0	0	1	0	1	0	Proprietary, scrambler off
OQPSK-SIN-250	-	-	-	0	1	1	0	0	IEEE 802.15.4-2006: channel page 2, channel 1 to 10
OQPSK-SIN-500	-	-	-	0	1	1	0	1	Proprietary
OQPSK-SIN-1000-SCR-ON	-	-	1	0	1	1	1	0	Proprietary, scrambler on
OQPSK-SIN-1000-SCR-OFF	-	-	0	0	1	1	1	0	Proprietary, scrambler off
OQPSK-RC-250	-	-	-	1	1	1	0	0	IEEE 802.15.4c-2009 (China): channel page 5, channel 0 to 3
OQPSK-RC-500	-	-	-	1	1	1	0	1	Proprietary
OQPSK-RC-1000-SCR-ON	-	-	1	1	1	1	1	0	Proprietary, scrambler on
OQPSK-RC-1000-SCR-OFF	-	-	0	1	1	1	1	0	Proprietary, scrambler off

7.2 Receiver (RX)

7.2.1 Overview

The AT86RF212 transceiver is split into an analog radio front-end and a digital domain, see Figure 1-1. Referring to the receiver part of the analog domain, the differential RF signal is amplified by a low noise amplifier (LNA) and split into quadrature signals by a poly-phase filter (PPF). Two mixer circuits convert the quadrature signal down to an intermediate frequency. Channel selectivity is achieved by an integrated band-pass filter (BPF). The subsequent analog-to-digital converter (ADC) samples the receive signal and additionally generates a digital RSSI signal, see section 6.4. The ADC output is then further processed by the digital baseband receiver (RX BBP), which is part of the digital domain.

The BBP performs further filtering and signal processing. In RX_ON state, the receiver searches for the synchronization header. Once the synchronization is established and the SFD is found, the received signal is demodulated and provided to the Frame Buffer. The receiver performs a state change indicated by register bits TRX_STATUS (register 0x01, TRX_STATUS) to BUSY_RX. Once the whole frame is received, the receiver switches back to RX_ON to listen on the channel. A similar scheme applies to the Extended Operating Mode.

The receiver is designed to handle reference oscillator accuracies up to ±60 ppm; refer to section 10.5, parameter 10.5.6. This results in the estimation and correction of frequency and symbol rate errors up to ±120 ppm.

Several status information are generated during the receive process: LQI, ED, and RX_STATUS. They are automatically appended during Frame Read Access, refer to section 4.3.2. Some information is also available through register access, e.g. ED value (register 0x07, PHY_ED_LEVEL) and FCS correctness (register 0x06, PHY_RSSI).

The Extended Operating Mode of the AT86RF212 supports frame filtering and pending data indication.

The frame receive procedure, including the radio transceiver setup for reception and reading PSDU data from the Frame Buffer, is described in section 8.1.

7.2.2 Configuration

In Basic Operating Mode, the receiver is enabled by writing command RX_ON to register bits TRX_CMD (register 0x02, TRX_STATE) in states TRX_OFF or PLL_ON. In Extended Operating Mode, the receiver is enabled for RX_AACK operation from state PLL_ON by writing the command RX_AACK_ON.

There is no additional configuration required to receive IEEE 802.15.4 compliant frames when using the Basic Operating Mode. However, the frame reception in the Extended Operating Mode requires further register configurations. For details, refer to section 5.2.2.

For specific applications, the receiver can be configured to handle critical environments, to simplify the interaction with the microcontroller, or to operate different data rates.

The AT86RF212 receiver has an outstanding sensitivity performance. At certain conditions (interference floor, High Data Rate Modes, refer to section 7.1.4), it may be useful to manually decrease this sensitivity. This is achieved by adjusting the synchronization header detector threshold using register bits RX_PDT_LEVEL (register 0x15, RX_SYN). Received signals with a RSSI value below the threshold do not activate the demodulation process.

Furthermore, it may be useful to protect a received frame against overwriting by subsequent received frames. A Dynamic Frame Buffer Protection is enabled with register bit RX_SAFE_MODE (register 0x0C, TRX_CTRL_2) set, see section 9.7. The receiver remains in RX_ON or RX_AACK_ON state until the whole frame is uploaded by the microcontroller, indicated by /SEL = H during the SPI Frame Receive Mode. The Frame Buffer content is only protected if the FCS is valid.

A Static Frame Buffer Protection is enabled with register bit RX_PDT_DIS (register 0x15, RX_SYN) set. The receiver remains in RX_ON or RX_AACK_ON state and no further SHR is detected until the register bit RX_PDT_DIS is set back.

7.2.3 Register Description

Table 7-6. Register 0x19 (RF_CTRL_1)

Bit	7	6	5	4
Name	RF_MC[3]	RF_MC[2]	RF_MC[1]	RF_MC[0]
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0
Bit	3	2	1	0
Name	Reserved	Reserved	Reserved	Reserved
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0

- **Bit 7:4 – RF_MC**

These register bits provide the matching control of the differential RF pins (RFN, RFP) by switching capacitances to ground, see Figure 2-2. Each step increases the capacitance by 36 fF at each pin. The capacitance setting at the RF pins is valid for both RX and TX operation.

Table 7-7. RF Pin Matching Control

Register Bits	Value	Capacitance at RF Pins [fF]
RF_MC	0	0
	1	36
	2	72
	3	108
	…	…
	15	540

- **Bit 3:0 – Reserved**

Register 0x15 (RX_SYN):

This register controls the sensitivity threshold of the receiver.

Table 7-8. Register 0x15 (RX_SYN)

Bit	7	6	5	4
Name	RX_PDT_DIS	Reserved	Reserved	Reserved
Read/Write	R/W	R	R	R
Reset Value	0	0	0	0
Bit	3	2	1	0
Name	RX_PDT_LEVEL[3]	RX_PDT_LEVEL[2]	RX_PDT_LEVEL[1]	RX_PDT_LEVEL[0]
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0

- **Bit 7 – RX_PDT_DIS**

RX_PDT_DIS = 1 prevents the reception of a frame, even if the radio transceiver is in receive mode. An ongoing frame reception is not affected.

- **Bit 6:4 – Reserved**
- **Bit 3:0 – RX_ PDT_LEVEL**

With these register bits, the receiver can be desensitized such that frames with an RSSI value below a threshold level are not received. The threshold level can be calculated according to the following formula if RX_PDT_LEVEL > 0.

RX_THRES [dBm] = RSSI_BASE_VAL + 3.1 · RX_PDT_LEVEL

RSSI_BASE_VAL is described in section 6.4.3.

If register bits RX_PDT_LEVEL = 0 (reset value), this feature is disabled which corresponds to the highest sensitivity.

If register bits RX_PDT_LEVEL > 0, the current consumption of the receiver in states RX_ON and RX_AACK_ON is reduced by 500 µA, refer to parameter 10.8.2 in section 10.8.

7.3 Transmitter (TX)

7.3.1 Overview

The AT86RF212 transmitter utilizes a direct up-conversion topology. The digital transmitter (TX BBP) generates the in-phase (I) and quadrature (Q) component of the modulation signal. A digital-to-analog converter (DAC) forms the analog modulation signal. A quadrature mixer pair converts the analog modulation signal to the RF domain. The power amplifier (PA) provides signal power delivered to the differential antenna pins (RFP, RFN). Both, the LNA the PA are internally connected to the bidirectional differential antenna pins so that no external antenna switch is needed.

Using the default settings, the PA incorporates an equalizer to improve its linearity. The enhanced linearity keeps the spectral side lobes of the transmit spectrum low in order to meet the requirements of the European 868.3 MHz band.

If the PA boost mode is turned on, the equalizer is disabled. This allows to deliver a higher transmit power of up to 10 dBm at the cost of higher spectral side lobes and higher harmonic power.

In Basic Operating Mode, a transmission is started from PLL_ON state by either writing TX_START to register bits TRX_CMD (register 0x02, TRX_STATE) or by a rising edge of SLP_TR.

In Extended Operating Modes, a transmission might be started automatically depending on the transaction phase of either RX_AACK or TX_ARET, refer to section 5.2.

7.3.2 Frame Transmit Procedure

The frame transmit procedure, including writing PSDU data into the Frame Buffer and initiating a transmission, is described in section 8.2.

7.3.3 Spectrum Masks

The AT86RF212 can be operated in different frequency bands, using different power levels, modulation schemes, chip rates, and pulse shaping filters. The occupied bandwidth of the transmit signal depends on the chosen mode of operation. Values listed in Table 7-9 are based on a default power setting (PHY_TX_PWR = 0x60) and usage of the Continuous Transmission Test Mode with Frame Buffer content {0x01, 0x00}, refer to Appendix A on page 164.

Knowledge of modulation bandwidth, power spectrum, and side lobes is essential for proper system setup, i.e. non-overlapping channel spacing.

Table 7-9. Physical Layer Mode and Occupied Bandwidth

PHY Mode	99% Occupied Bandwidth [kHz]	6 dB Bandwidth [kHz]	20 dB Bandwidth [kHz]
Reference	ETSI EN 300 220 [5]	FCC 15.247 [4]	FCC 15.247 [4]
Detector	RMS	Peak	Peak
Span	2 MHz	2 MHz	2 MHz
RBW	1 kHz	100 kHz	20 kHz
VBW	10 kHz	1 MHz	200 kHz
Sweep	2 s	2 s	2 s
BPSK-20	400	240	480
BPSK-40	760	630	900
OQPSK-SIN-RC-100	330	370	380
OQPSK-SIN-250	1200	730	1220
OQPSK-RC-250	1200	850	1220

Figure 7-4 to Figure 7-8 show power spectra for different modes listed in Table 7-9. The spectra were captured using default settings of AT86RF212. The resolution bandwidth of the spectrum analyzer was set to 30 kHz; the video bandwidth was set to 10 kHz.

Figure 7-4. Spectrum of BPSK-20

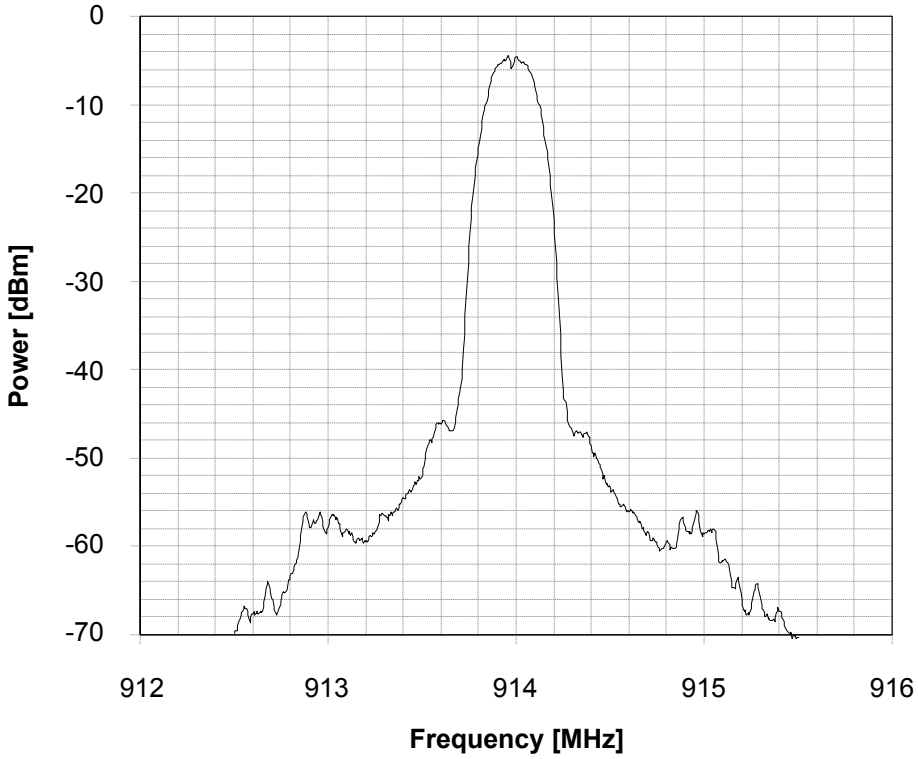


Figure 7-5. Spectrum of BPSK-40

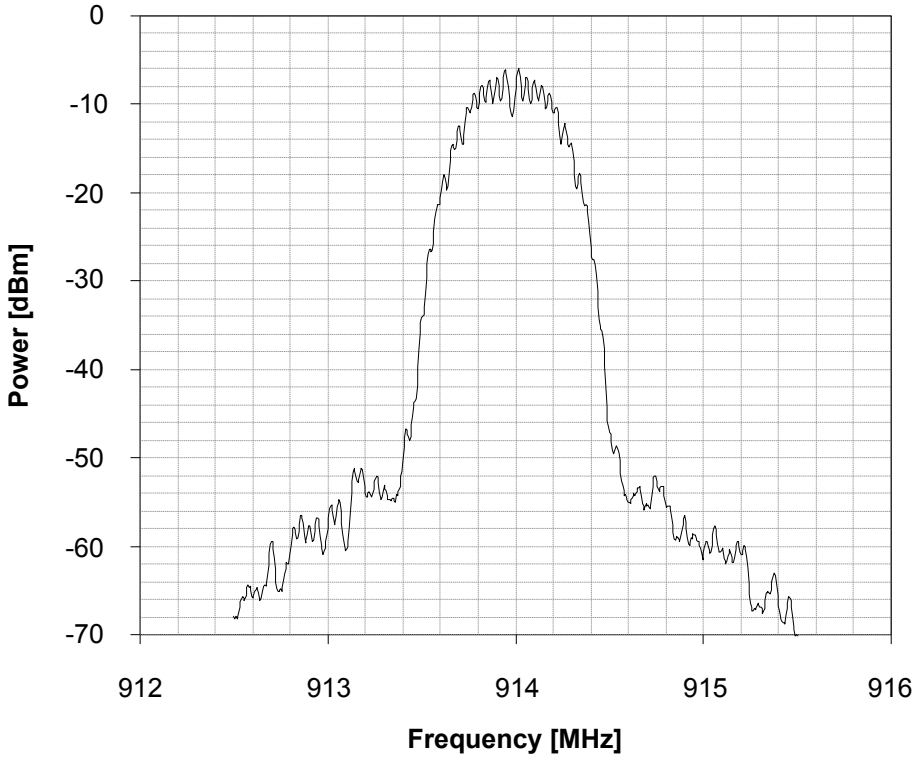


Figure 7-6. Spectrum of OQPSK-SIN-RC-100

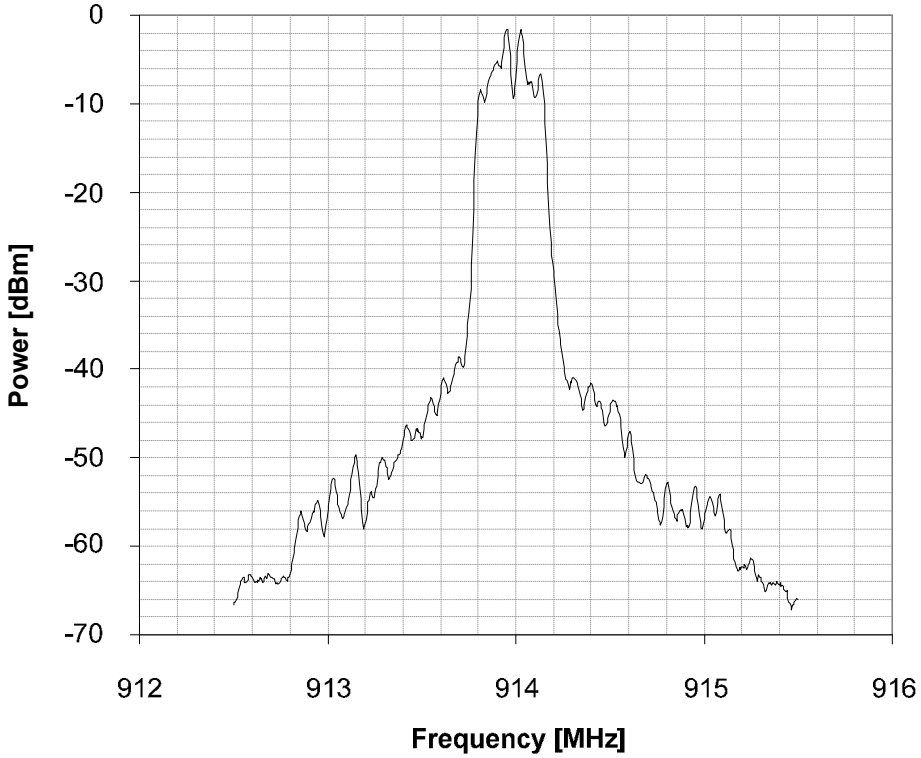


Figure 7-7. Spectrum of OQPSK-SIN-250

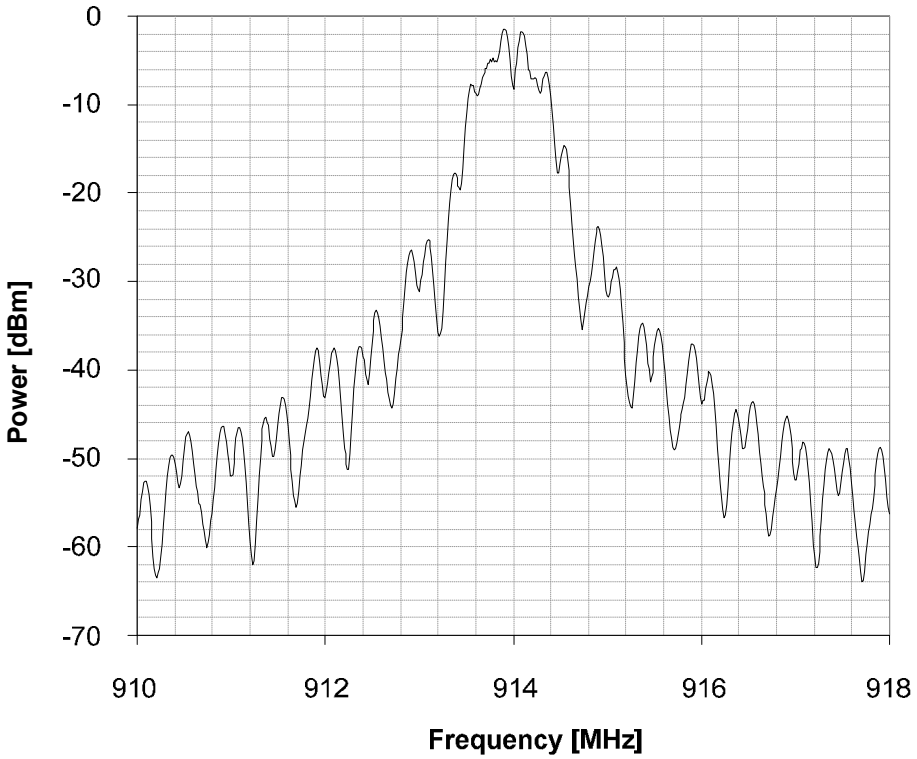


Figure 7-8. Spectrum of OQPSK-RC-250

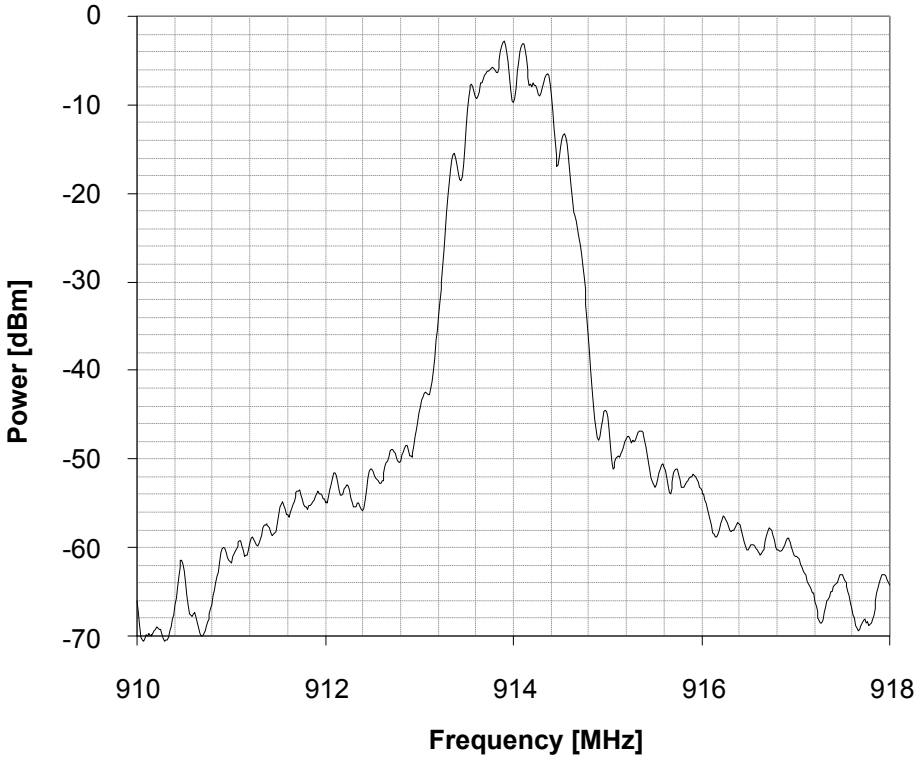


Figure 7-4 to Figure 7-8 illustrate typical spectra of the transmitted signals of the AT86RF212 and do not claim any limits.

Refer to the local authority bodies (FCC, ETSI, etc.) for further details about definition of power spectral density masks, definition of spurious emission, allowed modulation bandwidth, transmit power, and its limits.

7.3.4 TX Output Power

The maximum output power of the transmitter is typically 5 dBm in normal mode and 10 dBm in boost mode. The TX output power can be set via register bits TX_PWR (register 0x05, PHY_TX_PWR). The output power of the transmitter can be controlled down to -11 dBm dB with 1 dB resolution.

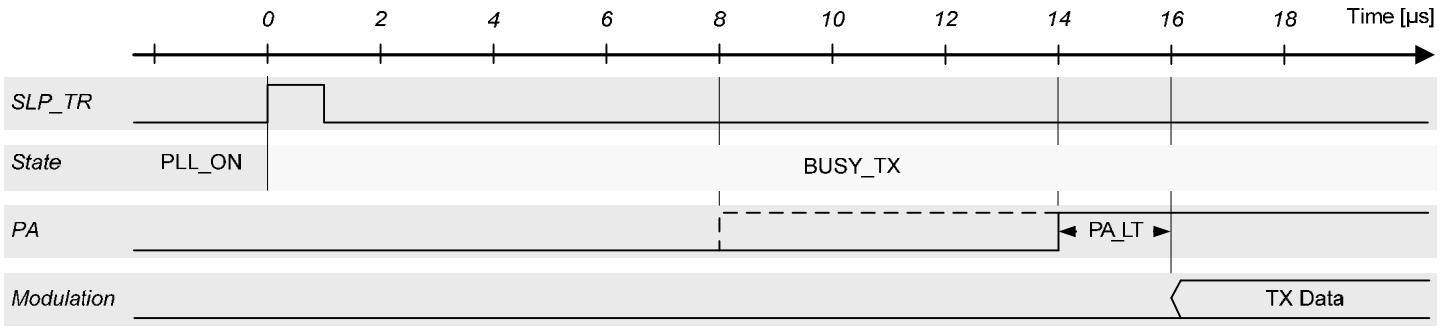
To meet the spectral requirements of the European and Chinese bands, it is necessary to limit the TX power by appropriate setting of TX_PWR, GC_PA (register 0x05, PHY_TX_PWR), and GC_TX_OFFS (register 0x16, TX_CTRL_0). See Table 7-15 and Table 7-16 for recommended values.

7.3.5 TX Power Ramping

To optimize the output power spectral density (PSD), individual transmitter blocks are enabled sequentially. A transmit action is started by either the rising edge of pin SLP_TR or the command TX_START in register 0x02. One symbol period later the data transmission begins. During this time period, the PLL settles to the frequency used for transmission. The PA is enabled prior to the data transmission start. This PA lead time can be adjusted with the value PA_LT in register 0x16 (RF_CTRL_0). The PA is always enabled at the lowest gain value corresponding to GC_PA = 0. Then the PA gain is increased automatically to the value set by GC_PA in register 0x16 (RF_CTRL_0). After transmission is completed, TX power ramping down is performed in an inverse order.

The control signals associated with TX power ramping are shown in Figure 7-9. In this example, the transmission is initiated with the rising edge of pin 11 (SLP_TR). The radio transceiver state changes from PLL_ON to BUSY_TX.

Figure 7-9. TX Power Ramping Example (O-QPSK 250 kbit/s Mode)



Using an external RF front-end (refer to section 9.4), it may be required to adjust the startup time of the external PA relative to the internal building blocks to optimize the overall PSD. This can be achieved using register bits PA_LT (register 0x16, RF_CTRL_0).

7.3.6 Register Description

Register 0x16 (RF_CTRL_0):

This register contains control signals to configure the transmit path.

Table 7-10. Register 0x16 (RF_CTRL_0)

Bit	7	6	5	4
Name	PA_LT[1]	PA_LT[0]	Reserved	Reserved
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	1	1

Bit	3	2	1	0
Name	Reserved	Reserved	GC_TX_OFFS[1]	GC_TX_OFFS[0]
Read/Write	R	R	R/W	R/W
Reset Value	0	0	0	1

- **Bit 7:6 – PA_LT**

These register bits control the lead time of the PA enable signal relative to the TX data start, see Figure 7-9. This allows to enable the PA 2, 4, 6, or 8 µs before the transmit signal starts. The PA enable signal can also be output at pin DIG3/DIG4 to provide a control signal for an external RF front-end; for details, refer to section 9.4.

Table 7-11. PA Enable Time Relative to the TX start

Register Bits	Value	PA Enable Lead Time [µs]
PA_LT	0	2
	1	4
	2	6
	3	8

Setting of PA_LT is only effective in TRX_OFF, PLL_ON, and TX_ARET_ON mode.

- **Bit 5:2 – Reserved**
- **Bit 1:0 – GC_TX_OFFS**

These register bits provide an offset between the TX power control word TX_PWR (register 0x05, PHY_TX_PWR) and the actual TX power. This 2-bit word is added to the TX power control word before it is applied to the circuit block which adjusts the TX power. It can be used to compensate differences of the average TX power depending of the modulation format, see Table 7-16 .

Table 7-12. TX Power Offset

Register Bits	Value	TX Power Offset [dB]
GC_TX_OFFS	0	-1
	1	0
	2	+1
	3	+2

Register 0x05 (PHY_TX_PWR):

This register controls the transmitter output power.

Table 7-13. Register 0x05 (PHY_TX_PWR)

Bit	7	6	5	4
Name	PA_BOOST	GC_PA[1]	GC_PA[0]	TX_PWR[4]
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	1	1	0
Bit	3	2	1	0
Name	TX_PWR[3]	TX_PWR[2]	TX_PWR[1]	TX_PWR[0]
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0

- **Bit 7 – PA_BOOST**

This bit enables the PA boost mode where the TX output power is increased by approximately 5 dB when PA_BOOST = 1. In PA boost mode, the PA linearity is decreased compared to the normal mode when PA_BOOST = 0. This leads to higher spectral side lobes of the TX power spectrum and higher power of the harmonics. Consequently, the higher TX power settings do not fulfill the regulatory requirements of the European 868.3 MHz band regarding spurious emissions in adjacent frequency bands (see ETSI EN 300 220-1, ERC/REC 70-03, and ERC/DEC/(01)04).

- **Bit 6:5 – GC_PA**

These register bits control the gain of the PA by changing its bias current. GC_PA needs to be set in TRX_OFF mode only. It can be used to reduce the supply current in TX mode when a reduced TX power is selected with the TX_PWR control word. A reduced PA bias current causes lower RF gain and lowers the 1 dB- compression point of the PA. Hence, it is advisable to use a reduced bias current of the PA only in combination with lower values of TX_PWR. A reasonable combination of TX_PWR and GC_PA is shown in Table 7-15.

Table 7-14. PA Gain Reduction Relative to the Gain at GC_PA=3

Register Bits	Value	PA Gain [dB]
GC_PA	0	-2.9
	1	-1.3
	2	-0.9
	3	0

- **Bit 4:0 – TX_PWR**

These register bits control the transmitter output power. The value of TX_PWR describes the power reduction relative to the maximum output power. The value GC_TX = 0 provides the maximum output power. The resolution is 1 dB per step. Since TX_PWR adjusts the gain in the TX path prior to the PA, the PA bias setting is not optimal for increased values of TX_PWR regarding PA efficiency.

PA power efficiency can be improved when PA bias is reduced (decreased GC_PA value) along with the TX power setting (increased TX_PWR value). A recommended combination of TX power control (TX_PWR), PA bias control (GC_PA), and PA boost mode (PA_BOOST) is listed in Table 7-15. It is a recommended mapping of intended TX power to the 8-bit word in register 0x05. The value of TX_PWR shall be within the range of 0 to 13 to guarantee the transmit signal quality.

Table 7-15. Recommended Mapping of TX Power, Frequency Band, and PHY_TX_PWR (register 0x05)

TX Power [dBm]	PHY_TX_PWR (register 0x05)							
	915 MHz North American Band PHY Modes: BPSK-40, OQPSK-SIN-{250,500,1000}		868.3 MHz European Band PHY Modes: BPSK-20, OQPSK-SIN-RC-{100,200,400}				780 MHz Chinese Band PHY Modes: OQPSK-RC-{250,500,1000}	
			EU1		EU2			
10	0xe1	Note 1						
9	0xa1							
8	0x81						0xe4	Note 6
7	0x82	Note 2					0xe5	
6	0x83						0xe6	
5	0x84				0xe8	Note 4	0xe8	Note 7
4	0x85	Note 3	0x62	Note 4	0xe9		0xe9	
3	0x42		0x63		0xea		0xea	
2	0x22		0x64		0xeb	Note 5	0xca	
1	0x23		0x65		0xab		0xaa	
0	0x24		0x66		0xac		0xab	
-1	0x25		0x47	Note 5	0xad		0xac	
-2	0x04		0x48		0x48		0x46	
-3	0x05		0x28		0x28		0x25	
-4	0x06		0x29		0x29		0x03	
-5	0x07		0x2a		0x2a		0x04	
-6	0x08		0x08		0x08		0x05	
-7	0x09		0x09		0x09		0x06	
-8	0x0a		0x0a		0x0a		0x07	
-9	0x0b		0x0b		0x0b		0x08	
-10	0x0c		0x0c		0x0c		0x09	
-11	0x0d		0x0d		0x0d		0x0a	

Note 1: Power settings can be used with BPSK-40 and O-QPSK-SIN-250. It is recommended to limit the maximum output power of the O-QPSK-SIN-{500,1000} modes because these modes are more sensitive to non-linearities than the 250 kbit/s mode with larger spreading.

Note 2: Power settings can be used with BPSK-40 and O-QPSK-SIN-{250,500}.

Note 3: Power settings can be used with BPSK-40 and O-QPSK-SIN-{250,500,1000}.

Note 4: Power settings can be used with BPSK-20. Spectral side lobes remain < -36 dBm / 100 kHz measured with a RMS detector outside the 868.0-868.6 MHz band.

Note 5: Power settings can be used with both BPSK-20 and O-QPSK-SIN-RC-{100, 200,400}. Spectral side lobes remain < -36 dBm / 100 kHz measured with a RMS detector outside the 868.0-868.6 MHz band.

Note 6: Power settings can be used with OQPSK-RC-{250,500}. Spectral side lobes remain < -36 dBm / 100 kHz measured with a RMS detector outside F_c ± 1 MHz.

Note 7: Power settings can be used with OQPSK-RC-{250,500,1000}. Spectral side lobes remain < -36 dBm / 100 kHz measured with a RMS detector outside F_c ± 1 MHz.

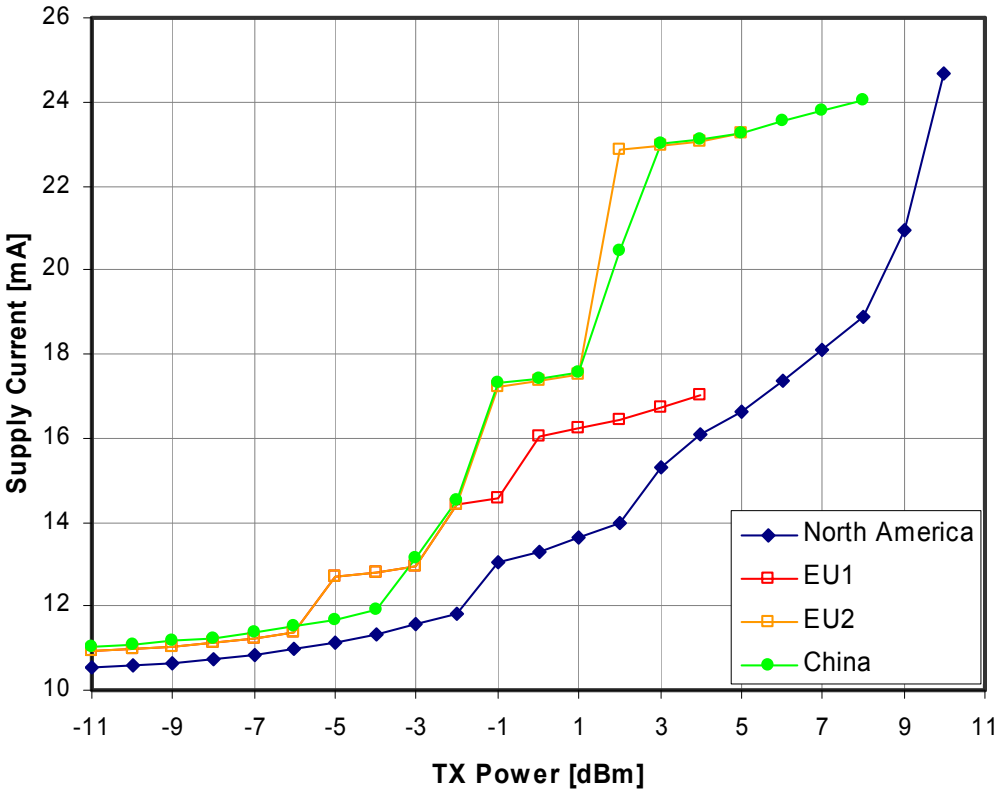
Values of Table 7-15 are based on a mode dependent setting of GC_TX_OFFS (register 0x16, RF_CTRL_0) which is shown in Table 7-16.

Table 7-16. Mode-dependent setting of GC_TX_OFFS

Mode	BPSK	O-QPSK
GC_TX_OFFS	3	2

Figure 7-10 shows supply currents for O-QPSK modulation based on Table 7-15.

Figure 7-10. Supply Currents for O-QPSK Modulation depending on TX Power Setting (according to Table 7-15)



The North American mapping table is optimized for lowest supply current. The more relaxed spectral side lobe requirements of the IEEE 802.15.4 standard are fulfilled.

The EU1 and EU2 mapping tables take into account that linearity is needed to keep the out-of-band spurious emissions below the ETSI requirements, refer to [5]. Regulatory requirements with respect to power density (depending on the frequency band used) are not considered, refer to [6].

The map EU1 takes more supply current than the North American map and uses the normal (linearized) PA mode to provide medium output power up to -1 dBm for O-QPSK-SIN-RC-{100/200/400} modes and 4 dBm for BPSK-20 mode.

The map EU2 uses the boost mode to provide higher TX power levels at the expense of higher supply current. As a result, the maximum TX power is 2 dBm for O-QPSK-SIN-RC-{100/200/400} and 5 dBm for BPSK-20.

Due to great regional distinctions of regulatory requirements, it is not possible to cover all restrictions in this data sheet. Manufactures must take the responsibility to check measurement results against the latest regulations of nations into which they market.

7.4 Frame Buffer

The AT86RF212 contains a 128 byte dual port SRAM. One port is connected to the SPI interface, the other one to the internal transmitter and receiver modules. For data communication, both ports are independent and simultaneously accessible.

The Frame Buffer utilizes the SRAM address space 0x00 to 0x7F for RX and TX operation of the radio transceiver and can keep a single IEEE 802.15.4 RX or a single TX frame of maximum length at a time.

Frame Buffer access modes are described in section 4.3.2. Frame Buffer access conflicts are indicated by an underrun interrupt IRQ_6 (TRX_UR). Note that this interrupt also occurs on the attempt to write frames longer than 127 octets to the Frame Buffer (overflow). In this case, the content of the Frame Buffer is undefined.

Frame Buffer access is only possible if the digital voltage regulator is turned on. This is valid in all device states except in SLEEP state. An access in P_ON state is possible once pin 17 (CLKM) provides the 1 MHz master clock.

7.4.1 Data Management

Data in Frame Buffer (received data or data to be transmitted) can be changed by:

- Frame Buffer or SRAM write access over SPI
- receiving a new frame in BUSY_RX or BUSY_RX_AACK state
- a change into SLEEP state
- a reset

By default, there is no protection of the Frame Buffer against overwriting. Therefore, if a frame is received during Frame Buffer read access of a previously received frame, interrupt IRQ_6 (TRX_UR) is issued and the stored data might be overwritten.

Even so, the old frame data can be read if the SPI data rate is higher than the effective over air data rate. For a data rate of 250 kbit/s, a minimum SPI clock rate of 1 MHz is recommended. Finally, the microcontroller should check the transferred frame data integrity by an FCS check.

To protect the Frame Buffer content against being overwritten by newly incoming frames, the radio transceiver state should be changed to PLL_ON state after reception. This can be achieved by writing the command PLL_ON to register bits TRX_CMD (register 0x02, TRX_STATE) while or immediately after receiving the frame. Alternatively, Dynamic Frame Buffer Protection can be used to protect received frames against overwriting; for details, refer to section 9.7. Both procedures do not protect the Frame Buffer from overwriting by the microcontroller.

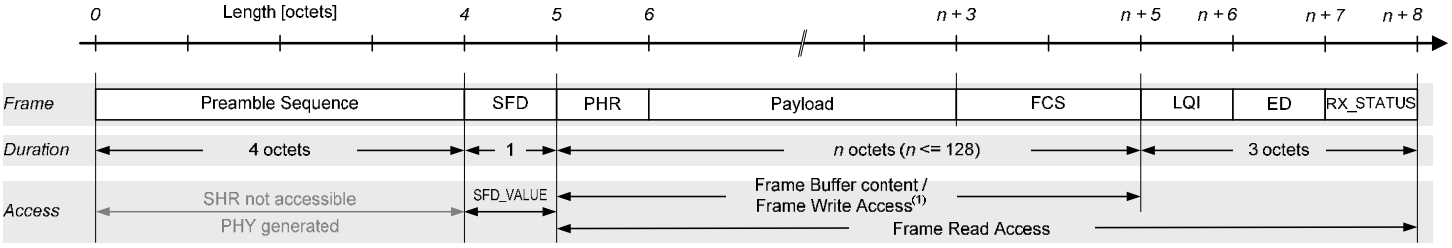
In Extended Operating Mode during TX_ARET operation (see section 5.2.4), the radio transceiver switches to receive state if an acknowledgement of a previously transmitted frame was requested. During this period, received frames are evaluated but not stored in the Frame Buffer. This allows the radio transceiver to wait for an acknowledgement frame and retry the frame transmission without writing the frame again.

A radio transceiver state change, except a transition to SLEEP state or a reset, does not affect the Frame Buffer content. If the radio transceiver is taken into SLEEP, the Frame Buffer is powered off and the stored data get lost.

7.4.2 Frame Content

The AT86RF212 supports an IEEE 802.15.4 compliant frame format as shown in Figure 7-11.

Figure 7-11. AT86RF212 Frame Structure



Note: 1. Writing the FCS can be omitted if TX_AUTO_CRC_ON = 1 (register 0x04, TRX_CTRL_1).

A frame comprises two sections, the radio transceiver internally generated SHR field and the user accessible part stored in the Frame Buffer. The SHR contains the preamble and the SFD field. The variable frame section contains the PHR and the PSDU including the FCS, see section 6.3. To access the data, follow the procedures described in section 4.3.2.

The frame length information (PHR field) and the PSDU are stored in the Frame Buffer. During frame reception, the link quality indicator (LQI) value, the energy detection (ED) value, and the status information (RX_STATUS) of a received frame are additionally stored. The radio transceiver appends these values to the frame data during Frame Buffer read access. For more information, see sections 6.8, 6.5, and 4.3.2, respectively.

If the SRAM read access is used to read an RX frame, the frame length field (PHR) can be accessed at address 0. The SHR (except the SFD value used to generate the SHR) cannot be read by the microcontroller.

For frame transmission, the PHR and the PSDU need to be stored in the Frame Buffer. The maximum Frame Buffer size supported by the radio transceiver is 128 bytes. If the TX_AUTO_CRC_ON bit is set in register 0x05 (PHY_TX_PWR), the FCS field of the PSDU is replaced by the automatically calculated FCS during frame transmission. There is no need to write the FCS field when using the automatic FCS generation.

To manipulate individual bytes of the Frame Buffer, a SRAM write access can be used.

For non IEEE 802.15.4 compliant frames, the minimum frame length supported by the radio transceiver is 1 byte (Frame Length Field + 1 byte of data).

7.4.3 Interrupt Handling

Access conflicts may occur when reading and writing data simultaneously at the independent ports of the Frame Buffer, TX/RX BBP and SPI. These ports have their own address counter that points to the Frame Buffer's current address.

Access violations may cause data corruption and are indicated by IRQ_6 (TRX_UR) interrupt when using the Frame Buffer access mode. Note that access violations are not indicated when using the SRAM access mode.

While receiving a frame, first the data need to be stored in the Frame Buffer before reading it. This can be ensured by accessing the Frame Buffer at least 8 symbols (BPSK) or 2 symbols (O-QPSK) after interrupt IRQ_2 (RX_START). When reading the frame data continuously, the SPI data rate shall be lower than the current TRX bit rate to ensure no underrun interrupt occurs. To avoid access conflicts and to simplify the Frame Buffer read access, Frame Buffer Empty indication may be used; for details, refer to section 9.6.

When writing data to the Frame Buffer during frame transmission, the SPI data rate shall be higher than the PHY data rate avoiding underrun. The first byte of the PSDU data must be available in the Frame Buffer before SFD transmission is complete, which takes 41 symbol periods for BPSK (1 symbol PA ramp up + 40 symbols SHR) and 11 symbol periods for O-QPSK (1 symbol PA ramp up + 10 symbols SHR) from the rising edge of SLP_TR pin (see Figure 5-2).

Notes

- Interrupt IRQ_6 (TRX_UR) is valid 2 octets after IRQ_2 (RX_START).
- If a Frame Buffer read access is not finished until a new frame is received, a TRX_UR interrupt occurs. Nevertheless, the old frame data can be read if the SPI data rate is higher than the effective PHY data rate. A minimum SPI clock rate of 1 MHz is recommended in this case. Finally, the microcontroller should check the integrity of the transferred frame data by calculating the FCS.

7.5 Voltage Regulators (AVREG, DVREG)

The main features of the Voltage Regulator blocks are:

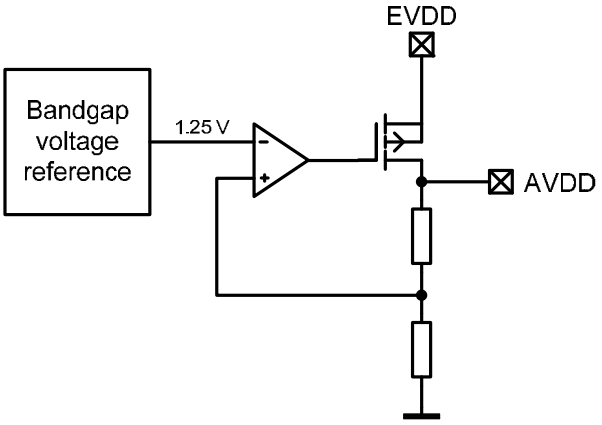
- Bandgap stabilized 1.8 V supply for analog and digital domain
- Low dropout (LDO) voltage regulator
- Configurable for usage of an external voltage regulator

7.5.1 Overview

The internal voltage regulators supply a stabilized voltage to the AT86RF212. The AVREG provides the regulated 1.8 V supply voltage for the analog domain and the DVREG supplies the 1.8 V supply voltage for the digital domain.

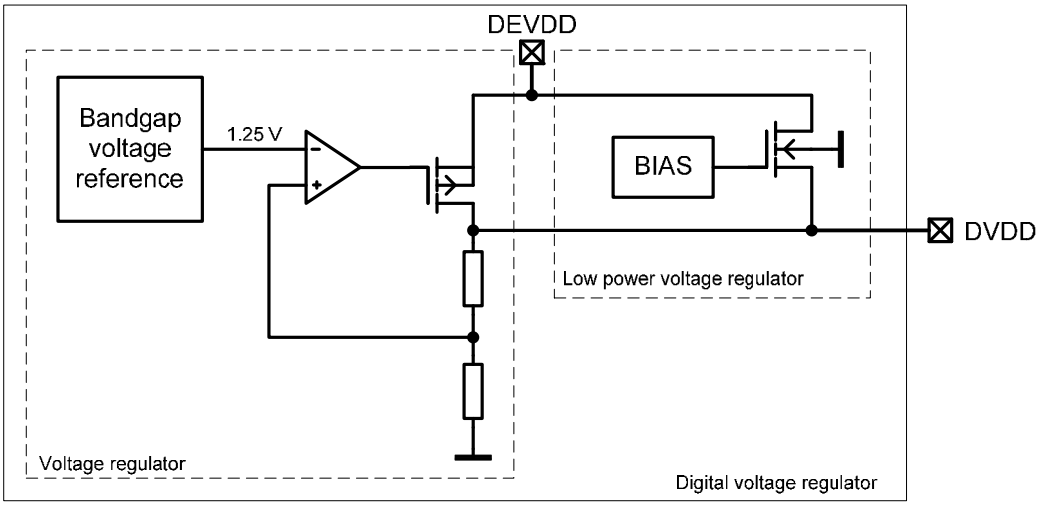
A simplified schematic of the internal analog voltage regulator is shown in Figure 7-12.

Figure 7-12. Simplified Schematic of AVREG



A simplified schematic of the internal digital voltage regulator is shown in Figure 7-13.

Figure 7-13. Simplified Schematic of DVREG



The block “Low power voltage regulator” within the “Digital voltage regulator” maintains the DVDD supply voltage when the voltage regulator is disabled, which is the case during sleep mode. The DVDD voltage drops down to 1.5 V (typical) if the AT86RF212 is in sleep mode; all configuration register values are stored.

The low power voltage regulator is always enabled. Therefore, its bias current contributes to the leakage current in sleep mode of about 100 nA (typical).

The voltage regulators (AVREG, DVREG) require bypass capacitors for stable operation. The value of the bypass capacitors determine the settling time of the voltage regulators. The bypass capacitors shall be placed as close as possible to the pins and shall be connected to ground with the shortest possible traces (see Table 3-1).

7.5.2 Configuration

The voltage regulators can be configured by the register 0x10 (VREG_CTRL).

It is recommended to use the internal regulators, but it is also possible to supply the low voltage domains by an external voltage supply. For this configuration, the internal

regulators need to be switched off by setting the register bits to the values AVREG_EXT = 1 and DVREG_EXT = 1. A regulated external supply voltage of 1.8 V needs to be connected to the pins 13, 14 (DVDD), and pin 29 (AVDD). When turning on the external supply, ensure a sufficiently long stabilization time before interacting with the AT86RF212.

7.5.3 Data Interpretation

The status bits AVDD_OK = 1 and DVDD_OK = 1 of register 0x10 (VREG_CTRL) indicate an enabled and stable internal supply voltage. Reading value 0 indicates a disabled voltage regulator or the internal supply voltage is not settled to the final value. Setting AVREG_EXT = 1 and DVREG_EXT = 1 forces the signals AVDD_OK and DVDD_OK to 1.

7.5.4 Register Description

Register 0x10 (VREG_CTRL):

This register controls the use of the voltage regulators and indicates the status of these.

Table 7-17. Register 0x10 (VREG_CTRL)

Bit	7	6	5	4
Name	AVREG_EXT	AVDD_OK	Reserved	Reserved
Read/Write	R/W	R	R/W	R/W
Reset Value	0	0	0	0
Bit	3	2	1	0
Name	DVREG_EXT	DVDD_OK	Reserved	Reserved
Read/Write	R/W	R	R/W	R/W
Reset Value	0	0	0	0

- **Bit 7 – AVREG_EXT**

If set, this register bit disables the internal analog voltage regulator to apply an external regulated 1.8 V supply for the analog building blocks.

Table 7-18. Regulated Voltage Supply Control for Analog Building Blocks

Register Bit	Value	Description
AVREG_EXT	0	Internal voltage regulator enabled (analog domain)
	1	Internal voltage regulator disabled; use external regulated 1.8 V supply voltage for the analog domain

- **Bit 6 – AVDD_OK**

This register bit indicates if the internal 1.8 V regulated voltage supply AVDD has settled. The bit is set to logic high if AVREG_EXT = 1.

Table 7-19. Regulated Voltage Supply Control for Analog Building Blocks

Register Bit	Value	Description
AVDD_OK	0	Analog voltage regulator disabled or supply voltage not stable
	1	Analog supply voltage has settled

- **Bit 5:4 – Reserved**

- **Bit 3 – DVREG_EXT**

If set, this register bit disables the internal digital voltage regulator to apply an external regulated 1.8 V supply for the digital building blocks.

Table 7-20. Regulated Voltage Supply Control for Digital Building Blocks

Register Bit	Value	Description
DVREG_EXT	0	Internal voltage regulator enabled (digital domain)
	1	Internal voltage regulator disabled; use external regulated 1.8 V supply voltage for the digital domain

- **Bit 2 – DVDD_OK**

This register bit indicates if the internal 1.8 V regulated voltage supply DVDD has settled. The bit is set to logic high if DVREG_EXT = 1.

Table 7-21. Regulated Voltage Supply Control for Digital Building Blocks

Register Bit	Value	Description
DVDD_OK	0	Digital voltage regulator disabled or supply voltage not stable
	1	Digital supply voltage has settled

While the reset value of this bit is 0, any practical access to the register is only possible when DVREG is active. So this bit is normally always read out as 1.

- **Bit 1:0 – Reserved**

Register 0x0C (TRX_CTRL_2):

This register controls the TRX behavior.

Table 7-22. Register 0x0C (TRX_CTRL_2)

Bit	7	6	5	4
Name	RX_SAFE_MODE	TRX_OFF_AVDD_EN	OQPSK_SCRAM_EN	OQPSK_SUB1_RC_EN
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	1	0

Bit	3	2	1	0
Name	BPSK_OQPSK	SUB_MODE	OQPSK_DATA_RATE	OQPSK_DATA_RATE
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	1	0	0

- **Bit 7 – RX_SAFE_MODE**

Refer to section 9.7.2.

- **Bit 6 – TRX_OFF_AVDD_EN**

If this register bit is set, the analog voltage regulator is turned on (kept on) during TRX_OFF, enabling faster RX/TX turn on time. This is especially useful for a short stopover in TRX_OFF state. The recharge time for capacitances is avoided in this case. The current consumption increases by typical 100 µA.

- **Bit 5:0**

Refer to section 7.1.5.

7.6 Battery Monitor (BATMON)

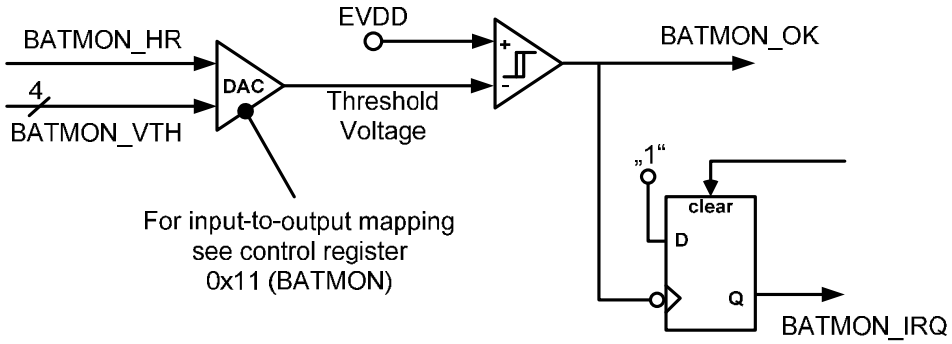
The main features of the battery monitor are:

- Configurable voltage threshold from 1.7 V to 3.675 V
- Generation of an interrupt when supply voltage drops below the threshold
- Current state can be monitored in a register bit

7.6.1 Overview

The battery monitor (BATMON) detects and indicates a low voltage of the external supply voltage at pin 28 (EVDD). This is done by comparing the voltage on the external supply pin 28 (EVDD) with a configurable internal threshold voltage. A simplified schematic of the BATMON with the most important input and output signals is shown in Figure 7-14.

Figure 7-14. Simplified Schematic of BATMON



7.6.2 Configuration

The BATMON can be configured using the register 0x11 (BATMON). Register subfield BATMON_VTH sets the threshold voltage. It is configurable with a resolution of 75 mV in the upper voltage range (BATMON_HR = 1) and with a resolution of 50 mV in the lower voltage range (BATMON_HR = 0); for details, refer to register 0x11 (BATMON).

7.6.3 Data Interpretation

The register bit BATMON_OK of register 0x11 (BATMON) represents the current value of the supply voltage:

- If BATMON_OK = 0, the supply voltage is lower than the threshold voltage.
- If BATMON_OK = 1, the supply voltage is higher than the threshold voltage.

After setting a new threshold, the value BATMON_OK should be read out to verify the current supply voltage value.

Note, the battery monitor is inactive during P_ON and SLEEP states, see status register 0x01 (TRX_STATUS).

7.6.4 Interrupt Handling

A supply voltage drop below the configured threshold value is indicated by interrupt IRQ_7 (BAT_LOW), see section 4.7. Note that the interrupt is issued only if BATMON_OK changes from 1 to 0.

No interrupt is generated when

- the supply voltage is below the default 1.8 V threshold at power up (BATMON_OK was never 1), or
- a new threshold is set which is still above the current supply voltage (BATMON_OK remains 0).

When the battery voltage is close to the programmed threshold voltage, noise or temporary voltage drops may generate unwanted interrupts. To avoid this,

- disable the IRQ_7 (BAT_LOW) in register 0x0E (IRQ_MASK) and treat the battery as empty, or
- set a lower threshold value.

7.6.5 Register Description

Register 0x11 (BATMON):

This register configures the battery monitor to compare the supply voltage at pin 28 (EVDD) to the threshold. Additionally, the supply voltage status at pin 28 (EVDD) can be read from register bit BATMON_OK according to the actual BATMON settings.

Table 7-23. Register 0x11 (BATMON)

Bit	7	6	5	4
Name	PLL_LOCK_CP	Reserved	BATMON_OK	BATMON_HR
Read/Write	R	R/W	R	R/W
Reset Value	0	0	0	0

Bit	3	2	1	0
Name	BATMON_VTH[3]	BATMON_VTH[2]	BATMON_VTH[1]	BATMON_VTH[0]
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	1	0

- **Bit 7 – PLL_LOCK_CP**

Refer to section 7.8.6.

- **Bit 6 – Reserved**
- **Bit 5 – BATMON_OK**

The register bit BATMON_OK indicates the level of the external supply voltage with respect to the programmed threshold BATMON_VTH.

Table 7-24. Battery Monitor Status

Register Bit	Value	Description
BATMON_OK	0	The battery voltage is below the threshold.
	1	The battery voltage is above the threshold.

- **Bit 4 – BATMON_HR**

The register bit BATMON_HR sets the range and resolution of the battery monitor.

Table 7-25. Battery Monitor Range Selection

Register Bit	Value	Description
BATMON_HR	0	Enables the low range, see BATMON_VTH
	1	Enables the high range, see BATMON_VTH

- **Bit 3:0 – BATMON_VTH**

The threshold value for the battery monitor is set by register bits BATMON_VTH.

Table 7-26. Battery Monitor Threshold Voltage

Value BATMON_VTH[3:0]	Voltage [V] if BATMON_HR = 1	Voltage [V] if BATMON_HR = 0
0x0	2.550	1.70
0x1	2.625	1.75
0x2	2.700	1.80
0x3	2.775	1.85
0x4	2.850	1.90
0x5	2.925	1.95
0x6	3.000	2.00
0x7	3.075	2.05
0x8	3.150	2.10
0x9	3.225	2.15
0xA	3.300	2.20
0xB	3.375	2.25
0xC	3.450	2.30
0xD	3.525	2.35
0xE	3.600	2.40
0xF	3.675	2.45

7.7 Crystal Oscillator (XOSC) and Clock Output (CLKM)

The main features are:

- 16 MHz amplitude-controlled crystal oscillator
- Fast settling time after leaving SLEEP state
- Configurable trimming capacitance array
- Configurable clock output (CLKM)

7.7.1 Overview

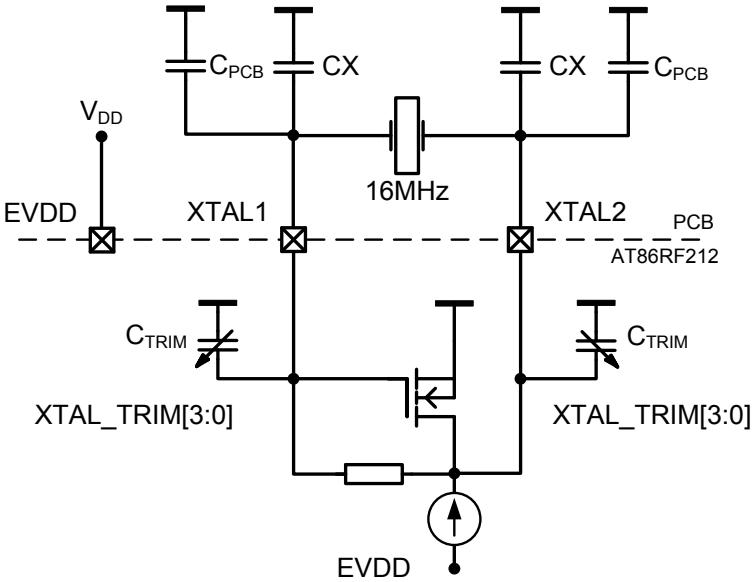
The crystal oscillator generates the reference frequency for the AT86RF212. All other internally generated frequencies of the radio transceiver are derived from this frequency. Therefore, the overall system performance is mainly determined by the accuracy of crystal reference frequency. The external components of the crystal oscillator should be selected carefully and the related board layout should be done with caution (see section 3).

Two operating modes are supported. The recommended mode is the integrated oscillator setup as described in Figure 7-15. Alternatively, a reference frequency can be fed to the internal circuitry by using an external clock reference as shown in Figure 7-16. The XOSC operating modes are configurable by register 0x12 (XOSC_CTRL).

7.7.2 Integrated Oscillator Setup

Using the internal oscillator, the oscillation frequency depends on the load capacitance between the crystal pins XTAL1 and XTAL2. The total load capacitance C_L must be equal to the specified load capacitance of the crystal itself. It consists of the external capacitors CX and parasitic capacitances connected to the XTAL nodes. Figure 7-15 shows parasitic capacitances, such as PCB stray capacitances.

Figure 7-15. Simplified XOSC Schematic with External Components



Additional internal trimming capacitors C_{TRIM} are available. Values in the range from 0 pF to 4.5 pF with 0.3 pF resolution are selectable using the bits XTAL_TRIM of register 0x12 (XOSC_CTRL). To calculate the total load capacitance, the following formula can be used while C_{PAR} represents the pin input capacitance defined in Table 2-2.

$$C_L = 0.5 \cdot (CX + C_{TRIM} + C_{PAR} + C_{PCB})$$

The trimming capacitors provide the possibility of reducing frequency deviations caused by production process variations or by external components tolerances. Note that the oscillation frequency can only be reduced by increasing the trimming capacitance. The frequency deviation caused by one step of C_{TRIM} decreases with increasing crystal load capacitor values.

An amplitude control circuit is included to ensure stable operation under different operating conditions and for different crystal types. Enabling the crystal oscillator in P_ON state and after leaving SLEEP state causes a slightly higher current during the amplitude build-up phase to guarantee a short start-up time. At stable operation, the current is reduced to the amount necessary for a robust operation. This also keeps the drive level of the crystal low.

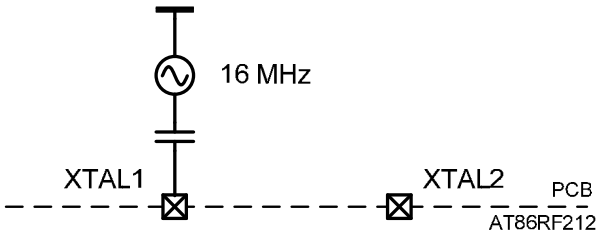
Generally, crystals with a higher load capacitance are less sensitive to parasitic pulling effects caused by external component variations or by variations of board and circuit parasitics. On the other hand, a larger crystal load capacitance results in a longer start-up time and a higher steady state current consumption.

7.7.3 External Reference Frequency Setup

When using an external reference frequency, the signal must be connected to pin 26 (XTAL1) as indicated in Figure 7-16. The oscillation peak-to-peak amplitude shall be between 100 mV and 500 mV; the optimum range is between 400 mV and 500 mV. It is possible, among other things, to use sine and square wave signals. Note that the quality of the external reference (i.e. phase noise) determines the system performance.

Pin 25 (XTAL2) should not be wired. For power saving reasons, it is recommended to set register bits XTAL_MODE (register 0x12, XOSC_CTRL) to the external oscillator mode.

Figure 7-16. Setup for Using an External Frequency Reference



7.7.4 Master Clock Signal Output (CLKM)

The generated reference clock signal can be fed into a microcontroller using pin 17 (CLKM). The internal 16 MHz raw clock can be divided by an internal prescaler. Thus, clock frequencies of 16 MHz, 8 MHz, 4 MHz, 2 MHz, 1 MHz, 250 kHz, or the current SHR symbol rate frequency can be supplied by pin CLKM.

The CLKM frequency, update scheme, and pin driver strength is configurable using register 0x03 (TRX_CTRL_0). There are two possibilities how a CLKM frequency change gets effective. If CLKM_SHA_SEL = 0 and/or CLKM_CTRL = 0, changing the register bits CLKM_CTRL immediately affects the CLKM clock rate. Otherwise (CLKM_SHA_SEL = 1 and CLKM_CTRL > 0 before changing the register bits CLKM_CTRL), the new clock rate is supplied when leaving the SLEEP state the next time.

To reduce power consumption and spurious emissions, it is recommended to turn off the CLKM clock when not in use or to reduce its driver strength to a minimum, refer to section 2.2.2.

CLKM reset behavior

During reset procedure (see section 5.1.4.5), register bits CLKM_CTRL are shadowed. Although the clock setting of CLKM remains after reset, a read access to register bits CLKM_CTRL delivers the reset value 1. For that reason, it is recommended to write the previous configuration (before reset) to register bits CLKM_CTRL (after reset) to align the radio transceiver behavior and register configuration. Otherwise, the CLKM clock rate is set back to the reset value (1 MHz) after the next SLEEP cycle.

For example, if the CLKM clock rate is configured to 16 MHz, the CLKM clock rate remains at 16 MHz after a reset, however, the register bits CLKM_CTRL are set back to 1. Since CLKM_SHA_SEL reset value is 1, the CLKM clock rate changes to 1 MHz after the next SLEEP cycle if the CLKM_CTRL setting is not updated.

7.7.5 Clock Jitter

AT86RF212 provides receiver sensitivities up to -110 dBm. Detection of such small RF signals requires very clean scenarios with respect to noise and interference. Harmonics of digital signals may degrade the performance if they interfere with the wanted RF signal. A small clock jitter of digital signals can spread harmonics over a wider frequency range, thus reducing the power of certain spectral lines. AT86RF212 provides such a clock jitter as an optional feature. The jitter module is working for the receiver part and all I/O signals, e.g. CLKM if enabled. The transmitter part and RF frequency generation are not influenced.

7.7.6 Register Description

Register 0x03 (TRX_CTRL_0):

Table 7-27. Register 0x03 (TRX_CTRL_0)

Bit	7	6	5	4
Name	PAD_IO[1]	PAD_IO[0]	PAD_IO_CLKM[1]	PAD_IO_CLKM[0]
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	0	1
Bit	3	2	1	0
Name	CLKM_SHA_SEL	CLKM_CTRL[2]	CLKM_CTRL[1]	CLKM_CTRL[0]
Read/Write	R/W	R/W	R/W	R/W
Reset Value	1	0	0	1

The TRX_CTRL_0 register controls the drive current of the digital outputs and the CLKM clock rate. It is recommended using the lowest value for the drive current to reduce the current consumption and the emission of signal harmonics.

- **Bit 7:6 – PAD_IO**

Refer to section 2.2.2.3.

- **Bit 5:4 – PAD_IO_CLKM**

These register bits set the output driver strength of pin CLKM. It is recommended to reduce the driver strength to 2 mA (PAD_IO_CLKM = 0) if possible. This reduces power consumption and spurious emissions.

Table 7-28. CLKM Driver Strength

Register Bits	Value	Description
PAD_IO_CLKM	0	2 mA
	1	4 mA
	2	6 mA
	3	8 mA

- **Bit 3 – CLKM_SHA_SEL**

The register bit CLKM_SHA_SEL defines whether a new clock rate (defined by CLKM_CTRL) is set immediately or gets effective after the next SLEEP cycle.

Table 7-29. CLKM Clock Rate Update Scheme

Register Bit	Value	Description
CLKM_SHA_SEL	0	CLKM clock rate change appears immediately
	1	CLKM clock rate change appears after SLEEP cycle

- **Bit 2:0 – CLKM_CTRL**

These register bits set the clock rate of pin 17 (CLKM).

Table 7-30. Clock Rate Setting at Pin CLKM

Register Bits	Value	Description		
CLKM_CTRL	0	No clock at pin 17 (CLKM); pin set to logic low		
	1	1 MHz		
	2	2 MHz		
	3	4 MHz		
	4	8 MHz		
	5	16 MHz		
	6	250 kHz		
	7	IEEE 802.15.4 symbol rate frequencies		
		BPSK_OQPSK (1)	SUB_MODE (1)	Frequency
		0	0	20 kHz
		0	1	40 kHz
		1	0	25 kHz
		1	1	62.5 kHz

Note: 1. Refer to section 7.1.5

Register 0x12 (XOSC_CTRL):

The register XOSC_CTRL configures the crystal oscillator.

Table 7-31. Register 0x12 (XOSC_CTRL)

Bit	7	6	5	4
Name	XTAL_MODE[3]	XTAL_MODE[2]	XTAL_MODE[1]	XTAL_MODE[0]
Read/Write	R/W	R/W	R/W	R/W
Reset Value	1	1	1	1
Bit	3	2	1	0
Name	XTAL_TRIM[3]	XTAL_TRIM[2]	XTAL_TRIM[1]	XTAL_TRIM[0]
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0

- **Bit 7:4 – XTAL_MODE**

These register bits set the operating mode of the crystal oscillator, see Table 7-32.

Table 7-32. Crystal Oscillator Operating Mode

Register Bits	Value	Description
XTAL_MODE	0x4	Internal crystal oscillator disabled; use external reference frequency
	0xF	Internal crystal oscillator enabled
	Other	Reserved

- **Bit 3:0 – XTAL_TRIM**

The register bits XTAL_TRIM control the two internal capacitance arrays connected to pins XTAL1 and XTAL2. A capacitance value in the range from 0 pF to 4.5 pF is selectable with a resolution of 0.3 pF.

Table 7-33. Crystal Oscillator Trimming Capacitors

Register Bits	Value	Description
XTAL_TRIM	0x0	0.0 pF
	0x1	0.3 pF
	…	…
	0xF	4.5 pF
	Other	Reserved

Register 0x0A (RX_CTRL):

The register RX_CTRL configures the clock jitter.

Table 7-34. Register 0x0A (RX_CTRL)

Bit	7	6	5	4
Name	Reserved	Reserved	JCM_EN	Reserved
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	0	1

Bit	3	2	1	0
Name	Reserved	Reserved	Reserved	Reserved
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	1	1	1

- **Bit 7:6 – Reserved**
- **Bit 5 – JCM_EN**

If this bit is set, the jitter module is enabled.

- **Bit 4:0 – Reserved**

7.8 Frequency Synthesizer (PLL)

The main PLL features are:

- Generate RX/TX frequencies for all supported channels
- Autonomous calibration loops for stable operation within the operating range
- Two PLL interrupts for status indication
- Fast PLL settling to support frequency hopping

7.8.1 Overview

The PLL generates the RF frequencies for the AT86RF212. During receive and transmit operations, the frequency synthesizer operates as a local oscillator. The frequency synthesizer is implemented as a fractional-N PLL with analog compensation of the fractional phase error. The VCO is running at double of the RF frequency. Two calibration loops ensure correct PLL functionality within the specified operating limits.

7.8.2 RF Channel Selection

The PLL is designed to support

- one channel in the European SRD band from 863 to 870 MHz at 868.3 MHz according to IEEE 802.15.4-2003/2006 (channel $k = 0$)
- 10 channels in the North American ISM band from 902 to 928 MHz with a channel spacing of 2 MHz according to IEEE 802.15.4-2003/2006. The center frequency of these channels is defined as

  $$F_c = 906 + 2\cdot(k\text{-}1) \quad [\text{MHz}]$$

  where k is the channel number ranging from 1 to 10.
- 4 channels in the Chinese WPAN band from 779 to 787 MHz with a channel spacing of 2 MHz according to IEEE 802.15.4c-2009. Center frequencies are 780, 782, 784, and 786 MHz.

Additionally, the PLL supports all frequencies from 769 to 935 MHz with 1 MHz frequency spacing and 3 bands with 100 kHz spacing from 769.0 to 794.5 MHz, 857.0 to 882.5 MHz, and 903.0 to 928.5 MHz.

The frequency is selected by register bits CC_BAND of register 0x14 (CC_CTRL_1) and register bits CC_NUMBER of register 0x13 (CC_CTRL_0). Table 7-35 shows the settings of CC_BAND and CC_NUMBER.

Table 7-35. Frequency Bands and Numbers

CC_BAND	CC_NUMBER	Description
0	Not used	European and North American channels according to IEEE 802.15.4-2003/2006; Frequency selected by register bits CHANNEL (register 0x08, PHY_CC_CCA), refer to section 7.8.6
1	0 – 255	769.0 – 794.5 MHz; F_c [MHz] = 769.0 + 0.1 · CC_NUMBER
2	0 – 255	857.0 – 882.5 MHz; F_c [MHz] = 857.0 + 0.1 · CC_NUMBER
3	0 – 255	903.0 – 928.5 MHz; F_c [MHz] = 903.0 + 0.1 · CC_NUMBER
4	0 – 94	769 – 863 MHz; F_c [MHz] = 769 + CC_NUMBER
5	0 – 102	833 – 935 MHz; F_c [MHz] = 833 + CC_NUMBER
6, 7	0 – 255	Reserved

7.8.3 PLL Settling Time and Frequency Agility

When the PLL is enabled during state transition from TRX_OFF to PLL_ON or RX_ON, the settling time is typically t_{TR4} = 200 µs (50 µs plus 150 µs settling time of the analog voltage regulator AVREG), including PLL self calibration. For more information, refer to Table 5-1 and section 7.8.4. The locking of the PLL is indicated with the interrupt IRQ_0 (PLL_LOCK).

Switching between channels within a frequency band in PLL_ON or RX_ON states is typically done within t_{TR20} = 11 µs. This makes the radio transceiver highly suitable for frequency hopping applications.

The PLL frequency in PLL_ON and receive states is 1 MHz below the PLL frequency in transmit states. When starting the transmit procedure, the PLL frequency is changed to the transmit frequency within a period of t_{TR23} = 16 µs before really starting the transmission. After the transmission, the PLL settles back to the receive frequency within a period of t_{TR24} = 32 µs. These frequency changes do not generate the interrupt IRQ_0 (PLL_LOCK) or IRQ_1 (PLL_UNLOCK).

7.8.4 Calibration Loops

Due to variation of temperature, supply voltage, and center frequency, the VCO characteristics may vary.

To ensure a stable operation, two automated control loops are implemented: center frequency and delay cell calibration. Both calibration loops are initiated automatically when the PLL is enabled during state transition from TRX_OFF to PLL_ON or RX_ON. Additionally, both calibration loops are initiated when the PLL changes to a different frequency setting.

If the PLL operates for a long time on the same channel or the operating temperature changes significantly, the calibration loops should be initiated manually. The recommended calibration interval is 5 minutes or less.

Both calibration loops can be initiated manually by SPI command. To start the calibration, the device should be in state PLL_ON.

The center frequency calibration can be initiated by setting PLL_CF_START = 1 (register 0x1A, PLL_CF). Center frequency calibration generates (if enabled) a PLL_UNLOCK interrupt. The calibration loop is completed when the PLL_LOCK interrupt (if enabled) occurs. The duration of the center frequency calibration loop depends on the difference between the current CF value and the final CF value. During the calibration, the CF value is incremented or decremented. Each step takes 8 µs. The minimum time is 8 µs; the maximum time is 270 µs. The recommended procedure to start the center frequency calibration is to read the register 0x1A (PLL_CF), to set the PLL_CF_START register bit to 1, and to write the value back to the register.

The delay cell calibration can be initiated by setting the bit PLL_DCU_START of register 0x1B (PLL_DCU) to 1. The delay time of the programmable delay unit is adjusted to the correct value. The calibration works as successive approximation and is independent of the values in the register 0x1B (PLL_DCU). The duration of the calibration is t_{TR22} = 10 µs.

During both calibration processes, no correct receive or transmit operation is possible. The recommended state for the calibration is therefore PLL_ON, but calibration is not blocked at receive or transmit states.

Both calibrations can be executed concurrently.

7.8.5 Interrupt Handling

Two different interrupts indicate the PLL status. IRQ_0 (PLL_LOCK) indicates that the PLL has locked. IRQ_1 (PLL_UNLOCK) indicates an unexpected unlock condition. A PLL_LOCK interrupt clears any preceding PLL_UNLOCK interrupt automatically and vice versa.

A PLL_LOCK interrupt occurs in the following situations:

- State change from TRX_OFF to PLL_ON / RX_ON
- Frequency setting change in states PLL_ON / RX_ON
- A manually started center frequency calibration has been completed

All other PLL_LOCK interrupt events indicate that the PLL locked again after a prior unlock happened.

A PLL_UNLOCK interrupt occurs in the following situations:

- A manually initiated center frequency calibration in states PLL_ON / (RX_ON)
- Frequency setting change in states PLL_ON / RX_ON

PLL_LOCK and PLL_UNLOCK affect the behavior of the transceiver:

In states BUSY_TX and BUSY_TX_ARET the transmission is stopped and the transceiver returns into state PLL_ON. During BUSY_RX and BUSY_RX_AACK, the transceiver returns to state RX_ON and RX_AACK_ON, respectively, once the PLL has locked.

7.8.6 Register Description

Register 0x08 (PHY_CC_CCA):

The register PHY_CC_CCA contains register bits to set the channel center frequency according to channel page 0 of IEEE 802.15.4-2003/2006 for the European and North American band. A write access to the register bits CHANNEL sets the channel number; a read access shows the current channel number. It is necessary to set register bits CC_BAND (register 0x14, CC_CTRL_1) to 0 in order to enable the above described channel selection, see Table 7-35.

Table 7-36. Register 0x08 (PHY_CC_CCA)

Bit	7	6	5	4
Name	CCA_REQUEST	CCA_MODE	CCA_MODE	CHANNEL[4]
Read/Write	W	R/W	R/W	R/W
Reset Value	0	0	1	0

Bit	3	2	1	0
Name	CHANNEL[3]	CHANNEL[2]	CHANNEL[1]	CHANNEL[0]
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	1	0	1

- **Bit 7:5**

Refer to section 6.6.6.

- **Bit 4:0 - CHANNEL**

Table 7-37. Channel Assignment according to IEEE 802.15.4-2003/2006, Channel Page 0

Register Bits	Value	Channel Number *k*	Frequency [MHz]
CHANNEL	0x00	0	868.3
	0x01	1	906
	0x02	2	908
	0x03	3	910
	0x04	4	912
	0x05	5	914
	0x06	6	916
	0x07	7	918
	0x08	8	920
	0x09	9	922
	0x0A	10	924
	0x0B … 0x1F	Reserved	

Register 0x13 (CC_CTRL_0):

This register controls the center frequency if the selection by channel number according to IEEE 802.15.4-2003/2006 is not used.

Table 7-38. Register 0x13 (CC_CTRL_0)

Bit	7	6	5	4	3	2	1	0
Name	CC_NUMBER[7:0]							
Read/Write	R/W							
Reset Value	0	0	0	0	0	0	0	0

Register 0x14 (CC_CTRL_1):

This register selects the frequency band if the selection by channel number according to IEEE 802.15.4-2003/2006 is not used.

Table 7-39. Register 0x14 (CC_CTRL_1)

Bit	7	6	5	4
Name	Reserved	Reserved	Reserved	Reserved
Read/Write	R	R	R	R
Reset Value	0	0	0	0

Bit	3	2	1	0
Name	Reserved	CC_BAND[2]	CC_BAND[1]	CC_BAND[0]
Read/Write	R	R/W	R/W	R/W
Reset Value	0	0	0	0

The functionality of CC_BAND and CC_NUMBER is documented in Table 7-35.

Register 0x1A (PLL_CF):

This register controls the operation of the center frequency calibration loop.

Table 7-40. Register 0x1A (PLL_CF)

Bit	7	6	5	4
Name	PLL_CF_START	Reserved	Reserved	PLL_CF[4]
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	1	0	0
Bit	3	2	1	0
Name	PLL_CF[3]	PLL_CF[2]	PLL_CF[1]	PLL_CF[0]
Read/Write	R/W	R/W	R/W	R/W
Reset Value	1	0	0	0

- **Bit 7 – PLL_CF_START**

PLL_CF_START = 1 initiates the center frequency calibration. When the calibration cycle has finished after at most 25 µs, the register bit PLL_CF_START is reset to 0.

- **Bit 6:5**

These bits are reserved and must always be written back using the reset values.

- **Bit 4:0 – PLL_CF**

Bits 4:0 represent the current CF state of the PLL. In order to assure the shortest possible calibration time, they should not be changed when starting center frequency tuning.

Register 0x1B (PLL_DCU):

This register controls the operation of the delay cell calibration loop.

Table 7-41. Register 0x1B (PLL_DCU)

Bit	7	6	5	4
Name	PLL_DCU_START	Reserved	Reserved	Reserved
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	1	0	0
Bit	3	2	1	0
Name	Reserved	Reserved	Reserved	Reserved
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0

- **Bit 7 – PLL_DCU_START**

PLL_DCU_START = 1 initiates the delay cell calibration. The calibration cycle is completed after 10 µs and the register bit PLL_DCU_START is set to 0. The register bit is cleared immediately after finishing the calibration.

- **Bit 6:0 – Reserved**

Register 0x11 (BATMON):

The MSB of this register indicates the lock status of the PLL.

Table 7-42. Register 0x11 (BATMON)

Bit	7	6	5	4
Name	PLL_LOCK_CP	Reserved	BATMON_OK	BATMON_HR
Read/Write	R	R/W	R	R/W
Reset Value	0	0	0	0

Bit	3	2	1	0
Name	BATMON_VTH[3]	BATMON_VTH[2]	BATMON_VTH[1]	BATMON_VTH[0]
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	1	0

- **Bit 7 – PLL_LOCK_CP**

This register bit can be used to read out the lock status of the PLL.

Table 7-43. PLL Lock Status

Register Bit	Value	Description
PLL_LOCK_CP	0	PLL is unlocked
	1	PLL is locked

- **Bit 6 – Reserved**
- **Bit 5:0**

Refer to section 7.6.5.

7.9 Automatic Filter Tuning (FTN)

7.9.1 Overview

The FTN is incorporated to compensate for temperature, supply voltage variations, and part-to-part variations of the radio transceiver. A calibration cycle is initiated automatically when entering the TRX_OFF state from the SLEEP, RESET, or P_ON states.

Although receiver and transmitter are very robust against these variations, it is recommended to initiate the FTN manually if the radio transceiver does not regularly use the SLEEP state. This applies in particular for the High Data Rate Modes with higher sensitivity against variations. The recommended calibration interval is about 5 minutes.

7.9.2 Register Description

Register 0x18 (FTN_CTRL):

This register controls the operation of the filter tuning calibration loop.

Table 7-44. Register 0x18 (FTN_CTRL)

Bit	7	6	5	4
Name	FTN_START	Reserved	Reserved	Reserved
Read/Write	S	R/W	R/W	R/W
Reset Value	0	1	0	1

Bit	3	2	1	0
Name	Reserved	Reserved	Reserved	Reserved
Read/Write	R/W	R/W	R/W	R/W
Reset Value	1	0	0	0

- **Bit 7 – FTN_START**

FTN_START = 1 initiates the filter tuning calibration loop. Ones the calibration cycle has finished within a maximum time period of 25 µs, the register bit is automatically reset to 0.

- **Bit 6:0 – Reserved**

8 Radio Transceiver Usage

This section describes basic procedures to receive and transmit frames using the AT86RF212.

8.1 Frame Receive Procedure

A frame reception comprises of two actions: The transceiver listens for, receives, and demodulates the frame to the Frame Buffer and signals the reception to the microcontroller. After or during that process, the microcontroller can read the available frame data from the Frame Buffer via the SPI interface.

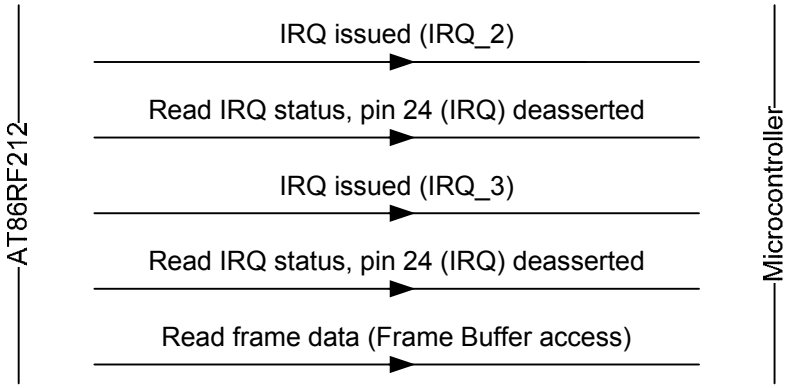
While being in state RX_ON or RX_AACK_ON, the radio transceiver searches for incoming frames on the selected channel. Assuming the appropriate interrupts are enabled, a detection of an IEEE 802.15.4-2006 compliant frame is indicated by interrupt IRQ_2 (RX_START). When the frame reception is completed, interrupt IRQ_3 (TRX_END) is issued.

Different Frame Buffer read access scenarios are recommended for

- non-time-critical applications: read access starts after IRQ_3 (TRX_END)
- time-critical applications: read access starts after IRQ_2 (RX_START)

For non-time-critical operations, it is recommended to wait for interrupt IRQ_3 (TRX_END) before starting a Frame Buffer read access. Figure 8-1 illustrates the frame receive procedure using IRQ_3 (TRX_END).

Figure 8-1. Transactions between AT86RF212 and Microcontroller during Receive



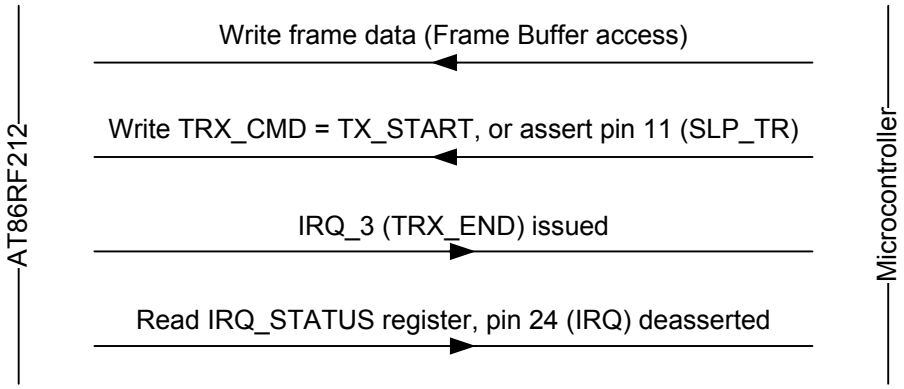
Critical protocol timing could require starting the Frame Buffer read access after interrupt IRQ_2 (RX_START). The first byte of the frame data can be read one octet time period after the IRQ_2 (RX_START) interrupt. The microcontroller must ensure to read slower than the frame is received. Otherwise, a Frame Buffer underrun occurs, IRQ_6 (TRX_UR) is issued, and the frame data may be not valid. To avoid this, the Frame Buffer read access can be controlled by using a Frame Buffer Empty Indicator, refer to section 9.6.

8.2 Frame Transmit Procedure

A frame transmission comprises of two actions, a Frame Buffer write access and the transmission of the Frame Buffer content. Both actions can be run in parallel if required by critical protocol timing.

Figure 8-2 illustrates the frame transmit procedure when writing and transmitting the frame consecutively. After a Frame Buffer write access, the frame transmission is initiated by asserting pin 11 (SLP_TR) or writing command TX_START to register 0x02 (TRX_STATE) while the radio transceiver is in state PLL_ON or TX_ARET_ON. The completion of the transaction is indicated by interrupt IRQ_3 (TRX_END).

Figure 8-2. Transaction between AT86RF212 and Microcontroller during Transmit

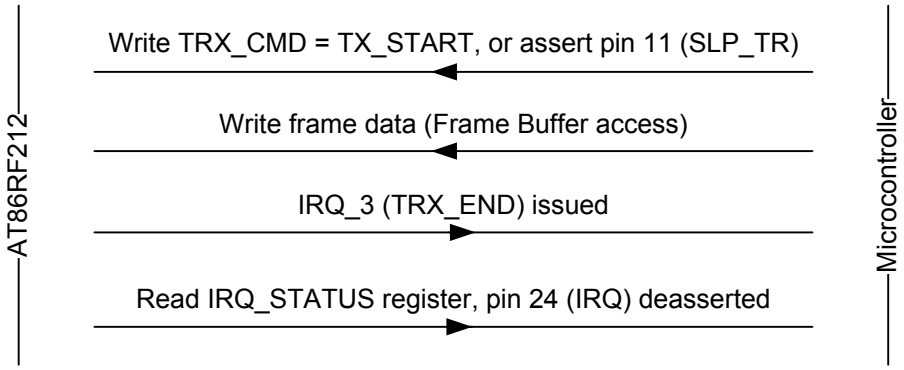


Alternatively, a frame transmission can be started first, followed by the Frame Buffer write access (PSDU data); refer to Figure 8-3. This is applicable for time critical applications.

Initiating a transmission, either by asserting pin 11 (SLP_TR) or command TX_START to register bits TRX_CMD (register 0x02, TRX_STATE), the radio transceiver starts transmitting the SHR which is internally generated.

Front end initialization takes one symbol period for PLL settling and PA ramp up. SHR transmission takes another 40 symbol periods for BPSK or 10 symbol periods for O-QPSK. The PHR must be available in the Frame Buffer before this time elapses. Furthermore, the SPI data rate must be higher than the PHY data rate to avoid a Frame Buffer underrun, which is indicated by IRQ_6 (TRX_UR).

Figure 8-3. Time Optimized Frame Transmit Procedure



9 Extended Feature Set

9.1 Security Module (AES)

The security module (AES) is characterized by:

- Hardware accelerated encryption and decryption
- Compatible with AES-128 standard (128 bit key and data block size)
- Support of ECB (encryption/decryption) mode and CBC (encryption) mode
- Stand-alone operation, independent of other blocks

9.1.1 Overview

The security module is based on an AES-128 core according to FIPS197 standard, refer to [9]. The security module is independent from other building blocks of the AT86RF212. Encryption and decryption can be performed in parallel to a frame transmission or reception.

Controlling of the security block is implemented as an SRAM access to address space 0x82 to 0x94. A Fast SRAM access mode allows simultaneously writing new data and reading data from previously processed data within the same SPI transfer. This access procedure is used to reduce the turnaround time for ECB mode, see section 9.1.5.

In addition, the security module contains another 128-bit register to store the initial key used for security operations. This initial key is not modified by the security module.

9.1.2 Security Module Preparation

The use of the security module requires a configuration of the security engine before starting a security operation. The required steps are listed in Table 9-1.

Table 9-1. AES Engine Configuration Steps

Step	Action	Description	Section
1	Key Setup	Write encryption or decryption key to SRAM	9.1.3
2	AES mode	Select AES mode: ECB or CBC Select encryption or decryption	9.1.4
3	Write Data	Write plaintext or cipher text to SRAM	9.1.5
4	Start operation	Start AES operation	
5	Read Data	Read cipher text or plaintext from SRAM	9.1.5

Before starting any security operation, a key must be written to the security engine. The key set up requires the configuration of the AES engine KEY mode using register bits AES_MODE (SRAM address 0x83, AES_CTRL). The following step selects the AES mode, either electronic code book (ECB) or cipher block chaining (CBC). These modes are explained in more detail in section 9.1.4. Further, encryption or decryption must be selected with register bit AES_DIR (SRAM address 0x83, AES_CTRL).

After this, the 128-bit plain text or cipher text data has to be provided to the AES hardware engine. The data uses the SRAM address range 0x84 – 0x93.

An encryption or decryption is initiated with register bit AES_REQUEST = 1 (SRAM address 0x83, i.e. AES_CTRL, or the mirrored version SRAM address 0x94, i.e. AES_CTRL_MIRROR).

The AES module control registers are only accessible using SRAM read and write accesses on address space 0x82 to 0x94. Configuring the AES mode, providing the data, and starting a decryption or encryption operation can be combined in a single SRAM access.

Notes

- No additional register access is required to operate the security block.
- Using AES in TRX_OFF state requires an activated clock at pin 17 (CLKM), i.e. register bits CLKM_CTRL ≠ 0. For further details, refer to section 7.7.4.
- Access to the security block is not possible while the radio transceiver is in state SLEEP.
- All configurations of the security module, the SRAM content, and keys are reset during SLEEP or RESET states.
- A read or write access to register 0x83 (AES_CTRL) during AES operation terminates the current processing.

9.1.3 Security Key Setup

The setup of the key is prepared by setting register bits AES_MODE = 0x1 (SRAM address 0x83, AES_CTRL). Afterwards, the 128 bit key must be written to SRAM addresses 0x84 through 0x93 (registers AES_KEY). It is recommended to combine the setting of control register 0x83 (AES_CTRL) and the 128 bit key transfer using only one SRAM access starting from address 0x83.

The address space of the 128-bit key and 128-bit data is identical from a programming point of view. However, both use different pages which are selected by register bit AES_MODE before storing the data.

A read access to registers AES_KEY (0x84 – 0x93) returns the last round key of the preceding security operation. After an ECB encryption operation, this is the key that is required for the corresponding ECB decryption operation. However, the initial AES key, written to the security module in advance of an AES run (see step 1 in Table 9-1), is not modified during an AES operation. This initial key is used for the next AES run, even it cannot be read from AES_KEY.

Note

- ECB decryption is not required for IEEE 802.15.4 or ZigBee security processing. The AT86RF212 provides this functionality as an additional feature.

9.1.4 Security Operation Modes

9.1.4.1 Electronic Code Book (ECB)

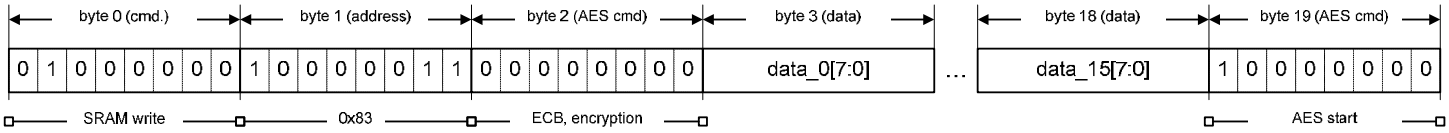
ECB is the basic operating mode of the security module. After setting up the initial AES key, register bits AES_MODE = 0 (SRAM address 0x83, AES_CTRL) set up the ECB mode. Register bit AES_DIR (SRAM address 0x83, AES_CTRL) selects the direction, either encryption or decryption. The data to be processed has to be written to SRAM addresses 0x84 through 0x93 (registers AES_STATE).

An example for a programming sequence is shown in Figure 9-1. This example assumes that a suitable key has been loaded before.

A security operation can be started within one SRAM access by appending the start command AES_REQUEST = 1 (register 0x94, AES_CTRL_MIRROR) to the SPI

sequence. Register AES_CTRL_MIRROR is a mirrored version of register 0x83 (AES_CTRL).

Figure 9-1. ECB Programming SPI Sequence – Encryption



In summary, the following steps are required to perform a security operation using only one SPI access:

1. Configure SPI access	a) SRAM write, refer to section 4.3 b) Start address 0x83
2. Configure AES operation	Address 0x83: select ECB mode and direction
3. Write 128-bit data block	Addresses 0x84 – 0x93: either plain or cipher text
4. Start AES operation	Address 0x94: start AES operation, ECB mode

This sequence is recommended because the security operation is configured and started within one SPI transaction.

The ECB encryption operation is illustrated in Figure 9-2. Figure 9-3 shows the ECB decryption mode, which is supported in a similar way.

Figure 9-2. ECB Mode - Encryption

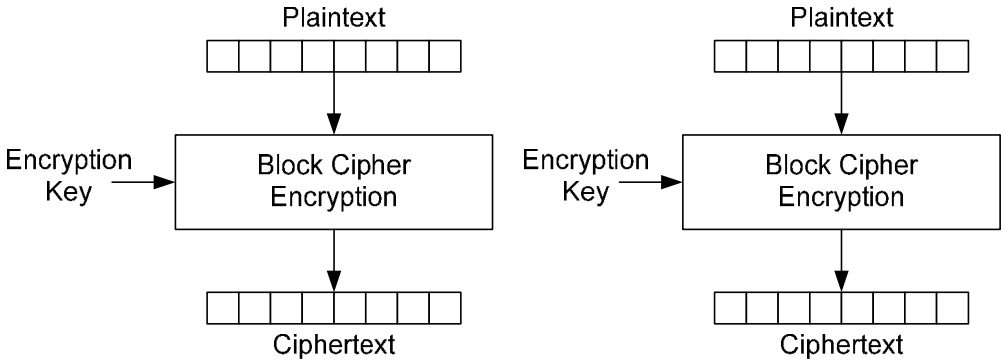
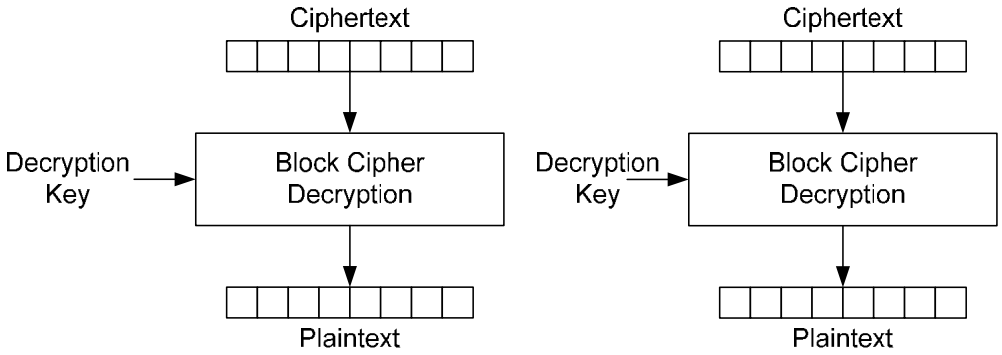


Figure 9-3. ECB Mode - Decryption



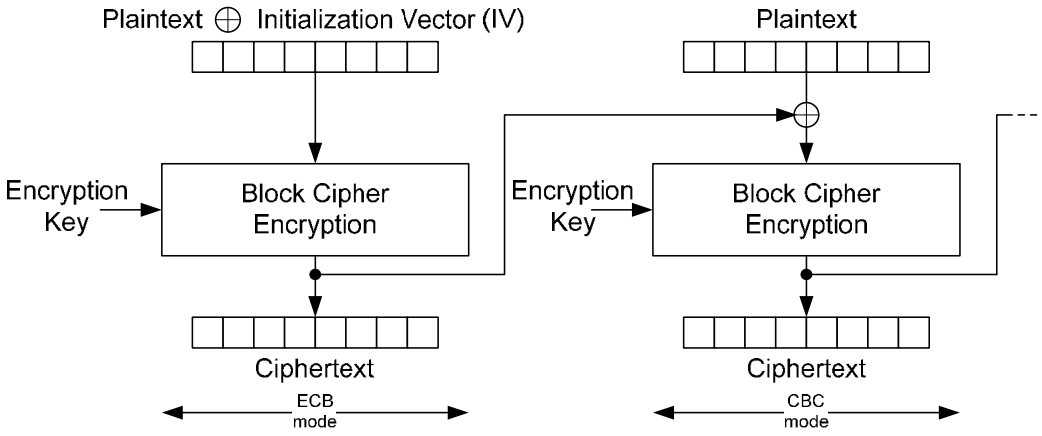
When decrypting, due to the nature of AES algorithm, the initial key to be used is not the same as the one used for encryption, but rather the last round key instead. This last round key is the content of the key address space stored after running one full encryption cycle and must be saved for decryption. If the decryption key has not been saved, it has to be recomputed by first running a dummy encryption (of an arbitrary plaintext) using the original encryption key, then fetching the resulting round key from the key memory, and writing it back into the key memory as the decryption key.

ECB decryption is not used by either IEEE 802.15.4 or ZigBee frame security. Both of these standards do not directly encrypt the payload, but rather a nonce instead, and protect the payload by applying an XOR operation between the resulting (AES-) cipher text and the original payload. As the nonce is the same for encryption and decryption, only ECB encryption is required. Decryption is performed by XORing the received cipher text with its own encryption result, which results in the original plaintext payload upon success.

9.1.4.2 Cipher Block Chaining (CBC)

In CBC mode, the result of a previous AES operation is XORed with the new incoming vector forming the new plaintext to encrypt, see Figure 9-4. This mode is used for the computation of a cryptographic checksum (message integrity code, MIC).

Figure 9-4. CBC Mode - Encryption



After preparing the AES key and defining the AES operation direction using SRAM register bit AES_DIR, the data has to be provided to the AES engine and the CBC operation can be started.

The first CBC run has to be configured as ECB to process the initial data (plaintext XORed with an initialization vector provided by the microcontroller). All succeeding AES runs are to be configured as CBC by setting register bits AES_MODE = 0x2 (register 0x83, AES_CTRL). Register bit AES_DIR (register 0x83, AES_CTRL) must be set to AES_DIR = 0 to enable AES encryption. The data to be processed has to be transferred to the SRAM starting with address 0x84 to 0x93 (register AES_STATE). Setting register bit AES_REQUEST = 1 (register 0x94, AES_CTRL_MIRROR), as described in section 9.1.4, starts the first encryption within one SRAM access. This causes the next 128 bits of plaintext data to be XORed with the previous cipher text data, see Figure 9-4.

According to IEEE 802.15.4, the input for the very first CBC operation has to be prepared by XORing a plaintext with an initialization vector (IV). The value of the

initialization vector is 0. However, for non-compliant usage any other initialization vector can be used. This operation has to be prepared by the microcontroller.

Note that IEEE 802.15.4-2006 standard MIC algorithm requires CBC mode encryption only, as it implements a one-way hash function.

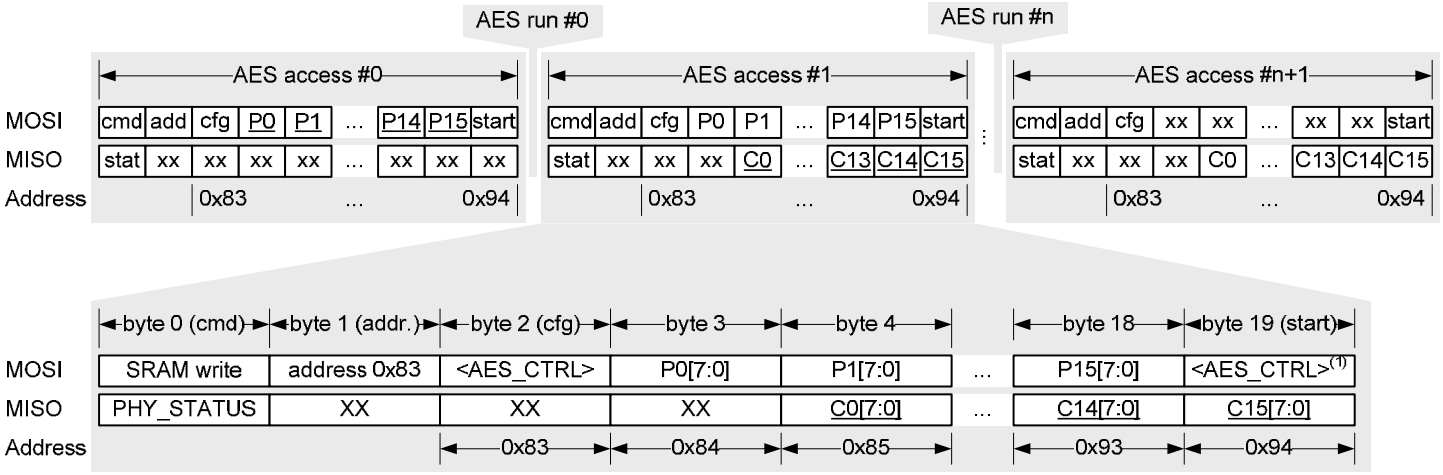
9.1.5 Data Transfer – Fast SRAM Access

The ECB and CBC modules, including the AES core, are clocked with 16 MHz. One AES operation takes 24 µs to execute, refer to parameter 10.4.14 in section 10.4. This means that the processing of the data is usually faster than the transfer of the data via the SPI interface.

To reduce the overall processing time, the AT86RF212 provides a Fast SRAM access for the address space 0x83 to 0x94. The Fast SRAM access allows writing and reading of data simultaneously during one SPI access for consecutive AES operations (*AES run*).

For each byte P0 transferred to pin 22 (MOSI), the previous content of the respective AES register C0 is clocked out at pin 20 (MISO) with an offset of one byte. See Figure 9-5 as an example for "*AES access #1*".

Figure 9-5. Packet Structure – Fast SRAM Access Mode



Note: 1. Byte 19 is the mirrored version of register AES_CTRL on SRAM address 0x94; see register description AES_CTRL_MIRROR for details.

In the example shown in Figure 9-5 the initial plaintext P0 – P15 is written to the SRAM within "*AES access #0*". The last command on address 0x94 (AES_CTRL_MIRROR) starts the AES operation ("*AES run #0*"). In the next "*AES access #1*" new plaintext data P0 – P15 is written to the SRAM for the second AES run, in parallel the cipher text C0 – C15 from the first AES run is clocked out at pin MISO. To read the cipher text from the last "*AES run #(n)*", one dummy "*AES access #(n+1)*" is needed.

Note that the SRAM write access always overwrites the previous processing result.

The Fast SRAM access automatically applies to all write operations to SRAM addresses 0x83 to 0x94.

9.1.6 Security Operation Status

The status of the security processing is indicated by register 0x82 (AES_STATUS). After 24 µs AES processing time register bit AES_DONE changes to 1 (register 0x82, AES_STATUS) indicating that the security operation has finished, see parameter 10.4.14 in section 10.4.

9.1.7 SRAM Register Summary

The following registers are required to control the security module:

Table 9-2. SRAM Security Module Address Space Overview

SRAM-Addr.	Register Name	Description
0x80 – 0x81		Reserved
0x82	AES_STATUS	AES status
0x83	AES_CTRL	Security module control, AES mode
0x84 – 0x93	AES_KEY AES_STATE	Depends on AES_MODE setting: AES_MODE = 1: - Contains AES_KEY (key) AES_MODE = 0 | 2: - Contains AES_STATE (128 bit data block)
0x94	AES_CTRL_MIRROR	Mirror of register 0x83 (AES_CTRL)
0x95 – 0xFF		Reserved

These registers are only accessible using SRAM write and read; for details, refer to section 4.3.3. Note that the SRAM registers are reset when entering the SLEEP state.

9.1.8 Register Description

Register 0x82 (AES_STATUS):

This read-only register signals the status of the security module and operation.

Table 9-3. Register 0x82 (AES_STATUS)

Bit	7	6	5	4
Name	AES_ER	Reserved	Reserved	Reserved
Read/Write	R	R	R	R
Reset Value	0	0	0	0

Bit	3	2	1	0
Name	Reserved	Reserved	Reserved	AES_DONE
Read/Write	R	R	R	R
Reset Value	0	0	0	0

- **Bit 7 – AES_ER**

This SRAM register bit indicates an error of the AES module. An error may occur for instance after an access to SRAM register 0x83 (AES_CTRL) while an AES operation is running or after reading less than 128 bits from SRAM register space 0x84 – 0x93 (AES_STATE).

Table 9-4. AES Core Operation Status

Register Bit	Value	Description
AES_ER	0	No error of the AES module
	1	AES module error

- **Bit 6:1 – Reserved**
- **Bit 0 – AES_DONE**

Table 9-5. AES Core Operation Status

Register Bit	Value	Description
AES_DONE	0	AES operation has not been completed
	1	AES operation has been completed

Register 0x83 (AES_CTRL):

This register controls the operation of the security module. A read or write access during AES operation terminates the current processing.

Table 9-6. Register 0x83 (AES_CTRL)

Bit	7	6	5	4
Name	AES_REQUEST	AES_MODE[2]	AES_MODE[1]	AES_MODE[0]
Read/Write	W	R/W	R/W	R/W
Reset Value	0	0	0	0

Bit	3	2	1	0
Name	AES_DIR	Reserved	Reserved	Reserved
Read/Write	R/W	R	R	R
Reset Value	0	0	0	0

- **Bit 7 – AES_REQUEST**

A write access with AES_REQUEST = 1 initiates the AES operation.

- **Bit 6:4 – AES_MODE**

This register bit sets the AES operation mode.

Table 9-7. AES Mode

Register Bits	Value	Description
AES_MODE	0	ECB mode, refer to section 9.1.4.1
	1	KEY mode, refer to section 9.1.3
	2	CBC mode, refer to section 9.1.4.2
	3 – 7	Reserved

- **Bits 3 – AES_DIR**

This register bit sets the AES operation direction, either encryption or decryption.

Table 9-8. AES Direction

Register Bit	Value	Description
AES_DIR	0	AES encryption (ECB, CBC)
	1	AES decryption (ECB)

- **Bit 2:0 – Reserved**

Register 0x94 (AES_CTRL_MIRROR):

Register 0x94 is a mirrored version of register 0x83 (AES_CTRL); for details, refer to register 0x83 (AES_CTRL).

Table 9-9. Register 0x94 (AES_CTRL_MIRROR)

Bit	7	6	5	4
Name	AES_REQUEST	AES_MODE[2]	AES_MODE[1]	AES_MODE[0]
Read/Write	W	R/W	R/W	R/W
Reset Value	0	0	0	0
Bit	3	2	1	0
Name	AES_DIR	Reserved	Reserved	Reserved
Read/Write	R/W	R	R	R
Reset Value	0	0	0	0

This register could be used to start a security operation within a single SRAM access by appending it to the data stream and setting register bit AES_REQUEST = 1.

9.2 Random Number Generator

9.2.1 Overview

The AT86RF212 provides a 2-bit random number generator. This random number can be used to

- generate random seeds for CSMA-CA algorithm, see section 5.2
- generate random values for AES key generation, see section 9.1

Random numbers are stored in register bits RND_VALUE (register 0x06, PHY_RSSI). The random number is updated at every read access in Basic Operating Mode receive states (RX_ON, BUSY_RX). The Random Number Generator does not work if the preamble detector is disabled (RX_PDT_DIS = 1, refer to section 7.2.3).

9.2.2 Register Description

Register 0x06 (PHY_RSSI):

Register 0x06 (PHY_RSSI) is a multi purpose register to indicate FCS validity, to provide random numbers, and an RSSI value.

Table 9-10. Register 0x06 (PHY_RSSI)

Bit	7	6	5	4
Name	RX_CRC_VALID	RND_VALUE[1]	RND_VALUE[0]	RSSI[4]
Read/Write	R	R	R	R
Reset Value	0	0	0	0

Bit	3	2	1	0
Name	RSSI[3]	RSSI[2]	RSSI[1]	RSSI[0]
Read/Write	R	R	R	R
Reset Value	0	0	0	0

- **Bit 7 – RX_CRC_VALID**

Refer to section 6.3.5.

- **Bit 6:5 – RND_VALUE**

The 2-bit random value can be retrieved by reading register bits RND_VALUE. Note that the radio transceiver shall be in one of the Basic Operating Mode receive states.

- **Bit 4:0 – RSSI**

Refer to section 6.4.4.

9.3 Differential Output supporting Software controlled Antenna Diversity

Digital output pins DIG1 and DIG2 can be used to drive a general purpose differential signal. The following sections describe software controlled antenna diversity as one possible application.

9.3.1 Overview

Due to multipath propagation effects between network nodes, the receive signal strength may vary and affects the link quality, even for small changes of the antenna location. These fading effects can result in an increased error floor or loss of the connection between devices.

To improve the reliability of a RF connection between network nodes, antenna diversity can be applied to reduce effects of multipath propagation and fading. Antenna diversity uses two antennas to select the most reliable RF signal path. To ensure highly independent receive signals on both antennas, the antennas should be carefully separated from each other.

The AT86RF212 supports software controlled antenna diversity, i.e. the microcontroller controls which antenna is used for transmission and reception. This is done by register settings.

Antenna Diversity can be used in Basic and Extended Operating Modes and can also be combined with other features and operating modes like High Data Rate Modes and RX/TX Indication.

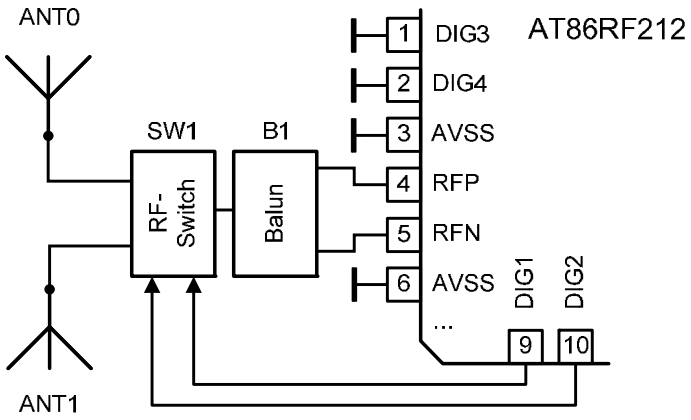
9.3.2 Application Example

A block diagram for a typical application is shown in Figure 9-6.

The use of pins 9 and 10 (DIG 1 and DIG2) for Antenna Diversity is enabled by ANT_EXT_SW_EN = 1 (register 0x0D, ANT_DIV). In this case, the internal connection of the control pins 9 and 10 to digital ground is disabled (refer to section 2.2.2), and they provide a differential control signal to the antenna switch (SW1).

For transmission and reception, the antenna defined by register bits ANT_CTRL (register 0x0D, ANT_DIV) is selected.

Figure 9-6. Antenna Diversity – Block Diagram



9.3.3 Register Description

Register 0x0D (ANT_DIV):

The ANT_DIV register controls Antenna Diversity.

Table 9-11. Register 0x0D (ANT_DIV)

Bit	7	6	5	4
Name	Reserved	Reserved	Reserved	Reserved
Read/Write	R	R	R	R
Reset Value	0	0	0	0

Bit	3	2	1	0
Name	Reserved	ANT_EXT_SW_EN	ANT_CTRL[1]	ANT_CTRL[0]
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	0	1

- **Bit 7:3 – Reserved**
- **Bit 2 – ANT_EXT_SW_EN**

If enabled, pin 9 (DIG1) and pin 10 (DIG2) become output pins and provide a differential control signal for an antenna diversity switch. The selection of a specific antenna is done according to register bits ANT_CTRL.

If RX Frame Time Stamping (refer to section 9.5) is used in combination with Antenna Diversity, DIG1 is used for Antenna Diversity and DIG2 is used for RX Frame Time Stamping. AT86RF212 does not provide a differential control signal in this case, see Figure 3-2.

If the register bit is set, the control pins DIG1/DIG2 are activated in all radio transceiver states as long as register bit ANT_EXT_SW_EN is set. If the AT86RF212 is not in a receive or transmit state, it is recommended to disable register bit ANT_EXT_SW_EN to reduce the power consumption or avoid leakage current of an external RF switch, especially during SLEEP state. If register bit ANT_EXT_SW_EN = 0, output pins DIG1 and DIG2 are internally connected to digital ground.

Table 9-12. Antenna Diversity RF Switch Enable

Register Bit	Value	Description
ANT_EXT_SW_EN	0	Antenna Diversity RF switch control disabled
	1	Antenna Diversity RF switch control enabled

- **Bit 1:0 – ANT_CTRL**

These register bits provide a static control of an Antenna Diversity switch. Although it is possible to change register bits ANT_CTRL in state TRX_OFF, this change will be effective at pins DIG1 and DIG2 in states PLL_ON and RX_ON.

Table 9-13. Antenna Diversity Switch Control

Register Bit	Value	Description
ANT_CTRL	0	Reserved
	1	Antenna 0 DIG1 = L DIG2 = H
	2	Antenna 1 DIG1 = H DIG2 = L
	3	Reserved

9.4 RX/TX Indicator

The main features are:

- RX/TX Indicator to control an external RF front-end
- Microcontroller independent RF front-end control
- Providing TX timing information

9.4.1 Overview

While IEEE 802.15.4 is targeting low cost and low power applications, solutions supporting higher transmit output power are occasionally desirable. To simplify the control of an optional external RF front-end, a differential control pin pair can indicate that the AT86RF212 is currently in transmit mode.

The control of an external RF front-end is done via digital control pins DIG3/DIG4. The function of this pin pair is enabled with register bit PA_EXT_EN (register 0x04, TRX_CTRL_1). While the transmitter is turned off, pin 1 (DIG3) is set to low level and pin 2 (DIG4) to high level. If the radio transceiver starts to transmit, the two pins change the polarity. This differential pin pair can be used to control PA, LNA, and RF switches.

If the AT86RF212 is not in a receive or transmit state, it is recommended to disable register bit PA_EXT_EN (register 0x04, TRX_CTRL_1) to reduce the power consumption or avoid leakage current of external RF switches and other building blocks, especially during SLEEP state. If register bits PA_EXT_EN = 0, output pins DIG3/DIG4 are internally connected to analog ground.

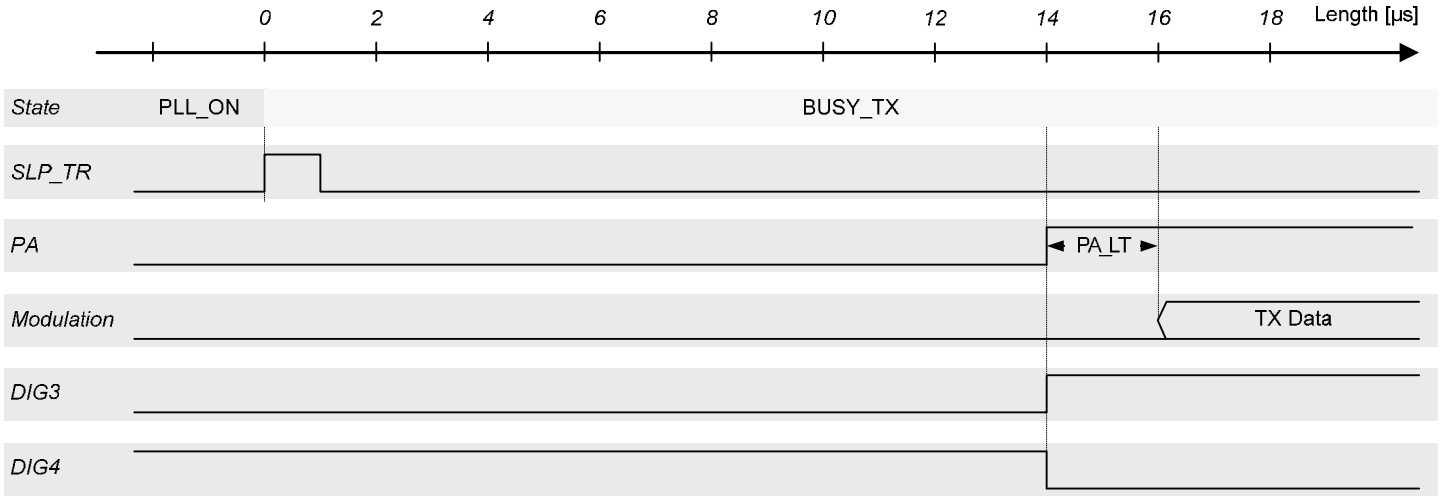
9.4.2 External RF-Front End Control

When using an external RF front-end including a power amplifier (PA), it may be required to adjust the setup time of the external PA relative to the internal building blocks to optimize the overall power spectral density (PSD) mask.

The start-up sequence of the individual building blocks of the internal transmitter is shown in Figure 9-7 where transmission is actually initiated by the rising edge of pin 11 (SLP_TR). The radio transceiver state changes from PLL_ON to BUSY_TX and the PLL settles to the transmit frequency within 1 symbol period. The modulation starts 1 symbol period after the rising edge of SLP_TR. During this time, the internal PA is initialized.

The control of the external PA is done via the differential pin pair DIG3/DIG4. DIG3 = H / DIG4 = L indicates that the transmission starts and can be used to enable the external PA. The timing of pins DIG3/DIG4 can be adjusted relative to the start of the frame using register bits PA_LT (register 0x16, RF_CTRL_0). For details, refer to section 7.3.5.

Figure 9-7. TX Power Ramping Control of RF Front-End for 250 kbit/s O-QPSK mode



9.4.3 Register Description

Register 0x04 (TRX_CTRL_1):

The TRX_CTRL_1 register is a multi purpose register to control various operating modes and settings of the radio transceiver.

Table 9-14. Register 0x04 (TRX_CTRL_1)

Bit	7	6	5	4
Name	PA_EXT_EN	IRQ_2_EXT_EN	TX_AUTO_CRC_ON	RX_BL_CTRL
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	1	0

Bit	3	2	1	0
Name	SPI_CMD_MODE	SPI_CMD_MODE	IRQ_MASK_MODE	IRQ_POLARITY
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0

- **Bit 7 – PA_EXT_EN**

This register bit enables pin 1 (DIG3) and pin 2 (DIG4) to indicate the transmit state of the radio transceiver.

Table 9-15. RF Front-End Control Pins

PA_EXT_EN	State	Pin	Value	Description
0	n/a	DIG3	L	External RF front-end control disabled
		DIG4	L	
1 (1)	BUSY_TX	DIG3	H	External RF front-end control enabled
		DIG4	L	
	Other	DIG3	L	
		DIG4	H	

Note: 1. It is recommended to set PA_EXT_EN = 1 only in receive or transmit states to reduce the power consumption or avoid leakage current of external RF switches or other building blocks, especially during SLEEP state.

- **Bit 6 – IRQ_2_EXT_EN**

Refer to section 9.5.2.

- **Bit 5 – TX_AUTO_CRC_ON**

Refer to section 6.3.5.

- **Bit 4 – RX_BL_CTRL**

Refer to section 9.6.2.

- **Bit 3:2 – SPI_CMD_MODE**

Refer to section 4.4.1.

- **Bit 1:0 – IRQ_MASK_MODE, IRQ_POLARITY**

Refer to section 4.7.2.

9.5 RX Frame Time Stamping

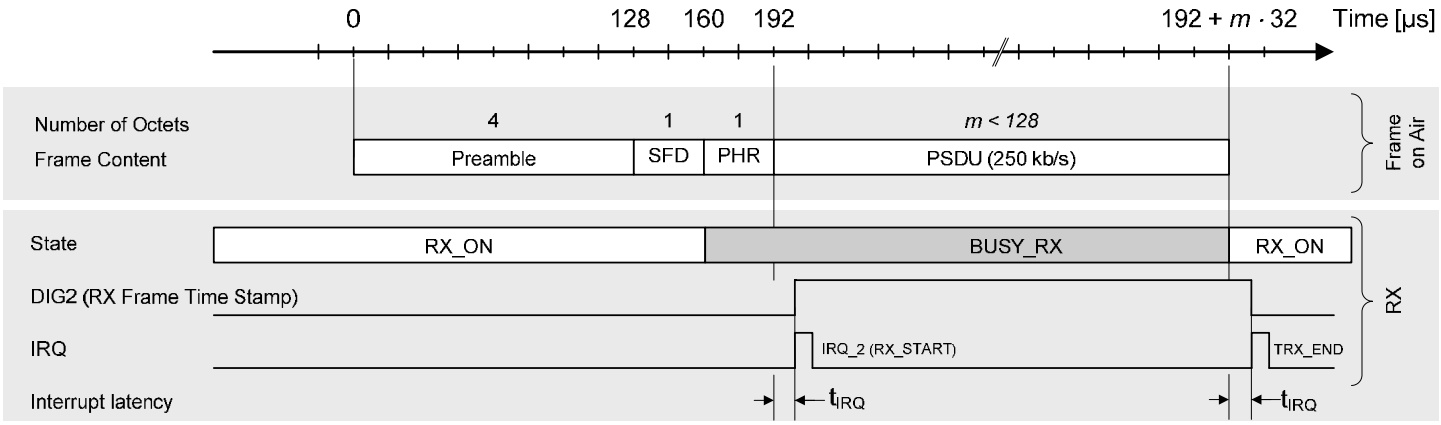
9.5.1 Overview

To determine the exact timing of an incoming frame, e.g. for beaconing networks, the reception of this frame can be signaled to the microcontroller via pin 10 (DIG2). The pin turns from L to H after detection of a valid PHR. When enabled, DIG2 is set to DIG2 = H at the same time as IRQ_2 (RX_START) occurs, even if IRQ_2 is disabled. The pin remains high for the length of the frame receive procedure, see Figure 9-8.

This function is enabled with register bit IRQ_2_EXT_EN (register 0x04, TRX_CTRL_1). Pin 10 (DIG2) can be connected to a timer capture unit of the microcontroller.

If this pin is not used for RX Frame Time Stamping, it can be configured for Antenna Diversity, refer to section 9.3. Otherwise, this pin is internally connected to ground.

Figure 9-8. Timing of RX_START and DIG2 for RX Frame Time Stamping within 250 kbit/s O-QPSK mode



Note: For timing figures, refer to section 10.4.

9.5.2 Register Description

Register 0x04 (TRX_CTRL_1):

Register 0x04 (TRX_CTRL_1) is a multi purpose register to control various operating modes and settings of the radio transceiver.

Table 9-16. Register 0x04 (TRX_CTRL_1)

Bit	7	6	5	4
Name	PA_EXT_EN	IRQ_2_EXT_EN	TX_AUTO_CRC_ON	RX_BL_CTRL
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	1	0

Bit	3	2	1	0
Name	SPI_CMD_MODE	SPI_CMD_MODE	IRQ_MASK_MODE	IRQ_POLARITY
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0

- **Bit 7 – PA_EXT_EN**

Refer to section 9.4.3.

- **Bit 6 – IRQ_2_EXT_EN**

If this register bit is set, the RX Frame Time Stamping Mode is enabled. An incoming frame with a valid PHR is signaled via pin 10 (DIG2). The pin remains at high level until the end of the frame receive procedure, see Figure 9-8.

- **Bit 5 – TX_AUTO_CRC_ON**

Refer to section 6.3.5.

- **Bit 4 – RX_BL_CTRL**

Refer to section 9.6.2.

- **Bit 3:2 – SPI_CMD_MODE**

Refer to section 4.4.1.

- **Bit 1:0 – IRQ_MASK_MODE, IRQ_POLARITY**

Refer to section 4.7.2.

9.6 Frame Buffer Empty Indicator

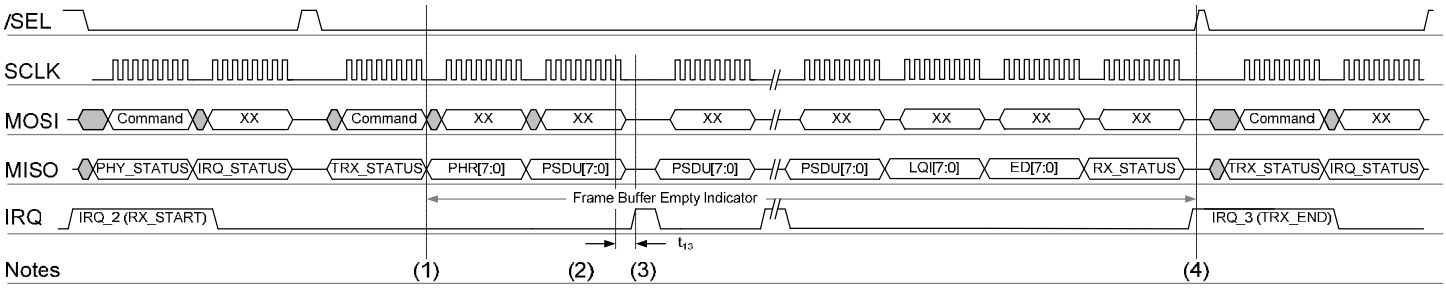
9.6.1 Overview

For time critical applications, it may be desirable to read the frame data as early as possible. To accomplish this, the Frame Buffer empty status can be indicated to the microcontroller through a dedicated pin.

Pin 24 (IRQ) can be configured as Frame Buffer Empty Indicator during the Frame Buffer read access. This mode is enabled by register bit RX_BL_CTRL (register 0x04, TRX_CTRL_1).

As shown in Figure 9-9, the pin 24 turns from IRQ into Frame Buffer Empty Indicator after the Frame Buffer read access command has been transferred on the SPI bus, see *(1)* in Figure 9-9. The pin 24 turns back to its regular function IRQ when the Frame Buffer read procedure has been completed by /SEL = H, see *(4)*.

Figure 9-9. Timing Diagram of Frame Buffer Empty Indicator



The microcontroller has to observe pin 24 during the Frame Buffer read procedure. A Frame Buffer read access can proceed as long as pin 24 = L, see *(2)*. Pin 24 = H indicates that the Frame Buffer is currently not ready for another SPI cycle, see *(3)*, and thus the Frame Buffer read procedure has to wait for valid data accordingly.

The Frame Buffer Empty Indicator pin 24 (IRQ) becomes effective t_{13} = 750 ns after the rising edge of last SCLK clock of the Frame Buffer read command byte.

After finishing the Frame Buffer read access by releasing /SEL = H, see *(4)*, pending interrupts are immediately indicated by pin IRQ.

If during the Frame Buffer read access a receive error occurs (e.g. a PLL unlock), the Frame Buffer Empty Indicator locks on 'empty' (pin 24 = H) too. To prevent possible deadlocks, the microcontroller should impose a timeout counter that checks whether the Frame Buffer Empty Indicator remains logic high for more than 2 octet periods. A new byte must have been arrived at the frame buffer during that period. If not, the Frame Buffer read access should be aborted.

9.6.2 Register Description

Register 0x04 (TRX_CTRL_1):

The TRX_CTRL_1 register is a multi purpose register to control various operating modes and settings of the radio transceiver.

Table 9-17. Register 0x04 (TRX_CTRL_1)

Bit	7	6	5	4
Name	PA_EXT_EN	IRQ_2_EXT_EN	TX_AUTO_CRC_ON	RX_BL_CTRL
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	1	0
Bit	3	2	1	0
Name	SPI_CMD_MODE	SPI_CMD_MODE	IRQ_MASK_MODE	IRQ_POLARITY
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0

- **Bit 7 – PA_EXT_EN**

Refer to section 9.4.3.

- **Bit 6 – IRQ_2_EXT_EN**

Refer to section 9.5.2.

- **Bit 5 – TX_AUTO_CRC_ON**

Refer to section 6.3.5.

- **Bit 4 – RX_BL_CTRL**

If this register bit is set, the Frame Buffer Empty Indicator is enabled. After sending a Frame Buffer read command (refer to section 4.3), pin 24 (IRQ) indicates that an access to the Frame Buffer is not possible since PSDU data are not available yet. Pin 24 (IRQ) does not indicate any interrupt during this time.

Table 9-18. Frame Buffer Empty Indicator

Register Bit	Value	Description
RX_BL_CTRL	0	Frame Buffer Empty Indicator disabled
	1	Frame Buffer Empty Indicator enabled

- **Bit 3:2 – SPI_CMD_MODE**

Refer to section 4.4.1.

- **Bit 1:0**

Refer to section 4.7.2.

9.7 Dynamic Frame Buffer Protection

9.7.1 Overview

The AT86RF212 continues the reception of incoming frames as long as it is in any receive state. When a frame is successfully received and stored in the Frame Buffer, the following frame overwrites the Frame Buffer content again.

To relax the timing requirements of a Frame Buffer read access, Dynamic Frame Buffer Protection prevents that a new incoming frame overwrites the Frame Buffer as long as the Frame Buffer read access has not been completed by /SEL = H, refer to section 4.3.

A received frame is automatically protected against overwriting

- in Basic Operating Mode if its FCS is valid
- in Extended Operating Mode if an IRQ_3 (TRX_END) is generated

The Dynamic Frame Buffer Protection is enabled if register bit RX_SAFE_MODE (register 0x0C, TRX_CTRL_2) is set and the transceiver state is RX_ON or RX_AACK_ON.

Note that Dynamic Frame Buffer Protection only prevents write accesses from the air interface and not from the SPI interface. A Frame Buffer or SRAM write access may still modify the Frame Buffer content.

9.7.2 Register Description

Register 0x0C (TRX_CTRL_2):

The TRX_CTRL_2 register is a multi purpose register to control various settings of the radio transceiver.

Table 9-19. Register 0x0C (TRX_CTRL_2)

Bit	7	6	5	4
Name	RX_SAFE_MODE	TRX_OFF_AVDD_EN	OQPSK_SCRAM_EN	OQPSK_SUB1_RC_EN
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	1	0
Bit	3	2	1	0
Name	BPSK_OQPSK	SUB_MODE	OQPSK_DATA_RATE	OQPSK_DATA_RATE
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0

- **Bit 7 – RX_SAFE_MODE**

If this bit is set, Dynamic Frame Buffer Protection is enabled.

Table 9-20. Dynamic Frame Buffer Protection Mode

Register Bit	Value	Description
RX_SAFE_MODE (1)	0	Disable Dynamic Frame Buffer protection
	1	Enable Dynamic Frame Buffer protection

Note: 1. Dynamic Frame Buffer Protection is deactivated automatically with the rising edge of pin 23 (/SEL) of a Frame Buffer read access (see section 4.3.2) or radio transceiver state change from RX_ON / RX_AACK_ON to another state.

- **Bit 6 – TRX_OFF_AVDD_EN**

Refer to sections 5.1.4.3 and 7.5.4.

- **Bit 5:0**

Refer to section 7.1.5.

9.8 Configurable Start-Of-Frame Delimiter (SFD)

9.8.1 Overview

The SFD is a field indicating the end of the SHR and the start of the packet data. The length of the SFD is 1 octet (8 symbols for BPSK and 2 symbols for O-QPSK). This octet is used for byte synchronization only and is not included in the Frame Buffer.

The value of the SFD can be changed if it is needed to operate non IEEE 802.15.4 compliant networks. An IEEE 802.15.4 compliant network node does not synchronize to frames with a different SFD value.

Due to the way the SHR is formed, it is not recommended to set the low-order 4 bits to 0. The LSB of the SFD is transmitted first, i.e. right after the last bit of the preamble sequence.

9.8.2 Register Description

Register 0x0B (SFD_VALUE):

This register contains the one octet start-of-frame delimiter (SFD) to synchronize to a received frame.

Table 9-21. Register 0x0B (SFD_VALUE)

Bit	7	6	5	4	3	2	1	0
Name	SFD_VALUE[7:0]							
Read/Write	R/W							
Reset Value	1	0	1	0	0	1	1	1

- **Bit 7:0 – SFD_VALUE**

For IEEE 802.15.4 compliant networks, set SFD_VALUE = 0xA7 as specified in [2]. This is the default value of the register.

To establish non IEEE 802.15.4 compliant networks, the SFD value can be changed to any other value. If enabled, IRQ_2 (RX_START) is issued only if the received SFD matches SFD_VALUE and a valid PHR is received.

10 Electrical Characteristics

10.1 Absolute Maximum Ratings

Note: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

No.	Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
10.1.1	T_{STOR}	Storage temperature		-50		150	°C
10.1.2	T_{LEAD}	Lead temperature	T = 10 s Soldering profile compliant with IPC/JEDEC J-STD-020B			260	°C
10.1.3	V_{ESD}	ESD robustness	Human Body Model (HBM) [7] Charged Device Model (CDM) [8]		6500 1250		V V
10.1.4	P_{RF}	Input RF level				10	dBm
10.1.5	V_{DIG}	Voltage on all pins except pins 4, 5, 13, 14, 29		-0.3		V_{DD}+0.3 ≤ 4.0	V
10.1.6	V_{ANA}	Voltage on pins 4, 5, 13, 14, 29		-0.3		2	V

10.2 Operating Range

No.	Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
10.2.1	T_{OP}	Operating temperature range		-40		85	°C
10.2.2	V_{DD}	Supply voltage	Voltage on pins 15, 28 (1)	1.8	3.0	3.6	V
10.2.3	$V_{DD1.8}$	Supply voltage	Voltage on pins 13, 14, 29 External voltage supply (1)(2)	1.7	1.8	1.9	V

Notes:
1. Even if an implementation uses the external 1.8 V voltage supply $V_{DD1.8}$, it is required to connect V_{DD}.
2. Register 0x10 (VREG_CTRL) needs to be programmed to disable internal voltage regulators and supply blocks, refer to section 7.5.

10.3 Digital Pin Specifications

Test Condition: T_{OP} = 25 °C

No.	Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
10.3.1	V_{IH}	High level input voltage (1)		V_{DD}-0.4			V
10.3.2	V_{IL}	Low level input voltage (1)				0.4	V
10.3.3	V_{OH}	High level output voltage (1)	For all output driver strength defined in TRX_CTRL_0	V_{DD}-0.4			V
10.3.4	V_{OL}	Low level output voltage (1)	For all output driver strength defined in TRX_CTRL_0			0.4	V

Note: 1. The capacitive load should not be larger than 50 pF for all I/Os when using the default driver strength settings, refer to section 2.2.2.1. Generally, large load capacitances increase the overall current consumption.

10.4 Digital Interface Timing Characteristics

Test Conditions: T_{OP} = 25 °C, V_{DD} = 3.0 V, C_L = 50 pF

No.	Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
10.4.1	f_{sync}	SCLK frequency	Synchronous operation			8	MHz
10.4.2	f_{async}	SCLK frequency	Asynchronous operation			7.5	MHz
10.4.3	t_1	/SEL falling edge to MISO active				180 (7)	ns
10.4.4	t_2	SCLK falling edge to MISO out	Data hold time	25 (7)			ns
10.4.5	t_3	MOSI setup time		10 (7)			ns
10.4.6	t_4	MOSI hold time		10 (7)			ns
10.4.7	t_5	LSB last byte to MSB next byte	SPI read/write, standard SRAM and frame access modes	250 (8)			ns
			Fast SRAM read/write access mode, refer to section 9.1.5	500 (8)			ns
10.4.8	t_6	/SEL rising edge to MISO tri state				10 (8)	ns
10.4.9	t_7	SLP_TR pulse width	TX start trigger	62.5		Note (1)	ns
10.4.10	t_8	SPI idle time between consecutive SPI accesses: SEL rising to falling edge	SPI read/write, standard SRAM and frame access modes	250 (8)			ns
			Fast SRAM read/write access mode, refer to section 9.1.5	500 (8)			ns
10.4.11	t_9	SCLK rising edge LSB to /SEL rising edge			250 (8)		ns
10.4.12	t_{10}	Reset pulse width	≥ 10 clock cycles at 16 MHz	625			ns
10.4.13	t_{11}	SPI access latency after reset	≥ 10 clock cycles at 16 MHz	625			ns
10.4.14	t_{12}	AES core cycle time			24		µs
10.4.15	t_{13}	Dynamic frame buffer protection: IRQ latency			750		ns
10.4.16	f_{CLKM}	Clock frequency at pin 17 (CLKM)	Programmable via register 0x03 (TRX_CTRL_0)		0 (2) 1 (2) 2 (2) 4 (2) 8 (2) 16 (2) 1/4 (2) 1/50 (3) 1/25 (4) 1/40 (5) 1/16 (6)		MHz MHz MHz MHz MHz MHz MHz MHz MHz MHz MHz
10.4.17	t_{IRQ}	IRQ_2, IRQ_3, IRQ_4 latency	Relative to the event to be indicated		9 (9)		µs

Notes:
1. Maximum pulse width less than (TX frame length + 16 µs)
2. All modes
3. Only in BPSK mode with f_{PSDU} = 20 kbit/s
4. Only in BPSK mode with f_{PSDU} = 40 kbit/s
5. Only in O-QPSK mode with f_{PSDU} = 100/200/400 kbit/s
6. Only in O-QPSK mode with f_{PSDU} = 250/500/1000 kbit/s
7. See Figure 4-3
8. See Figure 4-2
9. See Figure 5-2

10.5 General Transceiver Specifications

Test Conditions: T_{OP} = 25 °C, V_{DD} = 3.0 V

No.	Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
10.5.1	f_{RF}	Frequency range	1.0 MHz spacing 0.1 MHz spacing 0.1 MHz spacing 0.1 MHz spacing	769.0 769.0 857.0 903.0		935.0 794.5 882.5 928.5	MHz MHz MHz MHz
10.5.2	f_{CHIP}	Chip rate	BPSK as specified in [1, 2] BPSK as specified in [1, 2] O-QPSK as specified in [2] O-QPSK as specified in [2, 3]		300 600 400 1000		kchip/s kchip/s kchip/s kchip/s
10.5.3	f_{HDR}	Header bit rate (SHR, PHR)	BPSK as specified in [1, 2] BPSK as specified in [1, 2] O-QPSK as specified in [2] O-QPSK as specified in [2, 3]		20 40 100 250		kbit/s kbit/s kbit/s kbit/s
10.5.4	f_{PSDU}	PSDU bit rate	BPSK as specified in [1, 2] BPSK as specified in [1, 2] O-QPSK as specified in [2] O-QPSK as specified in [2, 3] O-QPSK O-QPSK O-QPSK O-QPSK		20 40 100 250 200 400 500 1000		kbit/s kbit/s kbit/s kbit/s kbit/s kbit/s kbit/s kbit/s
10.5.5	f_{CLK}	Crystal oscillator frequency	Reference oscillator		16		MHz
10.5.6		Reference oscillator accuracy	f_{PSDU} = 20/40/100/250 kbit/s f_{PSDU} = 200/400/500/1000 kbit/s	-60 (1) -40		+60 (1) +40	ppm ppm
10.5.7		Battery monitor threshold deviation		-0.1	0.0	0.1	V

Note:
1. A reference frequency accuracy of ±40 ppm is required by [1, 2, 3]

10.6 Transmitter Characteristics

Test Conditions: T_{OP} = 25 °C, V_{DD} = 3.0 V

No.	Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
10.6.1	P_{TX}	TX output power	Normal mode Boost mode		5 10		dBm dBm
10.6.2	P_{RANGE}	Output power range	22 steps		21		dB
10.6.3	P_{ACC}	Output power tolerance	868.3 MHz			±3	dB
10.6.4	P_{1dB}	1 dB compression point	Normal mode Boost mode		5 8		dBm dBm
10.6.5	EVM	Error vector magnitude	Power settings according to Table 7-15 Modulation: BPSK-20 BPSK-40 OQPSK-SIN-RC-100 OQPSK-SIN-250 OQPSK-RC-250		 5 8 29 10 10		 % RMS % RMS % RMS % RMS % RMS
10.6.6	P_{HARM}	Harmonics	Measured single ended @ RFP/ RFN into 50 Ω; constant wave signal Parameter: TX frequency, power				
		2^{nd} harmonic	914 MHz, 10 dBm		-23		dBm
			914 MHz, -2 dBm		-34		dBm
			868.3 MHz, 5 dBm		-33		dBm
			868.3 MHz, -2 dBm		-41		dBm
			782 MHz, 8 dBm		-26		dBm
			782 MHz, -2 dBm		-41		dBm
		3^{rd} harmonic	914 MHz, 10 dBm		-24		dBm
			914 MHz, -2 dBm		-37		dBm
			868.3 MHz, 5 dBm		-31		dBm
			868.3 MHz, -2 dBm		-39		dBm
			782 MHz, 8 dBm		-23		dBm
			782 MHz, -2 dBm		-34		dBm
10.6.7	P_{SPUR}	Spurious emissions	Except harmonics				
		30 – 1000 MHz	100 kHz RBW			-36	dBm
		1 – 12.75 GHz	1 MHz RBW			-30	dBm

10.7 Receiver Characteristics

Test Conditions: T_{OP} = 25 °C, V_{DD} = 3.0 V

No.	Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
10.7.1	P_{SENS}	Receiver sensitivity	AWGN channel, PER ≤ 1%				
		BPSK 20 kbit/s (1)(2)	PSDU length of 20 octets		-110		dBm
		BPSK 40 kbit/s (1)(2)	PSDU length of 20 octets		-108		dBm
		O-QPSK 100 kbit/s (2)	PSDU length of 20 octets		-101		dBm
		O-QPSK 250 kbit/s (2)(3)	PSDU length of 20 octets		-101		dBm
		O-QPSK 200 kbit/s	PSDU length of 127 octets		-98		dBm
		O-QPSK 400 kbit/s	PSDU length of 127 octets		-93		dBm
		O-QPSK 500 kbit/s	PSDU length of 127 octets		-98		dBm
		O-QPSK 1000 kbit/s	PSDU length of 127 octets		-93		dBm
10.7.2	NF	Noise figure			7		dB
10.7.3	P_{RXmax}	Maximum RX input level	PSDU length of 20 octets, PER ≤ 1%		-5		dBm
10.7.4		Channel rejection/selectivity BPSK-20 (1)(2)	P_{RX} = -89 dBm, PSDU length of 20 octets, PER ≤ 1%				
		Δf = -1 MHz			31		dB
		Δf = +1 MHz			19		dB
10.7.5		Channel rejection/selectivity BPSK-20 (1)(2)	P_{RX} = -89 dBm, PSDU length of 20 octets, PER ≤ 1%				
		|Δf | = 2 MHz			38		dB
10.7.6		Channel rejection/selectivity OQPSK-100 (2)	P_{RX} = -82 dBm, PSDU length of 20 octets, PER ≤ 1%				
		Δf = -1 MHz			24		dB
		Δf = +1 MHz			17		dB
10.7.7		Channel rejection/selectivity OQPSK-100 (2)	P_{RX} = -82 dBm, PSDU length of 20 octets, PER ≤ 1%				
		|Δf | = 2 MHz			35		dB
10.7.8		Adjacent channel rejection BPSK-40 (1)(2)	P_{RX} = -89 dBm, PSDU length of 20 octets, PER ≤ 1%				
		|Δf | = 2 MHz			36		dB
10.7.9		Alternate channel rejection BPSK-40 (1)(2)	P_{RX} = -89 dBm, PSDU length of 20 octets, PER ≤ 1%				
		|Δf | = 4 MHz			52		dB
10.7.10		Adjacent channel rejection OQPSK-SIN-250 (2)	P_{RX} = -82 dBm, PSDU length of 20 octets, PER ≤ 1%				
		|Δf | = 2 MHz			28 (4)		dB
10.7.11		Alternate channel rejection OQPSK-SIN-250 (2)	P_{RX} = -82 dBm, PSDU length of 20 octets, PER ≤ 1%				
		|Δf | = 4 MHz			42 (4)		dB

No.	Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
10.7.12		Adjacent channel rejection OQPSK-RC-250 (3) |Δf | = 2 MHz	P_{RX} = -82 dBm, PSDU length of 20 octets, PER ≤ 1%		 32		 dB
10.7.13		Alternate channel rejection OQPSK-RC-250 (3) |Δf | = 4 MHz	P_{RX} = -82 dBm, PSDU length of 20 octets, PER ≤ 1%		 49		 dB
10.7.14	P_{SPUR}	Spurious emissions LO leakage 30 – 1000 MHz 1 – 12.75 GHz	 Measured at $2 \cdot F_c$ - 4 MHz with balun (see Table 3-1) 100 kHz RBW 1 MHz RBW		 -71	 -57 -47	 dBm dBm dBm
10.7.15	IIP3	3rd-order intercept point	868.3 MHz, maximum gain Offset freq. interf. A = 2 MHz Offset freq. interf. B = 4 MHz		-12		dBm
10.7.16	IIP2	2nd-order intercept point	868.3 MHz, maximum gain Offset freq. interf. A = 3.2 MHz Offset freq. interf. B = 8.2 MHz		25		dBm
10.7.17		RSSI range	O-QPSK 250 kbit/s Lower threshold Upper threshold		 -100 -13		 dBm dBm
10.7.18		RSSI tolerance				±6	dB

Notes:
1. IEEE 802.15.4-2003 compliant
2. IEEE 802.15.4-2006 compliant
3. IEEE 802.15.4c-2009 compliant
4. Channel rejection is limited by modulation side lobes of interfering signal, see Figure 7-7.

10.8 Current Consumption Specifications

Test Conditions: T_{OP} = 25 °C, V_{DD} = 3.0 V, CLKM = OFF

No.	Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
10.8.1	I_{BUSY_TX}	Supply current transmit state	North American band, O-QPSK modulation P_{TX} = 0 dBm (normal mode) P_{TX} = 5 dBm (normal mode) P_{TX} = 10 dBm (boost mode)		 13 17 25		 mA mA mA
10.8.2	I_{RX_ON}	Supply current RX_ON (listen) state	North American band, O-QPSK modulation Highest sensitivity (RX_PDT_LEVEL = 0) Reduced sensitivity (RX_PDT_LEVEL > 0)		 9.2 8.7		 mA mA
10.8.3	I_{PLL_ON}	Supply current PLL_ON state			4.7		mA
10.8.4	I_{TRX_OFF}	Supply current TRX_OFF state			0.4		mA
10.8.5	I_{SLEEP}	Supply current SLEEP state			0.2		µA

10.9 Crystal Parameter Requirements

No.	Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
10.9.1	f_0	Crystal frequency			16		MHz
10.9.2	C_L	Load capacitance		8		14	pF
10.9.3	C_0	Crystal shunt capacitance				7	pF
10.9.4	ESR	Equivalent series resistance				100	Ω

11 Register Reference

The AT86RF212 provides a register space of 64 8-bit registers used to configure, control, and monitor the radio transceiver.

Note: All registers not mentioned within the following table are reserved for internal use and must not be overwritten. When writing to a register, any reserved bits shall be overwritten only with their reset value.

Table 11-1. Register Summary

Addr.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
0x00										
0x01	TRX_STATUS	CCA_DONE	CCA_STATUS		TRX_STATUS[4:0]					40,59,86
0x02	TRX_STATE	TRAC_STATUS[2:0]			TRX_CMD[4:0]					41, 60
0x03	TRX_CTRL_0	PAD_IO[1:0]		PAD_IO_CLKM[1]		CLKM_SHA_SEL	CLKM_CTRL[2:0]			8, 120
0x04	TRX_CTRL_1	PA_EXT_EN	IRQ_2_EXT_EN	TX_AUTO_CRC_ON	RX_BL_CTRL	SPI_CMD_MODE[1:0]		IRQ_MASK_MODE	IRQ_POLARITY	21,27,61, 78,143, 145,147
0x05	PHY_TX_PWR	PA_BOOST	GC_PA[1:0]		TX_PWR[4:0]					106
0x06	PHY_RSSI	RX_CRC_VALID	RND_VALUE[1:0]		RSSI[4:0]					79, 81, 140
0x07	PHY_ED_LEVEL	ED_LEVEL[7:0]								84
0x08	PHY_CC_CCA	CCA_REQUEST	CCA_MODE[1:0]		CHANNEL[4:0]					87, 89, 125
0x09	CCA_THRES					CCA_ED_THRES[3:0]				88, 90
0x0A	RX_CTRL			JCM_EN						122
0x0B	SFD_VALUE	SFD_VALUE[7:0]								149
0x0C	TRX_CTRL_2	RX_SAFE_MODE	TRX_OFF_AVDD_EN	OQPSK_SCRAM_EN	OQPSK_SUB1_RC_EN	BPSK_OQPSK	SUB_MODE	OQPSK_DATA_RATE[1:0]		95,114, 148
0x0D	ANT_DIV						ANT_EXT_SW_EN	ANT_CTRL[1:0]		141
0x0E	IRQ_MASK	MASK_BAT_LOW	MASK_TRX_UR	MASK_AMI	MASK_CCA_ED_DONE	MASK_TRX_END	MASK_RX_START	MASK_PLL_UNLOCK	MASK_PLL_LOCK	26
0x0F	IRQ_STATUS	BAT_LOW	TRX_UR	AMI	CCA_ED_DONE	TRX_END	RX_START	PLL_UNLOCK	PLL_LOCK	27
0x10	VREG_CTRL	AVREG_EXT	AVDD_OK			DVREG_EXT	DVDD_OK			113
0x11	BATMON	PLL_LOCK_CP		BATMON_OK	BATMON_HR	BATMON_VTH[3:0]				116, 128
0x12	XOSC_CTRL	XTAL_MODE[3:0]				XTAL_TRIM[3:0]				121
0x13	CC_CTRL_0	CC_NUMBER[7:0]								126
0x14	CC_CTRL_1						CC_BAND[2:0]			126
0x15	RX_SYN	RX_PDT_DIS				RX_PDT_LEVEL[3:0]				99
0x16	RF_CTRL_0	PA_LT[1:0]						GC_TX_OFFS[1:0]		105
0x17	XAH_CTRL_1		CSMA_LBT_MODE	AACK_FLTR_RES_FT	AACK_UPLD_RES_FT		AACK_ACK_TIME	AACK_PROM_MODE		62,73, 90
0x18	FTN_CTRL	FTN_START								129
0x19	RF_CTRL_1	RF_MC[3:0]								99
0x1A	PLL_CF	PLL_CF_START			PLL_CF[4:0]					127
0x1B	PLL_DCU	PLL_DCU_START								127
0x1C	PART_NUM	PART_NUM[7:0]								22
0x1D	VERSION_NUM	VERSION_NUM[7:0]								22
0x1E	MAN_ID_0	MAN_ID_0[7:0]								22
0x1F	MAN_ID_1	MAN_ID_1[7:0]								23
0x20	SHORT_ADDR_0	SHORT_ADDR_0[7:0]								74
0x21	SHORT_ADDR_1	SHORT_ADDR_1[7:0]								74

Addr.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
0x22	PAN_ID_0	PAN_ID_0[7:0]								74
0x23	PAN_ID_1	PAN_ID_1[7:0]								74
0x24	IEEE_ADDR_0	IEEE_ADDR_0[7:0]								75
0x25	IEEE_ADDR_1	IEEE_ADDR_1[7:0]								75
0x26	IEEE_ADDR_2	IEEE_ADDR_2[7:0]								75
0x27	IEEE_ADDR_3	IEEE_ADDR_3[7:0]								75
0x28	IEEE_ADDR_4	IEEE_ADDR_4[7:0]								76
0x29	IEEE_ADDR_5	IEEE_ADDR_5[7:0]								76
0x2A	IEEE_ADDR_6	IEEE_ADDR_6[7:0]								76
0x2B	IEEE_ADDR_7	IEEE_ADDR_7[7:0]								76
0x2C	XAH_CTRL_0	MAX_FRAME_RETRIES[3:0]				MAX_CSMA_RETRIES[2:0]			SLOTTED_OPERATION	63
0x2D	CSMA_SEED_0	CSMA_SEED_0[7:0]								64
0x2E	CSMA_SEED_1	AACK_FVN_MODE[1:0]		AACK_SET_PD	AACK_DIS_ACK	AACK_I_AM_ COORD	CSMA_SEED_1[2:0]			65, 76
0x2F	CSMA_BE	MAX_BE[3:0]				MIN_BE[3:0]				66
....										

Power-on reset values of the AT86RF212 registers in state P_ON are shown in Table 11-2. After a reset procedure (/RST = L as described in section 5.1.4.5), the reset values of selected registers (e.g. registers 0x01, 0x10, 0x11, 0x30) can differ from that in Table 11-2.

Table 11-2. Register Summary – Reset Values

Address	Reset Value		Address	Reset Value		Address	Reset Value		Address	Reset Value
0x00	0x00		0x10	0x00 (1)		0x20	0xFF		0x30	0x00 (3)
0x01	0x00		0x11	0x02 (2)		0x21	0xFF		0x31	0x00
0x02	0x00		0x12	0xF0		0x22	0xFF		0x32	0x00
0x03	0x19		0x13	0x00		0x23	0xFF		0x33	0x00
0x04	0x20		0x14	0x00		0x24	0x00		0x34	0x3F
0x05	0x60		0x15	0x00		0x25	0x00		0x35	0x00
0x06	0x00		0x16	0x31		0x26	0x00		0x36	0x00
0x07	0xFF		0x17	0x00		0x27	0x00		0x37	0x00
0x08	0x25		0x18	0x58		0x28	0x00		0x38	0x00
0x09	0x77		0x19	0x00		0x29	0x00		0x39	0x40
0x0A	0x17		0x1A	0x48		0x2A	0x00		0x3A	0x00
0x0B	0xA7		0x1B	0x40		0x2B	0x00		0x3B	0x00
0x0C	0x24		0x1C	0x07		0x2C	0x38		0x3C	0x00
0x0D	0x01		0x1D	VERSION_NUM		0x2D	0xEA		0x3D	0x00
0x0E	0x00		0x1E	0x1F		0x2E	0x42		0x3E	0x00
0x0F	0x00		0x1F	0x00		0x2F	0x53		0x3F	0x00

Notes:
1. While the reset value of register 0x10 is 0x00, any practical access to the register is only possible when DVREG is active. So this register is always read out as 0x04. For details, refer to section 7.5.
2. While the reset value of register 0x11 is 0x02, any practical access to the register is only possible when BATMON is activated. So this register is always read out as 0x22 in P_ON state. For details, refer to section 7.6.
3. While the reset value of register 0x30 is 0x00, any practical access to the register is only possible when the radio transceiver is accessible. So the register is usually read out as:

   a) 0x11 after a reset in P_ON state

   b) 0x07 after a reset in any other state

12 Abbreviations

ACK	—	Acknowledgement
ADC	—	Analog-to-Digital Converter
AES	—	Advanced Encryption Standard
AGC	—	Automatic Gain Control
AVREG	—	Analog Voltage Regulator
AWGN	—	Additive White Gaussian Noise
BATMON	—	Battery Monitor
BBP	—	Base-Band Processor
BPF	—	Band-Pass Filter
BPSK	—	Binary Phase Shift Keying
CBC	—	Cipher Block Chaining
CCA	—	Clear Channel Assessment
CF	—	Center Frequency
CRC	—	Cyclic Redundancy Check
CS	—	Carrier Sense
CSMA-CA	—	Carrier Sense Multiple Access – Collision Avoidance
CW	—	Continuous Wave
DAC	—	Digital-to-Analog Converter
DVREG	—	Digital Voltage Regulator
ECB	—	Electronic Code Book
ED	—	Energy Detect
ESD	—	Electro Static Discharge
F_c	—	Channel Center Frequency
FCF	—	Frame Control Field
FCS	—	Frame Check Sequence
FIFO	—	First In, First Out
FTN	—	Filter Tuning
GPIO	—	General Purpose Input/Output
IC	—	Integrated Circuit
IEEE	—	Institute of Electrical and Electronic Engineers
IF	—	Intermediate Frequency
I/O	—	Input/Output
IRQ	—	Interrupt Request
ISM	—	Industrial Scientific Medical
LBT	—	Listen Before Talk
LDO	—	Low Dropout
LNA	—	Low-Noise Amplifier
LO	—	Local Oscillator
LPF	—	Low-Pass Filter
LQI	—	Link Quality Indication
LSB	—	Least Significant Bit
MAC	—	Medium Access Control
MHR	—	MAC Header
MIC	—	Message Integrity Code
MISO	—	Master Input, Slave Output
MOSI	—	Master Output, Slave Input
MSB	—	Most Significant Bit
MSDU	—	MAC Service Data Unit
NOP	—	No Operation
O-QPSK	—	Offset Quadrature Phase Shift Keying
PA	—	Power Amplifier
PAN	—	Personal Area Network

PER	—	Packet Error Rate
PHR	—	PHY Header
PHY	—	Physical Layer
PLL	—	Phase-Looked Loop
PPDU	—	PHY Protocol Data Unit
PPF	—	Poly-Phase Filter
PRBS	—	Pseudo Random Binary Sequence
PSD	—	Power Spectrum Density
PSDU	—	PHY Service Data Unit
QFN	—	Quad Flat No-Lead Package
RBW	—	Resolution Bandwidth
RC	—	Raised Cosine
RF	—	Radio Frequency
RMS	—	Root Mean Square
RSSI	—	Received Signal Strength Indicator
RX	—	Receiver
SFD	—	Start-Of-Frame Delimiter
SHR	—	Synchronization Header
SPI	—	Serial Peripheral Interface
SRAM	—	Static Random Access Memory
SRD	—	Short Range Device
TRX	—	Transceiver
TX	—	Transmitter
VBW	—	Video Bandwidth
VCO	—	Voltage Controlled Oscillator
WPAN	—	Wireless Personal Area Network
XOSC	—	Crystal Oscillator
XTAL	—	Crystal

13 Ordering Information

Ordering Code	Packaging	Package	Voltage Range	Temperature Range
AT86RF212-ZU	Tray	QN	1.8 V – 3.6 V	Industrial (-40 °C to +85 °C) Lead-free/Halogen-free
AT86RF212-ZUR	Tape & Reel	QN	1.8 V – 3.6 V	Industrial (-40 °C to +85 °C) Lead-free/Halogen-free

Package Type	Description
QN	32QN2, 32-lead 5.0x5.0 mm Body, 0.50 mm Pitch, Quad Flat No-lead Package (QFN) Sawn

Note: T&R quantity 5,000.

Please contact your local Atmel sales office for more detailed ordering information and minimum quantities.

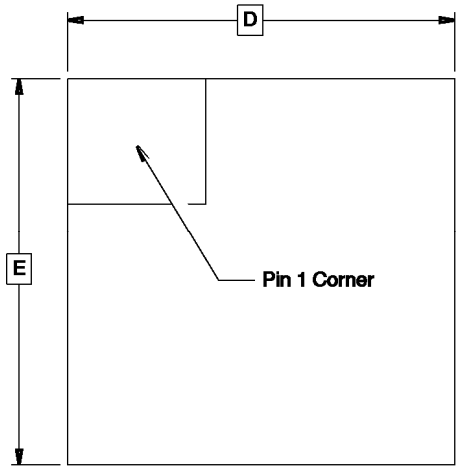
14 Soldering Information

Recommended soldering profile is specified in IPC/JEDEC J-STD-.020C.

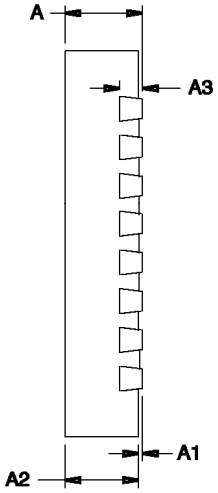
15 Package Thermal Properties

Thermal Resistance	
Velocity [m/s]	Theta ja [K/W]
0	40.9
1	35.7
2.5	32.0

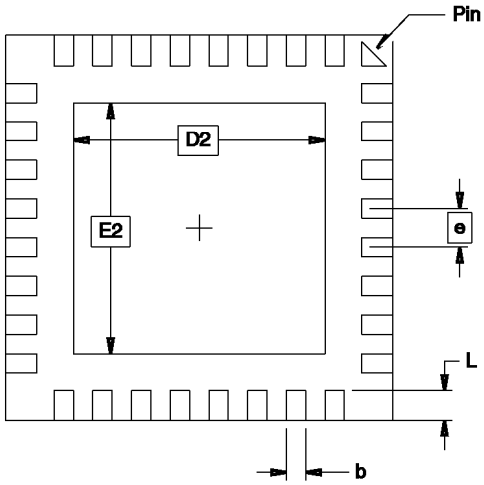
16 Package Drawing – 32QN2



Top View



Side View



Bottom View

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
D		5.00 BSC		
E		5.00 BSC		
D2	3.20	3.30	3.40	
E2	3.20	3.30	3.40	
A	0.80	0.90	1.00	
A1	0.0	0.02	0.05	
A2	0.0	0.65	1.00	
A3		0.20 REF		
L	0.30	0.40	0.50	
e		0.50 BSC		
b	0.18	0.23	0.30	2

Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MO-220, Variation VHHD-6, for proper dimensions, tolerances, datums, etc.
2. Dimension b applies to metallized terminal and is measured between 0.15 mm and 0.30 mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension should not be measured in that radius area.

11/26/07

	TITLE	GPC	DRAWING NO.	REV.
Package Drawing Contact: packagedrawings@atmel.com	**32QN2**, 32-lead 5.0 x 5.0 mm Body, 0.50 mm Pitch, Quad Flat No Lead Package (QFN) Sawn	ZJZ	32QN2	A

Appendix A – Continuous Transmission Test Mode

A.1 – Overview

The AT86RF212 offers a Continuous Transmission Test Mode to support application / production tests as well as certification tests. Using this test mode, the radio transceiver transmits continuously a previously transferred frame (PRBS mode) or a continuous wave signal (CW mode).

In CW mode, one of four different signal frequencies per channel can be transmitted:

- $f_1 = F_c + 0.25$ MHz using O-QPSK 1000 kbit/s mode
- $f_2 = F_c - 0.25$ MHz using O-QPSK 1000 kbit/s mode
- $f_3 = F_c + 0.1$ MHz using O-QPSK 400 kbit/s mode
- $f_4 = F_c - 0.1$ MHz using O-QPSK 400 kbit/s mode

F_c is the channel center frequency, refer to section 7.8.2. Note that in CW mode it is not possible to transmit a RF signal directly on the channel center frequency.

Data in the Frame Buffer must contain a valid PHR (see section 6.1) followed by PSDU data. After transmission of two non-PSDU symbols, PSDU data is repeated continuously.

A.2 – Configuration

Before enabling Continuous Transmission Test Mode, register configurations shall be done as follows:

- TX channel setting (optional)
- TX output power setting (optional)
- Mode selection: PRBS or CW mode. PRBS mode further requires selection of a modulation scheme; CW mode further requires selection of the carrier position.

Register write accesses to register 0x36 and 0x1C enable the Continuous Transmission Test Mode. The transmission is started by enabling the PLL (TRX_CMD = PLL_ON) and writing the TX_START command to register 0x02.

The detailed programming sequence is shown in Table A-1. The column R/W informs about writing (W) or reading (R) a register or the Frame Buffer.

Table A-1. Continuous Transmission Programming Sequence

Step	Action	Register	R/W	Value	Description
1	Reset				Reset AT86RF212
2	Register access	0x0E	W	0x01	Set IRQ mask register, enable IRQ_0 (PLL_LOCK)
3	Register access	0x02	W	0x03	Set radio transceiver state TRX_OFF
4	Register access		W		Set channel, refer to section 7.8.2.
5	Register access		W		Set TX output power, refer to section 7.3.4. For CW mode, GC_TX_OFFS should be set to 2.
6	Register access	0x01	R	0x08	Verify TRX_OFF state
7	Register access	0x36	W	0x0F	Enable Continuous Transmission Test Mode – step # 1

Step	Action	Register	R/W	Value	Description
8	Register access	0x0C	W		Select PRBS mode with modulation scheme or CW mode with carrier position:
				0x00	PRBS mode, BPSK-20
				0x04	PRBS mode, BPSK-40
				0x08	PRBS mode, OQPSK-SIN-RC-100
				0x0C	PRBS mode, OQPSK-SIN-250
				0x1C	PRBS mode, OQPSK-RC-250
				0x0A	CW mode, CW at F_c ± 0.1 MHz
				0x0E	CW mode, CW at F_c ± 0.25 MHz
9	Frame Buffer write access		W	{PHR, PSDU}	PRBS mode: Write PHR value (0x01 … 0x7F) followed by PSDU data. PHR determines how many bytes of the PSDU data are repeated continuously.
				{0x01, 0x00}	CW mode, CW at F_c - 0.1 MHz
				{0x01, 0xFF}	CW mode, CW at F_c + 0.1 MHz
				{0x01, 0x00}	CW mode, CW at F_c - 0.25 MHz
				{0x01, 0xFF}	CW mode, CW at F_c + 0.25 MHz
10	Register access	0x1C	W	0x54	Enable Continuous Transmission Test Mode – step # 2
11	Register access	0x1C	W	0x46	Enable Continuous Transmission Test Mode – step # 3
12	Register access	0x02	W	0x09	Enable PLL_ON state
13	Interrupt event	0x0F	R	0x01	Wait for IRQ_0 (PLL_LOCK)
14	Register access	0x02	W	0x02	Initiate transmission, enter BUSY_TX state
15	Measurement				Perform measurement
16	Register access	0x1C	W	0x00	Disable Continuous Transmission Test Mode
17	Reset				Reset AT86RF212

Appendix B – Errata

AT86RF212 Rev. A

1. **Power-on Reset**
   It can not be guaranteed that power-on reset (as described in section 5.1.2.1) is working under all circumstances.

   Problem Fix / Workaround
   The following programming sequence should be executed after power-on to completely reset the transceiver. Please note that the microcontroller can not count on CLKM before finalization of step 5, refer to Table A-5.

   Table A-5. Reset Procedure after Power-on

Step	Action	Register/Pin Access	Description
1	Power-on	Apply external supply voltage	
2	Set the input pins to the default operating values	SLP_TR = L /RST = H /SEL = H	Refer to section 5.1.2.1
3	Wait for at least 400 µs		Refer to section 5.1.4.1
4	Reset the transceiver	/RST = L for at least 625 ns (t_{10})	Refer to section 5.1.4.5
5	Set CLKM rate to 1 MHz	Register 0x03 = 0x19	Refer to section 7.7.6
6	Force TRX_OFF	Register 0x02 = 0x03	Refer to section 5.1.5

References

[1] IEEE Standard 802.15.4™-2003: Wireless Medium Access Control (MAC) and Physical Layer (PHY) Specifications for Low-Rate Wireless Personal Area Networks (WPANs).

[2] IEEE Standard 802.15.4™-2006: Wireless Medium Access Control (MAC) and Physical Layer (PHY) Specifications for Low-Rate Wireless Personal Area Networks (WPANs).

[3] IEEE Standard 802.15.4c™-2009: Wireless Medium Access Control (MAC) and Physical Layer (PHY) Specifications for Low-Rate Wireless Personal Area Networks (WPANs):
Amendment 2: Alternative Physical Layer Extension to support one or more of the Chinese 314-316 MHz, 430-434 MHz, and 779-787 MHz bands.

[4] FCC Title 47 (Telecommunication) of the Code of Federal Regulations, Part 15 (Radio Frequency Devices), October 2008

[5] ETSI EN 300 220-1 V2.3.1 (2009-04): Electromagnetic compatibility and Radio spectrum Matters (ERM); Short Range Devices (SRD); Radio equipment to be used in the 25 MHz to 1 000 MHz frequency range with power levels ranging up to 500 mW; Part 1: Technical characteristics and test methods.

[6] ERC Recommendation 70-03 relating to the use of short range devices (SRD). Version of 18 February 2009.

[7] ANSI/ESD STM5.1 – 2007, Electrostatic Discharge Sensitivity Testing – Human Body Model (HBM); JESD22-A114E – 2006; CEI/IEC 60749-26 – 2006; AEC-Q100-002-Ref-D

[8] ESD-STM5.3.1-1999: ESD Association Standard Test Method for electrostatic discharge sensitivity testing – Charged Device Model (CDM).

[9] NIST FIPS PUB 197: Advanced Encryption Standard (AES), Federal Information Processing Standards Publication 197, US Department of Commerce/NIST, November 26, 2001

Data Sheet Revision History

Please note that the referring page numbers in this section are referring to this document. Revisions in this section are referring to the document revisions.

Rev. 8168C-MCU Wireless-02/10

1. Updated Table 5-1on page 38 and Table 5-2 on page 39.
2. Updated section 6.4.3 on page 80.
3. Updated Table 7-9 on page 101.
4. Updated Table 7-15 on page 107 and corresponding Figure 7-10 on page 108.
5. Updated section 10 on page 150ff.
6. Added Appendix B – Errata.
7. Editorial updates.

Rev. 8168B-MCU Wireless-02/09

1. Added operation in the Chinese 780 MHz band.
2. Added section 7.7.5 “Clock Jitter” on page 120.
3. Updated Table 7-15 on page 107 and corresponding Figure 7-10 on page 108.
4. Updated section 10 on page 150ff.
5. Editorial updates.

Rev. 8168A-AVR-06/08

1. Initial revision.

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