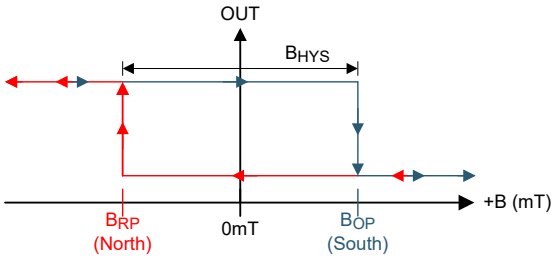
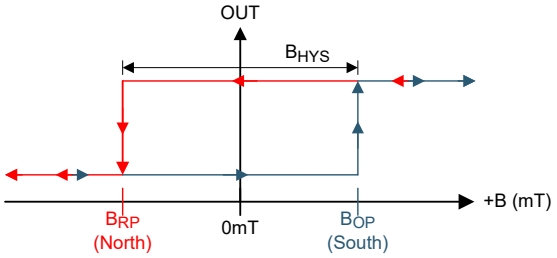
# DRV5013 Digital-Latch Hall Effect Sensor

## 1 Features

- Digital bipolar-latch Hall sensor
- Superior temperature stability
  - $B_{OP}$ ±10% over temperature
- Multiple sensitivity options ($B_{OP}$ / $B_{RP}$)
  - ±1.3mT (FA, FD, see *Device Nomenclature*)
  - ±2.7mT (AD, ND, see *Device Nomenclature*)
  - ±6mT (AG, see *Device Nomenclature*)
  - ±12mT (BC, see *Device Nomenclature*)
- Supports a wide voltage range
  - 2.5V to 38V
  - No external regulator required
- Wide operating temperature range
  - $T_A$ = –40 to +125°C (Q, see *Device Nomenclature*)
  - $T_A$ = –40 to +150°C (E, see *Device Nomenclature*)
- Open-drain output (30mA sink)
- Fast 35µs power-on time
- Small package and footprint
  - Surface mount 3-pin SOT-23 (DBZ)
    - 2.92mm × 2.37mm
  - Through-hole 3-pin TO-92 (LPG, LPE)
    - 4mm × 3.15mm
- **Protection features:**
  - Reverse supply protection (up to –22V)
  - Supports up to 40V load dump
  - Output short-circuit protection
  - Output current limitation




**Output State (FA, AD, AG, BC Versions)**




**Inverted Output State (ND, FD Version)**

## 2 Applications

- Power tools
- Flow meters
- Valve and solenoid status
- Brushless dc motors
- Proximity sensing
- Tachometers

## 3 Description

The DRV5013 device is a chopper-stabilized Hall effect sensor that offers a magnetic sensing solution with superior sensitivity stability over temperature and integrated protection features.

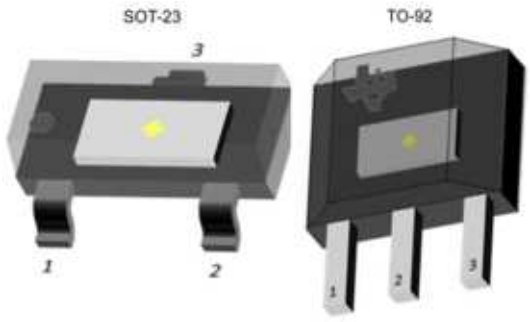
The magnetic field is indicated through a digital bipolar latch output. The IC has an open-drain output stage with 30-mA current sink capability. A wide operating voltage range from 2.5V to 38 V with reverse polarity protection up to –22 V makes the device suitable for a wide range of industrial applications.

Internal protection functions are provided for reverse supply conditions, load dump, and output short circuit or overcurrent.

**Package Information** (1)

| PART NUMBER | PACKAGE | BODY SIZE (NOM) (2) |
|---|---|---|
| DRV5013 | DBZ (SOT-23, 3) | 2.92mm × 2.37mm |
| | LPE (TO-92, 3) | 4mm × 3.15mm |
| | LPG (TO-92, 3) | 4mm × 3.15mm |

(1) For all available packages, see the package option addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.




**Device Packages**

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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## 4 Pin Configuration and Functions

For additional configuration information, see *Device Markings* and *Mechanical, Packaging, and Orderable Information*.

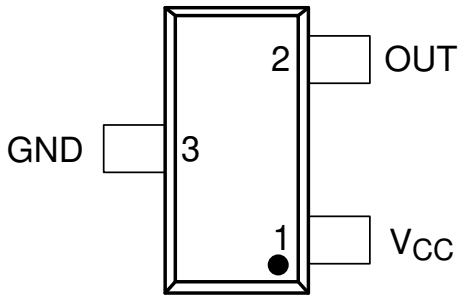



**Figure 4-1. DBZ Package 3-Pin SOT-23 Top View**

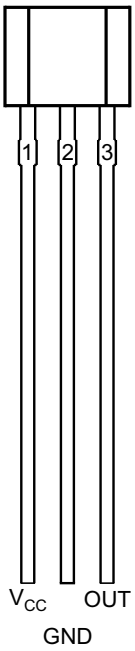



**Figure 4-2. LPG and LPE Packages 3-Pin TO-92 Top View**

**Table 4-1. Pin Functions**

| PIN | | | TYPE | DESCRIPTION |
|---|---|---|---|---|
| NAME | DBZ | LPG, LPE | | |
| GND | 3 | 2 | Ground | Ground pin |
| OUT | 2 | 3 | Output | Hall sensor open-drain output. The open drain requires a resistor pullup. |
| $V_{CC}$ | 1 | 1 | Power | 2.5 V to 38 V power supply. Bypass this pin to the GND pin with a 0.01-µF (minimum) ceramic capacitor rated for $V_{CC}$. |

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# 5 Specifications

## 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Power supply voltage | $V_{CC}$ | –22 (2) | 40 | V |
| | Voltage ramp rate ($V_{CC}$), $V_{CC}$ < 5V | Unlimited | | V/µs |
| | Voltage ramp rate ($V_{CC}$), $V_{CC}$ > 5V | 0 | 2 | |
| Output pin voltage | | –0.5 | 40 | V |
| Output pin reverse current during reverse supply condition | | 0 | 100 | mA |
| Magnetic flux density, $B_{MAX}$ | | Unlimited | | |
| Operating junction temperature, $T_J$ | Q, see Figure 8-1 | –40 | 150 | °C |
| | E, see Figure 8-1 | –40 | 175 | |
| Storage temperature, $T_{stg}$ | | –65 | 150 | °C |

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Specified by design. Only tested to –20 V.

## 5.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1) | ±2500 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2) | ±500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Power supply voltage | | 2.5 | 38 | V |
| $V_O$ | Output pin voltage (OUT) | | 0 | 38 | V |
| $I_{SINK}$ | Output pin current sink (OUT)(1) | | 0 | 30 | mA |
| $T_A$ | Operating ambient temperature | Q, see Figure 8-1 | –40 | 125 | °C |
| | | E, see Figure 8-1 | –40 | 150 | |

(1) Power dissipation and thermal limits must be observed.


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## 5.4 Thermal Information

| THERMAL METRIC[1] | | DRV5013 | | UNIT |
|---|---|---|---|---|
| | | DBZ (SOT-23) | LPG, LPE (TO-92) | |
| | | 3 PINS | 3 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 333.2 | 180 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 99.9 | 98.6 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 66.9 | 154.9 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 4.9 | 40 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 65.2 | 154.9 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **POWER SUPPLIES ($V_{CC}$)** | | | | | | |
| $V_{CC}$ | $V_{CC}$ operating voltage | | 2.5 | | 38 | V |
| $I_{CC}$ | Operating supply current | ND, FD Versions<br>$V_{CC}$ = 2.5V to 38V, $T_A$ = 25°C | | 1.5 | | mA |
| | | ND, FD Versions<br>$V_{CC}$ = 2.5V to 38V, $T_A$ = $T_{A, MAX}$ (1) | | 1.5 | 3.2 | |
| | | AD, AG, BC, FA Versions<br>$V_{CC}$ = 2.5V to 38V, $T_A$ = 25°C | | 2.7 | | |
| | | AD, AG, BC, FA Versions<br>$V_{CC}$ = 2.5V to 38V, $T_A$ = $T_{A, MAX}$ (1) | | 3 | 3.5 | |
| $t_{on}$ | Power-on time | AD, AG, BC, ND versions | | 35 | 50 | µs |
| | | FA, FD version | | 35 | 70 | |
| **OPEN DRAIN OUTPUT (OUT)** | | | | | | |
| $r_{DS(on)}$ | FET on-resistance | $V_{CC}$ = 3.3V, $I_O$ = 10mA, $T_A$ = 25°C | | 22 | | Ω |
| | | $V_{CC}$ = 3.3V, $I_O$ = 10mA, $T_A$ = $T_{A,MAX}$ (1) | | 36 | 50 | |
| $I_{lkg(off)}$ | Off-state leakage current | Output Hi-Z | | | 1 | µA |
| **PROTECTION CIRCUITS** | | | | | | |
| $V_{CCR}$ | Reverse supply voltage | | –22 | | | V |
| $I_{OCP}$ | Overcurrent protection level | OUT shorted $V_{CC}$ | 15 | 30 | 45 | mA |

(1) $T_{A, MAX}$ is 125°C for Q devices and 150°C for E devices (see Figure 8-1).

## 5.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **OPEN-DRAIN OUTPUT (OUT)** | | | | | | |
| $t_d$ | Output delay time | B = $B_{RP}$ – 10mT to $B_{OP}$ + 10mT in 1µs | | 13 | 25 | µs |
| $t_r$ | Output rise time (10% to 90%) | R1 = 1kΩ, $C_O$ = 50pF, $V_{CC}$ = 3.3V | | 200 | | ns |
| $t_f$ | Output fall time (90% to 10%) | R1 = 1kΩ, $C_O$ = 50pF, $V_{CC}$ = 3.3V | | 31 | | ns |

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## 5.7 Magnetic Characteristics

over operating free-air temperature range (unless otherwise noted)

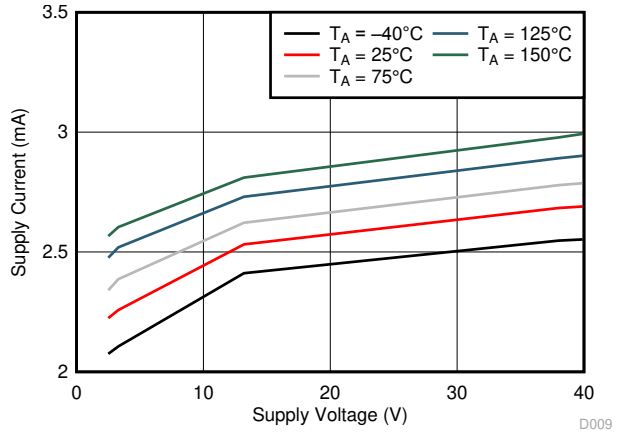
| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT(1) |
|---|---|---|---|---|---|---|
| **Bandwidth** | | | | | | |
| $f_{BW}$ | Bandwidth(2) | | 20 | 30 | | kHz |
| **DRV5013FA, DRV5013FD: ±1.3 mT** | | | | | | |
| $B_{OP}$ | Operate point; see Figure 6-2 | $T_A$ = –40°C to $T_{A,MAX}$ (3) | –0.6 | 1.3 | 3.4 | mT |
| $B_{RP}$ | Release point; see Figure 6-2 | | –3.4 | –1.3 | 0.6 | |
| $B_{hys}$ | Hysteresis; $B_{hys} = (B_{OP} – B_{RP})$ | | 1.2 | 2.6 | | |
| $B_O$ | Magnetic offset; $B_O = (B_{OP} + B_{RP}) / 2$ | | –1.5 | 0 | 1.5 | |
| **DRV5013AD: ±2.7 mT** | | | | | | |
| $B_{OP}$ | Operate point; see Figure 6-2 | $T_A$ = –40°C to $T_{A,MAX}$ (3) | 1 | 2.7 | 5 | mT |
| $B_{RP}$ | Release point; see Figure 6-2 | | –5 | –2.7 | –1 | |
| $B_{hys}$ | Hysteresis; $B_{hys} = (B_{OP} – B_{RP})$ | | | 5.4 | | |
| $B_O$ | Magnetic offset; $B_O = (B_{OP} + B_{RP}) / 2$ | | –1.5 | 0 | 1.5 | |
| **DRV5013ND: ±2.7 mT** | | | | | | |
| $B_{OP}$ | Operate point; see Figure 6-3 | $T_A$ = 25°C | 2 | 2.7 | 3.3 | mT |
| | | $T_A$ = –40°C to $T_{A,MAX}$ (3) | 1.5 | 2.7 | 3.6 | |
| $B_{RP}$ | Release point; see Figure 6-3 | $T_A$ = 25°C | –3.3 | –2.7 | –2 | |
| | | $T_A$ = –40°C to $T_{A,MAX}$ (3) | –3.6 | –2.7 | –1.5 | |
| $B_{hys}$ | Hysteresis; $B_{hys} = (B_{OP} – B_{RP})$ | $T_A$ = 25°C | 4.3 | 5.4 | | |
| | | $T_A$ = –40°C to $T_{A,MAX}$ (3) | 3 | 5.4 | | |
| $B_O$ | Magnetic offset; $B_O = (B_{OP} + B_{RP}) / 2$ | $T_A$ = 25°C | –0.5 | 0 | 0.5 | |
| | | $T_A$ = –40°C to $T_{A,MAX}$ (3) | –1 | 0 | 1 | |
| **DRV5013AG: ±6 mT** | | | | | | |
| $B_{OP}$ | Operate point | $T_A$ = –40°C to $T_{A,MAX}$ (3) | 3 | 6 | 9 | mT |
| $B_{RP}$ | Release point | | –9 | –6 | –3 | mT |
| $B_{hys}$ | Hysteresis; $B_{hys} = (B_{OP} – B_{RP})$ | $T_A$ = –40°C to $T_{A,MAX}$ (3) | | 12 | | mT |
| $B_O$ | Magnetic offset; $B_O = (B_{OP} + B_{RP}) / 2$ | | –1.5 | 0 | 1.5 | mT |
| **DRV5013BC: ±12 mT** | | | | | | |
| $B_{OP}$ | Operate point; see Figure 6-2 | $T_A$ = –40°C to $T_{A,MAX}$ (3) | 6 | 12 | 18 | mT |
| $B_{RP}$ | Release point; see Figure 6-2 | | –18 | –12 | –6 | |
| $B_{hys}$ | Hysteresis; $B_{hys} = (B_{OP} – B_{RP})$ | | | 24 | | |
| $B_O$ | Magnetic offset; $B_O = (B_{OP} + B_{RP}) / 2$ | | –1.5 | 0 | 1.5 | |

(1) 1 mT = 10 Gauss.
(2) Bandwidth describes the fastest changing magnetic field that can be detected and translated to the output.
(3) $T_{A, MAX}$ is 125°C for Q devices and 150°C for E devices (see Figure 8-1).


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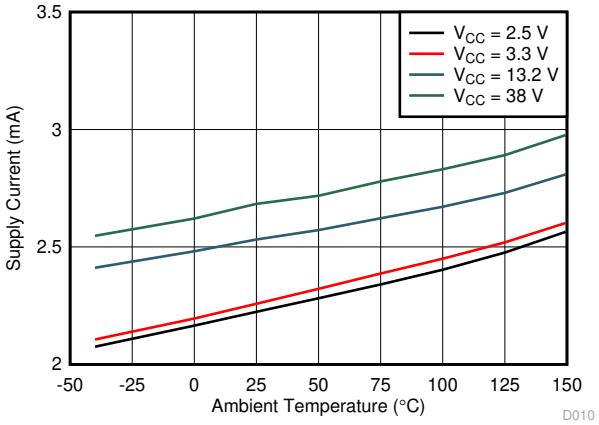
## 5.8 Typical Characteristics

$T_A$ > 125°C data is valid for devices with the "E" temperature range designator only, (see Device Nomenclature)



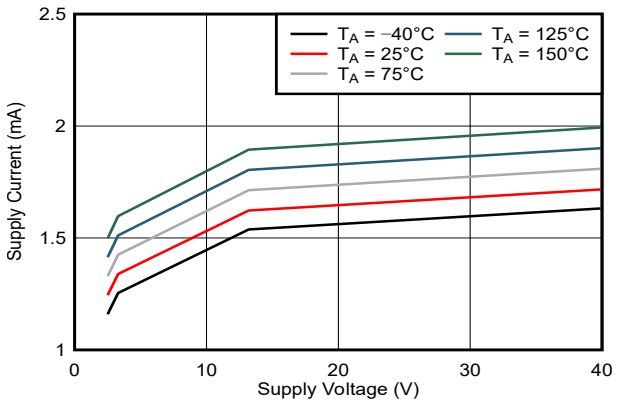

Versions: DRV5013AD, DRV5013AG, DRV5013BC, DRV5013FA

**Figure 5-1. $I_{CC}$ vs $V_{CC}$**



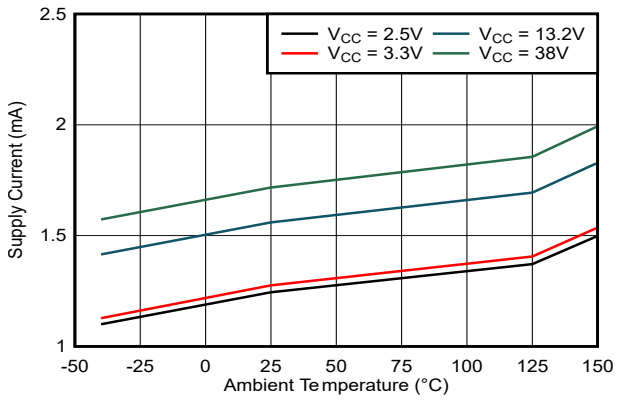

Versions: DRV5013AD, DRV5013AG, DRV5013BC, DRV5013FA

**Figure 5-2. $I_{CC}$ vs Temperature**



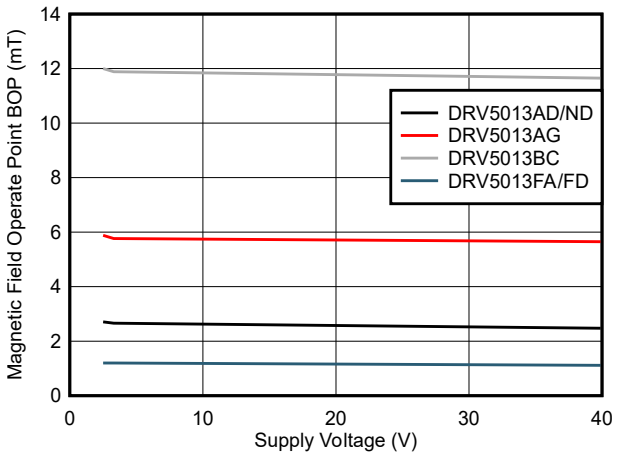

Version: DRV5013ND, DRV5013FD

**Figure 5-3. $I_{CC}$ vs $V_{CC}$**



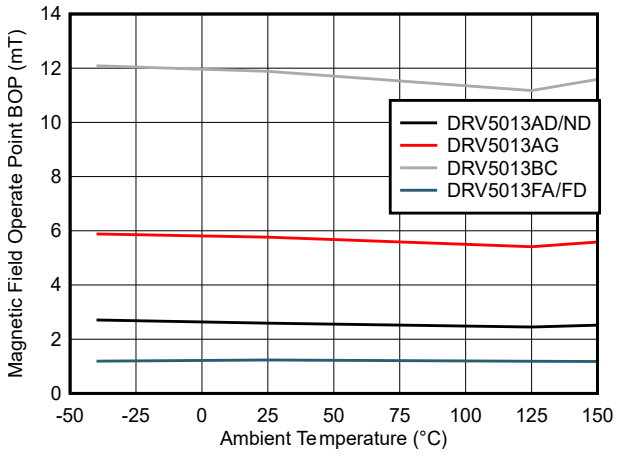

Version: DRV5013ND, DRV5013FD

**Figure 5-4. $I_{CC}$ vs Temperature**




$T_A$ = 25°C

**Figure 5-5. $B_{OP}$ vs $V_{CC}$**




$V_{CC}$ = 3.3 V

**Figure 5-6. $B_{OP}$ vs Temperature**

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## 5.8 Typical Characteristics (continued)

$T_A$ > 125°C data is valid for devices with the "E" temperature range designator only, (see Device Nomenclature)

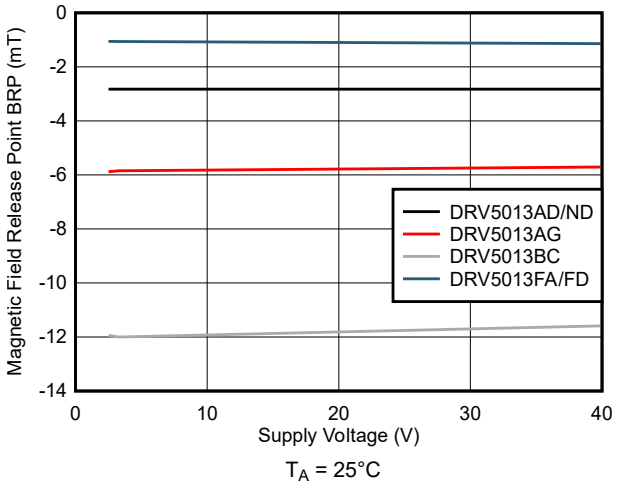



**Figure 5-7. $B_{RP}$ vs $V_{CC}$**

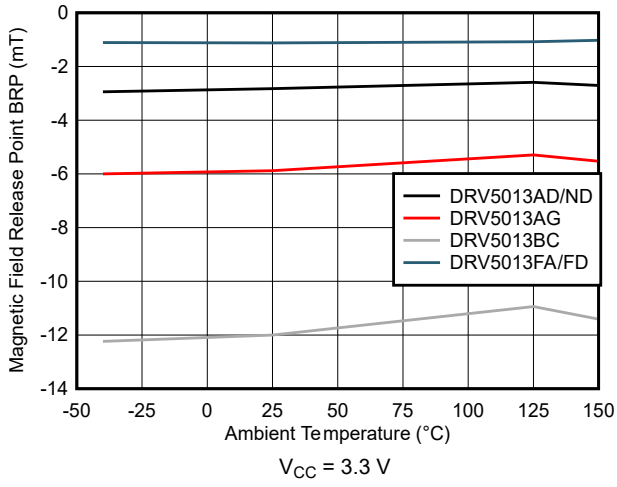



**Figure 5-8. $B_{RP}$ vs Temperature**

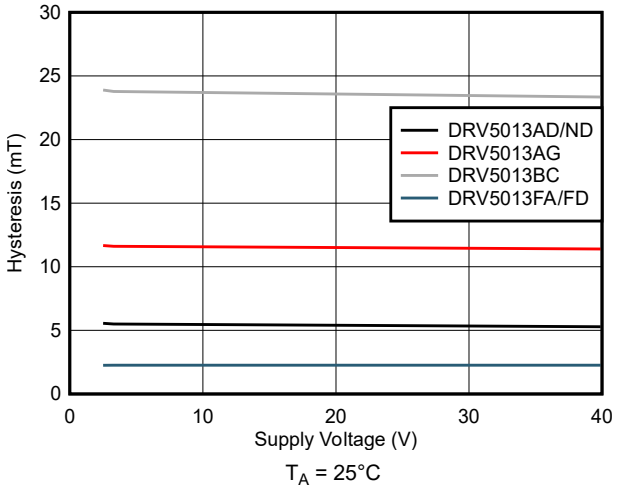



**Figure 5-9. Hysteresis vs $V_{CC}$**

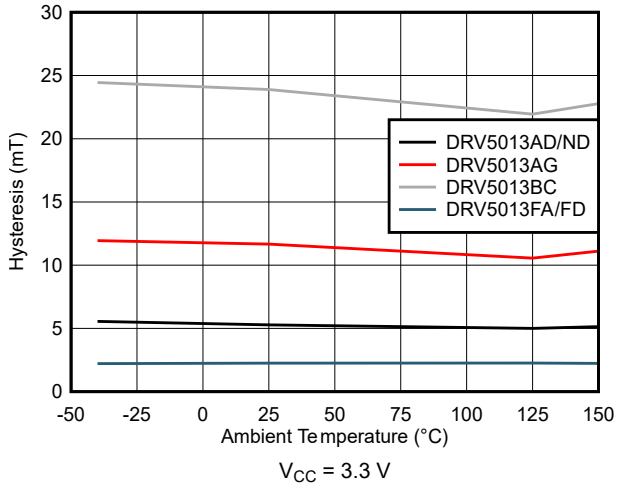



**Figure 5-10. Hysteresis vs Temperature**


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## 5.8 Typical Characteristics (continued)

$T_A$ > 125°C data is valid for devices with the "E" temperature range designator only, (see Device Nomenclature)

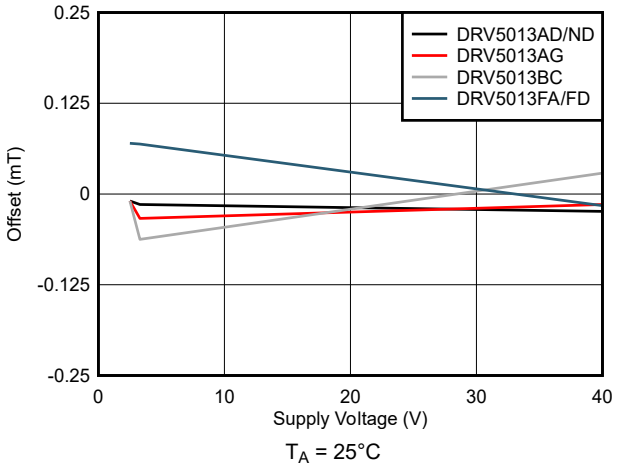



**Figure 5-11. Offset vs $V_{CC}$**

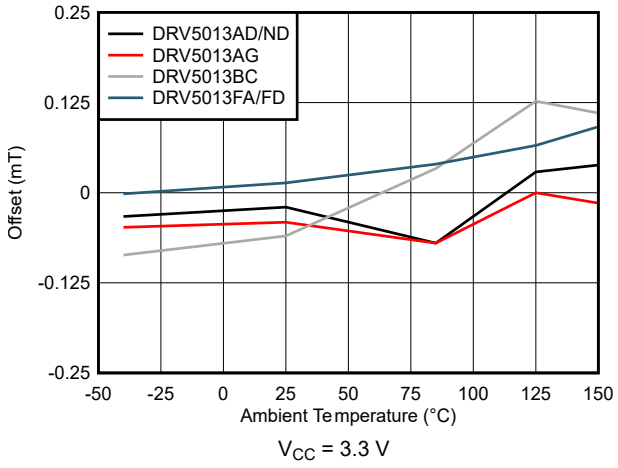



**Figure 5-12. Offset vs Temperature**

# 6 Detailed Description

## 6.1 Overview

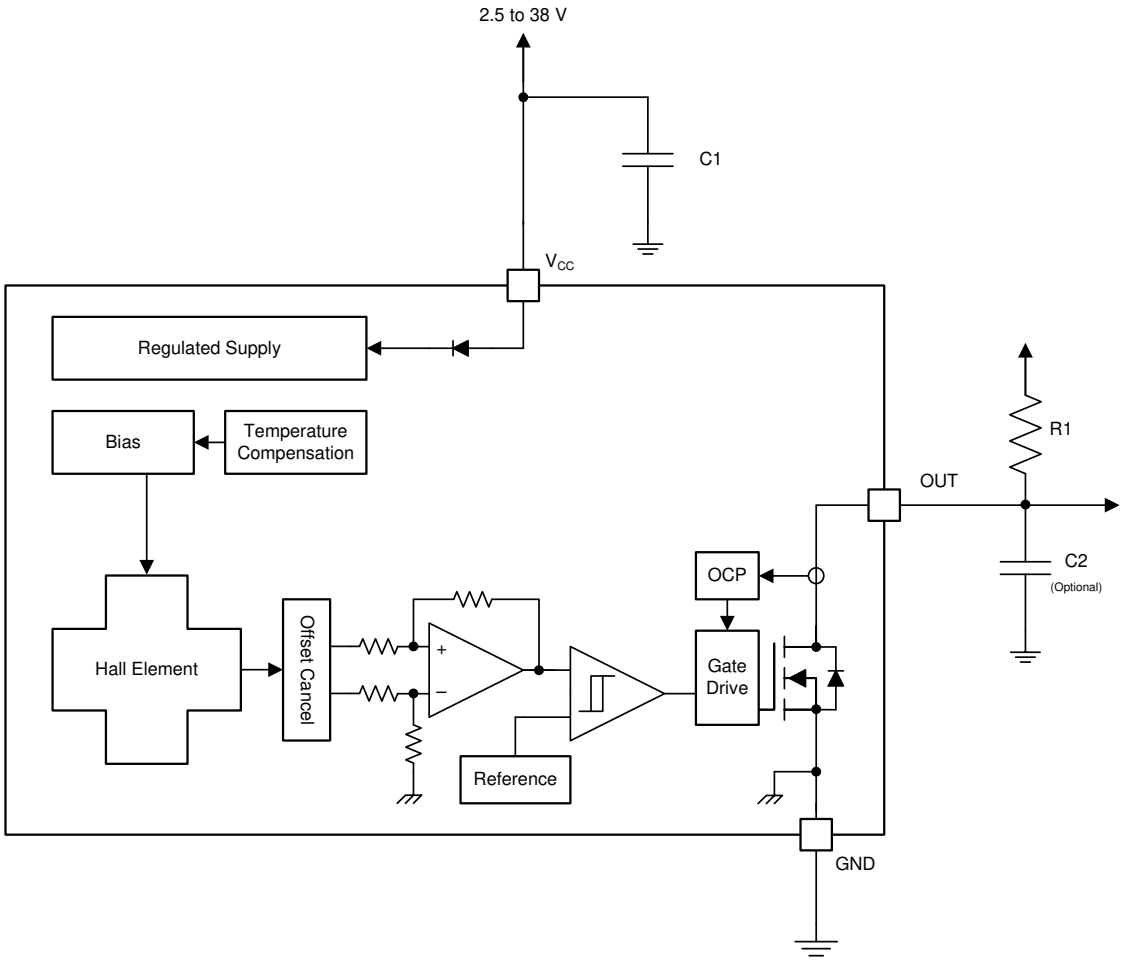
The DRV5013 device is a chopper-stabilized Hall sensor with a digital latched output for magnetic sensing applications. The DRV5013 device can be powered with a supply voltage ranging from 2.5 V to 38 V, and continuously withstand –22 V reverse-battery conditions. The DRV5013 device does not operate when –22 V to 2.4 V is applied to the $V_{CC}$ pin (with respect to the GND pin). In addition, the device can withstand voltages up to 40 V for transient durations.

The field polarity is defined as follows: a south pole near the marked side of the package induces a positive magnetic flux density on the sensor, while a north pole near the marked side of the package induces a negative magnetic flux density on the sensor.

The output state is dependent on the magnetic flux density perpendicular to the package. A positive magnetic flux density greater than the operate point threshold, $B_{OP}$, causes the output to pull low for the AD, AG, BC and FA device versions (release high for the inverted ND and FD device versions). A negative magnetic flux density less than the release point threshold, $B_{RP}$, causes the output to release high for the AD, AG, BC and FA device versions (pull low for the inverted ND and FD device versions). Hysteresis is included in between the operate point and the release point to help prevent magnetic noise from accidentally tripping the output.

An external pullup resistor is required on the OUT pin. The OUT pin can be pulled up to $V_{CC}$, or to a different voltage supply. This allows for easier interfacing with controller circuits.

## 6.2 Functional Block Diagram





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## 6.3 Feature Description

### 6.3.1 Field Direction Definition

Figure 6-1 illustrates that a positive magnetic flux density is defined as the presence of a south pole near the marked side of the package.

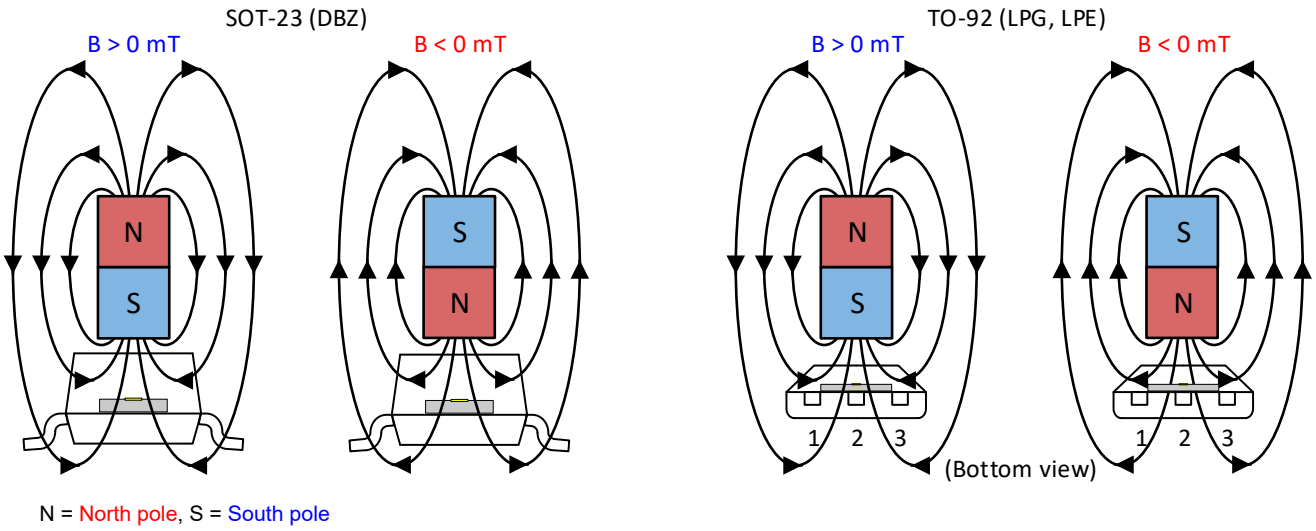



**Figure 6-1. Field Direction Definition**

### 6.3.2 Device Output

If the device is powered on with a magnetic flux density between $B_{RP}$ and $B_{OP}$, then the device output is indeterminate and can either be Hi-Z or Low. If the magnetic flux density is greater than $B_{OP}$, then the output is pulled low (released high for the inverted ND and FD versions). If the magnetic flux density is less than $B_{RP}$, then the output is released high according to the output reference voltage and pullup resistor (pulled low for the inverted ND and FD versions).

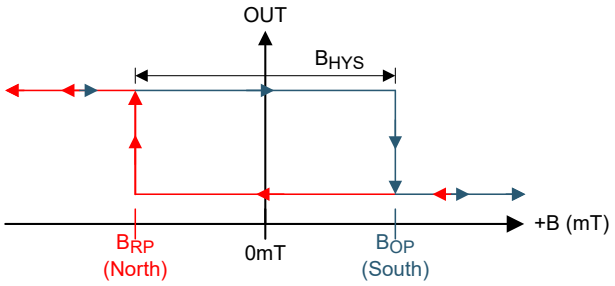



**Figure 6-2. Output State (FA, AD, AG, BC Versions)**

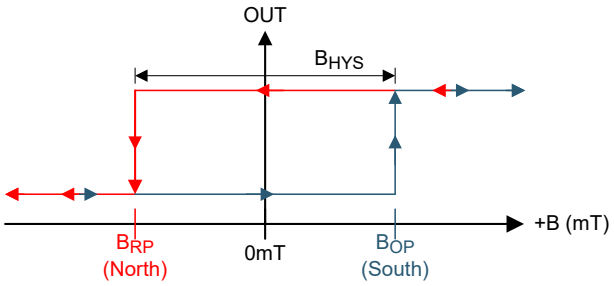



**Figure 6-3. Inverted Output State (ND, FD Versions)**

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### 6.3.3 Power-On Time

After applying $V_{CC}$ to the DRV5013 device, $t_{on}$ must elapse before the OUT pin is valid. During the power-up sequence, the output is Hi-Z. A pulse as shown in Figure 6-4 and Figure 6-5 occurs at the end of $t_{on}$. This pulse can allow the host processor to determine when the DRV5013 output is valid after start-up. The power-up sequence, including the pulse, is the same for all device output versions (AD, AG, BC, FA, FD, ND). Case 1, 2, 3 and 4 below show examples of valid outputs for the non-inverted output versions (AD, AG, BC, FA). In Case 1 (Figure 6-4) and Case 2 (Figure 6-5), the output is defined assuming a constant magnetic flux density B > $B_{OP}$ and B < $B_{RP}$.

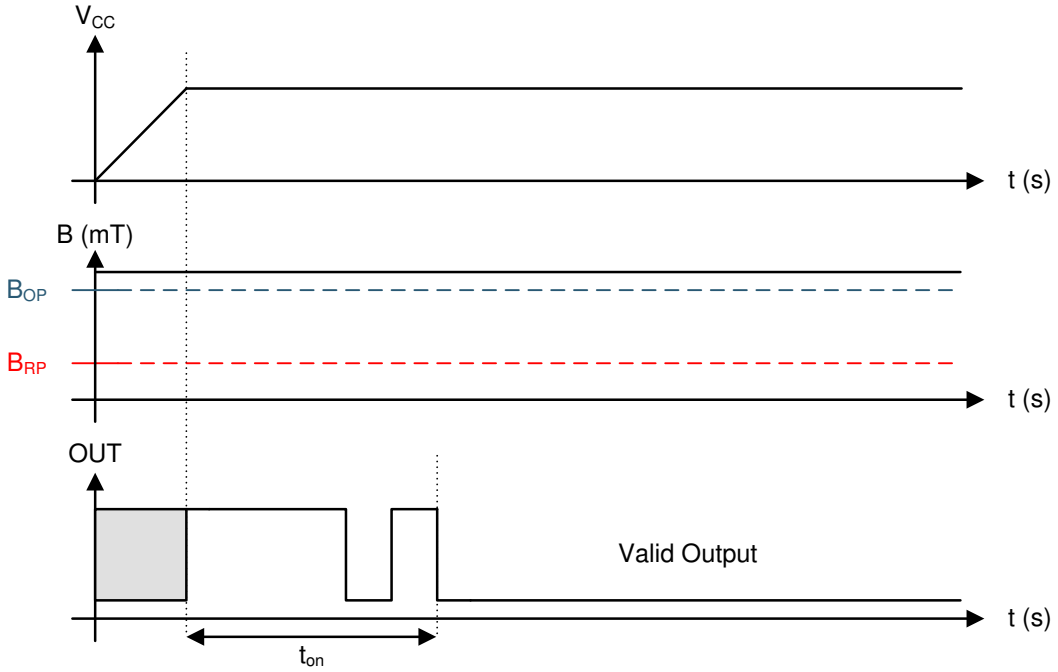



**Figure 6-4. Case 1: Power On When B > $B_{OP}$**

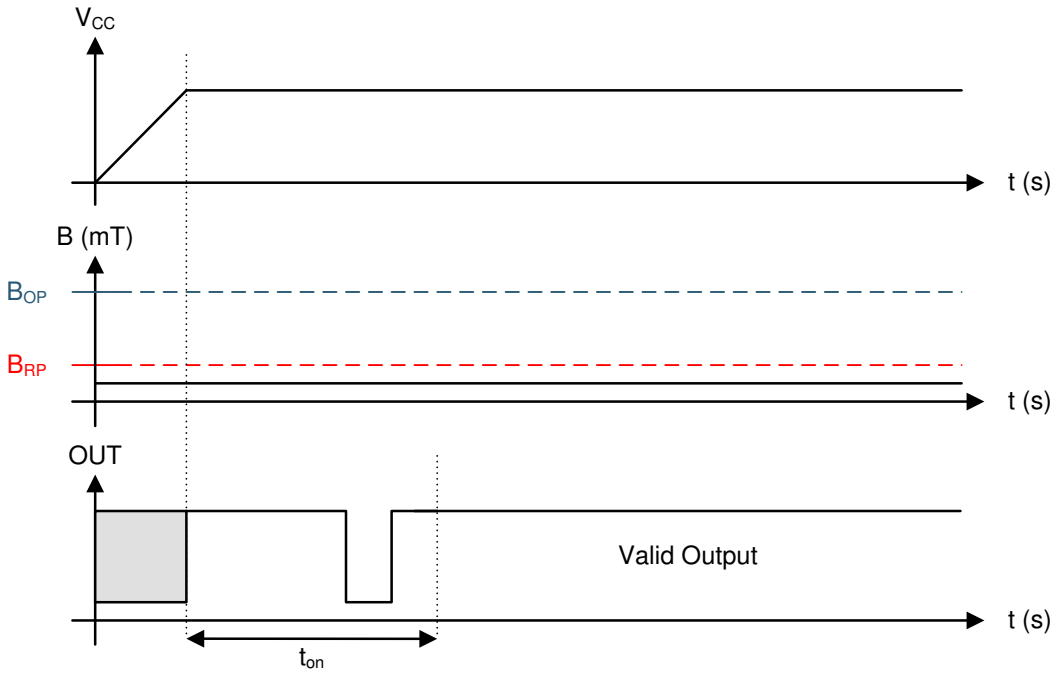



**Figure 6-5. Case 2: Power On When B < $B_{RP}$**


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If the device is powered on with the magnetic flux density $B_{RP}$ < B < $B_{OP}$, then the device output is indeterminate and can either be Hi-Z or pulled low. During the power-up sequence, the output is held Hi-Z until $t_{on}$ has elapsed. At the end of $t_{on}$, a pulse is given on the OUT pin to indicate that $t_{on}$ has elapsed. After $t_{on}$, if the magnetic flux density changes such that $B_{OP}$ < B, the output is released. Case 3 (Figure 6-6) and Case 4 (Figure 6-7) show examples of this behavior.

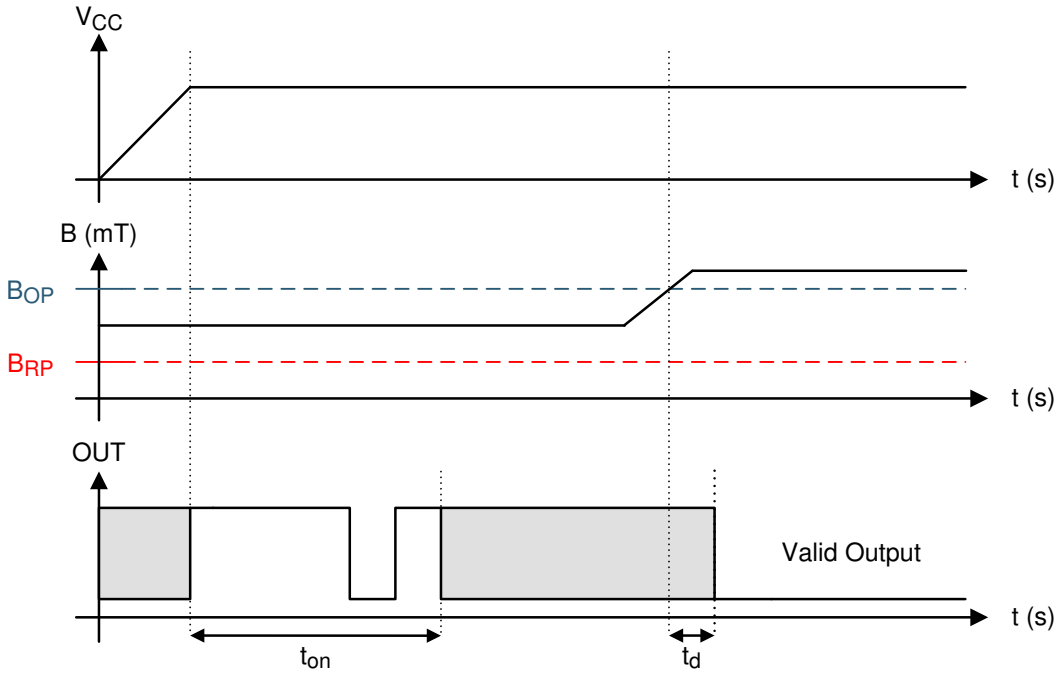



**Figure 6-6. Case 3: Power On When $B_{RP}$ < B < $B_{OP}$, Followed by B > $B_{OP}$**

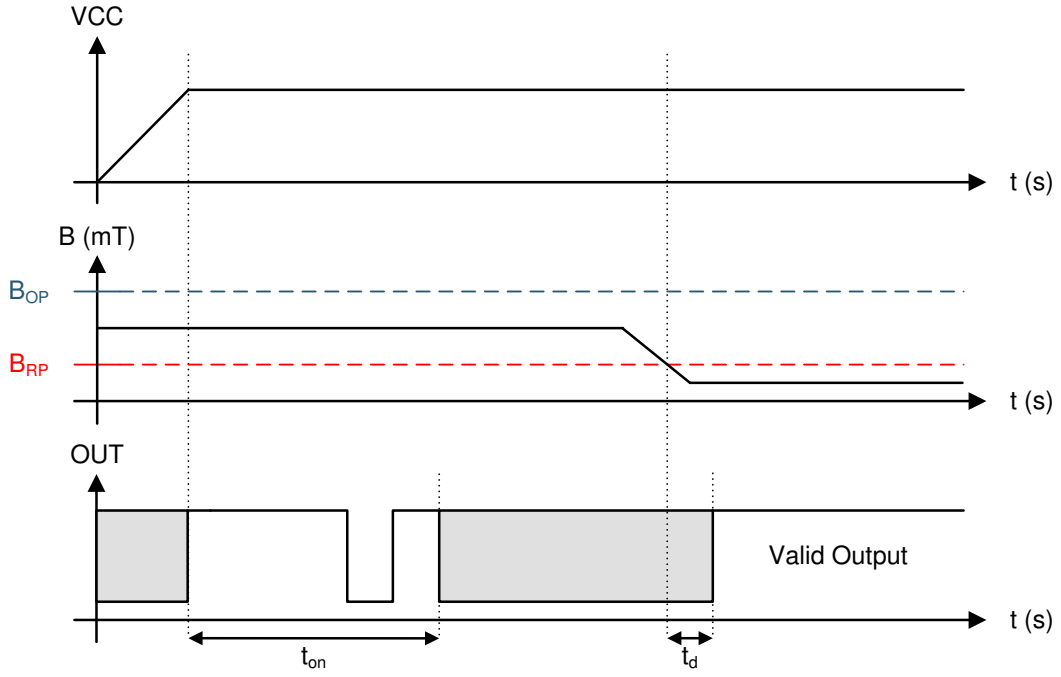



**Figure 6-7. Case 4: Power On When $B_{RP}$ < B < $B_{OP}$, Followed by B < $B_{RP}$**

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### 6.3.4 Output Stage

Figure 6-8 shows the DRV5013 open-drain NMOS output structure, rated to sink up to 30 mA of current. For proper operation, use Equation 1 to calculate the value of pullup resistor R1.

$$\frac{V_{ref}\ max}{30\ mA} \leq R1 \leq \frac{V_{ref}\ min}{100\ \mu A} \quad (1)$$

The size of R1 is a tradeoff between the OUT rise time and the current when OUT is pulled low. A lower current is generally better, however faster transitions and bandwidth require a smaller resistor for faster switching.

In addition, make sure that the value of R1 > 500 Ω so that the output driver can pull the OUT pin close to GND.

**Note**

$V_{ref}$ is not restricted to $V_{CC}$. The allowable voltage range of this pin is specified in the *Absolute Maximum Ratings*.

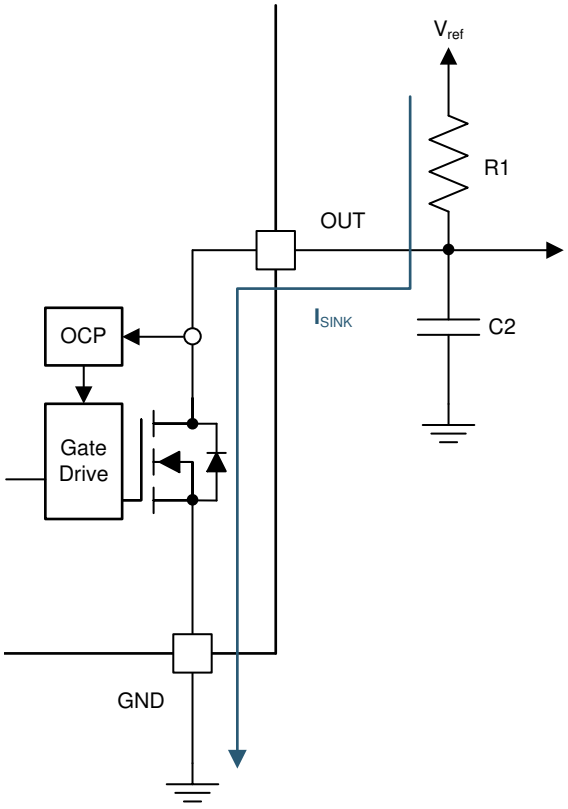



**Figure 6-8. NMOS Open-Drain Output**

Select a value for C2 based on the system bandwidth specifications as shown in Equation 2.

$$2 \times f_{BW}\ (Hz) < \frac{1}{2\pi \times R1 \times C2} \quad (2)$$

Most applications do not require this C2 filtering capacitor.


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### 6.3.5 Protection Circuits

The DRV5013 device is fully protected against overcurrent and reverse-supply conditions. Table 6-1 lists a summary of the protection circuits.

**Table 6-1. Protection Circuit Summary**

| FAULT | CONDITION | DEVICE | DESCRIPTION | RECOVERY |
|---|---|---|---|---|
| FET overload (OCP) | $I_{SINK} \geq I_{OCP}$ | Operating | Output current is clamped to $I_{OCP}$ | $I_O < I_{OCP}$ |
| Load dump | 38 V < $V_{CC}$ < 40 V | Operating | Device will operate for a transient duration | $V_{CC} \leq 38$ V |
| Reverse supply | –22 V < $V_{CC}$ < 0 V | Disabled | Device will survive this condition | $V_{CC} \geq 2.5$ V |

#### 6.3.5.1 Overcurrent Protection (OCP)

An analog current-limit circuit limits the current through the FET. The driver current is clamped to $I_{OCP}$. During this clamping, the $r_{DS(on)}$ of the output FET is increased from the nominal value.

#### 6.3.5.2 Load Dump Protection

The DRV5013 device operates at DC $V_{CC}$ conditions up to 38 V nominally, and can additionally withstand $V_{CC}$ = 40 V. No current-limiting series resistor is required for this protection.

#### 6.3.5.3 Reverse Supply Protection

The DRV5013 device is protected in the event that the $V_{CC}$ pin and the GND pin are reversed (up to –22 V).

**Note**

In a reverse supply condition, the OUT pin reverse-current must not exceed the ratings specified in the *Absolute Maximum Ratings*.

## 6.4 Device Functional Modes

The DRV5013 device is active only when $V_{CC}$ is between 2.5 V and 38 V.

When a reverse supply condition exists, the device is inactive.

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# 7 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 7.1 Application Information

The DRV5013 device is used in magnetic-field sensing applications.

## 7.2 Typical Applications

### *7.2.1 Standard Circuit*

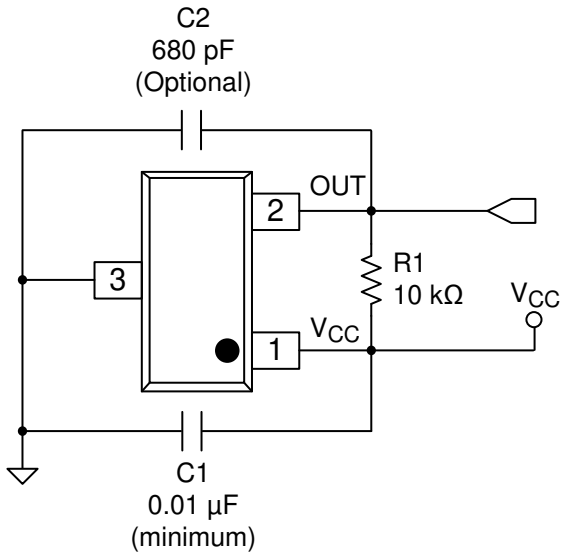



**Figure 7-1. Typical Application Circuit**

#### 7.2.1.1 Design Requirements

For this design example, use the parameters listed in Table 7-1 as the input parameters.

**Table 7-1. Design Parameters**

| DESIGN PARAMETER | REFERENCE | EXAMPLE VALUE |
|---|---|---|
| Supply voltage | $V_{CC}$ | 3.2 to 3.4 V |
| System bandwidth | $f_{BW}$ | 10 kHz |

#### 7.2.1.2 Detailed Design Procedure

**Table 7-2. External Components**

| COMPONENT | PIN 1 | PIN 2 | RECOMMENDED |
|---|---|---|---|
| C1 | $V_{CC}$ | GND | A 0.01-µF (minimum) ceramic capacitor rated for $V_{CC}$ |
| C2 | OUT | GND | **Optional**: Place a ceramic capacitor to GND |
| R1 | OUT | REF(1) | Requires a resistor pullup |

(1) REF is not a pin on the DRV5013 device, but a REF supply-voltage pullup is required for the OUT pin; the OUT pin may be pulled up to $V_{CC}$.


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#### 7.2.1.2.1 Configuration Example

In a 3.3-V system, 3.2 V ≤ $V_{ref}$ ≤ 3.4 V. Use Equation 3 to calculate the allowable range for R1.

$$\frac{V_{ref}\,\text{max}}{30\ \text{mA}} \leq R1 \leq \frac{V_{ref}\,\text{min}}{100\ \mu\text{A}} \tag{3}$$

For this design example, use Equation 4 to calculate the allowable range of R1.

$$\frac{3.4\ \text{V}}{30\ \text{mA}} \leq R1 \leq \frac{3.2\ \text{V}}{100\ \mu\text{A}} \tag{4}$$

Therefore:

$$113\ \Omega \leq R1 \leq 32\ \text{k}\Omega \tag{5}$$

After finding the allowable range of R1 (Equation 5), select a value between 500 Ω and 32 kΩ for R1.

Assuming a system bandwidth of 10 kHz, use Equation 6 to calculate the value of C2.

$$2 \times f_{BW}\ (\text{Hz}) < \frac{1}{2\pi \times R1 \times C2} \tag{6}$$

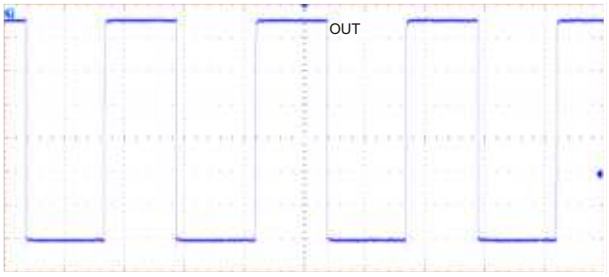
For this design example, use Equation 7 to calculate the value of C2.

$$2 \times 10\ \text{kHz} < \frac{1}{2\pi \times R1 \times C2} \tag{7}$$

An R1 value of 10 kΩ and a C2 value less than 820 pF satisfy the requirement for a 10-kHz system bandwidth.

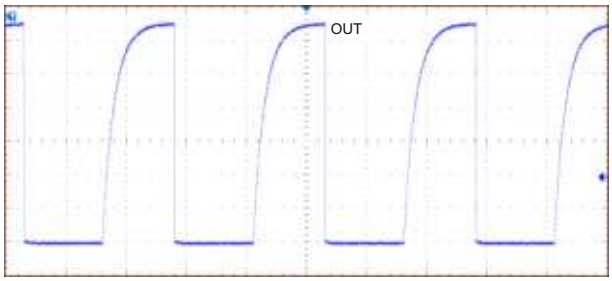
A selection of R1 = 10 kΩ and C2 = 680 pF would cause a low-pass filter with a corner frequency of 23.4 kHz.

### 7.2.1.3 Application Curves




R1 = 10 kΩ pull-up No C2

**Figure 7-2. 10-kHz Switching Magnetic Field**




R1 = 10-kΩ pull-up C2 = 680 pF

**Figure 7-3. 10-kHz Switching Magnetic Field**

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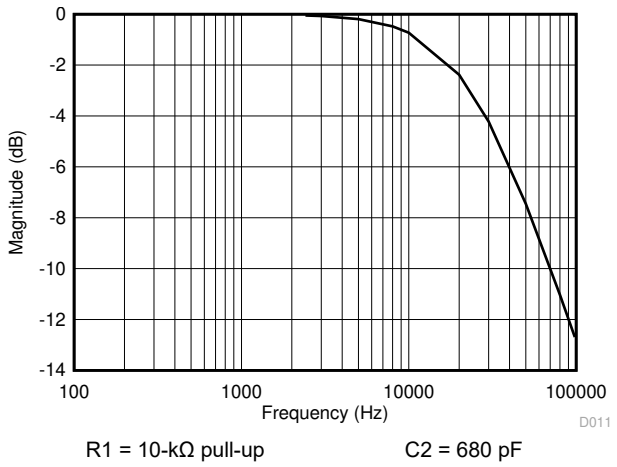



**Figure 7-4. Low-Pass Filtering**

### *7.2.2 Alternative Two-Wire Application*

For systems that require minimal wire count, the device output can be connected to $V_{CC}$ through a resistor, and the total supplied current can be sensed near the controller.

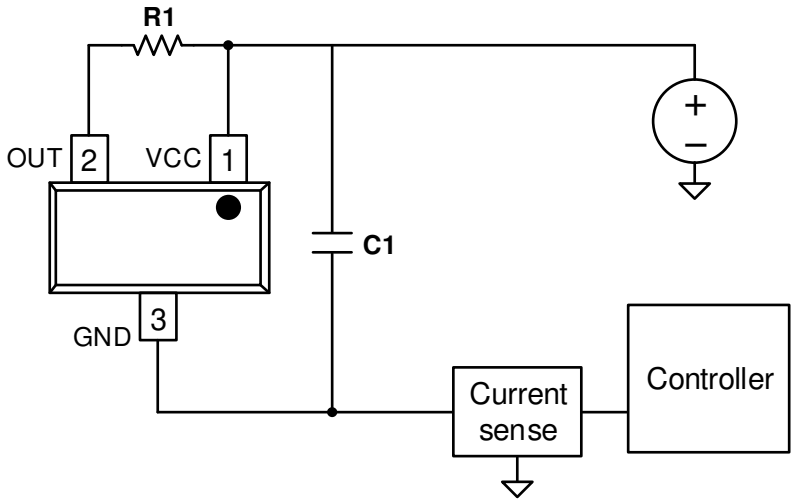



**Figure 7-5. 2-Wire Application**

Current can be sensed using a shunt resistor or other circuitry.

#### 7.2.2.1 Design Requirements

Table 7-3 lists the related design parameters.

**Table 7-3. Design Parameters**

| DESIGN PARAMETER | REFERENCE | EXAMPLE VALUE |
|---|---|---|
| Supply voltage | $V_{CC}$ | 12 V |
| OUT resistor | R1 | 1 kΩ |
| Bypass capacitor | C1 | 0.1 µF |
| Current when B < $B_{RP}$ | $I_{RELEASE}$ | About 3 mA |
| Current when B > $B_{OP}$ | $I_{OPERATE}$ | About 15 mA |


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#### 7.2.2.2 Detailed Design Procedure

When the open-drain output of the device is high-impedance, current through the path equals the $I_{CC}$ of the device (approximately 3 mA).

When the output pulls low, a parallel current path is added, equal to $V_{CC}$ / (R1 + $r_{DS(on)}$). Using 12 V and 1 kΩ, the parallel current is approximately 12 mA, making the total current approximately 15 mA.

The local bypass capacitor C1 should be at least 0.1 µF, and a larger value if there is high inductance in the power line interconnect.

## 7.3 Power Supply Recommendations

The DRV5013 device is designed to operate from an input voltage supply (VM) range between 2.5 V and 38 V. A 0.01-µF (minimum) ceramic capacitor rated for $V_{CC}$ must be placed as close to the DRV5013 device as possible. Larger values of the bypass capacitor may be needed to attenuate any significant high-frequency ripple and noise components generated by the power source. TI recommends limiting the supply voltage variation to less than 50 $mV_{PP}$.

## 7.4 Layout

### *7.4.1 Layout Guidelines*

The bypass capacitor should be placed near the DRV5013 device for efficient power delivery with minimal inductance. The external pullup resistor should be placed near the microcontroller input to provide the most stable voltage at the input; alternatively, an integrated pullup resistor within the GPIO of the microcontroller can be used.

Generally, using PCB copper planes underneath the DRV5013 device has no effect on magnetic flux, and does not interfere with device performance. This is because copper is not a ferromagnetic material. However, If nearby system components contain iron or nickel, they may redirect magnetic flux in unpredictable ways.

### *7.4.2 Layout Example*

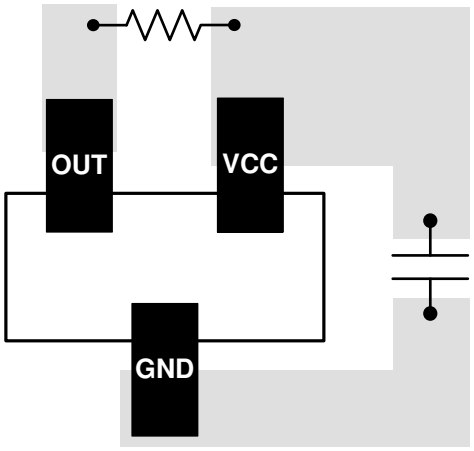



**Figure 7-6. DRV5013 Layout Example**

# 8 Device and Documentation Support

## 8.1 Device Support

### *8.1.1 Device Nomenclature*

Figure 8-1 shows a legend for reading the complete orderable part numbers for the DRV5013.

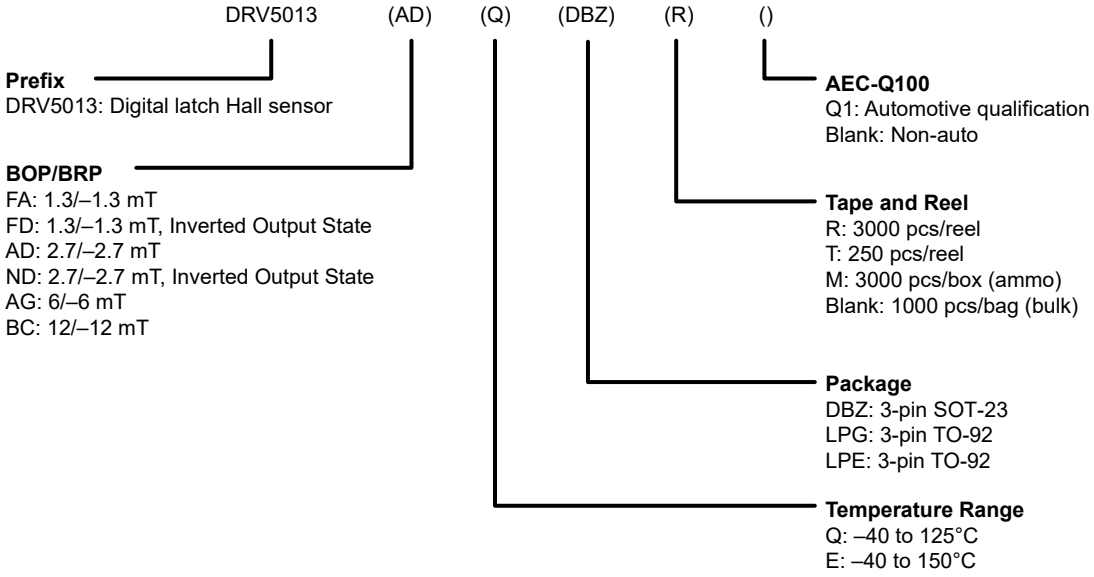



**Figure 8-1. Device Nomenclature**

### *8.1.2 Device Markings*

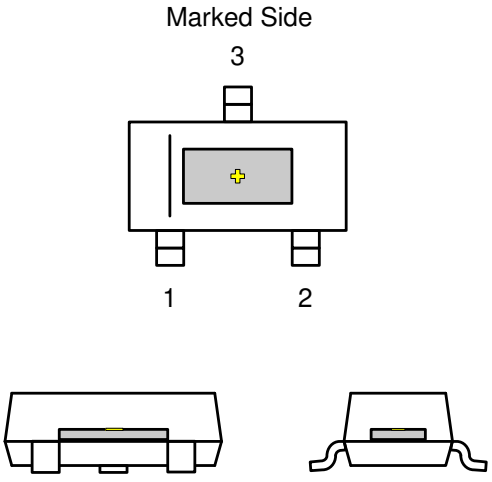



**Figure 8-2. SOT-23 (DBZ) Package**

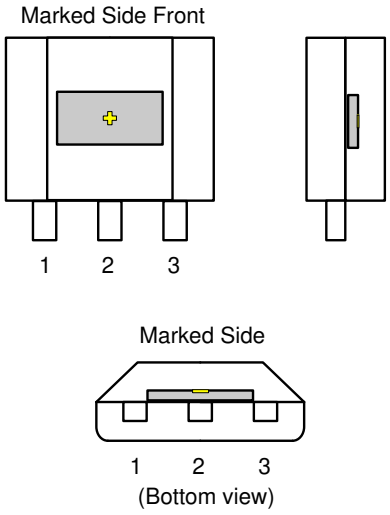



**Figure 8-3. TO-92 (LPG, LPE) Package**

## 8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.


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### 8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

### 8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

### 8.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 8.6 Glossary

| | |
|---|---|
| TI Glossary | This glossary lists and explains terms, acronyms, and definitions. |

## 9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision M (June 2024) to Revision N (July 2025)** — **Page**

- Added FD device information to the data sheet... 1
- Added graphs to the *Typical Characteristics* section to include the DRV5013FD device version... 7
- Updated text to describe switching of output device version FD ... 10
- Added text to the *Device Output* section to include the inverted output device version FD... 11
- Added text to the *Power-On Time* section concerning output device version FD... 12
- Updated legend to include inverted output device version FD... 20

**Changes from Revision L (February 2023) to Revision M (June 2024)** — **Page**

- Added ND device information to the data sheet... 1
- Changed the temperature condition statement in the *Typical Characteristics* section header... 7
- Added graphs to the *Typical Characteristics* section to include the DRV5013ND and DRV5013FA device versions... 7
- Added text to the *Overview* section to highlight the differences between the inverted and non-inverted output device versions... 10
- Changed the *Field Direction Definition* section ... 11
- Added text to the *Device Output* section to highlight the differences between the inverted and non-inverted output device versions... 11
- Added text to the *Power-On Time* section to highlight the differences between the inverted and non-inverted output device versions... 12

**Changes from Revision K (August 2019) to Revision L (February 2023)** — **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document... 1
- Changed table title from: Device Information to: Package Information... 1
- Moved the *Power Supply Recommendations* and *Layout* sections to the *Application and Implementation* section... 19

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**Changes from Revision J (June 2019) to Revision K (August 2019)** **Page**

- Changed $T_J$ to show existing range is for Q version device in the *Absolute Maximum Ratings* table....4
- Added E version for $T_J$ to the *Absolute Maximum Ratings* table....4
- Changed $T_A$ to show existing range is for Q version device in the *Recommended Operating Conditions* table 4
- Added E version for $T_A$ to the *Recommended Operating Conditions* table....4
- Changed $I_{CC}$ test condition for $T_A$ from 125 to $T_{A,MAX}$ to highlight the differences between the E and Q version devices....5
- Changed $r_{DS(on)}$ test condition for $T_A$ from 125 to $T_{A,MAX}$ to highlight the difference between the E and Q version devices....5
- Changed all test conditions for $T_A$ max from 125 to $T_{A,MAX}$ to highlight difference between the E and Q devices....6
- Added new condition statement to *Typical Characteristics* section....7
- Added data up to 150°C to Figure 1, Figure 2, Figure 4, Figure 6, Figure 8, and Figure 10....7

**Changes from Revision I (August 2018) to Revision J (June 2019)** **Page**

- Added TO-92 (LPE) package to data sheet .... 1

**Changes from Revision H (September 2016) to Revision I (August 2018)** **Page**

- Changed *Power Supply Recommendations* section .... 19

**Changes from Revision G (August 2016) to Revision H (September 2016)** **Page**

- Changed the power-on time for the FA version in the *Electrical Characteristics* table....5

**Changes from Revision F (May 2016) to Revision G (August 2016)** **Page**

- Changed the maximum $B_{OP}$ and the minimum $B_{RP}$ for the FA version in the Magnetic Characteristics table... 6
- Added the *Layout* section.... 19

**Changes from Revision E (February 2016) to Revision F (May 2016)** **Page**

- Revised preliminary limits for the FA version....6

**Changes from Revision D (December 2015) to Revision E (February 2016)** **Page**

- Added the FA device option....1
- Added the typical bandwidth value to *Magnetic Characteristics* table....6

**Changes from Revision C (September 2014) to Revision D (June 2015)** **Page**

- Corrected body size of SOT-23 package and SIP package name to TO-92 .... 1
- Added $B_{MAX}$ to *Absolute Maximum Ratings* .... 4
- Removed table note from junction temperature.... 4
- Added *Community Resources* .... 20
- Updated package tape and reel options for M and blank .... 20


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**Changes from Revision B (July 2014) to Revision C (September 2014)** **Page**

- Updated high sensitivity options ..... 1
- Changed the max operating junction temperature to 150°C..... 4
- Updated the output rise and fall time typical values and removed max values in *Switching Characteristics* .... 5
- Updated the values in *Magnetic Characteristics* ..... 6
- Updated all *Typical Characteristics* graphs ..... 7
- Updated Equation 4 ..... 17
- Updated *Device Nomenclature* ..... 20

**Changes from Revision A (March 2014) to Revision B (June 2014)** **Page**

- Changed $I_{OCP}$ MIN and MAX values from 20 and 40 to 15 and 45, respectively, in the *Electrical Characteristics* ..... 5
- Changed the MIN value for the ±2.3 mT $B_{RP}$ parameter from –4 to –5 in the *Magnetic Characteristics* table... 6
- Updated the hysteresis values for each device option in the *Magnetic Characteristics* table..... 6

**Changes from Revision * (March 2014) to Revision A (March 2014)** **Page**

- Changed all references to Hall IC to Hall Effect Sensor ..... 1
- Changed *RPM Meter* to *Tachometers* in the *Applications* list ..... 1
- Changed the power-on value from 50 to 35 µs in the *Features* list ..... 1
- Changed the type of the OUT terminal from OD to Output in the *Pin Functions* table ..... 3
- Deleted Output pin current and changed $V_{CC}$max to $V_{CC}$ after the voltage ramp rate for the supply voltage.... 4
- Changed $R_O$ to R1 in the test conditions for $t_r$ and $t_f$ in the *Switching Characteristics* table..... 5
- Added the bandwidth parameter to *Magnetic Characteristics* table..... 6
- Changed the MIN value for the ±2.3 mt $B_{RP}$ parameter from +2.3 to –2.3 in the *Magnetic Characteristics* table ..... 6
- Deleted condition statement from the *Typical Characteristics* and changed all $T_J$ to $T_A$ in the graph conditions ..... 7
- Deleted *Number* from the Power-On Time case names; added conditions to captions of case timing diagrams ..... 12
- Added the R1 tradeoff and lower current text after the equation in the *Output Stage* section ..... 14
- Added the C2 not required for most applications text after the second equation in the *Output Stage* section. 14
- Changed $I_O$ to $I_{SINK}$ in condition statement of FET overload fault condition in *Reverse Supply Protection* section..... 15

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| DRV5013ADQDBZR | Active | Production | SOT-23 (DBZ) \| 3 | 3000 \| LARGE T&R | Yes | NIPDAUAG \| SN | Level-1-260C-UNLIM | -40 to 125 | (+NLAD, 13AD, 1J52) |
| DRV5013ADQDBZR.A | Active | Production | SOT-23 (DBZ) \| 3 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | (+NLAD, 13AD, 1J52) |
| DRV5013ADQDBZT | Obsolete | Production | SOT-23 (DBZ) \| 3 | - | - | Call TI | Call TI | -40 to 125 | (+NLAD, 13AD, 1J52) |
| DRV5013ADQLPG | Active | Production | TO-92 (LPG) \| 3 | 1000 \| BULK | Yes | SN | N/A for Pkg Type | -40 to 125 | +NLAD |
| DRV5013ADQLPG.A | Active | Production | TO-92 (LPG) \| 3 | 1000 \| BULK | Yes | SN | N/A for Pkg Type | -40 to 125 | +NLAD |
| DRV5013ADQLPGM | Active | Production | TO-92 (LPG) \| 3 | 3000 \| AMMO | Yes | SN | N/A for Pkg Type | -40 to 125 | +NLAD |
| DRV5013ADQLPGM.A | Active | Production | TO-92 (LPG) \| 3 | 3000 \| AMMO | Yes | SN | N/A for Pkg Type | -40 to 125 | +NLAD |
| DRV5013AGQDBZR | Active | Production | SOT-23 (DBZ) \| 3 | 3000 \| LARGE T&R | Yes | NIPDAUAG \| SN | Level-1-260C-UNLIM | -40 to 125 | (+NLAG, 13AG, 1IW2) |
| DRV5013AGQDBZR.A | Active | Production | SOT-23 (DBZ) \| 3 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | (+NLAG, 13AG, 1IW2) |
| DRV5013AGQLPG | Active | Production | TO-92 (LPG) \| 3 | 1000 \| BULK | Yes | SN | N/A for Pkg Type | -40 to 125 | +NLAG |
| DRV5013AGQLPG.A | Active | Production | TO-92 (LPG) \| 3 | 1000 \| BULK | Yes | SN | N/A for Pkg Type | -40 to 125 | +NLAG |
| DRV5013AGQLPGM | Active | Production | TO-92 (LPG) \| 3 | 3000 \| AMMO | Yes | SN | N/A for Pkg Type | -40 to 125 | +NLAG |
| DRV5013AGQLPGM.A | Active | Production | TO-92 (LPG) \| 3 | 3000 \| AMMO | Yes | SN | N/A for Pkg Type | -40 to 125 | +NLAG |
| DRV5013BCELPE | Active | Production | TO-92 (LPE) \| 3 | 1000 \| BULK | Yes | SN | N/A for Pkg Type | -40 to 150 | 1UVJ |
| DRV5013BCELPE.A | Active | Production | TO-92 (LPE) \| 3 | 1000 \| BULK | Yes | SN | N/A for Pkg Type | -40 to 150 | 1UVJ |
| DRV5013BCELPEM | Active | Production | TO-92 (LPE) \| 3 | 3000 \| LARGE T&R | Yes | SN | N/A for Pkg Type | -40 to 150 | 1UVJ |
| DRV5013BCELPEM.A | Active | Production | TO-92 (LPE) \| 3 | 3000 \| LARGE T&R | Yes | SN | N/A for Pkg Type | -40 to 150 | 1UVJ |
| DRV5013BCQDBZR | Active | Production | SOT-23 (DBZ) \| 3 | 3000 \| LARGE T&R | Yes | NIPDAUAG \| SN | Level-1-260C-UNLIM | -40 to 125 | (+NLBC, 1IX2) |
| DRV5013BCQDBZR.A | Active | Production | SOT-23 (DBZ) \| 3 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | (+NLBC, 1IX2) |
| DRV5013BCQDBZT | Obsolete | Production | SOT-23 (DBZ) \| 3 | - | - | Call TI | Call TI | -40 to 125 | (+NLBC, 1IX2) |
| DRV5013BCQLPG | Active | Production | TO-92 (LPG) \| 3 | 1000 \| BULK | Yes | SN | N/A for Pkg Type | -40 to 125 | +NLBC |
| DRV5013BCQLPG.A | Active | Production | TO-92 (LPG) \| 3 | 1000 \| BULK | Yes | SN | N/A for Pkg Type | -40 to 125 | +NLBC |
| DRV5013BCQLPGM | Active | Production | TO-92 (LPG) \| 3 | 3000 \| AMMO | Yes | SN | N/A for Pkg Type | -40 to 125 | +NLBC |
| DRV5013BCQLPGM.A | Active | Production | TO-92 (LPG) \| 3 | 3000 \| AMMO | Yes | SN | N/A for Pkg Type | -40 to 125 | +NLBC |
| DRV5013FAQDBZR | Active | Production | SOT-23 (DBZ) \| 3 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | (+NLFA, 1IZ2) |

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| DRV5013FAQDBZR.A | Active | Production | SOT-23 (DBZ) \| 3 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | (+NLFA, 1IZ2) |
| DRV5013FDQDBZR | Active | Production | SOT-23 (DBZ) \| 3 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 150 | 13FD |
| DRV5013NDQDBZR | Active | Production | SOT-23 (DBZ) \| 3 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | 13ND |
| DRV5013NDQDBZR.A | Active | Production | SOT-23 (DBZ) \| 3 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | 13ND |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**OTHER QUALIFIED VERSIONS OF DRV5013 :**

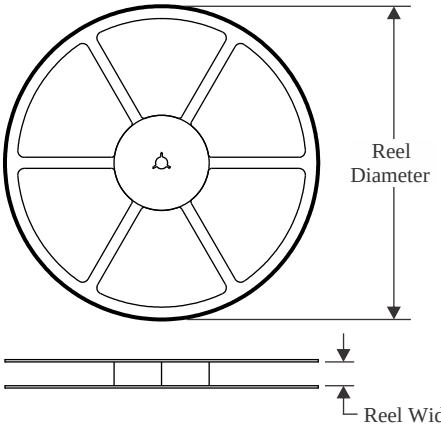
- Automotive : DRV5013-Q1

NOTE: Qualified Version Definitions:

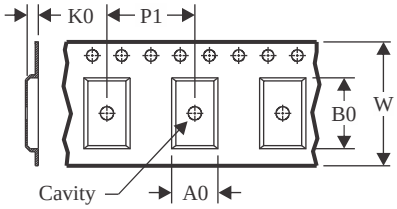
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

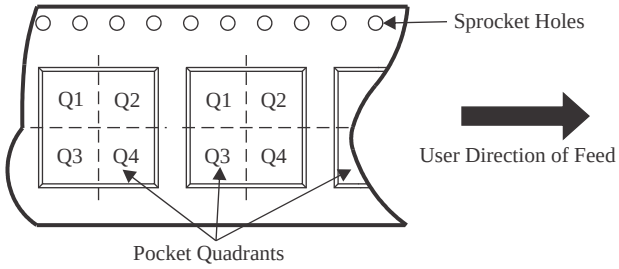



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

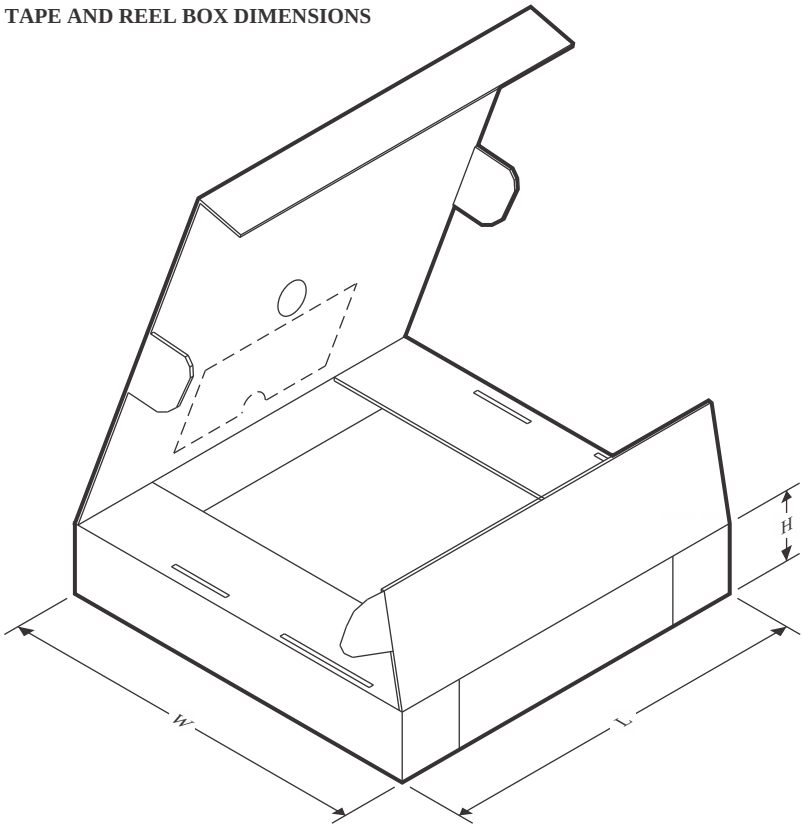
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DRV5013ADQDBZR | SOT-23 | DBZ | 3 | 3000 | 178.0 | 9.0 | 3.15 | 2.77 | 1.22 | 4.0 | 8.0 | Q3 |
| DRV5013AGQDBZR | SOT-23 | DBZ | 3 | 3000 | 180.0 | 8.4 | 3.2 | 2.85 | 1.3 | 4.0 | 8.0 | Q3 |
| DRV5013AGQDBZR | SOT-23 | DBZ | 3 | 3000 | 178.0 | 9.0 | 3.15 | 2.77 | 1.22 | 4.0 | 8.0 | Q3 |
| DRV5013BCQDBZR | SOT-23 | DBZ | 3 | 3000 | 178.0 | 9.0 | 3.15 | 2.77 | 1.22 | 4.0 | 8.0 | Q3 |
| DRV5013BCQDBZR | SOT-23 | DBZ | 3 | 3000 | 180.0 | 8.4 | 3.2 | 2.85 | 1.3 | 4.0 | 8.0 | Q3 |
| DRV5013FAQDBZR | SOT-23 | DBZ | 3 | 3000 | 180.0 | 8.4 | 3.15 | 2.77 | 1.22 | 4.0 | 8.0 | Q3 |
| DRV5013FAQDBZR | SOT-23 | DBZ | 3 | 3000 | 180.0 | 8.4 | 3.2 | 2.85 | 1.3 | 4.0 | 8.0 | Q3 |
| DRV5013FDQDBZR | SOT-23 | DBZ | 3 | 3000 | 180.0 | 8.4 | 2.9 | 3.35 | 1.35 | 4.0 | 8.0 | Q3 |
| DRV5013NDQDBZR | SOT-23 | DBZ | 3 | 3000 | 180.0 | 8.4 | 3.2 | 2.85 | 1.3 | 4.0 | 8.0 | Q3 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

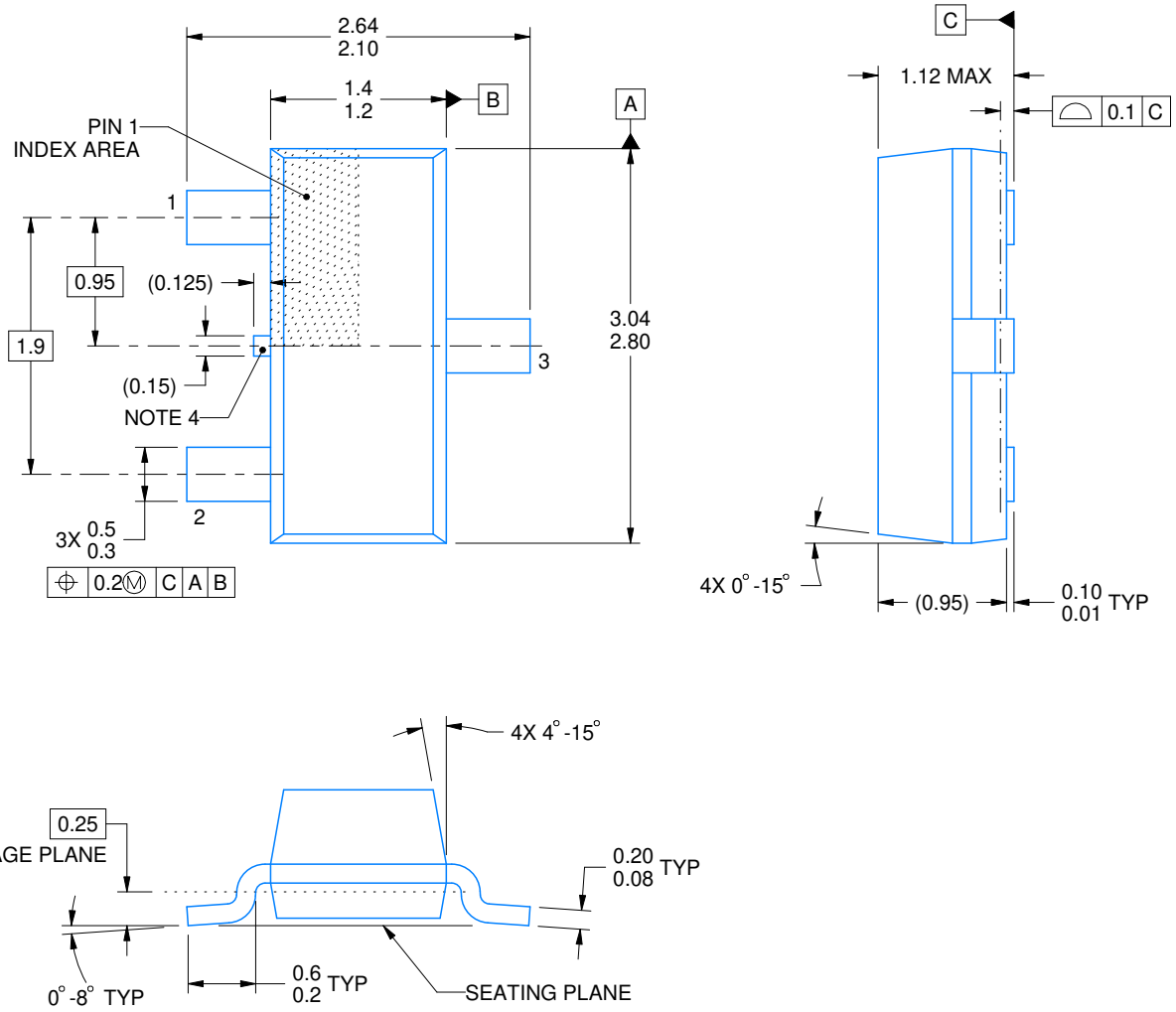
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| DRV5013ADQDBZR | SOT-23 | DBZ | 3 | 3000 | 180.0 | 180.0 | 18.0 |
| DRV5013AGQDBZR | SOT-23 | DBZ | 3 | 3000 | 210.0 | 185.0 | 35.0 |
| DRV5013AGQDBZR | SOT-23 | DBZ | 3 | 3000 | 180.0 | 180.0 | 18.0 |
| DRV5013BCQDBZR | SOT-23 | DBZ | 3 | 3000 | 180.0 | 180.0 | 18.0 |
| DRV5013BCQDBZR | SOT-23 | DBZ | 3 | 3000 | 210.0 | 185.0 | 35.0 |
| DRV5013FAQDBZR | SOT-23 | DBZ | 3 | 3000 | 202.0 | 201.0 | 28.0 |
| DRV5013FAQDBZR | SOT-23 | DBZ | 3 | 3000 | 210.0 | 185.0 | 35.0 |
| DRV5013FDQDBZR | SOT-23 | DBZ | 3 | 3000 | 210.0 | 185.0 | 35.0 |
| DRV5013NDQDBZR | SOT-23 | DBZ | 3 | 3000 | 210.0 | 185.0 | 35.0 |

# PACKAGE OUTLINE

## DBZ0003A

## SOT-23 - 1.12 mm max height

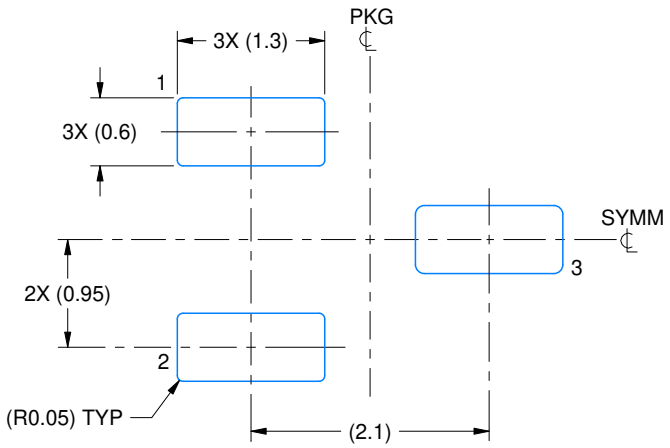
SMALL OUTLINE TRANSISTOR



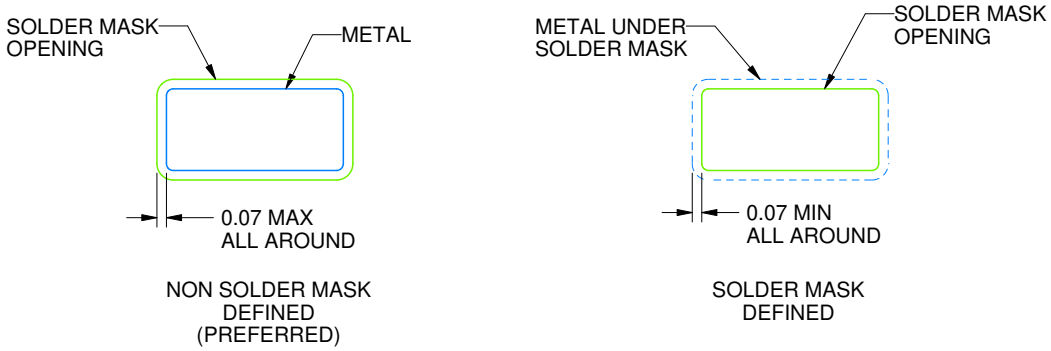

4214838/F 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-236, except minimum foot length.
4. Support pin may differ or may not be present.
5. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side




LAND PATTERN EXAMPLE
SCALE:15X

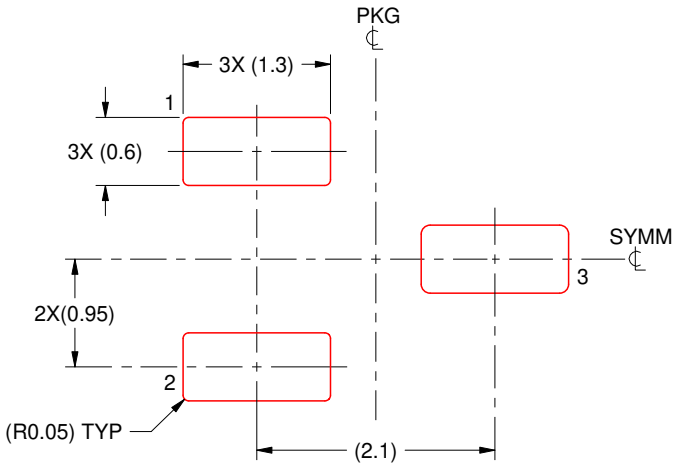



SOLDER MASK DETAILS

4214838/F 08/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4214838/F 08/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

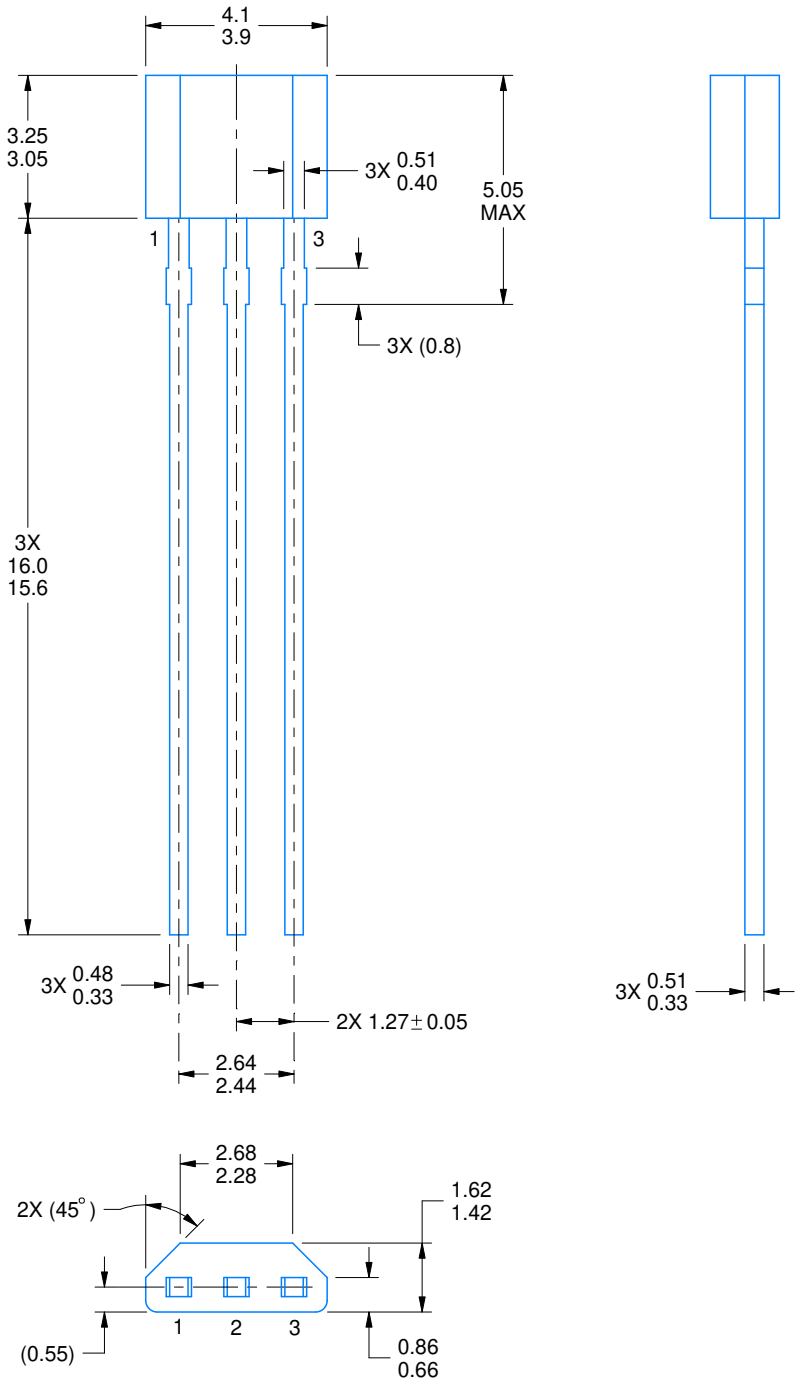


# PACKAGE OUTLINE

## LPE0003A

## TO-92 - 5.05 mm max height

TRANSISTOR OUTLINE




4224358/A 06/2018

NOTES:

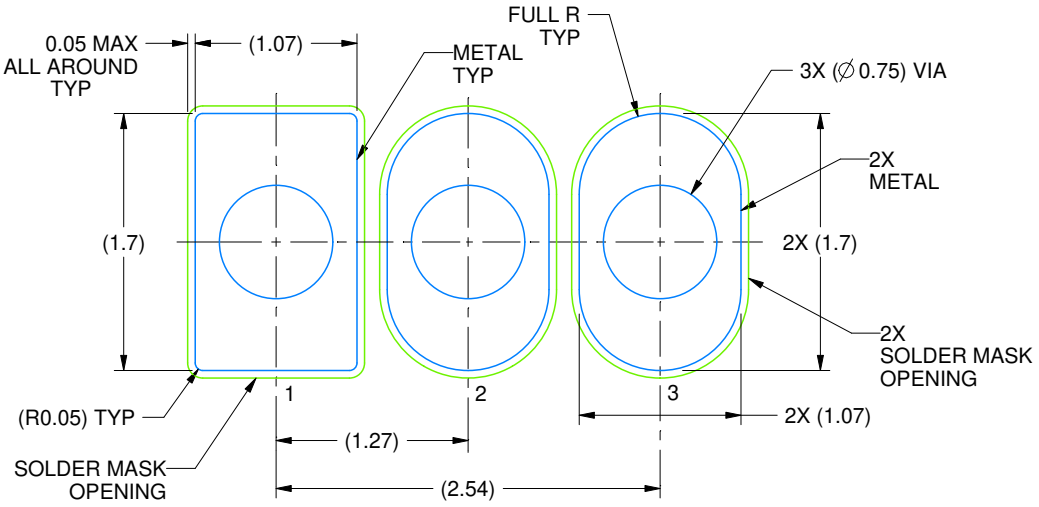
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

## LPE0003A

### TO-92 - 5.05 mm max height

TRANSISTOR OUTLINE




LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE:20X

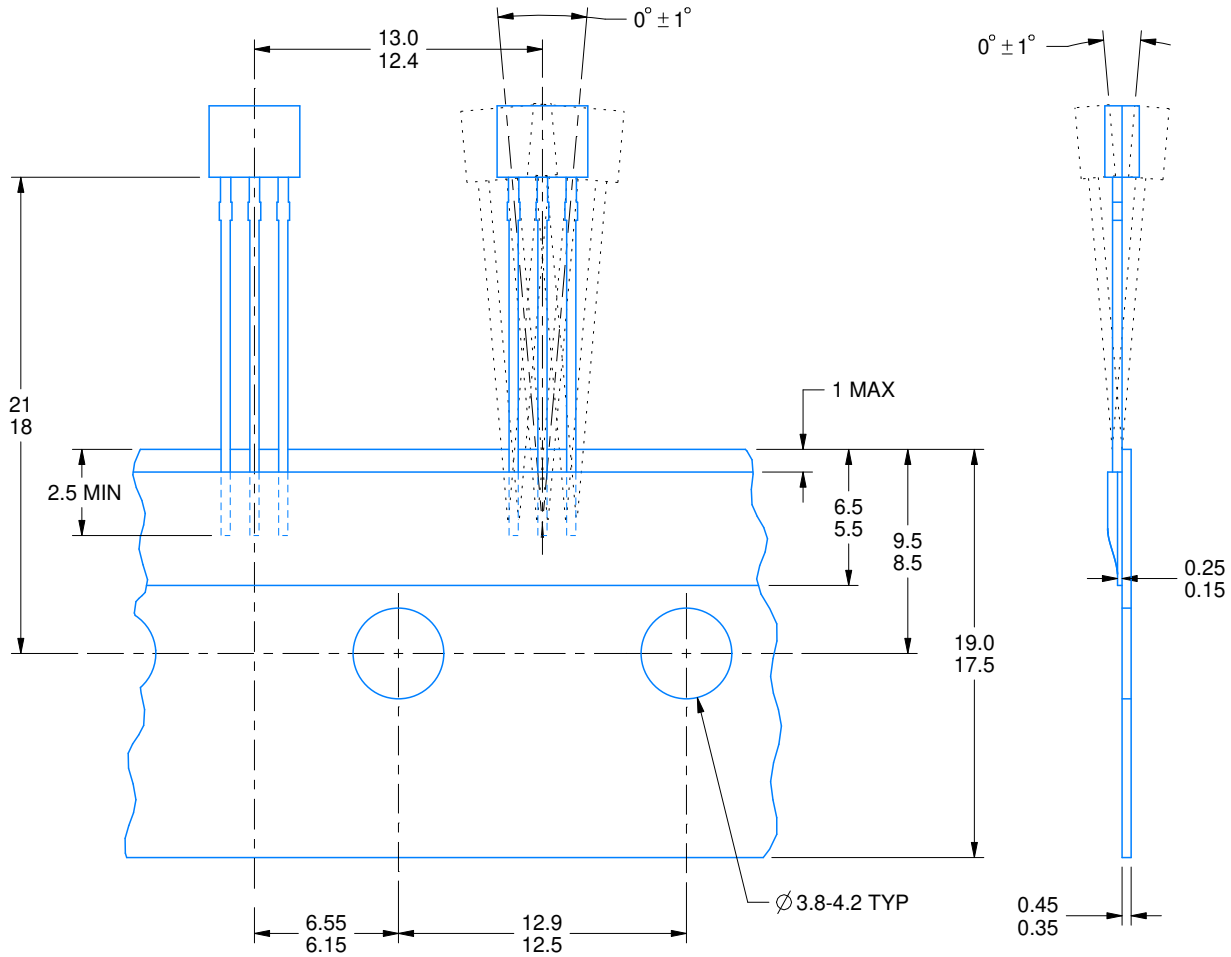
4224358/A 06/2018

# TAPE SPECIFICATIONS

## LPE0003A

## TO-92 - 5.05 mm max height

TRANSISTOR OUTLINE




4224358/A 06/2018

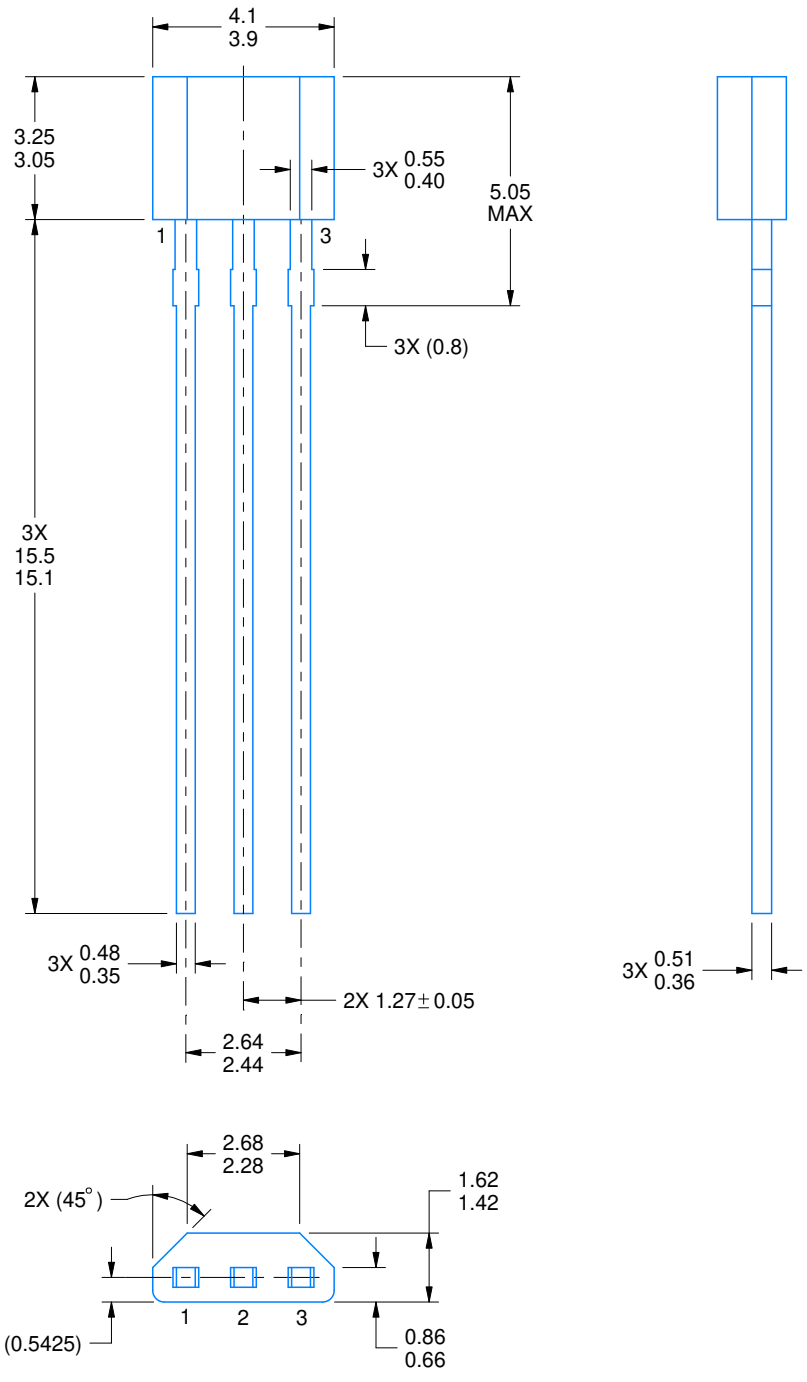


# PACKAGE OUTLINE

## LPG0003A

## TO-92 - 5.05 mm max height

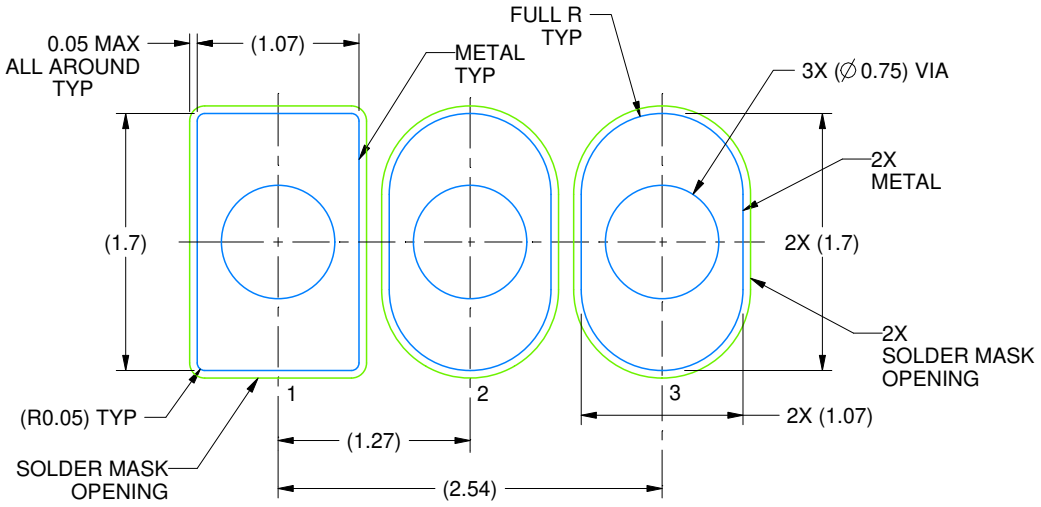
TRANSISTOR OUTLINE




4221343/C 01/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



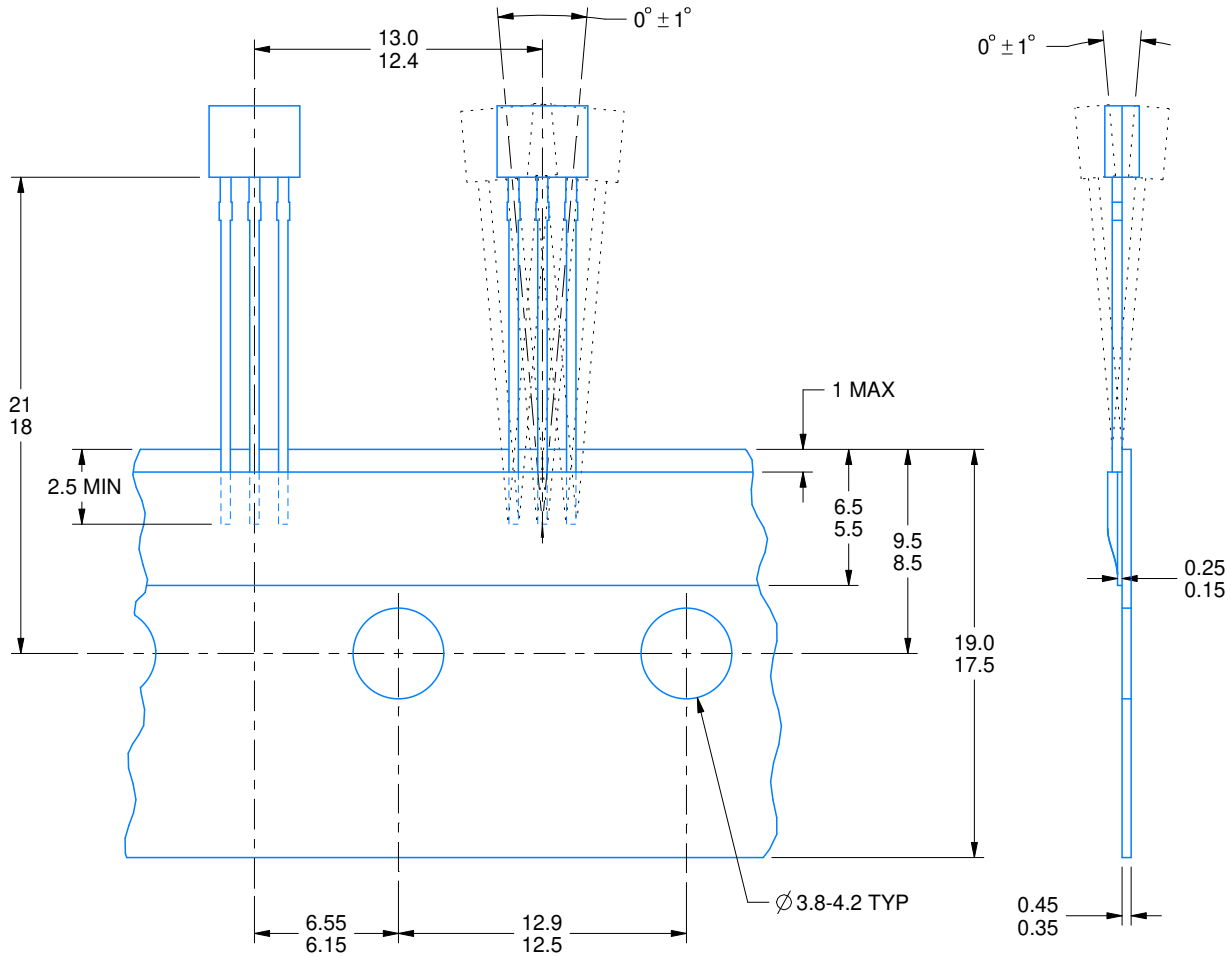

LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE:20X

4221343/C 01/2018

# LPG0003A

## TO-92 - 5.05 mm max height

TRANSISTOR OUTLINE




4221343/C 01/2018

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