DRV8210 11-V H-Bridge Motor Driver with PWM, PH/EN, and Half-Bridge Control Interfaces and Low-Power Sleep Mode

1 Features

- N-channel H-bridge motor driver
  - MOSFET on-resistance: HS + LS 1 Ω
  - Drives one bidirectional brushed DC motor
  - Two unidirectional brushed DC motors
  - One single- or dual-coil latching relay
  - Push-pull and bistable solenoids
  - Other resistive, inductive, or LED loads
- 1.65-V to 11-V operating supply voltage range
- High output current capability:
  - Full-bridge: 1.76-A peak
  - Half-bridge: 1.76-A peak per output
  - Parallel half-bridge: 3.52-A peak
- Multiple interfaces for flexibility and reduced GPIO
- Standard PWM Interface (IN1/IN2)
- Supports 1.8-V, 3.3-V, and 5-V logic inputs
- Ultra low-power sleep mode
  - <84.5 nA @ V_{VM} = 5 V, V_{VCC} = 3.3 V, T_J = 25°C
  - Timed autosleep mode to reduce GPIO
- Protection features
  - Undervoltage lockout (UVLO)
  - Overcurrent protection (OCP)
  - Thermal shutdown (TSD)
- Family of devices. See Device Comparison for details.
  - DRV8210: 1.65-11 V, 1 Ω, multiple interfaces
  - DRV8210P: Sleep pin, PWM interface
  - DRV8212: 1.65-11 V, 280 mΩ, multiple interfaces
  - DRV8212P: Sleep pin, PWM interface
  - DRV8220: 4.5-18 V, 1 Ω, multiple interfaces

2 Applications

- Brushed DC motor, solenoid, & relay driving
- Water, gas, & electricity meters
- IP network camera IR cut filter
- Video doorbell
- Machine vision camera
- Electronic smart lock
- Electronic and robotic toys
- Blood pressure monitors
- Infusion pumps
- Electric toothbrush
- Beauty & grooming

3 Description

The DRV8210 is an integrated motor driver with four N-channel power FETs, charge pump regulator, and protection circuitry. The tripler charge pump architecture allows the device to operate down to 1.65 V to accommodate 1.8-V supply rails and low-battery conditions. The charge pump integrates all capacitors to reduce the overall solution size of the motor driver on a PCB and allows for 100% duty cycle operation.

The DRV8210 supports multiple control interface modes including: PWM (IN1/IN2), phase/enable (PH/EN), independent half-bridge, and parallel half-bridge. Each interface supports a low-power sleep mode to achieve ultra-low quiescent current draw by shutting down most of the internal circuitry.

The device can supply up to 1.76-A peak output current. It operates with a supply voltage from 1.65 V to 5.5 V.

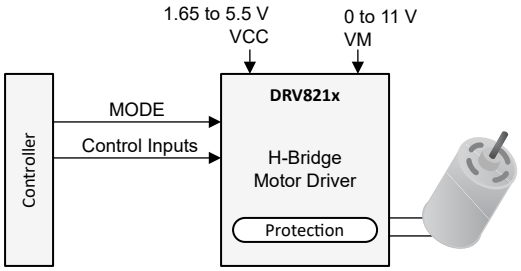
The driver offers robust internal protection features include supply undervoltage lockout (UVLO), output overcurrent (OCP), and device overtemperature (TSD).

The DRV8210 is part of a family of devices which come in pin-to-pin scalable $R_{DS(on)}$ and supply voltage options to support various loads and supply rails with minimal design changes. See Device Comparison for information on the devices in this family. View our full portfolio of brushed motor drivers on ti.com.

Device Information

PART NUMBER (1)	PACKAGE	BODY SIZE (NOM)
DRV8210DSG	WSON (8)	2.00 mm × 2.00 mm
DRV8210DRL	SOT563 (6)	1.20 mm × 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Schematic

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 Features....1
2 Applications....1
3 Description....1
4 Revision History....2
5 Device Comparison....3
6 Pin Configuration and Functions....4
7 Specifications....5
7.1 Absolute Maximum Ratings....5
7.2 ESD Ratings....5
7.3 Recommended Operating Conditions....5
7.4 Thermal Information....5
7.5 Electrical Characteristics....6
7.6 Typical Characteristics DSG Package....7
7.7 Typical Characteristics DRL Package....10
8 Detailed Description....12
8.1 Overview....12
8.2 Functional Block Diagram....12
8.3 Feature Description....13
8.4 Device Functional Modes....16
9 Application and Implementation....18
9.1 Application Information....18
9.2 Typical Application....18
9.3 Current Capability and Thermal Performance....28
10 Power Supply Recommendations....35
10.1 Bulk Capacitance....35
11 Layout....36
11.1 Layout Guidelines....36
11.2 Layout Example....36
12 Device and Documentation Support....38
12.1 Documentation Support....38
12.2 Receiving Notification of Documentation Updates....38
12.3 Support Resources....38
12.4 Trademarks....38
12.5 Electrostatic Discharge Caution....38
12.6 Glossary....38
13 Mechanical, Packaging, and Orderable Information....39

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (February 2020) to Revision A (April 2021)	Page
• Updated product family references on first page and Device comparison table	1
• Added technical information about the DRL package option to Pin Configuration and Functions, Specifications tables, Detailed Description, Applications and Implementation, and Layout sections	1

Changes from Revision A (April 2021) to Revision B (August 2021)	Page
• Updated Device Status to Production Data	1

Copyright © 2021 Texas Instruments Incorporated

5 Device Comparison

Table 5-1. Device Comparison Table

Device name	Supply voltage (V)	$R_{DS(on)}$ (mΩ)	I_{OCP} (A)	Interface options	Sleep mode entry	Pin-to-pin devices	Packages
DRV8210	1.65 to 11	950 (DRL), 1050 (DSG)	1.76	PWM, PH/EN, Half Bridge	Autosleep, VCC	DRV8210, DRV8212, DRV8220	SOT563 (DRL), WSON (DSG)
DRV8212	1.65 to 11	280	4				
DRV8220	4.5 to 18	1000	1.76		Autosleep, nSLEEP pin		
DRV8210P	1.65 to 11	1050	1.76	PWM	nSLEEP pin	DRV8837, DRV8837C, DRV8210P, DRV8212P	WSON (DSG)
DRV8212P	1.65 to 11	280	4				WSON (DSG)

6 Pin Configuration and Functions

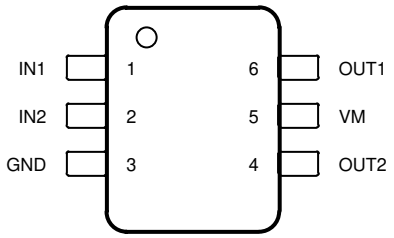


Figure 6-1. DRV8210 DRL Package 6-Pin SOT Top View

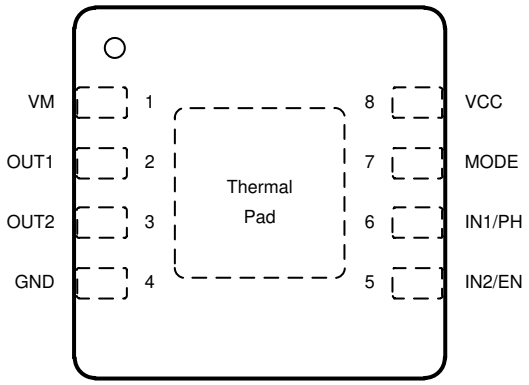


Figure 6-2. DRV8210 DSG Package 8-Pin WSON Top View

Table 6-1. Pin Functions

PIN			TYPE	DESCRIPTION
NAME	DRL	DSG		
GND	3	4	PWR	Device ground. Connect to system ground.
IN1	1	—	I	H-bridge control input. See Section 8.3.2. Internal pulldown resistor.
IN1/PH	—	6	I	H-bridge control input. See Section 8.3.2. Internal pulldown resistor.
IN2	2	—	I	H-bridge control input. See Section 8.3.2. Internal pulldown resistor.
IN2/EN	—	5	I	H-bridge control input. See Section 8.3.2. Internal pulldown resistor.
MODE	—	7	I	H-bridge control input mode. See Section 8.3.2. Tri-level input referenced to VCC pin voltage.
OUT1	6	2	O	H-bridge output. Connect to the motor or other load.
OUT2	4	3	O	H-bridge output. Connect to the motor or other load.
VM	5	1	PWR	Motor power supply. Bypass this pin to the GND pin with a 0.1-µF ceramic capacitor as well as sufficient bulk capacitance rated for VM.
VCC	—	8	PWR	Logic power supply. Bypass this pin to the GND pin with a 0.1-µF ceramic capacitor rated for VCC.
PAD	—	—	—	Thermal pad. Connect to system ground.

Copyright © 2021 Texas Instruments Incorporated

7 Specifications

7.1 Absolute Maximum Ratings

Over operating temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Power supply pin voltage	VM	-0.5	12	V
Logic power supply pin voltage, DSG	VCC	-0.5	5.75	V
Power supply transient voltage ramp	VM, VCC	0	2	V/µs
Logic pin voltage	INx, IN1/PH, IN2/EN	-0.5	5.75	V
Tri-level pin voltage	MODE	-0.5	V_{VCC}+0.3	
Output pin voltage	OUTx	$-V_{SD}$	$V_{VM}+V_{SD}$	V
Output current[1]	OUTx	Internally Limited	Internally Limited	A
Ambient temperature, T_A		–40	125	°C
Junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101[2]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ± 2000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ± 500 V may actually have higher performance.

7.3 Recommended Operating Conditions

Over operating temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{VM}	Motor power supply voltage, DRL	VM	1.65		11	V
V_{VM}	Motor power supply voltage DSG	VM	0		11	V
V_{VCC}	Logic power supply voltage DSG	VCC	1.65		5.5	V
V_{IN}	Logic pin voltage	INx, IN1/PH, IN2/EN, MODE	0		5.5	V
f_{PWM}	PWM frequency	INx, IN1/PH, IN2/EN	0		100	kHz
I_{OUT} [1]	Peak output current	OUTx	0		1.76	A
T_A	Operating ambient temperature		–40		125	°C
T_J	Operating junction temperature		–40		150	°C

(1) Power dissipation and thermal limits must be observed.

7.4 Thermal Information

THERMAL METRIC[1]		DRV8210 DRL (SOT563) 6 PINS	DRV8210 DSG (WSON) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	153.2	99.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	67.1	119.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	40.4	66.3	°C/W

Copyright © 2021 Texas Instruments Incorporated

THERMAL METRIC[1]		DRV8210 DRL (SOT563) 6 PINS	DRV8210 DSG (WSON) 8 PINS	UNIT
Ψ_{JT}	Junction-to-top characterization parameter	2.0	13.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	40.0	66.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		43.6	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

DRL: 1.65 V ≤ V_{VM} ≤ 11 V, DSG: 0 V ≤ V_{VM} ≤ 11 V and 1.65 V ≤ V_{VCC} ≤ 11 V, –40°C ≤ T_J ≤ 150°C (unless otherwise noted). Typical values are at T_J = 27°C, V_{VCC} = 3.3 V, and V_{VM} = 5 V.

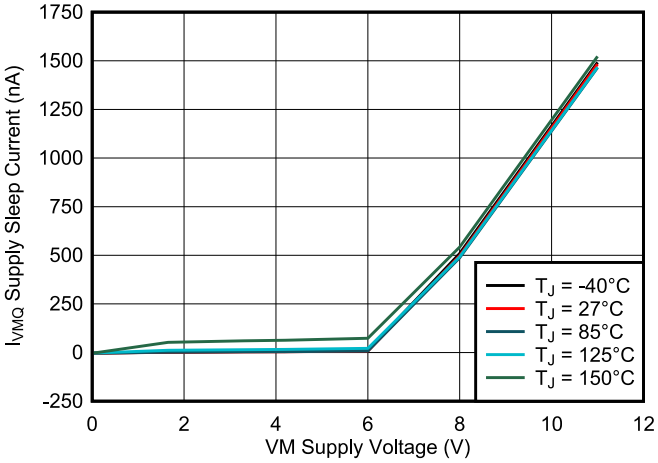
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY, DRL (VM)						
I_{VM}	VM active mode current	IN1 = 0 V, IN2 = 3.3 V		1.6	3.6	mA
I_{VMQ}	VM sleep mode current	INx = 0 V, after waiting t_{sleep}, V_{VM} = 5 V, T_J = 27°C		1	55	nA
t_{WAKE}	Turnon time	Sleep mode to active mode delay			100	µs
$t_{AUTOSLEEP}$	Autosleep turnoff time	Active mode to autosleep mode delay	0.9		2.6	ms
POWER SUPPLIES, DSG (VM, VCC)						
I_{VM}	VM active mode current	IN1 = 0 V, IN2 = 3.3 V		1.4	3.6	mA
I_{VMQ}	VM sleep mode current	Sleep mode, V_{VM} = 5 V, V_{VCC} = 3.3 V, T_J = 27°C		1	82	nA
I_{VMQ_UV}	VM sleep mode current	INx = 0 V, V_{VM} = 5 V, V_{VCC} < 0.35 V, T_J = 27°C		2	89	nA
I_{VCC}	VCC active mode current	IN1 = 0 V, IN2 = 3.3 V		0.18	3.6	mA
I_{VCCQ}	VCC sleep mode current	Sleep mode, V_{VM} = 5 V, V_{VCC} = 3.3 V, T_J = 27°C			2.5	nA
I_{VCCQ_UV}	VCC sleep mode current	INx = 0 V, V_{VM} = 5 V, V_{VCC} < 0.35 V, T_J = 27°C			35	nA
t_{WAKE}	Turnon time	Sleep mode to active mode delay			100	µs
$t_{AUTOSLEEP}$	Autosleep turnoff time	Active mode to autosleep mode delay	0.9		2.6	ms
LOGIC-LEVEL INPUTS (INx, IN1/PH, IN2/EN)						
V_{IL}	Input logic low voltage		0		0.4	V
V_{IH}	Input logic high voltage		1.45		5.5	V
V_{HYS}	Input logic hysteresis		49			mV
I_{IL}	Input logic low current	V_I = 0 V	-1		1	µA
I_{IH}	Input logic high current	V_I = 3.3 V	20		50	µA
R_{PD}	Input pulldown resistance	To GND		100		kΩ
TRI-LEVEL INPUTS (MODE)						
V_{TIL}	Tri-level input logic low voltage		0		0.22 × V_{VCC}	V
V_{TIZ}	Tri-level input Hi-Z voltage		0.60 × V_{VCC}		0.675 × V_{VCC}	V
V_{TIH}	Tri-level input logic high voltage		0.75 × V_{VCC}		5.5	V
R_{TPD}	Tri-level pulldown resistance	to GND		130		kΩ
R_{TPU}	Tri-level pullup resistance	to VCC		75		kΩ
DRIVER OUTPUTS (OUTx)						
$R_{DS(on)_HS}$	High-side MOSFET on resistance	I_O = 0.2 A, DRL		475		mΩ
$R_{DS(on)_HS}$	High-side MOSFET on resistance	I_O = 0.2 A, DSG		525		mΩ
$R_{DS(on)_LS}$	Low-side MOSFET on resistance	I_O = –0.2 A, DRL		475		mΩ
$R_{DS(on)_LS}$	Low-side MOSFET on resistance	I_O = –0.2 A, DSG		525		mΩ

Copyright © 2021 Texas Instruments Incorporated

DRL: 1.65 V ≤ V_{VM} ≤ 11 V, DSG: 0 V ≤ V_{VM} ≤ 11 V and 1.65 V ≤ V_{VCC} ≤ 11 V, –40°C ≤ T_J ≤ 150°C (unless otherwise noted). Typical values are at T_J = 27°C, V_{VCC} = 3.3 V, and V_{VM} = 5 V.

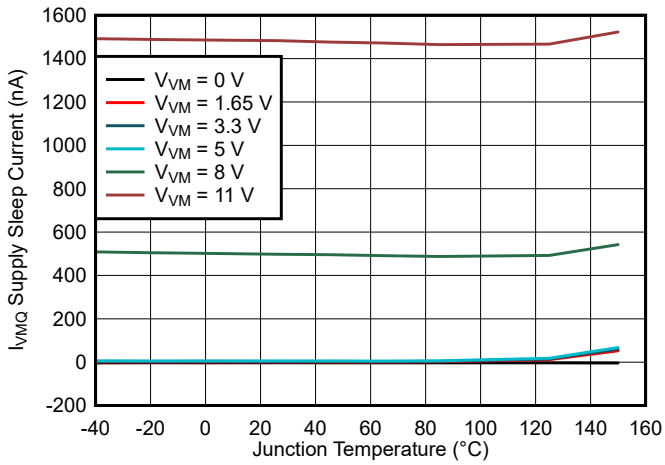
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{SD}	Body diode forward voltage	I_O = –0.5 A		1		V
t_{RISE}	Output rise time	V_{OUTx} rising from 10% to 90% of V_{VM}		150		ns
t_{FALL}	Output fall time	V_{OUTx} falling from 90% to 10% of V_{VM}		150		ns
t_{PD}	Input to output propagation delay	Input crosses 0.8 V to V_{OUTx} = 0.1×V_{VM}, I_O = 1 A		135		ns
t_{DEAD}	Output dead time	Internal dead time		500		ns
I_{OUT}	Leakage current into OUTx	OUTx is Hi-Z, R_L = 20 Ω to VM		186		µA
		OUTx is Hi-Z, R_L = 20 Ω to GND		-3		nA
PROTECTION CIRCUITS						
$V_{UVLO,VM}$	VM supply undervoltage lockout (UVLO), DRL	Supply rising			1.65	V
		Supply falling	1.30			V
$V_{UVLO,VCC}$	VCC supply undervoltage lockout (UVLO), DSG	Supply rising			1.65	V
		Supply falling	1.30			V
V_{UVLO_HYS}	Supply UVLO hysteresis	Rising to falling threshold		80		mV
t_{UVLO}	Supply undervoltage deglitch time	V_{VM} falling (DRL) or V_{VCC} falling (DSG) to OUTx disabled		3.8		µs
I_{OCP}	Overcurrent protection trip point		1.76			A
t_{OCP}	Overcurrent protection deglitch time			4.2		µs
t_{RETRY}	Overcurrent protection retry time			1.7		ms
T_{TSD}	Thermal shutdown temperature		153		193	°C
T_{HYS}	Thermal shutdown hysteresis			22		°C

7.6 Typical Characteristics DSG Package



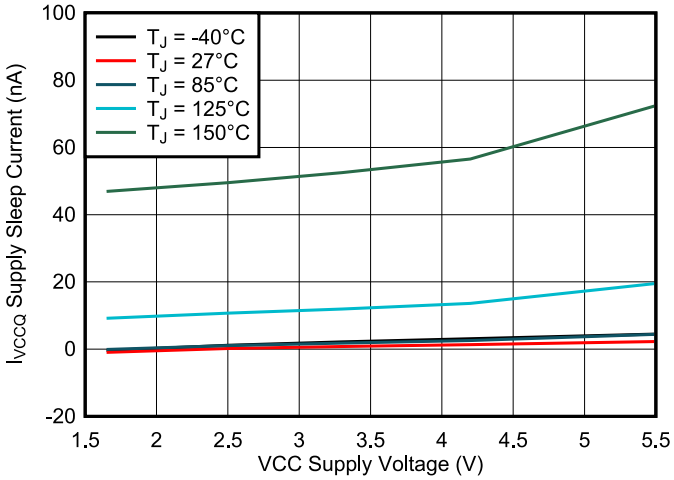
A. V_{VCC} = 3.3 V

Figure 7-1. Sleep Current (I_{VMQ}) vs. Supply Voltage (V_{VM})



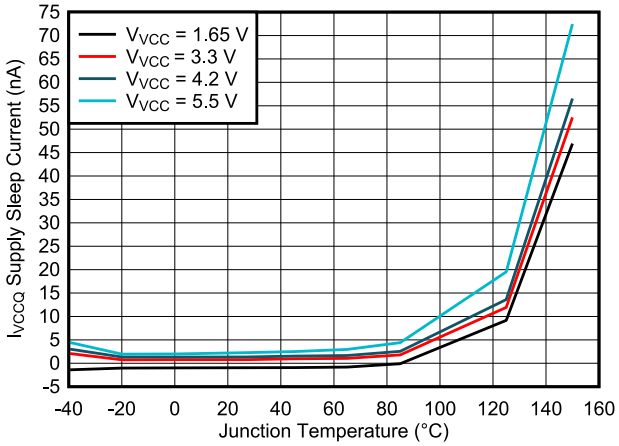
A. V_{VCC} = 3.3 V

Figure 7-2. Sleep Current (I_{VMQ}) vs. Junction Temperature (T_J)



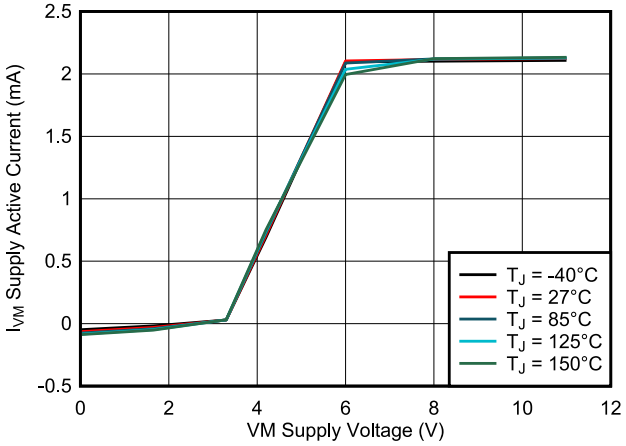
A. V_{VM} = 5 V

Figure 7-3. Sleep Current (I_{VCCQ}) vs. Supply Voltage (V_{VCC})



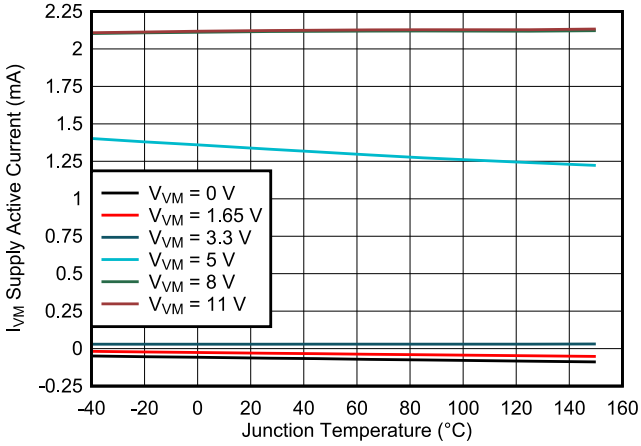
A. V_{VM} = 5 V

Figure 7-4. Sleep Current (I_{VCCQ}) vs. Junction Temperature (T_J)



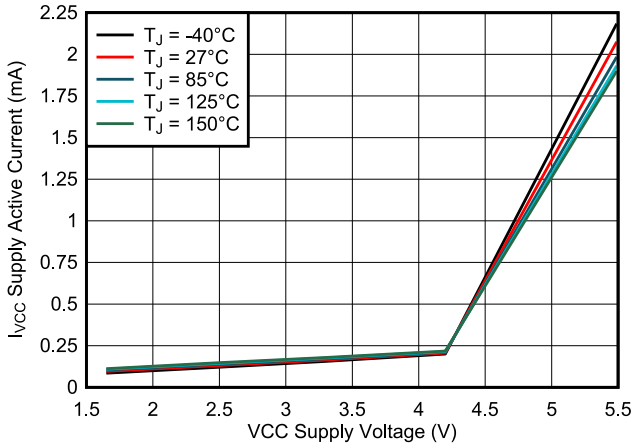
A. V_{VCC} = 3.3 V

Figure 7-5. Active Current (I_{VM}) vs. Supply Voltage (V_{VM})



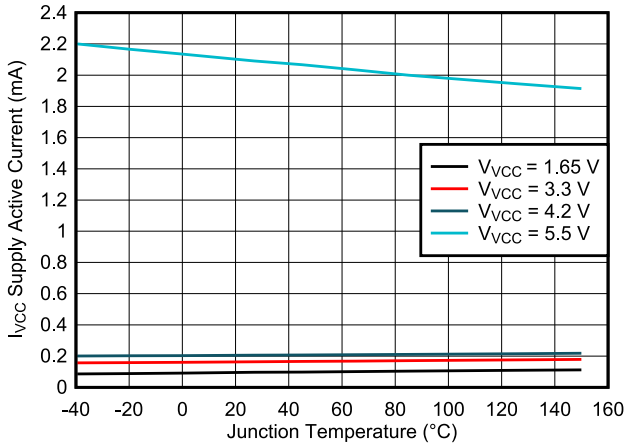
A. V_{VCC} = 3.3 V

Figure 7-6. Active Current (I_{VM}) vs. Junction Temperature (T_J)



A. V_{VM} = 5 V

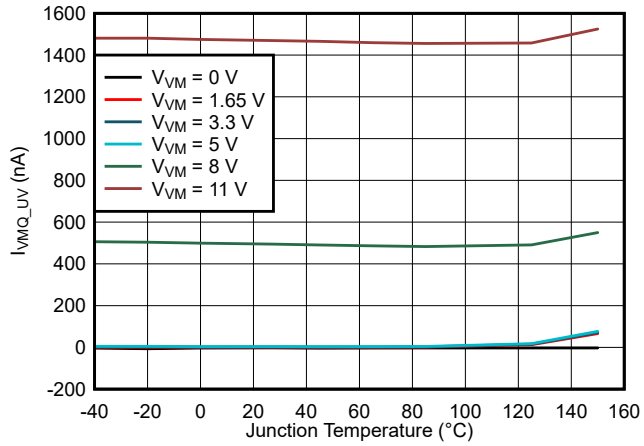
Figure 7-7. Active Current (I_{VCC}) vs. Supply Voltage (V_{VCC})



A. V_{VM} = 5 V

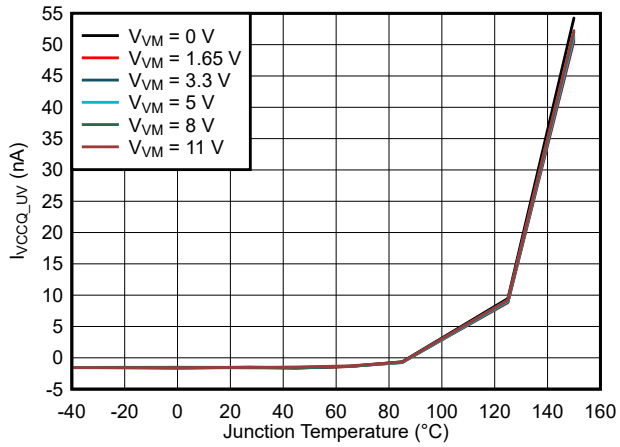
Figure 7-8. Active Current (I_{VCC}) vs. Junction Temperature (T_J)

Copyright © 2021 Texas Instruments Incorporated



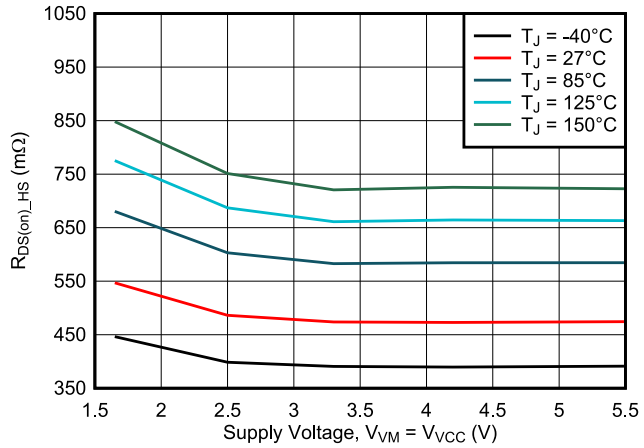
A. V_{VCC} < 0.35 V

Figure 7-9. VM supply current when VCC is low (I_{VMQ_UV}) vs. Junction Temperature (T_J)



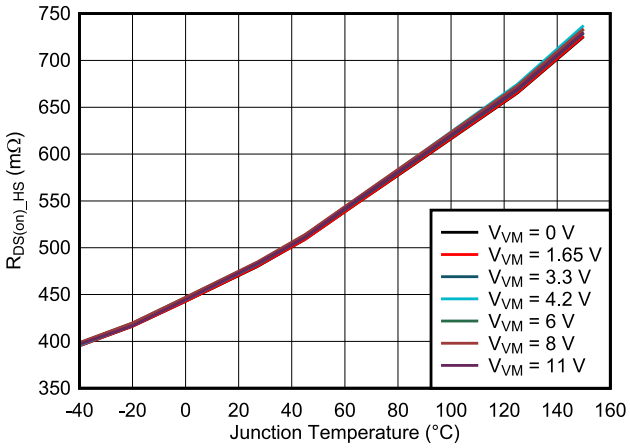
A. V_{VCC} < 0.35 V

Figure 7-10. VCC supply current when VCC is low (I_{VCCQ_UV}) vs. Junction Temperature (T_J)



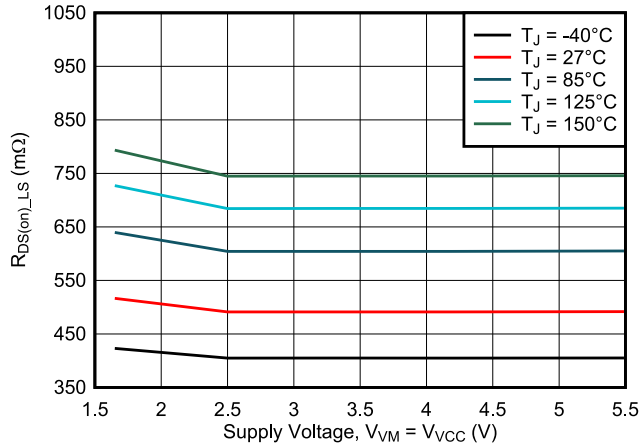
A. V_{VM} = V_{VCC}

Figure 7-11. High-Side $R_{DS(on)}$ vs. Supply Voltage



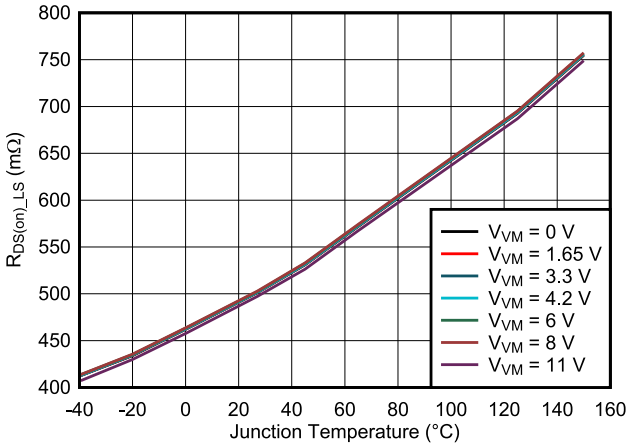
A. V_{VCC} = 3.3 V

Figure 7-12. High-Side $R_{DS(on)}$ vs. Junction Temperature (T_J)



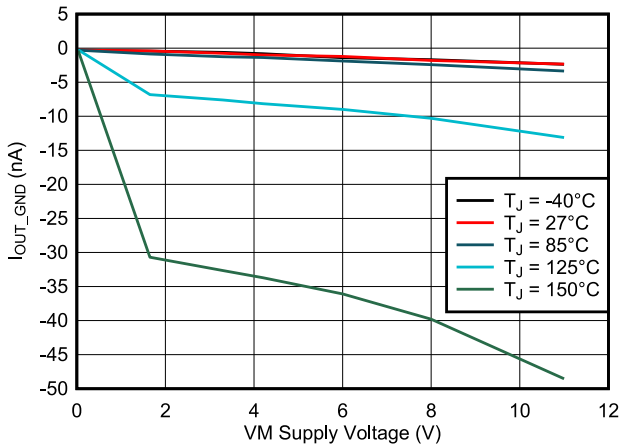
A. V_{VM} = V_{VCC}

Figure 7-13. Low-Side $R_{DS(on)}$ vs. Supply Voltage



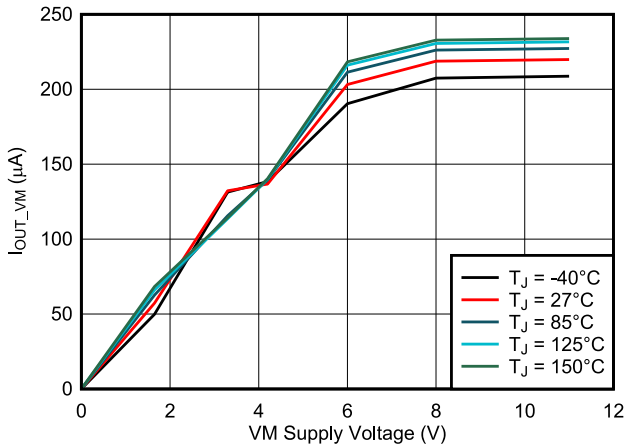
A. V_{VCC} = 3.3 V

Figure 7-14. Low-Side $R_{DS(on)}$ vs. Junction Temperature (T_J)



A. V_{VCC} = 3.3 V

Figure 7-15. High-Z Leakage Current into OUTx (I_{OUT}) with OUTx connected to GND vs. Supply Voltage (V_{VM})



A. V_{VCC} = 3.3 V

Figure 7-16. High-Z Leakage Current into OUTx (I_{OUT}) with OUTx connected to VM vs. Supply Voltage (V_{VM})

7.7 Typical Characteristics DRL Package

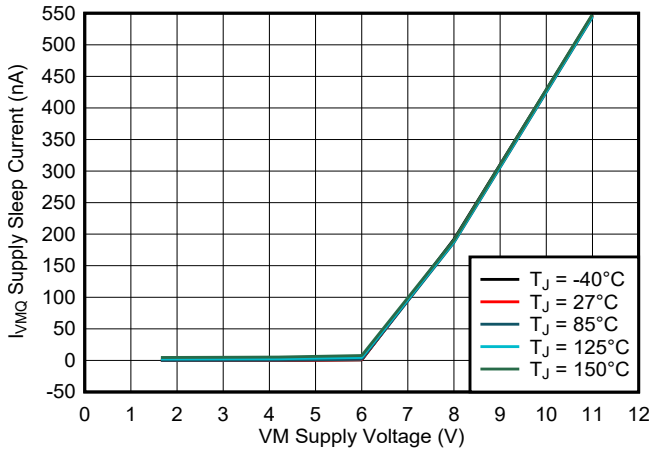


Figure 7-17. Sleep Current (I_{VMQ}) vs. Supply Voltage (V_{VM})

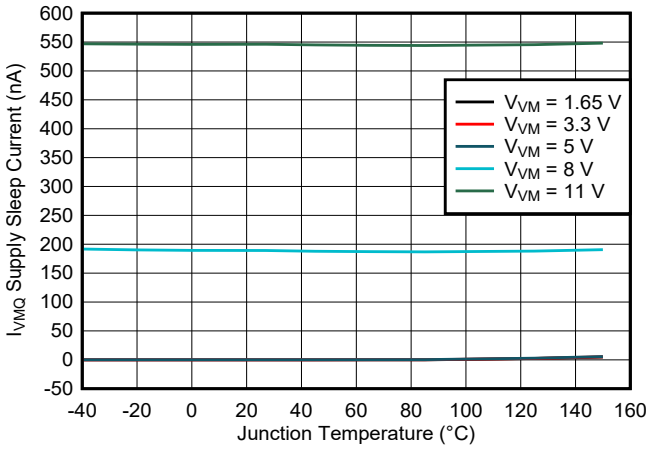


Figure 7-18. Sleep Current (I_{VMQ}) vs. Junction Temperature (T_J)

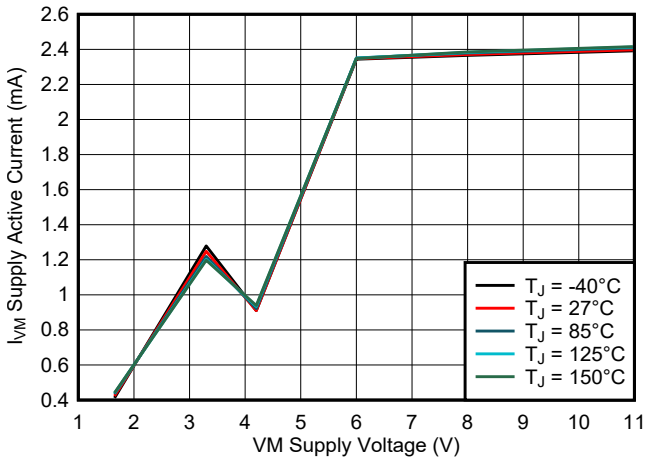


Figure 7-19. Active Current (I_{VM}) vs. Supply Voltage (V_{VM})

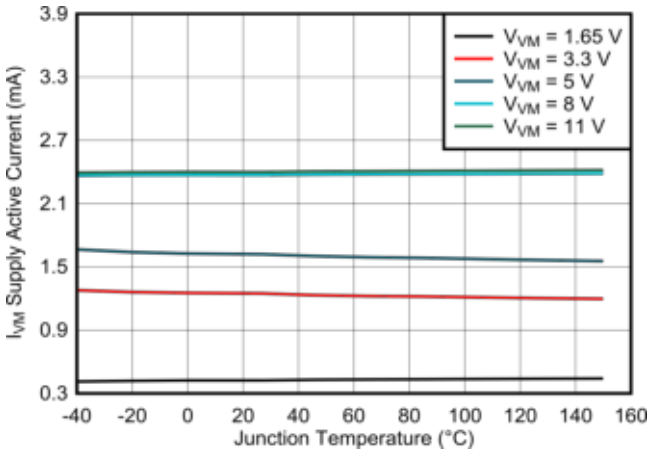


Figure 7-20. Active Current (I_{VM}) vs. Junction Temperature (T_J)

Copyright © 2021 Texas Instruments Incorporated

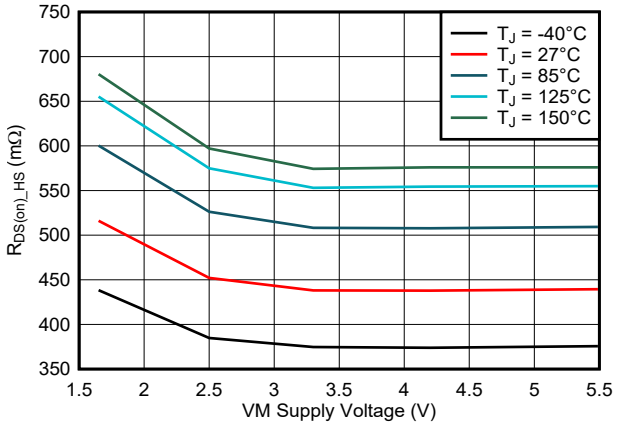


Figure 7-21. High-Side $R_{DS(on)}$ vs. Supply Voltage

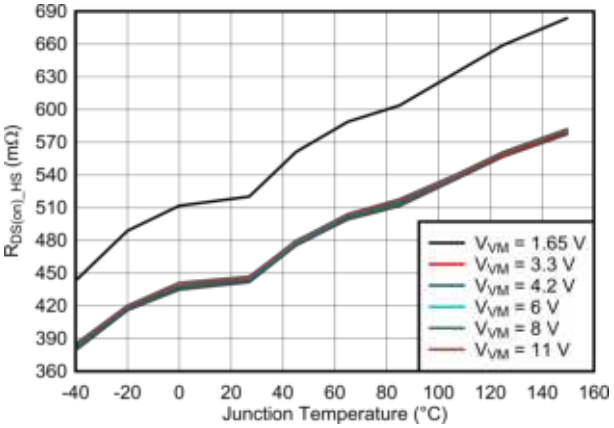


Figure 7-22. High-Side $R_{DS(on)}$ vs. Junction Temperature (T_J)

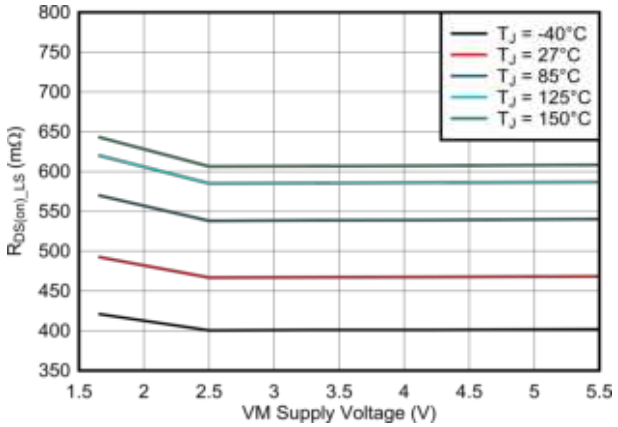


Figure 7-23. Low-Side $R_{DS(on)}$ vs. Supply Voltage

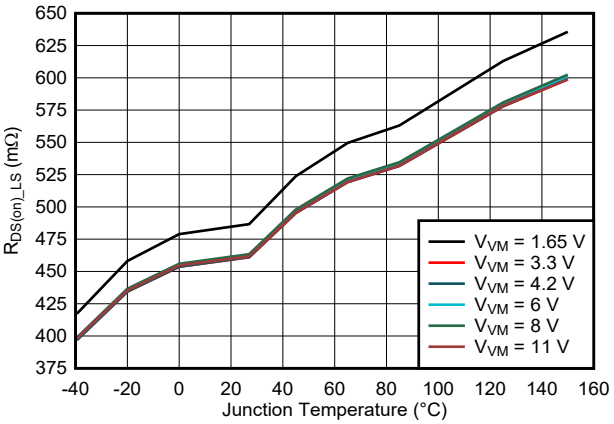


Figure 7-24. Low-Side $R_{DS(on)}$ vs. Junction Temperature (T_J)

8 Detailed Description

8.1 Overview

DRV8210 is an integrated H-bridge driver with multiple control interface options: PWM (IN1/IN2) interface (DRL and DSG packages), PH/EN (DSG only), or half-bridge interface (DSG only). To reduce area and external components on a printed circuit board, the device integrates a charge pump regulator and its capacitors. In the DSG package, the separate motor (VM) and logic (VCC) supplies allow the motor supply voltage to drop to 0 V without significant impact to $R_{DS(on)}$ and without triggering UVLO as long as the VCC supply is stable. A timed auto-sleep mode reduces microcontroller GPIO connections by eliminating a disable/sleep pin and automatically putting the device into a low-power sleep mode when the inputs remain inactive for 1-2 ms.

The PWM interface is a standard 2-pin (IN1/IN2) motor drive interface. The PH/EN interface allows bi-directional PWM control using only one PWM resource from the controller. PWM and PH/EN interfaces can drive loads like brushed DC motors and bistable relays bidirectionally. Independent half-bridge mode allows for full control over each half-bridge. The half-bridges can independently control two loads with each channel acting as a high-side or low-side driver with half of the $R_{DS(on)}$ of full-bridge driving. Alternatively, half-bridge mode also allows the inputs and outputs to be connected together, or "paralleled," to drive a single load as a high-side or low-side driver with one-forth the $R_{DS(on)}$ of full-bridge driving.

The integrated protection features protect the device in the case of a system fault. These include undervoltage lockout (UVLO), overcurrent protection (OCP), and overtemperature shutdown (TSD).

8.2 Functional Block Diagram

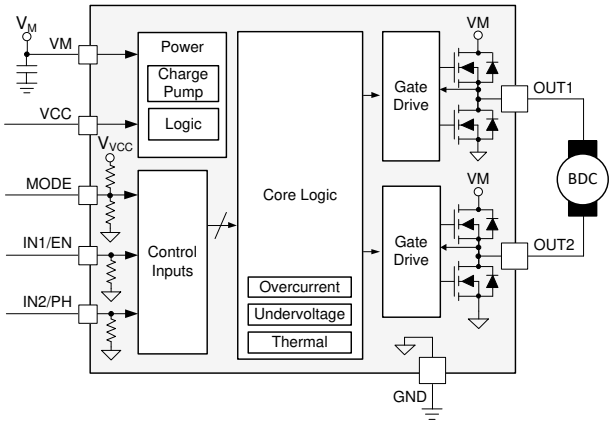


Figure 8-1. Multiple interface variant in DSG package

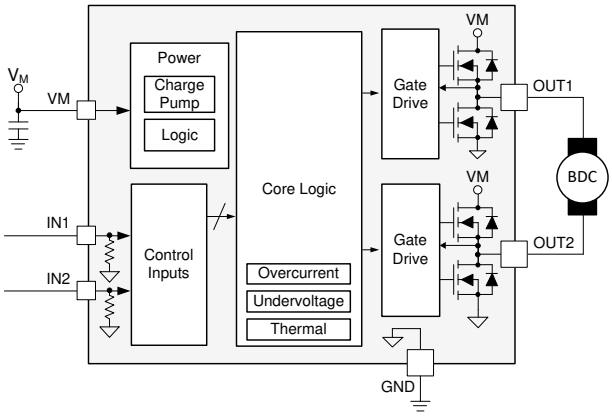


Figure 8-2. PWM interface variant in DRL package

Copyright © 2021 Texas Instruments Incorporated

8.3 Feature Description

8.3.1 External Components

Table 8-1 lists the recommended external components for the device.

Table 8-1. Recommended external components

COMPONENT	PIN 1	PIN 2	RECOMMENDED
C_{VM1}	VM	GND	0.1-µF, low ESR ceramic capacitor, VM-rated.
C_{VM2}	VM	GND	Section 10.1, VM-rated.
C_{VCC}	VCC	GND	0.1-µF, low ESR ceramic capacitor, VCC-rated. Only needed for DSG package variant.

8.3.2 Control Modes

The DRV8210 provides three modes to support different control schemes with the PH/IN1 and EN/IN2 pins. The MODE pin selects the control interface mode by setting it either logic low, logic high, or Hi-Z as shown in Table 8-2. The MODE pin does not latch its state, so it may be changed during operation.

The DRL package variant only supports the PWM interface (see Table 8-3).

Table 8-2. MODE pin functions for DSG variant

MODE STATE	CONTROL MODE
MODE = Logic Low	PWM
MODE = Logic High	PH/EN
MODE = Hi-Z	Half-Bridge

The inputs can accept DC or pulse-width modulated (PWM) voltage signals with duty cycles from 0% to 100%. By default, the INx, PH/IN1, and EN/IN2 pins have internal pulldown resistors to ensure the outputs are Hi-Z if no inputs are present (the only exception is half-bridge mode, where OUTx = L if INx is floating).

The following sections show the truth tables for each control mode. Additionally, the DRV8210 automatically handles the dead-time generation when switching between the high-side and low-side MOSFET of a half-bridge. Figure 8-3 describes the naming and configuration for the various H-bridge states described in the following sections.

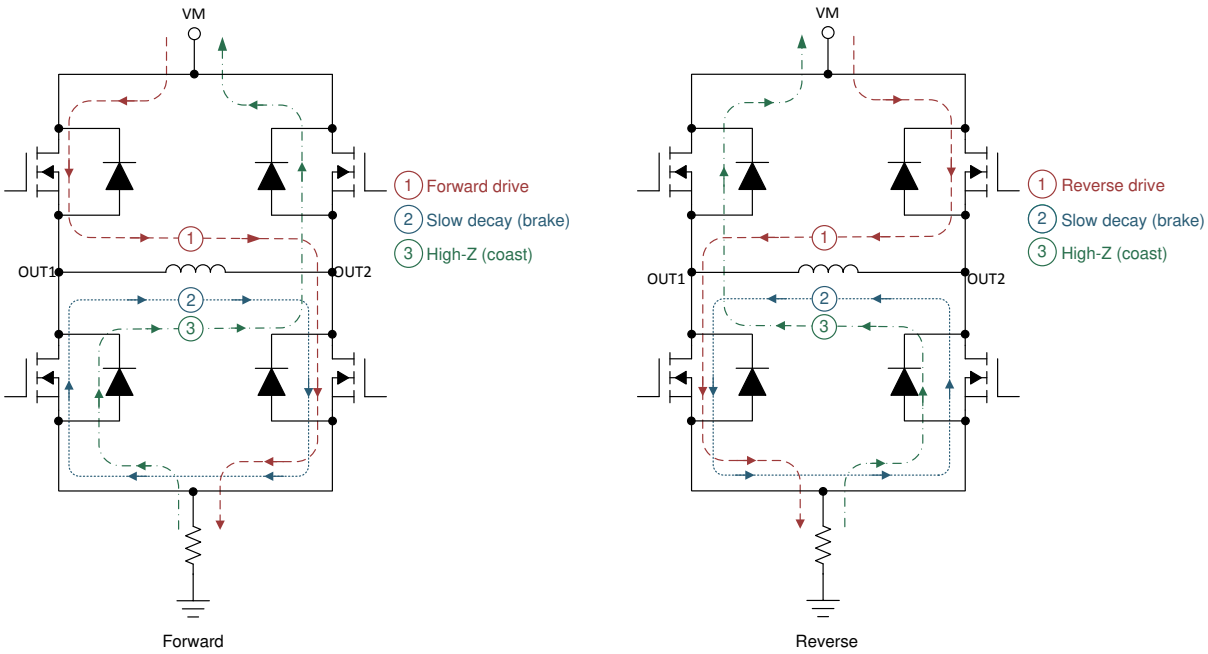


Figure 8-3. H-bridge states

8.3.2.1 PWM Control Mode (DSG: MODE = 0 and DRL)

The PWM interface (IN1/IN2) controls the OUTx pins according to the logic table in Table 8-3. In the DSG package, setting the MODE pin logic low selects PWM mode. The coast/Hi-Z state doubles as an automatic sleep mode. After staying in the coast/Hi-Z state for t_{SLEEP}, the device will automatically go into low-power sleep mode (autosleep). The PWM mode is the only interface mode available in the DRL package.

Table 8-3. PWM control mode with automatic sleep

IN1	IN2	OUT1	OUT2	DESCRIPTION
0	0	Hi-Z	Hi-Z	Coast (H-bridge Hi-Z)/ low-power automatic sleep mode
0	1	L	H	Reverse (OUT2 → OUT1)
1	0	H	L	Forward (OUT1 → OUT2)
1	1	L	L	Brake (low-side slow decay)

8.3.2.2 PH/EN Control Mode (DSG: MODE = 1)

When the MODE pin is logic high on power up, the device selects "phase-enable" mode (PH/EN). PH/EN mode allows for the H-bridge to be controlled with a speed and direction type of interface. Table 8-4 shows the truth table for PH/EN mode. When the EN pin is low, the device enters brake mode. This allows the controller to use a single PWM generator peripheral on the EN pin while a standard GPIO pin controls directions using the PH pin. However, if the EN pin remains low for longer than t_{SLEEP}, the device goes into low-power sleep mode and the outputs are disabled.

Table 8-4. PH/EN control mode

EN	PH	OUT1	OUT2	DESCRIPTION
0	X	L → Hi-Z	L → Hi-Z	Brake (low-side slow decay) for t_{SLEEP}, then auto-sleep mode (H-bridge Hi-Z)
1	0	L	H	Reverse (OUT2 → OUT1)
1	1	H	L	Forward (OUT1 → OUT2)

8.3.2.3 Half-Bridge Control Mode (DSG: MODE = Hi-Z)

When the MODE pin is floating (Hi-Z), selects the half-bridge control mode. This mode allows for each half-bridge to be directly controlled in order to support high-side slow decay (or brake), driving two independent loads, or paralleling the outputs for higher current capability for a single load. Table 8-5 shows the truth table for independent half-bridge mode.If the MODE pin is connected to a GPIO pin from a microcontroller, the microcontroller can achieve the Hi-Z state by setting the GPIO pin as an input. When using half-bridge mode, the device can go into sleep mode by bringing the MODE, IN1, and IN2 pins logic low. The GPIO controlling the MODE pin will need to be reconfigured as an output set to logic low. Alternatively, the VCC pin can be supplied from a GPIO and used to put the device to sleep in some cases. See Section 8.4.2 for more details.

Table 8-5. Half-bridge control mode

VCC	MODE	IN1	IN2	OUT1	OUT2	DESCRIPTION
0 V	X	X	X	Hi-Z	Hi-Z	Low-power sleep mode
1.65-5.5 V	0	0	0	Hi-Z	Hi-Z	H-bridge disable/low-power automatic sleep mode
1.65-5.5 V	Hi-Z	0	X	L	X	OUT1 low-side On
1.65-5.5 V	Hi-Z	1	X	H	X	OUT1 high-side On
1.65-5.5 V	Hi-Z	X	0	X	L	OUT2 low-side On
1.65-5.5 V	Hi-Z	X	1	X	H	OUT2 high-side On

Copyright © 2021 Texas Instruments Incorporated

8.3.3 Protection Circuits

The DRV8210 is fully protected against supply undervoltage, output overcurrent, and device overtemperature events.

8.3.3.1 Supply Undervoltage Lockout (UVLO)

If at any time the supply voltage falls below the undervoltage lockout threshold voltage, all MOSFETs in the H-bridge will be disabled. The charge pump and device logic are disabled in this condition. When powered by split supplies (DSG package only), the UVLO triggers when the VCC pin voltage drops below $V_{UVLO,VCC}$ falling threshold. This allows the VM supply to dip all the way to 0 V. When operating from a single supply (DRL package only), the UVLO triggers when the VM pin voltage drops below $V_{UVLO,VM}$ falling threshold. Normal operation resumes when the supply voltage rises above the V_{UVLO} rising threshold. Table 8-6 summarizes the conditions when the device enters UVLO.

Table 8-6. UVLO response conditions

Package variant	V_{VM}	V_{VCC}	Device response
DSG	0 V to V_{VM_MAX}	<1.65 V	UVLO
	0 V to V_{VM_MAX}	>1.65 V	Normal operation
DRL	<1.65 V	N/A	UVLO
	1.65 V to V_{VM_MAX}	N/A	Normal operation

8.3.3.2 OUTx Overcurrent Protection (OCP)

An analog current limit circuit on each MOSFET limits the peak current out of the device even in hard short circuit events. If the output current exceeds the overcurrent threshold, I_{OCP}, for longer than the overcurrent deglitch time, t_{OCP}, all MOSFETs in the H-bridge will be disabled. After t_{RETRY}, the MOSFETs are re-enabled according to the state of the PH/IN1 and EN/IN2 pins. If the overcurrent condition is still present, the cycle repeats; otherwise normal device operation resumes.

In half-bridge control mode, the OCP behavior is slightly modified. If an overcurrent event is detected, only the corresponding half-bridge will be disabled. The other half-bridge will continue normal operation. This allows for the device to manage independent fault events when driving independent loads. If an overcurrent event is detected in both half-bridges, both half-bridges will be disabled. Both half-bridges share the same overcurrent retry timer. If an overcurrent event occurs first in OUT1, that output will disable for the duration of t_{RETRY}. If OUT2 experiences an overcurrent event after OUT1, but before t_{RETRY} has expired, then both OUTx pins will remain disabled for a full duration of t_{RETRY}.

8.3.3.3 Thermal Shutdown (TSD)

If the die temperature exceeds the overtemperature limit T_{TSD}, all MOSFETs in the H-bridge will be disabled. Normal operation will resume when the overtemperature condition is removed and the die temperature drops below the T_{TSD} threshold.

8.3.4 Pin Diagrams

8.3.4.1 Logic-Level Inputs

Figure 8-4 shows the input structure for the logic-level input pins IN1, IN2, PH/IN1, and EN/IN2.

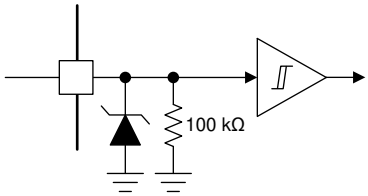


Figure 8-4. Logic-level input

8.3.4.2 Tri-Level Input

Figure 8-5 shows the input structure for the tri-level input pin, MODE.

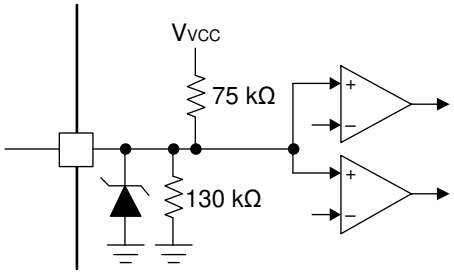


Figure 8-5. MODE tri-level input

8.4 Device Functional Modes

The DRV8210 has several different modes of operation depending on the system inputs and conditions.

8.4.1 Active Mode

In active mode, the H-bridge, charge pump, and internal logic are active and the device is ready to receive inputs. The device leaves active mode when entering low-power sleep mode or fault mode. When waking from autosleep, the INx pins (DRL package or DSG package when MODE = 0) or EN pin (DSG package when MODE = 1) must be held high for the duration of t_{WAKE} to enable the device. After the t_{WAKE} time has elapsed, the device is awake, and the INx pins or EN pin may receive a PWM signal.

When $V_{VCC} < V_{VM}$, the DRV8210 draws active current from the VM pin rather than the VCC pin. During this operating condition, I_{VCC} is typically less than 500 nA (see Figure 7-5 and Figure 7-7.)

8.4.2 Low-Power Sleep Mode

The DRV8210 supports a low-power sleep mode to reduce current consumption from VM and VCC when the driver is not active. There are two ways to enter low-power sleep mode: autosleep and using the VCC pin. In autosleep mode, the device draws minimal current denoted by I_{VCCQ} and I_{VMQ}. Both DSG and DRL packages support autosleep. In VCC sleep mode, the device draws minimal current denoted by I_{VMQ_UV} and I_{VCCQ_UV}. Only the DSG package can go into low-power mode using the VCC pin. Table 8-7 describes how to enter low-power sleep mode.

Table 8-7. Sleep mode summary

Variant	Input pin state	OUT1	OUT2	Description
DRL	IN1 = IN2 = 0	Hi-Z	Hi-Z	**Autosleep for PWM or half-bridge interface:** Upon entering this state, the outputs are disabled. The device remains in Active Mode for t_{SLEEP}, then goes into low-power mode.
DSG	MODE = 0, IN1 = IN2 = 0	Hi-Z	Hi-Z	
	MODE = 1, EN = 0	L → Hi-Z	L → Hi-Z	**Autosleep for PH/EN interface:** Upon entering this state, both outputs go into brake mode by turning the low-side FETs on. The device remains in this state for t_{SLEEP}, then goes into low-power mode. Once in low-power mode, the outputs are disabled.
	VCC = 0 V	Hi-Z	Hi-Z	**VCC supply as sleep pin:** The VCC pin can be supplied from a GPIO pin and used to put the device to sleep. By bringing the GPIO pin low, the device enters low-power mode by using UVLO. To wake up the device, set the GPIO pin high (VCC > V_{UVLO}), then set EN = 1 if MODE = 1, or set/toggle either INx input to 1 if MODE = Hi-Z or 1. See Section 9.2.2.2.3 for more information on using the VCC pin for sleep.

The device returns to active mode when the input pins move to a state other than the ones in Table 8-7. To wake up the device from autosleep mode, the INx pins or EN pin (depending on MODE state) must be asserted high for longer than t_{WAKE} before receiving PWM input signals.

Copyright © 2021 Texas Instruments Incorporated

To wake up the device from VCC sleep mode, the VCC pin voltage must be greater than $V_{UVLO,VCC}$. Once the VCC pin has a valid voltage, either or both INx pins must be asserted high for longer than t_{WAKE} to fully wake up the device. To protect the microcontroller GPIO pin from excess current due to the decoupling capacitor charging current, a resistor may need to be added between the GPIO and the decoupling capacitor on the VCC pin. See Section 9.2.2.2.3 for more information on designing this limiting resistor.

To ensure lowest supply current draw, TI recommends setting all input pins to logic low to eliminate current draw through the pulldown resistors in sleep mode. If the MODE pin is set to Hi-Z or logic low, it will not draw current in sleep mode. However, the MODE pin will draw some current in sleep mode when it is logic high.

8.4.3 Fault Mode

The DRV8210 enters a fault mode when a fault is encountered. This protects the device and the output load. The device behavior in the fault mode is described in Section 8.3.3 and depends on the fault condition. The device leaves the fault mode and re-enters the active mode once the recovery condition is met. Table 8-8 summarizes the fault conditions, response, and recovery.

Table 8-8. Fault condition summary

FAULT	CONDITION	H-BRIDGE	RECOVERY
Undervoltage Lockout (UVLO), DSG	VCC < $V_{UVLO,VCC}$ falling	Disabled	VCC > $V_{UVLO,VCC}$ rising
Undervoltage Lockout (UVLO), DRL	VM < $V_{UVLO,VM}$ falling	Disabled	VM > $V_{UVLO,VM}$ rising
Overcurrent (OCP)	$I_{OUT} > I_{OCP}$	Disabled	t_{RETRY}
Thermal Shutdown (TSD)	$T_J > T_{TSD}$	Disabled	$T_J < T_{TSD} – T_{HYS}$

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The DRV8210 can be used in a variety of applications that require either a half-bridge or H-bridge power stage configuration. Common application examples include brushed DC motors, solenoids, bistable latching relays, and actuators. These devices can also drive many common passive loads such as LEDs, resistive elements, relays, etc. This section highligts some application examples for the DRV8210.

9.2 Typical Application

9.2.1 Full-Bridge Driving

A typical application for the DRV8210 is to drive a brushed DC motor or single-coil latching relay bidriectionally (in forward and reverse) using the outputs as a full-bridge, or H-bridge, configuration. Figure 9-1 and Figure 9-2 show examples for each package variant driving a motor with the PWM interface. Figure 9-3 shows an example of driving a single-coil latching relay with the PWM interface. Figure 9-4 shows an example of driving a motor with the PH/EN interface.

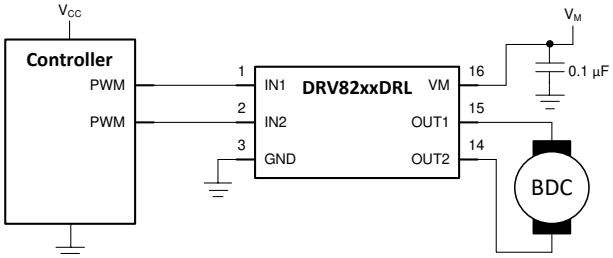


Figure 9-1. PWM interface motor-driving application for DRL package

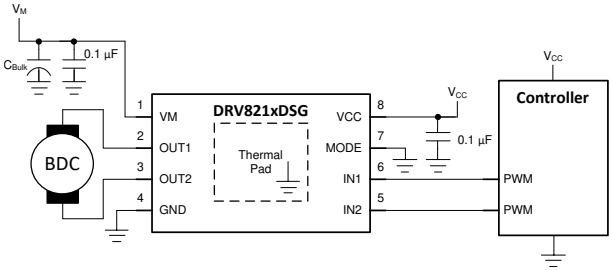


Figure 9-2. PWM interface motor-driving application for DSG package

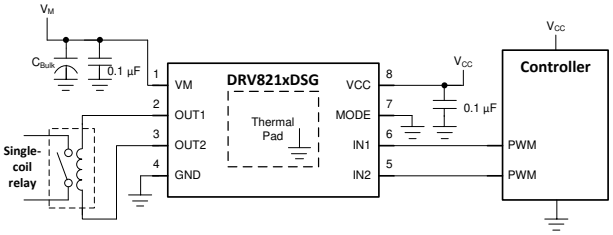


Figure 9-3. PWM interface single-coil latching relay application

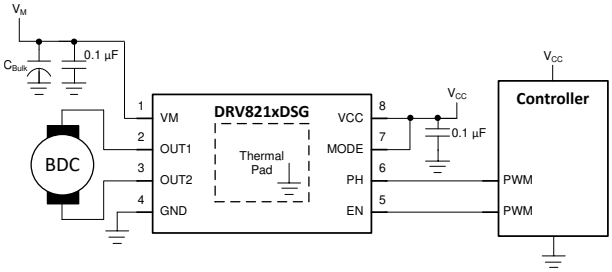


Figure 9-4. PH/EN interface motor-driving application for DSG package

9.2.1.1 Design Requirements

Table 9-1 lists the required parameters for a typical usage case.

Table 9-1. System design requirements

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Motor supply voltage	V_M	11 V
Logic supply voltage	V_{CC}	3.3 V

Copyright © 2021 Texas Instruments Incorporated

Table 9-1. System design requirements (continued)

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Target motor RMS current	I_{motor}	300 mA
Target relay current	I_{relay}	50 mA

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Supply Voltage

The appropriate supply voltage depends on the ratings of the load (motor, solenoid, relay, etc.). In the case of a brushed DC motor, the supply voltage will impact the desired RPM. A higher voltage spins a brushed dc motor faster with the same PWM duty cycle applied to the power FETs. A higher voltage also increases the rate of current change through the inductive windings of a motor, solenoid, or relay.

9.2.1.2.2 Control Interface

Section 8.3.2.1 describes the PWM control interface depending on selected package. TI recommends connecting the the MODE pin directly to the GND net as shown in Figure 9-2. However, if other interface states are required in the application, the MODE pin may be connected to a GPIO pin to select the other interface options during operation. The autosleep feature allows for bidirectional control of the motor and low-power mode using only two pins. This eliminates the need for another GPIO to control a sleep pin. Figure 9-5 and Figure 9-6 show waveform examples of driving a motor with the PWM interface.

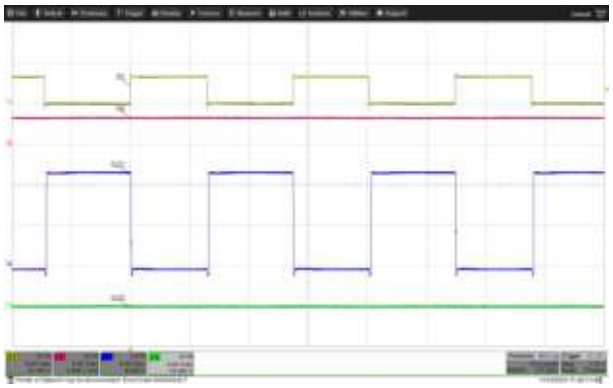
Figure 9-7 and Figure 9-8 show waveform examples of driving a single coil relay with the PWM interface. The relay can be driven between the forward/reverse states and the brake/coast states as shown in the figures.

Section 8.3.2.2 describes the PH/EN control interface. Connecting the MODE pin to the microcontroller supply selects the PH/EN interface. PH/EN mode helps to reduce the number of microcontroller PWM generators needed for motor driving by toggling only the EN pin. The PH pin controls the direction of motor driving with this interface. The device will enter sleep mode if EN is held low for longer than t_{SLEEP}.

9.2.1.2.3 Low-Power Operation

Section 8.4.2 describes how to enter low-power sleep mode. When entering sleep mode, TI recommends setting all inputs as a logic low to minimize system power.

9.2.1.3 Application Curves

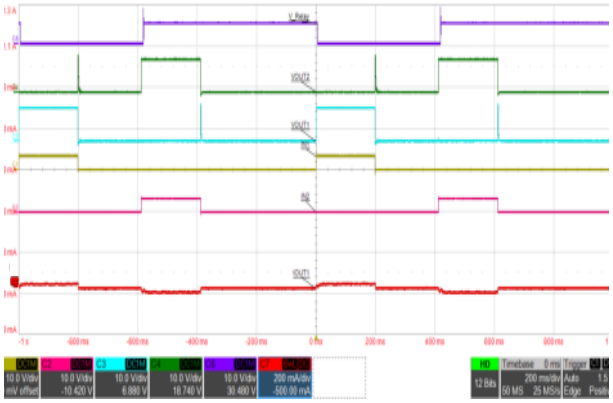


A. Channel 1 = IN1 Channel 2 = IN2 Channel 3 = OUT1 Channel 4 = OUT2

Figure 9-5. PWM driving for a motor with 50% duty cycle, INx and OUTx voltages

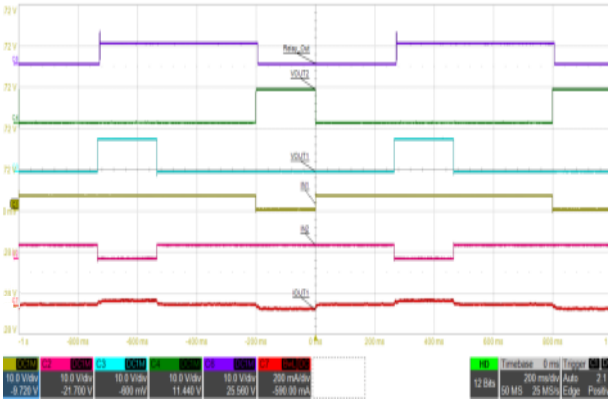
A. Channel 1 = IN1 Channel 2 = Motor Current Channel 3 = OUT1 Channel 4 = OUT2

Figure 9-6. PWM driving for a motor with 50% duty cycle, signals and motor current



A. Channel 1 = IN1 Channel 2 = IN2 Channel 3 = V_{OUT1} Channel 4 = V_{OUT2} Channel 6 = Relay Switch Channel 7 = Relay Coil Current

Figure 9-7. PWM driving for a single-coil latching relay with driving profile FORWARD → COAST → REVERSE → COAST



A. Channel 1 = IN1 Channel 2 = IN2 Channel 3 = V_{OUT1} Channel 4 = V_{OUT2} Channel 6 = Relay Switch Channel 7 = Relay Coil Current

Figure 9-8. PWM driving for a single-coil latching relay with driving profile FORWARD → BRAKE → REVERSE → BRAKE

9.2.2 Half-Bridge Driving

The DRV8210 can be configured to half-bridge mode by leaving the MODE pin floating. In this mode, the device outputs can be used as low-side or high-side drivers. This allows the device to drive various loads such as one or two motors unidirectionally (only in one direction), solenoids, valves, and relays. Figure 9-9 shows the device used as a low-side driver on OUT1 and high-side driver on OUT2. Both loads may also be driven from the high-side or from the low-side. By tying the INx pins together and OUTx pins together, as shown in Figure 9-10 and Figure 9-11, the device can drive a single load with half of the $R_{DS(on)}$. This can accommodate larger current requirements. This configuration is called "parallel half-bridge mode."

In half-bridge mode, the other FETs and body diodes in the half-bridge will recirculate freewheeling current during the off-time of the PWM duty cycle, so extra external diodes are not needed.

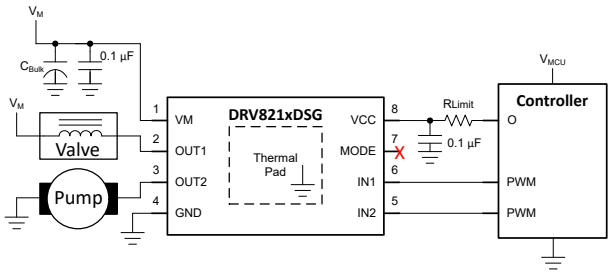


Figure 9-9. Half-bridge mode used as a high-side and low-side driver for two loads

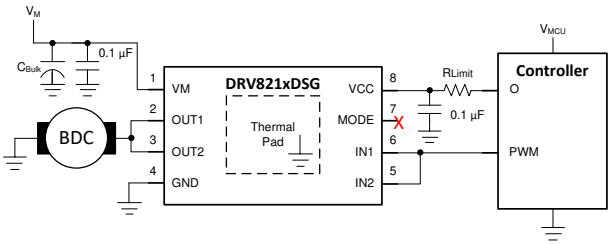


Figure 9-10. Half-bridge mode used as a high-side driver with outputs paralleled

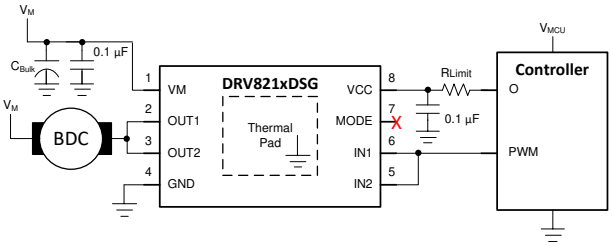


Figure 9-11. Half-bridge mode used as a low-side driver with outputs paralleled

Copyright © 2021 Texas Instruments Incorporated

9.2.2.1 Design Requirements

Table 9-2 lists the required parameters for the use case shown in Figure 9-9.

Table 9-2. System design requirements

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Load supply voltage	V_M	6 V
Logic supply voltage	V_{MCU}	3.3 V
Maximum valve current	I_{OUT1}	100 mA pulse for 100 ms
Maximum pump current	I_{OUT2}	600 mA, RMS

9.2.2.2 Detailed Design Procedure

9.2.2.2.1 Supply Voltage

The appropriate supply voltage depends on the ratings of the load.

9.2.2.2.2 Control Interface

Section 8.3.2.3 describes the half-bridge control interface for the DSG package.

9.2.2.2.3 Low-Power Operation

Bringing VCC to 0 V puts the DRV8210 to sleep in half-bridge mode. Section 8.4.2 describes how to enter low-power sleep mode in detail. When entering sleep mode, TI recommends setting all inputs as a logic low to minimize system power. To wake up the DRV8210 in half-bridge mode, bring VCC high, then set IN1 or IN2 high for longer than t_{WAKE} before returning low or sending a PWM signal. Figure 9-19 and Figure 9-20 show this wakeup procedure.

Because of the decoupling capacitor on the VCC pin, TI recommends adding a resistor between the GPIO pin of the controller and the VCC pin as shown in Figure 9-9, Figure 9-10, and Figure 9-11. The purpose of this resistor is to protect the GPIO pin from large currents from the capacitor when switching the GPIO pin. However, this resistor must be sized appropriately to allow the operating current, I_{VCC}, to flow into the VCC pin. Table 9-3 shows the design considerations for the R_{LIMIT} resistor. V_{OL} is the GPIO voltage when logic low, V_{OH} is the GPIO voltage when logic high, and I_{OL} is the maximum current that the GPIO can sink. The controller datasheet should specify V_{OL}, V_{OH} and I_{OL} for the GPIO pin.

Table 9-3. GPIO pin current limiting resistor design requirements

Design consideration	Equation	Example
Minimum resistance needed to protect GPIO pin. Here, V_{Cap} is the voltage on the capacitor when the GPIO pin switches from high to low. To simplify calculation and assume a worst-case condition, V_{Cap} is assumed to be equivalent to the controller supply voltage, V_{MCU}. See Figure 9-12 for example circuit.	$R_{Limit} \geq (V_{Cap} - V_{OL}) / I_{OL}$	$R_{Limit} \geq (3.3\ V - 0.3\ V) / 24\ mA = 125\ \Omega$
Keep the VCC pin voltage high enough so device does not go into undervoltage lockout. See Figure 9-13 for example circuit.	$V_{OH} - (I_{VCC} \times R_{Limit}) = V_{VCC} \geq 1.65\ V$	$3.0\ V - (3.6\ mA \times 125\ \Omega) = 2.55\ V \geq 1.65\ V$

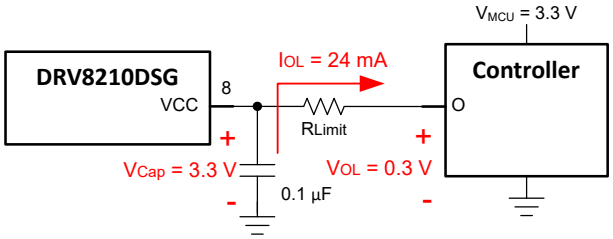


Figure 9-12. GPIO current when switching output from logic high to logic low

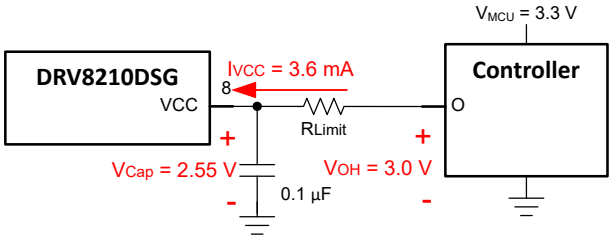


Figure 9-13. GPIO current with logic high output when $V_{VCC} > V_{VM}$

In cases where the specified GPIO current is too small, there are a few other options to put the device to sleep. One option is to parallel multiple GPIO to supply the appropriate current. A second option is to set MODE = IN1 = IN2 = 0 to put the device into the autosleep state. This will require the GPIO pin that controls MODE to be configured as an input during operation and an output low during sleep. A third option is to place a GPIO-controlled transistor between the supply and the VCC pin as shown in Figure 9-14.

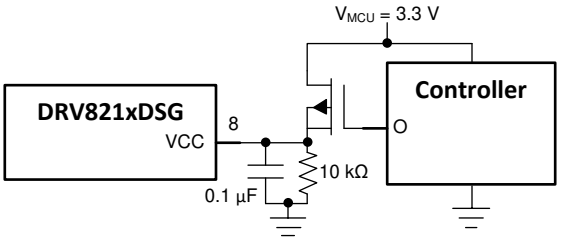


Figure 9-14. GPIO with transistor

To minimize leakage current into the OUTx pins (especially in battery-powered applications), connect the load from OUTx to GND. As mentioned earlier, connecting the load from OUTx to VM is also possible, but there may be some small leakage current into OUTx when it is disabled. No leakage current is expected if loads are connected in H-bridge configuration.

9.2.2.3 Application Curves

The figures below show waveform examples of high-side and low-side driving in half-bridge mode. Figure 9-15 and Figure 9-16 show example waveforms of driving a motor unidirectionally using high-side and low-side driving. Figure 9-17 and Figure 9-18 show example waveforms of driving a solenoid using high-side and low-side driving. Figure 9-19 and Figure 9-20 show examples of driving a motor using high-side and low-side driving when the OUTx pins are paralleled together to create a single half bridge.

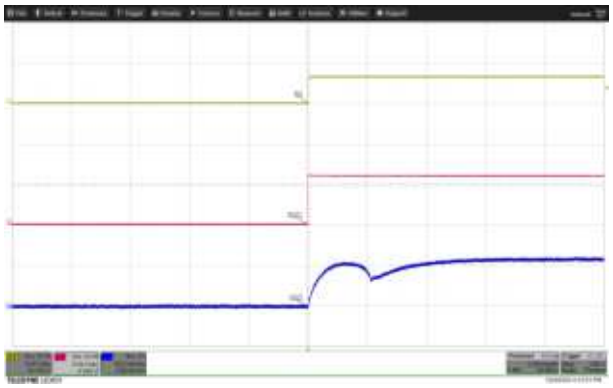
Copyright © 2021 Texas Instruments Incorporated

A. Channel 1 = IN2 Channel 2 = V_{OUT2} Channel 4 = Motor Current

Figure 9-15. Driving a motor in half-bridge mode with 50% duty cycle using the high-side FET

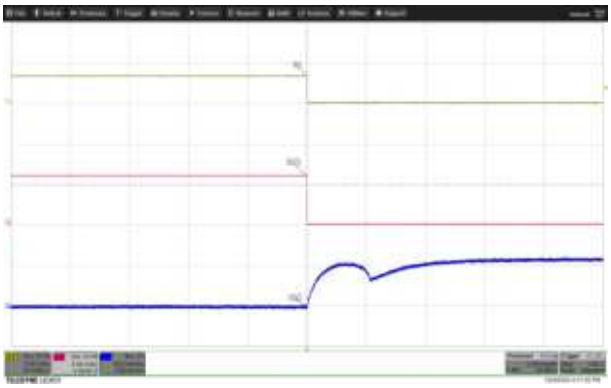
A. Channel 1 = IN2 Channel 2 = V_{OUT2} Channel 4 = Motor Current

Figure 9-16. Driving a motor in half-bridge mode with 50% duty cycle using the low-side FET



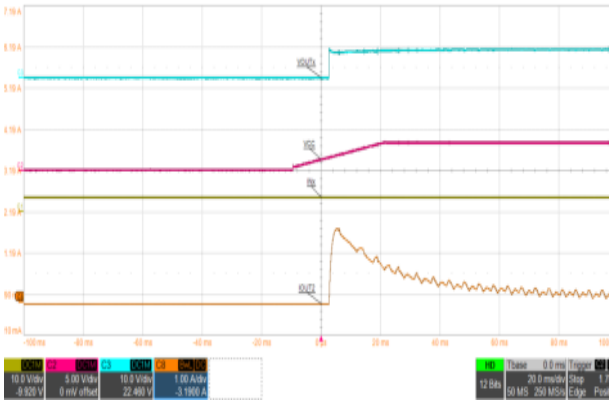
A. Channel 1 = IN1 Channel 2 = V_{OUT1} Channel 4 = Solenoid Current

Figure 9-17. Driving a solenoid in half-bridge mode using the high-side FET



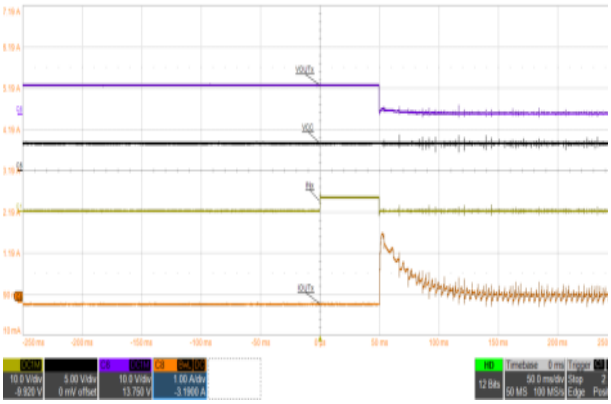
A. Channel 1 = IN1 Channel 2 = V_{OUT1} Channel 4 = Solenoid Current

Figure 9-18. Driving a solenoid in half-bridge mode using the low-side FET



A. Channel 1 = IN1, IN2 (paralleled) Channel 2 = V_{VCC} Channel 3 = V_{OUT} (OUT1/2 paralleled) Channel 8 = Motor Current

Figure 9-19. Driving a motor in parallel half-bridge mode using the high-side FETs



A. Channel 1 = IN1, IN2 (paralleled) Channel 5 = V_{VCC} Channel 6 = V_{OUT} (OUT1/2 paralleled) Channel 8 = Motor Current

Figure 9-20. Driving a motor in parallel half-bridge mode using the low-side FETs

9.2.3 Dual-Coil Relay Driving

The PWM interface may also be used to drive a dual-coil latching relay. The figures in this section show example schematics.

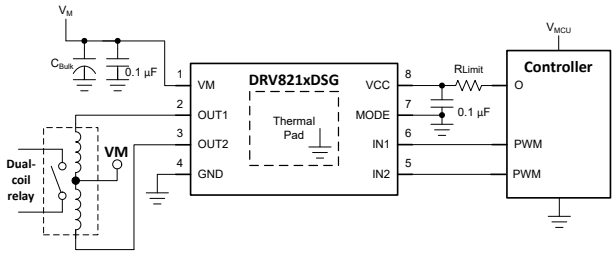


Figure 9-21. Dual-coil relay driving, DSG package

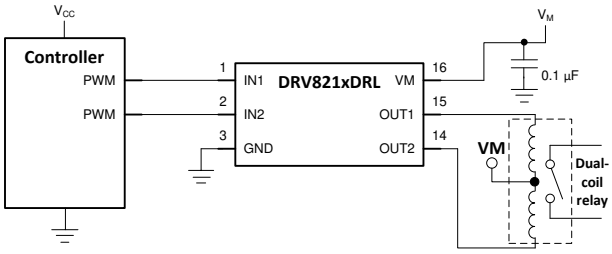


Figure 9-22. Dual-coil relay driving, DRL package

9.2.3.1 Design Requirements

Table 9-4 provides example requirements for a dual-coil relay application.

Table 9-4. System design requirements

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Motor supply voltage	V_M	6 V
Logic supply voltage	V_{CC}	3.3 V
Relay current	I_{OUT1}, I_{OUT2}	500 mA pulse for 100 ms

9.2.3.2 Detailed Design Procedure

9.2.3.2.1 Supply Voltage

The appropriate supply voltage depends on the ratings of the load.

9.2.3.2.2 Control Interface

The PWM interface can be used to drive dual-coil relays. Section 8.3.2.1 describes the PWM control interface. Figure 9-23 and Figure 9-24 show a schematic and timing diagram for driving a dual-coil relay with the PWM interface.

Copyright © 2021 Texas Instruments Incorporated

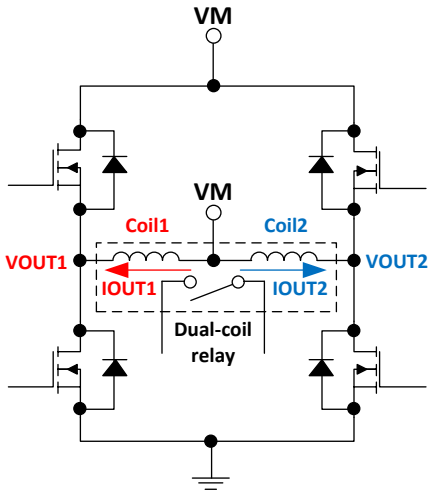


Figure 9-23. Schematic of dual-coil relay driven by the OUTx H-bridge

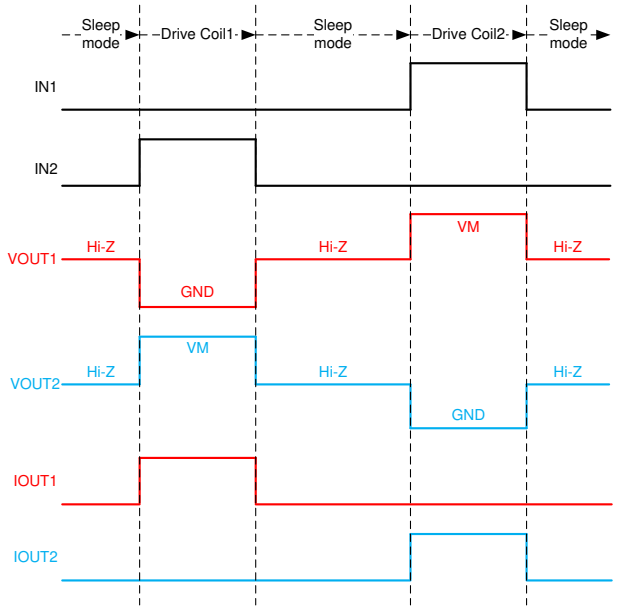


Figure 9-24. Timing diagram for driving a dual-coil relay with PWM interface

Table 9-5 shows the logic table for the PWM interface. The descriptions in this table reflect how the input and output states drive the dual coil relay. When Coil1 is driven (OUT1 voltage is at GND), The voltage at OUT2 will go to VM. Because the center tap of the relay is also at VM, no current flows through Coil2. The same is true when Coil2 is driven; Coil1 shorts to VM. The body diodes of the high-side FETs act as freewheeling diodes, so extra external diodes are not needed. Figure 9-25 shows oscilloscope traces for this application.

Table 9-5. PWM control table for dual-coil relay driving

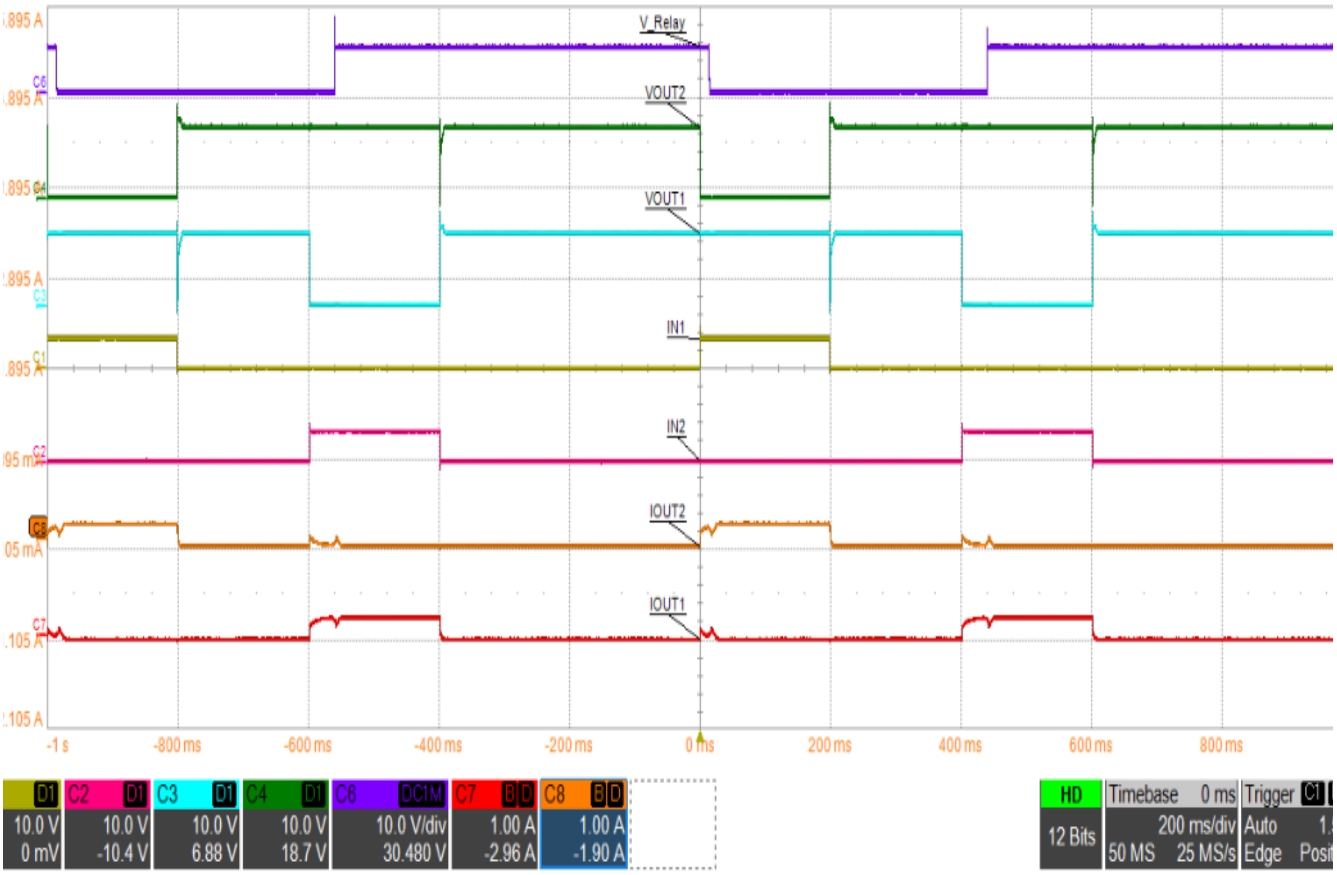
IN1	IN2	OUT1	OUT2	DESCRIPTION
0	0	Hi-Z	Hi-Z	Outputs disabled (H-Bridge Hi-Z)
0	1	L	H	Drive Coil1
1	0	H	L	Drive Coil2
1	1	L	L	Drive Coil1 and Coil2 (invalid state for a dual-coil latching relay)

9.2.3.2.3 Low-Power Operation

Section 8.4.2 describes how to enter low-power sleep mode. When entering sleep mode, TI recommends setting all inputs as a logic low to minimize system power.

To minimize leakage current into the OUTx pins (especially in battery-powered applications), connect the load from OUTx to GND. As shown in the previous section, connecting the load from OUTx to VM is also possible, but there may be some small leakage current into OUTx when it is disabled.

9.2.3.3 Application Curves



A. Channel 1 = IN1 Channel 2 = IN2 Channel 3 = V_{OUT1}

Channel 4 = V_{OUT2} Channel 6 = Relay Switch Channel 7 = Relay Coil1 Current

Channel 8 = Relay Coil2 Current

Figure 9-25. PWM driving for dual-coil relay

9.2.4 Current Sense

A small shunt resistor on the GND pin can provide current sense information back to the microcontroller ADC. The microcontroller can use this information to detect motor load conditions, such as stall. Figure 9-26 shows an example schematic using the DRL package. If better current sensing dynamic range is needed, an amplifier can be added as shown in Figure 9-27.

The DSG thermal pad may be connected to the board ground net or the GND pin/sense signal net.

Copyright © 2021 Texas Instruments Incorporated

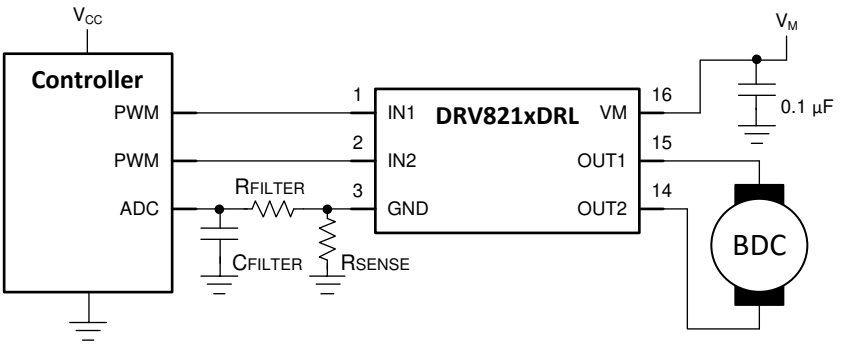


Figure 9-26. Shunt resistor on GND pin of the DRL package variant

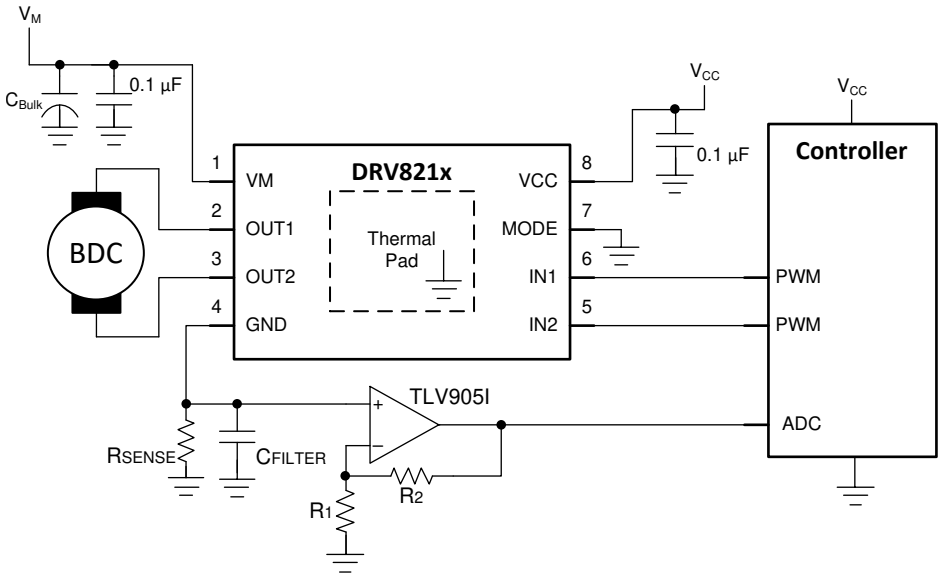


Figure 9-27. Current sense amplifier example

9.2.4.1 Design Requirements

Table 9-6 provides example requirements for a current sensing application.

Table 9-6. System design requirements

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Motor supply voltage	V_M	6 V
Logic supply voltage	V_{CC}	3.3 V
Maximum voltage across R_{SENSE}	V_{SENSE}	150 mV
Motor RMS current	I_{OUT1}, I_{OUT2}	500 mA
Motor stall current	$I_{OUT1,stall}$, $I_{OUT2,stall}$	1 A

9.2.4.2 Detailed Design Procedure

9.2.4.2.1 Shunt Resistor Sizing

The Absolute Maximum Ratings for the INx pins set the maximum voltage across the shunt resistor. If the signal on the INx pin is low, referenced at the board ground, then the INx pins are at a negative voltage with respect to the GND pin voltage. This sets the maximum sense voltage/GND pin voltage to 0.5 V. Figure 9-28 shows the relative pin voltages.

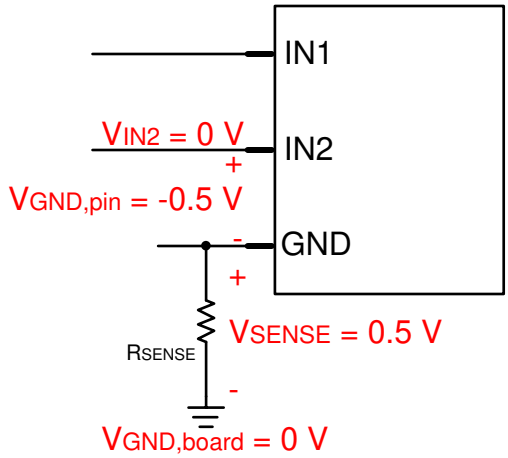


Figure 9-28. Pin voltages with respect to board ground using current sense resistor

This example uses 150 mV for the maximum V_{SENSE}, which is less than 0.5 V and provides some margin for safety or error. The maximum current through the motor will be the stall current, which is 1 A for this example. With this information, the sense resistance R_{SENSE} can be calculated from the equation below.

$$R_{SENSE} = V_{SENSE} / I_{STALL} = 0.15 / 1 = 0.15\ \Omega \quad (1)$$

Because the device GND pin voltage will vary with current through the sense resistor, the designers must also ensure that the logic pins meet V_{IL} and V_{IH} parameters,the MODE pin meets the V_{TIL}, V_{TIZ}, and V_{TIH} parameters, and the supply remains above V_{UVLO} for proper operation.

9.2.4.2.2 RC Filter

The RC filter shown in Figure 9-26 is used to filter noise and transients from the sense signal. TI recommends R_{FILTER} = 1 kΩ and C_{FILTER} = 100 nF. Different values can be chosen depending on the specific system conditions.

9.3 Current Capability and Thermal Performance

The output current and power dissipation capabilities of the driver depends heavily on the PCB design and external system conditions. This section provides some guidelines for calculating these values.

9.3.1 Power Dissipation and Output Current Capability

Total power dissipation for the device consists of three main components: quiescent supply current dissipation (P_{VM} and P_{VCC}), the power MOSFET switching losses (P_{SW}), and the power MOSFET $R_{DS(on)}$ (conduction) losses (P_{RDS}). While other factors may contribute additional power losses, they are typically insignificant compared to the three main items.

$$P_{TOT} = P_{VM} + P_{VCC} + P_{SW} + P_{RDS} \quad (2)$$

P_{VM} can be calculated from the nominal motor supply voltage (V_{VM}) and the I_{VM} active mode current specification. P_{VCC} can be calculated from the nominal logic supply voltage (V_{VCC}) and the I_{VCC} active mode current specification. When $V_{VCC} < V_{VM}$, the DRV8210 draws active current from the VM pin rather than the VCC pin. During this operating condition, I_{VCC} is typically less than 500 nA (see Figure 7-5 and Figure 7-7).

$$P_{VM} = V_{VM} \times I_{VM} \quad (3)$$

$$P_{VM} = 7\ \text{mW} = 5\ \text{V} \times 1.4\ \text{mA} \quad (4)$$

$$P_{VCC} = V_{VCC} \times I_{VCC} \quad (5)$$

$$P_{VCC} = 0.594\ \text{mW} = 3.3\ \text{V} \times 0.18\ \text{mA} \quad (6)$$

Copyright © 2021 Texas Instruments Incorporated

P_{SW} can be calculated from the nominal motor supply voltage (V_{VM}), average output current (I_{RMS}), switching frequency (f_{PWM}) and the device output rise (t_{RISE}) and fall (t_{FALL}) time specifications.

$$P_{SW} = P_{SW_RISE} + P_{SW_FALL} \quad (7)$$

$$P_{SW_RISE} = 0.5 \times V_M \times I_{RMS} \times t_{RISE} \times f_{PWM} \quad (8)$$

$$P_{SW_FALL} = 0.5 \times V_M \times I_{RMS} \times t_{FALL} \times f_{PWM} \quad (9)$$

$$P_{SW_RISE} = 3.75\ \text{mW} = 0.5 \times 5\ \text{V} \times 0.5\ \text{A} \times 150\ \text{ns} \times 20\ \text{kHz} \quad (10)$$

$$P_{SW_FALL} = 3.75\ \text{mW} = 0.5 \times 5\ \text{V} \times 0.5\ \text{A} \times 150\ \text{ns} \times 20\ \text{kHz} \quad (11)$$

$$P_{SW} = 7.5\ \text{mW} = 3.75\ \text{mW} + 3.75\ \text{mW} \quad (12)$$

P_{RDS} can be calculated from the device $R_{DS(on)}$ and average output current (I_{RMS}).

$$P_{RDS} = I_{RMS}^{\ 2} \times (R_{DS(ON)_HS} + R_{DS(ON)_LS}) \quad (13)$$

$R_{DS(ON)}$ has a strong correlation with the device temperature. Assuming a device junction temperature of 85 °C, $R_{DS(on)}$ could increase ~1.5x based on the normalized temperature data. The calculation below shows this derating factor. Alternatively, the Section 7.6 section shows curves that plot how $R_{DS(on)}$ changes with temperature.

$$P_{RDS} = 394\ \text{mW} = (0.5\ \text{A})^2 \times (525\ \text{m}\Omega \times 1.5 + 525\ \text{m}\Omega \times 1.5) \quad (14)$$

Based on the example calculations above, the expressions below calculate the total expected power dissipation for the device.

$$P_{TOT} = P_{VM} + P_{VCC} + P_{SW} + P_{RDS} \quad (15)$$

$$P_{TOT} = 409\ \text{mW} = 7\ \text{mW} + 0.594\ \text{mW} + 7.5\ \text{mW} + 394\ \text{mW} \quad (16)$$

The driver's junction temperature can be estimated using P_{TOT}, device ambient temperature (T_A), and package thermal resistance ($R_{\theta JA}$). The value for $R_{\theta JA}$ depends heavily on the PCB design and copper heat sinking around the device. Section 9.3.2 describes this dependence in greater detail.

$$T_J = (P_{TOT} \times R_{\theta JA}) + T_A \quad (17)$$

$$T_J = 126°\text{C} = (0.409\ \text{W} \times 99.6\ °\text{C/W}) + 85°\text{C} \quad (18)$$

The device junction temperature should remain below its absolute maximum rating for all system operating conditions. The calculations in this section provide reasonable estimates for junction temperature. However, other methods based on temperature measurements taken during system operation are more realistic and reliable. Additional information on motor driver current ratings and power dissipation can be found in Section 9.3.2 and Section 12.1.1.

9.3.2 Thermal Performance

The datasheet-specified junction-to-ambient thermal resistance, $R_{\theta JA}$, is primarily useful for comparing various drivers or approximating thermal performance. However, the actual system performance may be better or worse than this value depending on PCB stackup, routing, number of vias, and copper area around the thermal pad. The length of time the driver drives a particular current will also impact power dissipation and thermal performance. This section considers how to design for steady-state and transient thermal conditions.

The data in this section was simulated using the following criteria:

WSON (DSG package)

- 2-layer PCB, standard FR4, 1-oz (35 mm copper thickness) or 2-oz copper thickness. Thermal vias are only present under the thermal pad (2 vias, 1.2mm spacing, 0.3 mm diameter, 0.025 mm Cu plating).

  - Top layer: DRV8210 WSON package footprint and copper plane heatsink. Top layer copper area is varied in simulation.
  - Bottom layer: ground plane thermally connected through vias under the thermal pad for DRV8210. Bottom layer copper area varies with top copper area.
- 4-layer PCB, standard FR4. Outer planes are 1-oz (35 mm copper thickness) or 2-oz copper thickness. Inner planes are kept at 1-oz. Thermal vias are only present under the thermal pad (2 vias, 1.2mm spacing, 0.3 mm diameter, 0.025 mm Cu plating).
  - Top layer: DRV8210 WSON package footprint and copper plane heatsink. Top layer copper area is varied in simulation.
  - Mid layer 1: GND plane thermally connected to DRV8210 thermal pad through vias. The area of the ground plane is 74.2 mm x 74.2 mm.
  - Mid layer 2: power plane, no thermal connection. The area of the power plane is 74.2 mm x 74.2 mm.
  - Bottom layer: signal layer with small copper pad underneath DRV8210 and thermally connected through via stitching from the TOP and internal GND planes. Bottom layer thermal pad is the same size as the package (2 mm x 2 mm). Bottom pad size remains constant as top copper plane is varied.

Figure 9-29 shows an example of the simulated board for the HTSSOP package. Table 9-7 shows the dimensions of the board that were varied for each simulation.

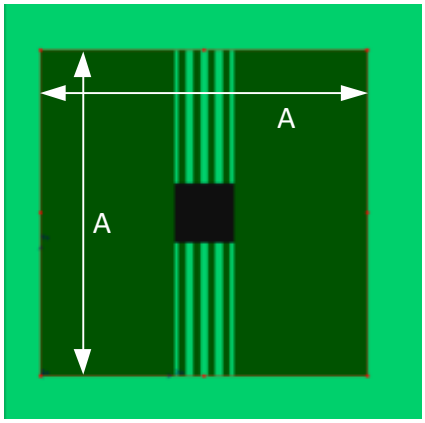


Figure 9-29. WSON PCB model top layer

Table 9-7. Dimension A for 16-pin PWP package

Cu area (mm^2)	Dimension A (mm)
2	15.11
4	20.98
8	29.27
16	40.99

SOT (DRL package)

- 2-layer PCB, standard FR4, 1-oz (35 mm copper thickness) or 2-oz copper thickness. Thermal vias are only present under the package footprint (2 vias, 1.2mm spacing, 0.3 mm diameter, 0.025 mm Cu plating).
  - Top layer: DRV8210 SOT package footprint and copper plane heatsink. Top layer copper area is varied in simulation.
  - Bottom layer: ground plane thermally connected through vias under the DRV8210DRL package footprint. Bottom layer copper area varies with top copper area.
- 4-layer PCB, standard FR4. Outer planes are 1-oz (35 mm copper thickness) or 2-oz copper thickness. Inner planes are kept at 1-oz. Thermal vias are only present under the DRV8210DRL package footprint (2 vias, 1.2mm spacing, 0.3 mm diameter, 0.025 mm Cu plating).
  - Top layer: DRV8210 SOT package footprint and copper plane heatsink. Top layer copper area is varied in simulation.

Copyright © 2021 Texas Instruments Incorporated

- Mid layer 1: GND plane thermally connected under DRV8210DRL package footprint through vias. The area of the ground plane is 74.2 mm x 74.2 mm.
- Mid layer 2: power plane, no thermal connection. The area of the power plane is 74.2 mm x 74.2 mm.
- Bottom layer: signal layer with small copper pad underneath DRV8210DRL and thermally connected through via stitching from the TOP and internal GND planes. Bottom layer thermal pad is the same size as the package (1.2 mm x 1.6 mm). Bottom pad size remains constant as top copper plane is varied.

Figure 9-30 shows an example of the simulated board for the HTSSOP package. Table 9-8 shows the dimensions of the board that were varied for each simulation.

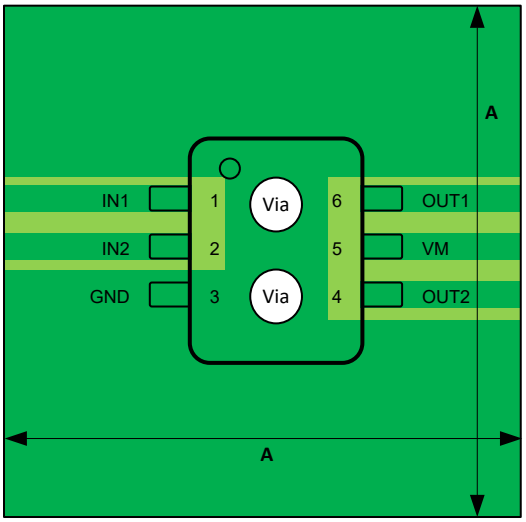


Figure 9-30. SOT PCB model top layer

Table 9-8. Dimension A for 16-pin PWP package

Cu area (mm^2)	Dimension A (mm)
2	15.11
4	20.98
8	29.27
16	40.99

9.3.2.1 Steady-State Thermal Performance

"Steady-state" conditions assume that the motor driver operates with a constant RMS current over a long period of time. The figures in this section show how $R_{\theta JA}$ and Ψ_{JB} (junction-to-board characterization parameter) change depending on copper area, copper thickness, and number of layers of the PCB. More copper area, more layers, and thicker copper planes decrease $R_{\theta JA}$ and Ψ_{JB}, which indicate better thermal performance from the PCB layout.

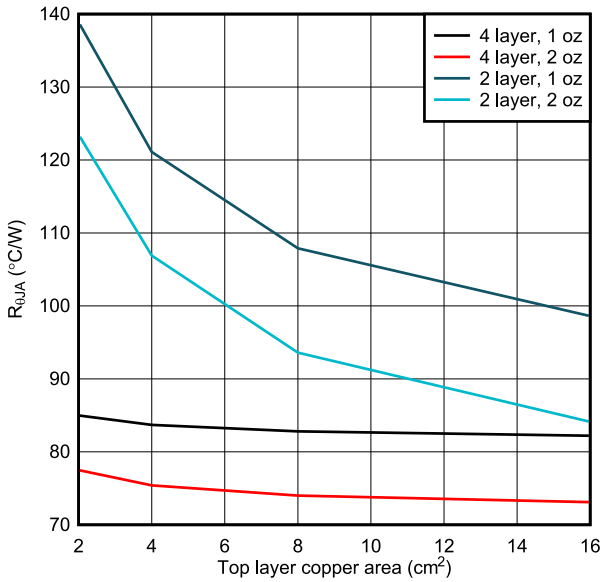


Figure 9-31. WSON, PCB junction-to-ambient thermal resistance vs copper area

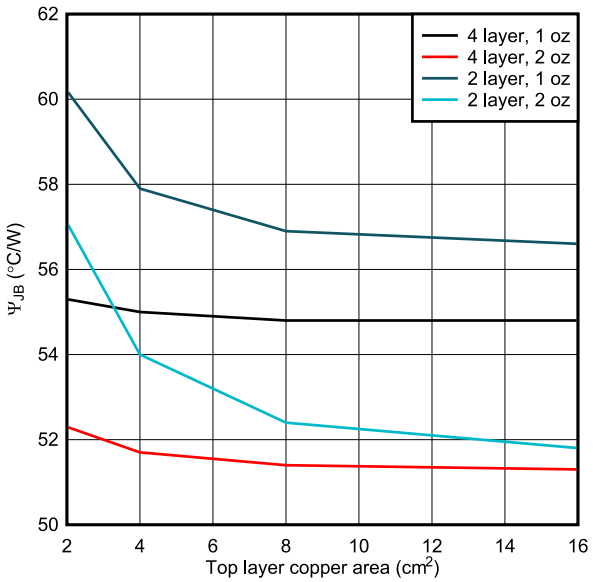


Figure 9-32. WSON, junction-to-board characterization parameter vs copper area

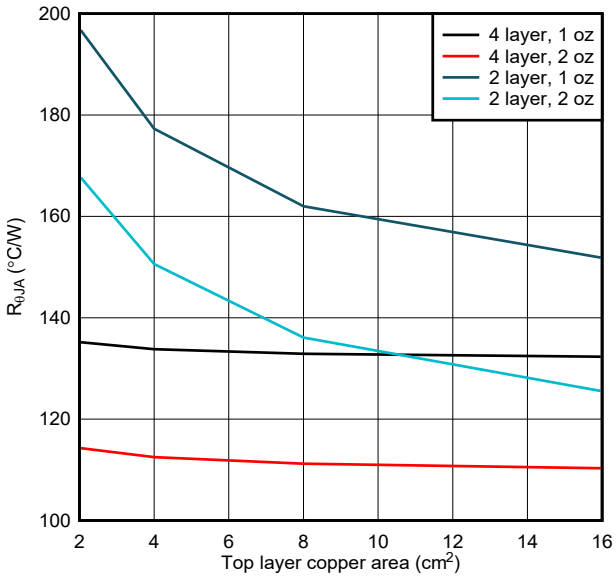


Figure 9-33. SOT, PCB junction-to-ambient thermal resistance vs copper area

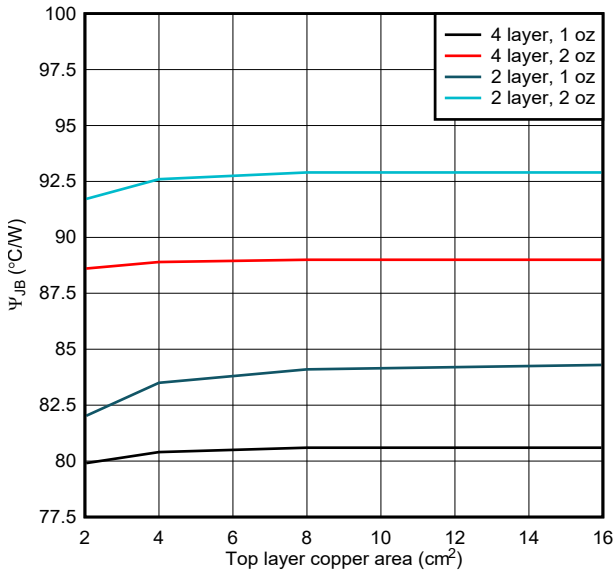


Figure 9-34. SOT, junction-to-board characterization parameter vs copper area

9.3.2.2 Transient Thermal Performance

The motor driver may experience different transient driving conditions that cause large currents to flow for a short duration of time. These may include

- Motor start-up when the rotor is initially stationary.
- Fault conditions when there is a supply or ground short to one of the motor outputs, and the overcurrent protection triggers.
- Briefly energizing a motor or solenoid for a limited time, then de-energizing.

For these transient cases, the duration of drive time is another factor that impacts thermal performance in addition to copper area and thickness. In transient cases, the thermal impedance parameter $Z_{\theta JA}$ denotes the

Copyright © 2021 Texas Instruments Incorporated

junction-to-ambient thermal performance. The figures in this section show the simulated thermal impedances for 1-oz and 2-oz copper layouts for the WSON and SOT packages. These graphs indicate better thermal performance with short current pulses. For short periods of drive time, the device die size and package dominates the thermal performance. For longer drive pulses, board layout has a more significant impact on thermal performance. Both graphs show the curves for thermal impedance split due to number of layers and copper area as the duration of the drive pulse duration increases. Long pulses can be considered steady-state performance.

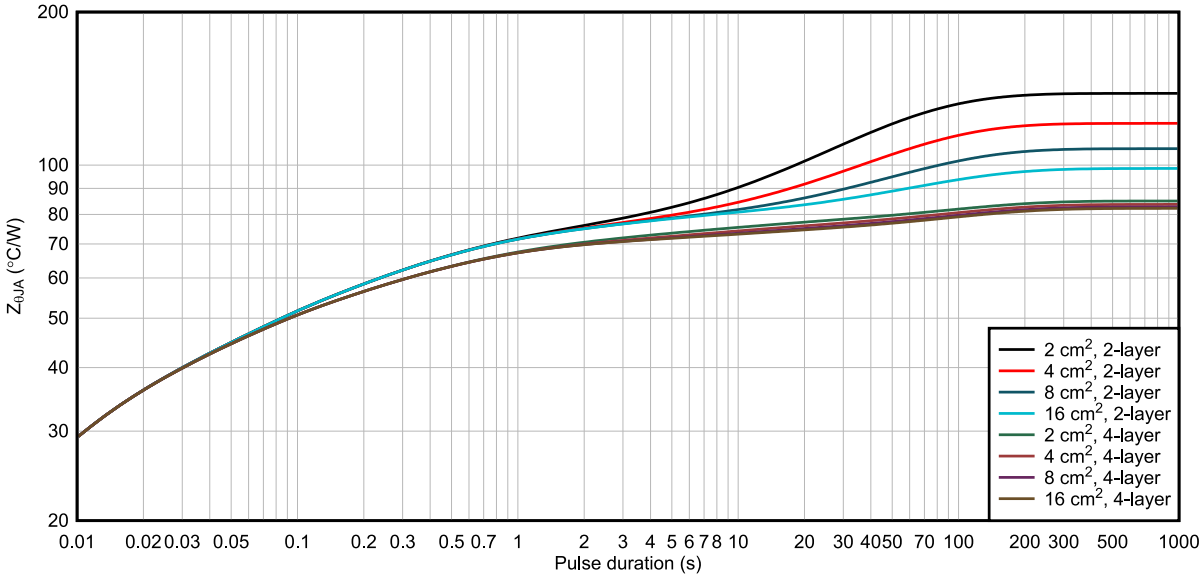


Figure 9-35. WSON package junction-to-ambient thermal impedance for 1-oz copper layouts

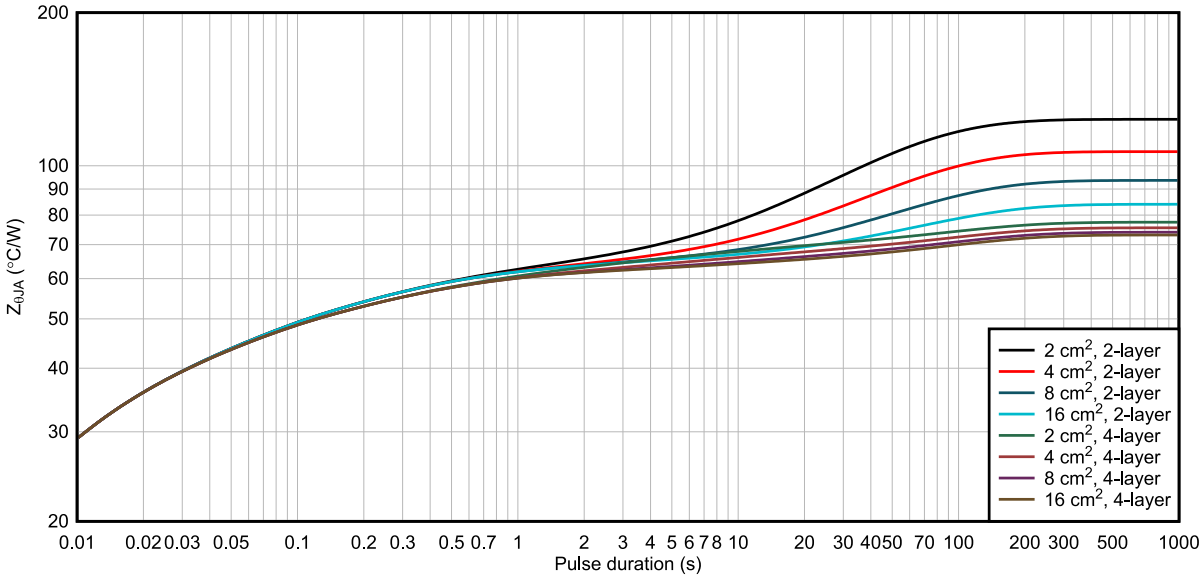


Figure 9-36. WSON package junction-to-ambient thermal impedance for 2-oz copper layouts

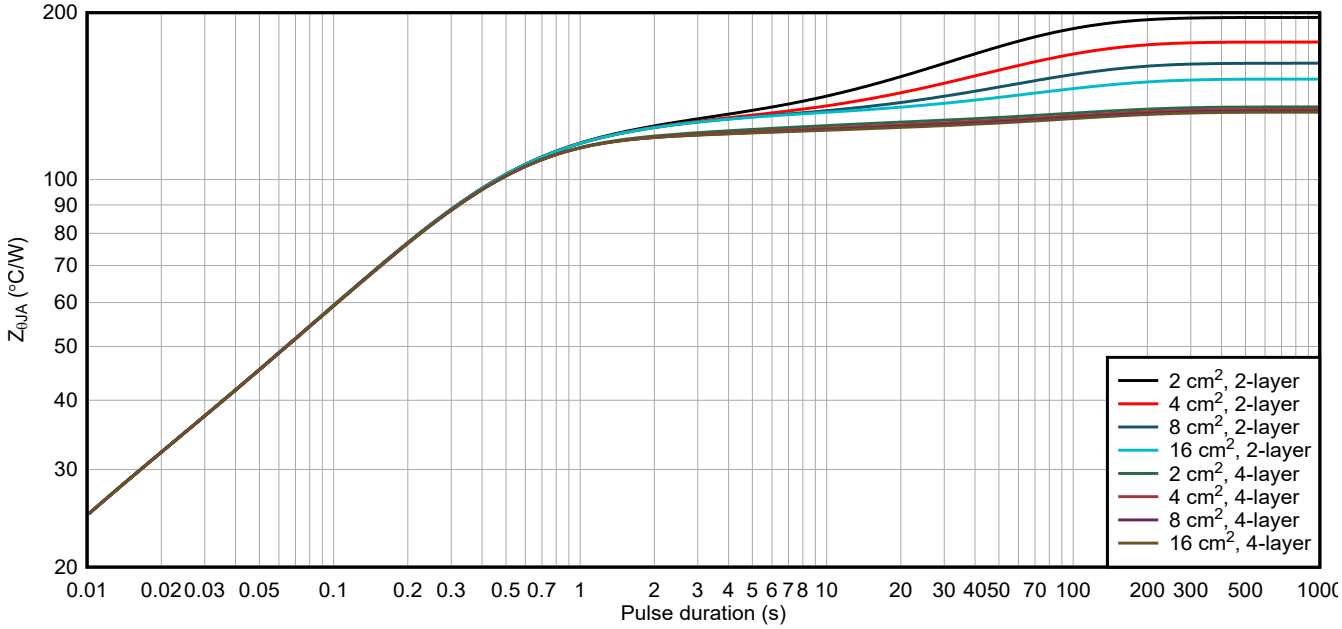


Figure 9-37. SOT package junction-to-ambient thermal impedance for 1-oz copper layouts

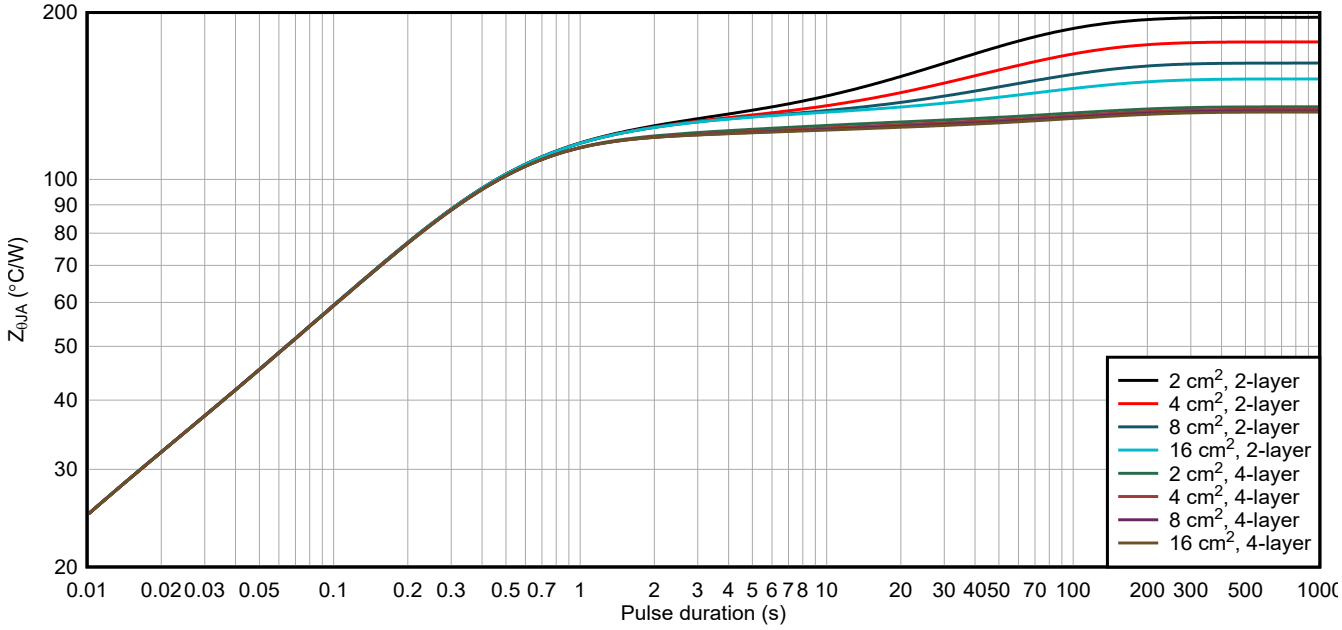


Figure 9-38. SOT package junction-to-ambient thermal impedance for 2-oz copper layouts

Copyright © 2021 Texas Instruments Incorporated

10 Power Supply Recommendations

10.1 Bulk Capacitance

Having appropriate local bulk capacitance is an important factor in motor drive system design. Having more bulk capacitance is generally beneficial, while the disadvantages are increased cost and physical size.

The amount of local bulk capacitance needed depends on a variety of factors, including:

- The highest current required by the motor or load
- The capacitance of the power supply and ability to source current
- The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripple of the system
- The motor braking method (if applicable)

The inductance between the power supply and motor drive system limits how the rate current can change from the power supply. If the local bulk capacitance is too small, the system responds to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended minimum value, but system level testing is required to determine the appropriately sized bulk capacitor.

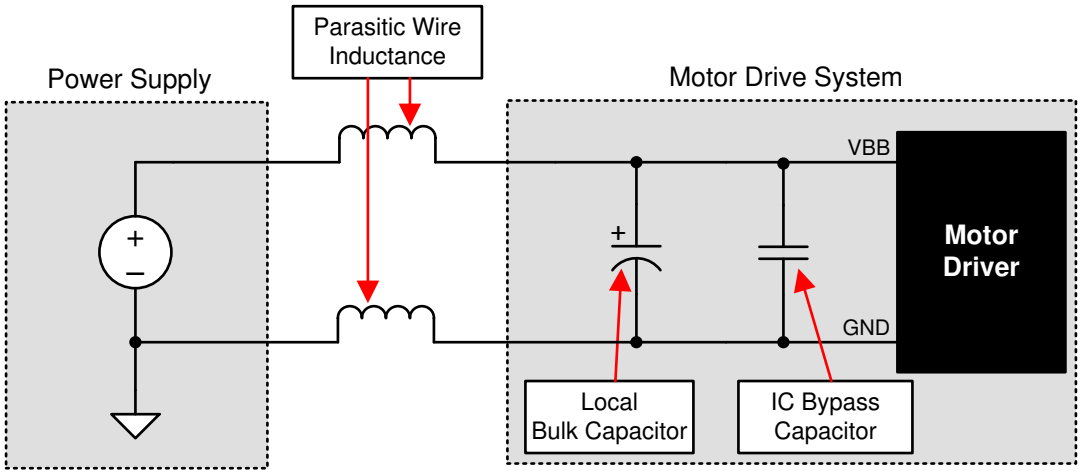


Figure 10-1. System Supply Parasitics Example

11 Layout

11.1 Layout Guidelines

Since the DRV8210 device has integrated power MOSFETs capable of driving high current, careful attention should be paid to the layout design and external component placement. Some design and layout guidelines are provided below. For more information on layout recommendations, please see the application note *Best Practices for Board Layout of Motor Drivers*.

- Low ESR ceramic capacitors should be utilized for the VM-to-GND and VCC-to-GND bypass capacitors. X5R and X7R types are recommended.
- The VM and VCC power supply capacitors should be placed as close to the device as possible to minimize the loop inductance.
- The VM power supply bulk capacitor can be of ceramic or electrolytic type, but should also be placed as close as possible to the device to minimize the loop inductance.
- VM, OUT1, OUT2, and GND carry the high current from the power supply to the outputs and back to ground. Thick metal routing should be utilized for these traces as is feasible.
- GND should connect directly on the PCB ground plane.
- The device thermal pad should be attached to the PCB top layer ground plane and internal ground plane (when available) through thermal vias to maximize the PCB heat sinking.
- The copper plane area attached to the thermal pad should be maximized to ensure optimal heat sinking.

11.2 Layout Example

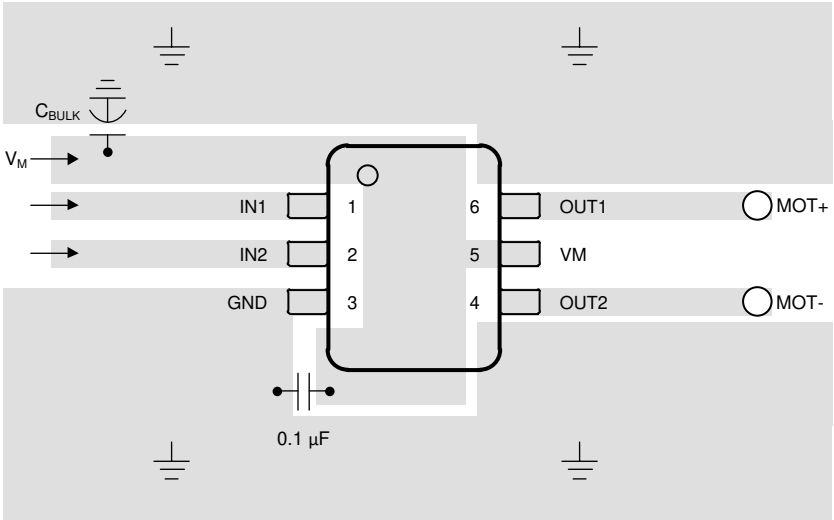


Figure 11-1. Simplified Layout Example of DRL Package without Vias

Copyright © 2021 Texas Instruments Incorporated

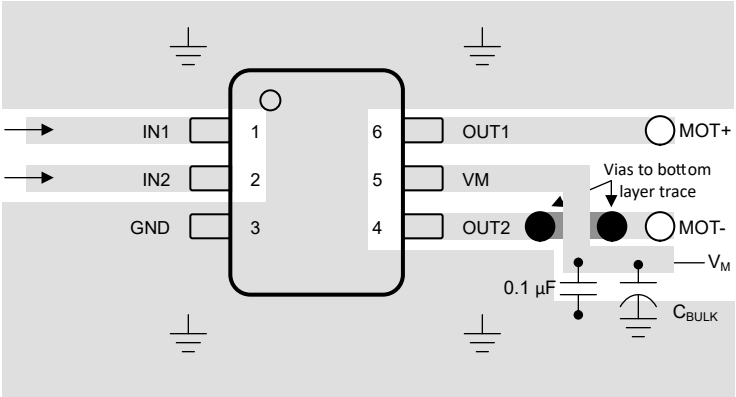


Figure 11-2. Simplified Layout Example of DRL Package with Larger Copper Area for Better Thermal Dissipation

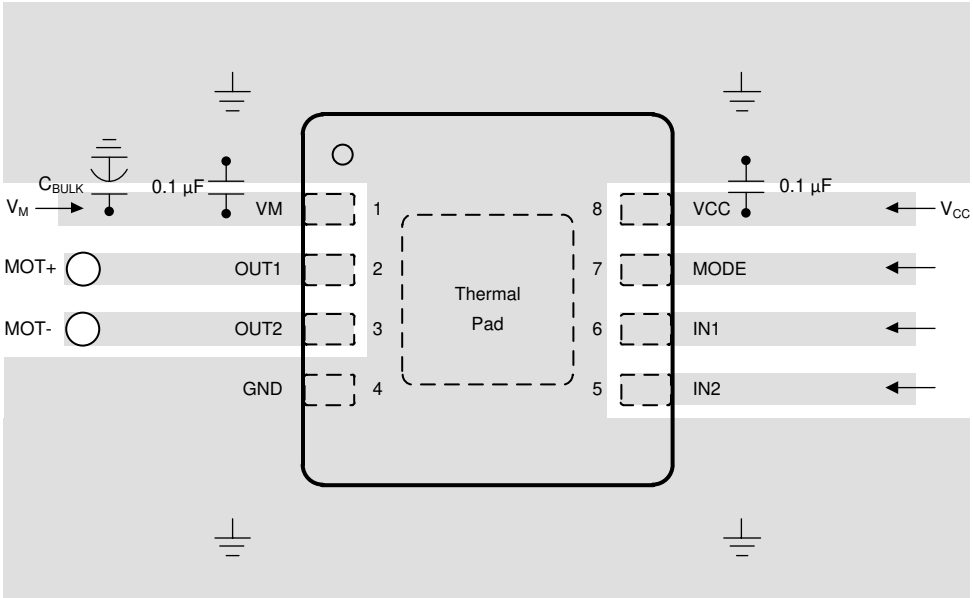


Figure 11-3. Simplified Layout Example for DSG package

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Calculating Motor Driver Power Dissipation* application report
- Texas Instruments, *PowerPAD™ Made Easy application report* application report
- Texas Instruments, *PowerPAD™ Thermally Enhanced Package* application report
- Texas Instruments, *Understanding Motor Driver Current Ratings* application report
- Texas Instruments, *Best Practices for Board Layout of Motor Drivers* application report

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

Copyright © 2021 Texas Instruments Incorporated

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DRV8210DRLR	Active	Production	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	Yes	Call TI | Sn	Level-1-260C-UNLIM	-40 to 125	8210
DRV8210DRLR.A	Active	Production	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	8210
DRV8210DSGR	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	210
DRV8210DSGR.A	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	210
DRV8210DSGRG4	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	210
DRV8210DSGRG4.A	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	210

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

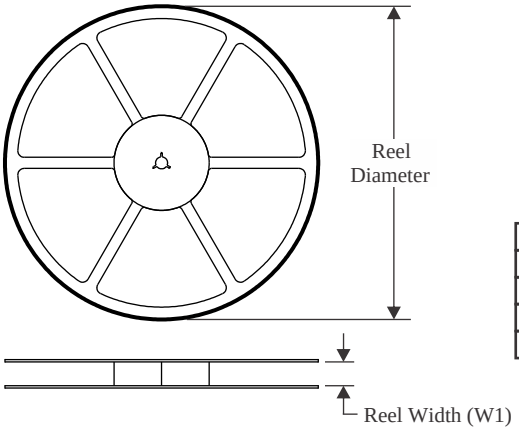
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

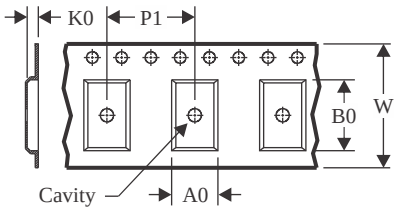
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

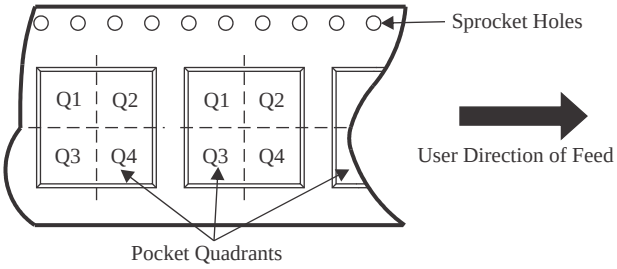


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

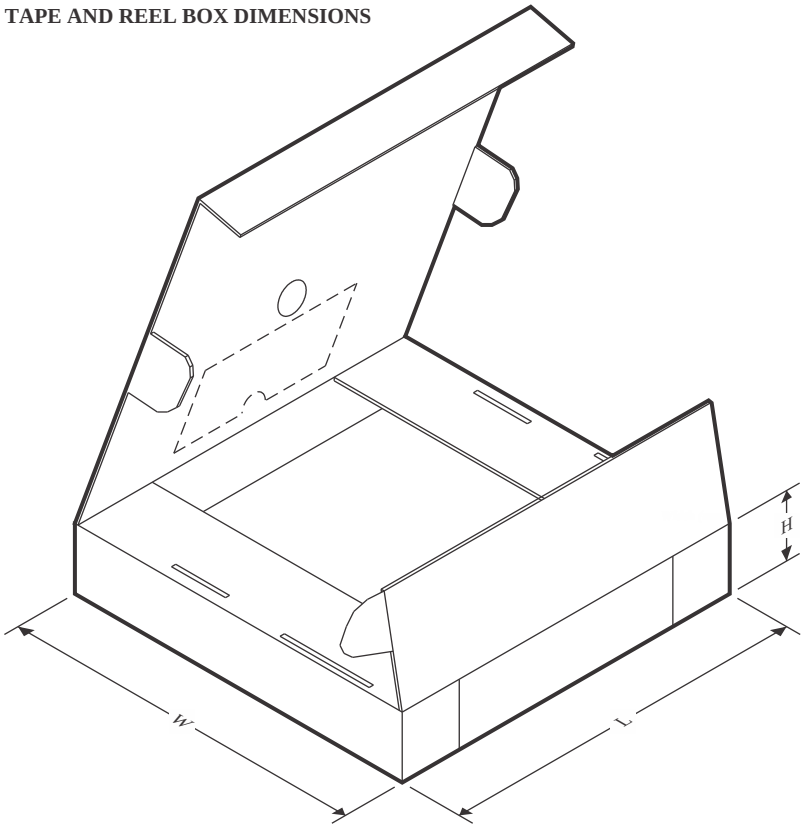
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

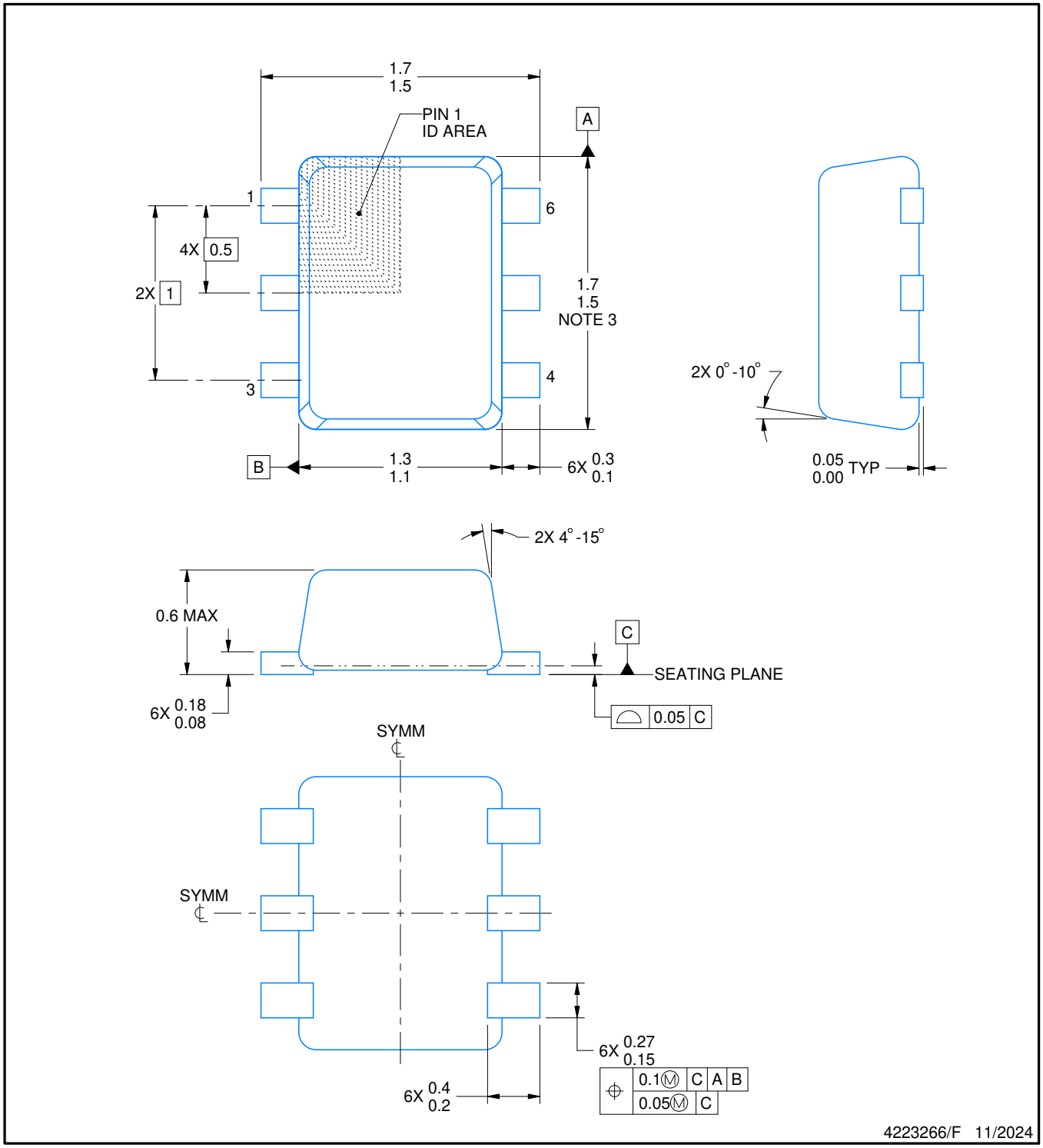
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8210DRLR	SOT-5X3	DRL	6	4000	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3
DRV8210DSGR	WSON	DSG	8	3000	178.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
DRV8210DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
DRV8210DSGRG4	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



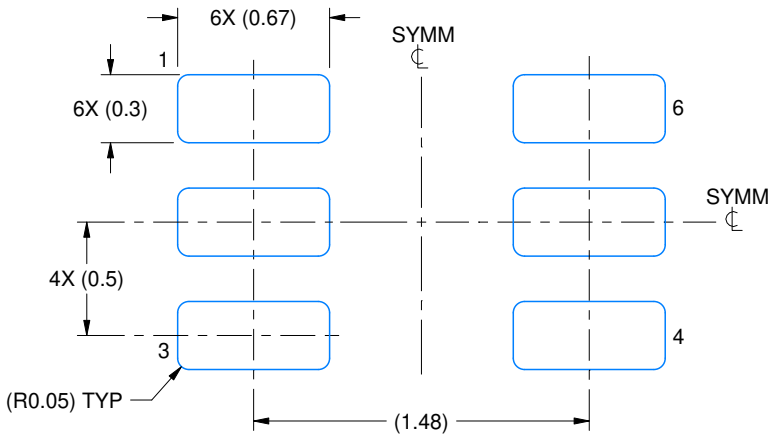
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8210DRLR	SOT-5X3	DRL	6	4000	210.0	185.0	35.0
DRV8210DSGR	WSON	DSG	8	3000	208.0	191.0	35.0
DRV8210DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
DRV8210DSGRG4	WSON	DSG	8	3000	210.0	185.0	35.0

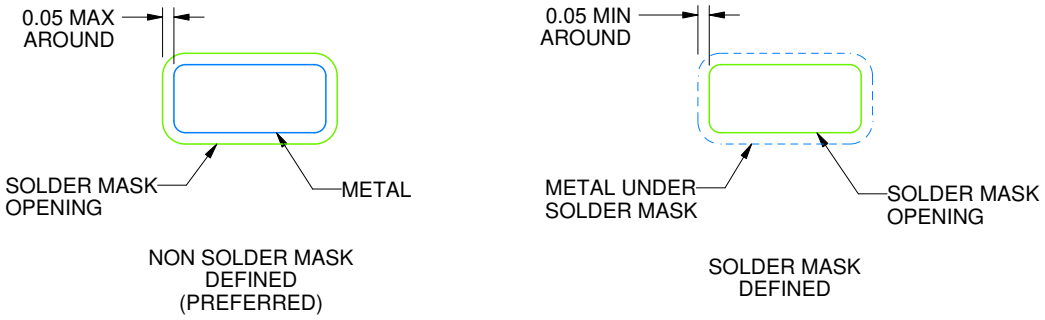


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD



LAND PATTERN EXAMPLE
SCALE:30X

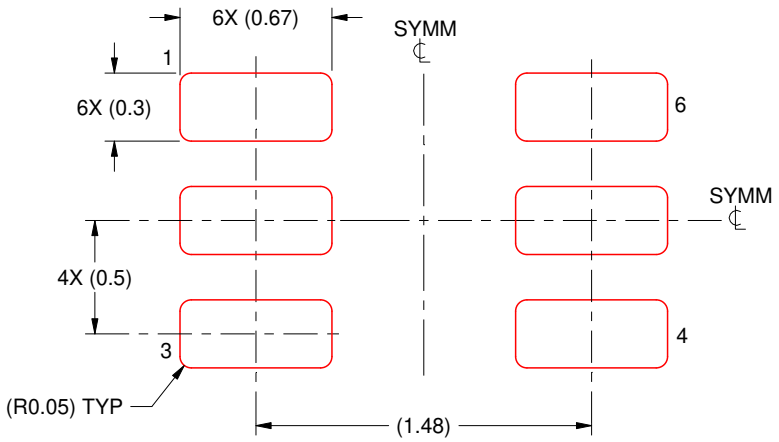


SOLDERMASK DETAILS

4223266/F 11/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4223266/F 11/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

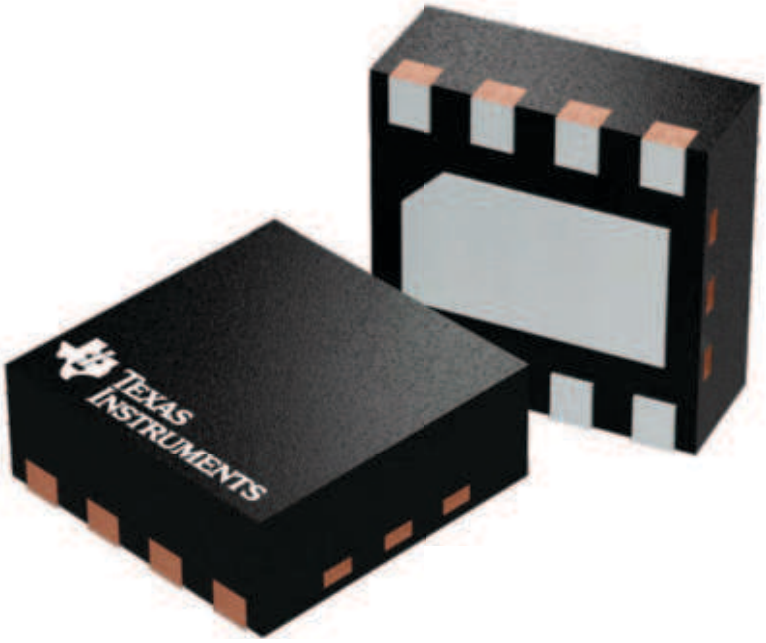
DSG 8

WSON - 0.8 mm max height

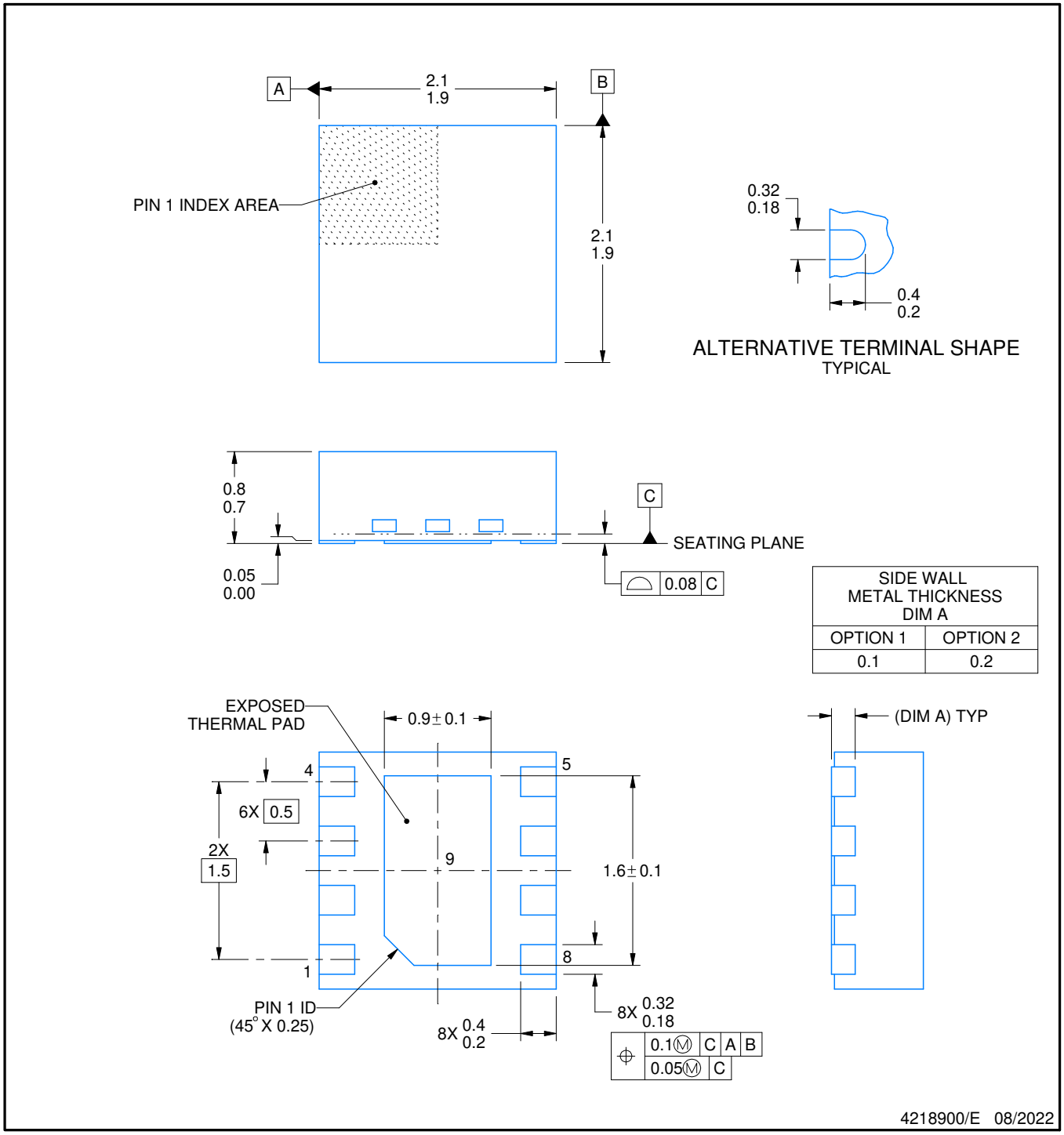
2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

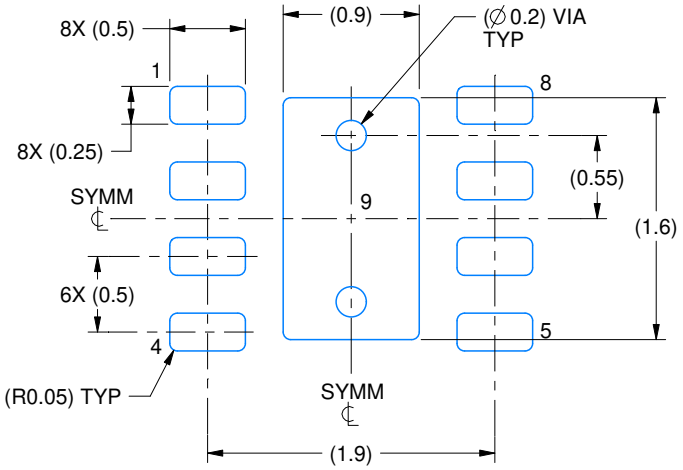


4224783/A

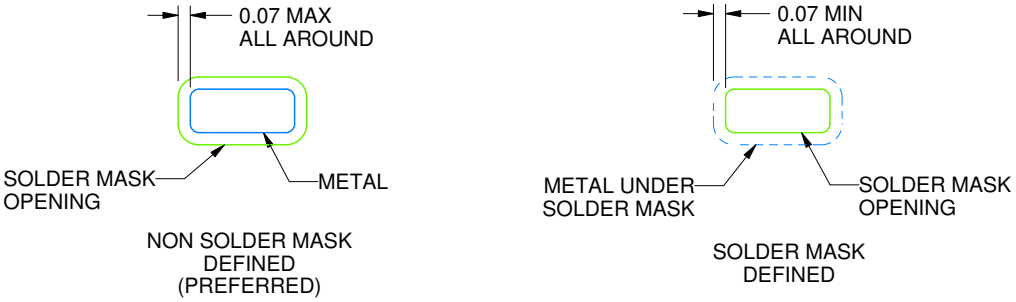


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

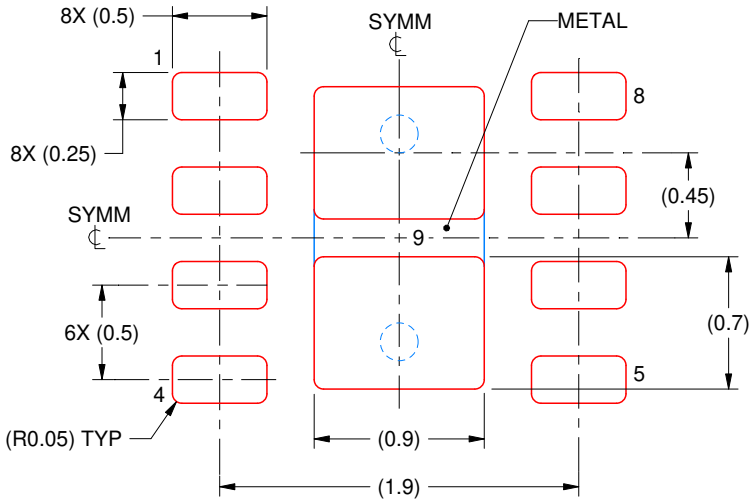


SOLDER MASK DETAILS

4218900/E 08/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4218900/E 08/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025