Rev 1; 11/03

DALLAS SEMICONDUCTOR MAXIM

3.3V Spread-Spectrum EconOscillator

General Description

The DS1087L is a clock generator that produces a spread-spectrum (dithered) square-wave output of frequencies from 130kHz to 66.6MHz. The DS1087L is shipped from the factory programmed at a specific frequency and spread-spectrum percentage. The user still has access to an internal frequency divider, selectable 2% or 4% dithered output, and programmable output power-down/disable mode through a 2-wire programming interface. All the device settings are stored in nonvolatile (NV) EEPROM allowing it to operate in stand-alone applications. The DS1087L has power-down and output-enable control pins for power-sensitive applications.

Applications

Printers
Copiers
PCs
Computer Peripherals
Cell Phones
Cable Modems

Features

- **Factory Programmed Square-Wave Generator from 130kHz to 66.6MHz**
- **No External Timing Components Required**
- **EMI Reduction**
- **2.7V to 3.6V Supply**
- **User Programmable Down to 130kHz with Divider (Dependent on Master Oscillator Frequency)**
- **2% or 4% Selectable Dithered Output**
- **Glitchless Output-Enable Control**
- **2-Wire Serial Interface**
- **Nonvolatile Settings**
- **Power-Down Mode**
- **Programmable Output Power-Down/Disable Mode**

Ordering Information

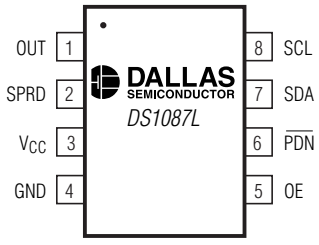
PART	TEMP RANGE	PIN-PACKAGE
DS1087LU-yxx	-40°C to +85°C	8 µSOP (118 mils)

Standard Frequency Options

PART	FREQUENCY (MHz)	SPREAD (%)
DS1087LU-202	2.0480	2
DS1087LU-402	2.0480	4
DS1087LU-210	10.0	2
DS1087LU-216	16.6	2
DS1087LU-266	66.6	2
DS1087LU-466	66.6	4
DS1087LU-yxx	Fixed up to 66.6	2 or 4

Custom frequencies and over 20 standard frequencies available, contact factory.

Pin Configuration



µSOP (118 mils)

EconOscillator is a trademark of Dallas Semiconductor.
Typical Operating Circuits appear at end of data sheet.

For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

3.3V Spread-Spectrum EconOscillator

ABSOLUTE MAXIMUM RATINGS

Voltage Range on V_{CC} Relative to Ground .....-0.5V to +6.0V
Voltage Range on SPRD, $\overline{PDN}$, OE, SDA, SCL
Relative to Ground* .....-0.5V to (V_{CC} + 0.5V)
Operating Temperature Range .....-40°C to +85°C
Programming Temperature Range .....0°C to +70°C
Storage Temperature Range .....-55°C to +125°C
Soldering Temperature .....See IPC/JEDEC J-STD-020A

*This voltage must not exceed 6.0V.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(V_{CC} = 2.7V to 3.6V, T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}	(Note 1)	2.7		3.6	V
High-Level Input Voltage (SDA, SCL, SPRD, $\overline{PDN}$, OE)	V_{IH}		0.7 x V_{CC}		V_{CC} + 0.3	V
Low-Level Input Voltage (SDA, SCL, SPRD, $\overline{PDN}$, OE)	V_{IL}		-0.3		0.3 x V_{CC}	V

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.7V to 3.6V, T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
High-Level Output Voltage (OUT)	V_{OH}	I_{OH} = -4mA, V_{CC} = min	2.4			V
Low-Level Output Voltage (OUT)	V_{OL}	I_{OL} = 4mA			0.4	V
Low-Level Output Voltage (SDA)	V_{OL1}	3mA sink current	0		0.4	V
	V_{OL2}	6mA sink current	0		0.6	
High-Level Input Current	I_{IH}	V_{CC} = 3.6V			1	µA
Low-Level Input Current	I_{IL}	V_{IL} = 0	-1			µA
Supply Current (Active)	I_{CC}	C_L = 15pF (output at f_0)			15	mA
Standby Current (Power-Down)	I_{CCQ}	Power-down mode			5	µA

MASTER OSCILLATOR CHARACTERISTICS

(V_{CC} = 2.7V to 3.6V, T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Master Oscillator Range Available	f_0		33.3		66.6	MHz
Master Oscillator Frequency Tolerance	$\frac{\Delta f_0}{f_0}$	V_{CC} = 3.3V, T_A = +25°C (Notes 2, 13)	-0.5		+0.5	%
Voltage Frequency Variation	$\frac{\Delta f_V}{f_0}$	Over voltage range, T_A = +25°C (Note 3)	-0.75		+0.75	%
Temperature Frequency Variation	$\frac{\Delta f_T}{f_0}$	0°C to +70°C, V_{CC} = 3.3V (Note 4)	-0.5		+0.5	%
Temperature Frequency Variation	$\frac{\Delta f_T}{f_0}$	-40°C to +85°C, V_{CC} = 3.3V (Note 4)	-1.5		+0.5	%
Dither Frequency Range		Prescaler bit J0 = 1 (Note 5)		2		%
		Prescaler bit J0 = 0 (Note 5)		4		
Dither Rate				f_0 / 4096		Hz

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.7V to 3.6V, T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Frequency Stable After PRESCALER Change					1	period
Power-Up Time	t_{POR} + t_{STAB}	(Note 6)		0.1	0.5	ms
Enable of OUT After Exiting Power-Down Mode	t_{STAB}				500	µs
OUT Disabled After Entering Power-Down Mode	t_{PDN}				1	ms
Load Capacitance	C_L	(Note 7)		15	50	pF
Output Duty Cycle (OUT)		T_A = +25°C	45		55	%

AC ELECTRICAL CHARACTERISTICS—2-WIRE INTERFACE

(V_{CC} = 2.7V to 3.6V, T_A = 0°C to +70°C.)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}	Fast mode (Note 8)			400	kHz
		Standard mode (Note 8)			100	
Bus Free Time Between a STOP and START Condition	t_{BUF}	Fast mode (Note 8)	1.3			µs
		Standard mode (Note 8)	4.7			
Hold Time (repeated) START Condition	$t_{HD:STA}$	Fast mode (Notes 8 and 9)	0.6			µs
		Standard mode (Notes 8 and 9)	4.0			
LOW Period of SCL	t_{LOW}	Fast mode (Note 8)	1.3			µs
		Standard mode (Note 8)	4.7			
HIGH Period of SCL	t_{HIGH}	Fast mode (Note 8)	0.6			µs
		Standard mode (Note 8)	4.0			
Setup Time for a Repeated START	$t_{SU:STA}$	Fast mode	0.6			µs
		Standard mode	4.7			
Data Hold Time	$t_{HD:DAT}$	Fast mode (Notes 8, 10, and 11)	0		0.9	µs
		Standard mode (Notes 8, 10, and 11)	0		0.9	
Data Setup Time	$t_{SU:DAT}$	Fast mode (Note 8)	100			ns
		Standard mode (Note 8)	250			
Rise Time of Both SDA and SCL Signals	t_R	Fast mode (Note 12)	$20 + 0.1C_B$		300	ns
		Standard mode (Note 12)	$20 + 0.1C_B$		1000	
Fall Time of Both SDA and SCL Signals	t_F	Fast mode (Note 12)	$20 + 0.1C_B$		300	ns
		Standard mode (Note 12)	$20 + 0.1C_B$		1000	
Setup Time for STOP	$t_{SU:STO}$	Fast mode	0.6			µs
		Standard mode	4.0			
Capacitive Load for Each Bus	C_B	(Note 12)			400	pF
NV Write Cycle Time	t_{WR}				10	ms
Input Capacitance	C_I			5		pF

NONVOLATILE MEMORY CHARACTERISTICS

(V_{CC} = 2.7V to 3.6V)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Writes		+70°C	10,000			

Note 1: All voltages are referenced to ground.

Note 2: This is the absolute accuracy of the master oscillator frequency at the default settings.

Note 3: This is the change that is observed in master oscillator frequency with changes in voltage from nominal voltage at T_A = +25°C.

Note 4: This is the percentage frequency change from the +25°C frequency due to temperature at V_{CC} = 3.3V.

Note 5: The dither deviation of the master oscillator frequency is unidirectional and lower than the undithered frequency.

Note 6: This indicates the time elapsed between power-up and the output becoming active. An on-chip delay is intentionally introduced to allow the oscillator to stabilize. t_{stab} is equivalent to approximately 512 master clock cycles and depends on the programmed master oscillator frequency.

Note 7: Output voltage swings may be impaired at high frequencies combined with high output loading.

Note 8: A fast-mode device can be used in a standard-mode system, but the requirement $t_{SU:DAT}$ > 250ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line at least $t_{R\ MAX}$ + $t_{SU:DAT}$ = 1000ns + 250ns = 1250ns before the SCL line is released.

Note 9: After this period, the first clock pulse is generated.

Note 10: A device must internally provide a hold time of at least 300ns for the SDA signal (referred to as the $V_{IH\ MIN}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL.

Note 11: The maximum $t_{HD:DAT}$ need only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.

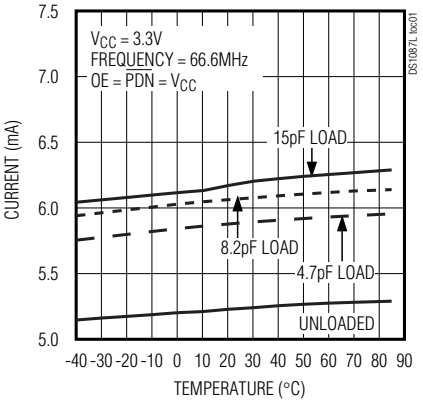
Note 12: C_B—total capacitance of one bus line, timing referenced to 0.9 x V_{CC} and 0.1 x V_{CC}.

Note 13: Typical frequency shift due to aging is ±0.5%. Aging stressing includes Level 1 moisture reflow preconditioning (24hr +125°C bake, 168hr 85°C/85%RH moisture soak, and 3 solder reflow passes +240 +0/-5°C peak) followed by 1000hr max V_{CC} biased 125°C HTOL, 1000 temperature cycles at -55°C to +125°C, and 168hr 121°C/2 ATM Steam/Unbiased Autoclave.

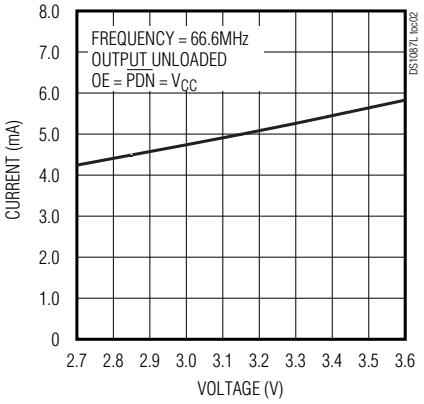
Typical Operating Characteristics

(V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.)

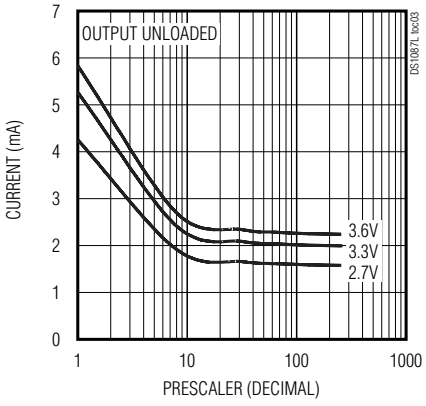
ACTIVE SUPPLY CURRENT vs. TEMPERATURE



ACTIVE SUPPLY CURRENT vs. VOLTAGE



SUPPLY CURRENT vs. PRESCALER

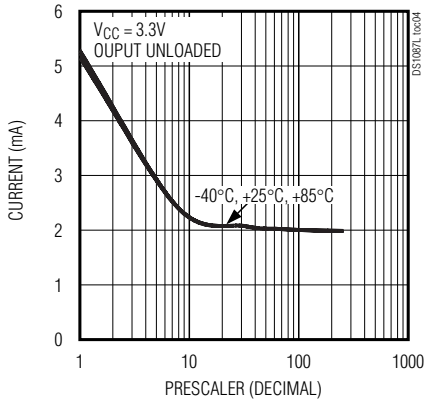


3.3V Spread-Spectrum EconOscillator

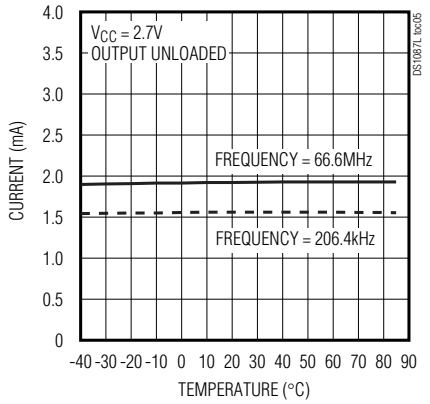
Typical Operating Characteristics

(V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.)

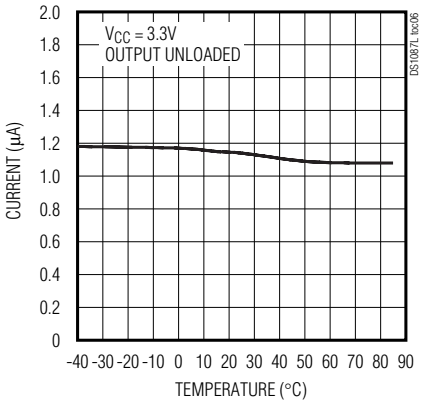
SUPPLY CURRENT vs. PRESCALER



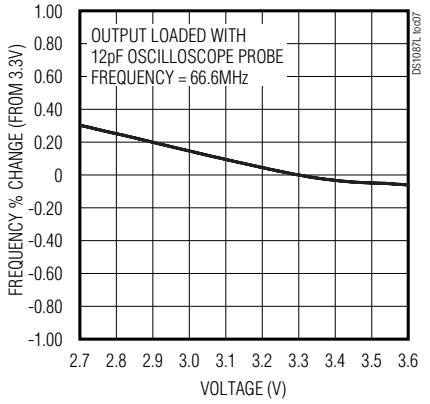
SUPPLY CURRENT vs. TEMPERATURE WITH OE = 0



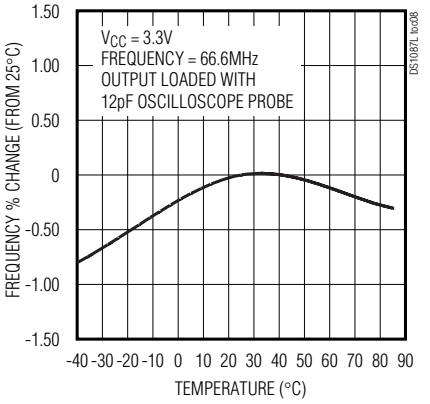
SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



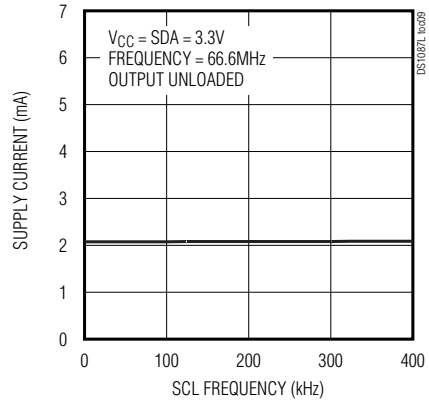
FREQUENCY % CHANGE vs. SUPPLY VOLTAGE



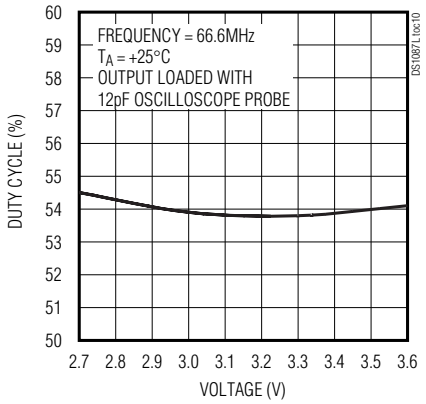
FREQUENCY % CHANGE vs. TEMPERATURE



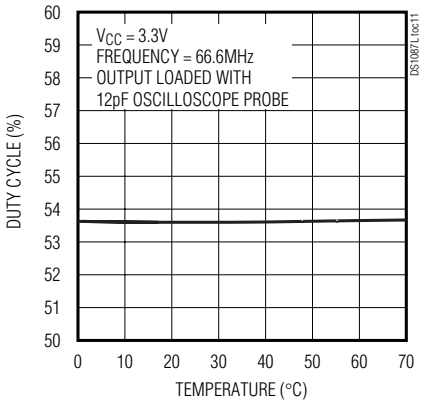
ACTIVE SUPPLY CURRENT vs. SCL FREQUENCY



DUTY CYCLE vs. VOLTAGE



DUTY CYCLE vs. TEMPERATURE



Pin Description

PIN	NAME	FUNCTION
1	OUT	Oscillator Output
2	SPRD	Dither Enable. When the pin is high, the dither is enabled. When the pin is low, the dither is disabled.
3	V_{CC}	Power Supply
4	GND	Ground
5	OE	Output Enable. When the pin is high, the output buffer is enabled. When the pin is low, the output is disabled but the internal master oscillator is still on.
6	$\overline{PDN}$	Power-Down. When the pin is high, the master oscillator is enabled. When the pin is low, the master oscillator is disabled (power-down mode).
7	SDA	2-Wire Serial Data. This pin is for serial data transfer to and from the device.
8	SCL	2-Wire Serial Clock. This pin is used to clock data into and out of the device.

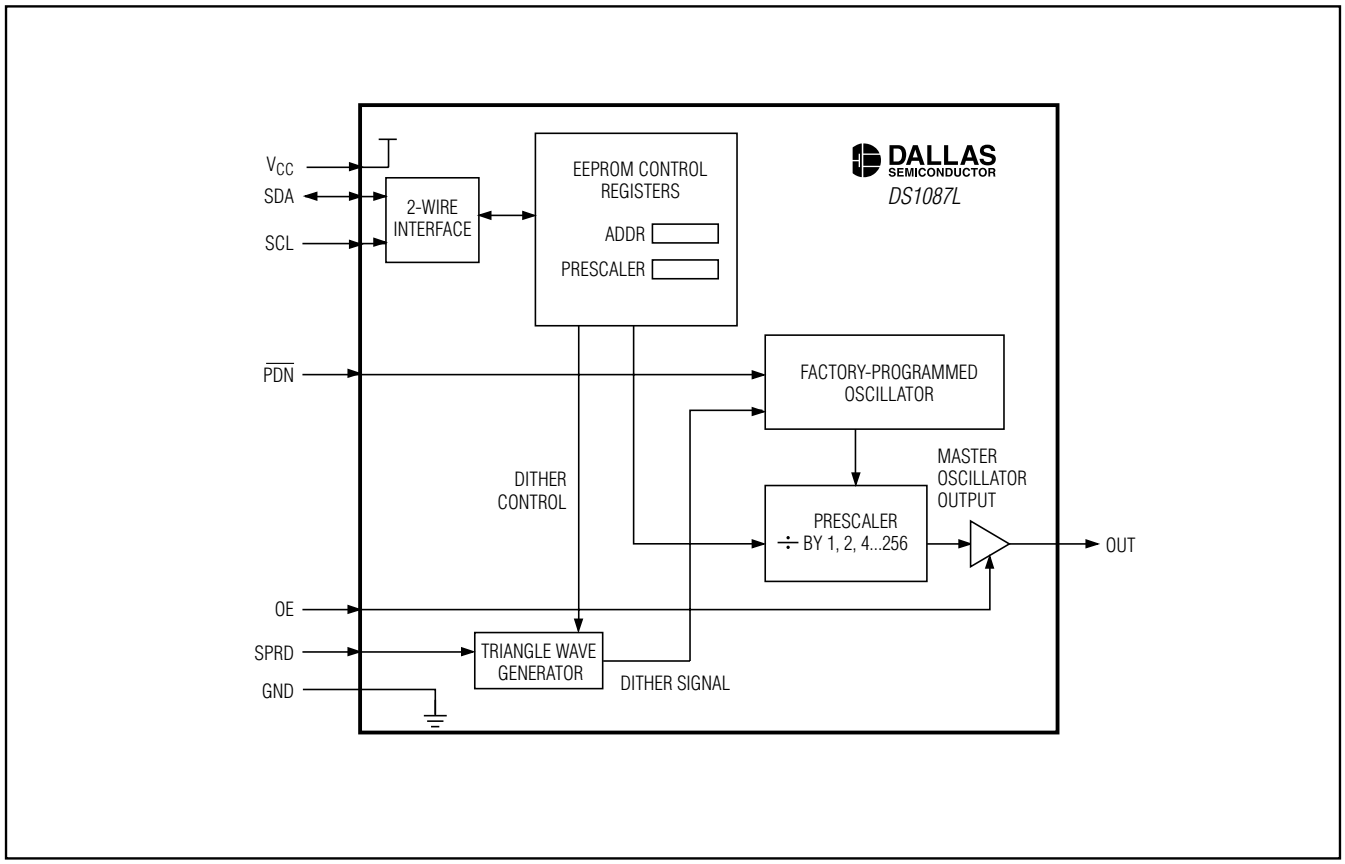


Figure 1. Functional Diagram

3.3V Spread-Spectrum EconOscillator

Table 1. Register Summary

REGISTER	ADDR	BINARY								FACTORY DEFAULT	ACCESS
PRESCALER	02h	X_1	X_1	LO/$\overline{HIZ}$	J0	P3	P2	P1	P0	110- - - - - b	R/W
ADDR	0Dh	X_1	X_1	X_1	X_1	WC	A2	A1	A0	11110000b	R/W
WRITE EE	3Fh	No Data								—	—

X_1 = Don't care; read as one.

Detailed Description

A block diagram of the DS1087L is shown in Figure 1.

Output Frequency

The internal master oscillator can generate a square wave with a frequency range of 33.3MHz to 66.6MHz. The master oscillator frequency and output frequency are factory programmed, although the user can use the programmable divider to divide the master oscillator frequency by 2^X (where x equals 0 to 8).

Output Control and Power-Down

Two user control signals control the output. The output-enable pin, OE, gates the clock output buffer and the $\overline{PDN}$ pin disables the master oscillator and turns off the output for power-sensitive applications (note: the power-down command must persist for at least two output frequency cycles plus 10µs for deglitching purposes). On power-up, the output is disabled until power is stable and the master oscillator has generated 512 clock cycles.

Both controls feature a synchronous enable, which ensures there are no output glitches when the output is enabled. The synchronous enable also ensures a constant time interval (for a given frequency setting) from an enable signal to the first output transition.

Spread Spectrum

The DS1087L can reduce radiated emission peaks. The output frequency can be dithered 2% or 4% below the programmed frequency. Although the output frequency changes when the dither is enabled, the duty cycle does not change.

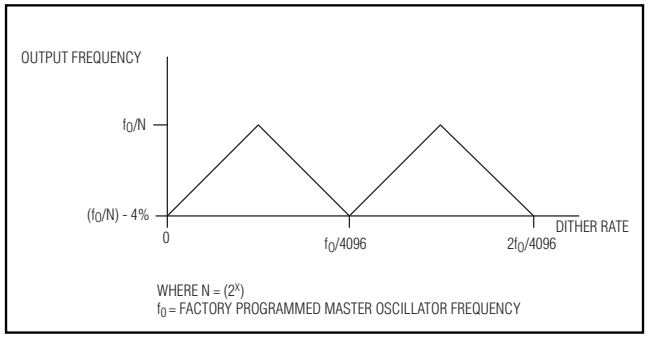


Figure 2. Output Frequency vs. Dither Rate

The dither is controlled by the J0 bit in the PRESCALER register and enabled with the SPRD pin. The maximum spectral attenuation occurs when the prescaler is set to 1. The spectral attenuation is reduced by 2.7dB for every factor of 2 that is used in the prescaler. This happens because the prescaler's divider function tends to average the dither in creating the lower frequency. However, the most stringent spectral emission limits are imposed on the higher frequencies where the prescaler is set to a low divider ratio.

A triangle-wave generator injects an offset element into the master oscillator to dither its output. The dither rate (see Equation 1) is based on the master oscillator frequency. Figure 2 shows a plot of the output frequency versus dither rate.

$$\text{Dither Rate} = \frac{f_0}{4096} \quad (1)$$

where f_0 = master oscillator frequency

Register Summary

The DS1087L registers are used to change the dither amount, output frequency, and slave address. A summary of the registers is shown in Table 1. Once programmed into EEPROM, the settings only need to be reprogrammed if it is desired to reconfigure the device.

PRESCALER Register

Bit 5: **Output Low or High-Z.** The LO/$\overline{HIZ}$ bit controls the output. During power-down, while the output is deactivated, if the LO/$\overline{HIZ}$ bit is set to 0, the output is high-Z. If the LO/$\overline{HIZ}$ bit is set to 1, the output is driven low.

Bit 4: **Dither Control.** The J0 bit controls the dither applied to the output. When J0 is high, 2% peak dither is selected. When J0 is low, 4% peak dither is selected.

Bits 3 to 0: **Prescaler Divider.** The prescaler bits (bits P3 to P0) divide the master oscillator frequency by 2^x where x can be from 0 to 8. Any prescaler bit value entered that is greater than 8 decodes as 8.

ADDR Register

Bit 3: **Write Control.** The WC bit determines if the EEPROM is to be written to after register contents have been changed. If WC = 0 (default), EEPROM is written automatically after a write. If WC = 1, the EEPROM is only written when the WRITE EE command is issued. See the *WRITE EE Command* section for more information.

Bits 2 to 0: **Address.** The A0, A1, A2 bits determine the lower nibble of the 2-wire slave address.

WRITE EE Command

The WRITE EE command is useful in closed-loop applications where the registers are frequently written. In applications where the register contents are frequently written, the WC bit should be set to 1 to prevent wearing out the EEPROM. Regardless of the value of the WC bit, the value of the ADDR register is always written immediately to EEPROM. When the WRITE EE command has been received, the contents of the registers are copied into the EEPROM, thus locking in the register settings.

2-Wire Serial Port Operation

2-Wire Serial Data Bus

The DS1087L communicates through a 2-wire serial interface. A device that sends data onto the bus is defined as a transmitter, and a device receiving data as a receiver. The device that controls the message is called a "master." The devices that are controlled by the master are "slaves." A master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions must control the bus. The DS1087L operates as a slave on the 2-wire bus. Connections to the bus are made through the open-drain I/O lines SDA and SCL.

The following bus protocol has been defined (see Figures 3 and 5):

- Data transfer can be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH are interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus not busy: Both data and clock lines remain HIGH.

Start data transfer: A change in the state of the data line, from HIGH to LOW, while the clock is HIGH, defines a START condition.

Stop data transfer: A change in the state of the data line, from LOW to HIGH, while the clock line is HIGH, defines the STOP condition.

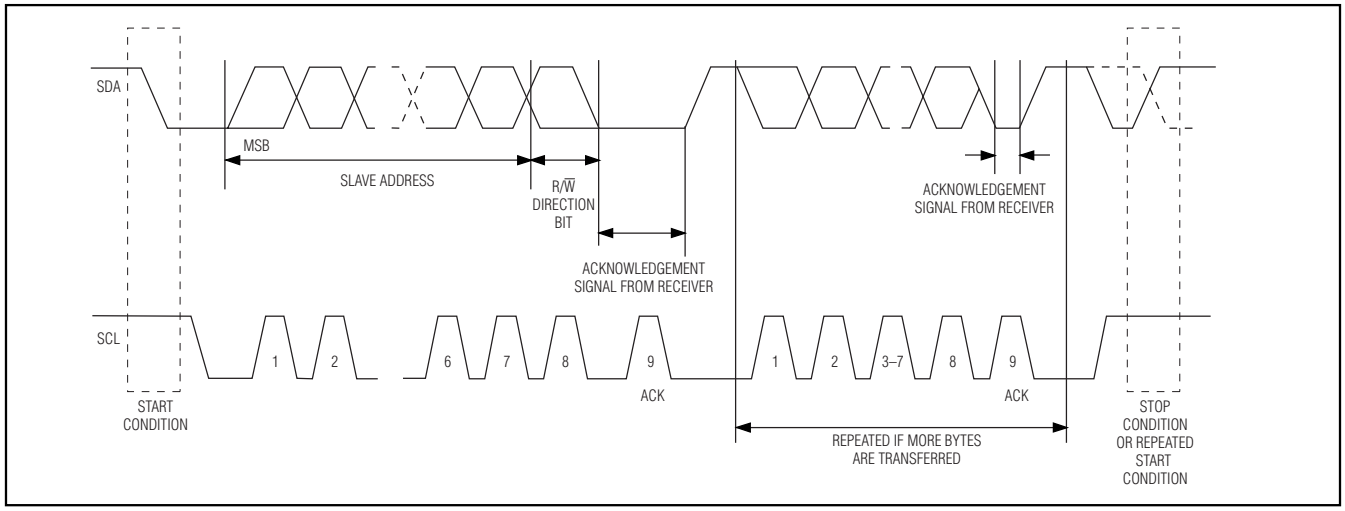


Figure 3. 2-Wire Data Transfer Protocol

3.3V Spread-Spectrum EconOscillator

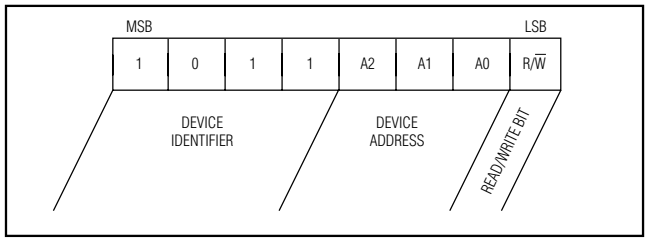


Figure 4. Slave Address

Data valid: The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions is not limited, and is determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth bit.

Within the bus specifications a standard mode (100kHz clock rate) and a fast mode (400kHz clock rate) are defined. The DS1087L works in both modes.

Acknowledge: Each receiving device, when addressed, is obliged to generate an acknowledge after the byte has been received. The master device must generate an extra clock pulse that is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse. Of course, setup and hold times must be taken into account. When the DS1087L EEPROM is being written to, it is not able to perform additional responses. In this case, the slave DS1087L sends a not acknowledge to any data transfer request made by the master. It resumes normal operation when the EEPROM operation is complete.

A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

Figures 3, 4, 5, and 6 detail how data transfer is accomplished on the 2-wire bus. Depending upon the state of the R/$\overline{W}$ bit, two types of data transfer are possible:

1) Data transfer from a master transmitter to a slave receiver. The first byte transmitted by the master is the slave address. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte.
2) Data transfer from a slave transmitter to a master receiver. The first byte (the slave address) is transmitted by the master. The slave then returns an acknowledge bit. Next follows a number of data bytes transmitted by the slave to the master. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a not acknowledge is returned.

   The master device generates all the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus is not released.

The DS1087L can operate in the following two modes:

Slave receiver mode: Serial data and clock are received through SDA and SCL. After each byte is received, an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit.

Slave transmitter mode: The first byte is received and handled as in the slave receiver mode. However, in this mode, the direction bit indicates that the transfer direction is reversed. Serial data is transmitted on SDA by the DS1087L while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer.

Slave Address

Figure 4 shows the first byte sent to the device. It includes the device identifier, device address, and the R/$\overline{W}$ bit. The device address must match the address set in the ADDR register (bits A0, A1, and A2).

Registers/Commands

See Table 1 for the complete list of registers/commands and Figure 6 for an example of using them.

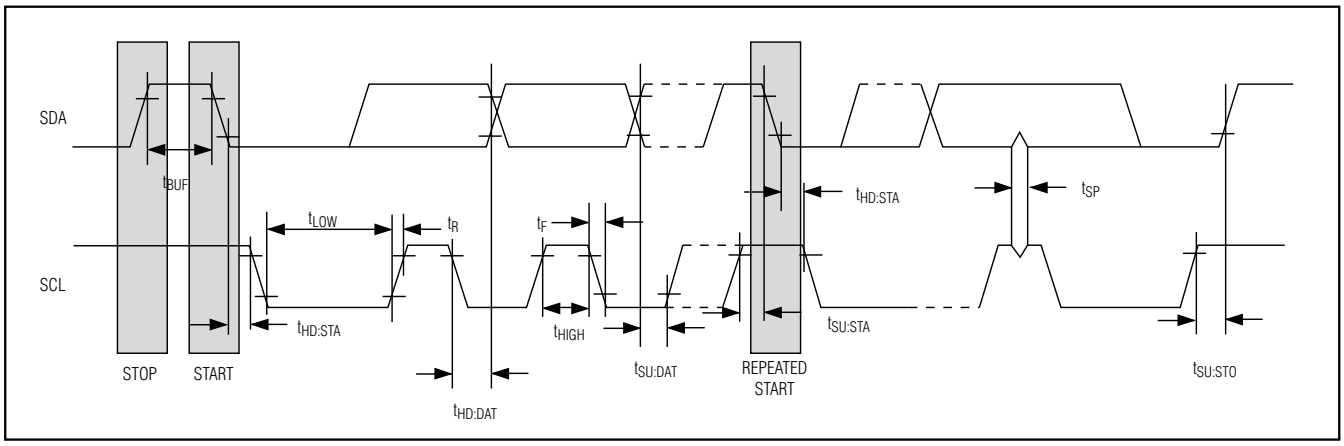


Figure 5. 2-Wire AC Characteristics

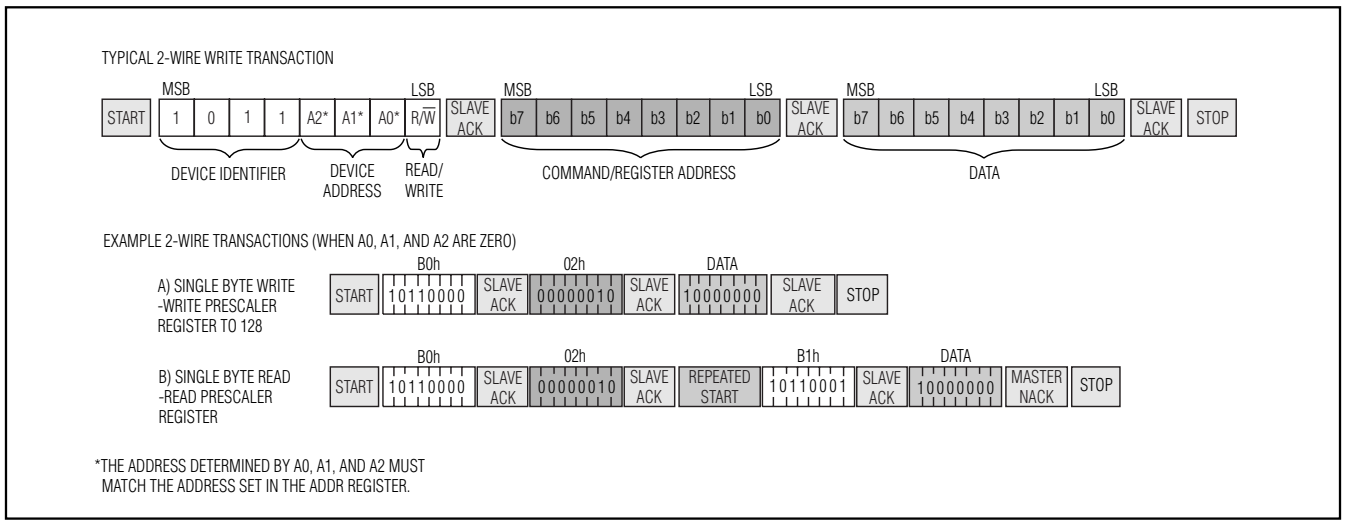


Figure 6. 2-Wire Transactions

Application Information

Power-Supply Decoupling

To achieve the best results when using the DS1087L, decouple the power supply with 0.01µF and 0.1µF high-quality, ceramic, surface-mount capacitors. Surface-mount components minimize lead inductance, which improves performance, and ceramic capacitors tend to have adequate high-frequency response for decoupling applications. These capacitors should be placed as close to the V_{CC} and GND pins as possible.

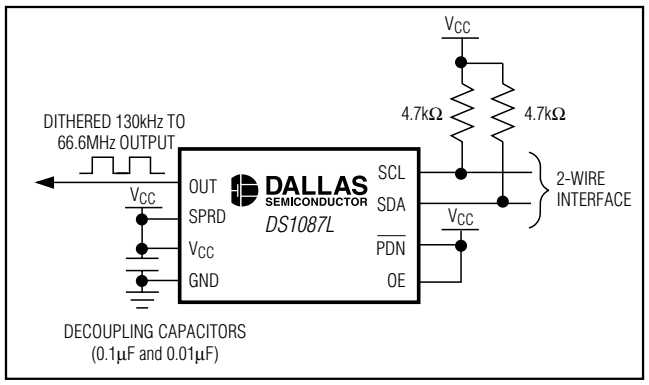
Stand-alone Mode

SCL and SDA cannot be left floating even in stand-alone mode. If the DS1087L never needs to be programmed in-circuit, including during production testing, SDA and SCL can be wired high.

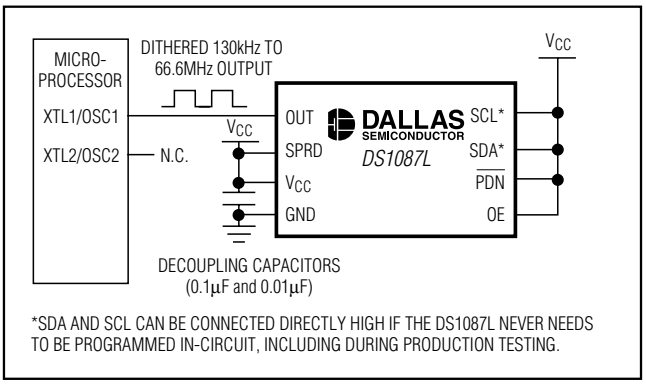
3.3V Spread-Spectrum EconOscillator

Typical Operating Circuits

Processor-Controlled Mode



Stand-Alone Mode



*SDA AND SCL CAN BE CONNECTED DIRECTLY HIGH IF THE DS1087L NEVER NEEDS TO BE PROGRAMMED IN-CIRCUIT, INCLUDING DURING PRODUCTION TESTING.

Chip Topology

TRANSISTOR COUNT: 10000

SUBSTRATE CONNECTED TO GROUND

Package Information

For the latest package outline information, go to **www.maxim-ic.com/DallasPackInfo**

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

© 2003 Maxim Integrated Products Printed USA MAXIM is a registered trademark of Maxim Integrated Products.