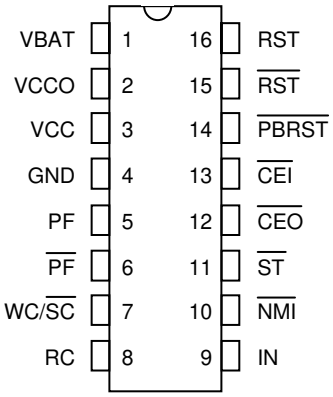
DS1236
MicroManager Chip

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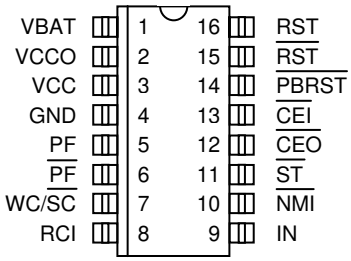
FEATURES

- Holds microprocessor in check during power transients
- Halts and restarts an out-of-control microprocessor
- Monitors pushbutton for external override
- Warns microprocessor of an impending power failure
- Converts CMOS SRAM into nonvolatile memory
- Unconditionally write-protects memory when power supply is out of tolerance
- Consumes less than 100 nA of battery current at 25°C
- Controls external power switch for high current applications
- Accurate 10% power supply monitoring
- Optional 5% power supply monitoring designated DS1236-5
- Provides orderly shutdown in nonvolatile microprocessor applications
- Supplies necessary control for low-power "stop mode" in battery operated hand-held applications
- Standard 16-pin DIP or space-saving 16-pin SOIC
- Optional industrial temperature range -40°C to +85°C

PIN ASSIGNMENT



16-Pin DIP (300-mil)
See Mech. Drawings Section



16-Pin SOIC (300-mil)
See Mech. Drawings Section

PIN DESCRIPTION

V_{BAT}	- +3-Volt Battery Input
V_{CCO}	- Switched SRAM Supply Output
V_{CC}	- +5-Volt Power Supply Input
GND	- Ground
PF	- Power-Fail (Active High)
$\overline{PF}$	- Power-Fail (Active Low)
WC/$\overline{SC}$	- Wake-Up Control (Sleep)
RC	- Reset Control
IN	- Early Warning Input
$\overline{NMI}$	- Non-Maskable Interrupt
$\overline{ST}$	- Strobe Input
$\overline{CEO}$	- Chip Enable Output
$\overline{CEI}$	- Chip Enable Input
$\overline{PBRST}$	- Pushbutton Reset Input
$\overline{RST}$	- Reset Output (Active Low)
RST	- Reset Output (Active High)

DESCRIPTION

The DS1236 MicroManager Chip provides all the necessary functions for power supply monitoring, reset control, and memory backup in microprocessor-based systems. A precise internal voltage reference and comparator circuit monitor power supply status. When an out-of-tolerance condition occurs, the microprocessor reset and power-fail outputs are forced active, and static RAM control unconditionally write protects external memory. The DS1236 also provides early warning detection of a user-defined threshold by driving a non-maskable interrupt. External reset control is provided by a pushbutton reset

input which is debounced and activates reset outputs. An internal watchdog timer can also force the reset outputs to the active state if the strobe input is not driven low prior to watchdog timeout. Reset control and wake-up/sleep control inputs also provide the necessary signals for orderly shutdown and startup in battery backup and battery operated applications. A block diagram of the DS1236 is shown in Figure 1.

PIN DESCRIPTION

PIN NAME	DESCRIPTION
V_{BAT}	+3V battery input provides nonvolatile operation of control functions.
V_{CCO}	V_{CC} output for nonvolatile SRAM applications.
V_{CC}	+5V primary power input.
PF	Power-fail indicator, active high, used for external power switching as shown in Figure 9.
$\overline{PF}$	Power-fail indicator, active low.
WC/$\overline{SC}$	Wake-up and Sleep control. Invokes low-power mode.
RC	Reset control input. Determines reset output. Normally low for NMOS processors and high for battery backed CMOS processors.
IN	Early warning power-fail input. This voltage sense point can be tied (via resistor divider) to a user-selected voltage.
$\overline{NMI}$	Non-maskable interrupt. Used in conjunction with the IN pin to indicate an impending power failure.
$\overline{ST}$	Strobe input. A high-to-low transition will reset the watchdog timer, indicating that software is still in control.
$\overline{CEO}$	Chip enable output. Used with nonvolatile SRAM applications.
$\overline{CEI}$	Chip enable input.
$\overline{PBRST}$	Pushbutton reset input.
$\overline{RST}$	Active low reset output.
RST	Active high reset output.

PROCESSOR MODE

A distinction is often made between CMOS and NMOS processor systems. In a CMOS system, power consumption may be a concern, and nonvolatile operation is possible by battery backing both the SRAM and the CMOS processor. All resources would be maintained in the absence of V_{CC}. A power-down reset is not issued since the low-power mode of most CMOS processors (Stop) is terminated with a Reset. A pulsed interrupt ($\overline{NMI}$) is issued to allow the CMOS processor to invoke a sleep mode to save power. For this case, a power-on reset is desirable to wake up and initialize the processor. The CMOS mode is invoked by connecting RC to V_{CCO}.

An NMOS processor consumes more power, and consequently may not be battery backed. In this case, it is desirable to notify the processor of a power-fail, then keep it in reset during the loss of V_{CC}. This avoids intermittent or aberrant operation. On power-up, the processor will continue to be reset until V_{CC} reaches an operational level to provide an orderly start. The NMOS mode is invoked by connecting RC to ground.

POWER MONITOR

The DS1236 employs a band gap voltage reference and a precision comparator to monitor the 5-volt supply (V_{CC}) in microprocessor-based systems. When an out-of-tolerance condition occurs, the RST and $\overline{RST}$ outputs are driven to the active state. The V_{CC} trip point (V_{CCTP}) is set for 10% operation so that the RST and $\overline{RST}$ outputs will become active as V_{CC} falls below 4.5 volts (4.37 typical). The V_{CCTP} for the 5% operation option (DS1236-5) is set for 4.75 volts (4.62 typical). The RST and $\overline{RST}$ signals are excellent for microprocessor reset control, as processing is stopped at the last possible moment of in-tolerance V_{CC}. On power-up, the RST and $\overline{RST}$ signals are held active for a minimum of 25 ms (100 ms typical) after V_{CCTP} is reached to allow the power supply and microprocessor to stabilize. Note: The operation described above is obtained with the reset control pin (RC) connected to GND (NMOS mode). Please review the reset control section for more information.

WATCHDOG TIMER

The DS1236 provides a watchdog timer function which forces the RST and $\overline{RST}$ signals to the active state when the strobe input ($\overline{ST}$) is not stimulated for a predetermined time period. This time period is 400 ms typically with a maximum time-out of 600 ms. The watchdog time-out period begins as soon as RST and $\overline{RST}$ are inactive. If a high-to-low transition occurs at the $\overline{ST}$ input prior to time-out, the watchdog timer is reset and begins to time out again. The $\overline{ST}$ input timing is shown in Figure 2. To guarantee the watchdog timer does not time out, a high-to-low transition on $\overline{ST}$ must occur at or less than 100 ms (minimum time-out) from a reset. If the watchdog timer is allowed to time out, the RST and $\overline{RST}$ outputs are driven to the active state for 25 ms minimum. The $\overline{ST}$ input can be derived from microprocessor address, data, and/or control signals. Under normal operating conditions, these signals would routinely reset the watchdog timer prior to time-out. If the watchdog timer is not required, two methods have been provided to disable it.

Permanently grounding the IN pin in the CMOS mode (RC=1) will disable the watchdog. In normal operation with RC=1, the watchdog is disabled as soon as the IN pin is below V_{TP}. With IN grounded, an $\overline{NMI}$ output will occur only at power-up, or when the $\overline{ST}$ pin is strobed. As shown in the Figure 3, a falling edge on $\overline{ST}$ will generate an $\overline{NMI}$ when IN is below V_{TP}. This allows the processor to verify that power is between V_{TP} and V_{CCTP}, as an $\overline{NMI}$ will be returned immediately after the $\overline{ST}$ strobe. The watchdog timer is not affected by the IN pin when in NMOS mode (RC=0).

If the $\overline{NMI}$ signal is required to monitor supply voltages, the watchdog may also be disabled by leaving the $\overline{ST}$ input open. Independent of the state of the RC pin, the watchdog is also disabled as soon as V_{CC} falls to V_{CCTP}.

PUSHBUTTON RESET

An input pin is provided on the DS1236 for direct connection to a pushbutton. The pushbutton reset input requires an active low signal. Internally, this input is pulled high by a 10k resistor whenever V_{CC} is greater than V_{BAT}. The $\overline{PBRST}$ pin is also debounced and timed such that the RST and $\overline{RST}$ outputs are driven to the active state for 25 ms minimum. This 25 ms delay begins as the pushbutton is released from a low level. A typical example of the power monitor, watchdog timer, and pushbutton reset connections are shown in Figure 4. The PBRST input is disabled whenever the IN pin voltage level is less than V_{TP} and the reset control (RC) is tied high (CMOS mode). The $\overline{PBRST}$ input is also disabled whenever V_{CC} is below V_{BAT}. Timing of the $\overline{PBRST}$ -generated RST is illustrated in Figure 5.

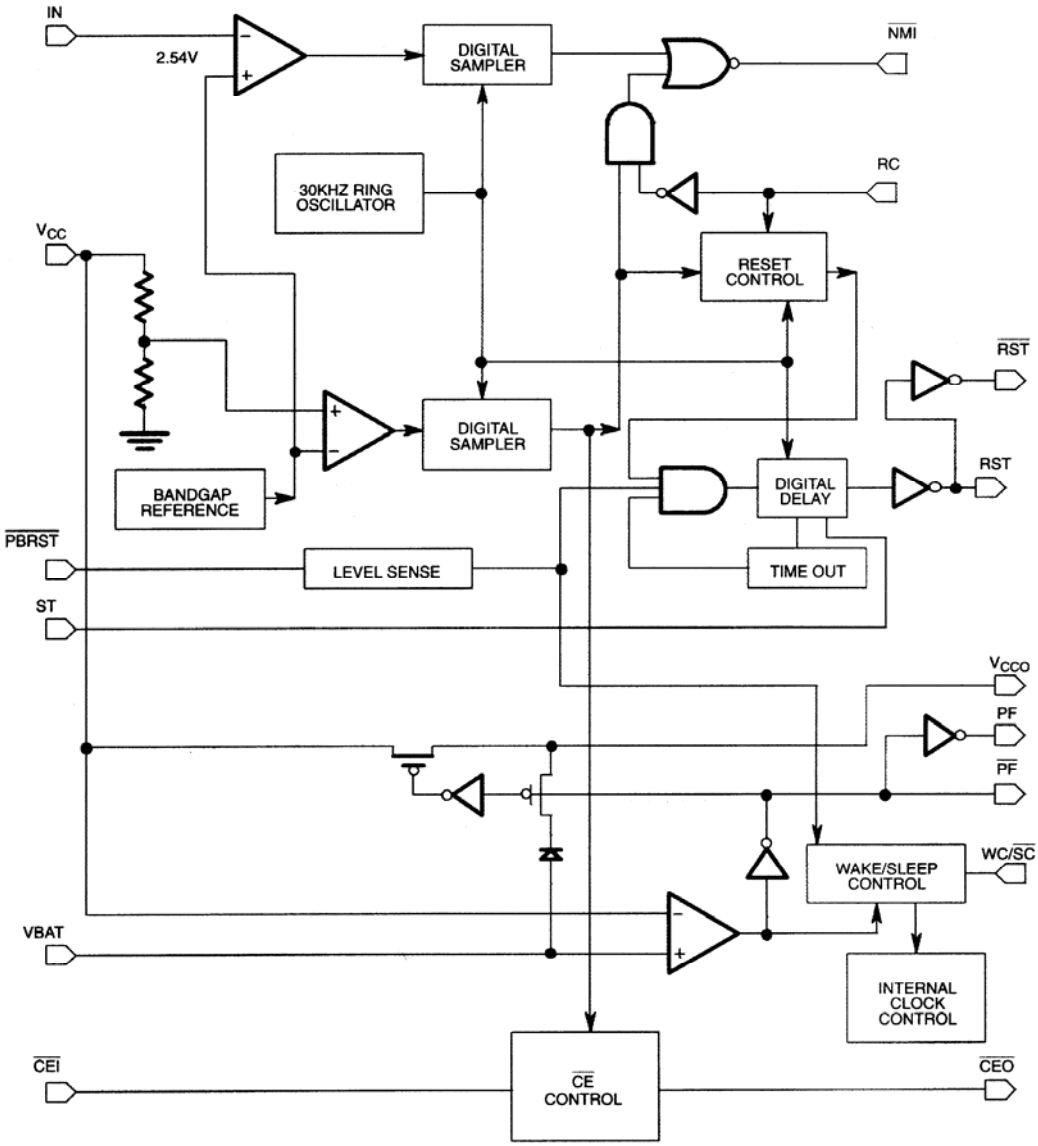
NON-MASKABLE INTERRUPT

The DS1236 generates a non-maskable interrupt $\overline{NMI}$ for early warning of power failure to a microprocessor. A precision comparator monitors the voltage level at the IN pin relative to a reference generated by the internal band gap. The IN pin is a high-impedance input allowing for a user-defined sense point. An external resistor voltage divider network (Figure 6) is used to interface with high voltage signals. This sense point may be derived from the regulated 5-volt supply or from a higher DC voltage level closer to the main system power input. Since the IN trip point V_{TP} is 2.54 volts, the proper values for R1 and R2 can be determined by the equation as shown in Figure 6. Proper operation of the DS1236 requires that the voltage at the IN pin be limited to V_{IN}. Therefore, the maximum allowable voltage at the supply being monitored (V_{MAX}) can also be derived as shown in Figure 6. A simple approach to solving this equation is to select a value for R2 high enough to keep power consumption low, and solve for R1. The flexibility of the IN input pin allows for detection of power loss at the earliest point in a power supply system, maximizing the amount of time for microprocessor shutdown between $\overline{NMI}$ and RST or $\overline{RST}$.

When the supply being monitored decays to the voltage sense point, the DS1236 pulses the $\overline{NMI}$ output to the active state for a minimum of 200 µs. The $\overline{NMI}$ power-fail detection circuitry also has built-in time domain hysteresis. That is, the monitored supply is sampled periodically at a rate determined by an internal ring oscillator running at approximately 30 kHz (33 µs/cycle). Three consecutive samplings of out-of-tolerance supply (below V_{SENSE}) must occur at the IN pin to activate $\overline{NMI}$. Therefore, the supply must be below the voltage sense point for approximately 100 µs or the comparator will reset. In this way, power supply noise is removed from the monitoring function, preventing false trips. During a power-up, any IN pin levels below V_{TP} are disabled from reaching the $\overline{NMI}$ pin until V_{CC} rises to V_{CCTP}. As a result, any potential $\overline{NMI}$ pulse will not be initiated until V_{CC} reaches V_{CCTP}.

Removal of an active low level on the $\overline{NMI}$ pin is controlled by either an internal time-out (when IN pin is less than V_{TP}) or by the subsequent rise of the IN pin above V_{TP}. The initiation and removal of the $\overline{NMI}$ signal during power-up results in an $\overline{NMI}$ pulse of from 0 µs minimum to 500 µs maximum, depending on the relative voltage relationship between V_{CC} and the IN pin voltage. As an example, when the IN pin is tied to ground during power-up, the internal time-out will result in a pulse of 200 µs minimum to 500 µs maximum. In contrast, if the IN pin is tied to V_{CCO} during power-up, $\overline{NMI}$ will not produce a pulse on power-up. Note that a fast slewing power supply may cause the $\overline{NMI}$ to be virtually nonexistent on power-up. This is of no consequence, however, since an RST will be active.

DS1236 FUNCTIONAL BLOCK DIAGRAM Figure 1



If the IN pin is connected to V_{CCO}, the $\overline{NMI}$ output will pulse low as V_{CC} decays to V_{CCTP} in the NMOS mode (RC=0). In the CMOS mode (RC=V_{CCO}) the power-down of V_{CC} out-of-tolerance at V_{CCTP} will not produce a pulse on the $\overline{NMI}$ pin. Given that any $\overline{NMI}$ pulse has been completed by the time V_{CC} decays to V_{CCTP}, the $\overline{NMI}$ pin will remain high. The $\overline{NMI}$ voltage will follow V_{CC} down until V_{CC} decays to V_{BAT}. Once V_{CC} decays to V_{BAT}, the $\overline{NMI}$ pin will either remain at V_{OHL} or enter tri-state mode as determined by the RC pin (see "Reset Control" section).

MEMORY BACKUP

The DS1236 provides all of the necessary functions required to battery back a static RAM. First, a switch is provided to direct SRAM power from the incoming 5-volt supply (V_{CC}) or from an external battery (V_{BAT}), whichever is greater. This switched supply (V_{CCO}) can also be used to battery back a CMOS microprocessor. For more information about nonvolatile processor applications, review the "Reset Control" and "Wake Control" sections. Second, the same power-fail detection described in the power monitor section is used to hold the chip enable output ($\overline{CEO}$) to within 0.3 volts of V_{CC} or to within 0.7 volts of V_{BAT}. This write protection mechanism occurs as V_{CC} falls below V_{CCTP} as specified. If $\overline{CEI}$ is

low at the time power-fail detection occurs, $\overline{CEO}$ is held in its present state until $\overline{CEI}$ is returned high, or the period t_{CE} expires. This delay of write protection until the current memory cycle is completed prevents the corruption of data. If $\overline{CEO}$ is in an inactive state at the time of V_{CC} fail detection, $\overline{CEO}$ will be unconditionally disabled within t_{CF}. During nominal supply conditions $\overline{CEO}$ will follow $\overline{CEI}$ with a maximum propagation delay of 20 ns. Figure 7 shows a typical nonvolatile SRAM application.

FRESHNESS SEAL

In order to conserve battery capacity during storage and/or shipment of an end system, the DS1236 provides a freshness seal to electrically disconnect the battery. Figure 8 depicts the three pulses below ground on the IN pin required to invoke the freshness seal. The freshness seal will be disconnected and normal operation will begin when V_{CC} is cycled and reapplied to a level above V_{BAT}.

To prevent negative pulses associated with noise from setting the freshness mode in system applications, a series diode and resistor can be used to shunt noise to ground. During manufacturing, the freshness seal can still be set by holding TP2 at -3 volts while applying the 0 to –3 volts clock to TP1.

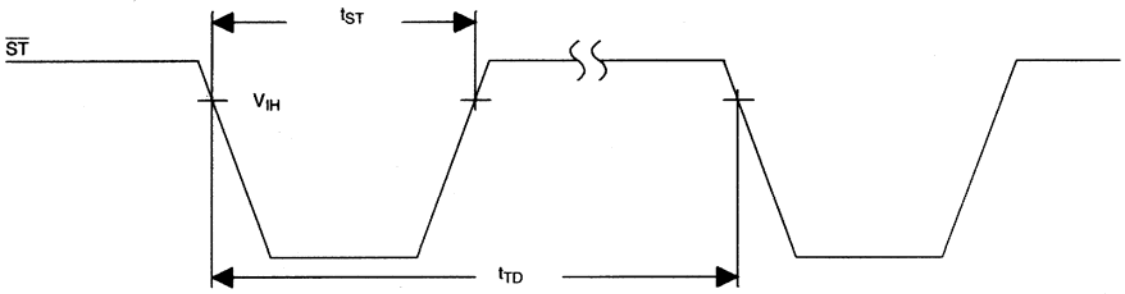
POWER SWITCHING

When larger operating currents are required in a battery backed system, the 5-volt supply and battery supply switches internal to the DS1236 may not be large enough to support the required load through V_{CCO} with a reasonable voltage drop. For these applications, the PF and $\overline{PF}$ outputs are provided to gate external power switching devices. As shown in Figure 9, power to the load is switched from V_{CC} to battery on power-down, and from battery to V_{CC} on power-up. The DS1336 is designed to use the $\overline{PF}$ output to switch between V_{BAT} and V_{CC}. It provides better leakage and switchover performance than currently available discrete components. The transition threshold for PF and $\overline{PF}$ is set to the external battery voltage V_{BAT}, allowing a smooth transition between sources. The load applied to the PF pin from the external switch will be supplied by the battery. Therefore, if a discrete switch is used, this load should be taken into consideration when sizing the battery.

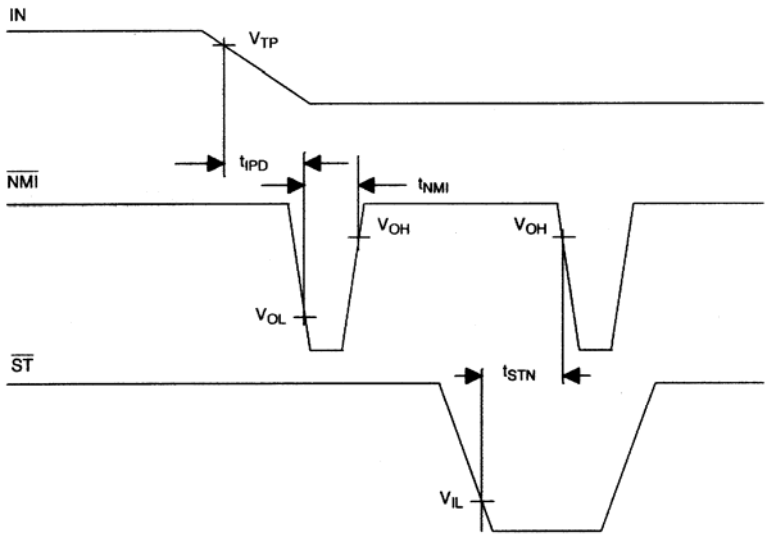
RESET CONTROL

As mentioned above, the DS1236 supports two modes of operation. The CMOS mode is used when the system incorporates a CMOS microprocessor which is battery backed. The NMOS mode is used when a non-battery backed processor is incorporated. The mode is selected by the RC (Reset Control) pin. The level of this pin distinguishes timing and level control on RST, $\overline{RST}$, and $\overline{NMI}$ outputs for volatile processor operation versus nonvolatile battery backup or battery operated processor applications.

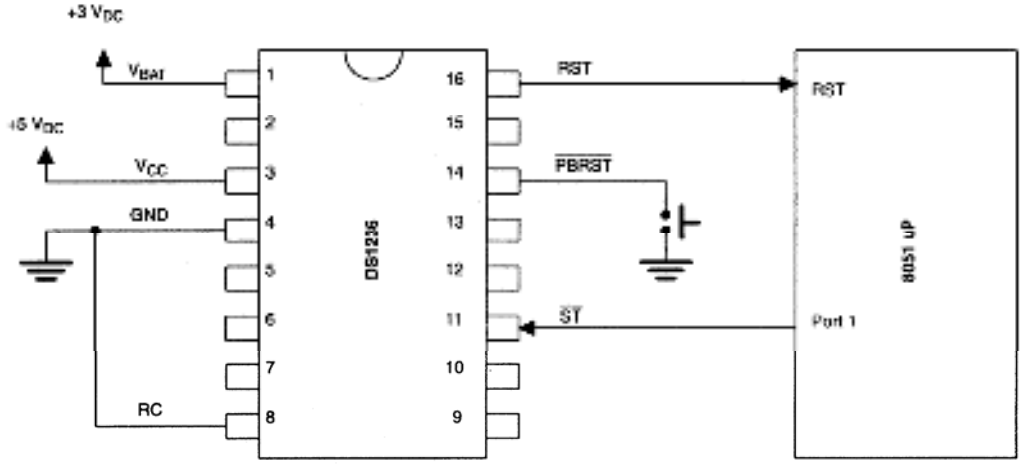
ST/INPUT TIMING Figure 2



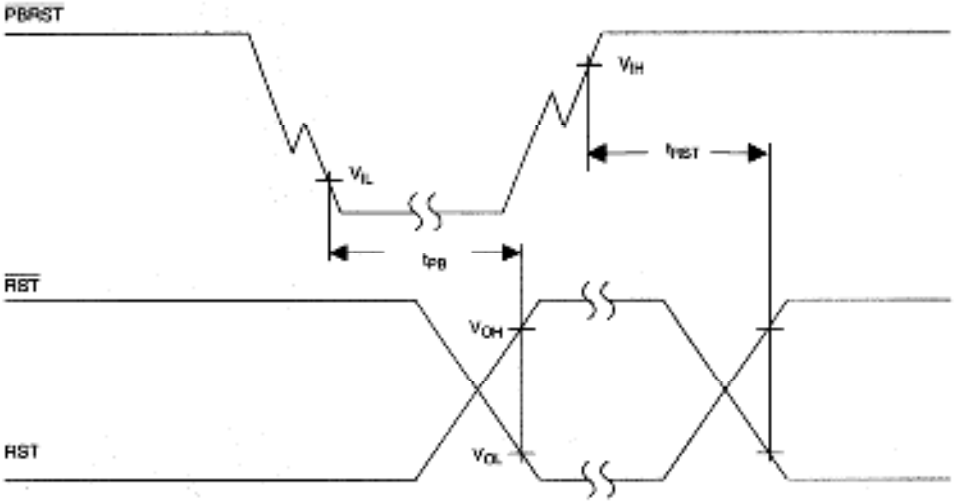
NMI/FROM ST/INPUT Figure 3



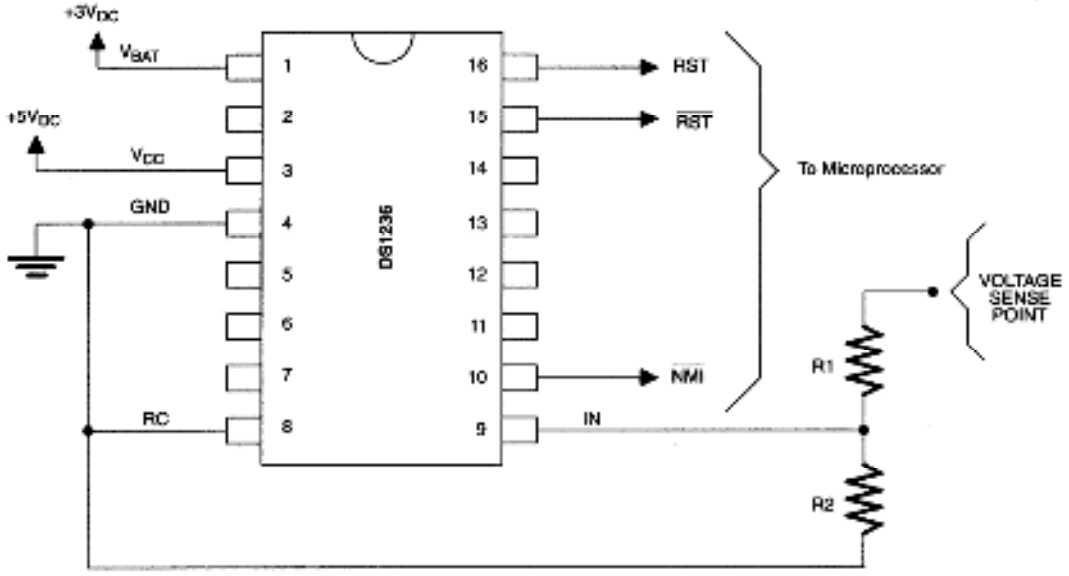
POWER MONITOR, WATCHDOG Figure 4



PUSH BUTTON RESET TIMING Figure 5



NON-MASKABLE INTERRUPT Figure 6



EXAMPLE 1: 5 VOLT SUPPLY, R2 = 10k OHM, V_{SENSE} = 4.80 VOLTS

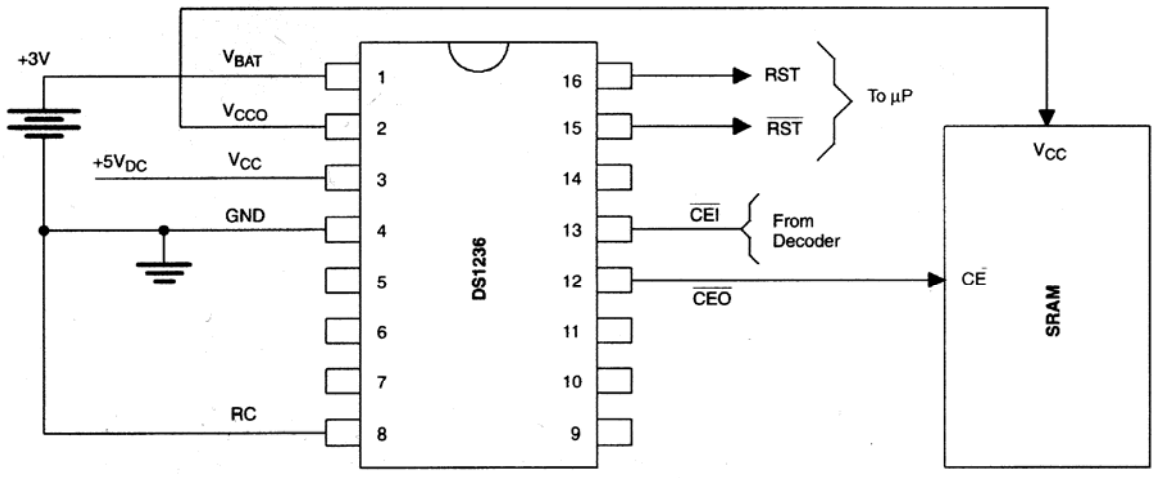
$$\therefore 4.80 = \frac{R1+10k}{10k} \text{ X } 2.54 \qquad R1 = 8.9k \text{ OHM}$$

EXAMPLE 2: 12 VOLT SUPPLY, R2 = 10k OHM, V_{SENSE} = 9.00 VOLTS

$$\therefore 9.00 = \frac{R1+10k}{10k} \text{ X } 2.54 \qquad R1 = 25.4k \text{ OHM}$$

$$V_{MAX} = \frac{9.00}{2.54} \text{ X } 5.00 = 17.7 \text{ VOLTS}$$

NONVOLATILE SRAM Figure 7



When the RC pin is tied to ground, the DS1236 is designed to interface with NMOS processors which do not have the microamp currents required during a battery backed mode. Grounding the RC pin does, however, continue to support nonvolatile backup of system SRAM memory. Nonvolatile systems incorporating NMOS processors generally require that only the SRAM memory and/or timekeeping functions be battery backed. When the processor is not battery backed (RC = 0), all signals connected from the processor to the DS1236 are disconnected from the backup battery supply, or grounded when system V_{CC} decays below V_{BAT}. In the NMOS processor system, the principal emphasis is placed on giving early warnings with $\overline{NMI}$, then providing a continuously active RST and RST signal during power-down while isolating the backup battery from the processor during a loss of V_{CC}.

During power-down, $\overline{NMI}$ will pulse low for a minimum of 200 µs, and then return high. If RC is tied low (NMOS mode), the voltage on $\overline{NMI}$ will follow V_{CC} until V_{CC} supply decays to V_{BAT}, at which point $\overline{NMI}$ will enter tri-state (see timing diagram). Also, upon V_{CC} out-of-tolerance at V_{CCTP}, the RST and $\overline{RST}$ outputs are driven active and RST will follow V_{CC} as the supply decays. On power-up, RST follows V_{CC} up, $\overline{RST}$ is held low, and both remain active for t_{RST} after valid V_{CC}. During a power-up from a V_{CC} voltage below V_{BAT}, any detected IN pin levels below V_{TP} are disabled from reaching the $\overline{NMI}$ pin until V_{CC} rises to V_{CCTP}. As a result, any potential $\overline{NMI}$ pulse will not be initiated until V_{CC} reaches V_{CCTP}. Removal of an active low level on the $\overline{NMI}$ pin is controlled by either an internal time-out (when the IN pin is less than V_{TP}), or by the subsequent rise of the IN pin above V_{TP}. The initiation and removal of the $\overline{NMI}$ signal results in an $\overline{NMI}$ pulse of 0 µs minimum to 500 µs maximum during power-up, depending on the relative voltage relationship between V_{CC} and the IN pin. As an example, when the IN pin is tied to ground, the internal timeout will result in a pulse of 200 µs minimum to 500 µs maximum. In contrast, if the IN pin is tied to V_{CCO}, $\overline{NMI}$ will not produce a pulse on power-up.

Connecting the RC pin to a high (V_{CCO}) invokes CMOS mode and provides nonvolatile support to both the system SRAM as well as a low power CMOS processor. When using CMOS microprocessors, it is possible to place the microprocessor into a very low-power mode termed the “stop” or “halt” mode. In this state the CMOS processor requires only microamp currents and is fully capable of being battery backed. This mode generally allows the CMOS microprocessor to maintain the contents of internal RAM as well as state control of I/O ports during battery backup. The processor can subsequently be restarted by any of several different signals. To maintain this low-power state, the DS1236 issues no $\overline{NMI}$ and/or reset signals to the processor until it is time to bring the processor back into full operation. To support the low-power processor battery backed mode (RC = 1), the DS1236 provides a pulsed $\overline{NMI}$ for early power failure warning. Waiting to initiate a Stop mode until after the $\overline{NMI}$ pin has returned high will guarantee the processor that no other active $\overline{NMI}$ or RST/$\overline{RST}$ will be issued by the DS1236 until one of two conditions occurs: 1) Voltage on the pin rises above V_{TP}, which activates the watchdog, or 2) V_{CC} cycles below then above V_{BAT}, which also results in an active RST and $\overline{RST}$. If V_{CC} does not fall below V_{CCTP}, the processor will be restarted by the reset derived from the watchdog timer as the IN pin rises above V_{TP}.

With the RC pin tied to V_{CCO}, RST and $\overline{RST}$ are not forced active as V_{CC} collapses to V_{CCTP}. The $\overline{RST}$ is held at a high level via the external battery as V_{CC} falls below battery potential. This mode of operation is intended for applications in which the processor is made nonvolatile with an external source, and allows the processor to power down into a Stop mode as signaled from $\overline{NMI}$ at an earlier voltage level. The $\overline{NMI}$ output pin will pulse low for t_{NMI} following a low voltage detect at the IN pin of V_{TP}. Following t_{NMI}, however, $\overline{NMI}$ will also be held at a high level (V_{BAT}) by the battery as V_{CC} decays below V_{BAT}. On power-up, RST and $\overline{RST}$ are held inactive until V_{CC} reaches V_{BAT}, then RST and $\overline{RST}$ are driven active for t_{RST}. If the IN pin falls below V_{TP} during an active reset, the reset outputs will be forced inactive by the $\overline{NMI}$ output. In addition, as long as the IN pin is less than V_{TP}, stimulation of the ST pin will result in

additional $\overline{NMI}$ pulses. In this way, the $\overline{ST}$ pin can be used to allow the CMOS processor to determine if the supply voltage, as monitored by the IN pin, is above or below a selected operating value. This is illustrated in Figure 3. As discussed above, the RC pin determines the timing relationships and levels of several signals. The following section describes the power-up and power-down timing diagrams in more detail.

TIMING DIAGRAMS

This section provides a description of the timing diagrams shown in Figure 10, Figure 11, Figure 12, and Figure 13. These diagrams show the relative timing and levels in both the NMOS and the CMOS mode for power-up and down. Figure 10 illustrates the relationship for power-down in CMOS mode. As V_{CC} falls, the IN pin voltage drops below V_{TP}. As a result, the processor is notified of an impending power failure via an active $\overline{NMI}$, which allows it to enter a sleep mode. As the power falls further, V_{CC} crosses V_{CCTP}, the power monitor trip point. Since the DS1236 is in CMOS mode, no reset is generated. The $\overline{RST}$ voltage will follow V_{CC} down, but will fall no further than V_{BAT}. At this time, $\overline{CEO}$ is brought high to write protect the RAM. When the V_{CC} reaches V_{BAT}, a power-fail is issued via the PF and $\overline{PF}$ pins.

Figure 11 illustrates operation of the power-down sequence in NMOS mode. Once again, as power falls, an $\overline{NMI}$ is issued. This gives the processor time to save critical data in nonvolatile SRAM. When V_{CC} reaches V_{CCTP}, an active RST and $\overline{RST}$ are given. The RST voltage will follow V_{CC} as it falls. $\overline{CEO}$, PF, and $\overline{PF}$ will operate in a similar manner to CMOS mode. Notice that the $\overline{NMI}$ will tri-state to prevent a loss of battery power.

Figure 12 shows the power-up sequence for the NMOS mode. As V_{CC} slews above V_{BAT}, the PF and $\overline{PF}$ pins are deactivated. An active reset occurs as well as an $\overline{NMI}$. Although the $\overline{NMI}$ may be short due to slew rates, reset will be maintained for the standard t_{RST} timeout period. At a later time, if the IN pin falls below V_{TP}, a new $\overline{NMI}$ will occur. If the processor does not issue a $\overline{ST}$, a watchdog reset will also occur. The second $\overline{NMI}$ and RST are provided to illustrate these possibilities.

Figure 13 illustrates the power-up timing for CMOS mode. The principal difference is that the DS1236 issues a reset immediately in the NMOS mode. In CMOS mode, a reset is issued when IN rises above V_{TP}. Depending on the processor type, the $\overline{NMI}$ may terminate the Stop mode in the processor.

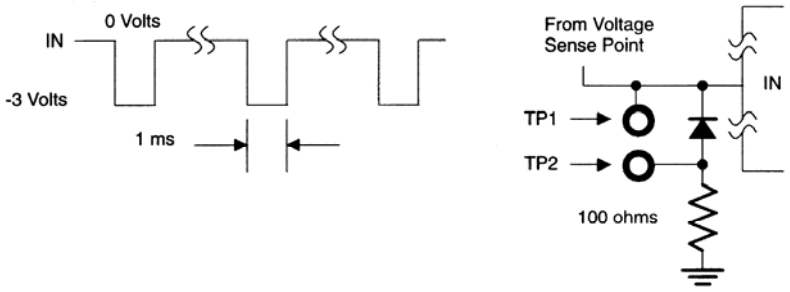
WAKE CONTROL/SLEEP CONTROL

The Wake/Sleep Control input (WC/$\overline{SC}$) allows the processor to disable all comparators on the DS1236 before entering the Stop mode. This feature allows the DS1236, processor, and static RAM to maintain nonvolatility in the lowest power mode possible. The processor may invoke the sleep mode in battery operated applications to conserve battery capacity when an absence of activity is detected. The operation of this signal is shown in Figure 14. The DS1236 may subsequently be restarted by a high-to-low transition on the $\overline{PBRST}$ input through human interface via a keyboard, touchpad, etc. The processor will then be restarted as the watchdog times out and drives RST and $\overline{RST}$ active. The DS1236 can also be started up by forcing the WC/$\overline{SC}$ pin high from an external source. Also, if the DS1236 is placed in a sleep mode by the processor and system power is lost, the DS1236 will wake up the next time V_{CC} rises above V_{BAT}. These possibilities are illustrated in Figure 15.

When the sleep mode is invoked during normal power-valid conditions, all operation on the DS1236 is disabled, thus leaving the $\overline{NMI}$, RST, and $\overline{RST}$ outputs disabled as well as the $\overline{ST}$ and IN inputs. However, a loss of power during a sleep mode will result in an active RST and $\overline{RST}$ when the RC pin is grounded (NMOS mode). If the RC pin is tied high, the RST and $\overline{RST}$ pins will remain inactive during

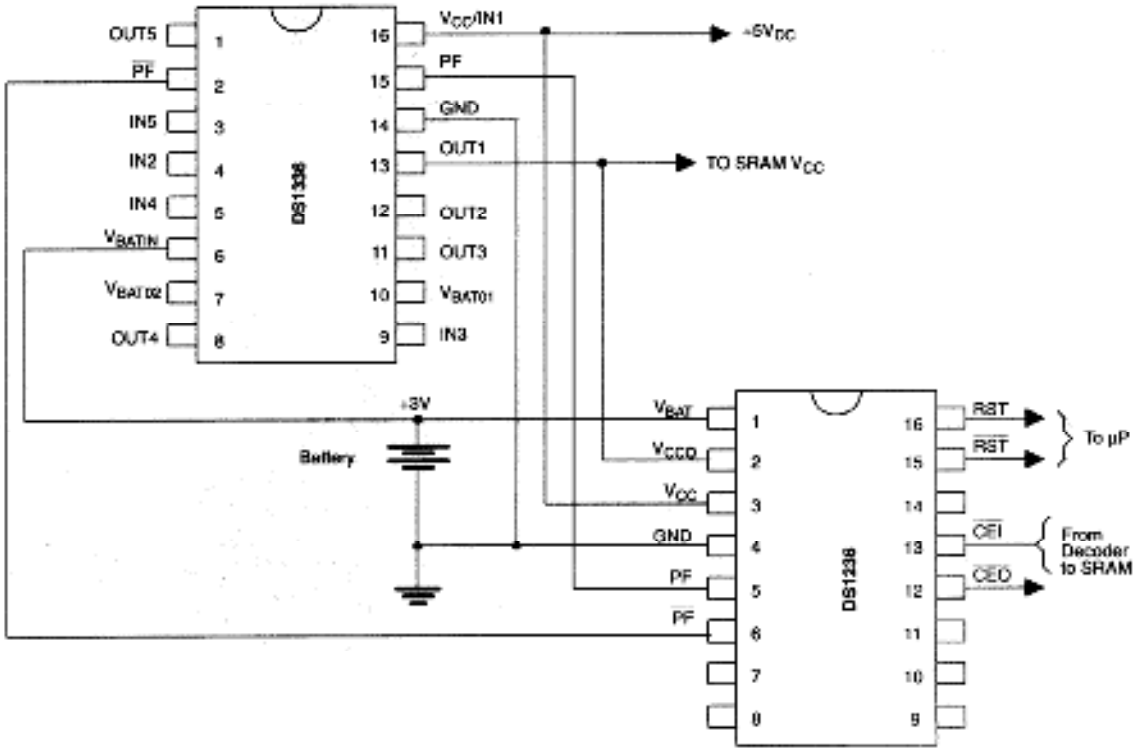
power-down in a sleep mode. Removal of the sleep mode by the $\overline{PBRST}$ input is not affected by the IN pin threshold at V_{TP} when the RC pin is tied high (CMOS mode). Subsequent power-up of the V_{CC} supply with the RC pin tied high will activate the RST and $\overline{RST}$ outputs as the main supply rises above V_{BAT}. A high-to-low transition on the WC/$\overline{SC}$ pin must follow a high-to-low transition on the ST pin by t_{WC} to invoke a Sleep mode for the DS1236.

FRESHNESS SEAL Figure 8

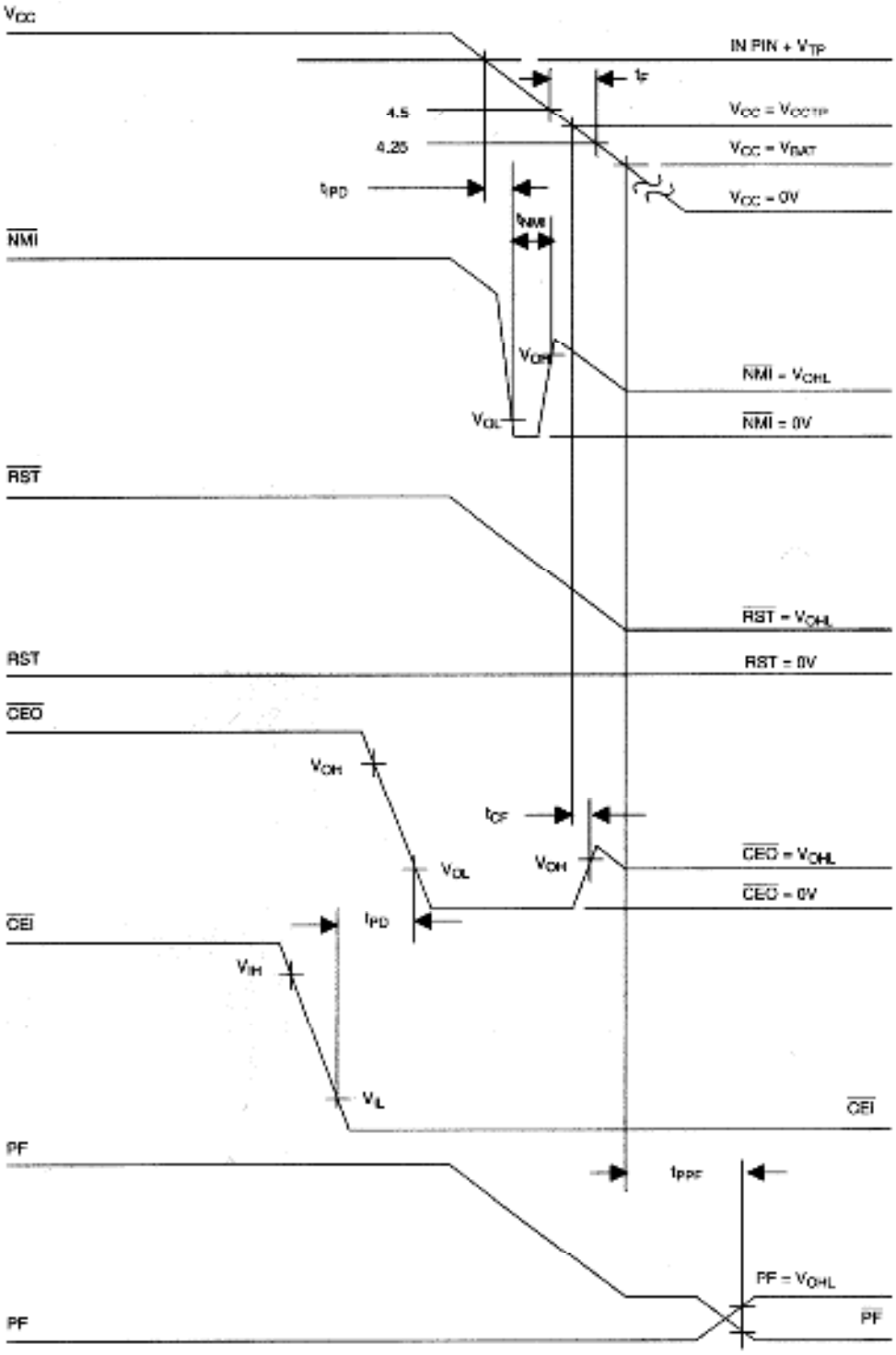


NOTE: This series of pulses must be applied during normal +5 volt operation.

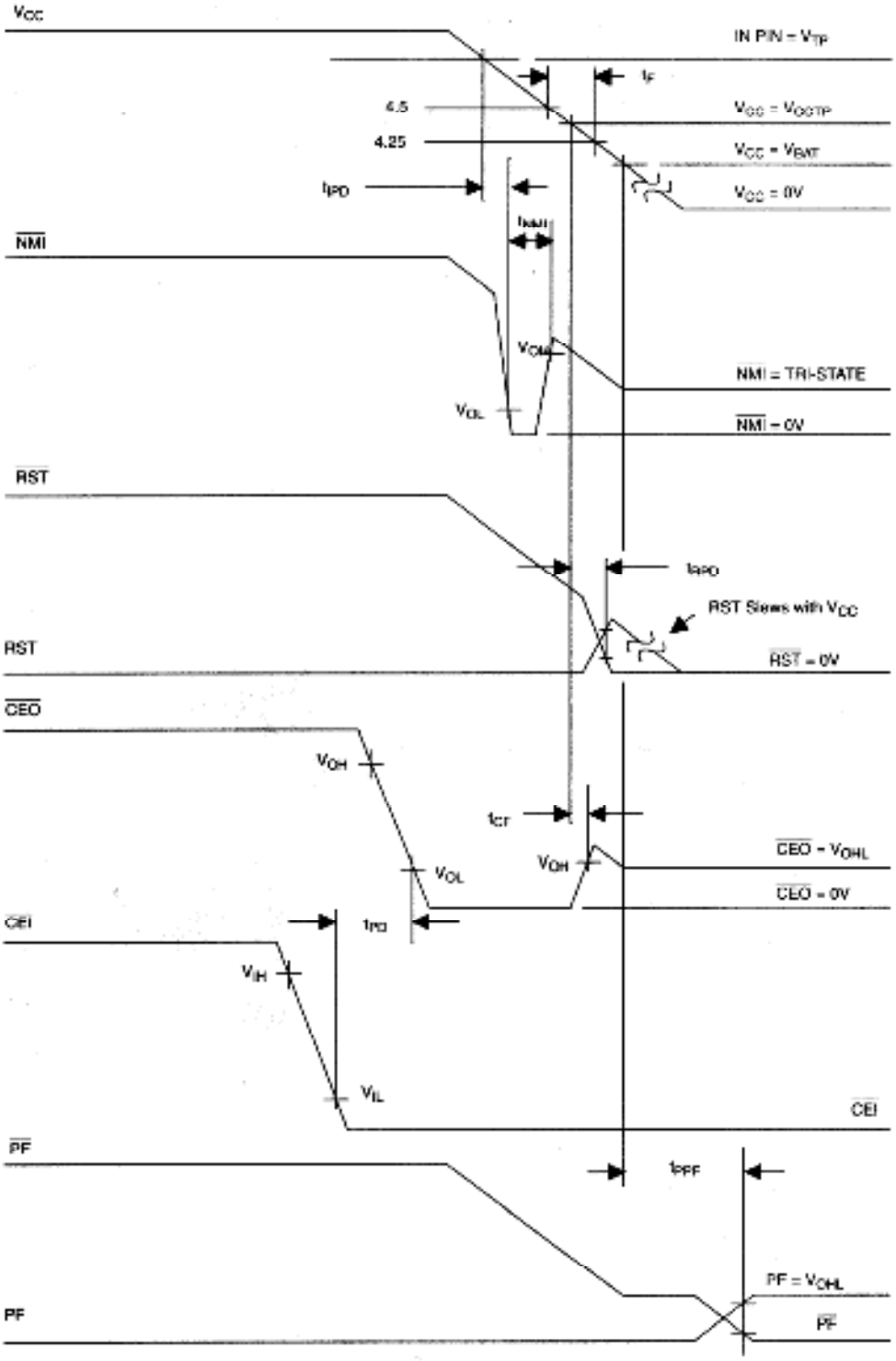
POWER SWITCHING Figure 9



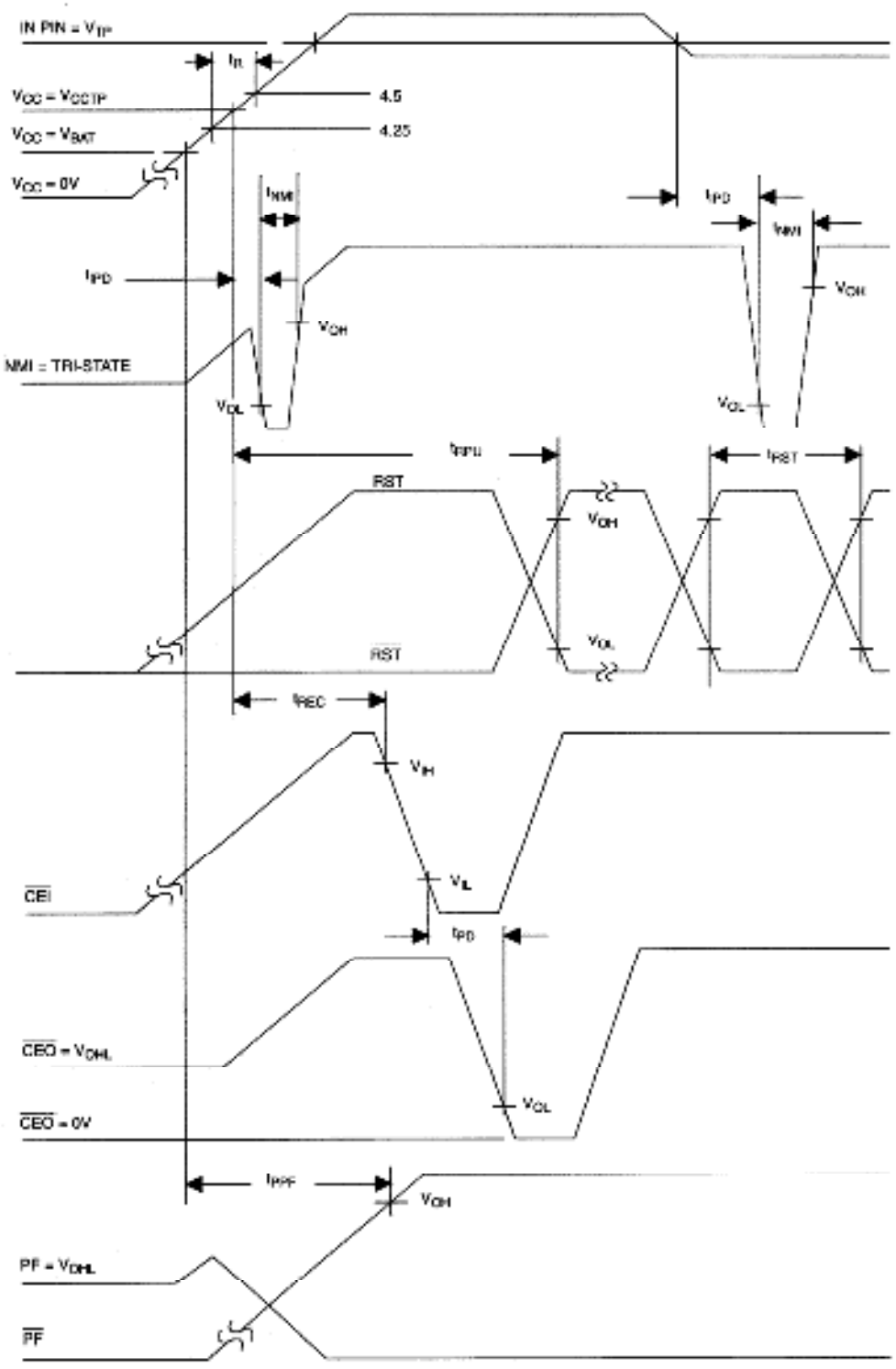
CMOS MODE POWER-DOWN (RC = V_{CCO}) Figure 10



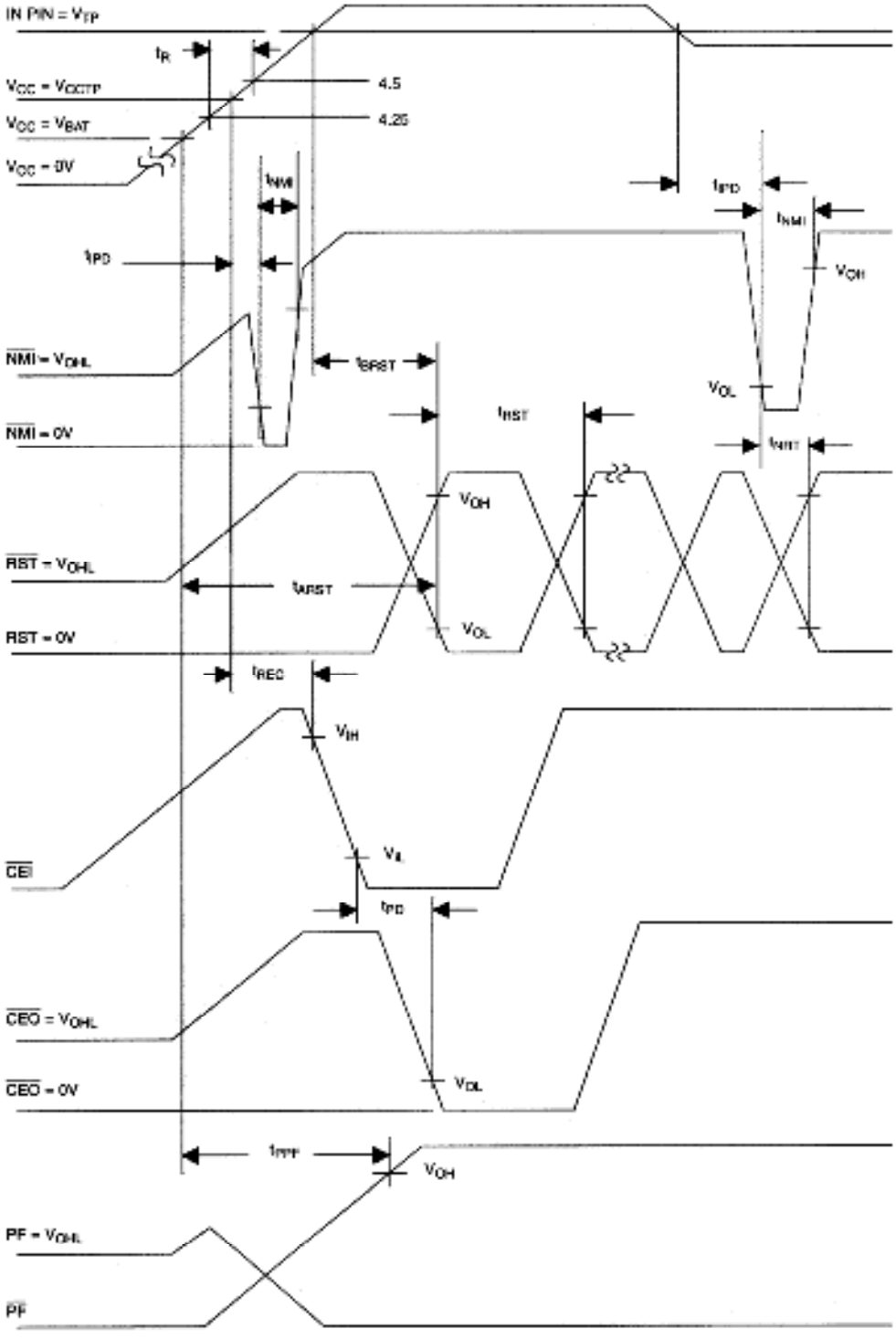
NMOS MODE POWER-DOWN (RC = GND) Figure 11



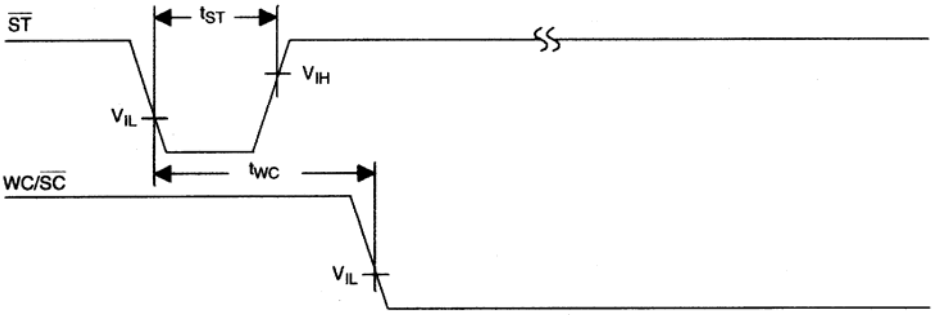
NMOS MODE POWER-UP (RC = GND) Figure 12



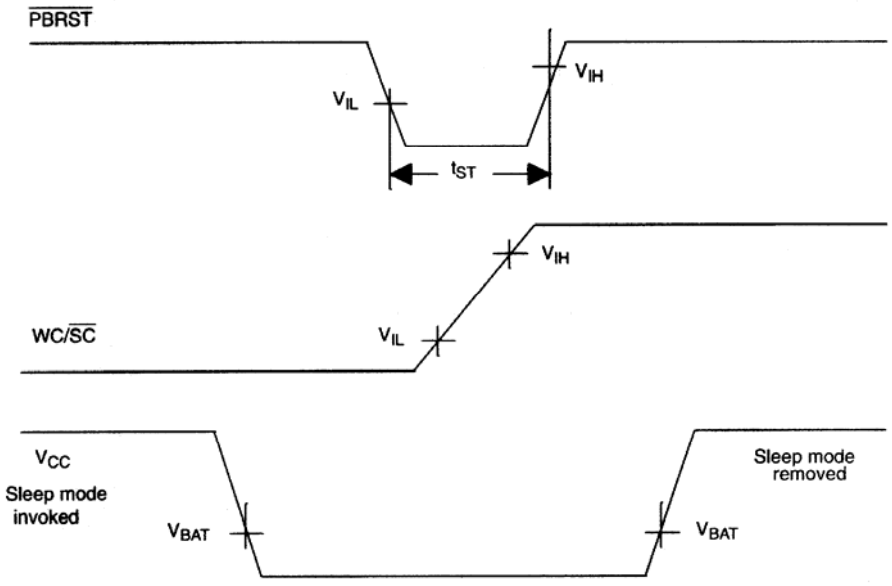
CMOS MODE POWER-UP (RC = V_{CCO}) Figure 13



WAKE/SLEEP CONTROL Figure 14



OPTIONS FOR INVOKING WAKEUP Figure 15



ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Pin Relative to Ground	-0.5V to +7.0V
Voltage on I/O Relative to Ground	-0.5V to V_{CC} + 0.5V
Voltage on IN Pin Relative to Ground	-3.5V to V_{CC} + 0.5V
Operating Temperature	0°C to 70°C
Operating Temperature (Industrial Version)	-40°C to +85°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Supply Voltage (5% Option)	V_{CC}	4.75	5.0	5.5	V	1
Input High Level	V_{IH}	2.0		V_{CC}+0.3	V	1
Input Low Level	V_{IL}	-0.3		+0.8	V	1
IN Input Pin	V_{IN}	-0.3		V_{CC}+0.3	V	1
Battery Input	V_{BAT}	2.7		4.0	V	1

DC ELECTRICAL CHARACTERISTICS (0°C to 70°C; V_{CC}= 4.5V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{CC}			4	mA	2
Sleep Supply Current in Sleep mode	I_{CC}			20	µA	
Battery Current	I_{BAT}			0.1	µA	2
Supply Output Current (V_{CCO}=V_{CC} - 0.3V)	I_{CC01}			100	mA	3
Supply Output Current in Data Retention (V_{CC} < V_{BAT})	I_{CC02}			1	mA	4
Supply Output Voltage	V_{CCO}		V_{CC}-0.3		V	1
Battery Backup Voltage	V_{CCO}		V_{BAT}-0.7		V	1, 6
Low Level @ RST	V_{OL}			0.4	V	1
Output Voltage @ -500 µA	V_{OH}	V_{CC}-0.5V	V_{CC}-0.1V		V	1
$\overline{CEO}$ and PF Output	V_{OHL}		V_{BAT}-0.7		V	1, 6
$\overline{PBRST}$ Pull-up Resist	R_{PBRST}	10k			Ohms	
Input Leakage Current	I_{LI}	-1.0		+1.0	µA	18
Output Leakage Current	I_{LO}	-1.0		+1.0	µA	18
Output Current @ 0.4V	I_{OL}	4.0			mA	12

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Output Current @ 2.4V	I_{OH}			-1.0	mA	13
Power Sup. Trip Point	V_{CCTP}	4.25	4.37	4.50	V	1
Power Supply Trip (5% Option)	V_{CCTP}	4.50	4.62	4.75	V	1
IN Input Pin Current	I_{CCIN}	-1.0		+1.0	µA	
IN Input Trip Point	V_{TP}	2.5	2.54	2.6	V	1

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC}= 4.5V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V_{CC} Fail Detect to RST, $\overline{RST}$	t_{RPD}	40	100	175	µs	
V_{TP} to $\overline{NMI}$	t_{IPD}	40	100	175	µs	
RESET Active Time	t_{RST}	25	100	150	ms	
$\overline{NMI}$ Pulse Width	t_{NMI}	200	300	500	µs	14
$\overline{ST}$ Pulse Width	t_{ST}	20			ns	19
$\overline{PBRST}$ @ V_{IL}	t_{PB}	40			ms	
V_{CC} Slew Rate 4.75 to 4.25	t_F	300			µs	
Chip Enable Propagation Delay	t_{PD}			20	ns	
V_{CC} Fail to Chip Enable High	t_{CF}	7	12	44	µs	17
V_{CC} Valid to RST, $\overline{RST}$ (RC=1)	t_{FPU}			100	ns	
V_{CC} Valid to RST & $\overline{RST}$	t_{RPU}	25	100	150	ms	5
V_{CC} Slew to 4.24 to V_{BAT}	t_{FB1}	10			µs	7
V_{CC} Slew 4.25 to 4.75 V_{BAT}	t_{FB2}	100			µs	8
Chip Enable Output Recovery Time	t_{REC}	.1			µs	9
V_{CC} Slew 4.25 to 4.75	t_R	0			µs	
Chip Enable Pulse Width	t_{CE}			5	s	10
Watchdog Time Delay	t_{TD}	100	400	600	ms	
$\overline{ST}$ to WC/$\overline{SC}$	t_{WC}	0.1		50	µs	
V_{BAT} Detect to PF, $\overline{PF}$	t_{PPF}			2	µs	7
$\overline{ST}$ to $\overline{NMI}$	t_{STN}			30	ns	11
$\overline{NMI}$ to RST & $\overline{RST}$	t_{NRT}			30	ns	
V_{BAT} Detect to RST & $\overline{RST}$	t_{ARST}			200	µs	15
V_{CC} Valid to RST, $\overline{RST}$	t_{BRST}	30	100	150	µs	16

CAPACITANCE

(t_A=25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

NOTES:

1. All voltages referenced to ground. A 0.1 µF capacitor is recommended between V_{CC} and GND.
2. Measured with V_{CCO}, $\overline{CEO}$, PF, $\overline{ST}$, $\overline{PBRST}$, RST, $\overline{RST}$, and $\overline{NMI}$ pin open. I_{BAT} specified at 25°C.
3. I_{CCO1} is the maximum average load which the DS1236 can supply at V_{CC}-0.3V through the V_{CCO} pin during normal 5-volt operation.
4. I_{CCO2} is the maximum average load which the DS1236 can supply through the V_{CCO} pin during data retention battery supply operation, with a maximum drop of 0.8 volts.
5. With t_R = 5 µs.
6. V_{CCO} is approximately V_{BAT}-0.5V at 1 µA load.
7. Sleep mode is not invoked.
8. Sleep mode is invoked.
9. t_{REC} is the minimum time required before $\overline{CEI}$ / $\overline{CEO}$ memory access is allowed.
10. t_{CE} maximum must be met to ensure data integrity on power loss.
11. IN input is less than V_{TP} but V_{CC} greater than V_{CCTP}.
12. All outputs except RST which is 25 µA minimum.
13. All outputs except $\overline{RST}$ and $\overline{NMI}$ which is 25 µA maximum.
14. Pulse width of $\overline{NMI}$ requires that the IN pin remain below V_{TP}. If the IN pin returns to a level above V_{TP} for a period longer than t_{IPD} and before the t_{NMI} period has elapsed, the $\overline{NMI}$ pin will immediately return to a high.
15. IN pin greater than V_{TP} when V_{CC} supply rises to V_{BAT}. Example: IN tied to GND.
16. IN pin less than V_{TP} when V_{CC} supply rises to V_{BAT}.
17. $\overline{CEI}$ low.
18. The WC/$\overline{SC}$ pin contains an internal latch which drives back on to the pin. This latch requires ±200 µamps to switch states. The $\overline{ST}$ pin will sink ±50 µamps in normal operation and ±1 µamp in the sleep mode.
19. $\overline{ST}$ should be active low before the watchdog is disabled (i.e., before the $\overline{ST}$ input is tristated).

