DS15BR400/DS15BR401 4-Channel LVDS Buffer/Repeater with Pre-Emphasis

Check for Samples: DS15BR400, DS15BR401

FEATURES

- **DC to 2 Gbps Low Jitter, High Noise Immunity, Low Power Operation**
- **6 dB of Pre-emphasis Drives Lossy Backplanes and Cables**
- **LVDS/CML/LVPECL Compatible Input, LVDS Output**
- **On-chip 100 Ω output termination, optional 100 Ω Input Termination**
- **15 kV ESD Protection on LVDS Inputs and Outputs**
- **Single 3.3V Supply**
- **Industrial -40 to +85°C Temperature Range**
- **Space Saving WQFN-32 or TQFP-48 Packages**

APPLICATIONS

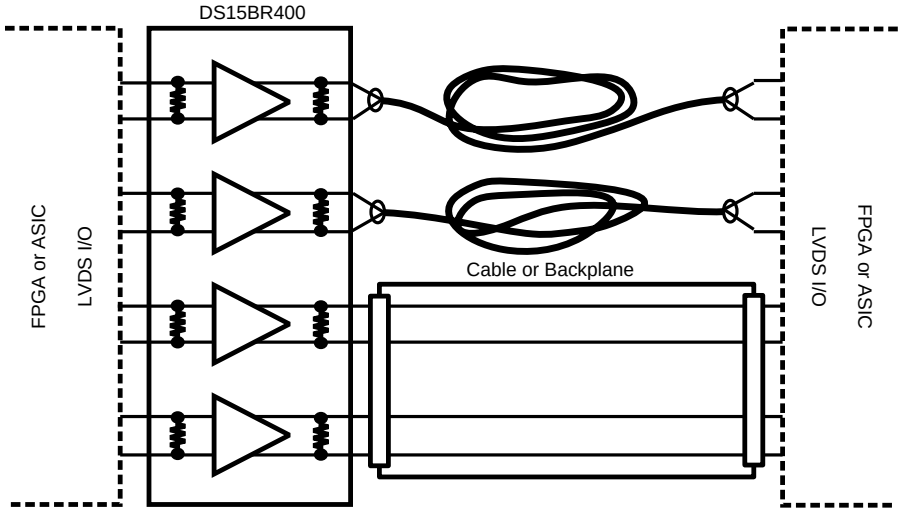
- **Cable Extension Applications**
- **Signal Repeating and Buffering**
- **Digital Routers**

DESCRIPTION

The DS15BR400/DS15BR401 are four channel LVDS buffer/repeaters capable of data rates of up to 2 Gbps. High speed data paths and flow-through pinout minimize internal device jitter and simplify board layout, while pre-emphasis overcomes ISI jitter effects from lossy backplanes and cables. The differential inputs interface to LVDS, and Bus LVDS signals such as those on TI's 10-, 16-, and 18- bit Bus LVDS SerDes, as well as CML and LVPECL. The differential inputs and outputs of the DS15BR400 are internally terminated with 100Ω resistors to improve performance and minimize board space. The DS15BR401 does not have input termination resistors. The repeater function is especially useful for boosting signals for longer distance transmission over lossy cables and backplanes.

The DS15BR400/DS15BR401 are powered from a single 3.3V supply and consume 578 mW (typ). They operate over the full -40°C to +85°C industrial temperature range and are available in space saving WQFN-32 and TQFP-48 packages.

Typical Application



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Block and Connection Diagrams

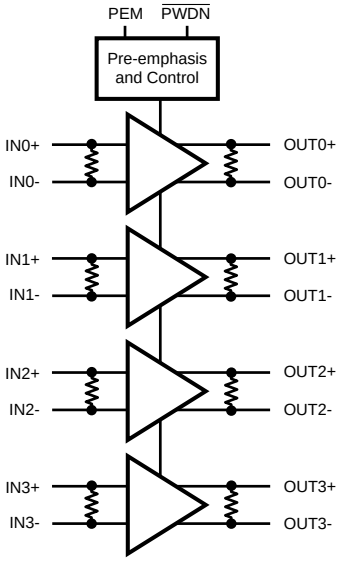


Figure 1. DS15BR400 Block Diagram

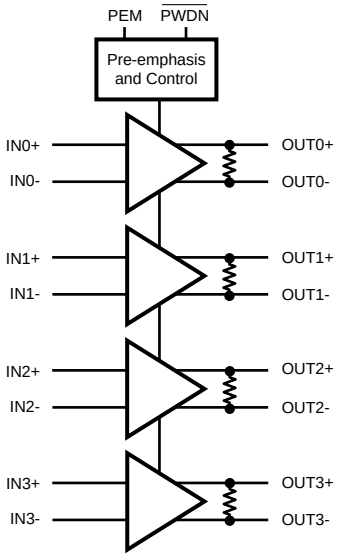


Figure 2. DS15BR401 Block Diagram

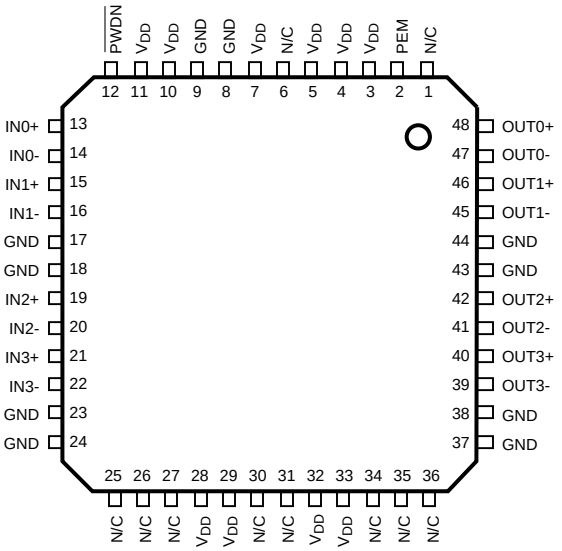


Figure 3. TQFP Pinout - Top View
Package Number PFB0048A

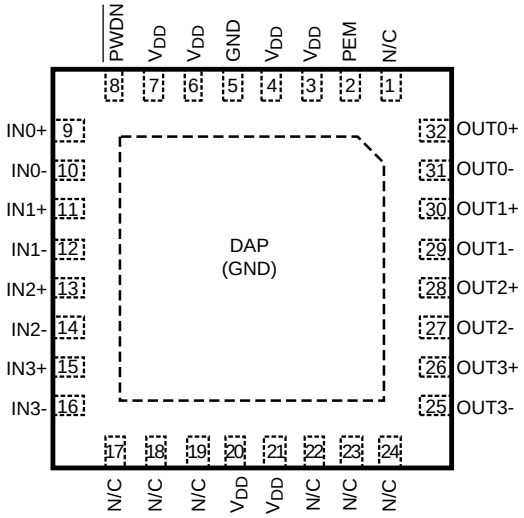


Figure 4. WQFN Pinout - Top View
Package Number RTV0032A

PIN DESCRIPTIONS

Pin Name	TQFP Pin Number	WQFN Pin Number	I/O, Type	Description
DIFFERENTIAL INPUTS				
IN0+ IN0−	13 14	9 10	I, LVDS	Channel 0 inverting and non-inverting differential inputs.
IN1+ IN1−	15 16	11 12	I, LVDS	Channel 1 inverting and non-inverting differential inputs.
IN2+ IN2−	19 20	13 14	I, LVDS	Channel 2 inverting and non-inverting differential inputs.
IN3+ IN3−	21 22	15 16	I, LVDS	Channel 3 inverting and non-inverting differential inputs.

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PIN DESCRIPTIONS (continued)

Pin Name	TQFP Pin Number	WQFN Pin Number	I/O, Type	Description
DIFFERENTIAL OUTPUTS				
OUT0+ OUT0−	48 47	32 31	O, LVDS	Channel 0 inverting and non-inverting differential outputs. (1)
OUT1+ OUT1−	46 45	30 29	O, LVDS	Channel 1 inverting and non-inverting differential outputs. (1)
OUT2+ OUT2−	42 41	28 27	O, LVDS	Channel 2 inverting and non-inverting differential outputs. (1)
OUT3+ OUT3-	40 39	26 25	O, LVDS	Channel 3 inverting and non-inverting differential outputs. (1)
DIGITAL CONTROL INTERFACE				
$\overline{\text{PWDN}}$	12	8	I, LVTTL	A logic low at $\overline{\text{PWDN}}$ activates the hardware power down mode (all channels).
PEM	2	2	I, LVTTL	Pre-emphasis Control Input (affects all Channels)
POWER				
V_{DD}	3, 4, 5, 7, 10, 11, 28, 29, 32, 33	3, 4, 6, 7, 20, 21	I, Power	V_{DD} = 3.3V, ±10%
GND	8, 9, 17, 18, 23, 24, 37, 38, 43, 44	5 (2)	I, Ground	Ground reference for LVDS and CMOS circuitry. For the WQFN package, the DAP is used as the primary GND connection to the device in addition to the pin numbers listed. The DAP is the exposed metal contact at the bottom of the WQFN-32 package. It should be connected to the ground plane with at least 4 vias for optimal AC and thermal performance.
N/C	1,6, 25, 26, 27, 30, 31, 34, 35, 36	1, 17, 18,19,22, 23, 24		No Connect

(1) The LVDS outputs do not support a multidrop (BLVDS) environment. The LVDS output characteristics of the DS15BR400 and DS15BR401 are optimized for point-to-point backplane and cable applications.
(2) Note that for the WQFN package the GND is connected thru the DAP on the back side of the WQFN package in addition to the actual pin numbers listed.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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Absolute Maximum Ratings(1)

Supply Voltage (V_{DD})	−0.3V to +4.0V
CMOS Input Voltage	−0.3V to (V_{DD}+0.3V)
LVDS Receiver Input Voltage	−0.3V to (V_{DD}+0.3V)
LVDS Driver Output Voltage	−0.3V to (V_{DD}+0.3V)
LVDS Output Short Circuit Current	+40 mA
Junction Temperature	+150°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Solder, 4sec)	260°C
Max Pkg Power Capacity @ 25°C TQFP WQFN	 1.64W 4.16W
Thermal Resistance (θ_{JA}) TQFP WQFN	 76°C/W 30°C/W
Package Derating above +25°C TQFP WQFN	 13.2mW/°C 33.3mW/°C
ESD Last Passing Voltage HBM, 1.5kΩ, 100pF	 8 kV
LVDS pins to GND only	15 kV
EIAJ, 0Ω, 200pF	250V
Charged Device Model	1000V

(1) Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. TI does not recommend operation of products outside of recommended operation conditions.

Recommended Operating Conditions

Supply Voltage (V_{DD})	3.0V to 3.6V
Input Voltage (V_I) (1)	0V to V_{DD}
Output Voltage (V_O)	0V to V_{DD}
Operating Temperature (T_A)	
Industrial	−40°C to +85°C

(1) V_{ID} max < 2.4V

Electrical Characteristics

Over recommended operating supply and temperature ranges unless other specified.

Symbol	Parameter	Conditions	Min	Typ (1)	Max	Units
LVCMOS DC SPECIFICATIONS ($\overline{PWDN}$, PEM)						
V_{IH}	High Level Input Voltage		2.0		V_{DD}	V
V_{IL}	Low Level Input Voltage		GND		0.8	V
I_{IH}	High Level Input Current	V_{IN} = V_{DD} = 3.6V ($\overline{PWDN}$ pin)	−10		+10	µA
I_{IHR}	High Level Input Current	V_{IN} = V_{DD} = 3.6V (PEM pin)	40		200	µA
I_{IL}	Low Level Input Current	V_{IN} = V_{SS}, V_{DD} = 3.6V	−10		+10	µA
C_{IN1}	LVCMOS Input Capacitance	Any Digital Input Pin to V_{SS}		5.5		pF
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA, V_{DD} = 0V	−1.5	−0.8		V

(1) Typical parameters are measured at V_{DD} = 3.3V, T_A = 25°C. They are for reference purposes, and are not production-tested.

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Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless other specified.

Symbol	Parameter	Conditions	Min	Typ (1)	Max	Units
LVDS INPUT DC SPECIFICATIONS (INn±)						
V_{TH}	Differential Input High Threshold (2)	V_{CM} = 0.8V to 3.55V, V_{DD} = 3.6V		0	100	mV
V_{TL}	Differential Input Low Threshold (2)	V_{CM} = 0.8V to 3.55V, V_{DD} = 3.6V	−100	0		mV
V_{ID}	Differential Input Voltage	V_{CM} = 0.8V to 3.55V, V_{DD} = 3.6V	100		2400	mV
V_{CMR}	Common Mode Voltage Range	V_{ID} = 150 mV, V_{DD} = 3.6V	0.05		3.55	V
C_{IN2}	LVDS Input Capacitance	IN+ or IN− to V_{SS}		3.0		pF
I_{IN}	Input Current	V_{IN} = 3.6V, V_{DD} = 3.6V	−10		+10	µA
		V_{IN} = 0V, V_{DD} = 3.6V	−10		+10	µA
LVDS OUTPUT DC SPECIFICATIONS (OUTn±)						
V_{OD}	Differential Output Voltage, 0% Pre-emphasis (2)	R_L = 100Ω external resistor between OUT+ and OUT− Figure 5	250	360	500	mV
ΔV_{OD}	Change in V_{OD} between Complementary States		−35		35	mV
V_{OS}	Offset Voltage (3)		1.05	1.18	1.475	V
ΔV_{OS}	Change in V_{OS} between Complementary States		−35		35	mV
C_{OUT}	LVDS Output Capacitance	OUT+ or OUT− to V_{SS}		2.5		pF
I_{OS}	Output Short Circuit Current	OUT+ or OUT− Short to GND		−21	−40	mA
		OUT+ or OUT− Short to VDD		6	40	mA
SUPPLY CURRENT (Static)						
I_{CC}	Supply Current	All inputs and outputs enabled and active, terminated with differential load of 100Ω between OUT+ and OUT-. PEM = L		175	215	mA
I_{CCZ}	Supply Current - Power Down Mode	$\overline{PWDN}$ = L, PEM = L		20	200	µA
SWITCHING CHARACTERISTICS—LVDS OUTPUTS						
t_{LHT}	Differential Low to High Transition Time (4)	Use an alternating 1 and 0 pattern at 200 Mbps, measure between 20% and 80% of V_{OD}. Figure 6 , Figure 8		170	250	ps
t_{HLT}	Differential High to Low Transition Time (4)			170	250	ps
t_{PLHD}	Differential Low to High Propagation Delay	Use an alternating 1 and 0 pattern at 200 Mbps, measure at 50% V_{OD} between input to output. Figure 6 , Figure 7		1.0	2.0	ns
t_{PHLD}	Differential High to Low Propagation Delay			1.0	2.0	ns
t_{SKD1}	Pulse Skew (4)	$\lvert t_{PLHD} - t_{PHLD} \rvert$		10	60	ps
t_{SKCC}	Output Channel to Channel Skew (4)	Difference in propagation delay (t_{PLHD} or t_{PHLD}) among all output channels.		25	75	ps
t_{SKP}	Part to Part Skew (4)	Common edge, parts at same temp and V_{CC}			550	ps

(2) Differential output voltage V_{OD} is defined as ABS(OUT+–OUT−). Differential input voltage V_{ID} is defined as ABS(IN+–IN−).
(3) Output offset voltage V_{OS} is defined as the average of the LVDS single-ended output voltages at logic high and logic low states.
(4) Not production tested. Ensured by a statistical analysis on a sample basis at the time of characterization.

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Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless other specified.

Symbol	Parameter	Conditions	Min	Typ (1)	Max	Units
t_{JIT}	Jitter (0% Pre-emphasis) (5)	RJ - Alternating 1 and 0 at 750 MHz (6)		0.5	1.5	ps
		DJ - K28.5 Pattern, 1.5 Gbps (7)		14	30	ps
		TJ - PRBS 2^{23}-1 Pattern, 1.5 Gbps (8)		14	31	ps
t_{ON}	LVDS Output Enable Time	Time from $\overline{PWDN}$ to OUT± change from TRI-STATE to active. Figure 9, Figure 10			20	µs
t_{OFF}	LVDS Output Disable Time	Time from $\overline{PWDN}$ to OUT± change from active to TRI-STATE. Figure 9, Figure 10			12	ns

(5) Jitter is not production tested, but ensured through characterization on a sample basis.
(6) Random Jitter, or RJ, is measured RMS with a histogram including 1500 histogram window hits. Stimulus and fixture Jitter has been subtracted. The input voltage = V_{ID} = 500 mV, input common mode voltage = V_{ICM} = 1.2V, 50% duty cycle at 750 MHz, t_r = t_f = 50 ps (20% to 80%).
(7) Deterministic Jitter, or DJ, is a peak to peak value. Stimulus and fixture jitter has been subtracted. The input voltage = V_{ID} = 500 mV, input common mode voltage = V_{ICM} = 1.2V, K28.5 pattern at 1.5 Gbps, t_r = t_f = 50 ps (20% to 80%). The K28.5 pattern is repeating bit streams of (0011111010 1100000101).
(8) Total Jitter, or TJ, is measured peak to peak with a histogram including 3500 window hits. Stimulus and fixture Jitter has been subtracted. The input voltage = V_{ID} = 500 mV, input common mode voltage = V_{ICM} = 1.2V, 2^{23}-1 PRBS pattern at 1.5 Gbps, t_r = t_f = 50 ps (20% to 80%).

DC Test Circuits

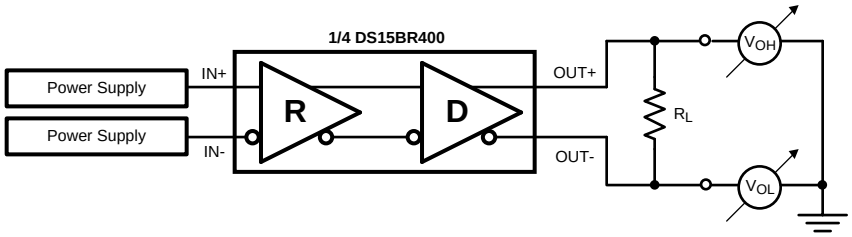


Figure 5. Differential Driver DC Test Circuit

AC Test Circuits and Timing Diagrams

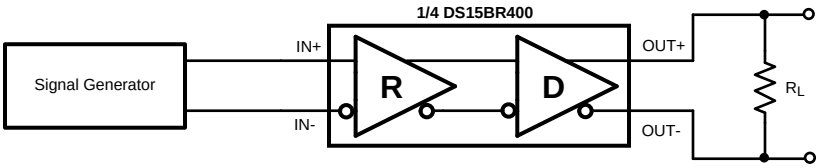


Figure 6. Differential Driver AC Test Circuit

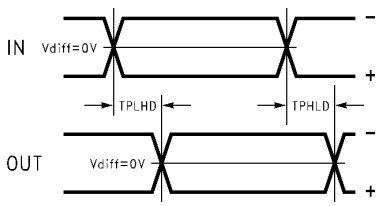


Figure 7. Propagation Delay Timing Diagram

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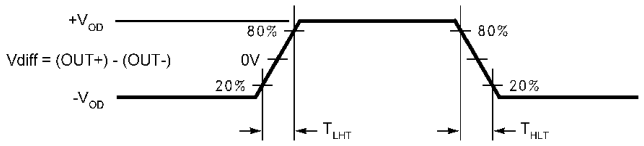


Figure 8. LVDS Output Transition Times

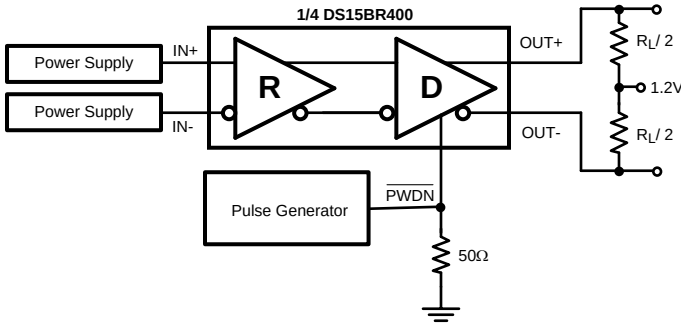


Figure 9. Enable/Disable Time Test Circuit

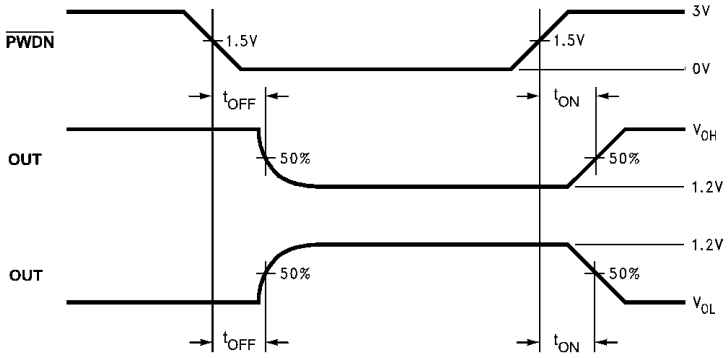


Figure 10. Enable/Disable Time Diagram

APPLICATION INFORMATION

INTERNAL TERMINATIONS

The DS15BR400 has integrated termination resistors on both the input and outputs. The inputs have a 100Ω resistor across the differential pair, placing the receiver termination as close as possible to the input stage of the device. The LVDS outputs also contain an integrated 100Ω ohm termination resistor, this resistor is used to minimize the output return loss and does not take the place of the 100 ohm termination at the inputs to the receiving device. The integrated terminations improve signal integrity and decrease the external component count resulting in space savings. The DS15BR401 has 100Ω output terminations only.

OUTPUT CHARACTERISTICS

The output characteristics of the DS15BRB400/DS15BR401 have been optimized for point-to-point backplane and cable applications, and are not intended for multipoint or multidrop signaling.

POWERDOWN MODE

The $\overline{\text{PWDN}}$ input activates a hardware powerdown mode. When the powerdown mode is active ($\overline{\text{PWDN}}$=L), all input and output buffers and internal bias circuitry are powered off. When exiting powerdown mode, there is a delay associated with turning on bandgap references and input/output buffer circuits as indicated in the LVDS Output Switching Characteristics.

Upon asserting the power down function ($\overline{\text{PWDN}}$ = Low), and if the Pre-emphasis feature is enable, it is possible for the driver output to source current for a short amount of time lifting the output common mode to V_{DD}. To prevent this occurrence, a load discharge pull down path can be used on either output (1 kΩ to ground recommended). Alternately, a commonly deployed external failsafe network will also provide this path (see INPUT FAILSAFE BIASING). The occurrence of this is application dependant, and parameters that will effect if this is of concern include: AC coupling, use of the powerdown feature, presence of the discharge path, presence of the failsafe biasing, the usage of the pre-emphasis feature, and input characteristics of the downstream LVDS Receiver.

PRE-EMPHASIS

Pre-emphasis dramatically reduces ISI jitter from long or lossy transmission media. One pin is used to select the pre-emphasis level for all outputs, off or on. The pre-emphasis boost is approximately 6 dB at 750 MHz.

Table 1. Pre-emphasis Control Selection Table

PEM	Pre-Emphasis
0	Off
1	On

INPUT FAILSAFE BIASING

Failsafe biasing of the LVDS link should be considered if the downstream Receiver is ON and enabled when the source is in TRI-STATE, powered off, or removed. This will set a valid known input state to the active receiver. This is accomplished by using a pull up resistor to V_{DD} on the 'plus' line, and a pull down resistor to GND on the 'minus' line. Resistor values are in the 750 Ohm to several kΩ range. The exact value depends upon the desired common mode bias point, termination resistor(s) and desired input differential voltage setting. Please refer to application note AN-1194 "Failsafe Biasing of LVDS interfaces" (SNLA051) for more information and a general discussion.

DECOUPLING

Each power or ground lead of the DS15BR400 should be connected to the PCB through a low inductance path. For best results, one or more vias are used to connect a power or ground pin to the nearby plane. Ideally, via placement is immediately adjacent to the pin to avoid adding trace inductance. Placing power plane closer to the top of the board reduces effective via length and its associated inductance.

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Bypass capacitors should be placed close to VDD pins. Small physical size capacitors, such as 0402, X7R, surface mount capacitors should be used to minimize body inductance of capacitors. Each bypass capacitor is connected to the power and ground plane through vias tangent to the pads of the capacitor. An X7R surface mount capacitor of size 0402 has about 0.5 nH of body inductance. At frequencies above 30 MHz or so, X7R capacitors behave as low impedance inductors. To extend the operating frequency range to a few hundred MHz, an array of different capacitor values like 100 pF, 1 nF, 0.03 µF, and 0.1 µF are commonly used in parallel. The most effective bypass capacitor can be built using sandwiched layers of power and ground at a separation of 2–3 mils. With a 2 mil FR4 dielectric, there is approximately 500 pF per square inch of PCB.

The center dap of the WQFN package housing the DS15BR400 should be connected to a ground plane through an array of vias. The via array reduces the effective inductance to ground and enhances the thermal performance of the WQFN package.

INPUT INTERFACING

The DS15BR400 and DS15BR401 accept differential signals and allow simple AC or DC coupling. With a wide common mode range, the DS15BR400 and DS15BR401 can be DC-coupled with all common differential drivers (i.e. LVPECL, LVDS, CML). The following three figures illustrate typical DC-coupled interface to common differential drivers. Note that the DS15BR400 inputs are internally terminated with a 100Ω resistor while the DS15BR401 inputs are not, therefore the latter requires external input termination.

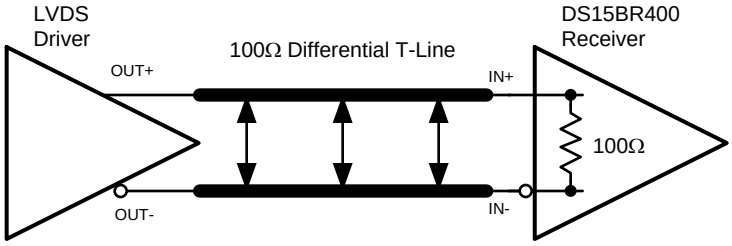


Figure 11. Typical LVDS Driver DC-Coupled Interface to DS15BR400 Input

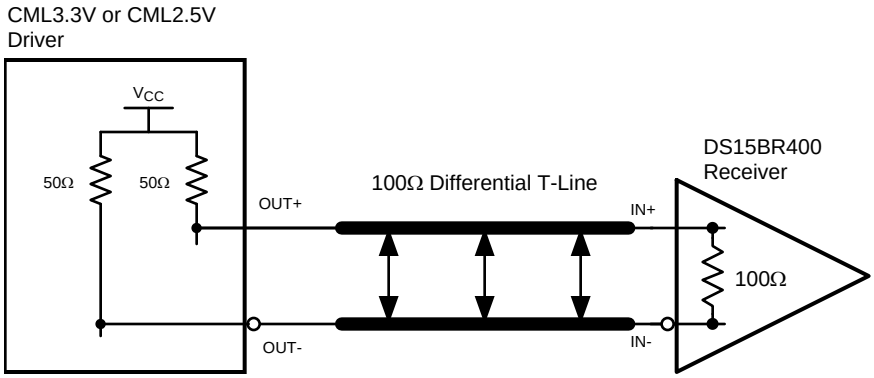


Figure 12. Typical CML Driver DC-Coupled Interface to DS15BR400 Input

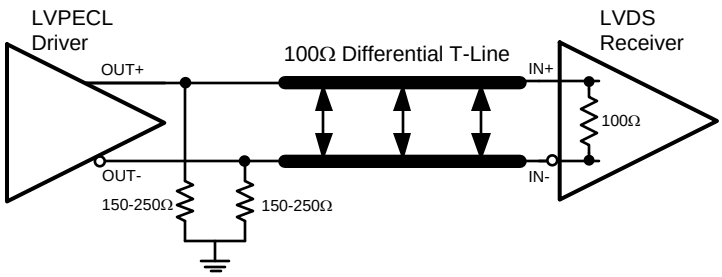


Figure 13. Typical LVPECL Driver DC-Coupled Interface to DS15BR400 Input

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OUTPUT INTERFACING

The DS15BR400 and DS15BR401 output signals that are compliant to the LVDS standard. Their outputs can be DC-coupled to most common differential receivers. Figure 14 illustrates typical DC-coupled interface to common differential receivers and assumes that the receivers have high impedance inputs. While most differential receivers have a common mode input range that can accomodate LVDS compliant signals, it is recommended to check respective receiver's data sheet prior to implementing the suggested interface implementation.

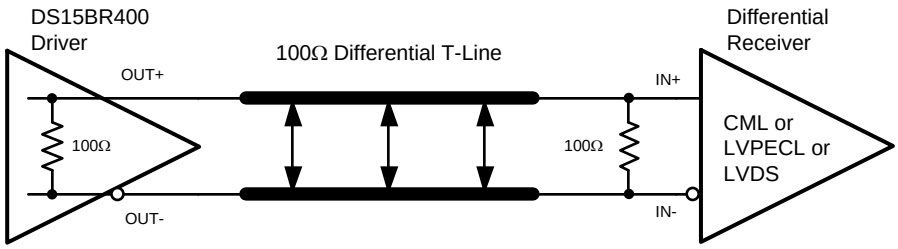


Figure 14. Typical DS15BR400 Output DC-Coupled Interface to an LVDS, CML or LVPECL Receiver

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Typical Performance Characteristics

Power Supply Current vs. Data Rate

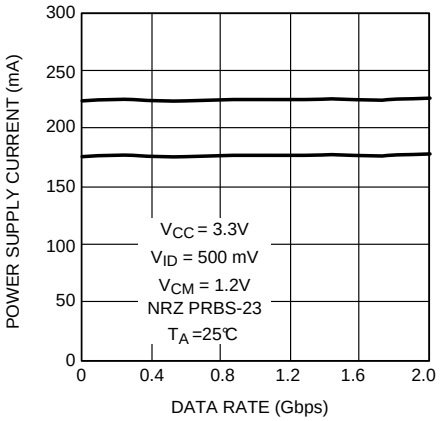


Figure 15.

Total Jitter vs. Ambient Temperature

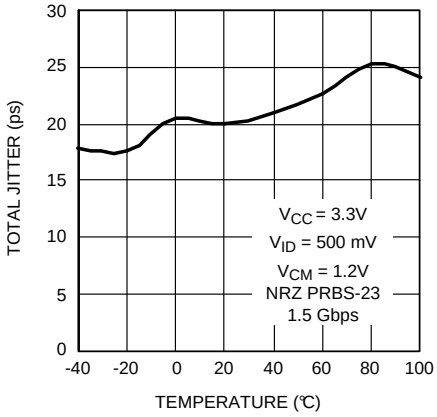


Figure 16.

Total Jitter vs. Data Rate

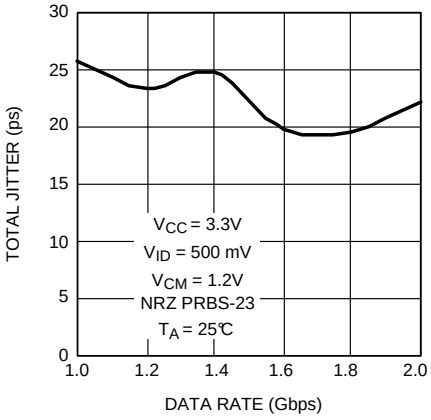


Figure 17.

Data Rate vs. Cable Length (0.25 UI Criteria)

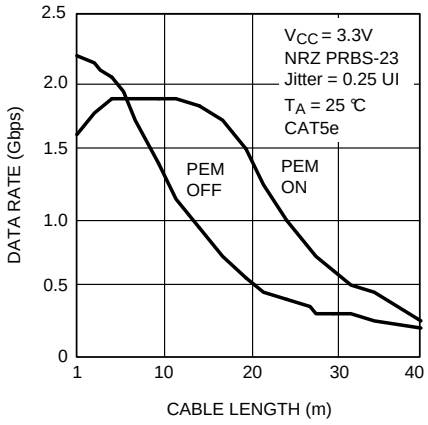


Figure 18. (1)

Data Rate vs. Cable Length (0.5 UI Criteria)

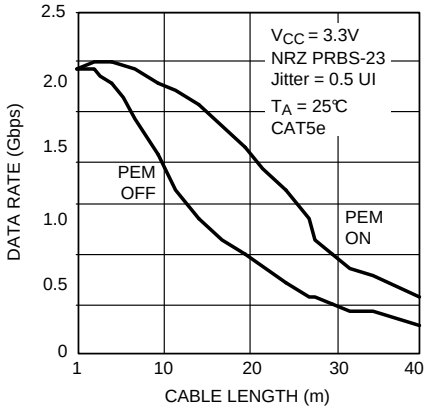


Figure 19. (1)

(1) Data presented in this graph was collected using the DS15BR400EVK, a pair of RJ-45 to SMA adapter boards and various length Belden 1700a cables. The maximum data rate was determined based on total jitter (0.25 UI criteria) measured after the cable. The total jitter was a peak to peak value measured with a histogram including 3000 window hits.

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REVISION HISTORY

Changes from Revision F (April 2013) to Revision G	Page
• Changed layout of National Data Sheet to TI format	11

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DS15BR400TSQ/NOPB	Active	Production	WQFN (RTV) | 32	1000 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	5R400SQ
DS15BR400TSQ/NOPB.A	Active	Production	WQFN (RTV) | 32	1000 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	5R400SQ
DS15BR400TVS/NOPB	Active	Production	TQFP (PFB) | 48	250 | JEDEC TRAY (10+1)	Yes	SN	Level-3-260C-168 HR	-40 to 85	DS15BR 400TVS
DS15BR400TVS/NOPB.A	Active	Production	TQFP (PFB) | 48	250 | JEDEC TRAY (10+1)	Yes	SN	Level-3-260C-168 HR	-40 to 85	DS15BR 400TVS
DS15BR400TVS/NOPB.B	Active	Production	TQFP (PFB) | 48	250 | JEDEC TRAY (10+1)	-	Call TI	Call TI	-40 to 85	
DS15BR400TVSX/NOPB	Active	Production	TQFP (PFB) | 48	1000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	DS15BR 400TVS
DS15BR400TVSX/NOPB.A	Active	Production	TQFP (PFB) | 48	1000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	DS15BR 400TVS
DS15BR400TVSX/NOPB.B	Active	Production	TQFP (PFB) | 48	1000 | LARGE T&R	-	Call TI	Call TI	-40 to 85	
DS15BR401TSQ/NOPB	Active	Production	WQFN (RTV) | 32	1000 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	5R401SQ
DS15BR401TSQ/NOPB.A	Active	Production	WQFN (RTV) | 32	1000 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	5R401SQ
DS15BR401TVS/NOPB	Active	Production	TQFP (PFB) | 48	250 | JEDEC TRAY (10+1)	Yes	SN	Level-3-260C-168 HR	-40 to 85	DS15BR 401TVS
DS15BR401TVS/NOPB.A	Active	Production	TQFP (PFB) | 48	250 | JEDEC TRAY (10+1)	Yes	SN	Level-3-260C-168 HR	-40 to 85	DS15BR 401TVS
DS15BR401TVSX/NOPB	Active	Production	TQFP (PFB) | 48	1000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	DS15BR 401TVS
DS15BR401TVSX/NOPB.A	Active	Production	TQFP (PFB) | 48	1000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	DS15BR 401TVS
DS15BR401TVSX/NOPB.B	Active	Production	TQFP (PFB) | 48	1000 | LARGE T&R	-	Call TI	Call TI	-40 to 85	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

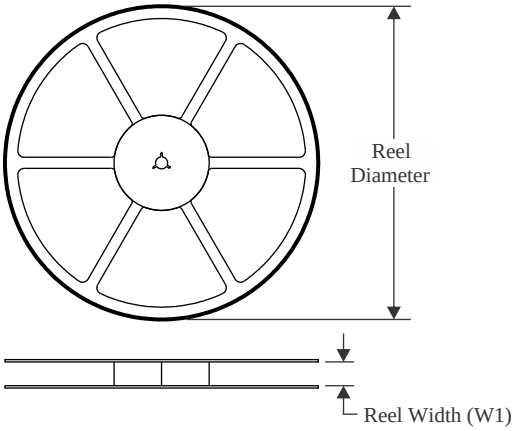
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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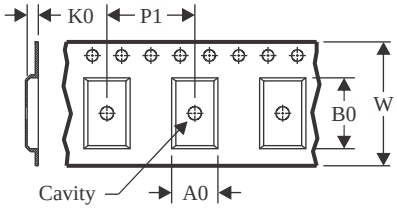
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

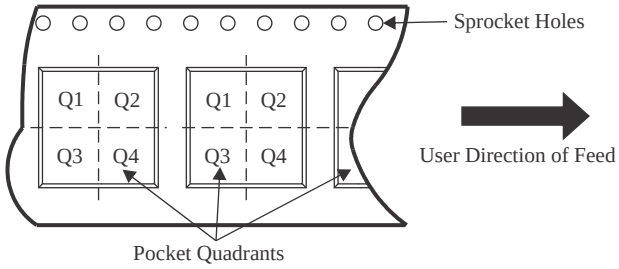


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

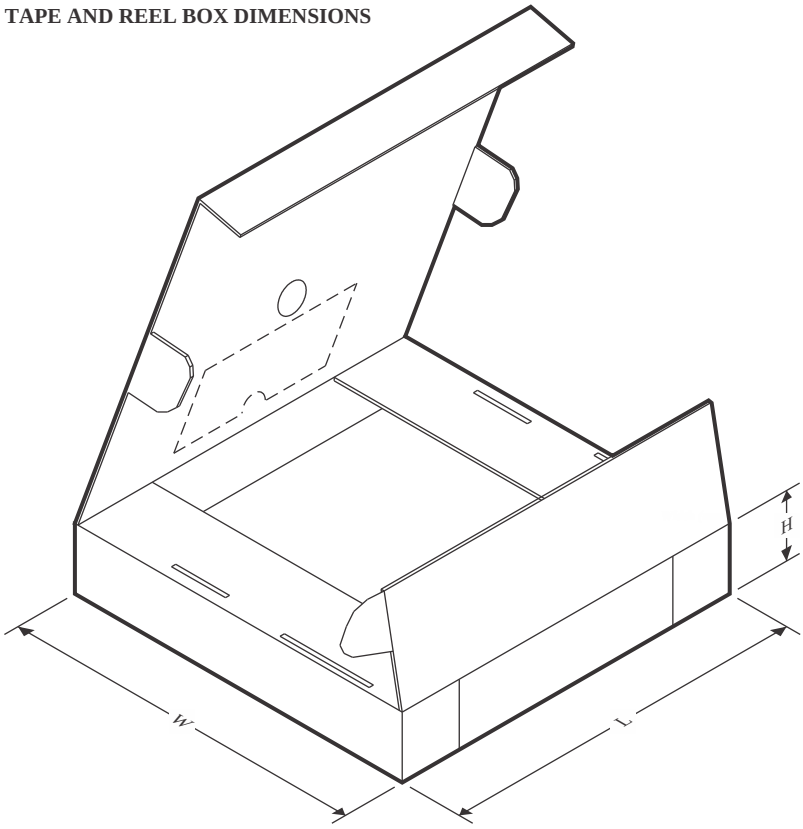
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS15BR400TSQ/NOPB	WQFN	RTV	32	1000	177.8	12.4	5.3	5.3	1.3	8.0	12.0	Q1
DS15BR400TVSX/NOPB	TQFP	PFB	48	1000	330.0	16.4	9.8	9.8	2.0	12.0	16.0	Q2
DS15BR401TSQ/NOPB	WQFN	RTV	32	1000	177.8	12.4	5.3	5.3	1.3	8.0	12.0	Q1
DS15BR401TVSX/NOPB	TQFP	PFB	48	1000	330.0	16.4	9.8	9.8	2.0	12.0	16.0	Q2

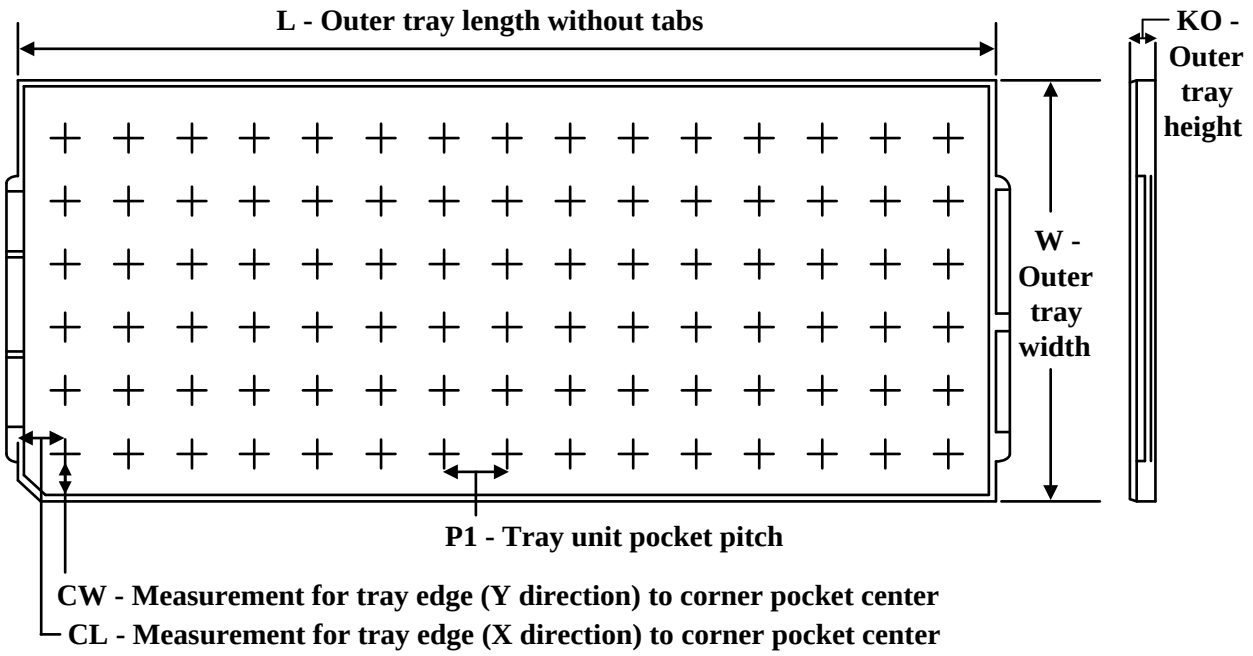
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS15BR400TSQ/NOPB	WQFN	RTV	32	1000	208.0	191.0	35.0
DS15BR400TVSX/NOPB	TQFP	PFB	48	1000	356.0	356.0	36.0
DS15BR401TSQ/NOPB	WQFN	RTV	32	1000	208.0	191.0	35.0
DS15BR401TVSX/NOPB	TQFP	PFB	48	1000	356.0	356.0	36.0

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

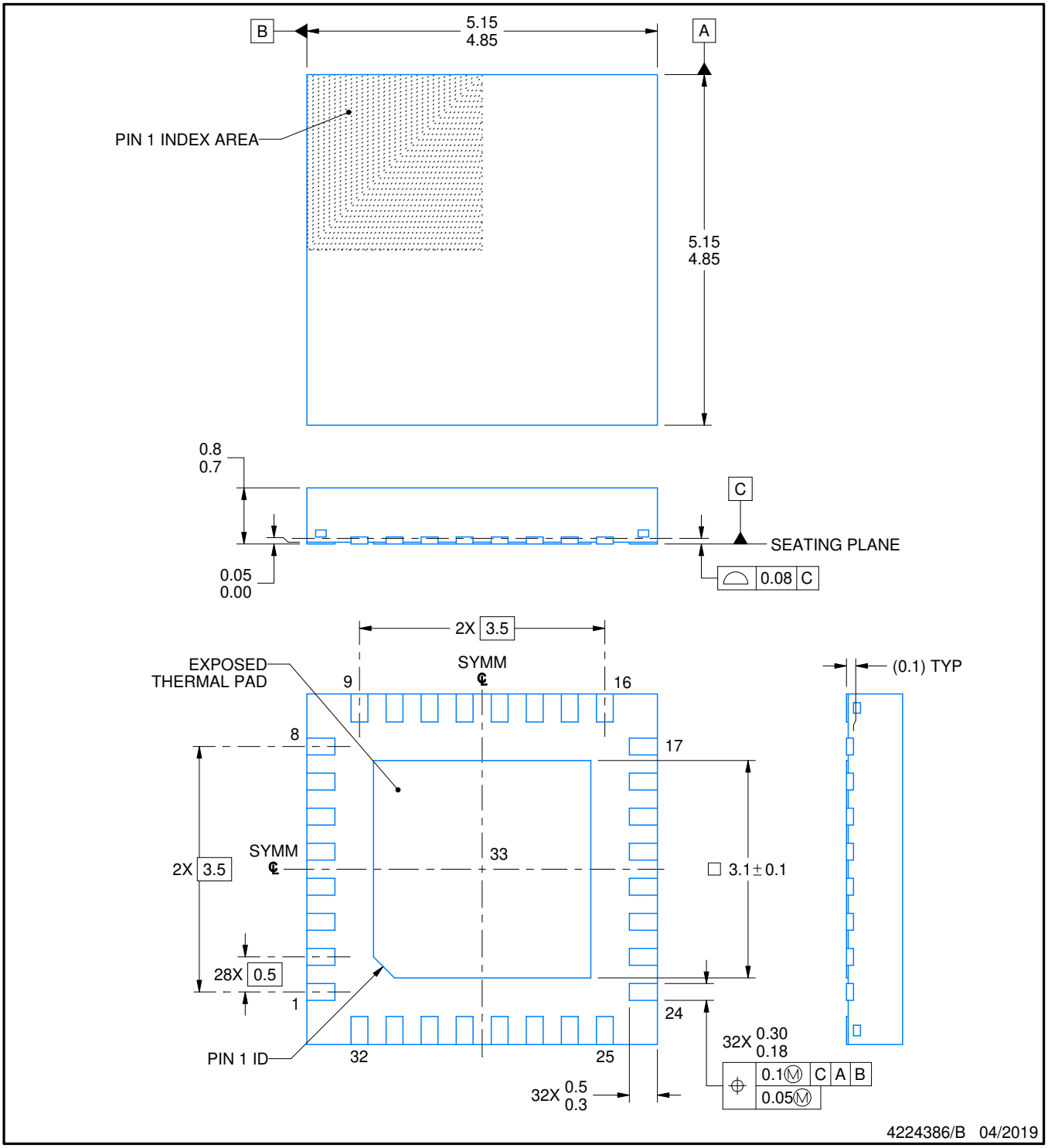
Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
DS15BR400TVS/NOPB	PFB	TQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
DS15BR400TVS/ NOPB.A	PFB	TQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
DS15BR401TVS/NOPB	PFB	TQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
DS15BR401TVS/ NOPB.A	PFB	TQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25

PACKAGE OUTLINE

RTV0032A

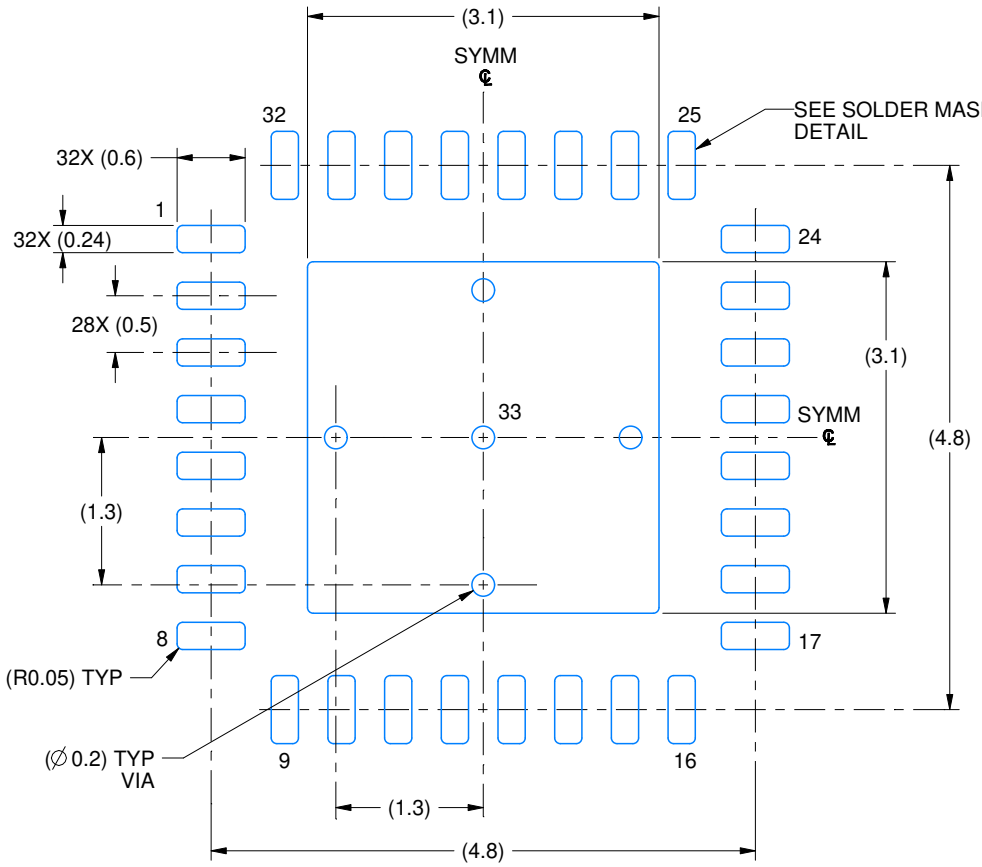
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

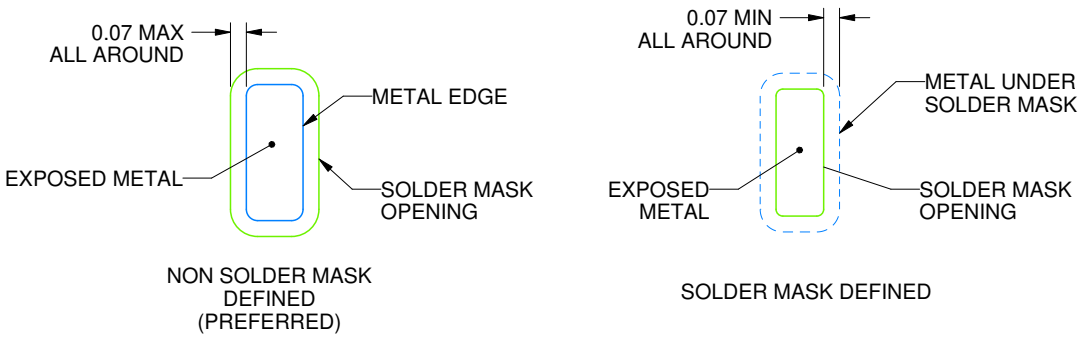


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

4224386/B 04/2019

NOTES: (continued)

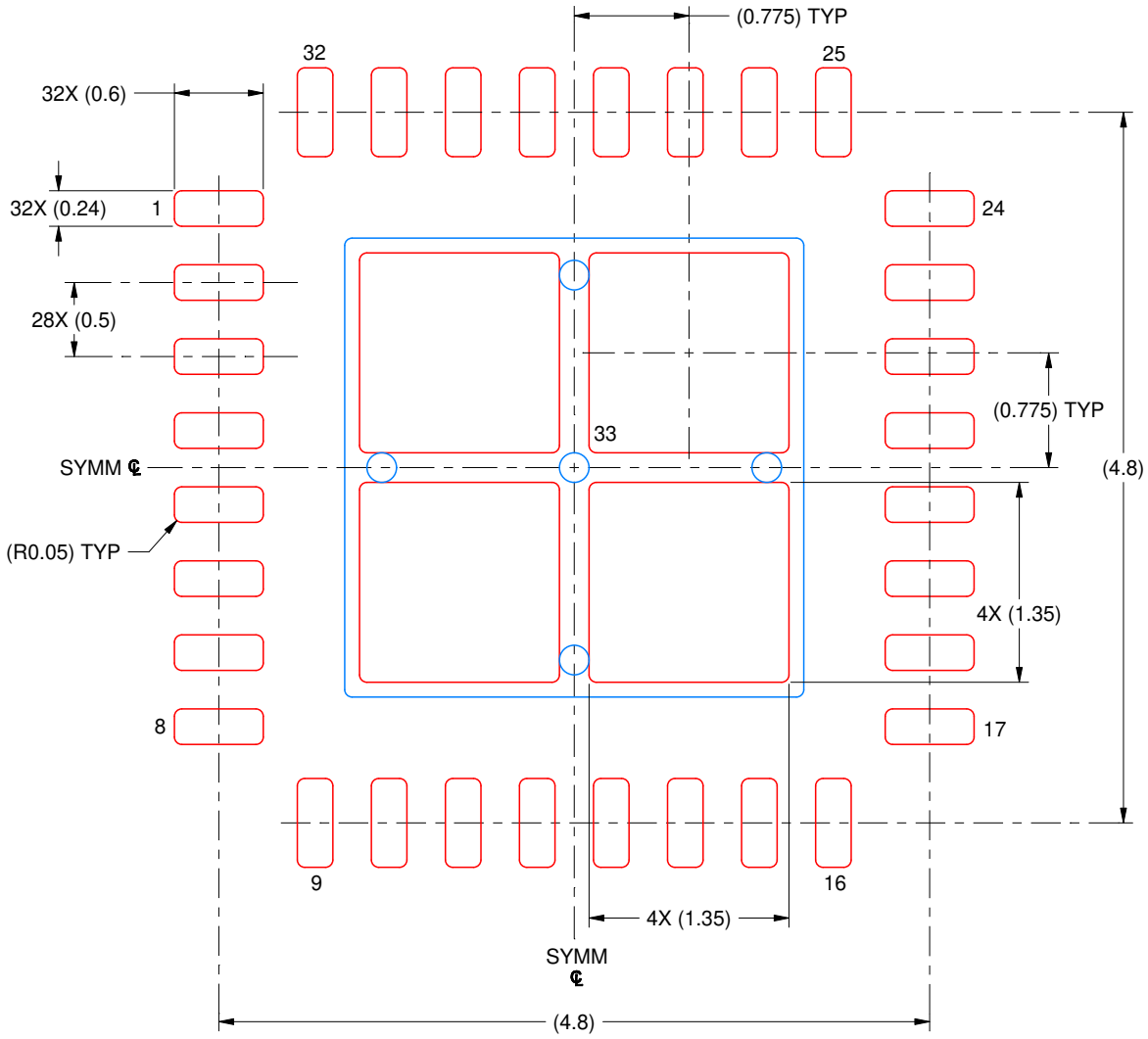
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RTV0032A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 33
76% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4224386/B 04/2019

NOTES: (continued)

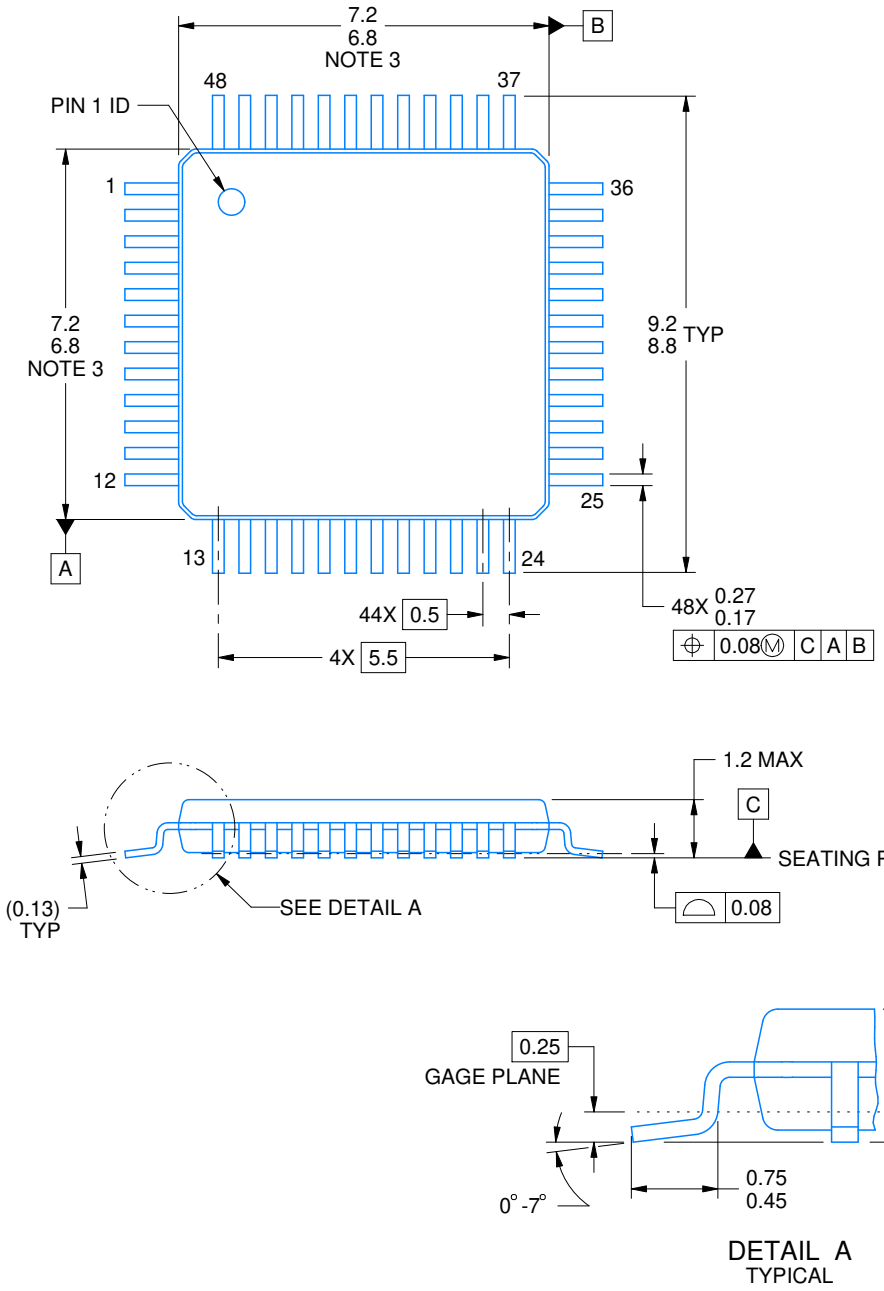
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

PFB0048A

TQFP - 1.2 mm max height

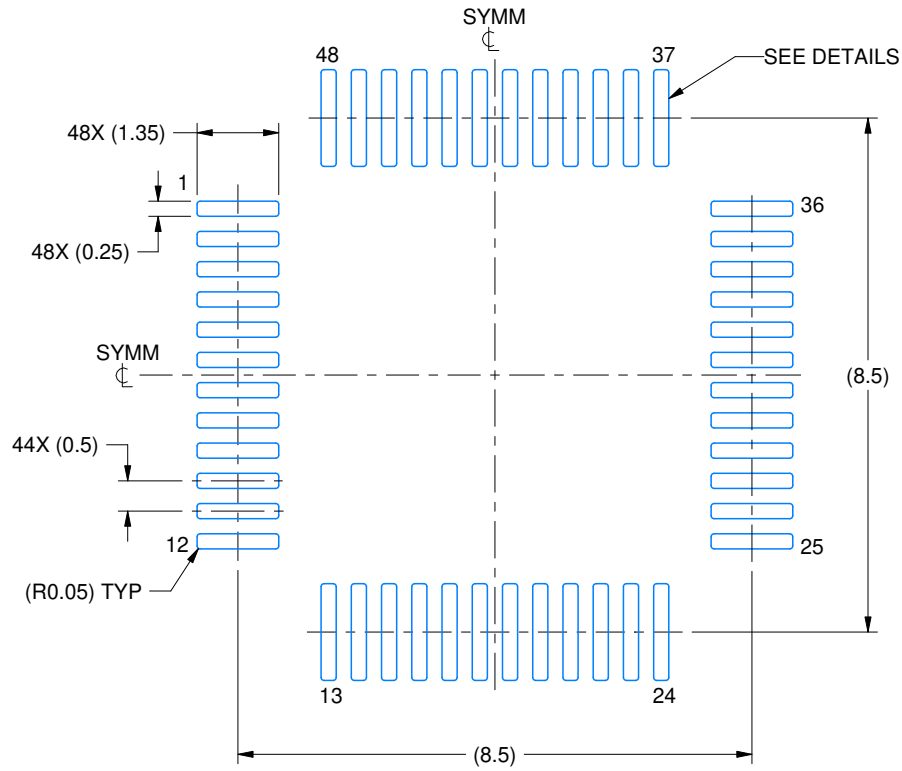
PLASTIC QUAD FLATPACK



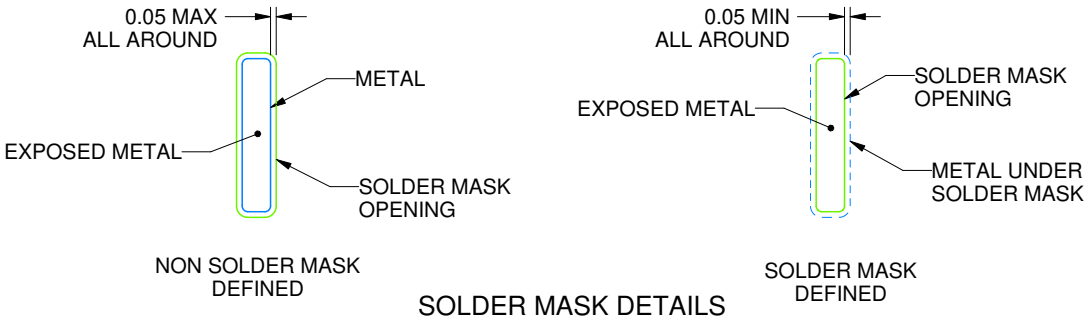
4215157/A 03/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

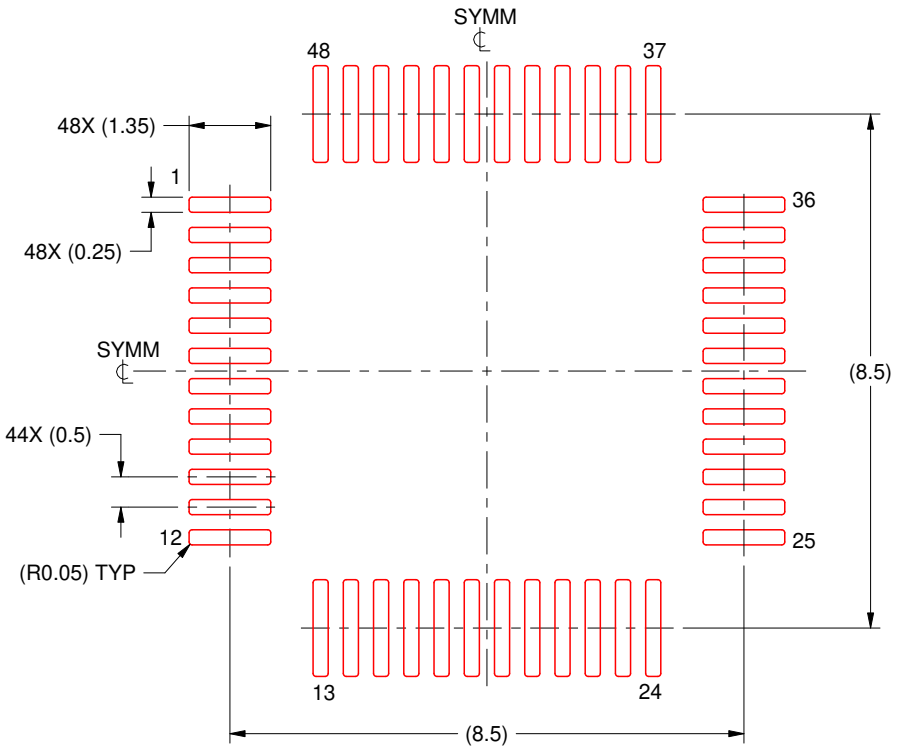


SOLDER MASK DETAILS

4215157/A 03/2024

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
SCALE:8X

4215157/A 03/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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