DS90LV004 4-Channel LVDS Buffer/Repeater with Pre-Emphasis

Check for Samples: DS90LV004

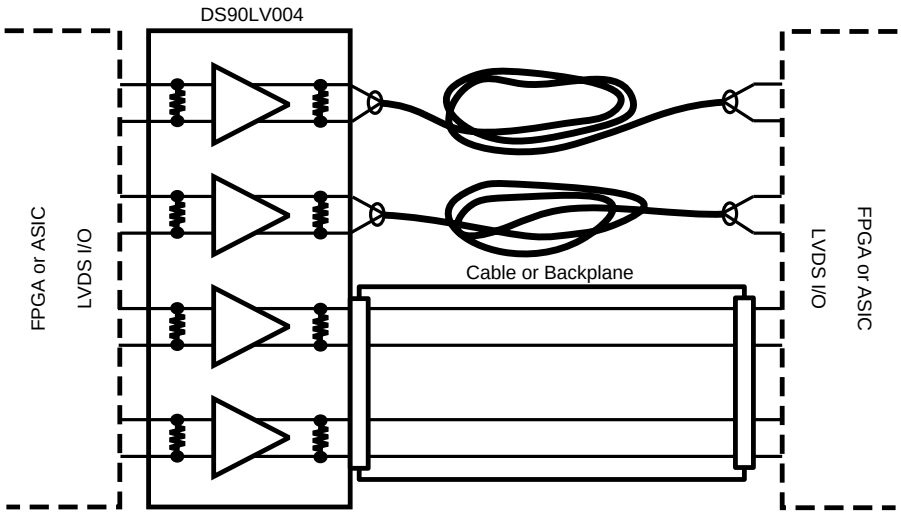
FEATURES

- **1.5 Gbps data rate per channel**
- **Configurable pre-emphasis drives lossy backplanes and cables**
- **Low output skew and jitter**
- **LVDS/CML/LVPECL compatible input, LVDS output**
- **On-chip 100Ω input and output termination**
- **12 kV ESD protection on LVDS outputs**
- **Single 3.3V supply**
- **Very low power consumption**
- **Industrial -40 to +85°C temperature range**
- **Small TQFP Package Footprint**
- **Evaluation Kit Available**
- **See SCAN90004 for JTAG-enabled version**

DESCRIPTION

The DS90LV004 is a four channel 1.5 Gbps LVDS buffer/repeater. High speed data paths and flow-through pinout minimize internal device jitter and simplify board layout, while configurable pre-emphasis overcomes ISI jitter effects from lossy backplanes and cables. The differential inputs interface to LVDS, and Bus LVDS signals such as those on TI's 10-, 16-, and 18- bit Bus LVDS SerDes, as well as CML and LVPECL. The differential inputs and outputs are internally terminated with a 100Ω resistor to improve performance and minimize board space. The repeater function is especially useful for boosting signals for longer distance transmission over lossy cables and backplanes.

Typical Application



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Block and Connection Diagrams

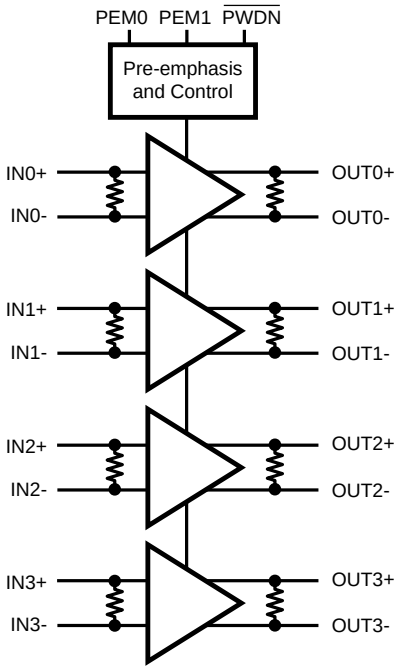


Figure 1. DS90LV004 Block Diagram

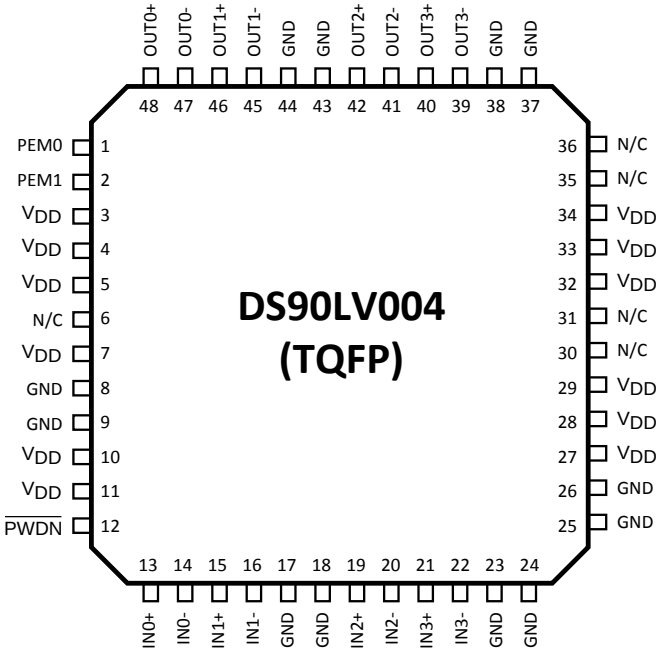


Figure 2. TQFP Pinout - Top View

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Pin Descriptions

Pin Name	TQFP Pin Number	I/O, Type	Description
DIFFERENTIAL INPUTS			
IN0+ IN0−	13 14	I, LVDS	Channel 0 inverting and non-inverting differential inputs.
IN1+ IN1−	15 16	I, LVDS	Channel 1 inverting and non-inverting differential inputs.
IN2+ IN2−	19 20	I, LVDS	Channel 2 inverting and non-inverting differential inputs.
IN3+ IN3−	21 22	I, LVDS	Channel 3 inverting and non-inverting differential inputs.
DIFFERENTIAL OUTPUTS			
OUT0+ OUT0−	48 47	O, LVDS	Channel 0 inverting and non-inverting differential outputs. (1)
OUT1+ OUT1−	46 45	O, LVDS	Channel 1 inverting and non-inverting differential outputs. (1)
OUT2+ OUT2−	42 41	O, LVDS	Channel 2 inverting and non-inverting differential outputs. (1)
OUT3+ OUT3-	40 39	O, LVDS	Channel 3 inverting and non-inverting differential outputs. (1)
DIGITAL CONTROL INTERFACE			
$\overline{\text{PWDN}}$	12	I, LVTTL	A logic low at $\overline{\text{PWDN}}$ activates the hardware power down mode.
PEM0 PEM1	1 2	I, LVTTL	Pre-emphasis Control Inputs (affects all Channels)
POWER			
V_{DD}	3, 4, 5, 7, 10, 11, 27, 28, 29, 32, 33, 34	I, Power	V_{DD} = 3.3V, ±5%
GND	8, 9, 17, 18, 23, 24, 25, 26, 37, 38, 43, 44	I, Power	Ground reference for LVDS and CMOS circuitry.
N/C	6, 30, 31, 35, 36		No Connect

(1) The LVDS outputs do not support a multidrop (BLVDS) environment. The LVDS output characteristics of the DS90LV004 device have been optimized for point-to-point backplane and cable applications.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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Absolute Maximum Ratings (1)

Supply Voltage (V_{DD})	−0.3V to +4.0V
CMOS Input Voltage	−0.3V to (V_{DD}+0.3V)
LVDS Input Voltage (2)	−0.3V to (V_{DD}+0.3V)
LVDS Output Voltage	−0.3V to (V_{DD}+0.3V)
LVDS Output Short Circuit Current	-90 mA
Junction Temperature	+150°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Solder, 4sec)	260°C
Max Pkg Power Capacity @ 25°C	1.64W
Thermal Resistance (θ_{JA})	76°C/W
Package Derating above +25°C	13.2mW/°C
ESD Last Passing Voltage (LVDS Output pins)	
HBM, 1.5kΩ, 100pF	12 kV
EIAJ, 0Ω, 200pF	250V
Charged Device Model	1000V
ESD Last Passing Voltage (All other pins)	
HBM, 1.5kΩ, 100pF	8 kV
EIAJ, 0Ω, 200pF	250V
Charged Device Model	1000V

(1) Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. TI does not recommend operation of products outside of recommended operation conditions.
(2) V_{ID} max < 2.4V

Recommended Operating Conditions

Supply Voltage (V_{CC})	3.15V to 3.45V
Input Voltage (V_I) (1)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
Industrial	−40°C to +85°C

(1) V_{ID} max < 2.4V

Electrical Characteristics

Over recommended operating supply and temperature ranges unless other specified.

Symbol	Parameter	Conditions	Min	Typ (1)	Max	Units
LVTTL DC SPECIFICATIONS ($\overline{PWDN}$, PEM0, PEM1)						
V_{IH}	High Level Input Voltage		2.0		V_{DD}	V
V_{IL}	Low Level Input Voltage		GND		0.8	V
I_{IH}	High Level Input Current	$V_{IN} = V_{DD} = V_{DDMAX}$	−10		+10	µA
I_{IL}	Low Level Input Current	$V_{IN} = V_{SS}$, $V_{DD} = V_{DDMAX}$	−10		+10	µA
C_{IN1}	Input Capacitance	Any Digital Input Pin to V_{SS}		3.5		pF
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA	−1.5	−0.8		V
LVDS INPUT DC SPECIFICATIONS (INn±)						
V_{TH}	Differential Input High Threshold (2)	V_{CM} = 0.8V to 3.4V, V_{DD} = 3.45V		0	100	mV
V_{TL}	Differential Input Low Threshold (2)	V_{CM} = 0.8V to 3.4V, V_{DD} = 3.45V	−100	0		mV
V_{ID}	Differential Input Voltage	V_{CM} = 0.8V to 3.4V, V_{DD} = 3.45V	100		2400	mV

(1) Typical parameters are measured at V_{DD} = 3.3V, T_A = 25°C. They are for reference purposes, and are not production-tested.
(2) Differential output voltage V_{OD} is defined as ABS(OUT+–OUT−). Differential input voltage V_{ID} is defined as ABS(IN+–IN−).

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Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless other specified.

Symbol	Parameter	Conditions	Min	Typ (1)	Max	Units
V_{CMR}	Common Mode Voltage Range	V_{ID} = 150 mV, V_{DD} = 3.45V	0.05		3.40	V
C_{IN2}	Input Capacitance	IN+ or IN− to V_{SS}		3.5		pF
I_{IN}	Input Current	V_{IN} = 3.45V, V_{DD} = V_{DDMAX}	−10		+10	µA
		V_{IN} = 0V, V_{DD} = V_{DDMAX}	−10		+10	µA
LVDS OUTPUT DC SPECIFICATIONS (OUTn±)						
V_{OD}	Differential Output Voltage, 0% Pre-emphasis (2)	R_L = 100Ω external resistor between OUT+ and OUT−	250	500	600	mV
ΔV_{OD}	Change in V_{OD} between Complementary States		−35		35	mV
V_{OS}	Offset Voltage (3)		1.05	1.18	1.475	V
ΔV_{OS}	Change in V_{OS} between Complementary States		−35		35	mV
I_{OS}	Output Short Circuit Current	OUT+ or OUT− Short to GND		−60	−90	mA
C_{OUT2}	Output Capacitance	OUT+ or OUT− to GND when TRI-STATE®		5.5		pF
SUPPLY CURRENT (Static)						
I_{CC}	Supply Current	All inputs and outputs enabled and active, terminated with differential load of 100Ω between OUT+ and OUT-, 0% pre-emphasis		117	140	mA
I_{CCZ}	Supply Current - Power Down Mode	$\overline{PWDN}$ = L, 0% pre-emphasis		2.7	6	mA
SWITCHING CHARACTERISTICS—LVDS OUTPUTS						
t_{LHT}	Differential Low to High Transition Time	Use an alternating 1 and 0 pattern at 200 Mbps, measure between 20% and 80% of V_{OD}. (4)		210	300	ps
t_{HLT}	Differential High to Low Transition Time			210	300	ps
t_{PLHD}	Differential Low to High Propagation Delay	Use an alternating 1 and 0 pattern at 200 Mbps, measure at 50% V_{OD} between input to output.		2.0	3.2	ns
t_{PHLD}	Differential High to Low Propagation Delay			2.0	3.2	ns
t_{SKD1}	Pulse Skew	$\lvert t_{PLHD} - t_{PHLD} \rvert$ (4)		25	80	ps
t_{SKCC}	Output Channel to Channel Skew	Difference in propagation delay (t_{PLHD} or t_{PHLD}) among all output channels. (4)		50	125	ps
t_{SKP}	Part to Part Skew	Common Edge, parts at same temp and V_{CC} (4)			1.1	ns
t_{JIT}	Jitter (0% Pre-emphasis) (5)	RJ - Alternating 1 and 0 at 750 MHz (6)		1.1	1.5	psrms
		DJ - K28.5 Pattern, 1.5 Gbps (7)		43	62	psp-p
		TJ - PRBS 2^{23}-1 Pattern, 1.5 Gbps (8)		35	85	psp-p
t_{ON}	LVDS Output Enable Time	Time from $\overline{PWDN}$ to OUT± change from TRI-STATE to active.			300	ns
t_{OFF}	LVDS Output Disable Time	Time from $\overline{PWDN}$ to OUT± change from active to TRI-STATE.			12	ns

(3) Output offset voltage V_{OS} is defined as the average of the LVDS single-ended output voltages at logic high and logic low states.
(4) Not production tested. Ensured by a statistical analysis on a sample basis at the time of characterization.
(5) Jitter is not production tested, but ensured through characterization on a sample basis.
(6) Random Jitter, or RJ, is measured RMS with a histogram including 1500 histogram window hits. The input voltage = V_{ID} = 500mV, 50% duty cycle at 750MHz, t_r = t_f = 50ps (20% to 80%).
(7) Deterministic Jitter, or DJ, is measured to a histogram mean with a sample size of 350 hits. The input voltage = V_{ID} = 500mV, K28.5 pattern at 1.5 Gbps, t_r = t_f = 50ps (20% to 80%). The K28.5 pattern is repeating bit streams of (0011111010 1100000101).
(8) Total Jitter, or TJ, is measured peak to peak with a histogram including 3500 window hits. Stimulus and fixture Jitter has been subtracted. The input voltage = V_{ID} = 500mV, 2^{23}-1 PRBS pattern at 1.5 Gbps, t_r = t_f = 50ps (20% to 80%).

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FEATURE DESCRIPTIONS

INTERNAL TERMINATIONS

The DS90LV004 has integrated termination resistors on both the input and outputs. The inputs have a 100Ω resistor across the differential pair, placing the receiver termination as close as possible to the input stage of the device. The LVDS outputs also contain an integrated 100Ω ohm termination resistor, this resistor is used to reduce the effects of Near End Crosstalk (NEXT) and does not take the place of the 100 ohm termination at the inputs to the receiving device. The integrated terminations improve signal integrity and decrease the external component count resulting in space savings.

OUTPUT CHARACTERISTICS

The output characteristics of the DS90LV004 have been optimized for point-to-point backplane and cable applications, and are not intended for multipoint or multidrop signaling.

POWERDOWN MODE

The $\overline{\text{PWDN}}$ input activates a hardware powerdown mode. When the powerdown mode is active ($\overline{\text{PWDN}}$=L), all input and output buffers and internal bias circuitry are powered off and disabled. Outputs are tri-stated in powerdown mode. When exiting powerdown mode, there is a delay associated with turning on bandgap references and input/output buffer circuits as indicated in the LVDS Output Switching Characteristics

PRE-EMPHASIS

Pre-emphasis dramatically reduces ISI jitter from long or lossy transmission media. Two pins are used to select the pre-emphasis level for all outputs: off, low, medium, or high.

Table 1. Pre-Emphasis Control Selection Table

PEM1	PEM0	Pre-Emphasis
0	0	Off
0	1	Low
1	0	Medium
1	1	High

INPUT FAILSAFE BIASING

External pull up and pull down resistors may be used to provide enough of an offset to enable an input failsafe under open-circuit conditions. This configuration ties the positive LVDS input pin to V_{DD} thru a pull up resistor and the negative LVDS input pin is tied to GND by a pull down resistor. The pull up and pull down resistors should be in the 5kΩ to 15kΩ range to minimize loading and waveform distortion to the driver. The common-mode bias point ideally should be set to approximately 1.2V (less than 1.75V) to be compatible with the internal circuitry. Please refer to application note AN-1194 “Failsafe Biasing of LVDS Interfaces” (SNLA051) for more information.

INPUT INTERFACING

The DS90LV004 accepts differential signals and allow simple AC or DC coupling. With a wide common mode range, the DS90LV004 can be DC-coupled with all common differential drivers (i.e. LVPECL, LVDS, CML). Figure 3, Figure 4, and Figure 5 illustrate typical DC-coupled interface to common differential drivers. Note that the DS90LV004 inputs are internally terminated with a 100Ω resistor.

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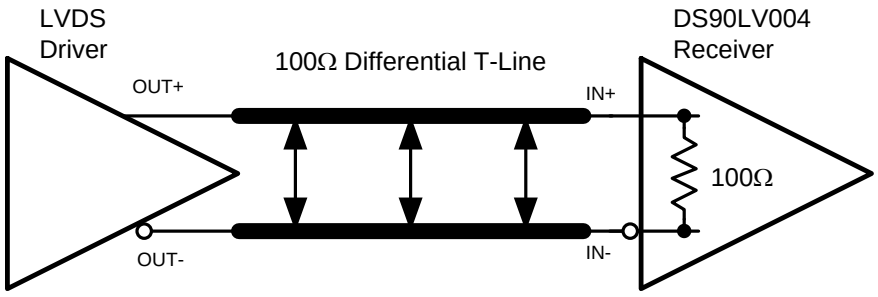


Figure 3. Typical LVDS Driver DC-Coupled Interface to DS90LV004 Input

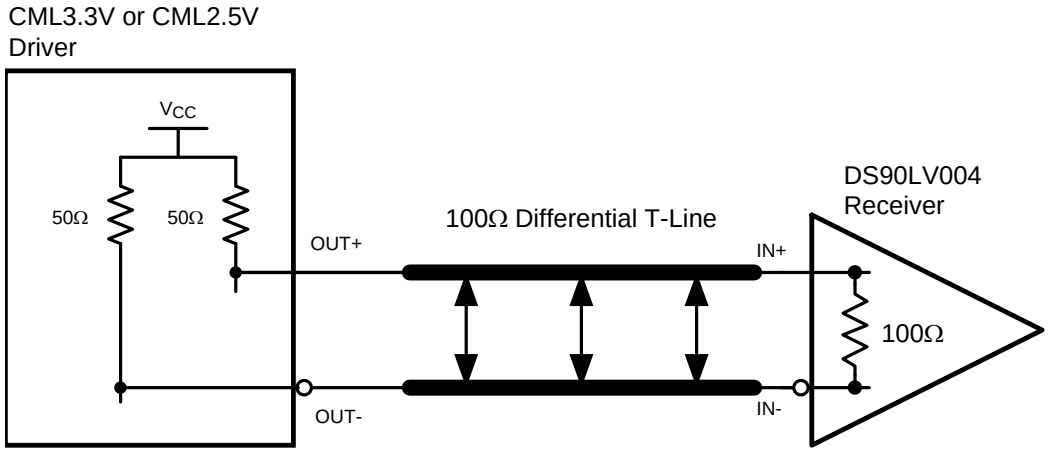


Figure 4. Typical CML Driver DC-Coupled Interface to DS90LV004 Input

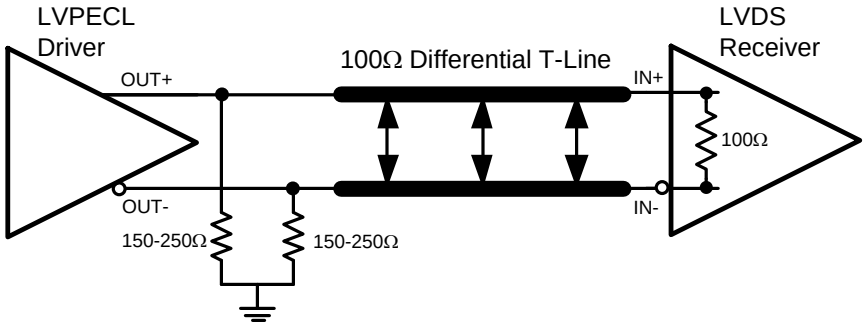


Figure 5. Typical LVPECL Driver DC-Coupled Interface to DS90LV004 Input

OUTPUT INTERFACING

The DS90LV004 outputs signals that are compliant to the LVDS standard. Their outputs can be DC-coupled to most common differential receivers. Figure 6 illustrates typical DC-coupled interface to common differential receivers and assumes that the receivers have high impedance inputs. While most differential receivers have a common mode input range that can accommodate LVDS compliant signals, it is recommended to check respective receiver's data sheet prior to implementing the suggested interface implementation.

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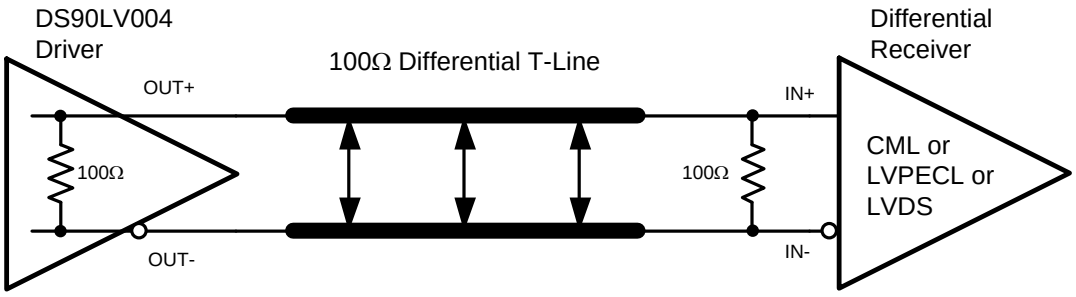
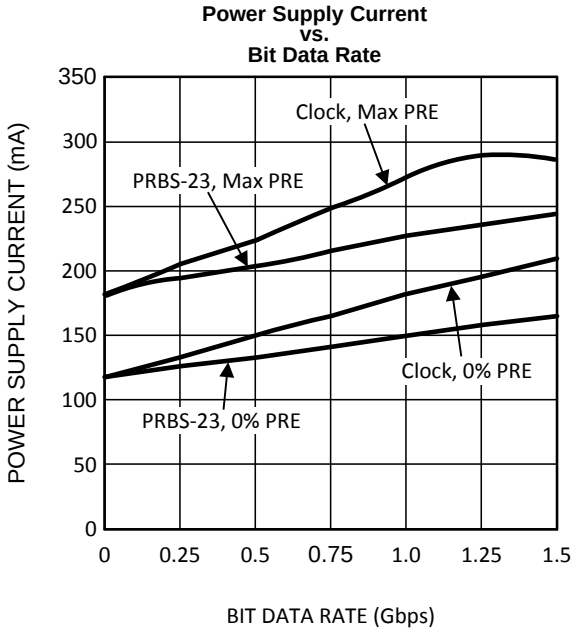


Figure 6. Typical DS90LV004 Output DC-Coupled Interface to an LVDS, CML or LVPECL Receiver

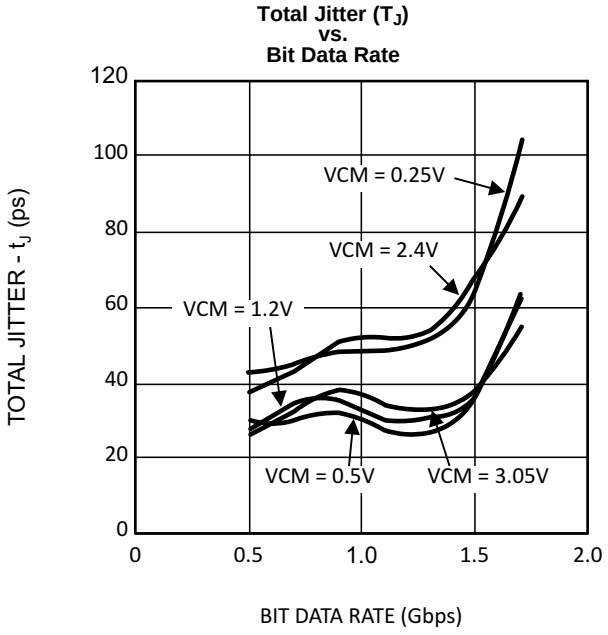
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TYPICAL PERFORMANCE CHARACTERISTICS



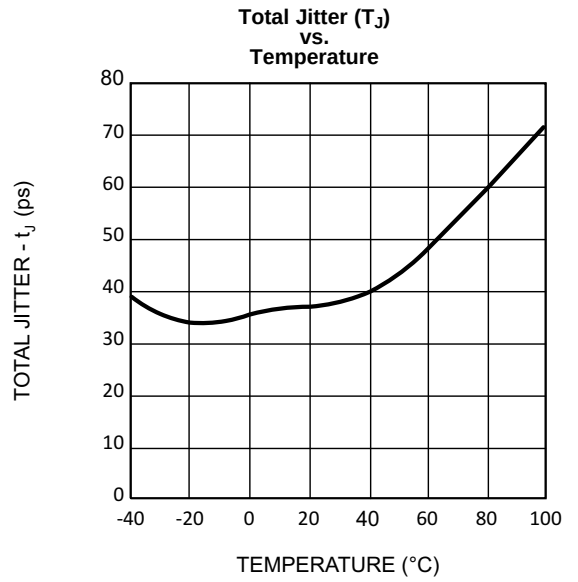
Dynamic power supply current was measured while running a clock or PRBS 2^{23}-1 pattern with all 4 channels active. V_{CC} = 3.3V, T_A = +25°C, V_{ID} = 0.5V, V_{CM} = 1.2V

Figure 7.



Total Jitter measured at 0V differential while running a PRBS 2^{23}-1 pattern with a single channel active. V_{CC} = 3.3V, T_A = +25°C, V_{ID} = 0.5V, 0% Pre-emphasis

Figure 8.



Total Jitter measured at 0V differential while running a PRBS 2^{23}-1 pattern with a single channel active. V_{CC} = 3.3V, V_{ID} = 0.5V, V_{CM} = 1.2V, 1.5 Gbps data rate, 0% Pre-emphasis

Figure 9.

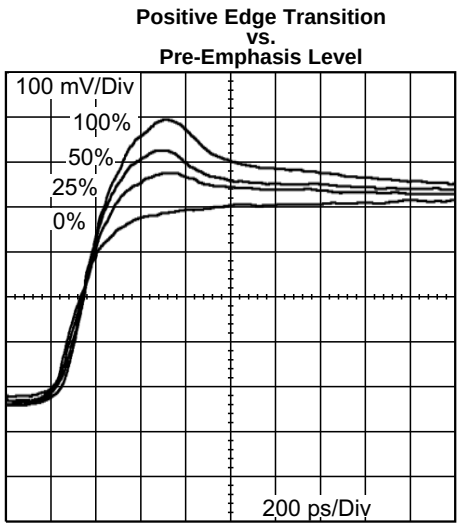


Figure 10.

REVISION HISTORY

Changes from Revision O (April 2013) to Revision P	Page
• Changed layout of National Data Sheet to TI format	9

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DS90LV004TVS/NOPB	Active	Production	TQFP (PFB) | 48	250 | JEDEC TRAY (10+1)	Yes	SN	Level-3-260C-168 HR	-40 to 85	DS90LV 004TVS
DS90LV004TVS/NOPB.A	Active	Production	TQFP (PFB) | 48	250 | JEDEC TRAY (10+1)	Yes	SN	Level-3-260C-168 HR	-40 to 85	DS90LV 004TVS
DS90LV004TVS/NOPB.B	Active	Production	TQFP (PFB) | 48	250 | JEDEC TRAY (10+1)	-	Call TI	Call TI	-40 to 85	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

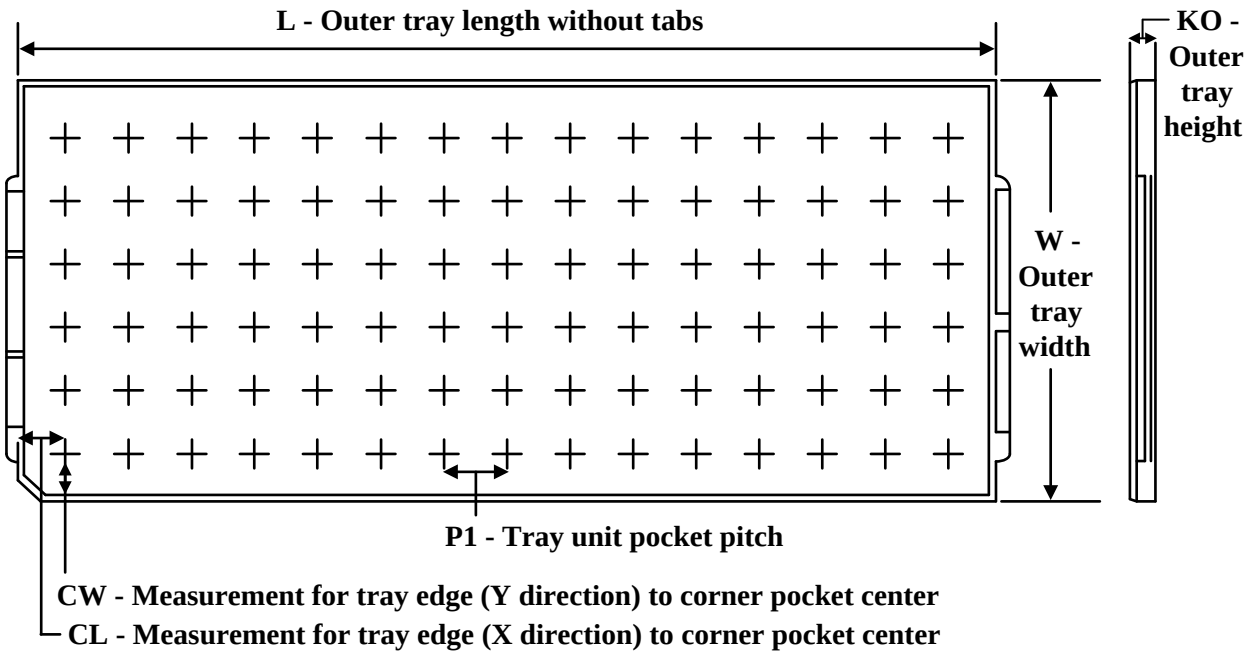
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

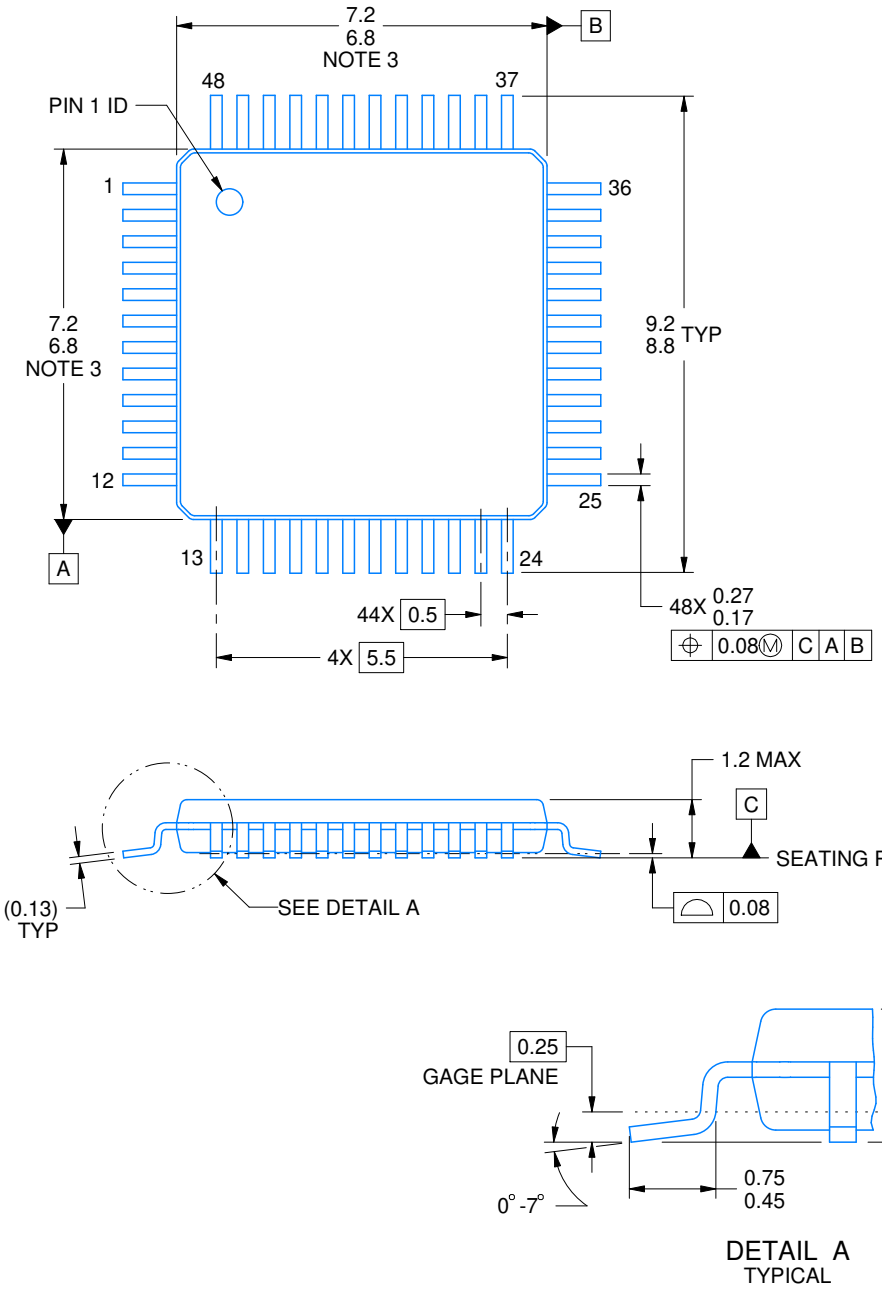
Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
DS90LV004TVS/NOPB	PFB	TQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
DS90LV004TVS/ NOPB.A	PFB	TQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25

PACKAGE OUTLINE

PFB0048A

TQFP - 1.2 mm max height

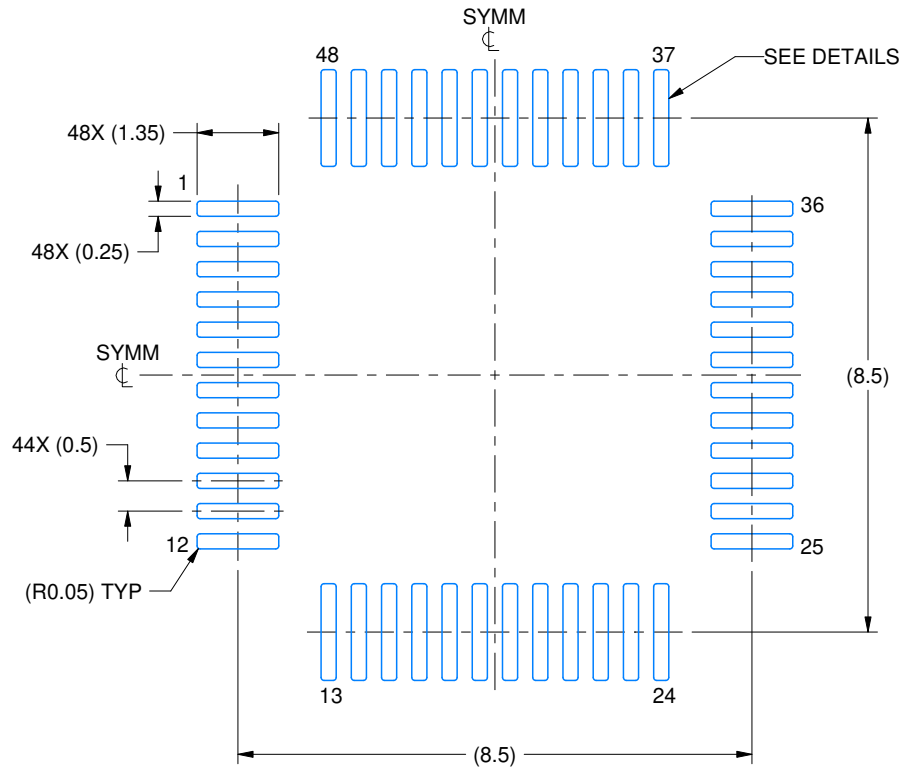
PLASTIC QUAD FLATPACK



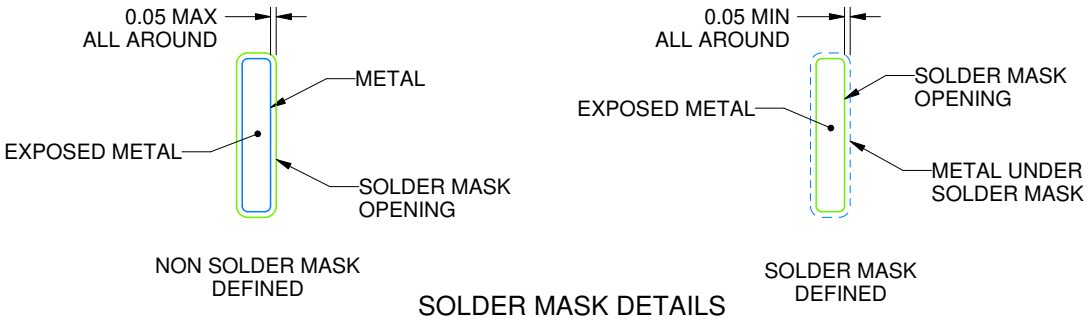
4215157/A 03/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

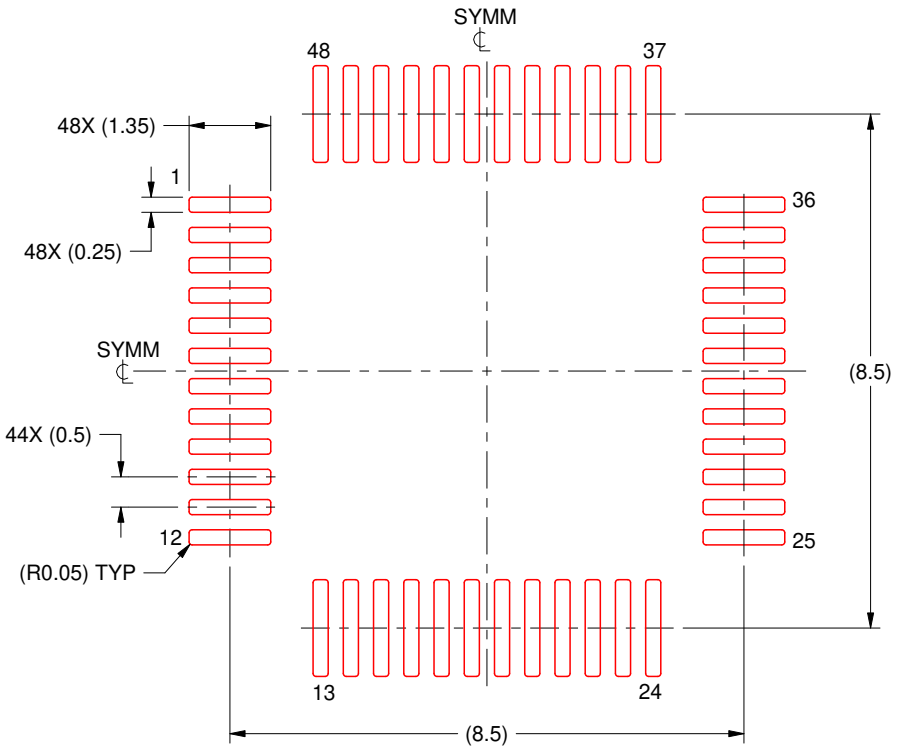


SOLDER MASK DETAILS

4215157/A 03/2024

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
SCALE:8X

4215157/A 03/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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