EFM32 Zero Gecko Family
EFM32ZG Data Sheet

The EFM32 Zero Gecko MCUs are the world's most energy-friendly microcontrollers.

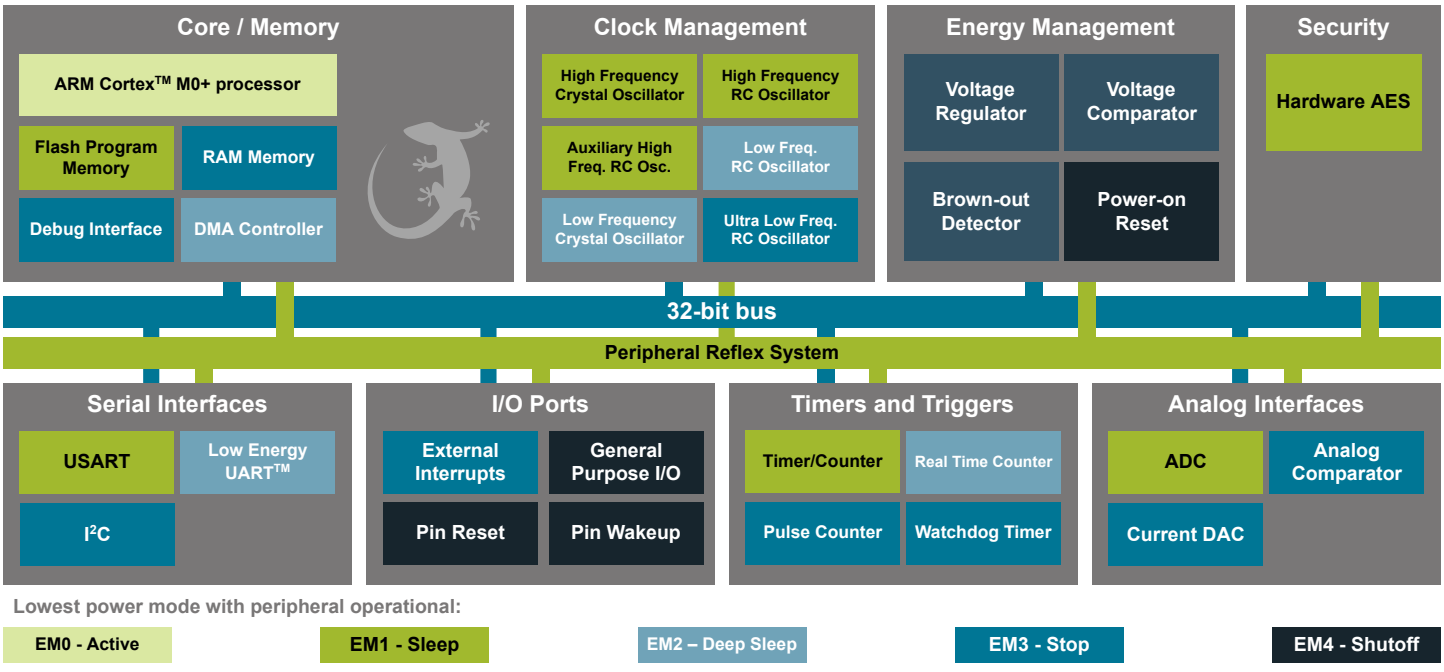
The EFM32ZG offers unmatched performance and ultra low power consumption in both active and sleep modes. EFM32ZG devices consume as little as 0.5 µA in Stop mode and 114 µA/MHz in Run mode. It also features autonomous peripherals, high overall chip and analog integration, and the performance of the industry standard 32-bit ARM Cortex-M0+ processor, making it perfect for battery-powered systems and systems with high-performance, low-energy requirements.

EFM32ZG applications include the following:

- Energy, gas, water and smart metering
- Health and fitness applications
- Smart accessories
- Alarm and security systems
- Industrial and home automation

KEY FEATURES

- ARM Cortex-M0+ at 24 MHz
- Ultra low power operation
  - 0.5 µA current in Stop (EM3), with brown-out detection and RAM retention
  - 48 µA/MHz in EM1
  - 114 µA/MHz in Run mode (EM0)
- Fast wake-up time of 2 µs
- Hardware cryptography (AES)
- Up to 32 kB of Flash and 4 kB of RAM



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1. Feature List

- ARM Cortex-M0+ CPU platform
  - High Performance 32-bit processor @ up to 24 MHz
  - Wake-up Interrupt Controller
  - SysTick System Timer
- Flexible Energy Management System
  - 20 nA @ 3 V Shutoff Mode
  - 0.5 µA @ 3 V Stop Mode, including Power-on Reset, Brown-out Detector, RAM and CPU retention
  - 0.9 µA @ 3 V Deep Sleep Mode, including RTC with 32.768 kHz oscillator, Power-on Reset, Brown-out Detector, RAM and CPU retention
  - 48 µA/MHz @ 3 V Sleep Mode
  - 114 µA/MHz @ 3 V Run Mode, with code executed from flash
- 32/16/8/4 kB Flash
- 4/2 kB RAM
- Up to 37 General Purpose I/O pins
  - Configurable push-pull, open-drain, pull-up/down, input filter, drive strength
  - Configurable peripheral I/O locations
  - Up to 16 asynchronous external interrupts
  - Output state retention and wake-up from Shutoff Mode
- 4 Channel DMA Controller
- 4 Channel Peripheral Reflex System (PRS) for autonomous inter-peripheral signaling
- Hardware AES with 128-bit keys in 54 cycles
- Timers/Counters
  - 2× 16-bit Timer/Counter
    - 2×3 Compare/Capture/PWM channels
  - 1× 24-bit Real-Time Counter
  - 1× 16-bit Pulse Counter
  - Watchdog Timer with dedicated RC oscillator @ 50 nA
- Communication interfaces
  - Universal Synchronous/Asynchronous Receiver/Transmitter
    - UART/SPI/SmartCard (ISO 7816)/IrDA/I2S
    - Triple buffered full/half-duplex operation
  - Low Energy UART
    - Autonomous operation with DMA in Deep Sleep Mode
  - I^2C Interface with SMBus support
    - Address recognition in Stop Mode
- Ultra low power precision analog peripherals
  - 12-bit 1 Msamples/s Analog-to-Digital Converter
    - 4 single-ended channels/2 differential channels
    - On-chip temperature sensor
  - Current Digital-to-Analog Converter
    - Selectable current range between 0.05 and 64 µA
  - 1× Analog Comparator
    - Capacitive sensing with up to 5 inputs
  - Supply Voltage Comparator
- Ultra efficient Power-on Reset and Brown-Out Detector
- 2-pin Serial Wire Debug interface
- Pre-Programmed UART Bootloader
- Temperature range -40 to 85 ºC
- Single power supply 1.98 to 3.8 V

- Packages:
  - QFN24 (5×5 mm)
  - QFN32 (6×6 mm)
  - TQFP48 (7×7 mm)

2. Ordering Information

The following table shows the available EFM32ZG devices.

Table 2.1. Ordering Information

Ordering Code	Flash (kB)	RAM (kB)	Max Speed (MHz)	Supply Voltage (V)	Temperature (°C)	Package
EFM32ZG108F4-B-QFN24	4	2	24	1.98 - 3.8	-40 - 85	QFN24
EFM32ZG108F8-B-QFN24	8	2	24	1.98 - 3.8	-40 - 85	QFN24
EFM32ZG108F16-B-QFN24	16	4	24	1.98 - 3.8	-40 - 85	QFN24
EFM32ZG108F32-B-QFN24	32	4	24	1.98 - 3.8	-40 - 85	QFN24
EFM32ZG110F4-B-QFN24	4	2	24	1.98 - 3.8	-40 - 85	QFN24
EFM32ZG110F8-B-QFN24	8	2	24	1.98 - 3.8	-40 - 85	QFN24
EFM32ZG110F16-B-QFN24	16	4	24	1.98 - 3.8	-40 - 85	QFN24
EFM32ZG110F32-B-QFN24	32	4	24	1.98 - 3.8	-40 - 85	QFN24
EFM32ZG210F4-B-QFN32	4	2	24	1.98 - 3.8	-40 - 85	QFN32
EFM32ZG210F8-B-QFN32	8	2	24	1.98 - 3.8	-40 - 85	QFN32
EFM32ZG210F16-B-QFN32	16	4	24	1.98 - 3.8	-40 - 85	QFN32
EFM32ZG210F32-B-QFN32	32	4	24	1.98 - 3.8	-40 - 85	QFN32
EFM32ZG222F4-B-QFP48	4	2	24	1.98 - 3.8	-40 - 85	TQFP48
EFM32ZG222F8-B-QFP48	8	2	24	1.98 - 3.8	-40 - 85	TQFP48
EFM32ZG222F16-B-QFP48	16	4	24	1.98 - 3.8	-40 - 85	TQFP48
EFM32ZG222F32-B-QFP48	32	4	24	1.98 - 3.8	-40 - 85	TQFP48

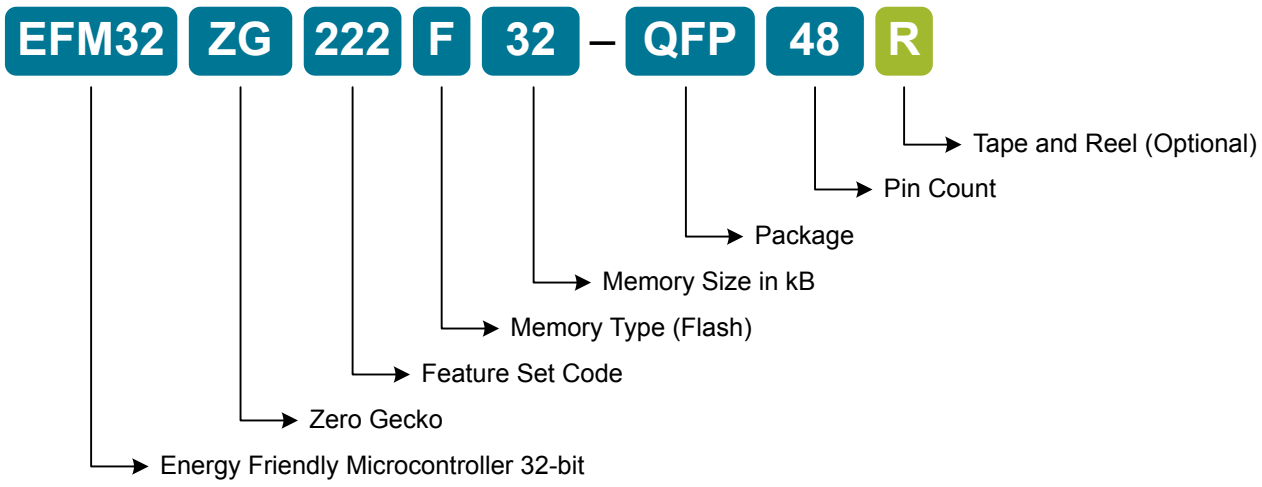


Figure 2.1. Ordering Code Decoder

Adding the suffix 'R' to the part number (e.g. EFM32ZG222F32-B-QFP48R) denotes tape and reel packaging.

Visit http://www.silabs.com for information on global distributors and representatives.

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3. System Summary

3.1 System Introduction

The EFM32 MCUs are the world's most energy friendly microcontrollers. With a unique combination of the powerful 32-bit ARM Cortex-M0+, innovative low energy techniques, short wake-up time from energy saving modes, and a wide selection of peripherals, the EFM32ZG microcontroller is well suited for any battery operated application as well as other systems requiring high performance and low-energy consumption. This section gives a short introduction to each of the modules in general terms and also shows a summary of the configuration for the EFM32ZG devices. For a complete feature set and in-depth information on the modules, refer to the EFM32ZG Reference Manual.

A block diagram of the EFM32ZG is shown in the following figure.

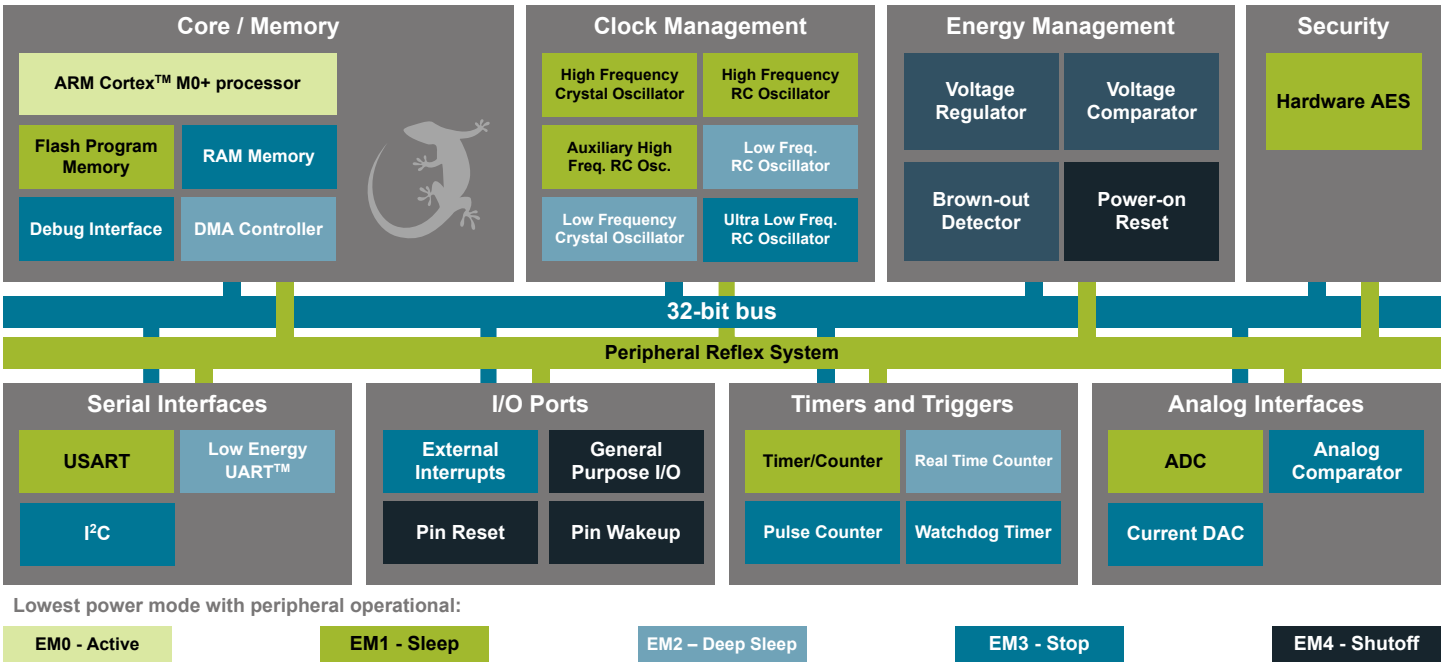


Figure 3.1. Block Diagram

3.1.1 ARM Cortex-M0+ Core

The ARM Cortex-M0+ includes a 32-bit RISC processor which can achieve as much as 0.9 Dhrystone MIPS/MHz. A wake-up Interrupt Controller handling interrupts triggered while the CPU is asleep is included as well. The EFM32 implementation of the Cortex-M0+ is described in detail in *ARM Cortex-M0+ Devices Generic User Guide*.

3.1.2 Debug Interface (DBG)

This device includes hardware debug support through a 2-pin serial-wire debug interface.

3.1.3 Memory System Controller (MSC)

The Memory System Controller (MSC) is the program memory unit of the EFM32ZG microcontroller. The flash memory is readable and writable from both the Cortex-M0+ and DMA. The flash memory is divided into two blocks; the main block and the information block. Program code is normally written to the main block. Additionally, the information block is available for special user data and flash lock bits. There is also a read-only page in the information block containing system and device calibration data. Read and write operations are supported in the energy modes EM0 and EM1.

3.1.4 Direct Memory Access Controller (DMA)

The Direct Memory Access (DMA) controller performs memory operations independently of the CPU. This has the benefit of reducing the energy consumption and the workload of the CPU, and enables the system to stay in low energy modes when moving for instance data from the USART to RAM or from the External Bus Interface to a PWM-generating timer. The DMA controller uses the PL230 µDMA controller licensed from ARM.

3.1.5 Reset Management Unit (RMU)

The RMU is responsible for handling the reset functionality of the EFM32ZG.

3.1.6 Energy Management Unit (EMU)

The Energy Management Unit (EMU) manage all the low energy modes (EM) in EFM32ZG microcontrollers. Each energy mode manages if the CPU and the various peripherals are available. The EMU can also be used to turn off the power to unused SRAM blocks.

3.1.7 Clock Management Unit (CMU)

The Clock Management Unit (CMU) is responsible for controlling the oscillators and clocks on-board the EFM32ZG. The CMU provides the capability to turn on and off the clock on an individual basis to all peripheral modules in addition to enable/disable and configure the available oscillators. The high degree of flexibility enables software to minimize energy consumption in any specific application by not wasting power on peripherals and oscillators that are inactive.

3.1.8 Watchdog (WDOG)

The purpose of the watchdog timer is to generate a reset in case of a system failure, to increase application reliability. The failure may e.g. be caused by an external event, such as an ESD pulse, or by a software failure.

3.1.9 Peripheral Reflex System (PRS)

The Peripheral Reflex System (PRS) system is a network which lets the different peripheral module communicate directly with each other without involving the CPU. Peripheral modules which send out Reflex signals are called producers. The PRS routes these reflex signals to consumer peripherals which apply actions depending on the data received. The format for the Reflex signals is not given, but edge triggers and other functionality can be applied by the PRS.

3.1.10 Inter-Integrated Circuit Interface (I2C)

The I^2C module provides an interface between the MCU and a serial I^2C-bus. It is capable of acting as both a master and a slave, and supports multi-master buses. Both standard-mode, fast-mode and fastmode plus speeds are supported, allowing transmission rates all the way from 10 kbit/s up to 1 Mbit/s. Slave arbitration and timeouts are also provided to allow implementation of an SMBus compliant system. The interface provided to software by the I^2C module, allows both fine-grained control of the transmission process and close to automatic transfers. Automatic recognition of slave addresses is provided in all energy modes.

3.1.11 Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The Universal Synchronous Asynchronous serial Receiver and Transmitter (USART) is a very flexible serial I/O module. It supports full duplex asynchronous UART communication as well as RS-485, SPI, MicroWire and 3-wire. It can also interface with ISO7816 SmartCards, IrDA, and I2S devices.

3.1.12 Pre-Programmed UART Bootloader

The bootloader presented in application note AN0003 is pre-programmed in the device at factory. Autobaud and destructive write are supported. The autobaud feature, interface and commands are described further in the application note.

3.1.13 Low Energy Universal Asynchronous Receiver/Transmitter (LEUART)

The unique LEUART™, the Low Energy UART, is a UART that allows two-way UART communication on a strict power budget. Only a 32.768 kHz clock is needed to allow UART communication up to 9600 baud/ s. The LEUART includes all necessary hardware support to make asynchronous serial communication possible with minimum of software intervention and energy consumption.

3.1.14 Timer/Counter (TIMER)

The 16-bit general purpose Timer has 3 compare/capture channels for input capture and compare/Pulse- Width Modulation (PWM) output.

3.1.15 Real Time Counter (RTC)

The Real Time Counter (RTC) contains a 24-bit counter and is clocked either by a 32.768 kHz crystal oscillator, or a 32.768 kHz RC oscillator. In addition to energy modes EM0 and EM1, the RTC is also available in EM2. This makes it ideal for keeping track of time since the RTC is enabled in EM2 where most of the device is powered down.

3.1.16 Pulse Counter (PCNT)

The Pulse Counter (PCNT) can be used for counting pulses on a single input or to decode quadrature encoded inputs. It runs off either the internal LFACLK or the PCNTn_S0IN pin as external clock source. The module may operate in energy mode EM0 - EM3.

3.1.17 Analog Comparator (ACMP)

The Analog Comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. Inputs can either be one of the selectable internal references or from external pins. Response time and thereby also the current consumption can be configured by altering the current supply to the comparator.

3.1.18 Voltage Comparator (VCMP)

The Voltage Supply Comparator is used to monitor the supply voltage from software. An interrupt can be generated when the supply falls below or rises above a programmable threshold. Response time and thereby also the current consumption can be configured by altering the current supply to the comparator.

3.1.19 Analog to Digital Converter (ADC)

The ADC is a Successive Approximation Register (SAR) architecture, with a resolution of up to 12 bits at up to one million samples per second. The integrated input mux can select inputs from 4 external pins and 6 internal signals.

3.1.20 Current Digital to Analog Converter (IDAC)

The current digital to analog converter can source or sink a configurable constant current, which can be output on, or sinked from pin or ADC. The current is configurable with several ranges of various step sizes.

3.1.21 Advanced Encryption Standard Accelerator (AES)

The AES accelerator performs AES encryption and decryption with 128-bit. Encrypting or decrypting one 128-bit data block takes 52 HFCORECLK cycles with 128-bit keys. The AES module is an AHB slave which enables efficient access to the data and key registers. All write accesses to the AES module must be 32-bit operations, i.e. 8- or 16-bit operations are not supported.

3.1.22 General Purpose Input/Output (GPIO)

In the EFM32ZG, there are up to 37 General Purpose Input/Output (GPIO) pins, which are divided into ports with up to 16 pins each. These pins can individually be configured as either an output or input. More advanced configurations like open-drain, filtering and drive strength can also be configured individually for the pins. The GPIO pins can also be overridden by peripheral pin connections, like Timer PWM outputs or USART communication, which can be routed to several locations on the device. The GPIO supports up to 16 asynchronous external pin interrupts, which enables interrupts from any pin on the device. Also, the input value of a pin can be routed through the Peripheral Reflex System to other peripherals.

3.2 Configuration Summary

3.2.1 EFM32ZG108

The features of the EFM32ZG108 is a subset of the feature set described in the EFM32ZG Reference Manual. The following table describes device specific implementation of the features.

Table 3.1. EFM32ZG108 Configuration Summary

Module	Configuration	Pin Connections
Cortex-M0+	Full configuration	NA
DBG	Full configuration	DBG_SWCLK, DBG_SWDIO
MSC	Full configuration	NA
DMA	Full configuration	NA
RMU	Full configuration	NA
EMU	Full configuration	NA
CMU	Full configuration	CMU_OUT0, CMU_OUT1
WDOG	Full configuration	NA
PRS	Full configuration	NA
I2C0	Full configuration	I2C0_SDA, I2C0_SCL
USART1	Full configuration with I2S and IrDA	US1_TX, US1_RX, US1_CLK, US1_CS
LEUART0	Full configuration	LEU0_TX, LEU0_RX
TIMER0	Full configuration	TIM0_CC[2:0]
TIMER1	Full configuration	TIM1_CC[2:0]
RTC	Full configuration	NA
PCNT0	Full configuration, 16-bit count register	PCNT0_S[1:0]
ACMP0	Full configuration	ACMP0_CH[1:0], ACMP0_O
VCMP	Full configuration	NA
GPIO	17 pins	Available pins are shown in 5.1.3 GPIO Pinout Overview

3.2.2 EFM32ZG110

The features of the EFM32ZG110 is a subset of the feature set described in the EFM32ZG Reference Manual. The following table describes device specific implementation of the features.

Table 3.2. EFM32ZG110 Configuration Summary

Module	Configuration	Pin Connections
Cortex-M0+	Full configuration	NA
DBG	Full configuration	DBG_SWCLK, DBG_SWDIO
MSC	Full configuration	NA
DMA	Full configuration	NA
RMU	Full configuration	NA
EMU	Full configuration	NA
CMU	Full configuration	CMU_OUT0, CMU_OUT1
WDOG	Full configuration	NA
PRS	Full configuration	NA
I2C0	Full configuration	I2C0_SDA, I2C0_SCL
USART1	Full configuration with I2S and IrDA	US1_TX, US1_RX, US1_CLK, US1_CS
LEUART0	Full configuration	LEU0_TX, LEU0_RX
TIMER0	Full configuration	TIM0_CC[2:0]
TIMER1	Full configuration	TIM1_CC[2:0]
RTC	Full configuration	NA
PCNT0	Full configuration, 16-bit count register	PCNT0_S[1:0]
ACMP0	Full configuration	ACMP0_CH[1:0], ACMP0_O
VCMP	Full configuration	NA
ADC0	Full configuration	ADC0_CH[1:0]
IDAC0	Full configuration	IDAC0_OUT
AES	Full configuration	NA
GPIO	17 pins	Available pins are shown in 5.2.3 GPIO Pinout Overview

3.2.3 EFM32ZG210

The features of the EFM32ZG210 is a subset of the feature set described in the EFM32ZG Reference Manual. The following table describes device specific implementation of the features.

Table 3.3. EFM32ZG210 Configuration Summary

Module	Configuration	Pin Connections
Cortex-M0+	Full configuration	NA
DBG	Full configuration	DBG_SWCLK, DBG_SWDIO
MSC	Full configuration	NA
DMA	Full configuration	NA
RMU	Full configuration	NA
EMU	Full configuration	NA
CMU	Full configuration	CMU_OUT0, CMU_OUT1
WDOG	Full configuration	NA
PRS	Full configuration	NA
I2C0	Full configuration	I2C0_SDA, I2C0_SCL
USART1	Full configuration with I2S and IrDA	US1_TX, US1_RX, US1_CLK, US1_CS
LEUART0	Full configuration	LEU0_TX, LEU0_RX
TIMER0	Full configuration	TIM0_CC[2:0]
TIMER1	Full configuration	TIM1_CC[2:0]
RTC	Full configuration	NA
PCNT0	Full configuration, 16-bit count register	PCNT0_S[1:0]
ACMP0	Full configuration	ACMP0_CH[1:0], ACMP0_O
VCMP	Full configuration	NA
ADC0	Full configuration	ADC0_CH[3:0]
IDAC0	Full configuration	IDAC0_OUT
AES	Full configuration	NA
GPIO	24 pins	Available pins are shown in 5.3.3 GPIO Pinout Overview

3.2.4 EFM32ZG222

The features of the EFM32ZG222 is a subset of the feature set described in the EFM32ZG Reference Manual. The following table describes device specific implementation of the features.

Table 3.4. EFM32ZG222 Configuration Summary

Module	Configuration	Pin Connections
Cortex-M0+	Full configuration	NA
DBG	Full configuration	DBG_SWCLK, DBG_SWDIO
MSC	Full configuration	NA
DMA	Full configuration	NA
RMU	Full configuration	NA
EMU	Full configuration	NA
CMU	Full configuration	CMU_OUT0, CMU_OUT1
WDOG	Full configuration	NA
PRS	Full configuration	NA
I2C0	Full configuration	I2C0_SDA, I2C0_SCL
USART1	Full configuration with I2S and IrDA	US1_TX, US1_RX, US1_CLK, US1_CS
LEUART0	Full configuration	LEU0_TX, LEU0_RX
TIMER0	Full configuration	TIM0_CC[2:0]
TIMER1	Full configuration	TIM1_CC[2:0]
RTC	Full configuration	NA
PCNT0	Full configuration, 16-bit count register	PCNT0_S[1:0]
ACMP0	Full configuration	ACMP0_CH[4:0], ACMP0_O
VCMP	Full configuration	NA
ADC0	Full configuration	ADC0_CH[3:0]
IDAC0	Full configuration	IDAC0_OUT
AES	Full configuration	NA
GPIO	37 pins	Available pins are shown in 5.4.3 GPIO Pinout Overview

3.3 Memory Map

The EFM32ZG memory map is shown in the following figure, with RAM and Flash sizes for the largest memory configuration.

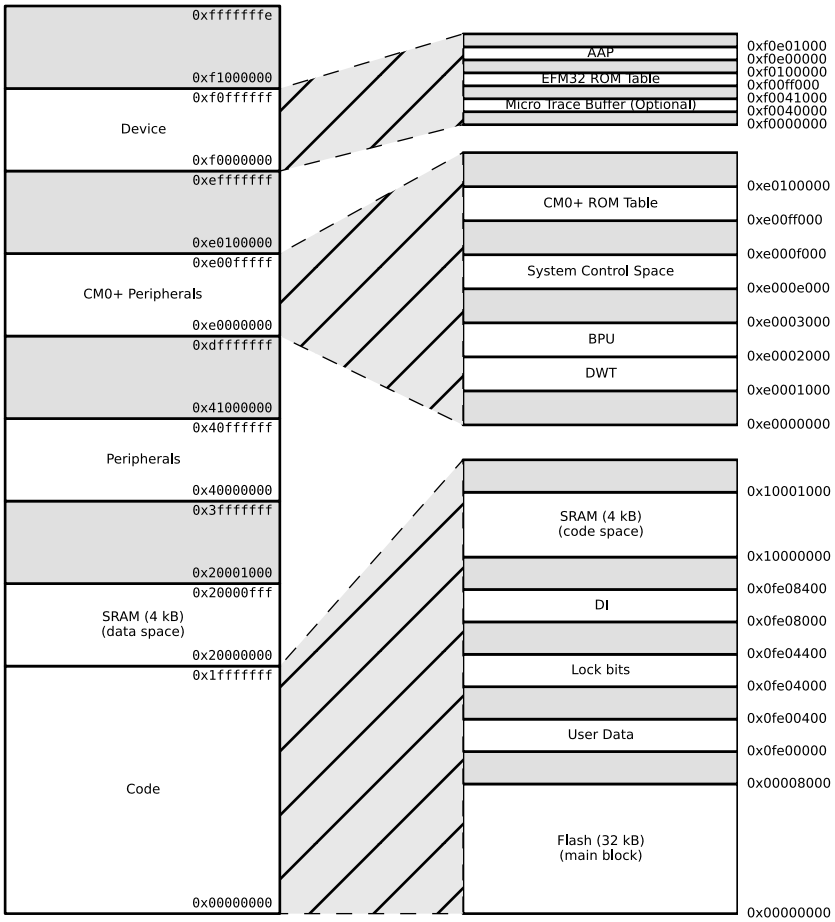


Figure 3.2. System Address Space with Core and Code Space Listing

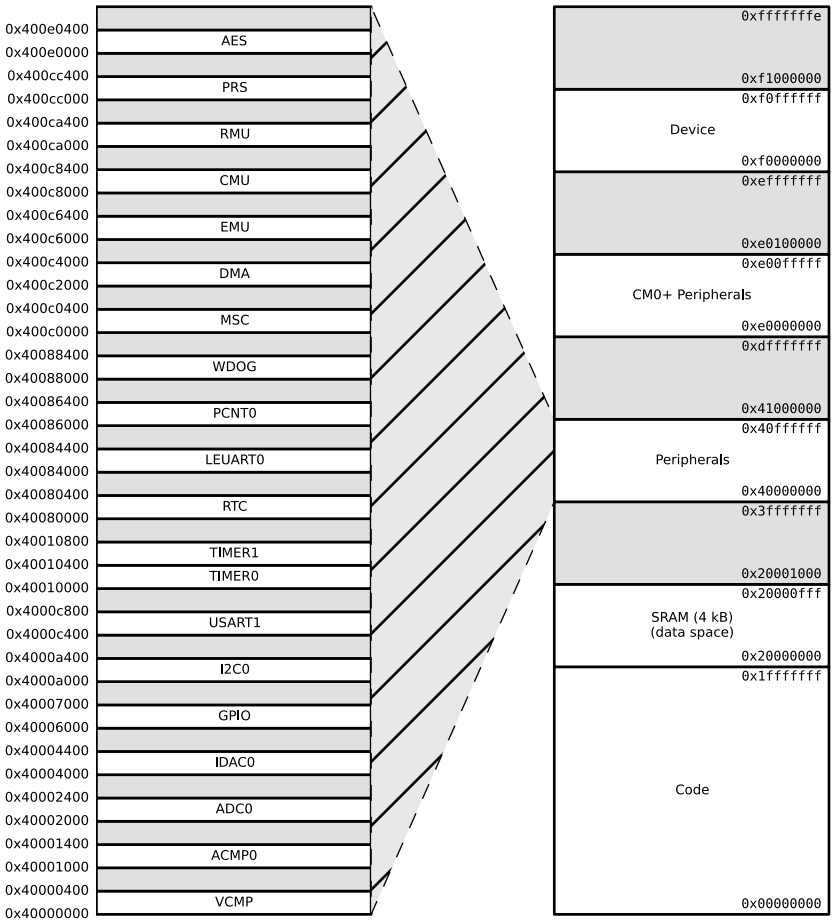


Figure 3.3. System Address Space with Peripheral Listing

4. Electrical Characteristics

4.1 Test Conditions

4.1.1 Typical Values

The typical data are based on T_{AMB}=25°C and V_{DD}=3.0 V, as defined in 4.3 General Operating Conditions, unless otherwise specified.

4.1.2 Minimum and Maximum Values

The minimum and maximum values represent the worst conditions of ambient temperature, supply voltage and frequencies, as defined in 4.3 General Operating Conditions, unless otherwise specified.

4.2 Absolute Maximum Ratings

Stresses above those listed below may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. For more information on the available quality and reliability data, see the Quality and Reliability Monitor Report at http://www.silabs.com/support/quality/pages/default.aspx.

Table 4.1. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Storage temperature range	T_{STG}		-40	—	150	°C
Maximum soldering temperature	T_S	Latest IPC/JEDEC J-STD-020 Standard	—	—	260	°C
External main supply voltage	V_{DDMAX}		0	—	3.8	V
Voltage on any I/O pin	V_{IOPIN}		-0.3	—	V_{DD}+0.3	V
Current per I/O pin (sink)	I_{IOMAX_SINK}		—	—	100	mA
Current per I/O pin (source)	I_{IOMAX_SOURCE}		—	—	-100	mA

4.3 General Operating Conditions

Table 4.2. General Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Ambient temperature range	T_{AMB}	-40	—	85	°C
Operating supply voltage	V_{DDOP}	1.98	—	3.8	V
Internal APB clock frequency	f_{APB}	—	—	24	MHz
Internal AHB clock frequency	f_{AHB}	—	—	24	MHz

4.4 Current Consumption

Table 4.3. Current Consumption

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
EM0 current. No prescaling. Running prime number calculation code from Flash. (Production test condition = 14 MHz)	I_{EM0}	24 MHz HFXO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25°C	—	115	132	µA/MHz
		24 MHz HFXO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85°C	—	117	136	µA/MHz
		21 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25°C	—	114	128	µA/MHz
		21 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85°C	—	116	132	µA/MHz
		14 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25°C	—	117	131	µA/MHz
		14 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85°C	—	118	133	µA/MHz
		11 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25°C	—	118	133	µA/MHz
		11 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85°C	—	120	135	µA/MHz
		6.6 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25°C	—	124	139	µA/MHz
		6.6 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85°C	—	125	142	µA/MHz
		1.2 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25°C	—	155	177	µA/MHz
		1.2 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85°C	—	162	181	µA/MHz

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
EM1 current (Production test condition = 14 MHz)	I_{EM1}	24 MHz HFXO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25°C	—	48	57	µA/MHz
		24 MHz HFXO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85°C	—	49	59	µA/MHz
		21 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25°C	—	48	52	µA/MHz
		21 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85°C	—	49	53	µA/MHz
		14 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25°C	—	50	54	µA/MHz
		14 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85°C	—	51	56	µA/MHz
		11 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25°C	—	52	56	µA/MHz
		11 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85°C	—	53	58	µA/MHz
		6.6 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25°C	—	57	63	µA/MHz
		6.6 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85°C	—	59	66	µA/MHz
		1.2 MHz HFRCO. all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25°C	—	89	99	µA/MHz
		1.2 MHz HFRCO. all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85°C	—	92	103	µA/MHz
EM2 current	I_{EM2}	EM2 current with RTC prescaled to 1 Hz, 32.768 kHz LFRCO, V_{DD}= 3.0 V, T_{AMB}=25°C	—	0.9	1.25	µA
		EM2 current with RTC prescaled to 1 Hz, 32.768 kHz LFRCO, V_{DD}= 3.0 V, T_{AMB}=85°C	—	1.7	2.35	µA
EM3 current	I_{EM3}	EM3 current (ULFRCO enabled, LFRCO/LFXO disabled), V_{DD}= 3.0 V, T_{AMB}=25°C	—	0.5	0.9	µA
		EM3 current (ULFRCO enabled, LFRCO/LFXO disabled), V_{DD}= 3.0 V, T_{AMB}=85°C	—	1.3	2.0	µA
EM4 current	I_{EM4}	V_{DD}= 3.0 V, T_{AMB}=25°C	—	0.02	0.035	µA
		V_{DD}= 3.0 V, T_{AMB}=85°C	—	0.29	0.700	µA

4.4.1 EM0 Current Consumption

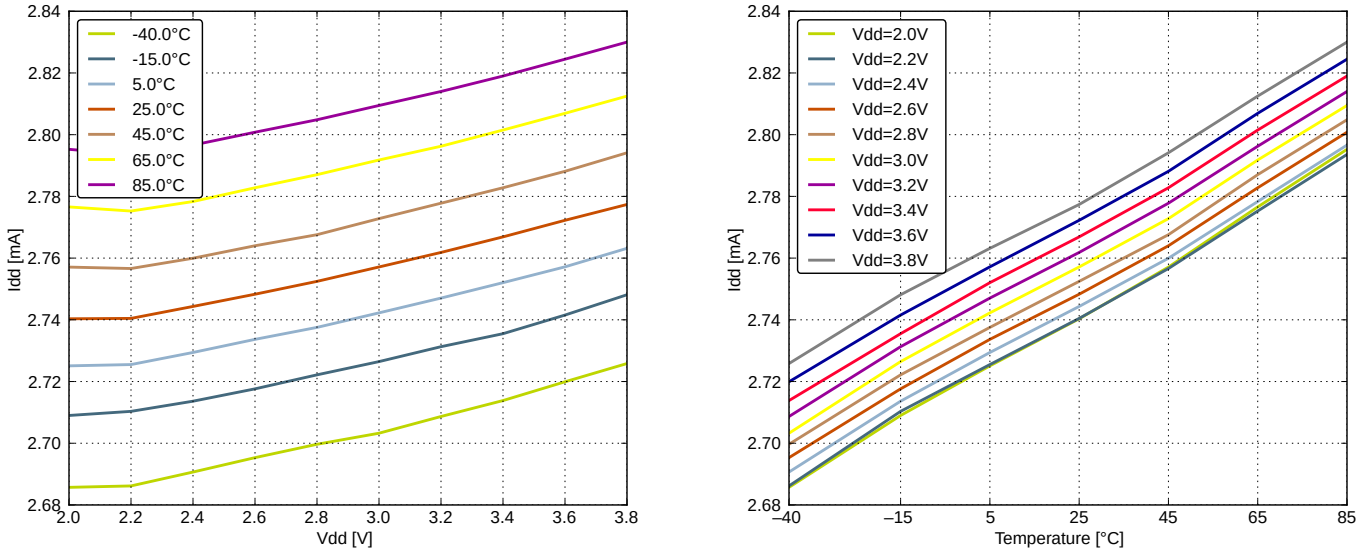


Figure 4.1. EM0 Current Consumption while Executing Prime Number Calculation Code from Flash with HFRCO Running at 24 MHz

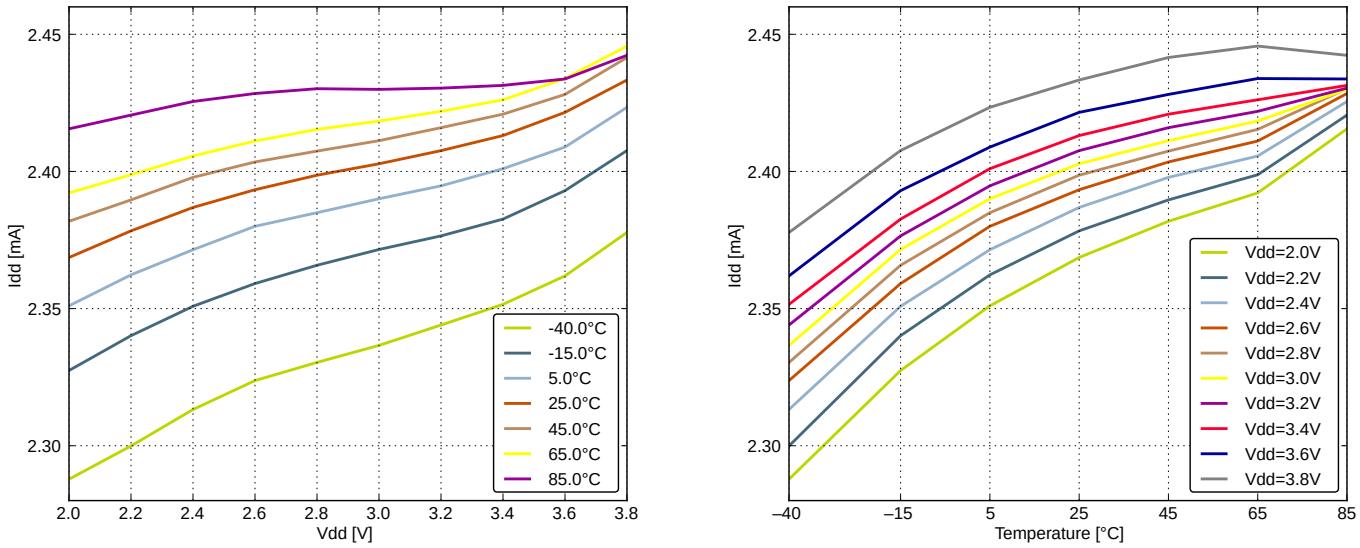


Figure 4.2. EM0 Current Consumption while Executing Prime Number Calculation Code from Flash with HFRCO Running at 21 MHz

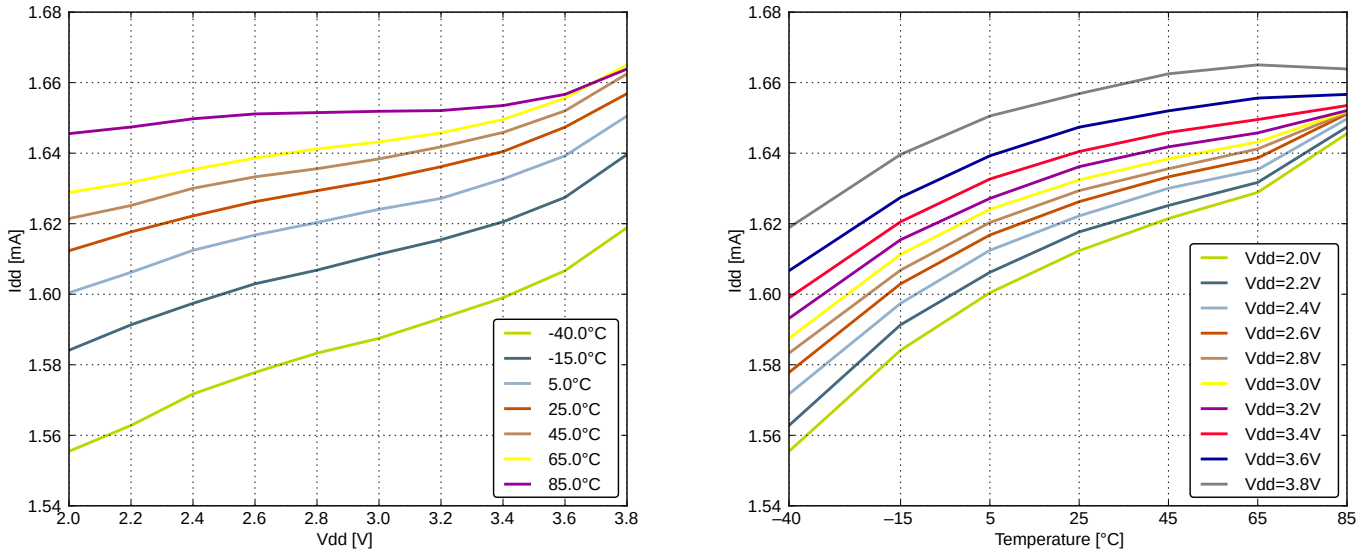


Figure 4.3. EM0 Current Consumption while Executing Prime Number Calculation Code from Flash with HFRCO Running at 14 MHz

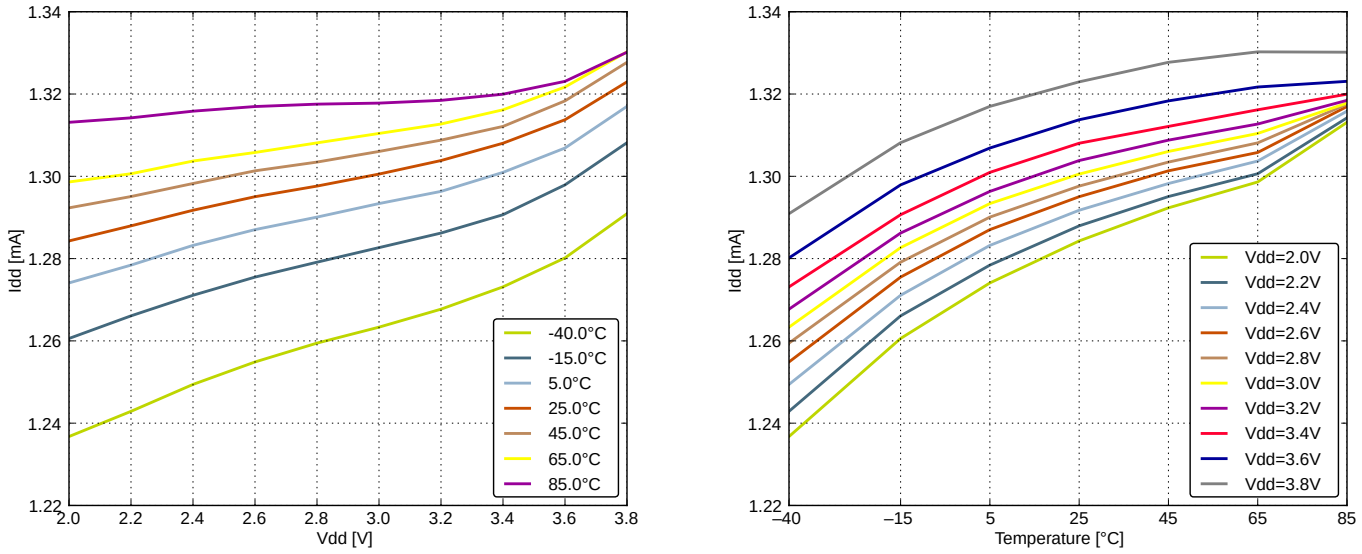


Figure 4.4. EM0 Current Consumption while Executing Prime Number Calculation Code from Flash with HFRCO Running at 11 MHz

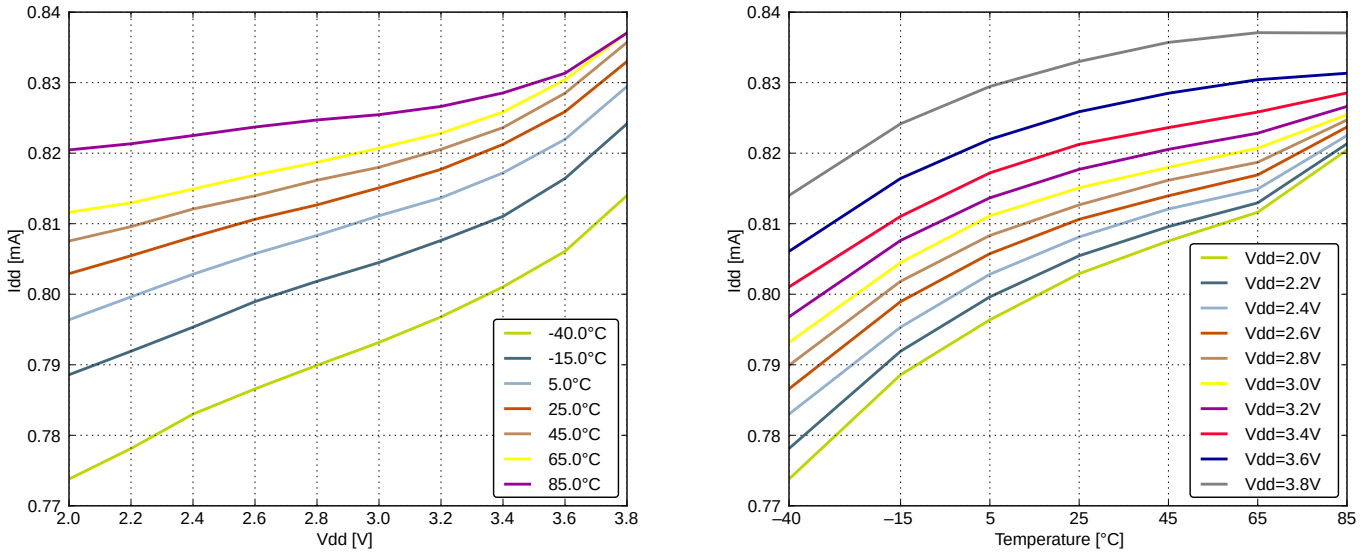


Figure 4.5. EM0 Current Consumption while Executing Prime Number Calculation Code from Flash with HFRCO Running at 6.6 MHz

4.4.2 EM1 Current Consumption

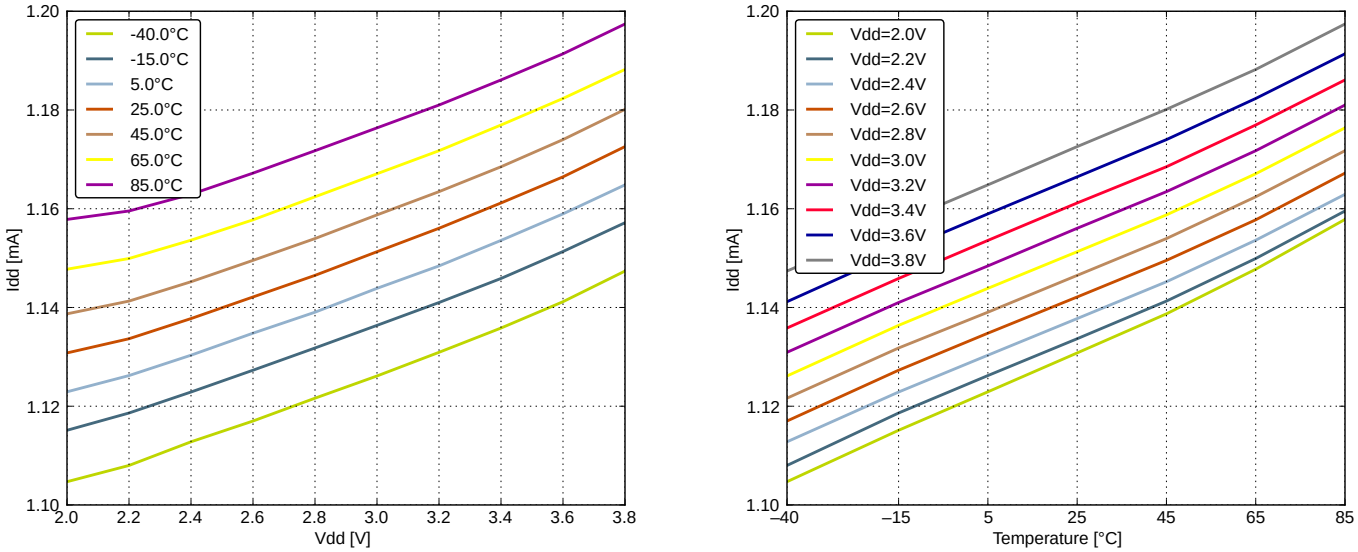


Figure 4.6. EM1 Current Consumption with all Peripheral Clocks Disabled and HFRCO Running at 24 MHz

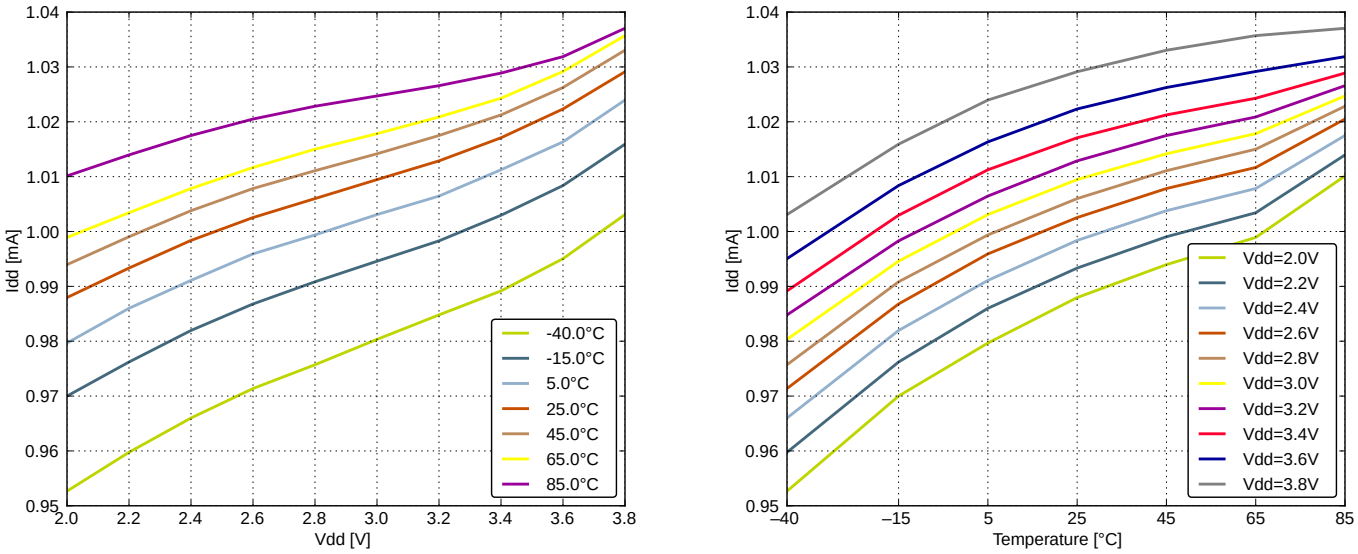


Figure 4.7. EM1 Current Consumption with all Peripheral Clocks Disabled and HFRCO Running at 21 MHz

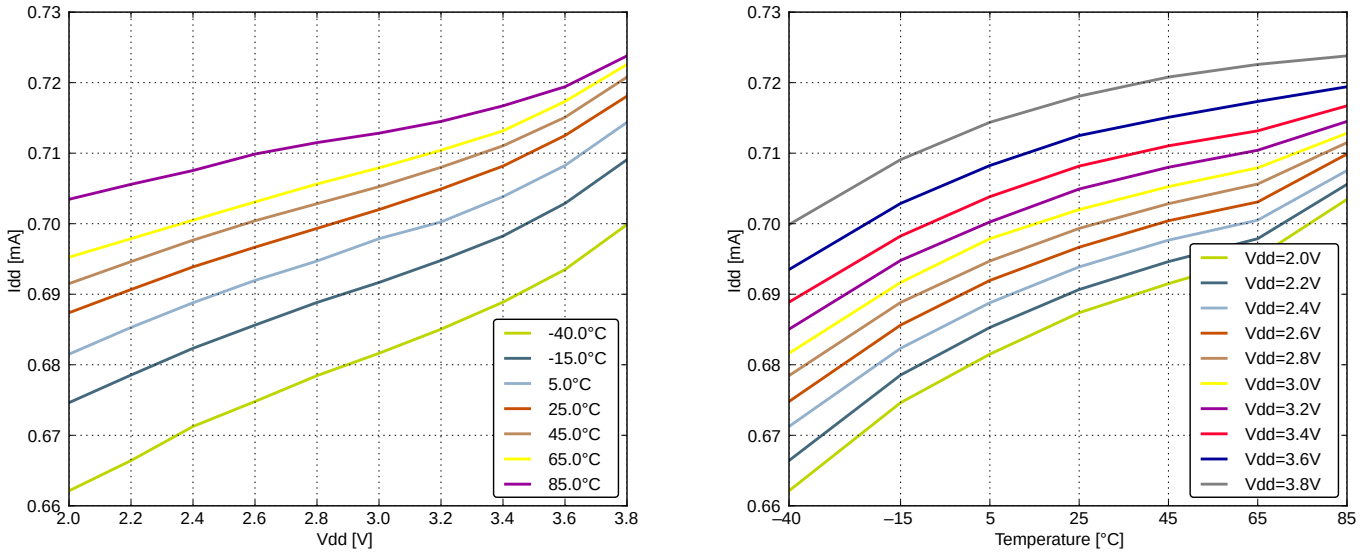


Figure 4.8. EM1 Current Consumption with all Peripheral Clocks Disabled and HFRCO Running at 14 MHz

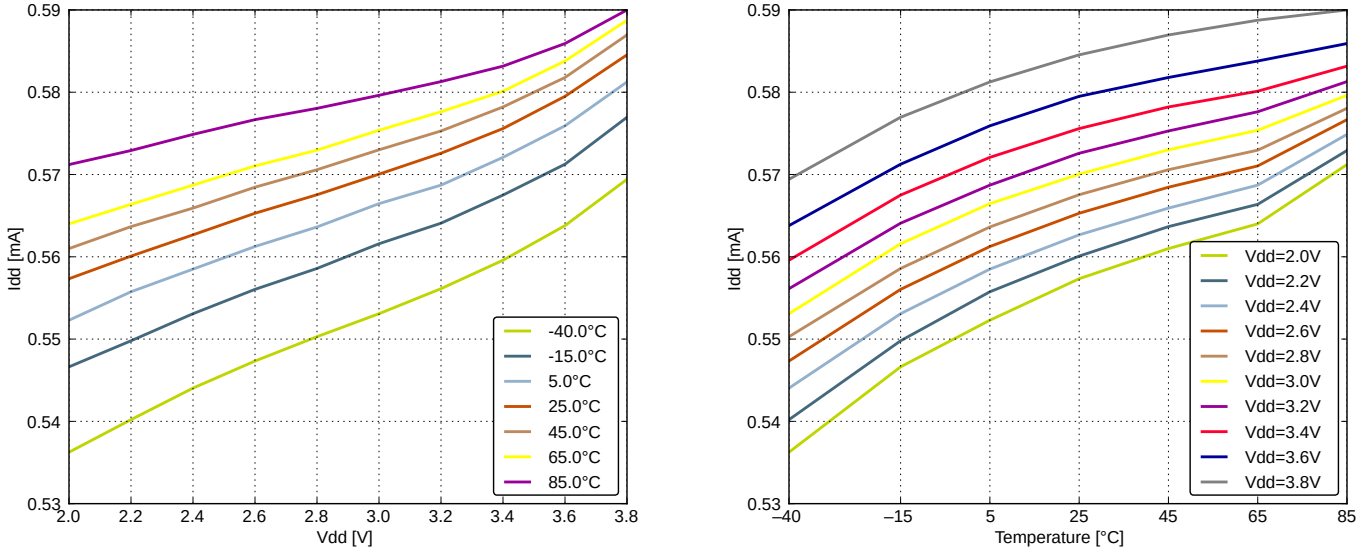


Figure 4.9. EM1 Current Consumption with all Peripheral Clocks Disabled and HFRCO Running at 11 MHz

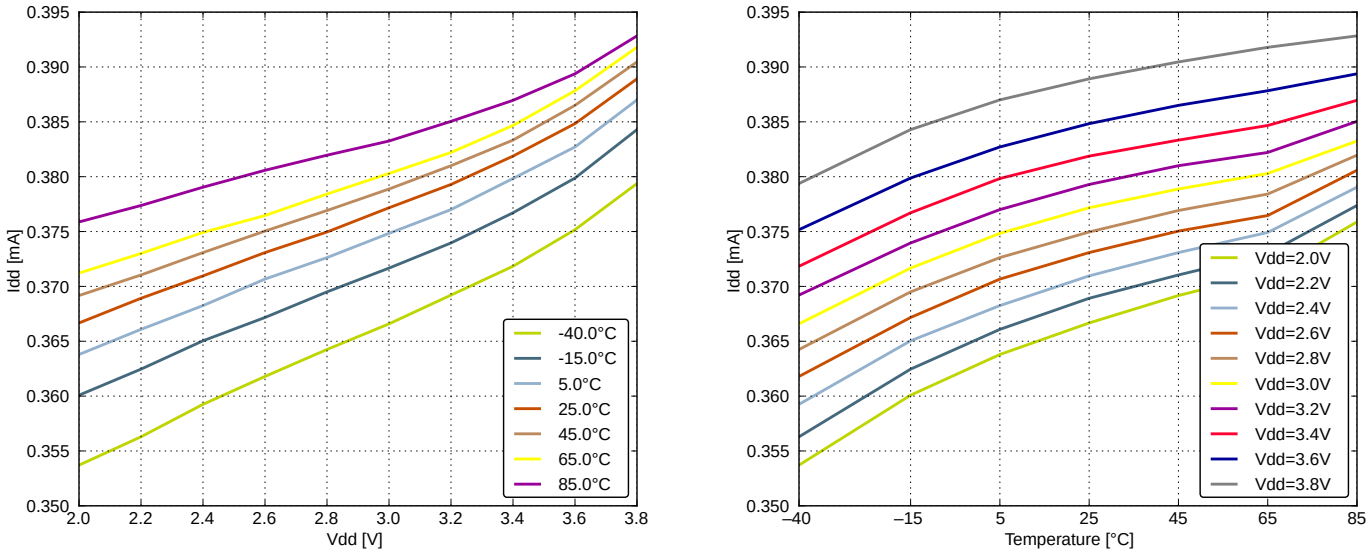


Figure 4.10. EM1 Current Consumption with all Peripheral Clocks Disabled and HFRCO Running at 6.6 MHz

4.4.3 EM2 Current Consumption

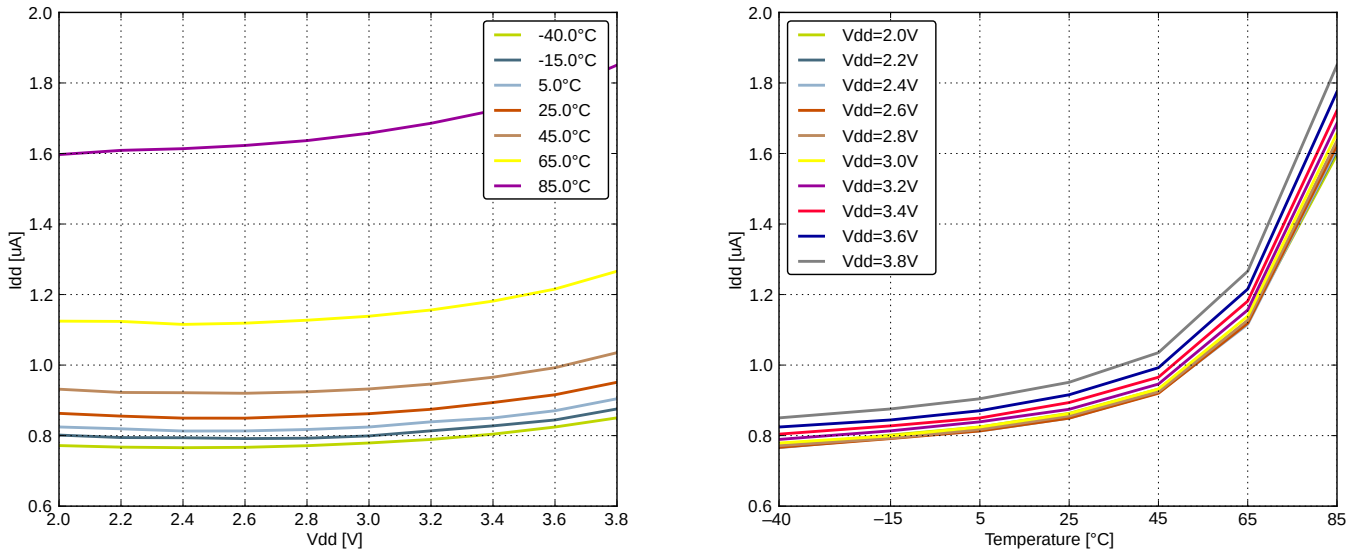


Figure 4.11. EM2 Current Consumption, RTC prescaled to 1 kHz, 32.768 kHz LFRCO

4.4.4 EM3 Current Consumption

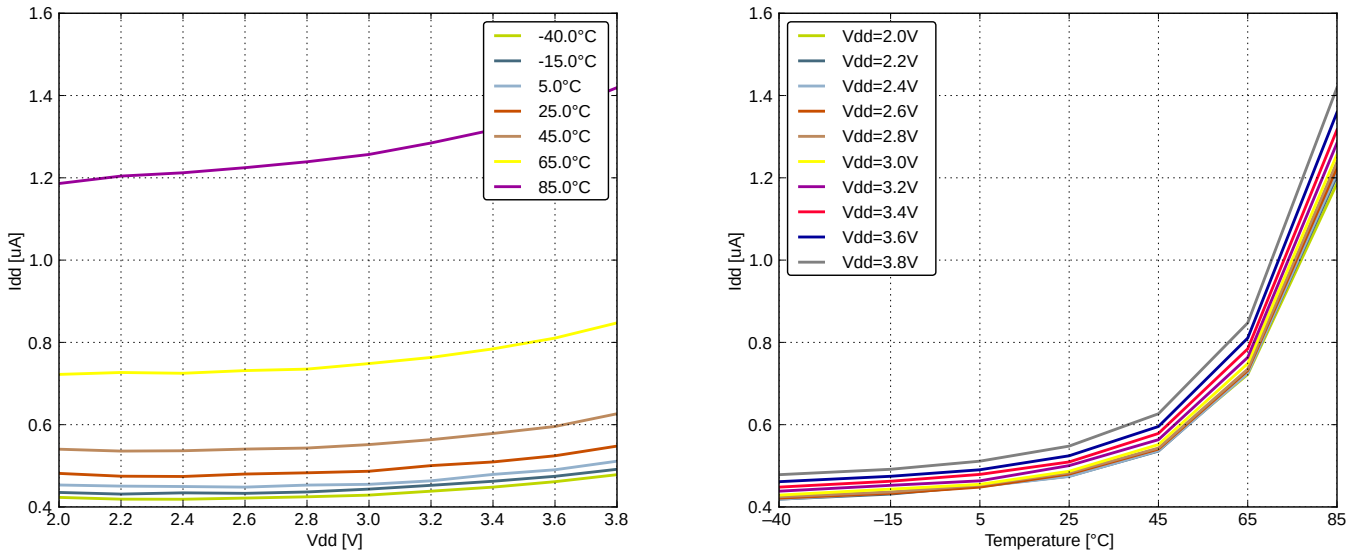


Figure 4.12. EM3 Current Consumption

4.4.5 EM4 Current Consumption

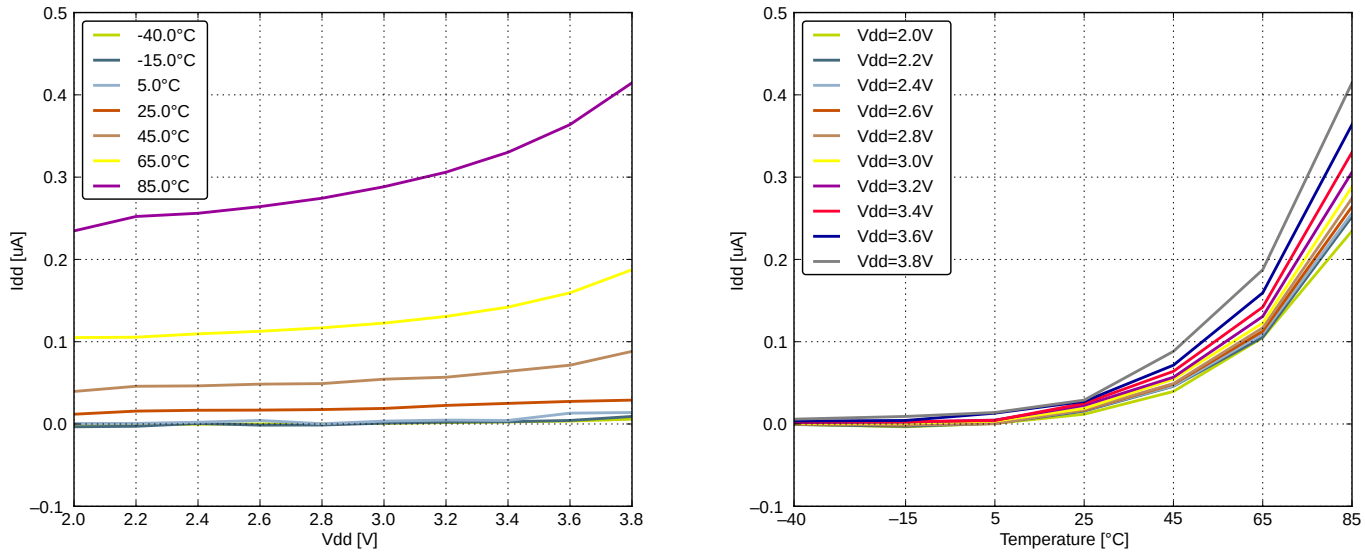


Figure 4.13. EM4 Current Consumption

4.5 Transition between Energy Modes

The transition times are measured from the trigger to the first clock edge in the CPU.

Table 4.4. Energy Modes Transitions

Parameter	Symbol	Min	Typ	Max	Unit
Transition time from EM1 to EM0	t_{EM10}	—	0	—	HFCORECLK cycles
Transition time from EM2 to EM0	t_{EM20}	—	2	—	µs
Transition time from EM3 to EM0	t_{EM30}	—	2	—	µs
Transition time from EM4 to EM0	t_{EM40}	—	163	—	µs

4.6 Power Management

The EFM32ZG requires the AVDD_x, VDD_DREG and IOVDD_x pins to be connected together (with optional filter) at the PCB level. For practical schematic recommendations, please see the application note, *AN0002 EFM32 Hardware Design Considerations*.

Table 4.5. Power Management

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
BOD threshold on falling external supply voltage	$V_{BODextthr-}$		1.74	—	1.96	V
BOD threshold on rising external supply voltage	$V_{BODextthr+}$		—	1.85	—	V
Delay from reset is released until program execution starts	t_{RESET}	Applies to Power-on Reset, Brown-out Reset and pin reset.	—	163	—	µs
Voltage regulator decoupling capacitor.	$C_{DECOUPLE}$	X5R capacitor recommended. Apply between DECOUPLE pin and GROUND	—	1	—	µF

4.7 Flash

Table 4.6. Flash

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Flash erase cycles before failure	EC_{FLASH}		20000	—	—	cycles
Flash word write cycles between erase	WWC_{FLASH}		—	—	2[1]	cycles
Flash data retention	RET_{FLASH}	T_{AMB}<150 °C	10000	—	—	h
		T_{AMB}<85 °C	10	—	—	years
		T_{AMB}<70 °C	20	—	—	years
Word (32-bit) programming time	t_{W_PROG}		20	—	—	µs
Page erase time	t_{PERASE}		20	20.4	20.8	ms
Device erase time	t_{DERASE}		40	40.8	41.6	ms
Erase current	I_{ERASE}		—	—	7[2]	mA
Write current	I_{WRITE}		—	—	7[2]	mA
Supply voltage during flash erase and write	V_{FLASH}		1.98	—	3.8	V

Note:

1. There is a maximum of two writes to the same word between each erase due to a physical limitation of the flash. No bit should be written to ‘0’ more than once between erases. To write a word twice between erases, any bit written to ‘0’ by the first write should be written to ‘1’ by the second write. This preserves the specified flash write/erase endurance and does not change the ‘0’ written by the first write.
2. Measured at 25 °C.

4.8 General Purpose Input Output

Table 4.7. GPIO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input low voltage	V_{IOIL}		—	—	0.30×V_{DD}	V
Input high voltage	V_{IOIH}		0.70×V_{DD}	—	—	V
Output high voltage (Production test condition = 3.0V, DRIVEMODE = STANDARD)	V_{IOOH}	Sourcing 0.1 mA, V_{DD}=1.98 V, GPIO_Px_CTRL DRIVEMODE = LOWEST	—	0.80×V_{DD}	—	V
		Sourcing 0.1 mA, V_{DD}=3.0 V, GPIO_Px_CTRL DRIVEMODE = LOWEST	—	0.90×V_{DD}	—	V
		Sourcing 1 mA, V_{DD}=1.98 V, GPIO_Px_CTRL DRIVEMODE = LOW	—	0.85×V_{DD}	—	V
		Sourcing 1 mA, V_{DD}=3.0 V, GPIO_Px_CTRL DRIVEMODE = LOW	—	0.90×V_{DD}	—	V
		Sourcing 6 mA, V_{DD}=1.98 V, GPIO_Px_CTRL DRIVEMODE = STANDARD	0.75×V_{DD}	—	—	V
		Sourcing 6 mA, V_{DD}=3.0 V, GPIO_Px_CTRL DRIVEMODE = STANDARD	0.85×V_{DD}	—	—	V
		Sourcing 20 mA, V_{DD}=1.98 V, GPIO_Px_CTRL DRIVEMODE = HIGH	0.60×V_{DD}	—	—	V
		Sourcing 20 mA, V_{DD}=3.0 V, GPIO_Px_CTRL DRIVEMODE = HIGH	0.80×V_{DD}	—	—	V
Output low voltage (Production test condition = 3.0V, DRIVEMODE = STANDARD)	V_{IOOL}	Sinking 0.1 mA, V_{DD}=1.98 V, GPIO_Px_CTRL DRIVEMODE = LOWEST	—	0.20×V_{DD}	—	V
		Sinking 0.1 mA, V_{DD}=3.0 V, GPIO_Px_CTRL DRIVEMODE = LOWEST	—	0.10×V_{DD}	—	V
		Sinking 1 mA, V_{DD}=1.98 V, GPIO_Px_CTRL DRIVEMODE = LOW	—	0.10×V_{DD}	—	V
		Sinking 1 mA, V_{DD}=3.0 V, GPIO_Px_CTRL DRIVEMODE = LOW	—	0.05×V_{DD}	—	V
		Sinking 6 mA, V_{DD}=1.98 V, GPIO_Px_CTRL DRIVEMODE = STANDARD	—	—	0.30×V_{DD}	V
		Sinking 6 mA, V_{DD}=3.0 V, GPIO_Px_CTRL DRIVEMODE = STANDARD	—	—	0.20×V_{DD}	V
		Sinking 20 mA, V_{DD}=1.98 V, GPIO_Px_CTRL DRIVEMODE = HIGH	—	—	0.35×V_{DD}	V
		Sinking 20 mA, V_{DD}=3.0 V, GPIO_Px_CTRL DRIVEMODE = HIGH	—	—	0.25×V_{DD}	V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input leakage current	I_{IOLEAK}	High Impedance IO connected to GROUND or VDD	—	±0.1	±100	nA
I/O pin pull-up resistor	R_{PU}		—	40	—	kΩ
I/O pin pull-down resistor	R_{PD}		—	40	—	kΩ
Internal ESD series resistor	R_{IOESD}		—	200	—	Ω
Pulse width of pulses to be removed by the glitch suppression filter	$t_{IO-GLITCH}$		10	—	50	ns
Output fall time	t_{IOOF}	GPIO_Px_CTRL DRIVEMODE = LOWEST and load capacitance C_L=12.5-25pF.	20+0.1×C_L	—	250	ns
		GPIO_Px_CTRL DRIVEMODE = LOW and load capacitance C_L=350-600pF	20+0.1×C_L	—	250	ns
I/O pin hysteresis (V_{IOTHR+} - V_{IOTHR-})	V_{IOHYST}	V_{DD} = 1.98 - 3.8 V	0.10×V_{DD}	—	—	V

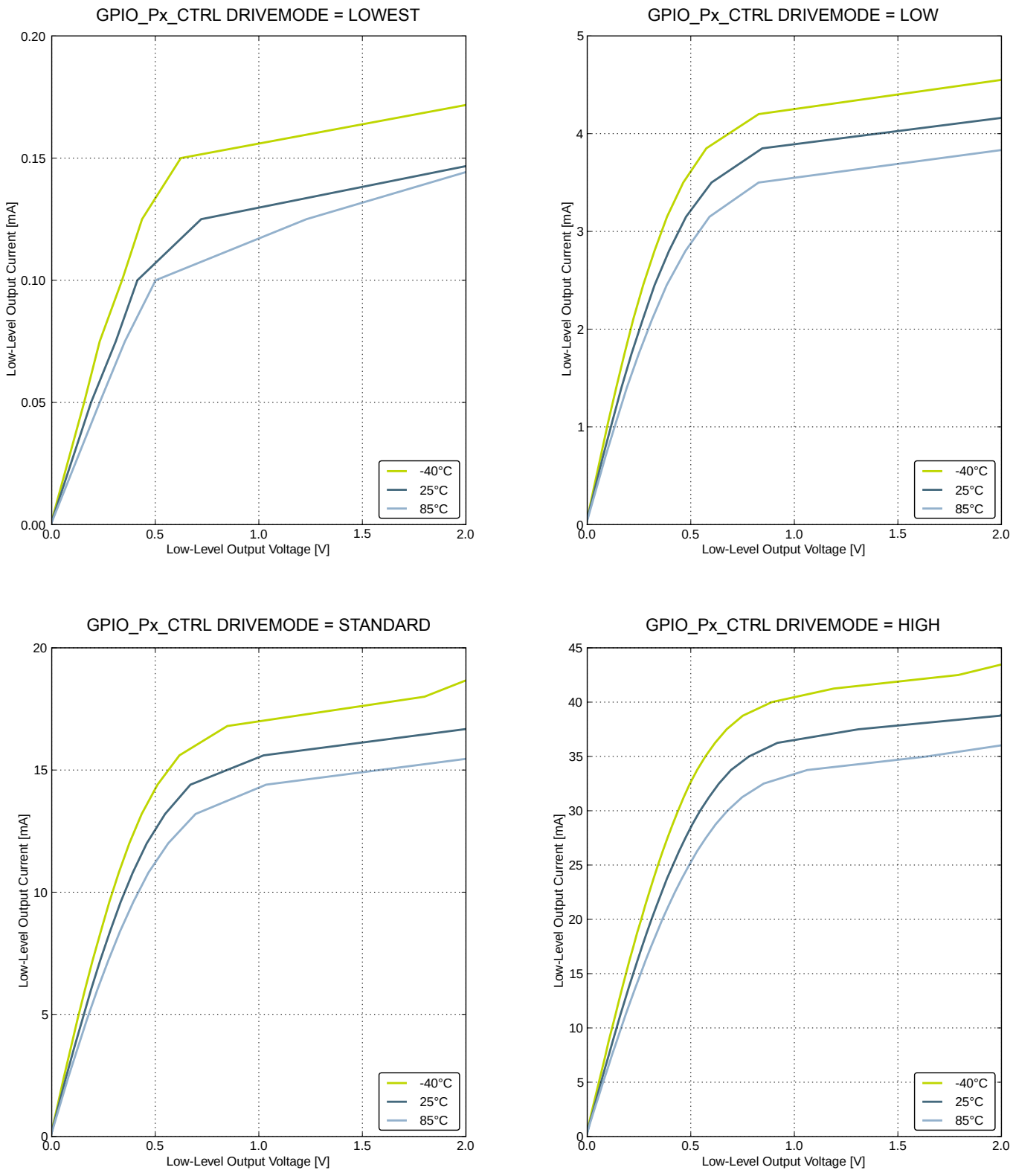


Figure 4.14. Typical Low-Level Output Current, 2V Supply Voltage

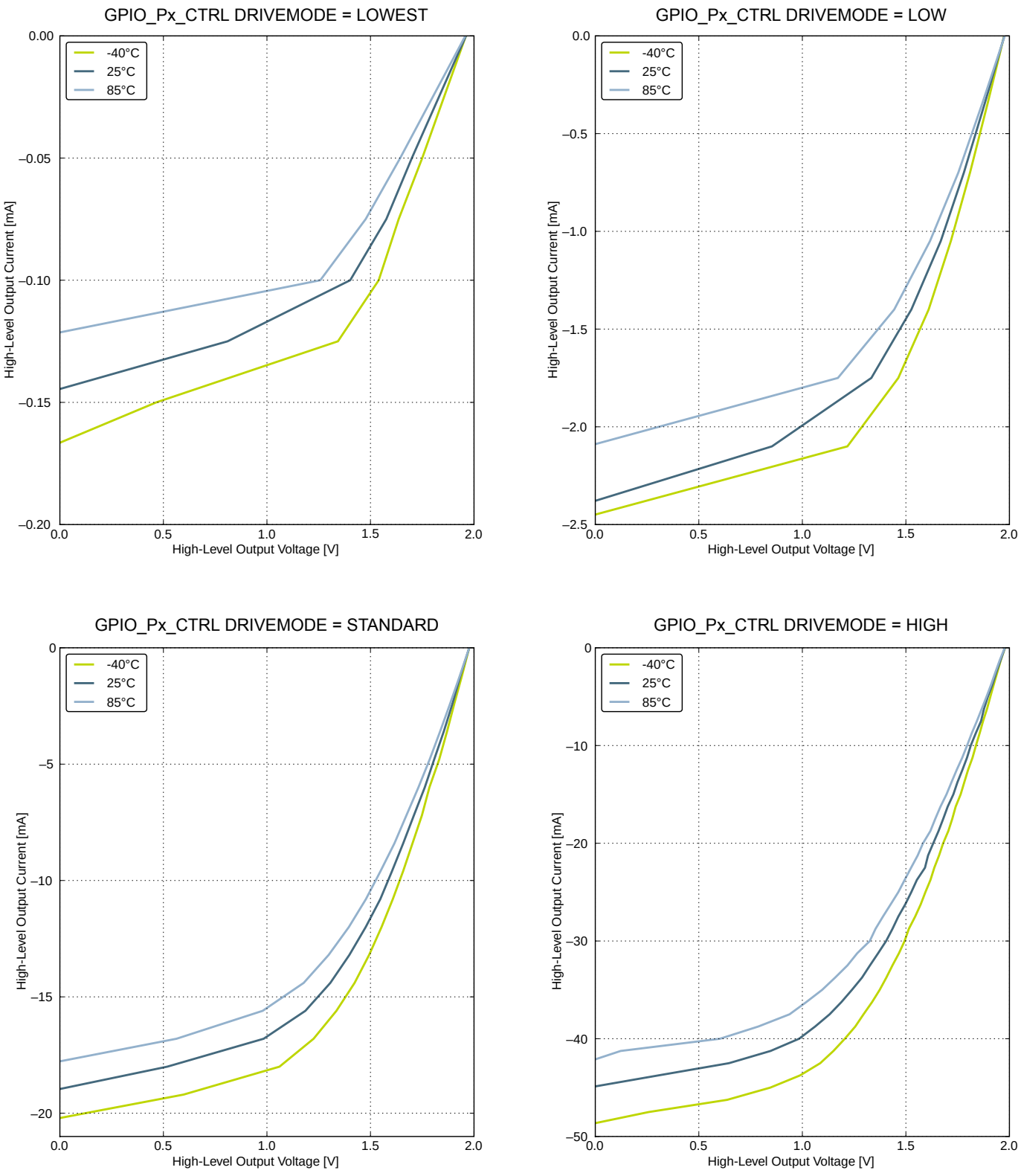


Figure 4.15. Typical High-Level Output Current, 2 V Supply Voltage

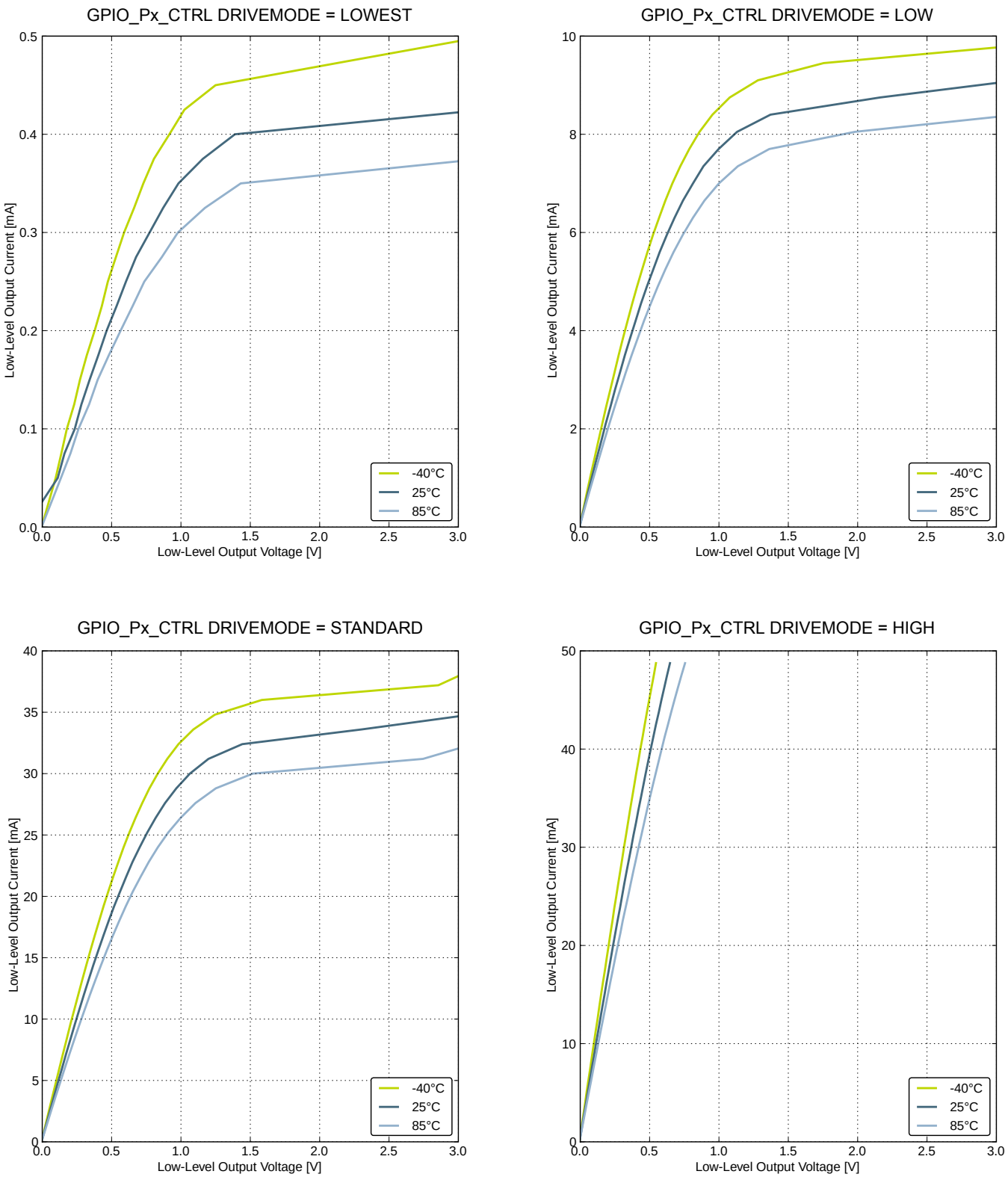


Figure 4.16. Typical Low-Level Output Current, 3 V Supply Voltage

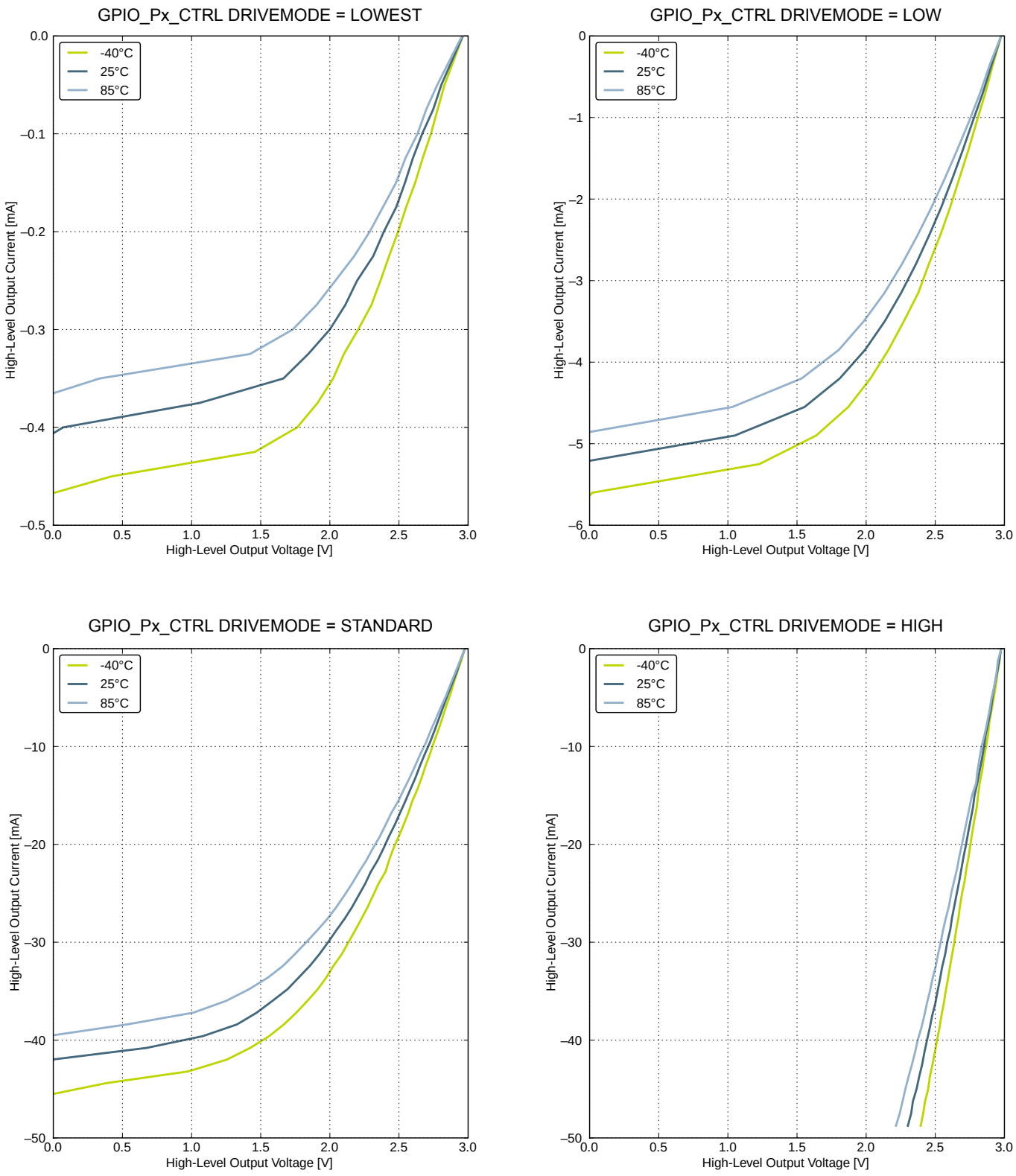


Figure 4.17. Typical High-Level Output Current, 3 V Supply Voltage

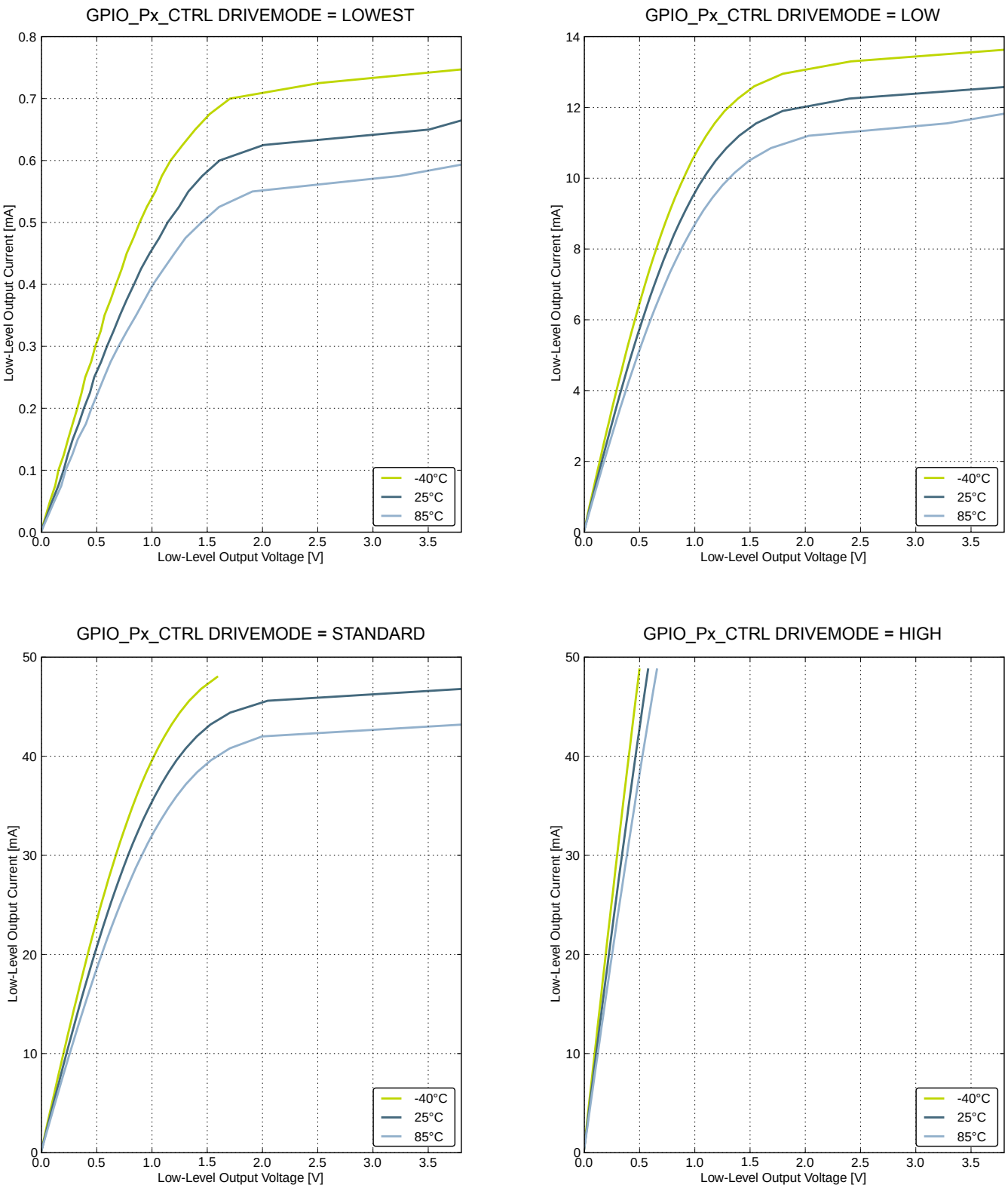


Figure 4.18. Typical Low-Level Output Current, 3.8 V Supply Voltage

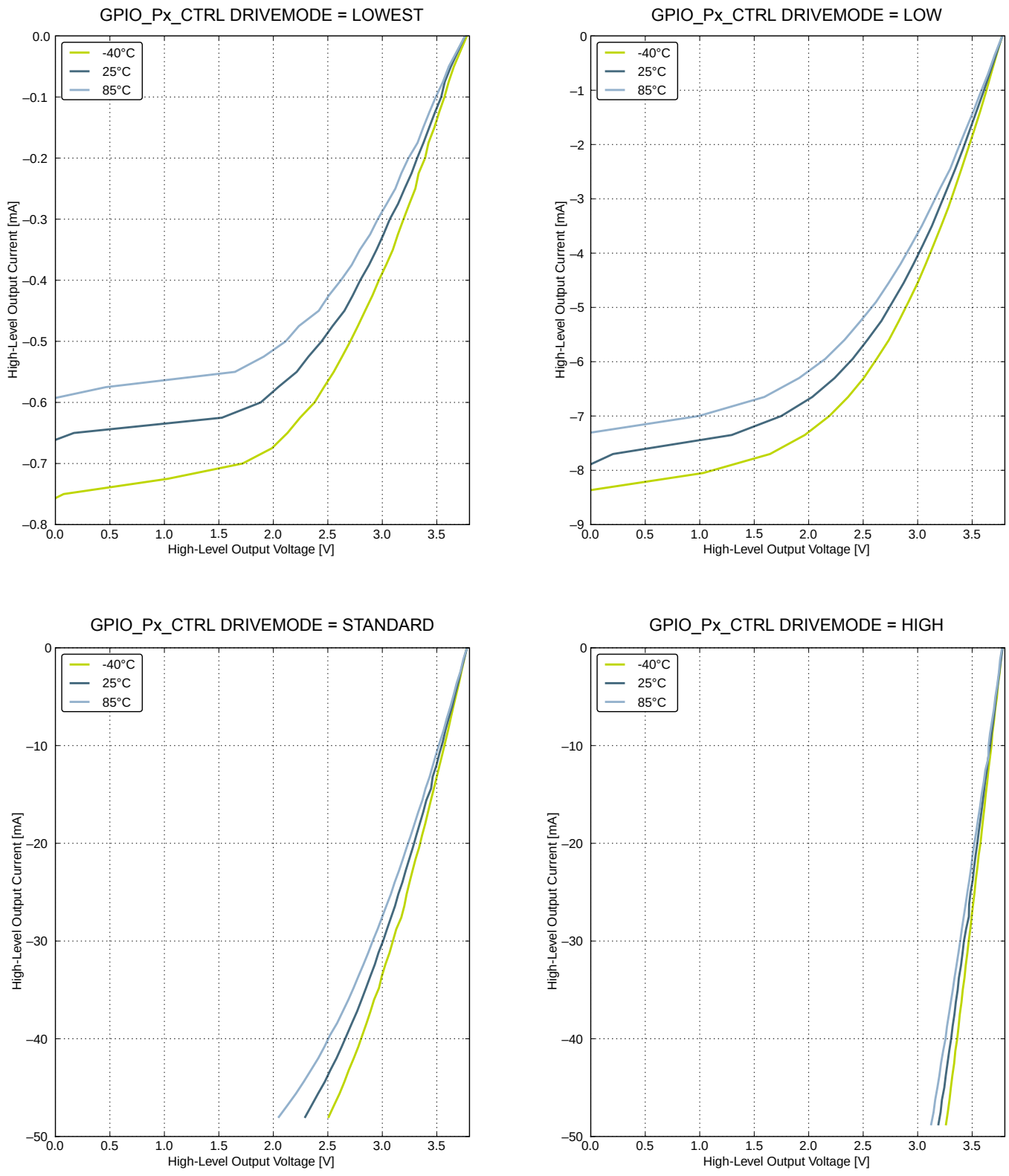


Figure 4.19. Typical High-Level Output Current, 3.8 V Supply Voltage

4.9 Oscillators

4.9.1 LFXO

Table 4.8. LFXO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supported nominal crystal frequency	f_{LFXO}		—	32.768	—	kHz
Supported crystal equivalent series resistance (ESR)	ESR_{LFXO}		—	30	120	kΩ
Supported crystal external load range	C_{LFXOL}		5	—	25	pF
Current consumption for core and buffer after startup.	I_{LFXO}	ESR=30 kΩ, C_L=10 pF, LFXOBOOST in CMU_CTRL is 1	—	190	—	nA
Start- up time.	t_{LFXO}	ESR=30 kΩ, CL=10 pF, 40% - 60% duty cycle has been reached, LFXOBOOST in CMU_CTRL is 1	—	1100	—	ms

For safe startup of a given crystal, the Configurator tool in Simplicity Studio contains a tool to help users configure both load capacitance and software settings for using the LFXO. For details regarding the crystal configuration, the reader is referred to application note *AN0016 EFM32 Oscillator Design Consideration*.

4.9.2 HFXO

Table 4.9. HFXO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supported nominal crystal Frequency	f_{HFXO}		4	—	24	MHz
Supported crystal equivalent series resistance (ESR)	ESR_{HFXO}	Crystal frequency 24 MHz	—	30	100	Ω
		Crystal frequency 4 MHz	—	400	1500	Ω
The transconductance of the HFXO input transistor at crystal startup	g_{mHFXO}	HFXOBOOST in CMU_CTRL equals 0b11	20	—	—	mS
Supported crystal external load range	C_{HFXOL}		5	—	25	pF
Current consumption for HFXO after startup	I_{HFXO}	4 MHz: ESR=400 Ω, C_L=20 pF, HFXOBOOST in CMU_CTRL equals 0b11	—	85	—	µA
		24 MHz: ESR=30 Ω, C_L=10 pF, HFXOBOOST in CMU_CTRL equals 0b11	—	165	—	µA
Startup time	t_{HFXO}	24 MHz: ESR=30 Ω, C_L=10 pF, HFXOBOOST in CMU_CTRL equals 0b11	—	785	—	µs

4.9.3 LFRCO

Table 4.10. LFRCO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Oscillation frequency, V_{DD}= 3.0 V, T_{AMB}=25°C	f_{LFRCO}		31.29	32.768	34.28	kHz
Startup time not including software calibration	t_{LFRCO}		—	150	—	µs
Current consumption	I_{LFRCO}		—	190	—	nA
Frequency step for LSB change in TUNING value	$TUNESTEP_{LFRCO}$		—	1.5	—	%

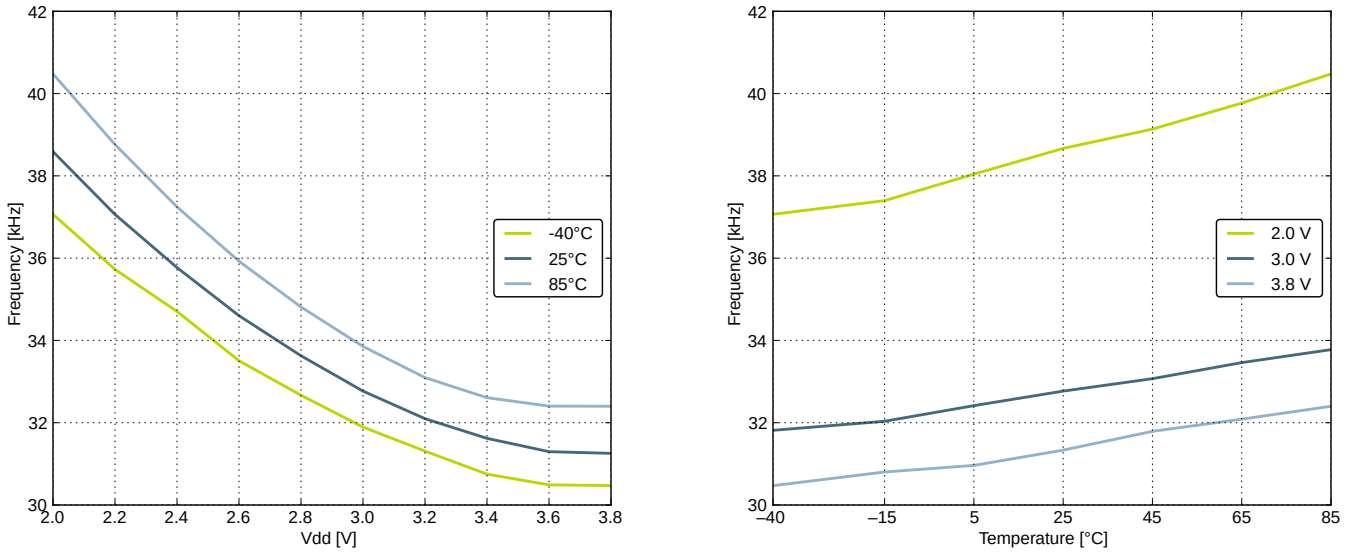


Figure 4.20. Calibrated LFRCO Frequency vs Temperature and Supply Voltage

4.9.4 HFRCO

Table 4.11. HFRCO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Oscillation frequency, V_{DD}= 3.0 V, T_{AMB}=25°C	f_{HFRCO}	21 MHz frequency band	20.37	21.0	21.63	MHz
		14 MHz frequency band	13.58	14.0	14.42	MHz
		11 MHz frequency band	10.67	11.0	11.33	MHz
		7 MHz frequency band	6.40	6.60	6.80	MHz
		1 MHz frequency band	1.15	1.20	1.25	MHz
Settling time after start-up	$t_{HFRCO_settling}$	f_{HFRCO} = 14 MHz	—	0.6	—	Cycles
Current consumption (Production test condition = 14 MHz)	I_{HFRCO}	f_{HFRCO} = 21 MHz	—	93	175	µA
		f_{HFRCO} = 14 MHz	—	77	140	µA
		f_{HFRCO} = 11 MHz	—	72	125	µA
		f_{HFRCO} = 6.6 MHz	—	63	105	µA
		f_{HFRCO} = 1.2 MHz	—	22	40	µA
Frequency step for LSB change in TUNING value	$TUNESTEP_{HFRCO}$	24 MHz frequency band	—	0.3[1]	—	%

Note:

1. The TUNING field in the CMU_HFRCOCTRL register may be used to adjust the HFRCO frequency. There is enough adjustment range to ensure that the frequency bands above 7 MHz will always have some overlap across supply voltage and temperature. By using a stable frequency reference such as the LFXO or HFXO, a firmware calibration routine can vary the TUNING bits and the frequency band to maintain the HFRCO frequency at any arbitrary value between 7 MHz and 28 MHz across operating conditions.

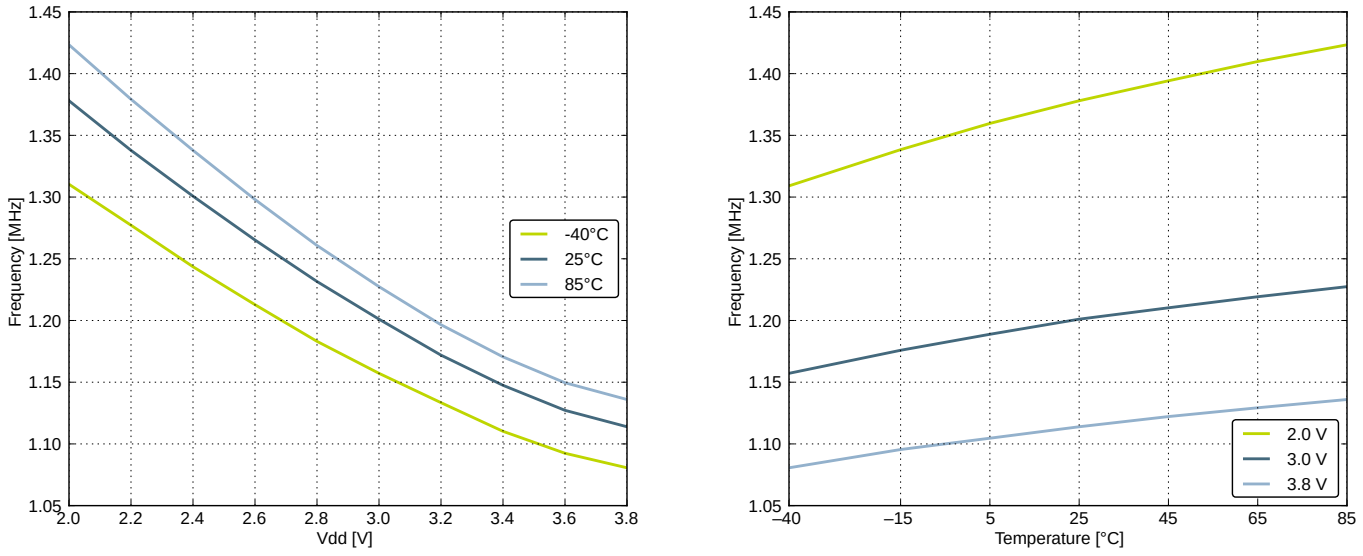


Figure 4.21. Calibrated HFRCO 1 MHz Band Frequency vs Supply Voltage and Temperature

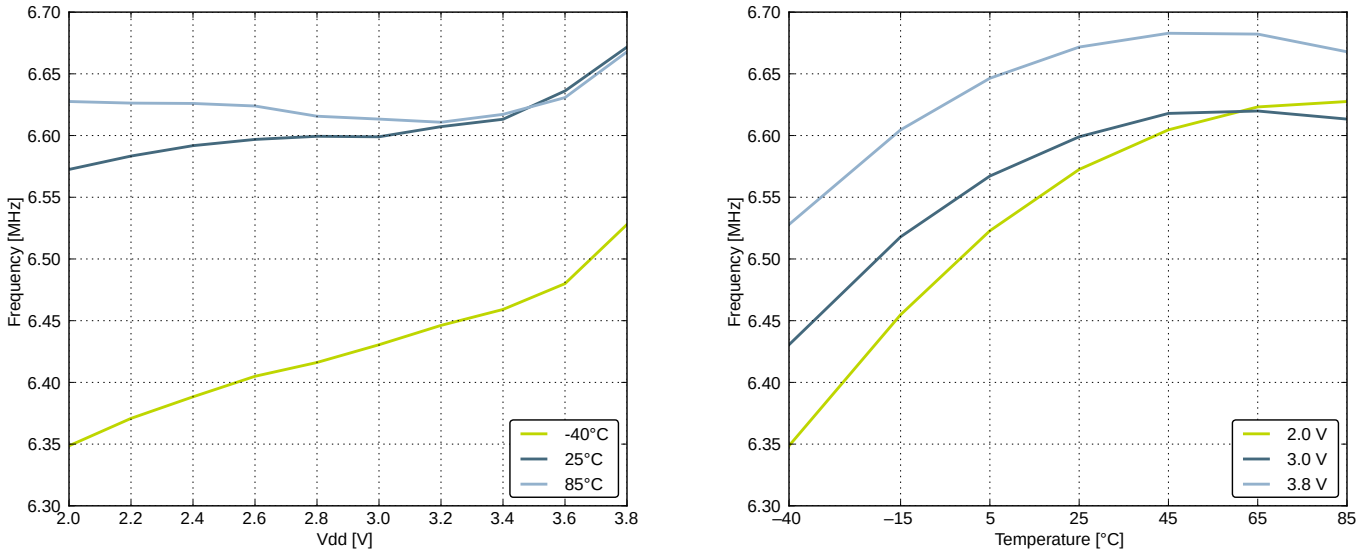


Figure 4.22. Calibrated HFRCO 7 MHz Band Frequency vs Supply Voltage and Temperature

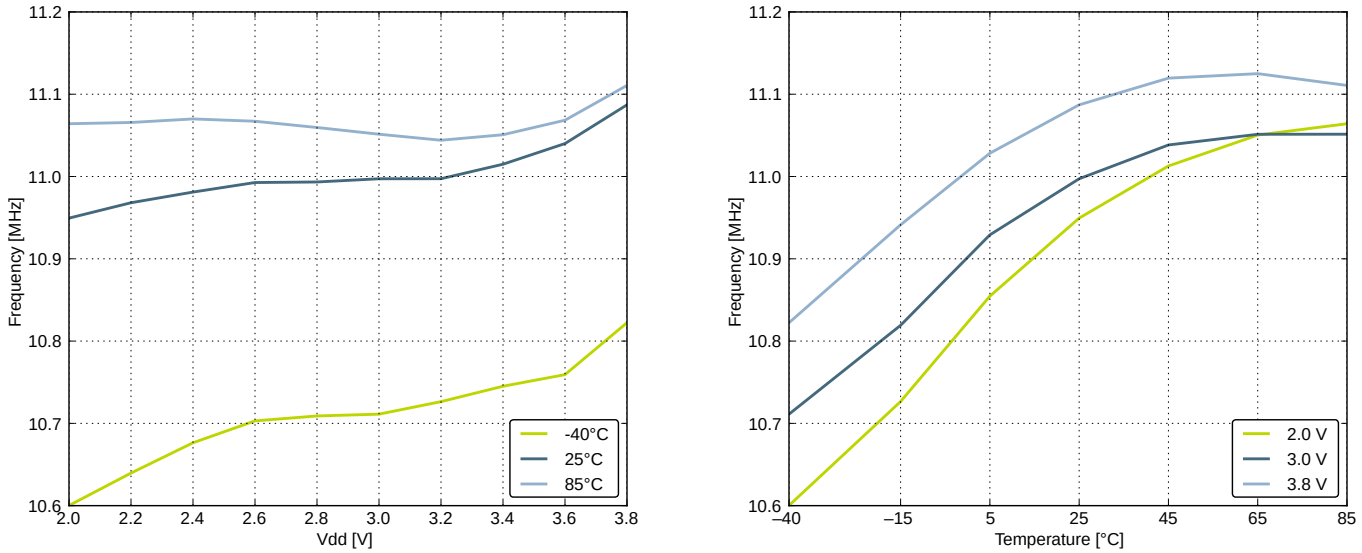


Figure 4.23. Calibrated HFRCO 11 MHz Band Frequency vs Supply Voltage and Temperature

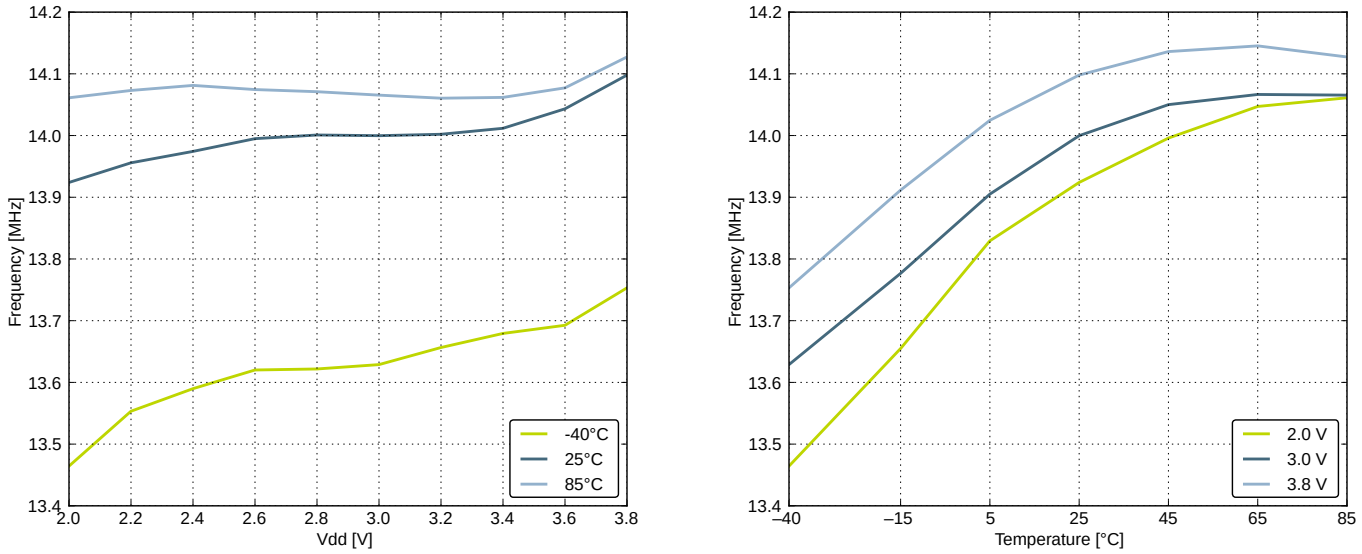


Figure 4.24. Calibrated HFRCO 14 MHz Band Frequency vs Supply Voltage and Temperature

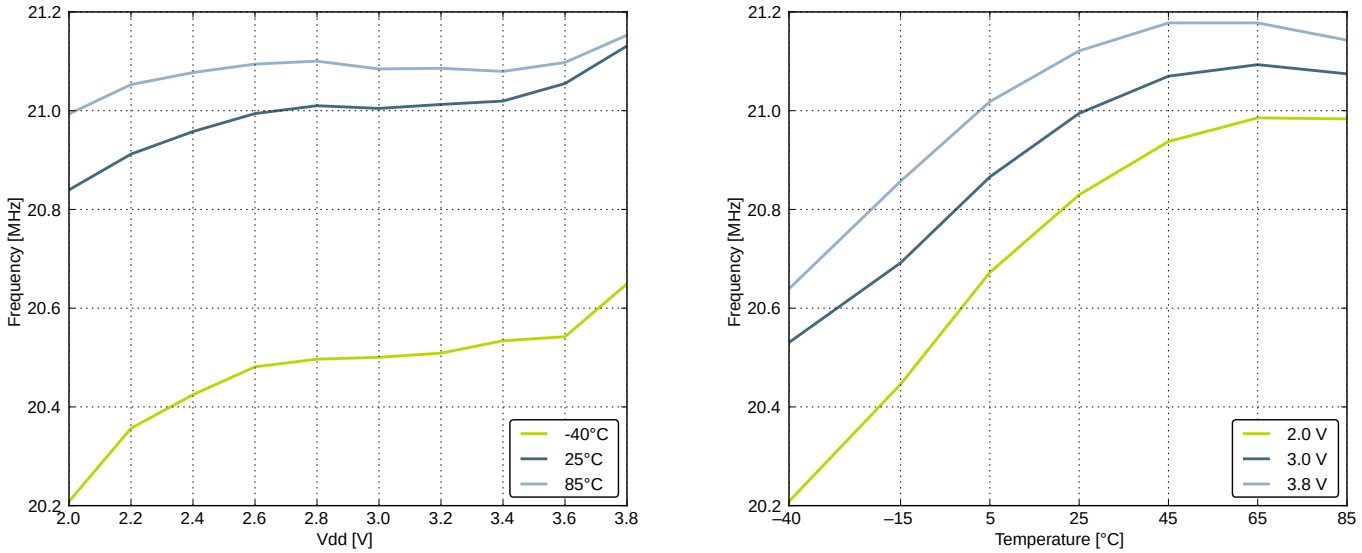


Figure 4.25. Calibrated HFRCO 21 MHz Band Frequency vs Supply Voltage and Temperature

4.9.5 AUXHFRCO

Table 4.12. AUXHFRCO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Oscillation frequency, V_{DD}= 3.0 V, T_{AMB}=25°C	$f_{AUXHFRCO}$	$f_{AUXHFRCO}$ = 21 MHz	20.37	21.0	21.63	MHz
		$f_{AUXHFRCO}$ = 14 MHz	13.58	14.0	14.42	MHz
		$f_{AUXHFRCO}$ = 11 MHz	10.67	11.0	11.33	MHz
		$f_{AUXHFRCO}$ = 6.6 MHz	6.40	6.60	6.80	MHz
		$f_{AUXHFRCO}$ = 1.2 MHz	1.15	1.20	1.25	MHz
Settling time after start-up	$t_{AUXHFRCO_settling}$	$f_{AUXHFRCO}$ = 14 MHz	—	0.6	—	Cycles
Frequency step for LSB change in TUNING value	$TUNESTEP_{AUXHFRCO}$		—	0.3	—	%

4.9.6 ULFRCO

Table 4.13. ULFRCO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Oscillation frequency	f_{ULFRCO}	25°C, 3V	0.70	—	1.75	kHz
Temperature coefficient	TC_{ULFRCO}		—	0.05	—	%/°C
Supply voltage coefficient	VC_{ULFRCO}		—	-18.2	—	%/V

4.10 Analog Digital Converter (ADC)

Table 4.14. ADC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input voltage range	V_{ADCIN}	Single-ended	0	—	V_{REF}	V
		Differential	$-V_{REF}/2$	—	$V_{REF}/2$	V
Input range of external reference voltage, single-ended and differential	$V_{ADCREFIN}$		1.25	—	V_{DD}	V
Input range of external negative reference voltage on channel 7	$V_{ADCREFIN_CH7}$	See $V_{ADCREFIN}$	0	—	V_{DD} - 1.1	V
Input range of external positive reference voltage on channel 6	$V_{ADCREFIN_CH6}$	See $V_{ADCREFIN}$	0.625	—	V_{DD}	V
Common mode input range	$V_{ADCCMIN}$		0	—	V_{DD}	V
Input current	I_{ADCIN}	2 pF sampling capacitors	—	<100	—	nA
Analog input common mode rejection ratio	$CMRR_{ADC}$		—	65	—	dB
Average active current	I_{ADC}	1 MSamples/s, 12-bit, external reference	—	351	500	µA
		10 kSamples/s 12-bit, internal 1.25 V reference, WARMUP-MODE in ADCn_CTRL set to 0b00	—	67	—	µA
		10 kSamples/s 12-bit, internal 1.25 V reference, WARMUP-MODE in ADCn_CTRL set to 0b01	—	63	—	µA
		10 kSamples/s 12-bit, internal 1.25 V reference, WARMUP-MODE in ADCn_CTRL set to 0b10	—	64	—	µA
Current Consumption of internal voltage referene	I_{ADCREF}	Internal voltage reference	—	65	127	µA
Input capacitance	C_{ADCIN}		—	2	—	pF
Input ON resistance	R_{ADCIN}		300	—	800	Ω
Input RC filter resistance	$R_{ADCFILT}$		—	10	—	kΩ
Input RC filter/decoupling capacitance	$C_{ADCFILT}$		—	250	—	fF
ADC Clock Frequency	f_{ADCCLK}		—	—	13	MHz
Conversion time	$t_{ADCCONV}$	6-bit	7	—	—	ADCCLK Cycles
		8-bit	11	—	—	ADCCLK Cycles
		12-bit	13	—	—	ADCCLK Cycles

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Acquisition time	t_{ADCACQ}	Programmable	1	—	256	ADCCLK Cycles
Required acquisition time for VDD/3 reference	$t_{ADCACQVDD3}$		2	—	—	µs
Startup time of reference generator and ADC core	$t_{ADCSTART}$	NORMAL mode	—	5	—	µs
		KEEPADCWARM mode	—	1	—	µs
Signal-to-Noise Ratio (SNR)	SNR_{ADC}	1 MSamples/s, 12-bit, single-ended, internal 1.25 V reference	—	59	—	dB
		1 MSamples/s, 12-bit, single-ended, internal 2.5 V reference	—	63	—	dB
		1 MSamples/s, 12-bit, single-ended, VDD reference	—	65	—	dB
		1 MSamples/s, 12-bit, differential, internal 1.25 V reference	—	60	—	dB
		1 MSamples/s, 12-bit, differential, internal 2.5 V reference	—	65	—	dB
		1 MSamples/s, 12-bit, differential, 5 V reference	—	54	—	dB
		1 MSamples/s, 12-bit, differential, VDD reference	—	67	—	dB
		1 MSamples/s, 12-bit, differential, 2xVDD reference	—	69	—	dB
		200 kSamples/s, 12-bit, single-ended, internal 1.25 V reference	—	62	—	dB
		200 kSamples/s, 12-bit, single-ended, internal 2.5 V reference	—	63	—	dB
		200 kSamples/s, 12-bit, single-ended, VDD reference	—	67	—	dB
		200 kSamples/s, 12-bit, differential, internal 1.25 V reference	—	63	—	dB
		200 kSamples/s, 12-bit, differential, internal 2.5 V reference	—	66	—	dB
		200 kSamples/s, 12-bit, differential, 5 V reference	—	66	—	dB
		200 kSamples/s, 12-bit, differential, VDD reference	63	66	—	dB
		200 kSamples/s, 12-bit, differential, 2xVDD reference	—	70	—	dB

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Signal-to-Noise And Distortion Ratio (SINAD)	$SINAD_{ADC}$	1 MSamples/s, 12-bit, single-ended, internal 1.25V reference	—	58	—	dB
		1 MSamples/s, 12-bit, single-ended, internal 2.5 V reference	—	62	—	dB
		1 MSamples/s, 12-bit, single-ended, VDD reference	—	64	—	dB
		1 MSamples/s, 12-bit, differential, internal 1.25 V reference	—	60	—	dB
		1 MSamples/s, 12-bit, differential, internal 2.5 V reference	—	64	—	dB
		1 MSamples/s, 12-bit, differential, 5 V reference	—	54	—	dB
		1 MSamples/s, 12-bit, differential, VDD reference	—	66	—	dB
		1 MSamples/s, 12-bit, differential, 2xVDD reference	—	68	—	dB
		200 kSamples/s, 12-bit, single-ended, internal 1.25 V reference	—	61	—	dB
		200 kSamples/s, 12-bit, single-ended, internal 2.5 V reference	—	65	—	dB
		200 kSamples/s, 12-bit, single-ended, VDD reference	—	66	—	dB
		200 kSamples/s, 12-bit, differential, internal 1.25 V reference	—	63	—	dB
		200 kSamples/s, 12-bit, differential, internal 2.5 V reference	—	66	—	dB
		200 kSamples/s, 12-bit, differential, 5V reference	—	66	—	dB
		200 kSamples/s, 12-bit, differential, VDD reference	62	66	—	dB
		200 kSamples/s, 12-bit, differential, 2xVDD reference	—	69	—	dB

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Spurious-Free Dynamic Range (SFDR)	$SFDR_{ADC}$	1 MSamples/s, 12-bit, single-ended, internal 1.25 V reference	—	64	—	dBc
		1 MSamples/s, 12-bit, single-ended, internal 2.5 V reference	—	76	—	dBc
		1 MSamples/s, 12-bit, single-ended, VDD reference	—	73	—	dBc
		1 MSamples/s, 12-bit, differential, internal 1.25 V reference	—	66	—	dBc
		1 MSamples/s, 12-bit, differential, internal 2.5 V reference	—	77	—	dBc
		1 MSamples/s, 12-bit, differential, VDD reference	—	76	—	dBc
		1 MSamples/s, 12-bit, differential, 2xVDD reference	—	75	—	dBc
		1 MSamples/s, 12-bit, differential, 5 V reference	—	69	—	dBc
		200 kSamples/s, 12-bit, single-ended, internal 1.25 V reference	—	75	—	dBc
		200 kSamples/s, 12-bit, single-ended, internal 2.5 V reference	—	75	—	dBc
		200 kSamples/s, 12-bit, single-ended, VDD reference	—	76	—	dBc
		200 kSamples/s, 12-bit, differential, internal 1.25 V reference	—	79	—	dBc
		200 kSamples/s, 12-bit, differential, internal 2.5 V reference	—	79	—	dBc
		200 kSamples/s, 12-bit, differential, 5 V reference	—	78	—	dBc
		200 kSamples/s, 12-bit, differential, VDD reference	68	79	—	dBc
		200 kSamples/s, 12-bit, differential, 2xVDD reference	—	79	—	dBc
Offset voltage	$V_{ADCOFFSET}$	After calibration, single-ended	-4	0.3	4	mV
		After calibration, differential	—	0.3	—	mV
Thermometer output gradient	$TGRAD_{ADCTH}$		—	-1.92	—	mV/°C
			—	-6.3	—	ADC Codes/°C
Differential non-linearity (DNL)	DNL_{ADC}	V_{DD}= 3.0 V, external 2.5V reference	-1	±0.7	4	LSB
Integral non-linearity (INL), End point method	INL_{ADC}	V_{DD}= 3.0 V, external 2.5V reference	—	±1.2	±3	LSB
Missing codes	MC_{ADC}		11.999 [1]	12	—	bits

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit

Note:

1. On the average every ADC will have one missing code, most likely to appear around 2048 +/- n*512 where n can be a value in the set {-3, -2, -1, 1, 2, 3}. There will be no missing code around 2048, and in spite of the missing code the ADC will be monotonic at all times so that a response to a slowly increasing input will always be a slowly increasing output. Around the one code that is missing, the neighbor codes will look wider in the DNL plot. The spectra will show spurs on the level of -78dBc for a full-scale input for chips that have the missing code issue.

The integral non-linearity (INL) and differential non-linearity parameters are explained in the following two figures.

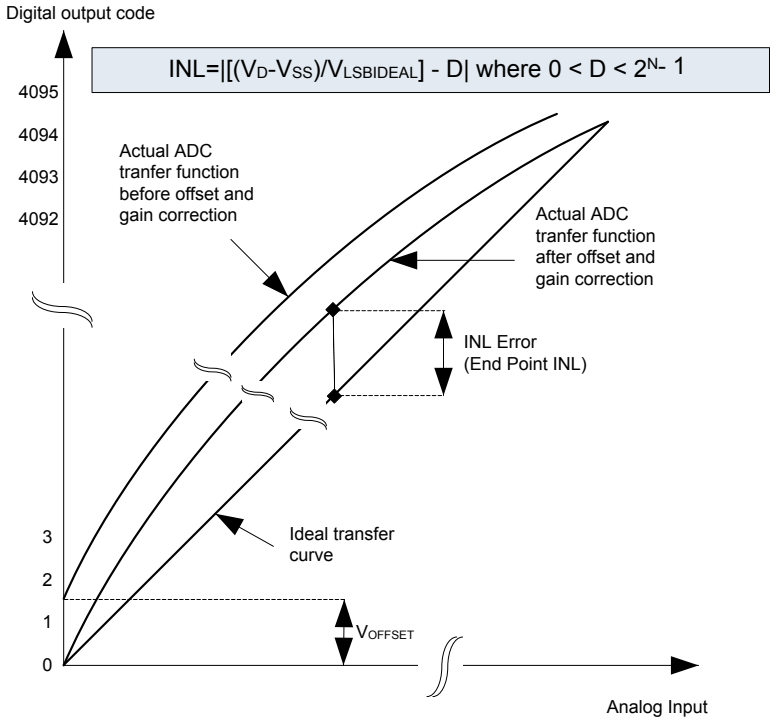


Figure 4.26. Integral Non-Linearity (INL)

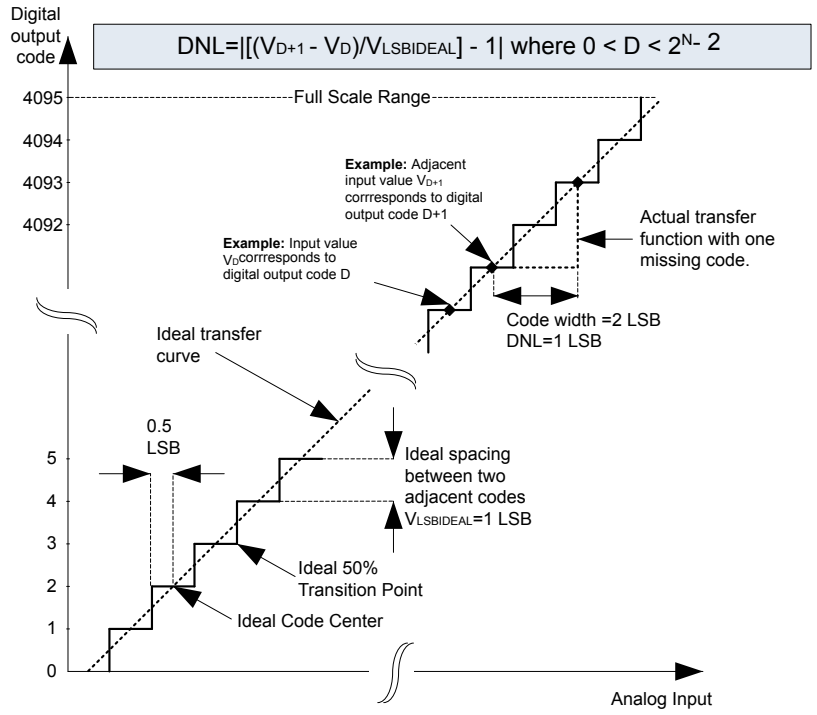


Figure 4.27. Differential Non-Linearity (DNL)

4.10.1 Typical Performance

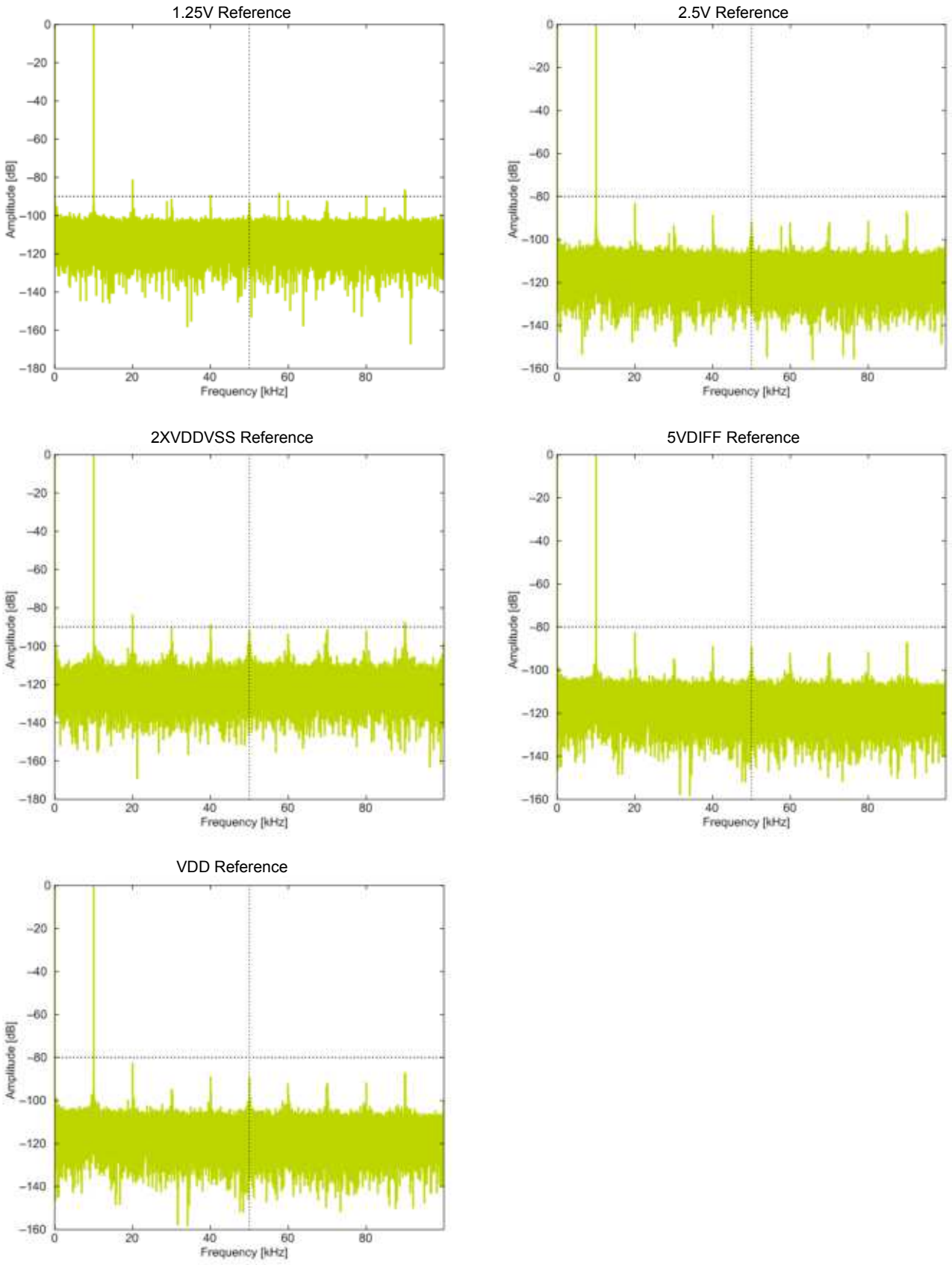


Figure 4.28. ADC Frequency Spectrum, VDD = 3 V, Temp = 25 °C

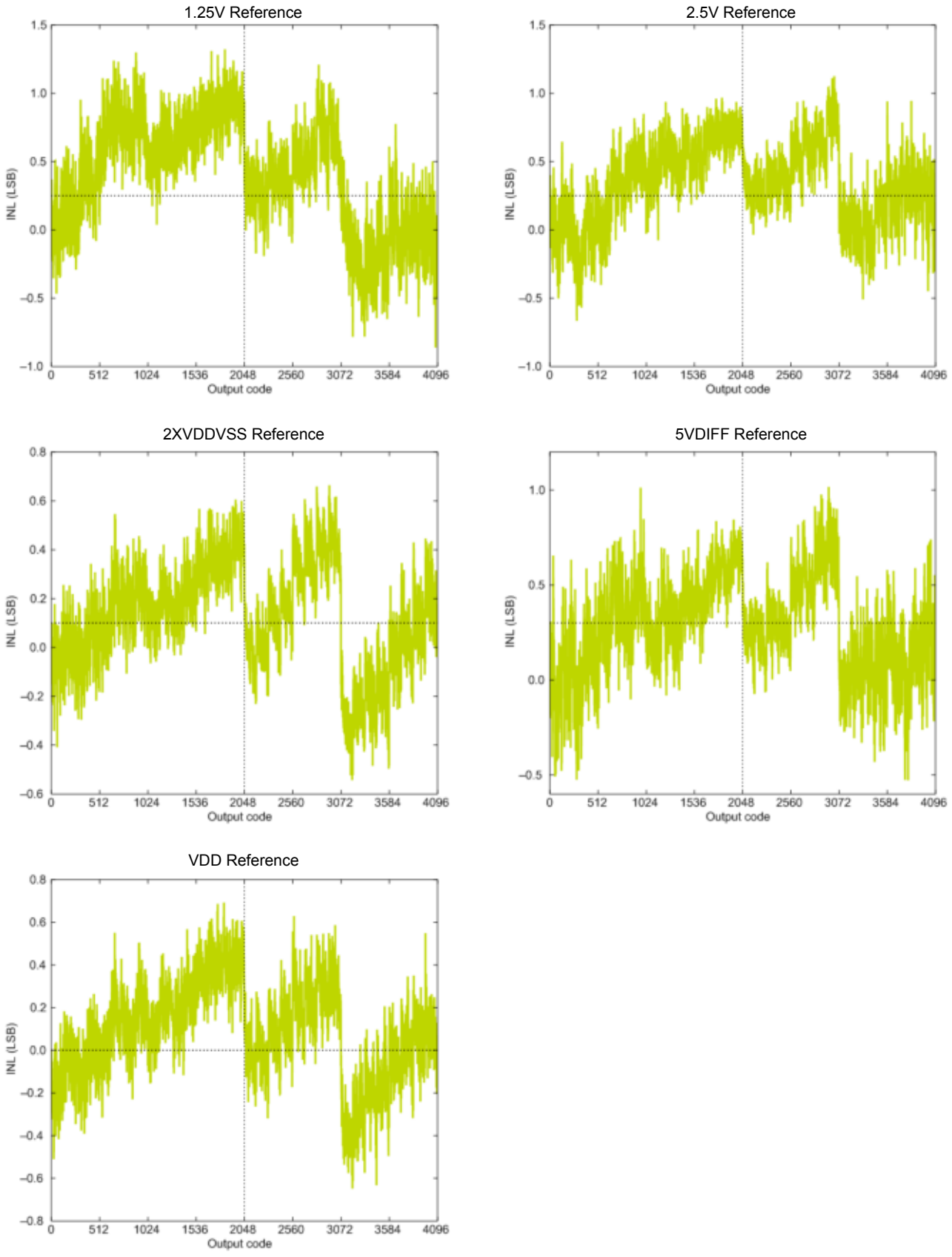


Figure 4.29. ADC Integral Linearity Error vs Code, VDD = 3 V, Temp = 25 °C

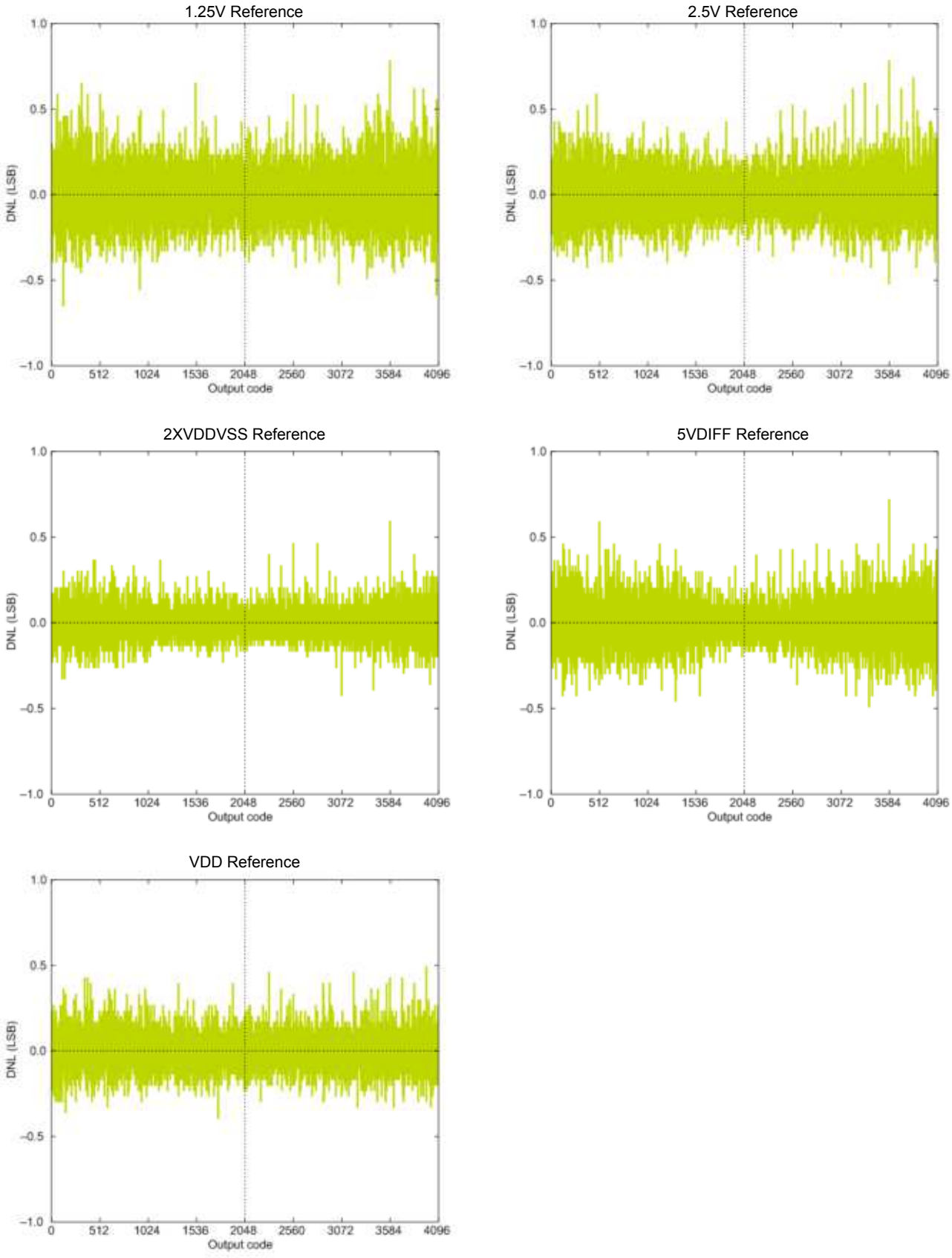


Figure 4.30. ADC Differential Linearity Error vs Code, VDD = 3 V, Temp = 25 °C

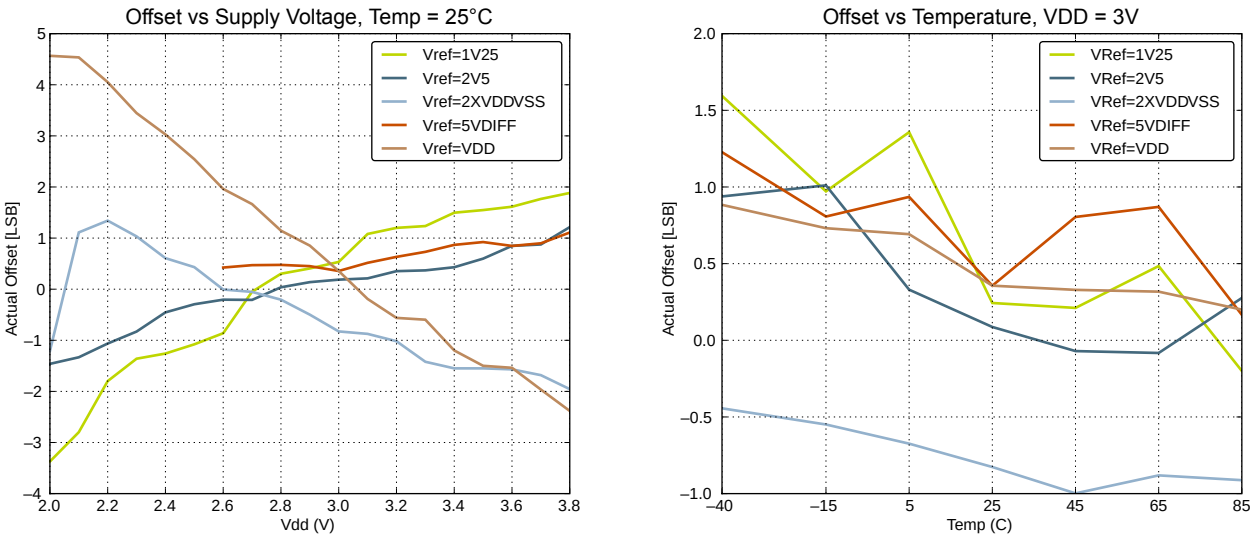


Figure 4.31. ADC Absolute Offset, Common Mode = VDD/2

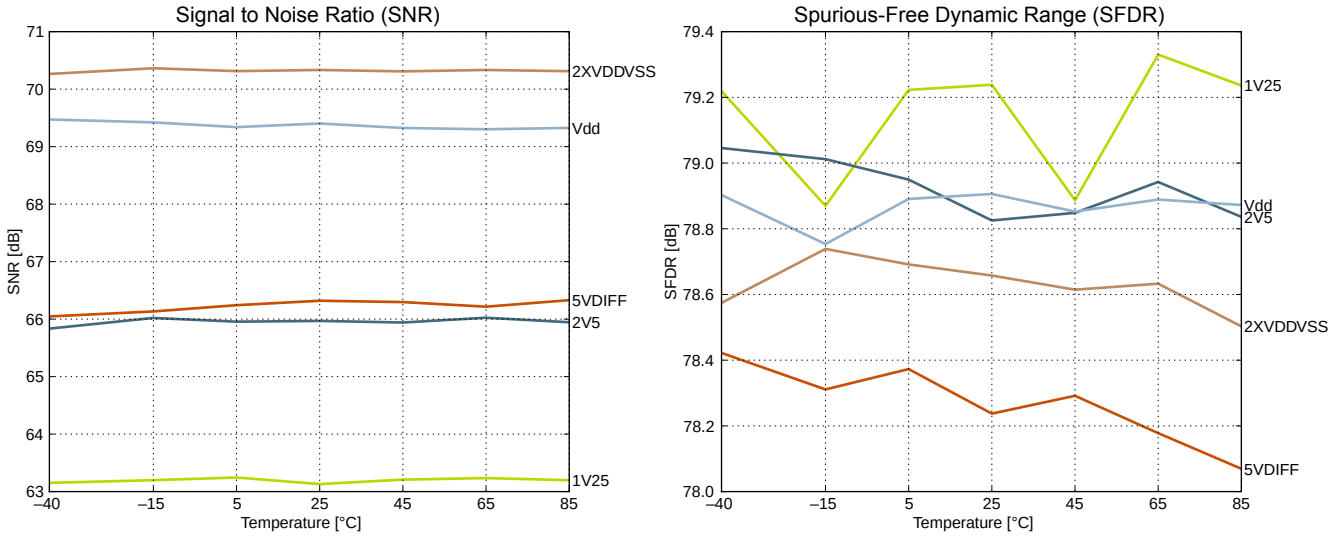


Figure 4.32. ADC Dynamic Performance vs Temperature for all ADC References, VDD = 3 V

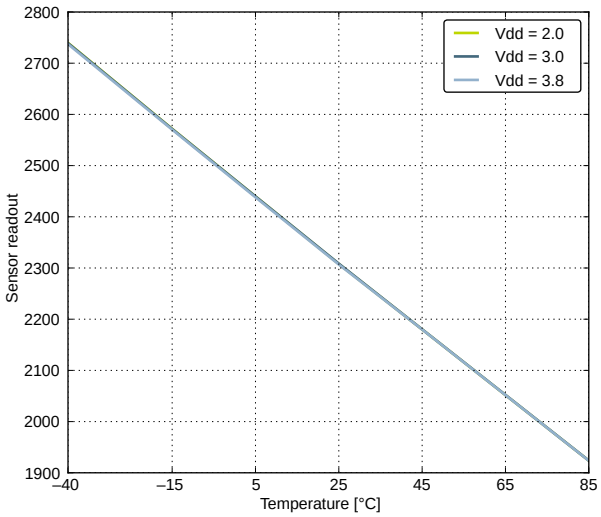


Figure 4.33. ADC Temperature Sensor Readout

4.11 Current Digital Analog Converter (IDAC)

Table 4.15. IDAC Range 0 Source

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Active current with STEP-SEL=0x10	I_{IDAC}	EM0, default settings	—	11.7	—	µA
		Duty-cycled	—	10	—	nA
Nominal IDAC output current with STEPSEL=0x10	I_{0x10}		—	0.84	—	µA
Step size	I_{STEP}		—	0.049	—	µA
Current drop at high impedance load	I_D	V_{IDAC_OUT} = VDD - 100mV	—	0.73	—	%
Temperature coefficient	TC_{IDAC}	VDD = 3.0V, STEPSEL=0x10	—	0.3	—	nA/°C
Voltage coefficient	VC_{IDAC}	T = 25°C, STEPSEL=0x10	—	11.7	—	nA/V

Table 4.16. IDAC Range 0 Sink

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Active current with STEP-SEL=0x10	I_{IDAC}	EM0, default settings	—	13.7	—	µA
Nominal IDAC output current with STEPSEL=0x10	I_{0x10}		—	0.84	—	µA
Step size	I_{STEP}		—	0.050	—	µA
Current drop at high impedance load	I_D	V_{IDAC_OUT} = 200mV	—	0.16	—	%
Temperature coefficient	TC_{IDAC}	VDD = 3.0V, STEPSEL=0x10	—	0.2	—	nA/°C
Voltage coefficient	VC_{IDAC}	T = 25°C, STEPSEL=0x10	—	12.5	—	nA/V

Table 4.17. IDAC Range 1 Source

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Active current with STEP-SEL=0x10	I_{IDAC}	EM0, default settings	—	13.0	—	µA
		Duty-cycled	—	10	—	nA
Nominal IDAC output current with STEPSEL=0x10	I_{0x10}		—	3.17	—	µA
Step size	I_{STEP}		—	0.097	—	µA
Current drop at high impedance load	I_D	V_{IDAC_OUT} = VDD - 100mV	—	0.79	—	%
Temperature coefficient	TC_{IDAC}	VDD = 3.0V, STEPSEL=0x10	—	0.7	—	nA/°C
Voltage coefficient	VC_{IDAC}	T = 25°C, STEPSEL=0x10	—	38.4	—	nA/V

Table 4.18. IDAC Range 1 Sink

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Active current with STEP-SEL=0x10	I_{IDAC}	EM0, default settings	—	17.9	—	µA
Nominal IDAC output current with STEPSEL=0x10	I_{0x10}		—	3.18	—	µA
Step size	I_{STEP}		—	0.098	—	µA
Current drop at high impedance load	I_D	V_{IDAC_OUT} = 200mV	—	0.20	—	%
Temperature coefficient	TC_{IDAC}	VDD = 3.0V, STEPSEL=0x10	—	0.7	—	nA/°C
Voltage coefficient	VC_{IDAC}	T = 25°C, STEPSEL=0x10	—	40.9	—	nA/V

Table 4.19. IDAC Range 2 Source

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Active current with STEP-SEL=0x10	I_{IDAC}	EM0, default settings	—	16.2	—	µA
		Duty-cycled	—	10	—	nA
Nominal IDAC output current with STEPSEL=0x10	I_{0x10}		—	8.40	—	µA
Step size	I_{STEP}		—	0.493	—	µA
Current drop at high impedance load	I_D	V_{IDAC_OUT} = VDD - 100mV	—	1.26	—	%
Temperature coefficient	TC_{IDAC}	VDD = 3.0V, STEPSEL=0x10	—	2.8	—	nA/°C
Voltage coefficient	VC_{IDAC}	T = 25°C, STEPSEL=0x10	—	96.6	—	nA/V

Table 4.20. IDAC Range 2 Sink

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Active current with STEP-SEL=0x10	I_{IDAC}	EM0, default settings	—	28.4	—	µA
Nominal IDAC output current with STEPSEL=0x10	I_{0x10}		—	8.44	—	µA
Step size	I_{STEP}		—	0.495	—	µA
Current drop at high impedance load	I_D	V_{IDAC_OUT} = 200mV	—	0.55	—	%
Temperature coefficient	TC_{IDAC}	VDD = 3.0V, STEPSEL=0x10	—	2.8	—	nA/°C
Voltage coefficient	VC_{IDAC}	T = 25°C, STEPSEL=0x10	—	94.4	—	nA/V

Table 4.21. IDAC Range 3 Source

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Active current with STEP-SEL=0x10	I_{IDAC}	EM0, default settings	—	18.3	—	µA
		Duty-cycled	—	10	—	nA
Nominal IDAC output current with STEPSEL=0x10	I_{0x10}		—	34.03	—	µA
Step size	I_{STEP}		—	1.996	—	µA
Current drop at high impedance load	I_D	V_{IDAC_OUT} = VDD - 100mV	—	3.18	—	%
Temperature coefficient	TC_{IDAC}	VDD = 3.0V, STEPSEL=0x10	—	10.9	—	nA/°C
Voltage coefficient	VC_{IDAC}	T = 25°C, STEPSEL=0x10	—	159.5	—	nA/V

Table 4.22. IDAC Range 3 Sink

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Active current with STEP-SEL=0x10	I_{IDAC}	EM0, default settings	—	62.9	—	µA
Nominal IDAC output current with STEPSEL=0x10	I_{0x10}		—	34.16	—	µA
Step size	I_{STEP}		—	2.003	—	µA
Current drop at high impedance load	I_D	V_{IDAC_OUT} = 200mV	—	1.65	—	%
Temperature coefficient	TC_{IDAC}	VDD = 3.0V, STEPSEL=0x10	—	10.9	—	nA/°C
Voltage coefficient	VC_{IDAC}	T = 25°C, STEPSEL=0x10	—	148.6	—	nA/V

Table 4.23. IDAC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Start-up time, from enabled to output settled	$t_{IDAC-START}$		—	40	—	µs

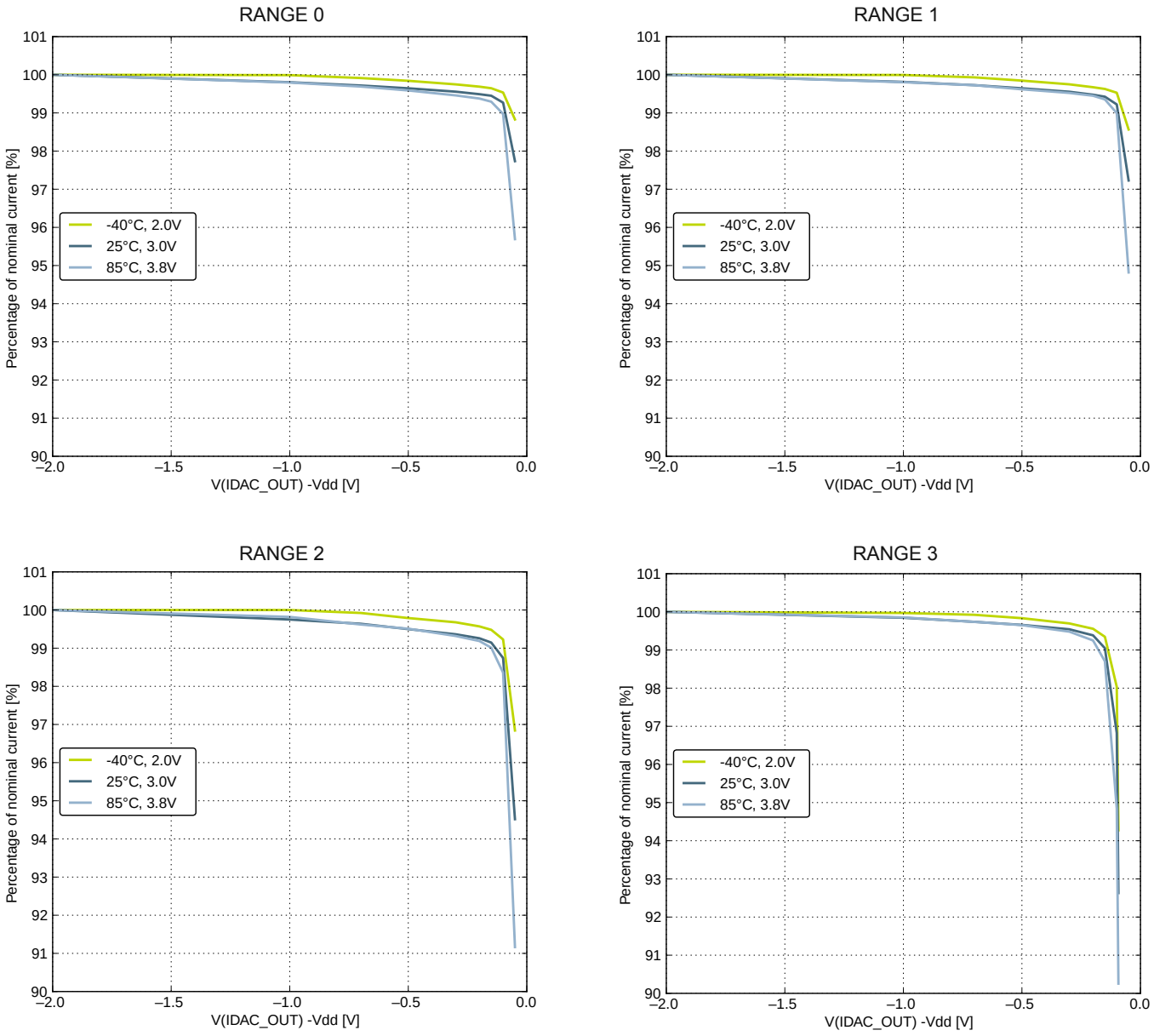


Figure 4.34. IDAC Source Current as a function of voltage on IDAC_OUT

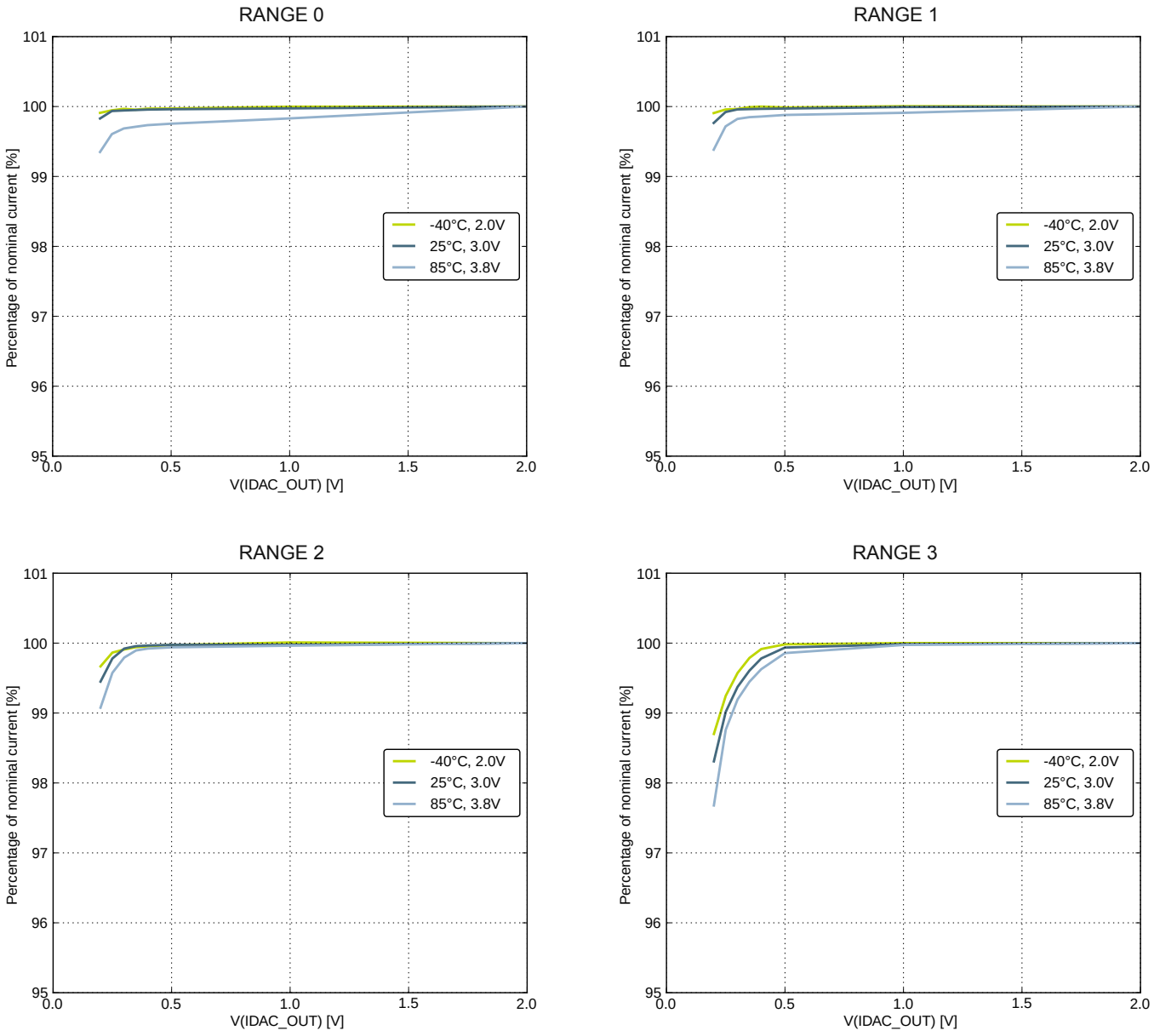


Figure 4.35. IDAC Sink Current as a function of voltage on IDAC_OUT

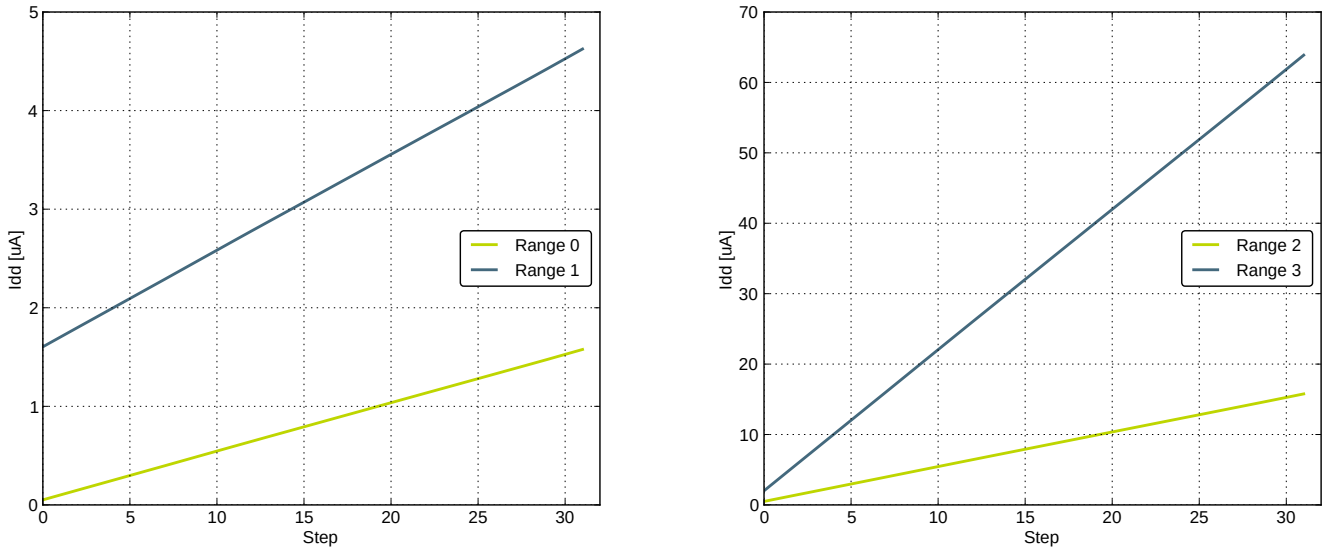


Figure 4.36. IDAC Linearity

4.12 Analog Comparator (ACMP)

Table 4.24. ACMP

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input voltage range	V_{ACMPIN}		0	—	V_{DD}	V
ACMP Common Mode voltage range	V_{ACMPCM}		0	—	V_{DD}	V
Active current	I_{ACMP}	BIASPROG=0b0000, FULLBIAS=0 and HALFBIAS=1 in ACMPn_CTRL register	—	0.1	0.4	µA
		BIASPROG=0b1111, FULLBIAS= 0 and HALFBIAS=0 in ACMPn_CTRL register	—	2.87	15	µA
		BIASPROG=0b1111, FULLBIAS= 1 and HALFBIAS=0 in ACMPn_CTRL register	—	195	520	µA
Current consumption of internal voltage reference	$I_{ACMPREF}$	Internal voltage reference off. Using external voltage reference	—	0	—	µA
		Internal voltage reference	—	5	—	µA
Offset voltage	$V_{ACMPOFFSET}$	BIASPROG= 0b1010, FULLBIAS=0 and HALFBIAS=0 in ACMPn_CTRL register	-12	0	12	mV
ACMP hysteresis	$V_{ACMPHYST}$	Programmable	—	17	—	mV
Capacitive Sense Internal Resistance	R_{CSRES}	CSRESSEL=0b00 in ACMPn_INPUTSEL	—	39	—	kΩ
		CSRESSEL=0b01 in ACMPn_INPUTSEL	—	71	—	kΩ
		CSRESSEL=0b10 in ACMPn_INPUTSEL	—	104	—	kΩ
		CSRESSEL=0b11 in ACMPn_INPUTSEL	—	136	—	kΩ
Startup time	$t_{ACMPSTART}$		—	—	10	µs

The total ACMP current is the sum of the contributions from the ACMP and its internal voltage reference as given in in the following equation. $I_{ACMPREF}$ is zero if an external voltage reference is used.

$$I_{ACMPTOTAL} = I_{ACMP} + I_{ACMPREF}$$

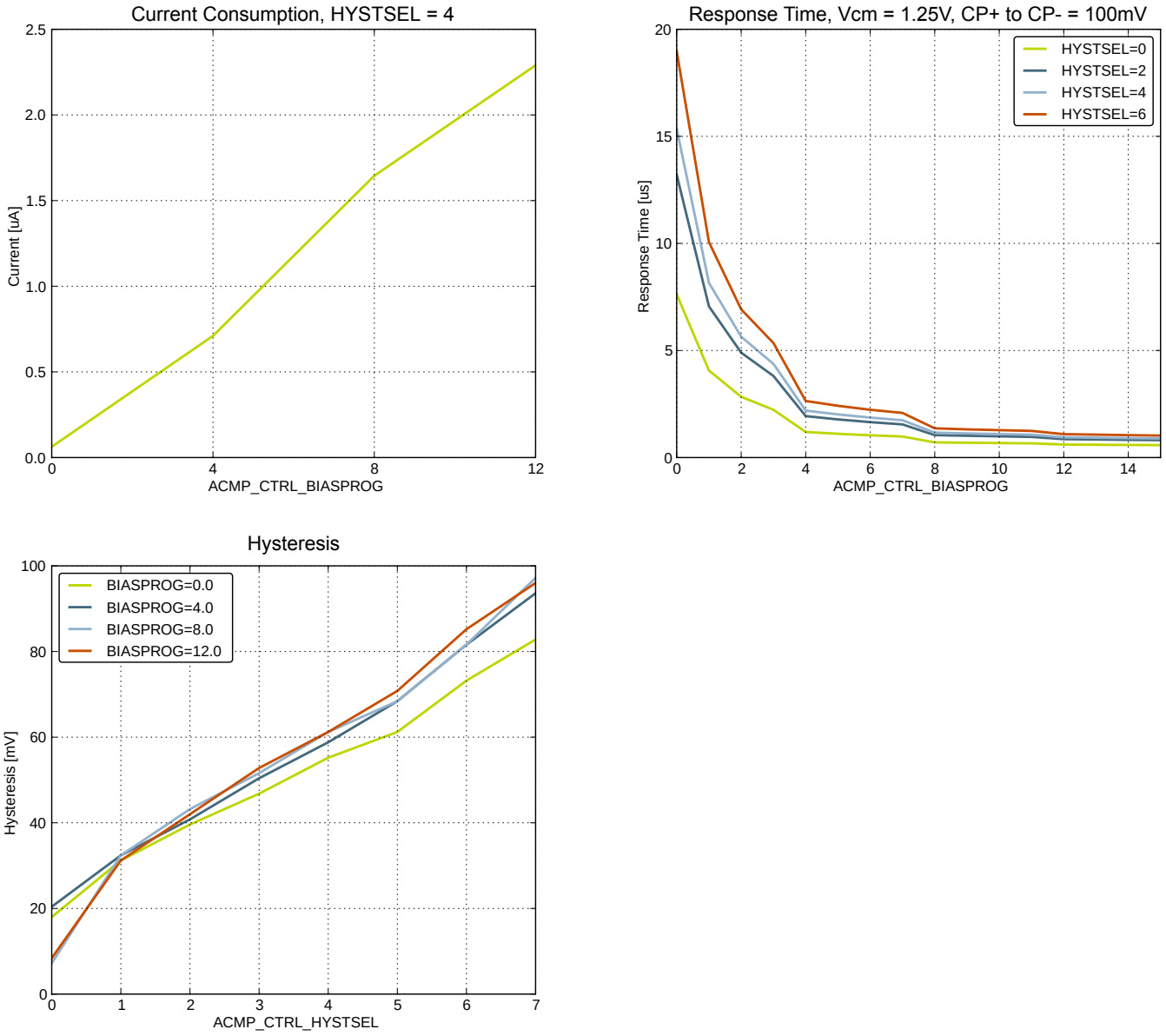


Figure 4.37. ACMP Characteristics, Vdd = 3 V, Temp = 25 °C, FULLBIAS = 0, HALFBIAS = 1

4.13 Voltage Comparator (VCMP)

Table 4.25. VCMP

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input voltage range	V_{VCMPIN}		—	V_{DD}	—	V
VCMP Common Mode voltage range	V_{VCMPCM}		—	V_{DD}	—	V
Active current	I_{VCMP}	BIASPROG=0b0000 and HALFBIAS=1 in VCMPn_CTRL register	—	0.1	0.8	µA
		BIASPROG=0b1111 and HALFBIAS=0 in VCMPn_CTRL register. LPREF=0.	—	14.7	35	µA
Startup time reference generator	$t_{VCMPREF}$	NORMAL	—	10	—	µs
Offset voltage	$V_{VCMPOFFSET}$	Single-ended	—	10	—	mV
		Differential	—	10	—	mV
VCMP hysteresis	$V_{VCMPHYST}$		—	17	—	mV
Startup time	$t_{VCMPSTART}$		—	—	10	µs

The V_{DD} trigger level can be configured by setting the TRIGLEVEL field of the VCMP_CTRL register in accordance with the following equation:

$$V_{\text{DD Trigger Level}} = 1.667V + 0.034 \times \text{TRIGLEVEL}$$

4.14 I2C

Table 4.26. I2C Standard-mode (Sm)

Parameter	Symbol	Min	Typ	Max	Unit
SCL clock frequency	f_{SCL}	0	—	100[1]	kHz
SCL clock low time	t_{LOW}	4.7	—	—	µs
SCL clock high time	t_{HIGH}	4.0	—	—	µs
SDA set-up time	$t_{SU,DAT}$	250	—	—	ns
SDA hold time	$t_{HD,DAT}$	8	—	3450[2,3]	ns
Repeated START condition set-up time	$t_{SU,STA}$	4.7	—	—	µs
(Repeated) START condition hold time	$t_{HD,STA}$	4.0	—	—	µs
STOP condition set-up time	$t_{SU,STO}$	4.0	—	—	µs
Bus free time between a STOP and a START condition	t_{BUF}	4.7	—	—	µs

Note:
1. For the minimum HFPERCLK frequency required in Standard-mode, see the I2C chapter in the EFM32ZG Reference Manual.
2. The maximum SDA hold time ($t_{HD,DAT}$) needs to be met only when the device does not stretch the low time of SCL (t_{LOW}).
3. When transmitting data, this number is guaranteed only when I2Cn_CLKDIV < ((3450*10^{-9} [s] * $f_{HFPERCLK}$ [Hz]) - 5).

Table 4.27. I2C Fast-mode (Fm)

Parameter	Symbol	Min	Typ	Max	Unit
SCL clock frequency	f_{SCL}	0	—	400[1]	kHz
SCL clock low time	t_{LOW}	1.3	—	—	µs
SCL clock high time	t_{HIGH}	0.6	—	—	µs
SDA set-up time	$t_{SU,DAT}$	100	—	—	ns
SDA hold time	$t_{HD,DAT}$	8	—	900[2,3]	ns
Repeated START condition set-up time	$t_{SU,STA}$	0.6	—	—	µs
(Repeated) START condition hold time	$t_{HD,STA}$	0.6	—	—	µs
STOP condition set-up time	$t_{SU,STO}$	0.6	—	—	µs
Bus free time between a STOP and a START condition	t_{BUF}	1.3	—	—	µs

Note:
1. For the minimum HFPERCLK frequency required in Fast-mode, see the I2C chapter in the EFM32ZG Reference Manual.
2. The maximum SDA hold time ($t_{HD,DAT}$) needs to be met only when the device does not stretch the low time of SCL (t_{LOW}).
3. When transmitting data, this number is guaranteed only when I2Cn_CLKDIV < ((900*10^{-9} [s] * $f_{HFPERCLK}$ [Hz]) - 5).

Table 4.28. I2C Fast-mode Plus (Fm+)

Parameter	Symbol	Min	Typ	Max	Unit
SCL clock frequency	f_{SCL}	0	—	1000[1]	kHz
SCL clock low time	t_{LOW}	0.5	—	—	µs
SCL clock high time	t_{HIGH}	0.26	—	—	µs
SDA set-up time	$t_{SU,DAT}$	50	—	—	ns
SDA hold time	$t_{HD,DAT}$	8	—	—	ns
Repeated START condition set-up time	$t_{SU,STA}$	0.26	—	—	µs
(Repeated) START condition hold time	$t_{HD,STA}$	0.26	—	—	µs
STOP condition set-up time	$t_{SU,STO}$	0.26	—	—	µs
Bus free time between a STOP and a START condition	t_{BUF}	0.5	—	—	µs

Note:
1. For the minimum HFPERCLK frequency required in Fast-mode Plus, see the I2C chapter in the EFM32ZG Reference Manual.

4.15 Digital Peripherals

Table 4.29. Digital Peripherals

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
USART current	I_{USART}	USART idle current, clock enabled	—	7.5	—	µA/MHz
LEUART current	I_{LEUART}	LEUART idle current, clock enabled	—	150	—	nA
I2C current	I_{I2C}	I2C idle current, clock enabled	—	6.25	—	µA/MHz
TIMER current	I_{TIMER}	TIMER_0 idle current, clock enabled	—	8.75	—	µA/MHz
PCNT current	I_{PCNT}	PCNT idle current, clock enabled	—	100	—	nA
RTC current	I_{RTC}	RTC idle current, clock enabled	—	100	—	nA
AES current	I_{AES}	AES idle current, clock enabled	—	2.5	—	µA/MHz
GPIO current	I_{GPIO}	GPIO idle current, clock enabled	—	5.31	—	µA/MHz
PRS current	I_{PRS}	PRS idle current	—	2.81	—	µA/MHz
DMA current	I_{DMA}	Clock enable	—	8.12	—	µA/MHz

5. Pin Definitions

Note: Please refer to the application note *AN0002 EFM32 Hardware Design Considerations* for guidelines on designing Printed Circuit Boards (PCBs) for the EFM32ZG.

5.1 EFM32ZG108 (QFN24)

5.1.1 Pinout

The EFM32ZG108 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

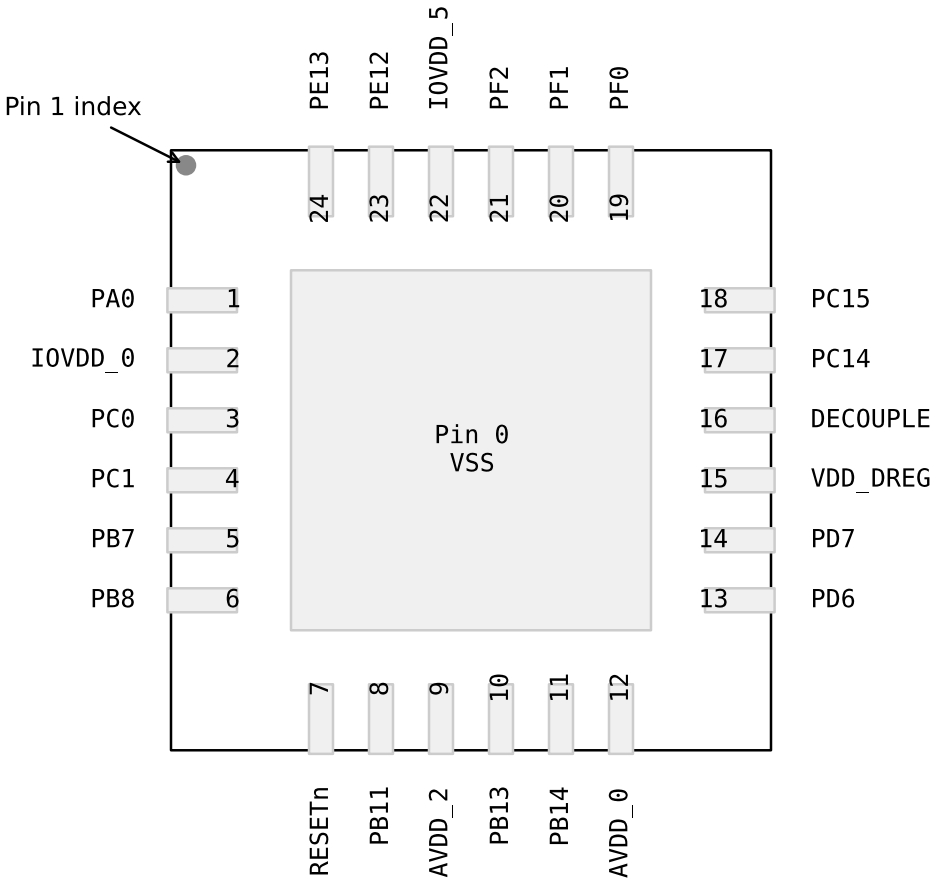


Figure 5.1. EFM32ZG108 Pinout (top view, not to scale)

Table 5.1. Device Pinout

QFN24 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
0	VSS	Ground.			
1	PA0		TIM0_CC0 #0/1/4	LEU0_RX #4 I2C0_SDA #0	PRS_CH0 #0 GPIO_EM4WU0
2	IOVDD_0	Digital IO power supply 0.			
3	PC0	ACMP0_CH0	TIM0_CC1 #4 PCNT0_S0IN #2	US1_TX #0 I2C0_SDA #4	PRS_CH2 #0
4	PC1	ACMP0_CH1	TIM0_CC2 #4 PCNT0_S1IN #2	US1_RX #0 I2C0_SCL #4	PRS_CH3 #0
5	PB7	LFXTAL_P	TIM1_CC0 #3	US1_CLK #0	
6	PB8	LFXTAL_N	TIM1_CC1 #3	US1_CS #0	
7	RESETn	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.			
8	PB11		TIM1_CC2 #3		
9	AVDD_2	Analog power supply 2.			
10	PB13	HFXTAL_P		LEU0_TX #1	
11	PB14	HFXTAL_N		LEU0_RX #1	
12	AVDD_0	Analog power supply 0.			
13	PD6		TIM1_CC0 #4 PCNT0_S0IN #3	US1_RX #2/3 I2C0_SDA #1	ACMP0_O #2
14	PD7		TIM1_CC1 #4 PCNT0_S1IN #3	US1_TX #2/3 I2C0_SCL #1	CMU_CLK0 #2
15	VDD_DREG	Power supply for on-chip voltage regulator.			
16	DECOUPLE	Decouple output for on-chip voltage regulator. An external capacitance of size $C_{DECOUPLE}$ is required at this pin.			
17	PC14		TIM1_CC1 #0 PCNT0_S1IN #0	US1_CS #3	PRS_CH0 #2
18	PC15		TIM1_CC2 #0	US1_CLK #3	PRS_CH1 #2
19	PF0		TIM0_CC0 #5	US1_CLK #2 LEU0_TX #3 I2C0_SDA #5	DBG_SWCLK #0 BOOT_TX
20	PF1		TIM0_CC1 #5	US1_CS #2 LEU0_RX #3 I2C0_SCL #5	DBG_SWDIO #0 GPIO_EM4WU3 BOOT_RX
21	PF2		TIM0_CC2 #5	LEU0_TX #4	GPIO_EM4WU4

QFN24 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
22	IOVDD_5	Digital IO power supply 5.			
23	PE12		TIM1_CC2 #1	I2C0_SDA #6	CMU_CLK1 #2
24	PE13			I2C0_SCL #6	ACMP0_O #0 GPIO_EM4WU5

5.1.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

Note: Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 5.2. Alternate functionality overview

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
ACMP0_CH0	PC0							Analog comparator ACMP0, channel 0.
ACMP0_CH1	PC1							Analog comparator ACMP0, channel 1.
ACMP0_O	PE13		PD6					Analog comparator ACMP0, digital output.
BOOT_RX	PF1							Bootloader RX.
BOOT_TX	PF0							Bootloader TX.
CMU_CLK0			PD7					Clock Management Unit, clock output number 0.
CMU_CLK1			PE12					Clock Management Unit, clock output number 1.
DBG_SWCLK	PF0							Debug-interface Serial Wire clock input. Note that this function is enabled to pin out of reset, and has a built-in pull down.
DBG_SWDIO	PF1							Debug-interface Serial Wire data input / output. Note that this function is enabled to pin out of reset, and has a built-in pull up.
GPIO_EM4WU0	PA0							Pin can be used to wake the system up from EM4
GPIO_EM4WU3	PF1							Pin can be used to wake the system up from EM4
GPIO_EM4WU4	PF2							Pin can be used to wake the system up from EM4
GPIO_EM4WU5	PE13							Pin can be used to wake the system up from EM4
HFXTAL_N	PB14							High Frequency Crystal negative pin. Also used as external optional clock input pin.
HFXTAL_P	PB13							High Frequency Crystal positive pin.
I2C0_SCL		PD7			PC1	PF1	PE13	I2C0 Serial Clock Line input / output.
I2C0_SDA	PA0	PD6			PC0	PF0	PE12	I2C0 Serial Data input / output.
LEU0_RX		PB14		PF1	PA0			LEUART0 Receive input.
LEU0_TX		PB13		PF0	PF2			LEUART0 Transmit output. Also used as receive input in half duplex communication.
LFXTAL_N	PB8							Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin.
LFXTAL_P	PB7							Low Frequency Crystal (typically 32.768 kHz) positive pin.
PCNT0_S0IN			PC0	PD6				Pulse Counter PCNT0 input number 0.
PCNT0_S1IN	PC14		PC1	PD7				Pulse Counter PCNT0 input number 1.

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
PRS_CH0	PA0		PC14					Peripheral Reflex System PRS, channel 0.
PRS_CH1			PC15					Peripheral Reflex System PRS, channel 1.
PRS_CH2	PC0							Peripheral Reflex System PRS, channel 2.
PRS_CH3	PC1							Peripheral Reflex System PRS, channel 3.
TIM0_CC0	PA0	PA0			PA0	PF0		Timer 0 Capture Compare input / output channel 0.
TIM0_CC1					PC0	PF1		Timer 0 Capture Compare input / output channel 1.
TIM0_CC2					PC1	PF2		Timer 0 Capture Compare input / output channel 2.
TIM1_CC0				PB7	PD6			Timer 1 Capture Compare input / output channel 0.
TIM1_CC1	PC14			PB8	PD7			Timer 1 Capture Compare input / output channel 1.
TIM1_CC2	PC15	PE12		PB11				Timer 1 Capture Compare input / output channel 2.
US1_CLK	PB7		PF0	PC15				USART1 clock input / output.
US1_CS	PB8		PF1	PC14				USART1 chip select input / output.
US1_RX	PC1		PD6	PD6				USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO).
US1_TX	PC0		PD7	PD7				USART1 Asynchronous Transmit.Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI).

5.1.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32ZG110 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

Table 5.3. GPIO Pinout

Port	Pin 15	Pin 14	Pin 13	Pin 12	Pin 11	Pin 10	Pin 9	Pin 8	Pin 7	Pin 6	Pin 5	Pin 4	Pin 3	Pin 2	Pin 1	Pin 0
Port A	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	PA0
Port B	-	PB14	PB13	-	PB11	-	-	PB8	PB7	-	-	-	-	-	-	-
Port C	PC15	PC14	-	-	-	-	-	-	-	-	-	-	-	-	PC1	PC0
Port D	-	-	-	-	-	-	-	-	PD7	PD6	-	-	-	-	-	-
Port E	-	-	PE13	PE12	-	-	-	-	-	-	-	-	-	-	-	-
Port F	-	-	-	-	-	-	-	-	-	-	-	-	-	PF2	PF1	PF0

5.2 EFM32ZG110 (QFN24)

5.2.1 Pinout

The EFM32ZG110 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

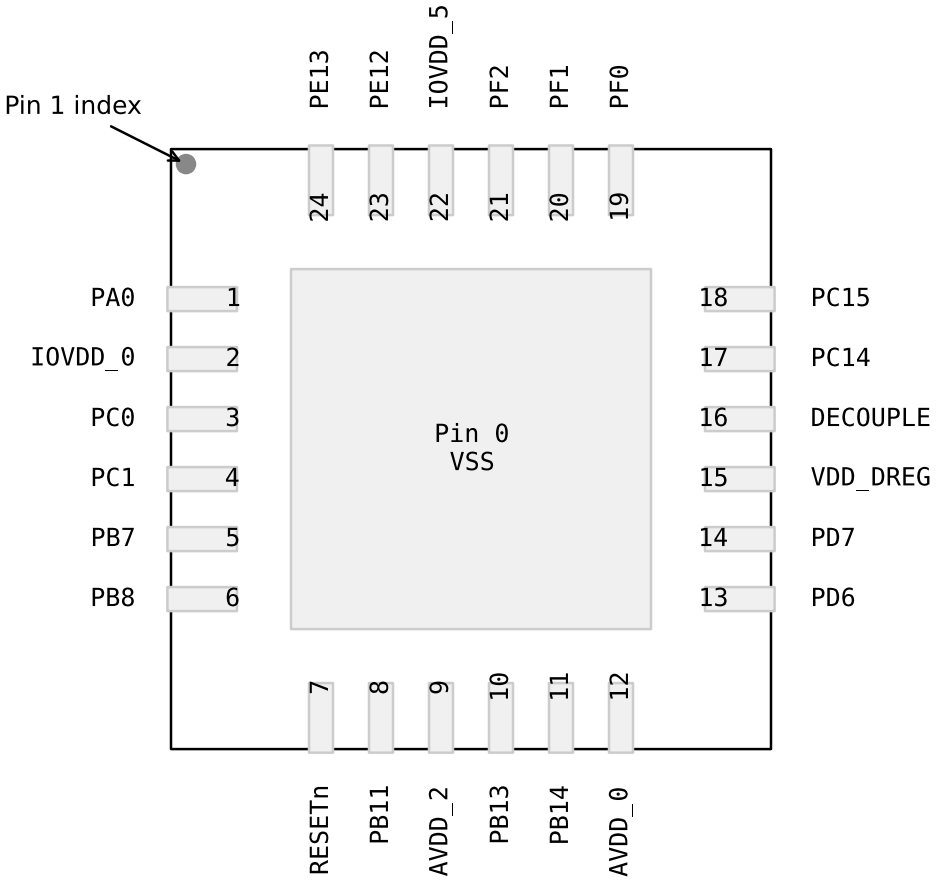


Figure 5.2. EFM32ZG110 Pinout (top view, not to scale)

Table 5.4. Device Pinout

QFN24 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
0	VSS	Ground.			
1	PA0		TIM0_CC0 #0/1/4	LEU0_RX #4 I2C0_SDA #0	PRS_CH0 #0 GPIO_EM4WU0
2	IOVDD_0	Digital IO power supply 0.			
3	PC0	ACMP0_CH0	TIM0_CC1 #4 PCNT0_S0IN #2	US1_TX #0 I2C0_SDA #4	PRS_CH2 #0

QFN24 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
4	PC1	ACMP0_CH1	TIM0_CC2 #4 PCNT0_S1IN #2	US1_RX #0 I2C0_SCL #4	PRS_CH3 #0
5	PB7	LFXTAL_P	TIM1_CC0 #3	US1_CLK #0	
6	PB8	LFXTAL_N	TIM1_CC1 #3	US1_CS #0	
7	RESETn	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.			
8	PB11	IDAC0_OUT	TIM1_CC2 #3		
9	AVDD_2	Analog power supply 2.			
10	PB13	HFXTAL_P		LEU0_TX #1	
11	PB14	HFXTAL_N		LEU0_RX #1	
12	AVDD_0	Analog power supply 0.			
13	PD6	ADC0_CH6	TIM1_CC0 #4 PCNT0_S0IN #3	US1_RX #2/3 I2C0_SDA #1	ACMP0_O #2
14	PD7	ADC0_CH7	TIM1_CC1 #4 PCNT0_S1IN #3	US1_TX #2/3 I2C0_SCL #1	CMU_CLK0 #2
15	VDD_DREG	Power supply for on-chip voltage regulator.			
16	DECOUPLE	Decouple output for on-chip voltage regulator. An external capacitance of size $C_{DECOUPLE}$ is required at this pin.			
17	PC14		TIM1_CC1 #0 PCNT0_S1IN #0	US1_CS #3	PRS_CH0 #2
18	PC15		TIM1_CC2 #0	US1_CLK #3	PRS_CH1 #2
19	PF0		TIM0_CC0 #5	US1_CLK #2 LEU0_TX #3 I2C0_SDA #5	DBG_SWCLK #0 BOOT_TX
20	PF1		TIM0_CC1 #5	US1_CS #2 LEU0_RX #3 I2C0_SCL #5	DBG_SWDIO #0 GPIO_EM4WU3 BOOT_RX
21	PF2		TIM0_CC2 #5	LEU0_TX #4	GPIO_EM4WU4
22	IOVDD_5	Digital IO power supply 5.			
23	PE12		TIM1_CC2 #1	I2C0_SDA #6	CMU_CLK1 #2
24	PE13			I2C0_SCL #6	ACMP0_O #0 GPIO_EM4WU5

5.2.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

Note: Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 5.5. Alternate functionality overview

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
ACMP0_CH0	PC0							Analog comparator ACMP0, channel 0.
ACMP0_CH1	PC1							Analog comparator ACMP0, channel 1.
ACMP0_O	PE13		PD6					Analog comparator ACMP0, digital output.
ADC0_CH6	PD6							Analog to digital converter ADC0, input channel number 6.
ADC0_CH7	PD7							Analog to digital converter ADC0, input channel number 7.
BOOT_RX	PF1							Bootloader RX.
BOOT_TX	PF0							Bootloader TX.
CMU_CLK0			PD7					Clock Management Unit, clock output number 0.
CMU_CLK1			PE12					Clock Management Unit, clock output number 1.
DBG_SWCLK	PF0							Debug-interface Serial Wire clock input. Note that this function is enabled to pin out of reset, and has a built-in pull down.
DBG_SWDIO	PF1							Debug-interface Serial Wire data input / output. Note that this function is enabled to pin out of reset, and has a built-in pull up.
GPIO_EM4WU0	PA0							Pin can be used to wake the system up from EM4
GPIO_EM4WU3	PF1							Pin can be used to wake the system up from EM4
GPIO_EM4WU4	PF2							Pin can be used to wake the system up from EM4
GPIO_EM4WU5	PE13							Pin can be used to wake the system up from EM4
HFXTAL_N	PB14							High Frequency Crystal negative pin. Also used as external optional clock input pin.
HFXTAL_P	PB13							High Frequency Crystal positive pin.
I2C0_SCL		PD7			PC1	PF1	PE13	I2C0 Serial Clock Line input / output.
I2C0_SDA	PA0	PD6			PC0	PF0	PE12	I2C0 Serial Data input / output.
IDAC0_OUT	PB11							IDAC0 output.
LEU0_RX		PB14		PF1	PA0			LEUART0 Receive input.
LEU0_TX		PB13		PF0	PF2			LEUART0 Transmit output. Also used as receive input in half duplex communication.
LFXTAL_N	PB8							Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin.

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
LFXTAL_P	PB7							Low Frequency Crystal (typically 32.768 kHz) positive pin.
PCNT0_S0IN			PC0	PD6				Pulse Counter PCNT0 input number 0.
PCNT0_S1IN	PC14		PC1	PD7				Pulse Counter PCNT0 input number 1.
PRS_CH0	PA0		PC14					Peripheral Reflex System PRS, channel 0.
PRS_CH1			PC15					Peripheral Reflex System PRS, channel 1.
PRS_CH2	PC0							Peripheral Reflex System PRS, channel 2.
PRS_CH3	PC1							Peripheral Reflex System PRS, channel 3.
TIM0_CC0	PA0	PA0			PA0	PF0		Timer 0 Capture Compare input / output channel 0.
TIM0_CC1					PC0	PF1		Timer 0 Capture Compare input / output channel 1.
TIM0_CC2					PC1	PF2		Timer 0 Capture Compare input / output channel 2.
TIM1_CC0				PB7	PD6			Timer 1 Capture Compare input / output channel 0.
TIM1_CC1	PC14			PB8	PD7			Timer 1 Capture Compare input / output channel 1.
TIM1_CC2	PC15	PE12		PB11				Timer 1 Capture Compare input / output channel 2.
US1_CLK	PB7		PF0	PC15				USART1 clock input / output.
US1_CS	PB8		PF1	PC14				USART1 chip select input / output.
US1_RX	PC1		PD6	PD6				USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO).
US1_TX	PC0		PD7	PD7				USART1 Asynchronous Transmit.Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI).

5.2.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32ZG110 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

Table 5.6. GPIO Pinout

Port	Pin 15	Pin 14	Pin 13	Pin 12	Pin 11	Pin 10	Pin 9	Pin 8	Pin 7	Pin 6	Pin 5	Pin 4	Pin 3	Pin 2	Pin 1	Pin 0
Port A	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	PA0
Port B	-	PB14	PB13	-	PB11	-	-	PB8	PB7	-	-	-	-	-	-	-
Port C	PC15	PC14	-	-	-	-	-	-	-	-	-	-	-	-	PC1	PC0
Port D	-	-	-	-	-	-	-	-	PD7	PD6	-	-	-	-	-	-
Port E	-	-	PE13	PE12	-	-	-	-	-	-	-	-	-	-	-	-
Port F	-	-	-	-	-	-	-	-	-	-	-	-	-	PF2	PF1	PF0

5.3 EFM32ZG210 (QFN32)

5.3.1 Pinout

The EFM32ZG210 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

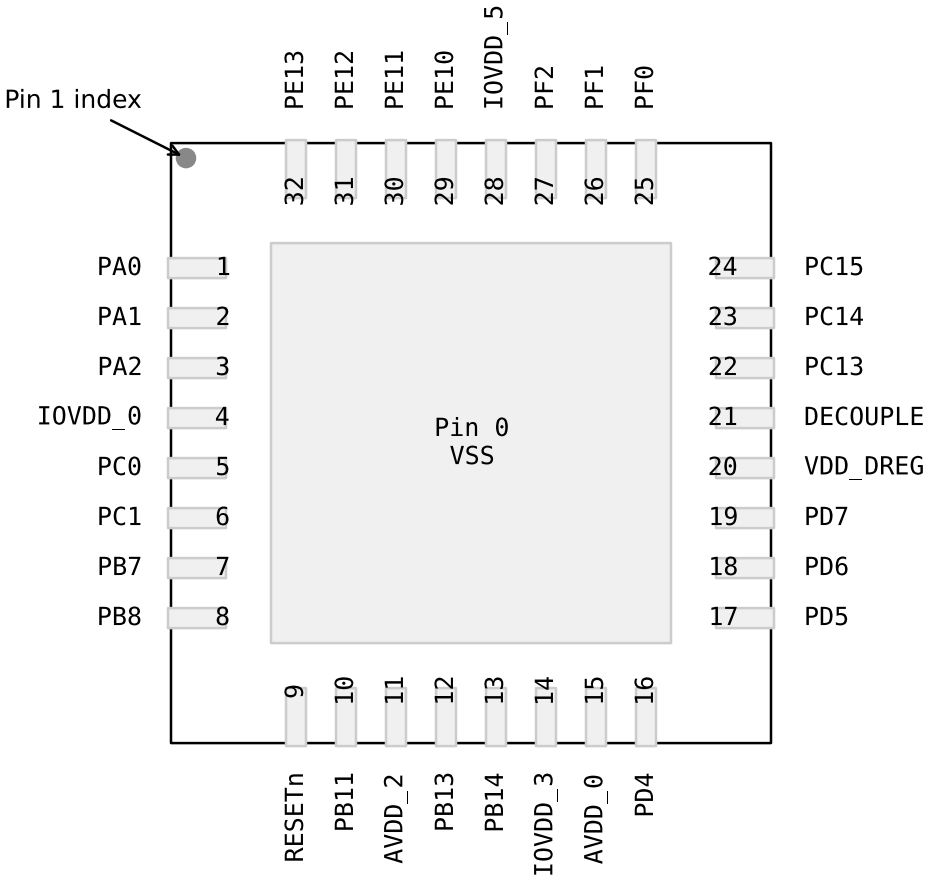


Figure 5.3. EFM32ZG210 Pinout (top view, not to scale)

Table 5.7. Device Pinout

QFN32 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
0	VSS	Ground.			
1	PA0		TIM0_CC0 #0/1/4	LEU0_RX #4 I2C0_SDA #0	PRS_CH0 #0 GPIO_EM4WU0
2	PA1		TIM0_CC1 #0/1	I2C0_SCL #0	CMU_CLK1 #0 PRS_CH1 #0
3	PA2		TIM0_CC2 #0/1		CMU_CLK0 #0

QFN32 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
4	IOVDD_0	Digital IO power supply 0.			
5	PC0	ACMP0_CH0	TIM0_CC1 #4 PCNT0_S0IN #2	US1_TX #0 I2C0_SDA #4	PRS_CH2 #0
6	PC1	ACMP0_CH1	TIM0_CC2 #4 PCNT0_S1IN #2	US1_RX #0 I2C0_SCL #4	PRS_CH3 #0
7	PB7	LFXTAL_P	TIM1_CC0 #3	US1_CLK #0	
8	PB8	LFXTAL_N	TIM1_CC1 #3	US1_CS #0	
9	RESETn	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.			
10	PB11	IDAC0_OUT	TIM1_CC2 #3		
11	AVDD_2	Analog power supply 2.			
12	PB13	HFXTAL_P		LEU0_TX #1	
13	PB14	HFXTAL_N		LEU0_RX #1	
14	IOVDD_3	Digital IO power supply 3.			
15	AVDD_0	Analog power supply 0.			
16	PD4	ADC0_CH4		LEU0_TX #0	
17	PD5	ADC0_CH5		LEU0_RX #0	
18	PD6	ADC0_CH6	TIM1_CC0 #4 PCNT0_S0IN #3	US1_RX #2/3 I2C0_SDA #1	ACMP0_O #2
19	PD7	ADC0_CH7	TIM1_CC1 #4 PCNT0_S1IN #3	US1_TX #2/3 I2C0_SCL #1	CMU_CLK0 #2
20	VDD_DREG	Power supply for on-chip voltage regulator.			
21	DECOUPLE	Decouple output for on-chip voltage regulator. An external capacitance of size $C_{DECOUPLE}$ is required at this pin.			
22	PC13		TIM1_CC0 #0 TIM1_CC2 #4 PCNT0_S0IN #0		
23	PC14		TIM1_CC1 #0 PCNT0_S1IN #0	US1_CS #3	PRS_CH0 #2
24	PC15		TIM1_CC2 #0	US1_CLK #3	PRS_CH1 #2
25	PF0		TIM0_CC0 #5	US1_CLK #2 LEU0_TX #3 I2C0_SDA #5	DBG_SWCLK #0 BOOT_TX
26	PF1		TIM0_CC1 #5	US1_CS #2 LEU0_RX #3 I2C0_SCL #5	DBG_SWDIO #0 GPIO_EM4WU3 BOOT_RX
27	PF2		TIM0_CC2 #5	LEU0_TX #4	GPIO_EM4WU4

QFN32 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
28	IOVDD_5	Digital IO power supply 5.			
29	PE10		TIM1_CC0 #1		PRS_CH2 #2
30	PE11		TIM1_CC1 #1		PRS_CH3 #2
31	PE12		TIM1_CC2 #1	I2C0_SDA #6	CMU_CLK1 #2
32	PE13			I2C0_SCL #6	ACMP0_O #0 GPIO_EM4WU5

5.3.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

Note: Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 5.8. Alternate functionality overview

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
ACMP0_CH0	PC0							Analog comparator ACMP0, channel 0.
ACMP0_CH1	PC1							Analog comparator ACMP0, channel 1.
ACMP0_O	PE13		PD6					Analog comparator ACMP0, digital output.
ADC0_CH4	PD4							Analog to digital converter ADC0, input channel number 4.
ADC0_CH5	PD5							Analog to digital converter ADC0, input channel number 5.
ADC0_CH6	PD6							Analog to digital converter ADC0, input channel number 6.
ADC0_CH7	PD7							Analog to digital converter ADC0, input channel number 7.
BOOT_RX	PF1							Bootloader RX.
BOOT_TX	PF0							Bootloader TX.
CMU_CLK0	PA2		PD7					Clock Management Unit, clock output number 0.
CMU_CLK1	PA1		PE12					Clock Management Unit, clock output number 1.
DBG_SWCLK	PF0							Debug-interface Serial Wire clock input. Note that this function is enabled to pin out of reset, and has a built-in pull down.
DBG_SWDIO	PF1							Debug-interface Serial Wire data input / output. Note that this function is enabled to pin out of reset, and has a built-in pull up.
GPIO_EM4WU0	PA0							Pin can be used to wake the system up from EM4
GPIO_EM4WU3	PF1							Pin can be used to wake the system up from EM4
GPIO_EM4WU4	PF2							Pin can be used to wake the system up from EM4
GPIO_EM4WU5	PE13							Pin can be used to wake the system up from EM4
HFXTAL_N	PB14							High Frequency Crystal negative pin. Also used as external optional clock input pin.
HFXTAL_P	PB13							High Frequency Crystal positive pin.
I2C0_SCL	PA1	PD7			PC1	PF1	PE13	I2C0 Serial Clock Line input / output.
I2C0_SDA	PA0	PD6			PC0	PF0	PE12	I2C0 Serial Data input / output.
IDAC0_OUT	PB11							IDAC0 output.
LEU0_RX	PD5	PB14		PF1	PA0			LEUART0 Receive input.

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
LEU0_TX	PD4	PB13		PF0	PF2			LEUART0 Transmit output. Also used as receive input in half duplex communication.
LFXTAL_N	PB8							Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin.
LFXTAL_P	PB7							Low Frequency Crystal (typically 32.768 kHz) positive pin.
PCNT0_S0IN	PC13		PC0	PD6				Pulse Counter PCNT0 input number 0.
PCNT0_S1IN	PC14		PC1	PD7				Pulse Counter PCNT0 input number 1.
PRS_CH0	PA0		PC14					Peripheral Reflex System PRS, channel 0.
PRS_CH1	PA1		PC15					Peripheral Reflex System PRS, channel 1.
PRS_CH2	PC0		PE10					Peripheral Reflex System PRS, channel 2.
PRS_CH3	PC1		PE11					Peripheral Reflex System PRS, channel 3.
TIM0_CC0	PA0	PA0			PA0	PF0		Timer 0 Capture Compare input / output channel 0.
TIM0_CC1	PA1	PA1			PC0	PF1		Timer 0 Capture Compare input / output channel 1.
TIM0_CC2	PA2	PA2			PC1	PF2		Timer 0 Capture Compare input / output channel 2.
TIM1_CC0	PC13	PE10		PB7	PD6			Timer 1 Capture Compare input / output channel 0.
TIM1_CC1	PC14	PE11		PB8	PD7			Timer 1 Capture Compare input / output channel 1.
TIM1_CC2	PC15	PE12		PB11	PC13			Timer 1 Capture Compare input / output channel 2.
US1_CLK	PB7		PF0	PC15				USART1 clock input / output.
US1_CS	PB8		PF1	PC14				USART1 chip select input / output.
US1_RX	PC1		PD6	PD6				USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO).
US1_TX	PC0		PD7	PD7				USART1 Asynchronous Transmit.Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI).

5.3.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32ZG210 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

Table 5.9. GPIO Pinout

Port	Pin 15	Pin 14	Pin 13	Pin 12	Pin 11	Pin 10	Pin 9	Pin 8	Pin 7	Pin 6	Pin 5	Pin 4	Pin 3	Pin 2	Pin 1	Pin 0
Port A	-	-	-	-	-	-	-	-	-	-	-	-	-	PA2	PA1	PA0
Port B	-	PB14	PB13	-	PB11	-	-	PB8	PB7	-	-	-	-	-	-	-
Port C	PC15	PC14	PC13	-	-	-	-	-	-	-	-	-	-	-	PC1	PC0
Port D	-	-	-	-	-	-	-	-	PD7	PD6	PD5	PD4	-	-	-	-
Port E	-	-	PE13	PE12	PE11	PE10	-	-	-	-	-	-	-	-	-	-
Port F	-	-	-	-	-	-	-	-	-	-	-	-	-	PF2	PF1	PF0

5.4 EFM32ZG222 (TQFP48)

5.4.1 Pinout

The EFM32ZG222 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

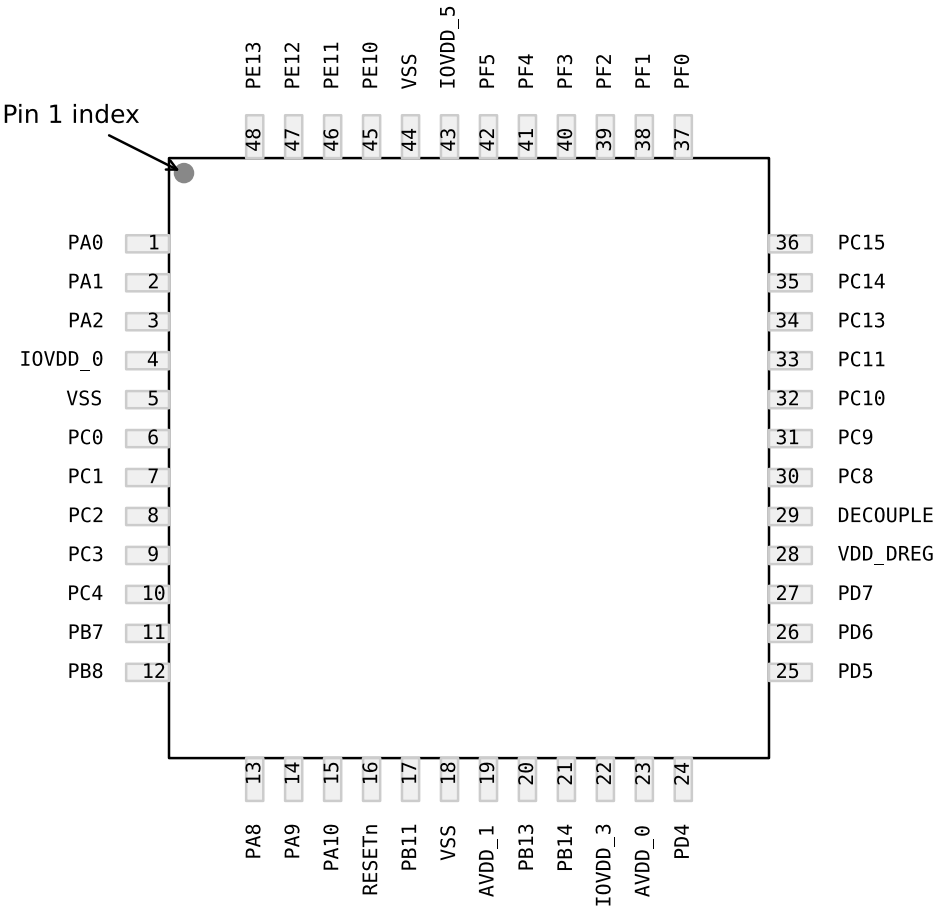


Figure 5.4. EFM32ZG222 Pinout (top view, not to scale)

Table 5.10. Device Pinout

QFP48 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
1	PA0		TIM0_CC0 #0/1/4	LEU0_RX #4 I2C0_SDA #0	PRS_CH0 #0 GPIO_EM4WU0
2	PA1		TIM0_CC1 #0/1	I2C0_SCL #0	CMU_CLK1 #0 PRS_CH1 #0
3	PA2		TIM0_CC2 #0/1		CMU_CLK0 #0

QFP48 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
4	IOVDD_0	Digital IO power supply 0.			
5	VSS	Ground.			
6	PC0	ACMP0_CH0	TIM0_CC1 #4 PCNT0_S0IN #2	US1_TX #0 I2C0_SDA #4	PRS_CH2 #0
7	PC1	ACMP0_CH1	TIM0_CC2 #4 PCNT0_S1IN #2	US1_RX #0 I2C0_SCL #4	PRS_CH3 #0
8	PC2	ACMP0_CH2			
9	PC3	ACMP0_CH3			
10	PC4	ACMP0_CH4			
11	PB7	LFXTAL_P	TIM1_CC0 #3	US1_CLK #0	
12	PB8	LFXTAL_N	TIM1_CC1 #3	US1_CS #0	
13	PA8				
14	PA9				
15	PA10				
16	RESETn	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.			
17	PB11	IDAC0_OUT	TIM1_CC2 #3		
18	VSS	Ground.			
19	AVDD_1	Analog power supply 1.			
20	PB13	HFXTAL_P		LEU0_TX #1	
21	PB14	HFXTAL_N		LEU0_RX #1	
22	IOVDD_3	Digital IO power supply 3.			
23	AVDD_0	Analog power supply 0.			
24	PD4	ADC0_CH4		LEU0_TX #0	
25	PD5	ADC0_CH5		LEU0_RX #0	
26	PD6	ADC0_CH6	TIM1_CC0 #4 PCNT0_S0IN #3	US1_RX #2/3 I2C0_SDA #1	ACMP0_O #2
27	PD7	ADC0_CH7	TIM1_CC1 #4 PCNT0_S1IN #3	US1_TX #2/3 I2C0_SCL #1	CMU_CLK0 #2
28	VDD_DREG	Power supply for on-chip voltage regulator.			
29	DECOUPLE	Decouple output for on-chip voltage regulator. An external capacitance of size $C_{DECOUPLE}$ is required at this pin.			
30	PC8				
31	PC9				GPIO_EM4WU2
32	PC10				
33	PC11				

QFP48 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
34	PC13		TIM1_CC0 #0 TIM1_CC2 #4 PCNT0_S0IN #0		
35	PC14		TIM1_CC1 #0 PCNT0_S1IN #0	US1_CS #3	PRS_CH0 #2
36	PC15		TIM1_CC2 #0	US1_CLK #3	PRS_CH1 #2
37	PF0		TIM0_CC0 #5	US1_CLK #2 LEU0_TX #3 I2C0_SDA #5	DBG_SWCLK #0 BOOT_TX
38	PF1		TIM0_CC1 #5	US1_CS #2 LEU0_RX #3 I2C0_SCL #5	DBG_SWDIO #0 GPIO_EM4WU3 BOOT_RX
39	PF2		TIM0_CC2 #5	LEU0_TX #4	GPIO_EM4WU4
40	PF3				PRS_CH0 #1
41	PF4				PRS_CH1 #1
42	PF5				PRS_CH2 #1
43	IOVDD_5	Digital IO power supply 5.			
44	VSS	Ground.			
45	PE10		TIM1_CC0 #1		PRS_CH2 #2
46	PE11		TIM1_CC1 #1		PRS_CH3 #2
47	PE12		TIM1_CC2 #1	I2C0_SDA #6	CMU_CLK1 #2
48	PE13			I2C0_SCL #6	ACMP0_O #0 GPIO_EM4WU5

5.4.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

Note: Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 5.11. Alternate functionality overview

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
ACMP0_CH0	PC0							Analog comparator ACMP0, channel 0.
ACMP0_CH1	PC1							Analog comparator ACMP0, channel 1.
ACMP0_CH2	PC2							Analog comparator ACMP0, channel 2.
ACMP0_CH3	PC3							Analog comparator ACMP0, channel 3.
ACMP0_CH4	PC4							Analog comparator ACMP0, channel 4.
ACMP0_O	PE13		PD6					Analog comparator ACMP0, digital output.
ADC0_CH4	PD4							Analog to digital converter ADC0, input channel number 4.
ADC0_CH5	PD5							Analog to digital converter ADC0, input channel number 5.
ADC0_CH6	PD6							Analog to digital converter ADC0, input channel number 6.
ADC0_CH7	PD7							Analog to digital converter ADC0, input channel number 7.
BOOT_RX	PF1							Bootloader RX.
BOOT_TX	PF0							Bootloader TX.
CMU_CLK0	PA2		PD7					Clock Management Unit, clock output number 0.
CMU_CLK1	PA1		PE12					Clock Management Unit, clock output number 1.
DBG_SWCLK	PF0							Debug-interface Serial Wire clock input. Note that this function is enabled to pin out of reset, and has a built-in pull down.
DBG_SWDIO	PF1							Debug-interface Serial Wire data input / output. Note that this function is enabled to pin out of reset, and has a built-in pull up.
GPIO_EM4WU0	PA0							Pin can be used to wake the system up from EM4
GPIO_EM4WU2	PC9							Pin can be used to wake the system up from EM4
GPIO_EM4WU3	PF1							Pin can be used to wake the system up from EM4
GPIO_EM4WU4	PF2							Pin can be used to wake the system up from EM4
GPIO_EM4WU5	PE13							Pin can be used to wake the system up from EM4
HFXTAL_N	PB14							High Frequency Crystal negative pin. Also used as external optional clock input pin.
HFXTAL_P	PB13							High Frequency Crystal positive pin.

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
I2C0_SCL	PA1	PD7			PC1	PF1	PE13	I2C0 Serial Clock Line input / output.
I2C0_SDA	PA0	PD6			PC0	PF0	PE12	I2C0 Serial Data input / output.
IDAC0_OUT	PB11							IDAC0 output.
LEU0_RX	PD5	PB14		PF1	PA0			LEUART0 Receive input.
LEU0_TX	PD4	PB13		PF0	PF2			LEUART0 Transmit output. Also used as receive input in half duplex communication.
LFXTAL_N	PB8							Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin.
LFXTAL_P	PB7							Low Frequency Crystal (typically 32.768 kHz) positive pin.
PCNT0_S0IN	PC13		PC0	PD6				Pulse Counter PCNT0 input number 0.
PCNT0_S1IN	PC14		PC1	PD7				Pulse Counter PCNT0 input number 1.
PRS_CH0	PA0	PF3	PC14					Peripheral Reflex System PRS, channel 0.
PRS_CH1	PA1	PF4	PC15					Peripheral Reflex System PRS, channel 1.
PRS_CH2	PC0	PF5	PE10					Peripheral Reflex System PRS, channel 2.
PRS_CH3	PC1		PE11					Peripheral Reflex System PRS, channel 3.
TIM0_CC0	PA0	PA0			PA0	PF0		Timer 0 Capture Compare input / output channel 0.
TIM0_CC1	PA1	PA1			PC0	PF1		Timer 0 Capture Compare input / output channel 1.
TIM0_CC2	PA2	PA2			PC1	PF2		Timer 0 Capture Compare input / output channel 2.
TIM1_CC0	PC13	PE10		PB7	PD6			Timer 1 Capture Compare input / output channel 0.
TIM1_CC1	PC14	PE11		PB8	PD7			Timer 1 Capture Compare input / output channel 1.
TIM1_CC2	PC15	PE12		PB11	PC13			Timer 1 Capture Compare input / output channel 2.
US1_CLK	PB7		PF0	PC15				USART1 clock input / output.
US1_CS	PB8		PF1	PC14				USART1 chip select input / output.
US1_RX	PC1		PD6	PD6				USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO).
US1_TX	PC0		PD7	PD7				USART1 Asynchronous Transmit.Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI).

5.4.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32ZG222 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

Table 5.12. GPIO Pinout

Port	Pin 15	Pin 14	Pin 13	Pin 12	Pin 11	Pin 10	Pin 9	Pin 8	Pin 7	Pin 6	Pin 5	Pin 4	Pin 3	Pin 2	Pin 1	Pin 0
Port A	-	-	-	-	-	PA10	PA9	PA8	-	-	-	-	-	PA2	PA1	PA0
Port B	-	PB14	PB13	-	PB11	-	-	PB8	PB7	-	-	-	-	-	-	-
Port C	PC15	PC14	PC13	-	PC11	PC10	PC9	PC8	-	-	-	PC4	PC3	PC2	PC1	PC0
Port D	-	-	-	-	-	-	-	-	PD7	PD6	PD5	PD4	-	-	-	-
Port E	-	-	PE13	PE12	PE11	PE10	-	-	-	-	-	-	-	-	-	-
Port F	-	-	-	-	-	-	-	-	-	-	PF5	PF4	PF3	PF2	PF1	PF0

6. QFN24 Package Specifications

6.1 QFN24 Package Dimensions

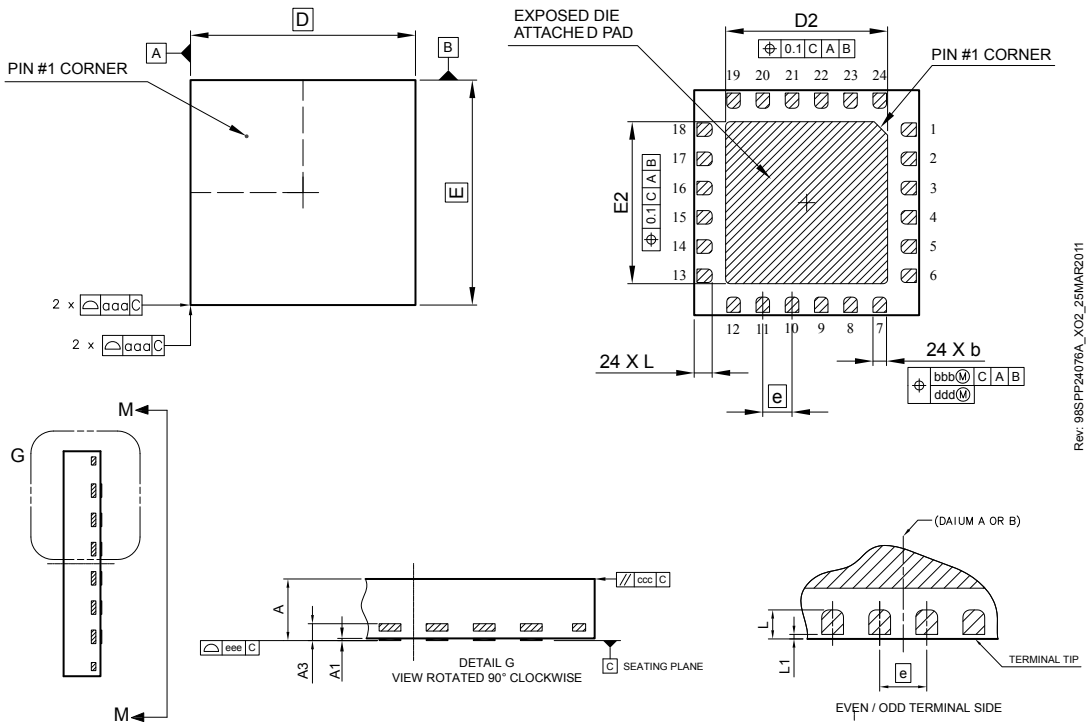


Figure 6.1. QFN24

Note:

1. Dimensioning & tolerancing confirm to ASME Y14.5M-1994.
2. All dimensions are in millimeters. Angles are in degrees.
3. Dimension 'b' applies to metallized terminal and is measured between 0.25 mm and 0.30 mm from the terminal tip. Dimension L1 represents terminal full back from package edge up to 0.1 mm is acceptable.
4. Coplanarity applies to the exposed heat slug as well as the terminal.
5. Radius on terminal is optional.

Table 6.1. QFN (Dimensions in mm)

Symbol	A	A1	A3	b	D	E	D2	E2	e	L	L1	aaa	bbb	ccc	ddd	eee
Min	0.80	0.00	0.203 REF	0.25	5.00 BSC	5.00 BSC	3.50	3.50	0.65 BSC	0.35	0.00	0.10	0.10	0.10	0.05	0.08
Nom	0.85	—		0.30			3.60	3.60		0.40						
Max	0.90	0.05		0.35			3.70	3.70		0.45	0.10					

The QFN24 package uses Nickel-Palladium-Gold preplated leadframe.

All EFM32 packages are RoHS compliant and free of Bromine (Br) and Antimony (Sb).

For additional Quality and Environmental information, please see: http://www.silabs.com/support/quality/pages/default.aspx.

6.2 QFN24 PCB Layout

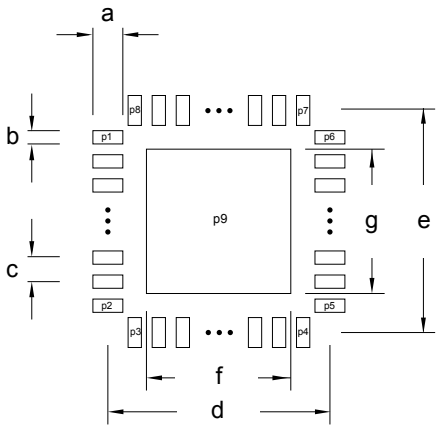


Figure 6.2. QFN24 PCB Land Pattern

Table 6.2. QFN24 PCB Land Pattern Dimensions (Dimensions in mm)

Symbol	Dim. (mm)	Symbol	Pin Number	Symbol	Pin Number
a	0.80	P1	1	P8	24
b	0.30	P2	6	P9	0
c	0.65	P3	7	-	-
d	5.00	P4	12	-	-
e	5.00	P5	13	-	-
f	3.60	P6	18	-	-
g	3.60	P7	19	-	-

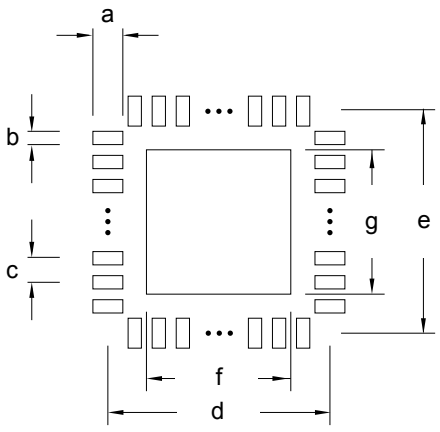


Figure 6.3. QFN24 PCB Solder Mask

Table 6.3. QFN24 PCB Solder Mask Dimensions (Dimensions in mm)

Symbol	Dim. (mm)
a	0.92
b	0.42
c	0.65

Symbol	Dim. (mm)
d	5.00
e	5.00
f	3.72
g	3.72

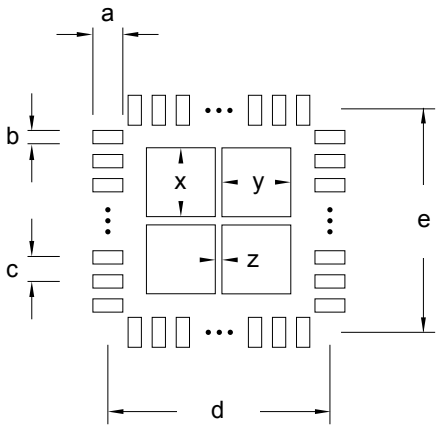


Figure 6.4. QFN24 PCB Stencil Design

Table 6.4. QFN24 PCB Stencil Design Dimensions (Dimensions in mm)

Symbol	Dim. (mm)
a	0.60
b	0.25
c	0.65
d	5.00
e	5.00
x	1.00
y	1.00
z	0.50

Note:

1. The drawings are not to scale.
2. All dimensions are in millimeters.
3. All drawings are subject to change without notice.
4. The PCB Land Pattern drawing is in compliance with IPC-7351B.
5. Stencil thickness 0.125 mm.
6. For detailed pin-positioning, see Pin Definitions.

6.3 QFN24 Package Marking

In the illustration below package fields and position are shown.

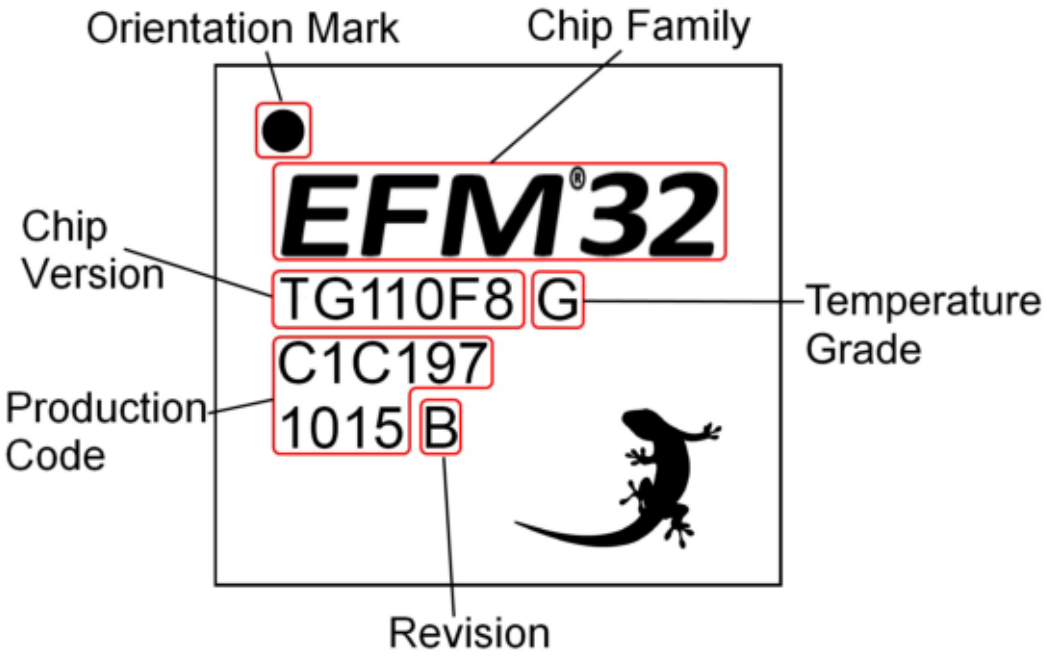


Figure 6.5. Example Chip Marking (Top View)

7. QFN32 Package Specifications

7.1 QFN32 Package Dimensions

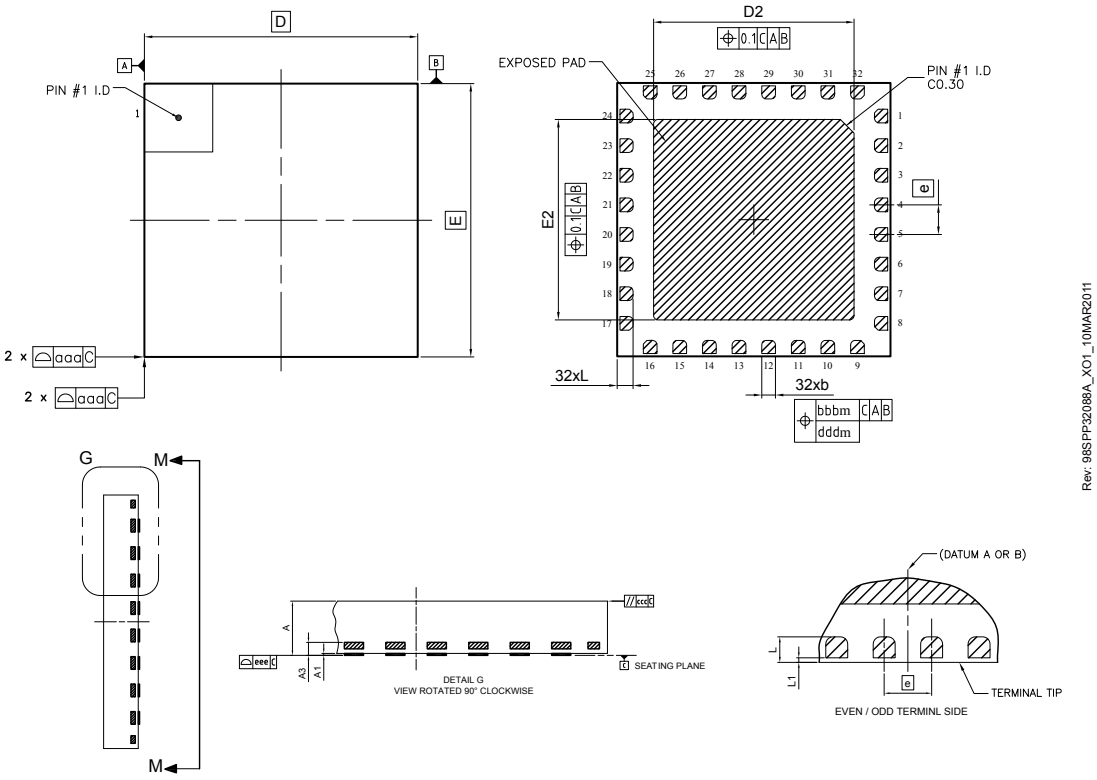


Figure 7.1. QFN32

Note:

1. Dimensioning & tolerancing confirm to ASME Y14.5M-1994.
2. All dimensions are in millimeters. Angles are in degrees.
3. Dimension 'b' applies to metallized terminal and is measured between 0.25 mm and 0.30 mm from the terminal tip. Dimension L1 represents terminal full back from package edge up to 0.1 mm is acceptable.
4. Coplanarity applies to the exposed heat slug as well as the terminal.
5. Radius on terminal is optional.

Table 7.1. QFN32 (Dimensions in mm)

Symbol	A	A1	A3	b	D	E	D2	E2	e	L	L1	aaa	bbb	ccc	ddd	eee
Min	0.80	0.00	0.203 REF	0.25	6.00 BSC	6.00 BSC	4.30	4.30	0.65 BSC	0.35	0.00	0.10	0.10	0.10	0.05	0.08
Nom	0.85	—		0.30			4.40	4.40		0.40						
Max	0.90	0.05		0.35			4.50	4.50		0.45	0.10					

The QFN32 package uses Nickel-Palladium-Gold preplated leadframe.

All EFM32 packages are RoHS compliant and free of Bromine (Br) and Antimony (Sb).

For additional Quality and Environmental information, please see: http://www.silabs.com/support/quality/pages/default.aspx.

7.2 QFN32 PCB Layout

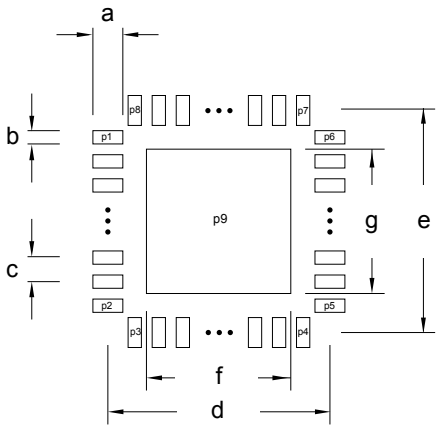


Figure 7.2. QFN32 PCB Land Pattern

Table 7.2. QFN32 PCB Land Pattern Dimensions (Dimensions in mm)

Symbol	Dim. (mm)	Symbol	Pin Number	Symbol	Pin Number
a	0.80	P1	1	P6	24
b	0.35	P2	8	P7	25
c	0.65	P3	9	P8	32
d	6.00	P4	16	P9	0
e	6.00	P5	17		
f	4.40				
g	4.40				

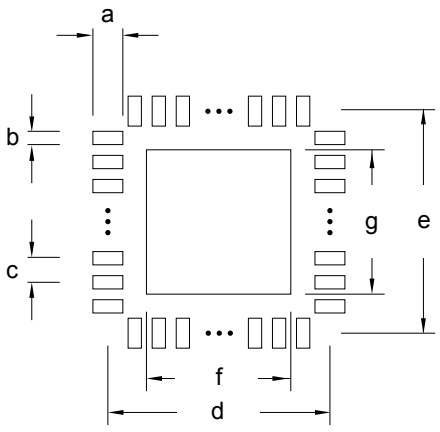


Figure 7.3. QFN32 PCB Solder Mask

Table 7.3. QFN32 PCB Solder Mask Dimensions (Dimensions in mm)

Symbol	Dim. (mm)
a	0.92
b	0.47
c	0.65
d	6.00
e	6.00
f	4.52
g	4.52

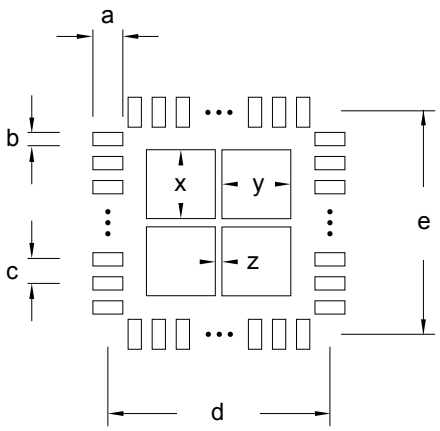


Figure 7.4. QFN32 PCB Stencil Design

Table 7.4. QFN32 PCB Stencil Design Dimensions (Dimensions in mm)

Symbol	Dim. (mm)
a	0.70
b	0.25
c	0.65
d	6.00
e	6.00
x	1.30
y	1.30
z	0.50

Note:

1. The drawings are not to scale.
2. All dimensions are in millimeters.
3. All drawings are subject to change without notice.
4. The PCB Land Pattern drawing is in compliance with IPC-7351B.
5. Stencil thickness 0.125 mm.
6. For detailed pin-positioning, see Pin Definitions.

7.3 QFN32 Package Marking

In the illustration below package fields and position are shown.

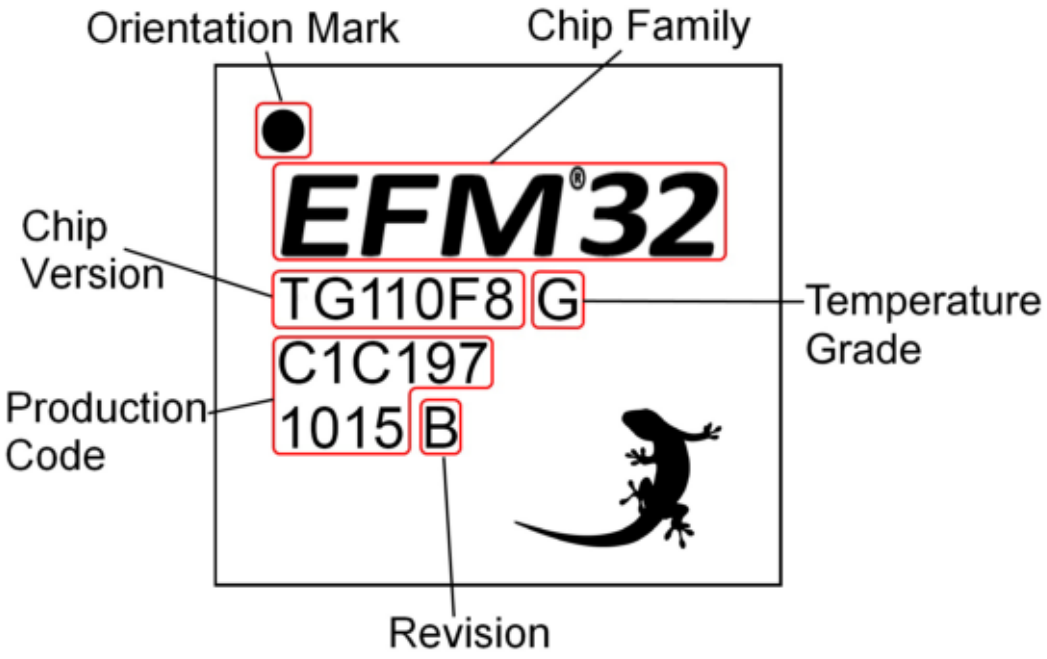


Figure 7.5. Example Chip Marking (Top View)

8. TQFP48 Package Specifications

8.1 TQFP48 Package Dimensions

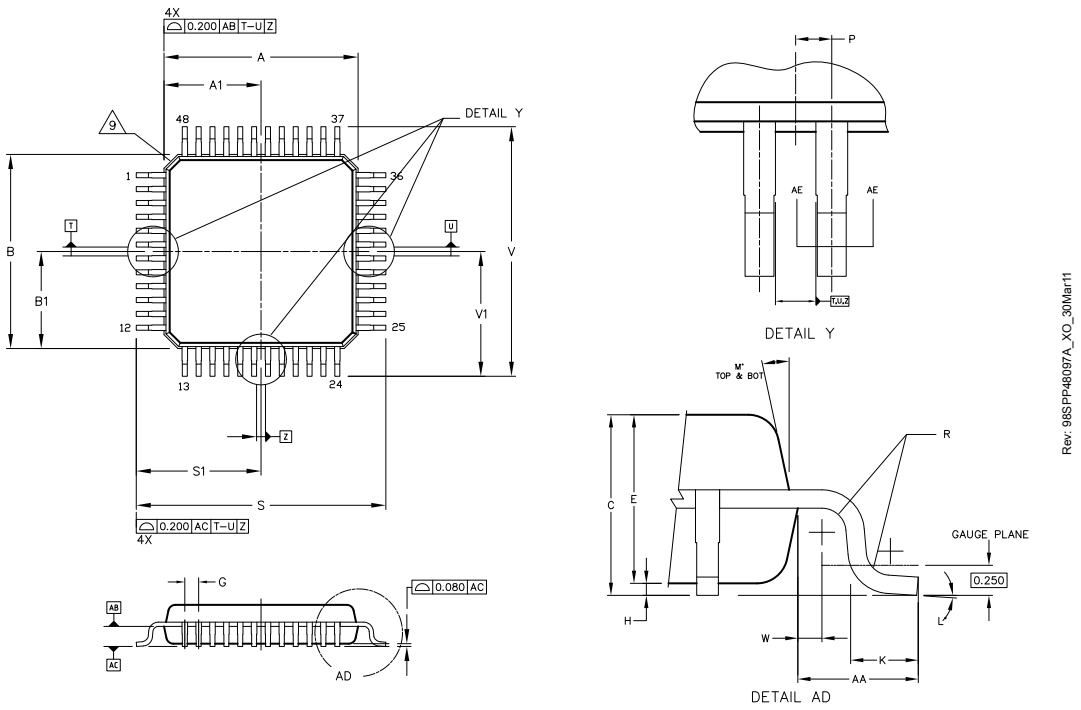


Figure 8.1. TQFP48

Note:

1. Dimensions and tolerance per ASME Y14.5M-1994
2. Control dimension: Millimeter
3. Datum plane AB is located at bottom of lead and is coincident with the lead where the lead exists from the plastic body at the bottom of the parting line.
4. Datums T, U and Z to be determined at datum plane AB.
5. Dimensions S and V to be determined at seating plane AC.
6. Dimensions A and B do not include mold protrusion. Allowable protrusion is 0.250 per side. Dimensions A and B do include mold mismatch and are determined at datum AB.
7. Dimension D does not include dambar protrusion. Dambar protrusion shall not cause the D dimension to exceed 0.350.
8. Minimum solder plate thickness shall be 0.0076.
9. Exact shape of each corner is optional.

Table 8.1. QFP48 (Dimensions in mm)

DIM	MIN	NOM	MAX	DIM	MIN	NOM	MAX
A	—	7.000 BSC	—	M	—	12DEG REF	
A1	—	3.500 BSC	—	N	0.090	—	0.160
B	—	7.000 BSC	—	P	—	0.250 BSC	—
B1	—	3.500 BSC	—	R	0.150	—	0.250
C	1.000	—	1.200	S	—	9.000 BSC	—
D	0.170	—	0.270	S1	—	4.500 BSC	—
E	0.950	—	1.050	V	—	9.000 BSC	—
F	0.170	—	0.230	V1	—	4.500 BSC	—
G	—	0.500 BSC	—	W	—	0.200 BSC	—
H	0.050	—	0.150	AA	—	1.000 BSC	—
J	0.090	—	0.200				
K	0.500	—	0.700				
L	0DEG	—	7DEG				

The TQFP48 package is 7 by 7 mm in size and has a 0.5 mm pin pitch.

The TQFP48 package uses Nickel-Palladium-Gold preplated leadframe.

All EFM32 packages are RoHS compliant and free of Bromine (Br) and Antimony (Sb).

For additional Quality and Environmental information, please see: http://www.silabs.com/support/quality/pages/default.aspx.

8.2 TQFP48 PCB Layout

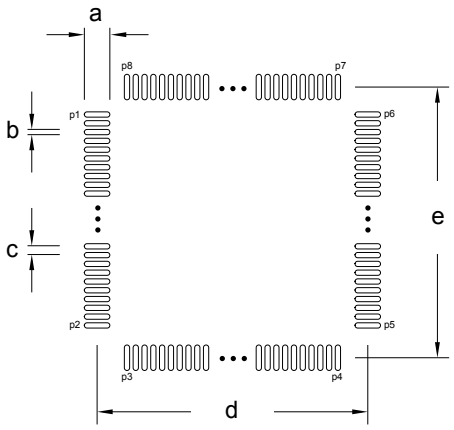


Figure 8.2. TQFP48 PCB Land Pattern

Table 8.2. TQFP48 PCB Land Pattern Dimensions (Dimensions in mm)

Symbol	Dim. (mm)	Symbol	Pin Number	Symbol	Pin Number
a	1.60	P1	1	P6	36
b	0.30	P2	12	P7	37
c	0.50	P3	13	P8	48
d	8.50	P4	24		
e	8.50	P5	25		

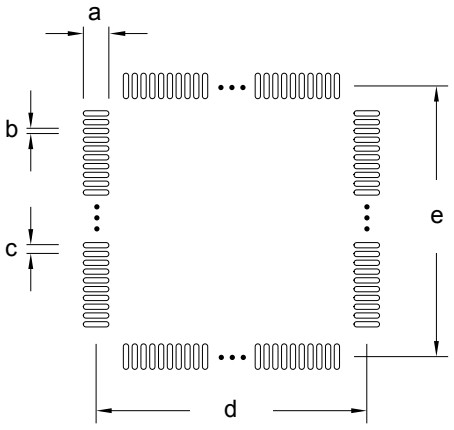


Figure 8.3. TQFP48 PCB Solder Mask

Table 8.3. TQFP48 PCB Solder Mask Dimensions (Dimensions in mm)

Symbol	Dim. (mm)
a	1.72
b	0.42
c	0.50
d	8.50
e	8.50

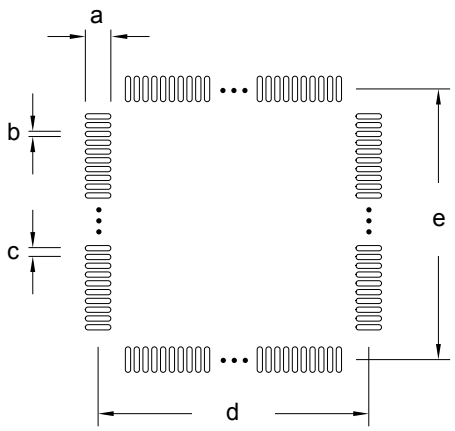


Figure 8.4. TQFP48 PCB Stencil Design

Table 8.4. TQFP48 PCB Stencil Design Dimensions (Dimensions in mm)

Symbol	Dim. (mm)
a	1.50
b	0.20
c	0.50
d	8.50
e	8.50

Note:

1. The drawings are not to scale.
2. All dimensions are in millimeters.
3. All drawings are subject to change without notice.
4. The PCB Land Pattern drawing is in compliance with IPC-7351B.
5. Stencil thickness 0.125 mm.
6. For detailed pin-positioning, see Pin Definitions.

8.3 TQFP48 Package Marking

In the illustration below package fields and position are shown.

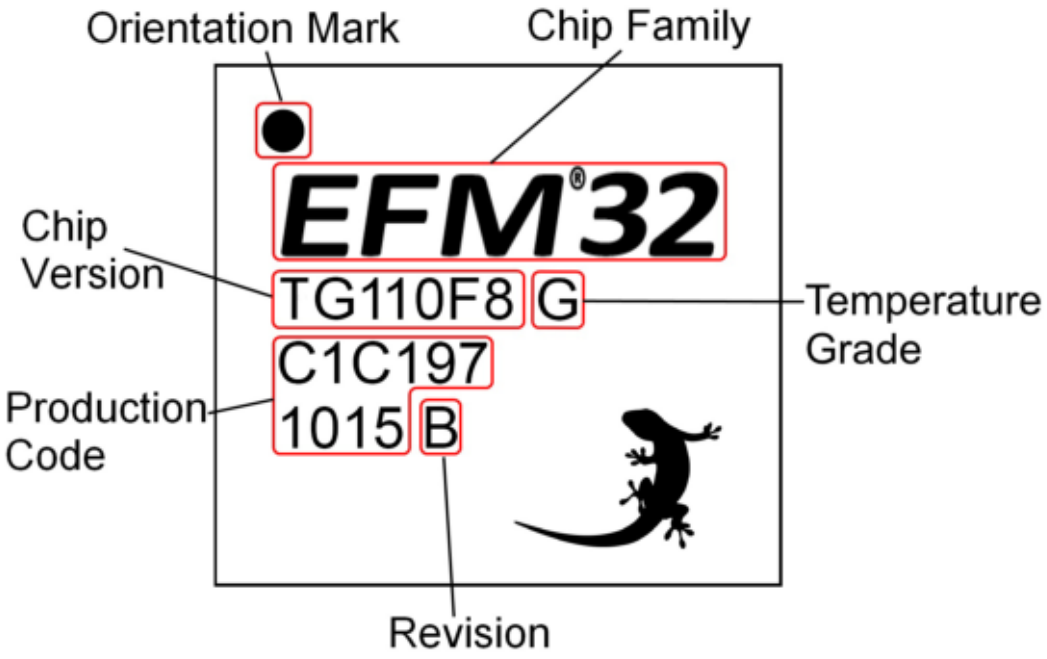


Figure 8.5. Example Chip Marking (Top View)

9. Chip Revision, Solder Information, Errata

9.1 Chip Revision

The revision of a chip can be determined from the "Revision" field in the package marking.

9.2 Soldering Information

The latest IPC/JEDEC J-STD-020 recommendations for Pb-Free reflow soldering should be followed.

9.3 Errata

See the errata document for description and resolution of device errata. This document is available in Simplicity Studio and online at: http://www.silabs.com/support/pages/document-library.aspx?p=MCUs--32-bit

10. Revision History

Revision 2.20

November, 2021

- Changed 2. Ordering Information to reflect Tape and Reel packaging.

Revision 2.10

September, 2019

- 1. Feature List:
  - Added SysTick.
  - Corrected bootloader type.
- 2. Ordering Information - Updated for release of revision B devices.
- 4.1.1 Typical Values - Removed reference to simulation.
- 4.1.2 Minimum and Maximum Values - Removed reference to simulation.
- 4.2 Absolute Maximum Ratings - Removed footnote about storage temperature and added max sink/source current per I/O pin.
- 4.10 Analog Digital Converter (ADC) - Updated ADC input impedance.
- 6.2 QFN24 PCB Layout - Corrected pin number for symbol P9.
- 7.2 QFN32 PCB Layout - Corrected pin number for symbol P9.

Revision 2.00

July, 2018

- Consolidated all EFM32ZG data sheets:
  - EFM32ZG108
  - EFM32ZG110
  - EFM32ZG210
  - EFM32ZG222
- Added a Feature List section.
- 2. Ordering Information – Added ordering code decoder.
- 3.3 Memory Map – Separated the Memory Map into two figures – one for core and code space listing and one for peripheral listing.
- 4.2 Absolute Maximum Ratings – Updated preface.
- 4.7 Flash – Added word write cycles between erase (WWC_{FLASH}) specification.
- 7.2 QFN32 PCB Layout - Corrected pin number for symbol P3 in Table 7.2 QFN32 PCB Land Pattern Dimensions (Dimensions in mm) on page 91.
- 9.2 Soldering Information - Removed MSL information (Moisture Sensitivity Level). MSL information can be found in the Qual report that is available on the Silicon Labs website.
- New formatting throughout.

Revision 1.10

March 6th, 2015

- This revision applies the following devices:
  - EFM32ZG108
  - EFM32ZG110
  - EFM32ZG210
  - EFM32ZG222
- For device with ADC, updated ADC data, updated temperature sensor graph and added clarification on conditions for INL_{ADC} and DNL_{ADC} parameters.
- Updated Max ESR_{HFXO} value for Crystal Frequency of 24 MHz.
- Updated current consumption.
- Updated LFXO and HFXO data.
- Updated LFRCO and HFRCO data.
- Updated ACMP data.
- Updated VCMP data.
- Updated Memory Map.
- Added DMA current in Digital Peripherals section.
- Added AUXHFRCO to block diagram and Electrical Characteristics.
- For QFN24 and QFN32 packages, updated Package dimensions table.
- Updated block diagram.

Revision 1.00

July 2nd, 2014

- This revision applies the following devices:
  - EFM32ZG108
  - EFM32ZG110
  - EFM32ZG210
  - EFM32ZG222
- Corrected single power supply voltage minimum value from 1.85V to 1.98V.
- Removed "Preliminary" markings.
- Updated current consumption.
- Updated transition between energy modes.
- Updated power management data.
- Updated GPIO data.
- Updated LFXO, HFXO, HFRCO and ULFRCO data.
- Updated LFRCO and HFRCO plots.
- For devices with ADC, updated ADC data.
- Updated ACMP data.

Revision 0.61

November 21st, 2013

- This revision applies the following devices:
  - EFM32ZG108
  - EFM32ZG110
  - EFM32ZG210
  - EFM32ZG222
- Updated figures.
- Updated errata-link.
- Updated chip marking.
- Added link to Environmental and Quality information.
- For devices with IDAC, re-added missing DAC-data.

Revision 0.60

October 9th, 2013

- This revision applies the following devices:
  - EFM32ZG108
  - EFM32ZG110
  - EFM32ZG210
  - EFM32ZG222
- Added I2C characterization data.
- For devices with IDAC, added IDAC characterization data.
- Updated current consumption table and figures in Electrical characteristics section.
- For devices with ADC, corrected the ADC resolution from 12, 10 and 6 bit to 12, 8 and 6 bit.
- Removed Environmental information.
- Updated trademark, disclaimer and contact information.
- Other minor corrections.

Revision 0.50

April 22nd, 2013

- This revision applies the following devices:
  - EFM32ZG108
  - EFM32ZG110
  - EFM32ZG210
  - EFM32ZG222
- Updated HFCORE max frequency from 32 MHz to 24 MHz.
- For EFM32ZG108, added DMA, AES and IDAC.
- For EFM32ZG108, added DMA module.
- Updated pinout.
- Other minor corrections.

Revision 0.40

September 11th, 2012

- This revision applies the following devices:
  - EFM32ZG108
  - EFM32ZG110
  - EFM32ZG210
  - EFM32ZG222
- Updated CPU core from Cortex M0 to Cortex M0+.
- Updated the HFRCO 1 MHz band typical value to 1.2 MHz.
- Updated the HFRCO 7 MHz band typical value to 6.6 MHz.
- Corrected operating voltage from 1.8 V to 1.85 V.
- Other minor corrections.

Revision 0.30

July 16th, 2011

- This revision applies the following devices:
  - EFM32ZG108
  - EFM32ZG110
  - EFM32ZG210
  - EFM32ZG222
- Updated the Electrical Characteristics section.

Revision 0.20

June 8th, 2011

- This revision applies the following devices:
  - EFM32ZG108
  - EFM32ZG110
  - EFM32ZG210
  - EFM32ZG222
- Corrected all current values in Electrical Characteristics section.
- Updated Cortex M0 related items in the memory map.
- For EFM32ZG222, corrected pinout to 37.

Revision 0.10

June 7th, 2011

- This revision applies the following devices:
  - EFM32ZG108
  - EFM32ZG110
  - EFM32ZG210
  - EFM32ZG222
- Initial preliminary release.

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