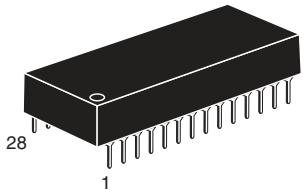
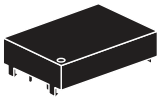
M48Z35, M48Z35Y

256 Kbit (32 Kbit x 8) ZEROPOWER® SRAM

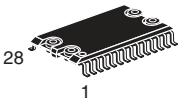
Datasheet - production data



PDIP 28.7
Battery CAPHAT™



SNAPHAT® battery



SOH28

Features

- Integrated, ultra low power SRAM, power-fail control circuit, and battery
- READ cycle time equals WRITE cycle time
- Automatic power-fail chip deselect and WRITE protection
- WRITE protect voltages:
  (V_{PFD} = power-fail deselect voltage)
- M48Z35: V_{CC} = 4.75 to 5.5 V;
  4.5 V ≤ V_{PFD} ≤ 4.75 V
- M48Z35Y: 4.5 to 5.5 V;
  4.2 V ≤ V_{PFD} ≤ 4.5 V
- Self-contained battery in the CAPHAT™ DIP package
- Packaging includes a 28-lead SOIC and SNAPHAT® top (to be ordered separately)
- Pin and function compatible with JEDEC standard 32 K x 8 SRAMs
- SOIC package provides direct connection for a SNAPHAT® top which contains the battery
- RoHS compliant
- Lead-free second level interconnect

Description

The M48Z35/Y ZEROPOWER® RAM is a 32 K x 8, non-volatile static RAM that integrates power-fail deselect circuitry and battery control logic on a single die. The monolithic chip is available in two special packages to provide a highly integrated battery-backed memory solution.

The M48Z35/Y is a non-volatile pin and function equivalent to any JEDEC standard 32 K x 8 SRAM. It also easily fits into many ROM, EPROM, and EEPROM sockets, providing the non-volatility of PROMs without any requirement for special WRITE timing or limitations on the number of WRITEs that can be performed. The 28-pin 600 mil DIP CAPHAT™ houses the M48Z35/Y silicon with a long life lithium button cell in a single package.

The 28-pin 330 mil SOIC provides sockets with gold plated contacts at both ends for direct connection to a separate SNAPHAT® housing containing the battery. The unique design allows the SNAPHAT battery package to be mounted on top of the SOIC package after the completion of the surface mount process. Insertion of the SNAPHAT housing after reflow prevents potential battery damage due to the high temperatures required for device surface-mounting. The SNAPHAT housing is keyed to prevent reverse insertion.

The SOIC and battery packages are shipped separately in plastic anti-static tubes or in tape & reel form.

For the 28-lead SOIC, the battery package (i.e. SNAPHAT) part number is “M4Z28-BR00SH1”.

This is information on a product in full production. www.st.com

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1 Diagram

Figure 1. Logic diagram

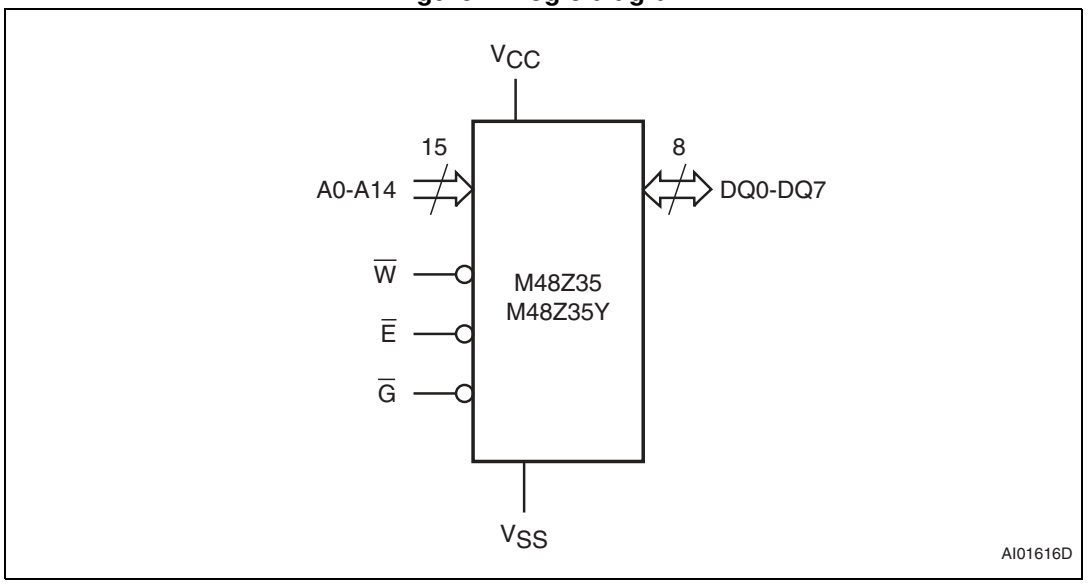


Table 1. Signal names

A0-A14	Address inputs
DQ0-DQ7	Data inputs / outputs
$\overline{E}$	Chip enable input
$\overline{G}$	Output enable input
$\overline{W}$	WRITE enable input
V_{CC}	Supply voltage
V_{SS}	Ground

2 Pin connection

Figure 2. DIP connections

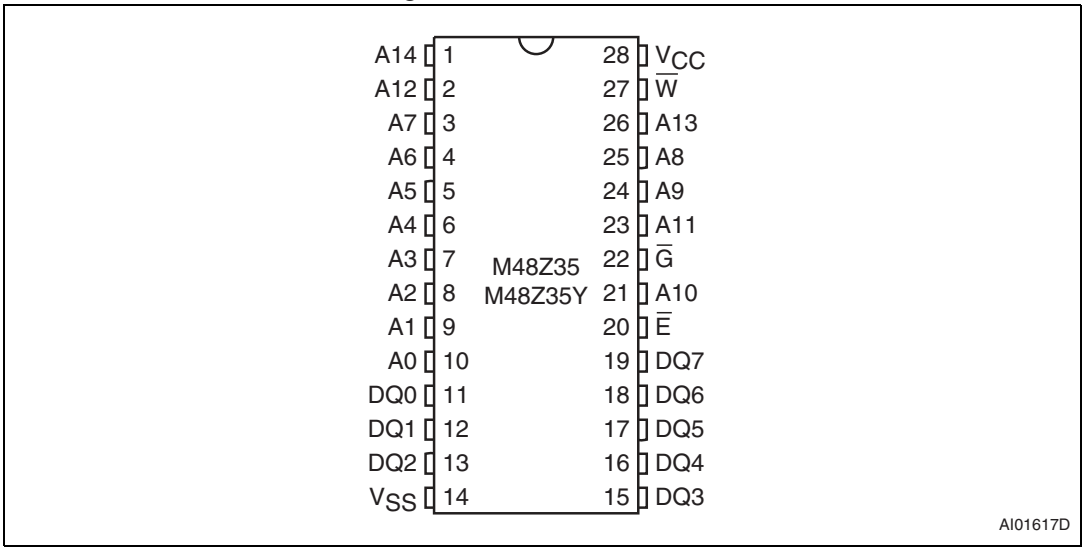


Figure 3. SOIC connections

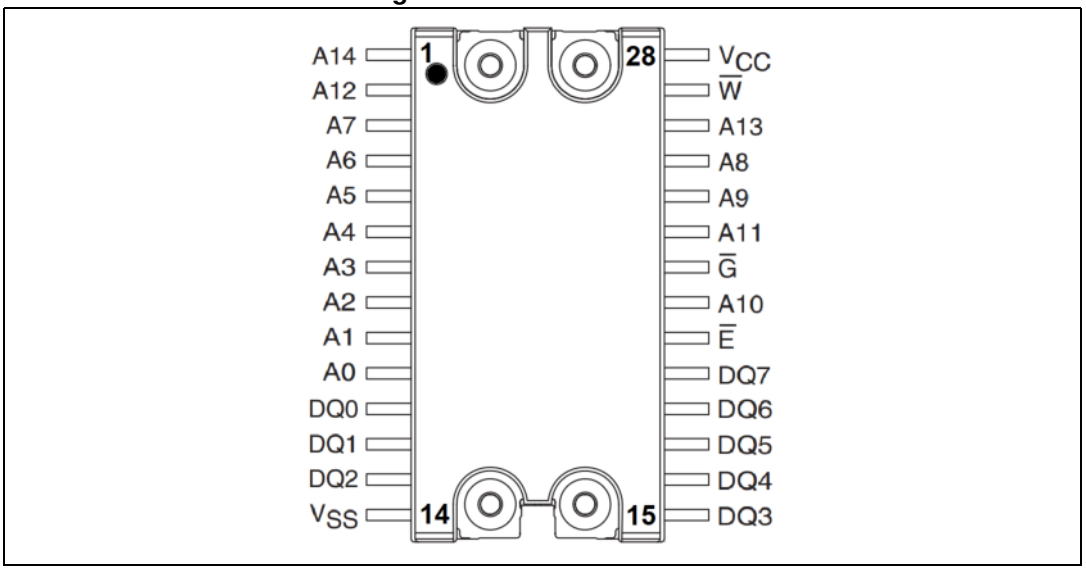
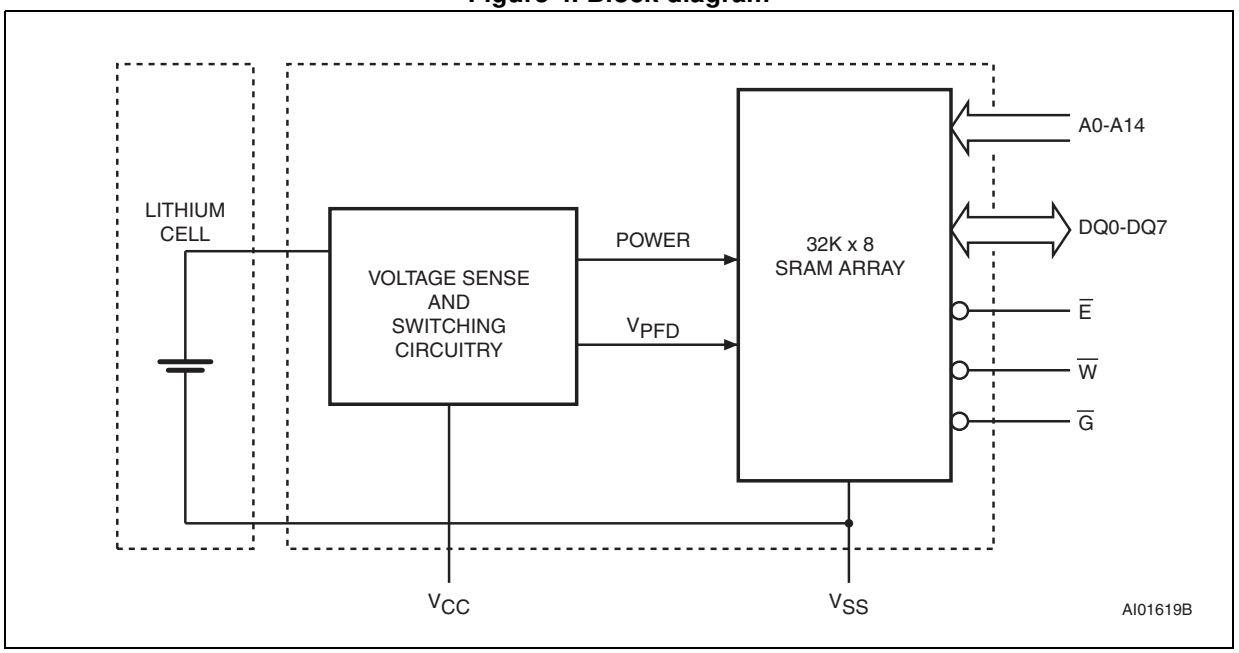


Figure 4. Block diagram



3 Operation modes

The M48Z35/Y also has its own power-fail detect circuit. The control circuitry constantly monitors the single 5 V supply for an out of tolerance condition. When V_{CC} is out of tolerance, the circuit write protects the SRAM, providing a high degree of data security in the midst of unpredictable system operation brought on by low V_{CC}. As V_{CC} falls below approximately 3 V, the control circuitry connects the battery which maintains data until valid power returns.

Table 2. Operating modes

Mode	V_{CC}	$\overline{E}$	$\overline{G}$	$\overline{W}$	DQ0-DQ7	Power
Deselect	4.75 to 5.5 V or 4.5 to 5.5 V	V_{IH}	X	X	High Z	Standby
WRITE		V_{IL}	X	V_{IL}	D_{IN}	Active
READ		V_{IL}	V_{IL}	V_{IH}	D_{OUT}	Active
READ		V_{IL}	V_{IH}	V_{IH}	High Z	Active
Deselect	V_{SO} to V_{PFD}(min)(1)	X	X	X	High Z	CMOS standby
Deselect	$\leq V_{SO}$(1)	X	X	X	High Z	Battery backup mode

1. See *Table 6* for details.

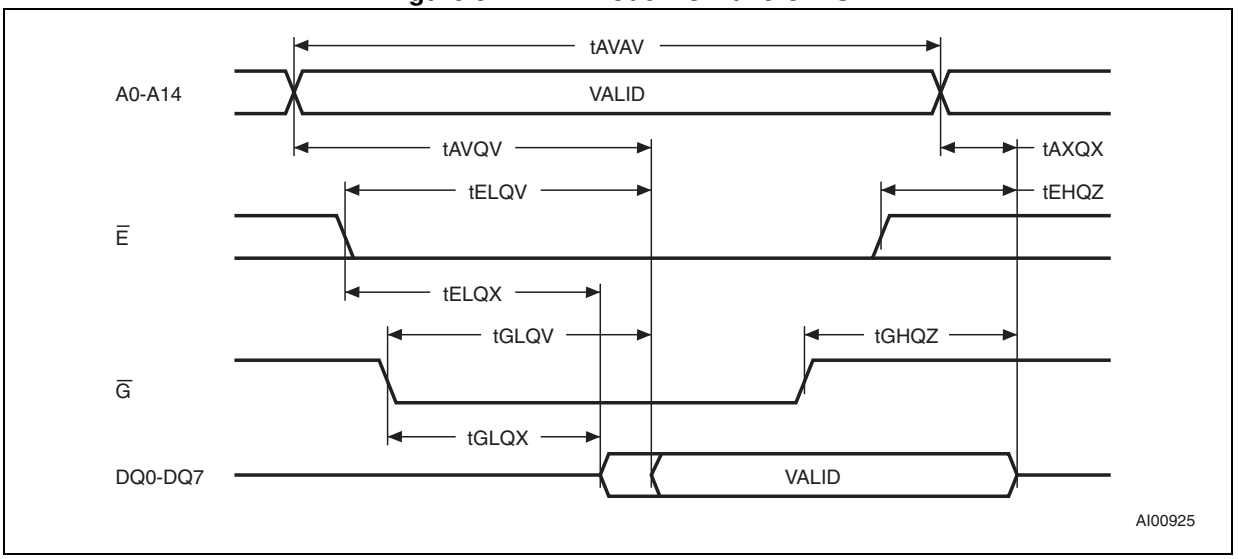
Note: X = V_{IH} or V_{IL}; V_{SO} = battery backup switchover voltage.

3.1 READ mode

The M48Z35/Y is in the READ mode whenever $\overline{W}$ (WRITE enable) is high, $\overline{E}$ (chip enable) is low. The device architecture allows ripple-through access of data from eight of 264,144 locations in the static storage array. Thus, the unique address specified by the 15 address inputs defines which one of the 32,768 bytes of data is to be accessed. Valid data will be available at the data I/O pins within address access time (t_{AVQV}) after the last address input signal is stable, providing that the $\overline{E}$ and $\overline{G}$ access times are also satisfied. If the $\overline{E}$ and $\overline{G}$ access times are not met, valid data will be available after the latter of the chip enable access time (t_{ELQV}) or output enable access time (t_{GLQV}).

The state of the eight three-state data I/O signals is controlled by $\overline{E}$ and $\overline{G}$. If the outputs are activated before t_{AVQV}, the data lines will be driven to an indeterminate state until t_{AVQV}. If the address inputs are changed while $\overline{E}$ and $\overline{G}$ remain active, output data will remain valid for output data hold time (t_{AXQX}) but will go indeterminate until the next address access.

Figure 5. READ mode AC waveforms



Note: WRITE enable ($\overline{W}$) = high.

Table 3. READ mode AC characteristics

Symbol	Parameter[1]	M48Z02/M48Z12		Unit
		Min.	Max.	
t_{AVAV}	READ cycle time	70		ns
t_{AVQV}[2]	Address valid to output valid		70	ns
t_{ELQV}[2]	Chip enable low to output valid		70	ns
t_{GLQV}[2]	Output enable low to output valid		35	ns
t_{ELQX}[3]	Chip enable low to output transition	5		ns
t_{GLQX}[3]	Output enable low to output transition	5		ns
t_{EHQZ}[3]	Chip enable high to output Hi-Z		25	ns
t_{GHQZ}[3]	Output enable high to output Hi-Z		25	ns
t_{AXQX}[2]	Address transition to output transition	10		ns

1. Valid for ambient operating temperature: T_A = 0 to 70 °C; V_{CC} = 4.75 to 5.5 V or 4.5 to 5.5 V (except where noted).
2. C_L = 100 pF
3. C_L = 5 pF

3.2 WRITE mode

The M48Z35/Y is in the WRITE mode whenever $\overline{W}$ and $\overline{E}$ are low. The start of a WRITE is referenced from the latter occurring falling edge of $\overline{W}$ or $\overline{E}$. A WRITE is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E}$. The addresses must be held valid throughout the cycle. $\overline{E}$ or $\overline{W}$ must return high for a minimum of t_{EHAX} from chip enable or t_{WHAX} from WRITE enable prior to the initiation of another READ or WRITE cycle. Data-in must be valid t_{DVWH} prior to the end of WRITE and remain valid for t_{WHDX} afterward. $\overline{G}$ should be kept high during WRITE cycles to avoid bus contention; although, if the output bus has been activated by a low on $\overline{E}$ and $\overline{G}$, a low on $\overline{W}$ will disable the outputs t_{WLQZ} after $\overline{W}$ falls.

Figure 6. WRITE enable controlled, WRITE AC waveform

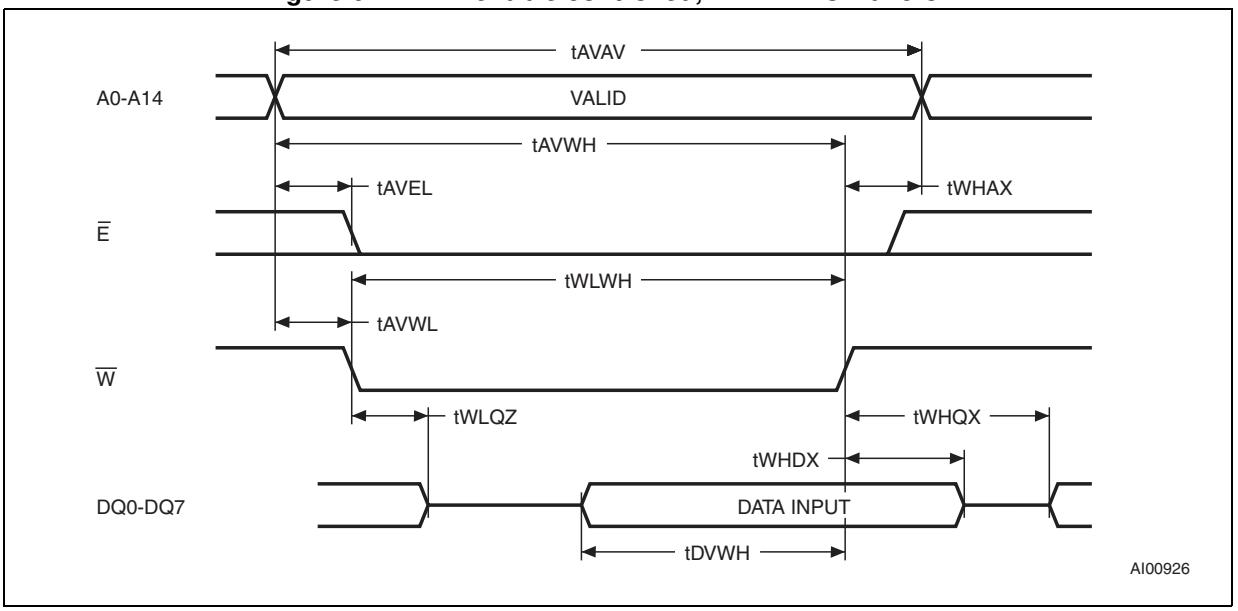


Figure 7. Chip enable controlled, WRITE AC waveforms

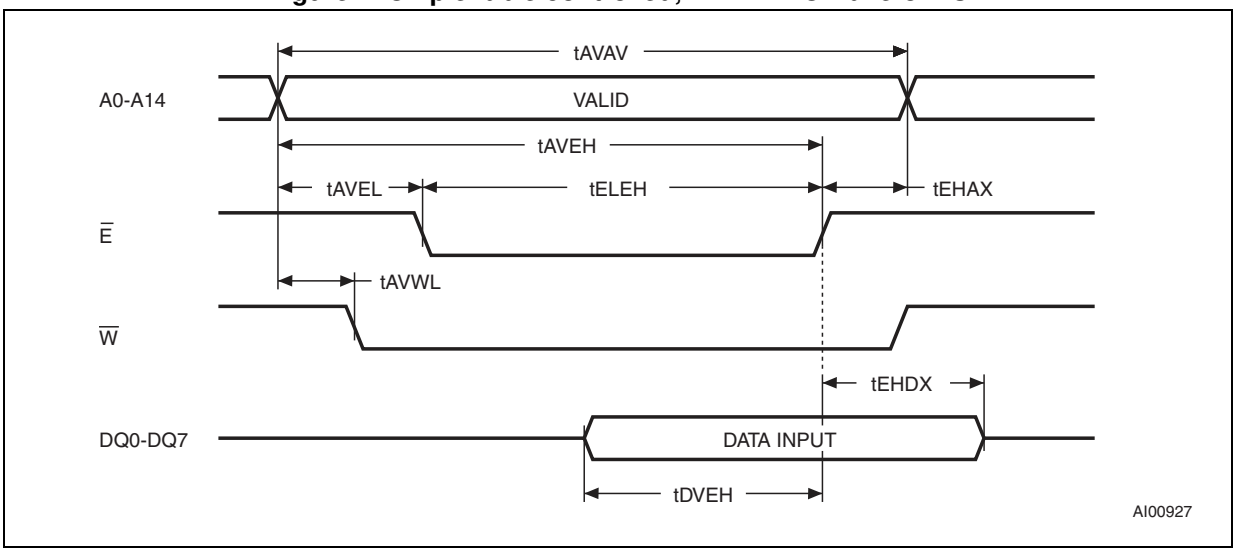


Table 4. WRITE mode AC characteristics

Symbol	Parameter[1]	M48Z35/M48Z35Y		Unit
		-70		
		Min.	Max.	
t_{AVAV}	WRITE cycle time	70		ns
t_{AVWL}	Address valid to WRITE enable low	0		ns
t_{AVEL}	Address valid to chip enable 1 low	0		ns
t_{WLWH}	WRITE enable pulse width	50		ns
t_{ELEH}	Chip enable low to chip enable 1 high	55		ns
t_{WHAX}	WRITE enable high to address transition	0		ns
t_{EHAX}	Chip enable high to address transition	0		ns
t_{DVWH}	Input valid to WRITE enable high	30		ns
t_{DVEH}	Input valid to chip enable high	30		ns
t_{WHDX}	WRITE enable high to input transition	5		ns
t_{EHDX}	Chip enable high to input transition	5		ns
t_{WLQZ}[2][3]	WRITE enable low to output Hi-Z		25	ns
t_{AVWH}	Address valid to WRITE enable high	60		ns
t_{AVEH}	Address valid to chip enable high	60		ns
t_{WHQX}[2][3]	WRITE enable high to output transition	5		ns

1. Valid for ambient operating temperature: T_A = 0 to 70 °C; V_{CC} = 4.75 to 5.5 V or 4.5 to 5.5 V (except where noted).
2. C_L = 5 pF.
3. If $\overline{E}$ goes low simultaneously with W going low, the outputs remain in the high impedance state.

3.3 Data retention mode

With valid V_{CC} applied, the M48Z35/Y operates as a conventional BYTEWIDE™ static RAM. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself when V_{CC} falls within the V_{PFD} (max), V_{PFD} (min) window. All outputs become high impedance, and all inputs are treated as “don't care.”

Note: A power failure during a WRITE cycle may corrupt data at the currently addressed location, but does not jeopardize the rest of the RAM's content. At voltages below V_{PFD} (min), the user can be assured the memory will be in a write protected state, provided the V_{CC} fall time is not less than t_F. The M48Z35/Y may respond to transient noise spikes on V_{CC} that reach into the deselect window during the time the device is sampling V_{CC}. Therefore, decoupling of the power supply lines is recommended.

When V_{CC} drops below V_{SO}, the control circuit switches power to the internal battery which preserves data. The internal button cell will maintain data in the M48Z35/Y for an accumulated period of at least 11 years when V_{CC} is less than V_{SO}.

As system power returns and V_{CC} rises above V_{SO}, the battery is disconnected, and the power supply is switched to external V_{CC}. Write protection continues until V_{CC} reaches V_{PFD} (min) plus t_{rec} (min). E should be kept high as V_{CC} rises past V_{PFD} (min) to prevent inadvertent write cycles prior to system stabilization. Normal RAM operation can resume t_{rec}

after V_{CC} exceeds V_{PFD} (max). For more information on battery storage life refer to the application note AN1012.

Figure 8. Power down/up mode AC waveforms

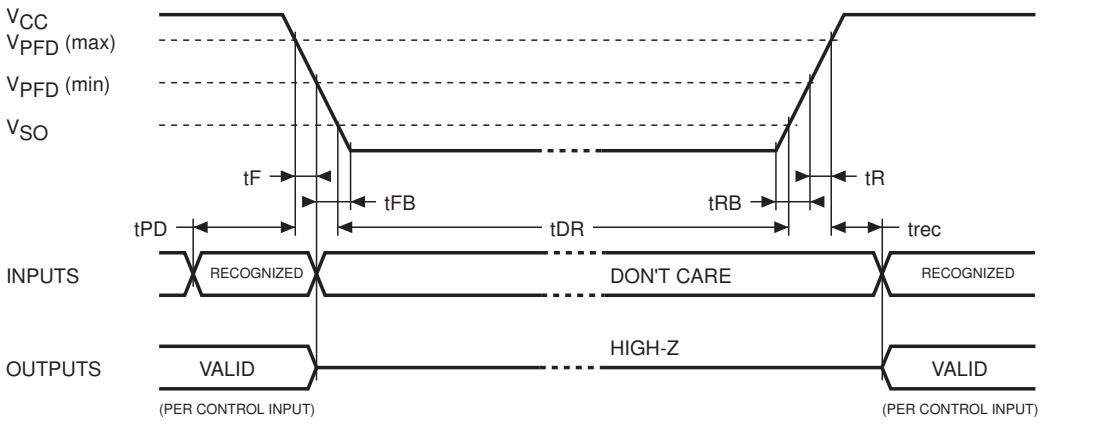


Table 5. Power down/up AC characteristics

Symbol	Parameter(1)	Min.	Max.	Unit
t_{PD}	$\overline{E}$ or $\overline{W}$ at V_{IH} before power down	0		µs
t_F(2)	V_{PFD} (max) to V_{PFD} (min) V_{CC} fall time	300		µs
t_{FB}(3)	V_{PFD} (min) to V_{SS} V_{CC} fall time	10		µs
t_R	V_{PFD} (min) to V_{PFD} (max) V_{CC} rise time	10		µs
t_{RB}	V_{SS} to V_{PFD} (min) V_{CC} rise time	1		µs
t_{rec}	V_{PFD} (max) to inputs recognized	40	200	ms

1. Valid for ambient operating temperature: T_A = 0 to 70 °C; V_{CC} = 4.75 to 5.5 V or 4.5 to 5.5 V (except where noted).
2. V_{PFD} (max) to V_{PFD} (min) fall time of less than t_F may result in deselection/write protection not occurring until 200 µs after V_{CC} passes V_{PFD} (min).
3. V_{PFD} (min) to V_{SS} fall time of less than t_{FB} may cause corruption of RAM data.

Table 6. Power down/up trip points DC characteristics

Symbol	Parameter(1)		Min.	Typ.	Max.	Unit
V_{PFD}	Power-fail deselect voltage	M48Z35	4.5	4.6	4.75	V
		M48Z35Y	4.2	4.35	4.5	V
V_{SO}	Battery backup switchover voltage	M48Z35/Y		3.0		V
t_{DR}(2)	Expected data retention time		10			Years

1. Valid for ambient operating temperature: T_A = 0 to 70 °C; V_{CC} = 4.75 to 5.5 V or 4.5 to 5.5 V (except where noted).
2. At 25 °C, V_{CC} = 0 V.

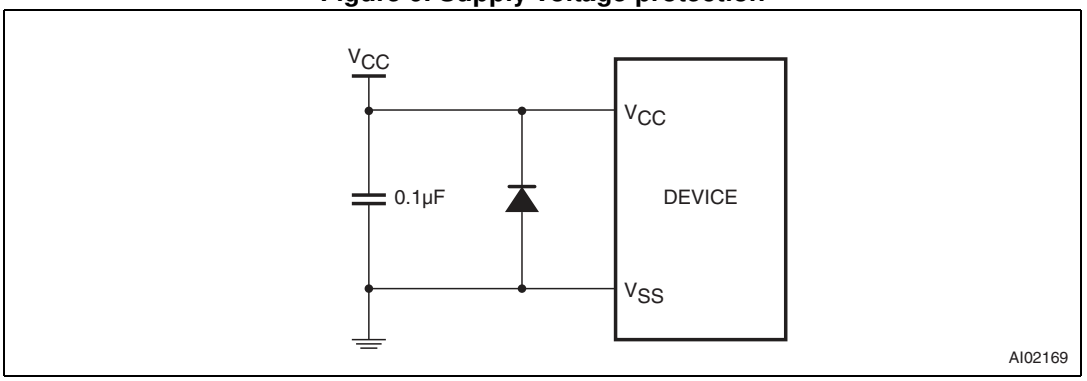
Note: All voltages referenced to V_{SS}.

3.4 V_{CC} noise and negative going transients

I_{CC} transients, including those produced by output switching, can produce voltage fluctuations, resulting in spikes on the V_{CC} bus. These transients can be reduced if capacitors are used to store energy which stabilizes the V_{CC} bus. The energy stored in the bypass capacitors will be released as low going spikes are generated or energy will be absorbed when overshoots occur. A ceramic bypass capacitor value of 0.1 µF (as shown in *Figure 9*) is recommended in order to provide the needed filtering.

In addition to transients that are caused by normal SRAM operation, power cycling can generate negative voltage spikes on V_{CC} that drive it to values below V_{SS} by as much as one volt. These negative spikes can cause data corruption in the SRAM while in battery backup mode. To protect from these voltage spikes, STMicroelectronics recommends connecting a Schottky diode from V_{CC} to V_{SS} (cathode connected to V_{CC}, anode to V_{SS}). Schottky diode 1N5817 is recommended for through hole and MBRS120T3 is recommended for surface mount.

Figure 9. Supply voltage protection



4 Maximum ratings

Stressing the device above the rating listed in the absolute maximum ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 7. Absolute maximum ratings

Symbol	Parameter		Value	Unit
T_A	Ambient operating temperature		0 to 70	°C
T_{STG}	Storage temperature (V_{CC} off, oscillator off)	SNAPHAT® top	–40 to 85	°C
		CAPHAT® DIP	–40 to 85	°C
		SOH28	–40 to 85	°C
T_{SLD} (1) (2)	Lead solder temperature for 10 seconds		260	°C
V_{IO}	Input or output voltages		–0.3 to 7	V
V_{CC}	Supply voltage		–0.3 to 7	V
I_O	Output current		20	mA
P_D	Power dissipation		1	W

1. For DIP package, soldering temperature of the IC leads is to not exceed 260 °C for 10 seconds. Furthermore, the devices shall not be exposed to IR reflow nor preheat cycles (as performed as part of wave soldering). ST recommends the devices be hand-soldered or placed in sockets to avoid heat damage to the batteries.
2. For SOH28 package, lead-free (Pb-free) lead finish: reflow at peak temperature of 260 °C (the time above 255 °C must not exceed 30 seconds).

Caution: *Negative undershoots below –0.3 V are not allowed on any pin while in the battery backup mode.*

Caution: *Do NOT wave solder SOIC to avoid damaging SNAPHAT® sockets.*

5 DC and AC parameters

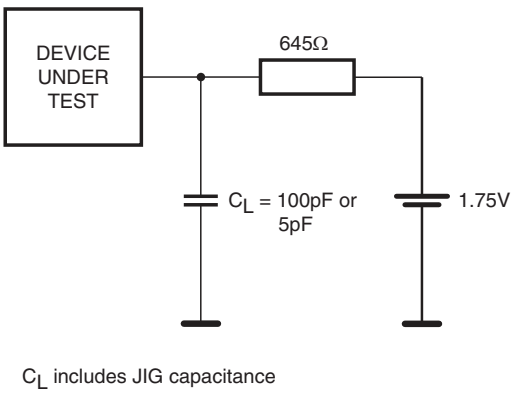
This section summarizes the operating and measurement conditions, as well as the DC and AC characteristics of the device. The parameters in the following DC and AC characteristic tables are derived from tests performed under the measurement conditions listed in *Table 8*. Designers should check that the operating conditions in their projects match the measurement conditions when using the quoted parameters.

Table 8. Operating and AC measurement conditions

Parameter	M48Z35	M48Z35Y	Unit
Supply voltage (V_{CC})	4.75 to 5.5	4.5 to 5.5	V
Ambient operating temperature (T_A)	0 to 70	0 to 70	°C
Load capacitance (C_L)	100	100	pF
Input rise and fall times	≤ 5	≤ 5	ns
Input pulse voltages	0 to 3	0 to 3	V
Input and output timing ref. voltages	1.5	1.5	V

Note: Output Hi-Z is defined as the point where data is no longer driven.

Figure 10. AC measurement load circuit



C_L includes JIG capacitance

AI03211

Table 9. Capacitance

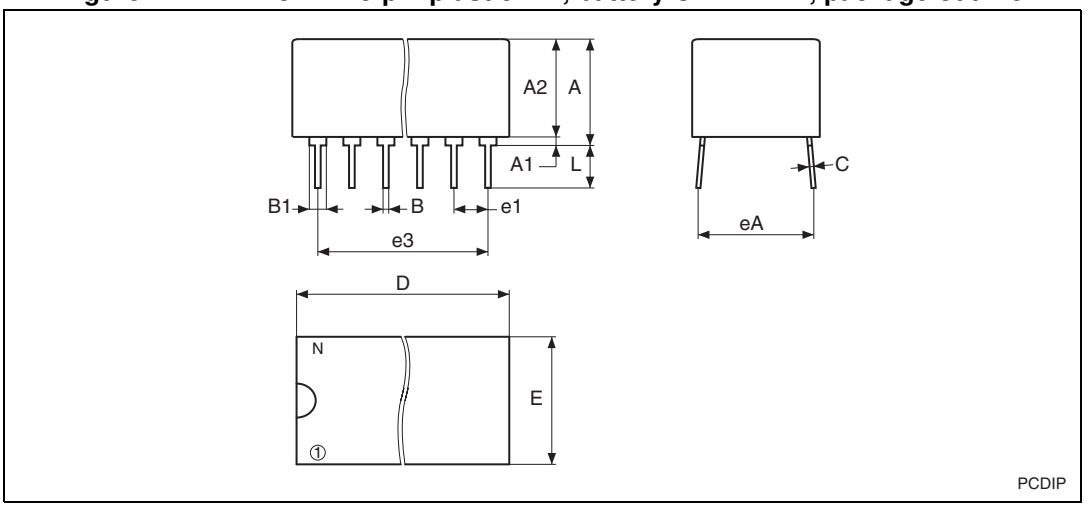
Symbol	Parameter[1][2]	Min.	Max.	Unit
C_{IN}	Input capacitance	-	10	pF
C_{IO}[3]	Input / output capacitance	-	10	pF

1. Effective capacitance measured with power supply at 5 V. Sampled only, not 100% tested.
2. Outputs deselected.
3. At 25°C.

6 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

Figure 11. PDIP 28.7 – 28-pin plastic DIP, battery CAPHAT™, package outline

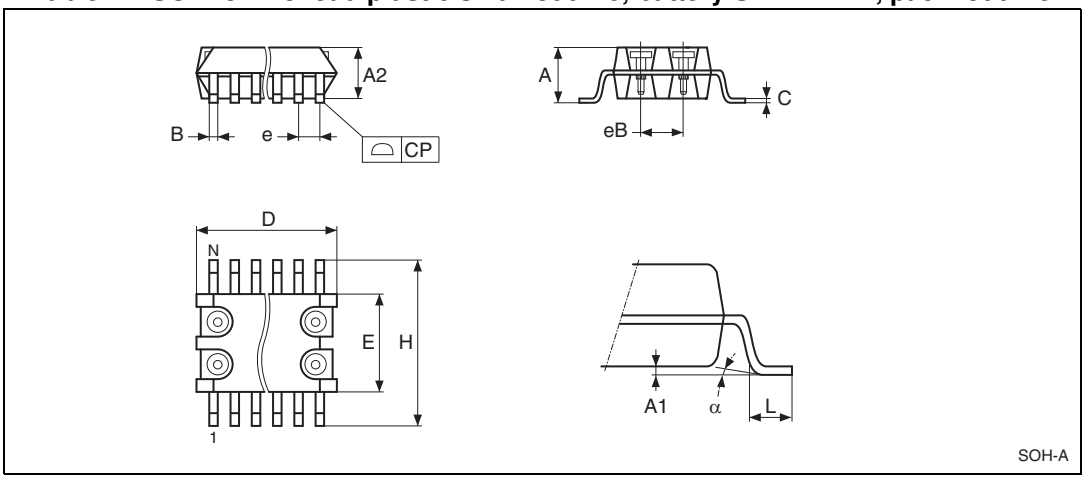


Note: Drawing is not to scale.

Table 10. PDIP 28.7 – 28 pin plastic DIP, battery CAPHAT™, package mech. data

Symb	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A		8.89	9.65		0.350	0.380
A1		0.38	0.76		0.015	0.030
A2		8.38	8.89		0.330	0.350
B		0.38	0.53		0.015	0.021
B1		1.14	1.78		0.045	0.070
C		0.20	0.31		0.008	0.012
D		39.37	39.88		1.550	1.570
E		17.83	18.34		0.702	0.722
e1		2.29	2.79		0.090	0.110
e3	33.02			1.3		
eA		15.24	16.00		0.600	0.630
L		3.05	3.81		0.120	0.150
N	28			28		

Table 11. SOH28 – 28-lead plastic small outline, battery SNAPHAT®, pack. outline

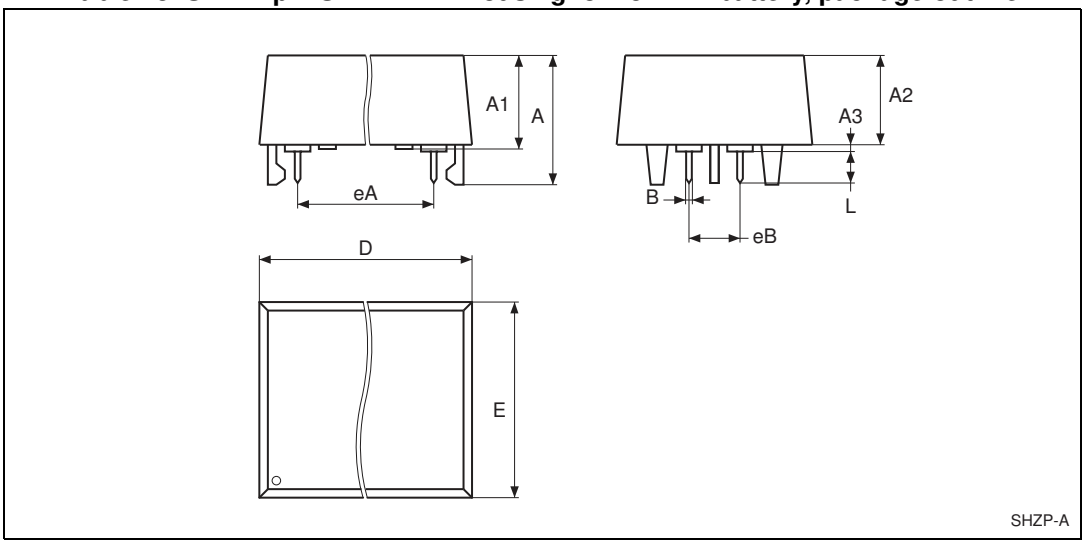


Note: Drawing is not to scale.

Table 12. SOH28 – 28-lead plastic small outline, battery SNAPHAT®, pack. mech. data

Symbol	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A			3.05			0.120
A1		0.05	0.36		0.002	0.014
A2		2.34	2.69		0.092	0.106
B		0.36	0.51		0.014	0.020
C		0.15	0.32		0.006	0.012
D		17.71	18.49		0.697	0.728
E		8.23	8.89		0.324	0.350
e	1.27	–	–	0.050	–	–
eB		3.20	3.61		0.126	0.142
H		11.51	12.70		0.453	0.500
L		0.41	1.27		0.016	0.050
a		0°	8°		0°	8°
N	28			28		
CP			0.10			0.004

Table 13. SH – 4-pin SNAPHAT® housing for 48 mAh battery, package outline



Note: Drawing is not to scale.

Table 14. SH – 4-pin SNAPHAT® housing for 48 mAh battery, pack. mech. data

Symbol	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A			9.78			0.385
A1		6.73	7.24		0.265	0.285
A2		6.48	6.99		0.255	0.275
A3			0.38			0.015
B		0.46	0.56		0.018	0.022
D		21.21	21.84		0.835	0.860
E		14.22	14.99		0.560	0.590
eA		15.55	15.95		0.612	0.628
eB		3.20	3.61		0.126	0.142
L		2.03	2.29		0.080	0.090

7 Part numbering

Table 15. Ordering information

Order code	Package	Temperature range	Speed	Supply voltage
M48Z35-70PC1	PDIP 28.7	0 to 70 °C	70	V_{CC} = 4.75 to 5.5 V; V_{PFD} = 4.5 to 4.75 V
M48Z35Y-70PC1				V_{CC} = 4.5 to 5.5 V; V_{PFD} = 4.2 to 4.5 V
M48Z35Y-70MH1F	SOH28			V_{CC} = 4.75 to 5.5 V; V_{PFD} = 4.5 to 4.75 V

Caution: Do not place the SNAPHAT battery package “M4Zxx-BR00SH1” in conductive foam as it will drain the lithium button-cell battery.

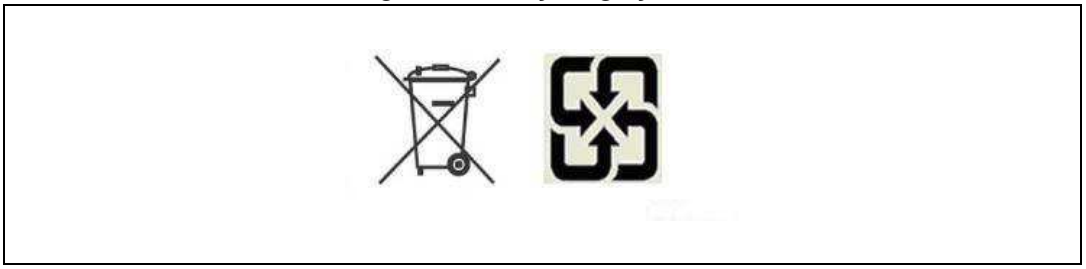
For other options, or for more information on any aspect of this device, please contact the ST sales office nearest you.

Table 16. SNAPHAT® battery table

Part number	Description	Package
M4Z28-BR00SH1	Lithium battery (48 mAh) SNAPHAT®	SH
M4Z32-BR00SH1	Lithium battery (120 mAh) SNAPHAT®	SH

8 Environmental information

Figure 12. Recycling symbols



This product contains a non-rechargeable lithium (lithium carbon monofluoride chemistry) button cell battery fully encapsulated in the final product.

Recycle or dispose of batteries in accordance with the battery manufacturer's instructions and local/national disposal and recycling regulations.

9 Revision history

Table 17. Document revision history

Date	Revision	Changes
Aug-1999	1	First issue
21-Apr-2000	1.1	SH and SH28 packages for 2-pin and 2-socket removed
10-May-2001	2	Reformatted; added temperature information (Table 9, 10, 3, 4, 5, 6)
29-May-2002	2.1	Modified reflow time and temperature footnotes (Table 7)
02-Apr-2003	3	v2.2 template applied; test condition updated (Table 6)
03-Mar-2004	4	Reformatted; updated with Lead-free information (Table 7, 15)
20-Aug-2004	5	Reformatted; remove references to ‘crystal’ (cover page)
09-Jun-2005	6	Removal of SNAPHAT®, industrial temperature sales types (Table 3, 4, 5, 6, 7, 8, 10, 15).
02-Nov-2007	7	Reformatted; added lead-free second level interconnect information to cover page and Section 5: Package mechanical data; updated Table 7, 15, 16
25-Mar-2009	8	Updated Table 7, text in Section 5: Package mechanical data; added Section 7: Environmental information.
19-Aug-2010	9	Updated Section 3, Table 11; reformatted document.
07-Jun-2011	10	Updated footnote 1 of Table 7: Absolute maximum ratings; updated Section 7: Environmental information.
06-Oct-2020	11	Added Table 15: Ordering information. Updated package name.
16-Apr-2024	12	Updated *Figure 3* and *Table 6*.

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