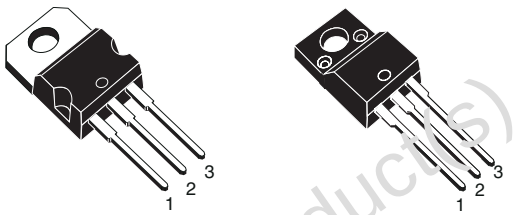
IRF640
IRF640FP

N-channel 200V - 0.15Ω - 18A TO-220/TO-220FP
Mesh overlay™ Power MOSFET

General features

Type	V_{DSS}	$R_{DS(on)}$	I_D
IRF640	200V	<0.18Ω	18A
IRF640FP	200V	<0.18Ω	18A

- Extremely high dv/dt capability
- Very low intrinsic capacitances
- Gate charge minimized

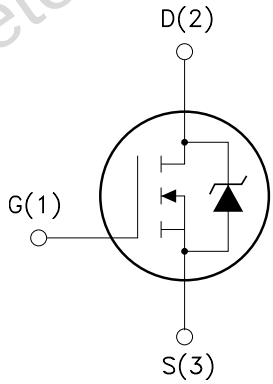


TO-220 TO-220FP

Description

This power MOSFET is designed using the company's consolidated strip layout-based MESH OVERLAY™ process. This technology matches and improves the performances compared with standard parts from various sources.

Internal schematic diagram



Applications

- Switching application

Obsolete Product(s) - Obsolete Product(s)
Obsolete Product(s) - Obsolete Product(s)

Order codes

Part number	Marking	Package	Packaging
IRF640	IRF640	TO-220	Tube
IRF640FP	IRF640FP	TO-220FP	Tube

Contents

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2 Electrical characteristics 4

2.1 Electrical characteristics (curves) 6

3 Test circuit 9

4 Package mechanical data 10

5 Revision history 13

Obsolete Product(s) - Obsolete Product(s)
Obsolete Product(s) - Obsolete Product(s)

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220	TO-220FP	
V_{DS}	Drain-source voltage (V_{GS} = 0)	200		V
V_{GS}	Gate-source voltage	± 20		V
I_D	Drain current (continuous) at T_C = 25°C	18	18(1)	A
I_D	Drain current (continuous) at T_C=100°C	11	11(1)	A
I_{DM}(2)	Drain current (pulsed)	72	72(1)	A
P_{TOT}	Total dissipation at T_C = 25°C	125	40	W
	Derating factor	1.0	0.32	W/°C
dv/dt(3)	Peak diode recovery voltage slope	5	5	V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1s; Tc= 25°C)	--	2500	V
T_J T_{stg}	Operating junction temperature Storage temperature	150 -65 to 150		°C

1. Limited only by maximum temperature allowed
2. Pulse width limited by safe operating area
3. I_{SD} ≤8A, di/dt ≤300A/µs, V_{DD} ≤$V_{(BR)DSS}$, Tj ≤T_{JMAX}

Table 2. Thermal data

Symbol	Parameter	Value		Unit
		TO-220	TO-220FP	
$R_{thj\text{-}case}$	Thermal resistance junction-case Max	1.0	3.12	°C/W
$R_{thj\text{-}a}$	Thermal resistance junction-ambient Max	62.5		°C/W
Rthc-sink	Thermal resistance case-sink typ	0.5		°C/W
T_l	Maximum lead temperature for soldering purpose	300		°C

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AS}	Avalanche current, repetitive or not-repetitive (pulse width limited by Tj Max)	18	A
E_{AS}	Single pulse avalanche energy (starting Tj=25°C, Id=Iar, Vdd=50V)	280	mJ

Obsolete Product(s) - Obsolete Product(s)

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250 µA, V_{GS}= 0	200			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max rating, V_{DS} = Max rating @125°C			1 10	µA µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ±20V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS}= V_{GS}, I_D = 250µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS}= 10V, I_D= 9A		0.15	0.18	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} > $I_{D(on)}$ x $R_{DS(on)max}$, I_D = 9A	7	11		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} =25V, f=1 MHz, V_{GS}=0		1200 200 60	1560 260 80	pF pF pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD}=160V, I_D = 18A V_{GS} =10V		55 10 21	72	nC nC nC

1. Pulsed: pulse duration=300µs, duty cycle 1.5%

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	V_{DD} = 100V, I_D = 9A, R_G = 4.7Ω, V_{GS} = 10V (see Figure 14)		13 27	17 35	ns ns
$t_{r(Voff)}$ t_f t_c	Off-voltage rise time fall time cross-over time	V_{DD}=160V, I_D=18A, R_G=4.7Ω, V_{GS}=10V (see Figure 16)		21 25 50	27 32 65	ns ns ns

Obsolete Product(s) - Obsolete Product(s)

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current				18	A
I_{SDM}(1)	Source-drain current (pulsed)				72	A
V_{SD}(2)	Forward on voltage	I_{SD}=18A, V_{GS}=0			1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD}=18A, di/dt = 100A/µs, V_{DD}=50V, Tj=150°C (see Figure 16)		240 1.8 15		ns µC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300µs, duty cycle 1.5%

Obsolete Product(s) - Obsolete Product(s)
Obsolete Product(s) - Obsolete Product(s)

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area for TO-220

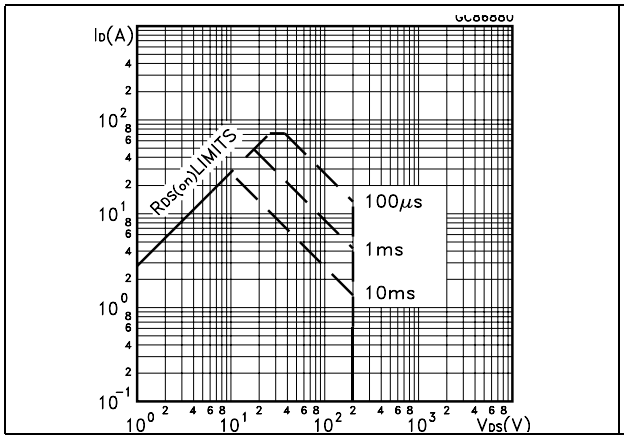


Figure 2. Thermal impedance for TO-220

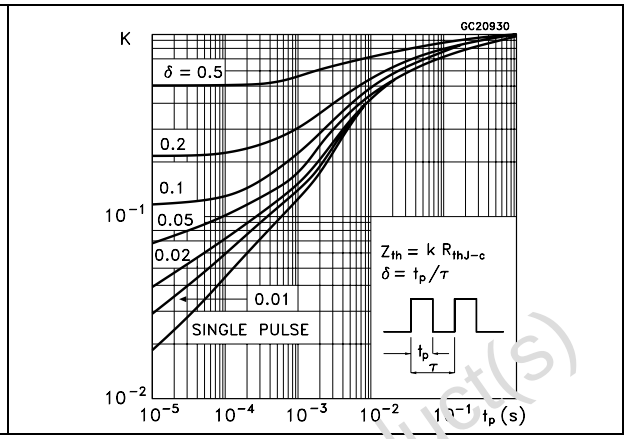


Figure 3. Safe operating area for TO-220/FP

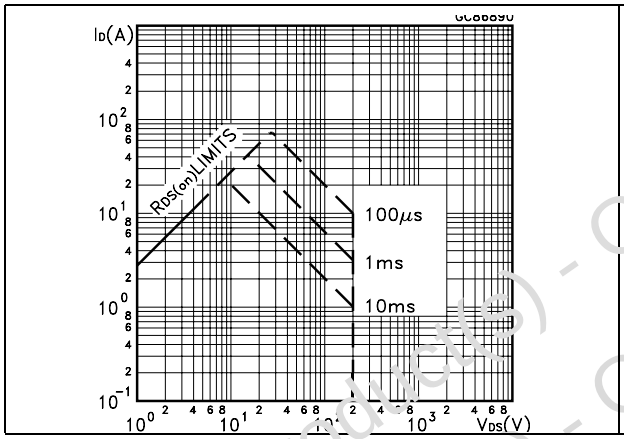


Figure 4. Thermal impedance for TO-220/FP

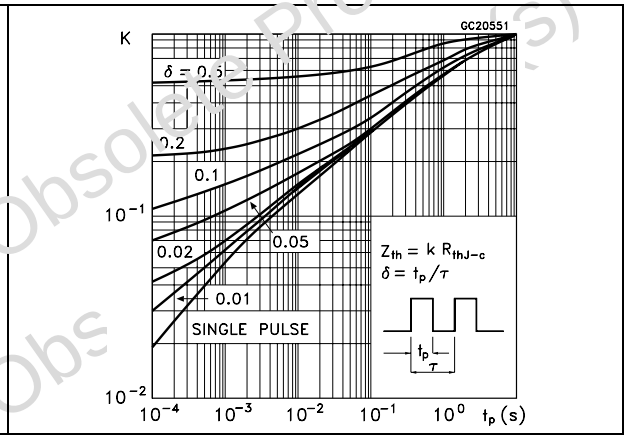


Figure 5. Output characterisics

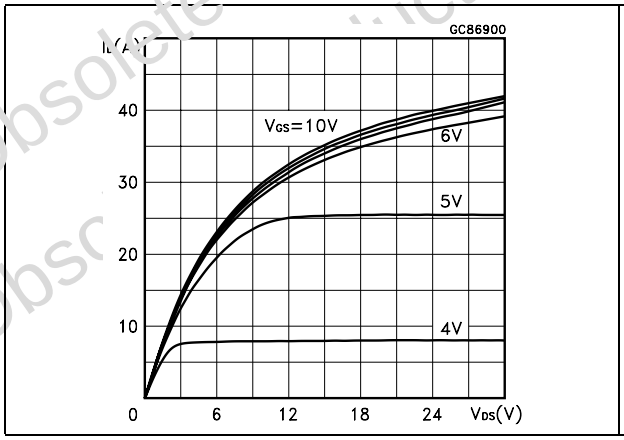
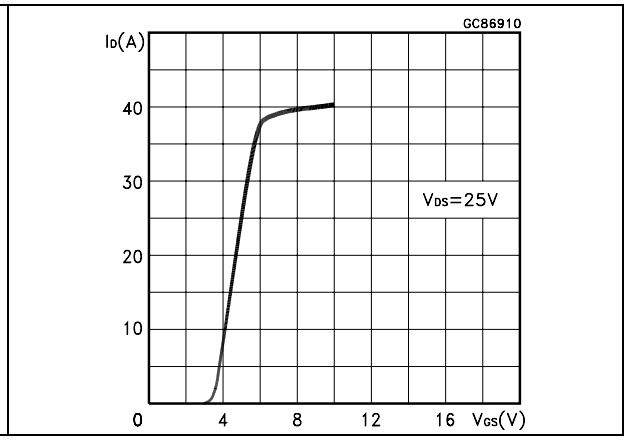


Figure 6. Transfer characteristics



Obsolete Product(s) - Obsolete Product(s)

Figure 7. Transconductance

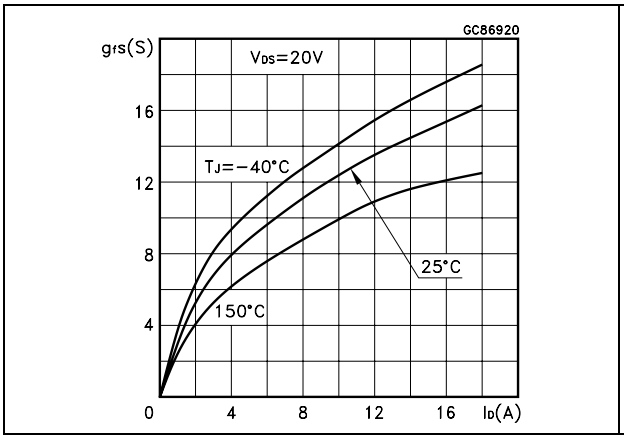


Figure 8. Static drain-source on resistance

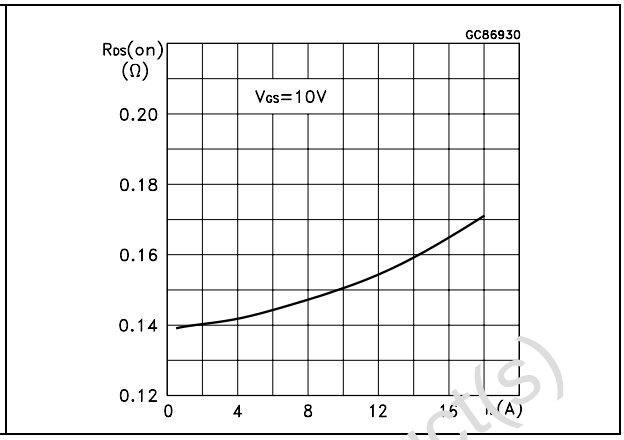


Figure 9. Gate charge vs gate-source voltage

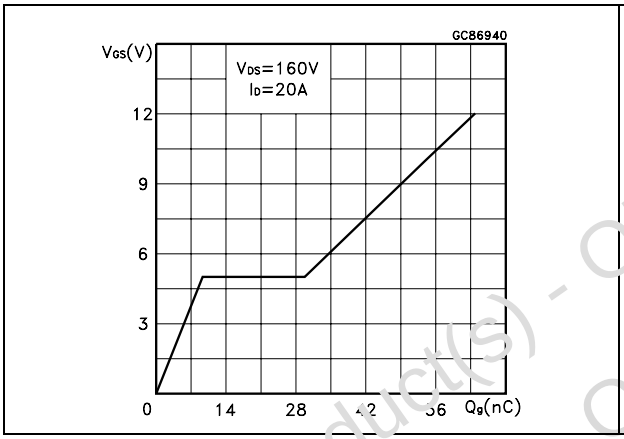


Figure 10. Capacitance variations

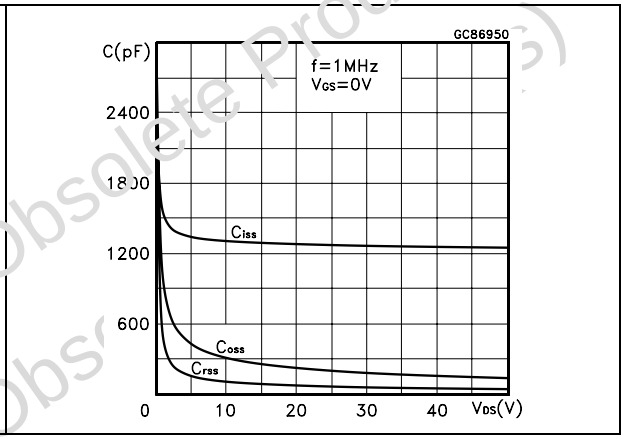


Figure 11. Normalized gate threshold voltage vs temperature

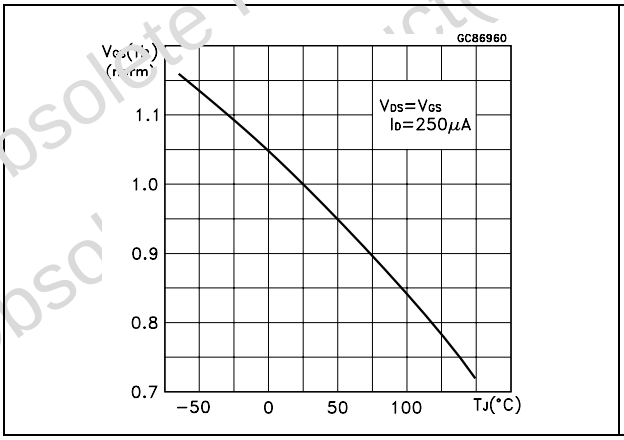
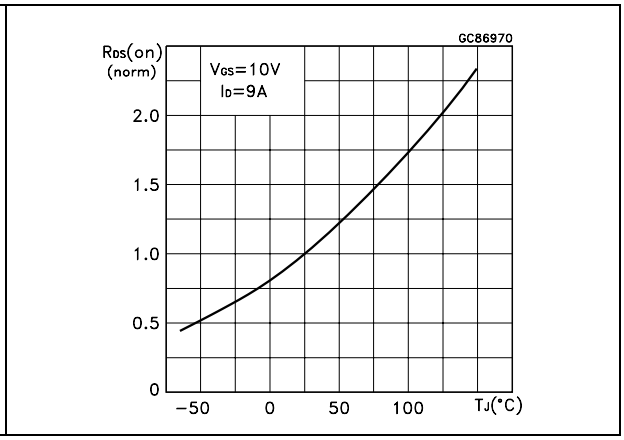
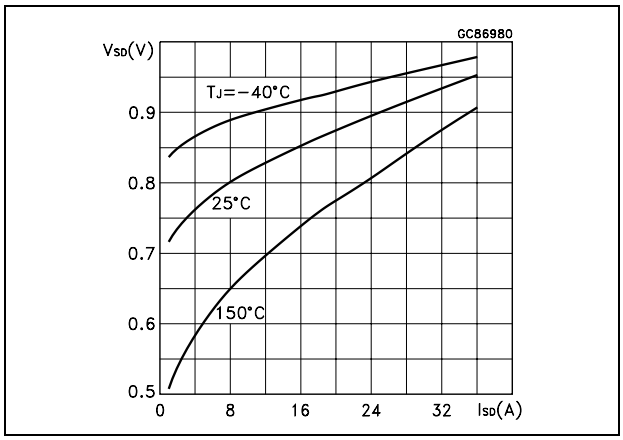


Figure 12. Normalized on resistance vs temperature



Obsolete Product(s) - Obsolete Product(s)

Figure 13. Source-drain diode forward characteristics



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Obsolete Product(s) - Obsolete Product(s)

3 Test circuit

Figure 14. Switching times test circuit for resistive load

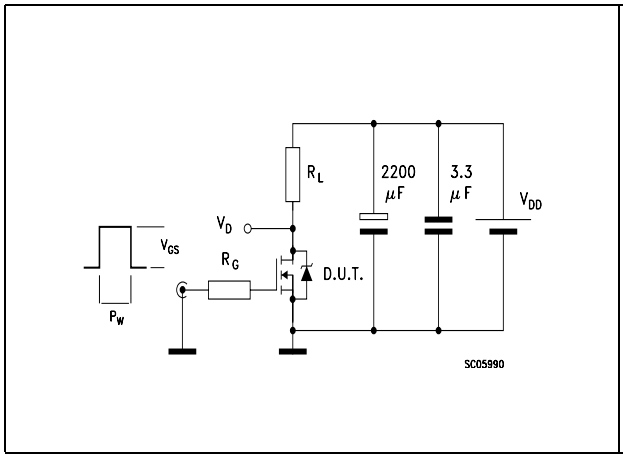


Figure 15. Gate charge test circuit

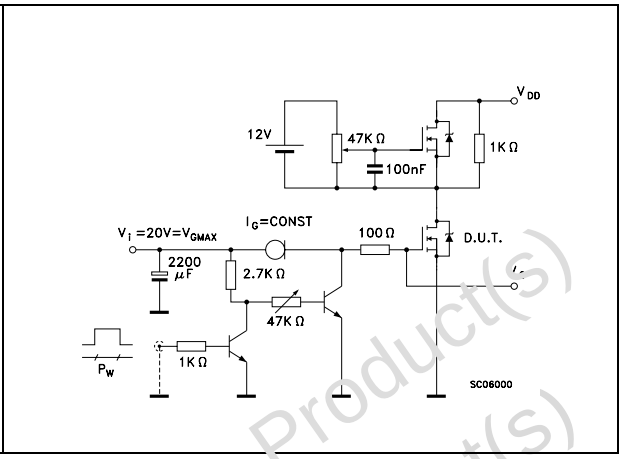


Figure 16. Test circuit for inductive load switching and diode recovery times

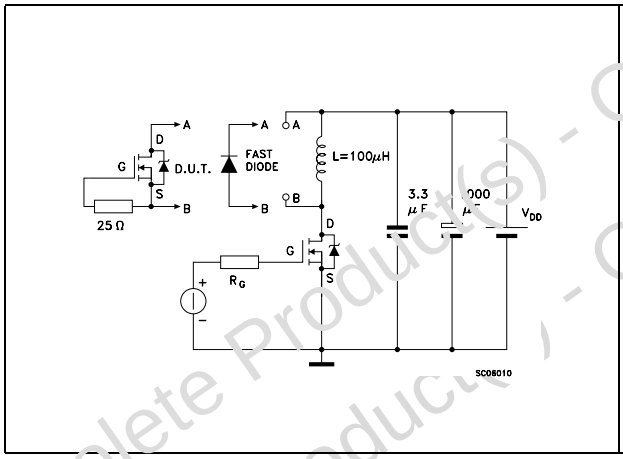


Figure 17. Unclamped Inductive load test circuit

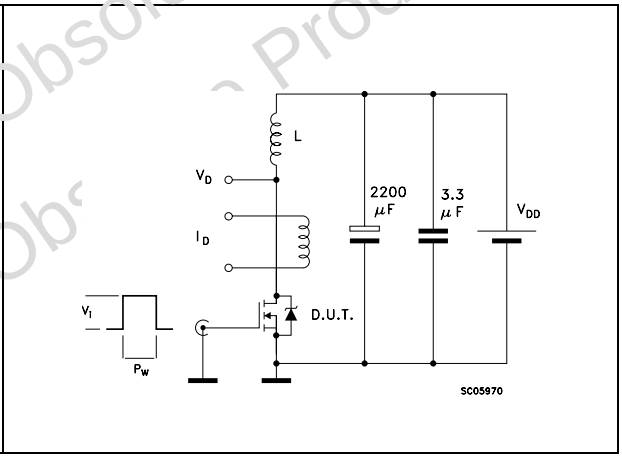


Figure 18. Unclamped inductive waveform

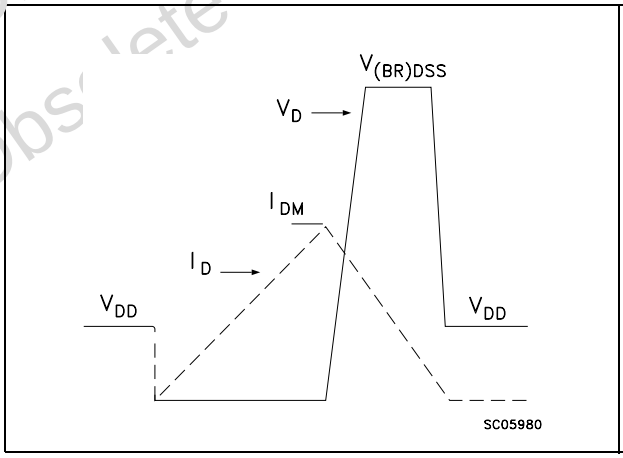
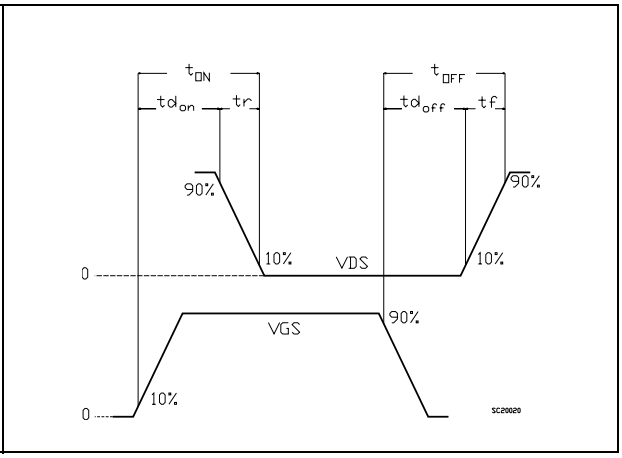


Figure 19. Switching time waveform



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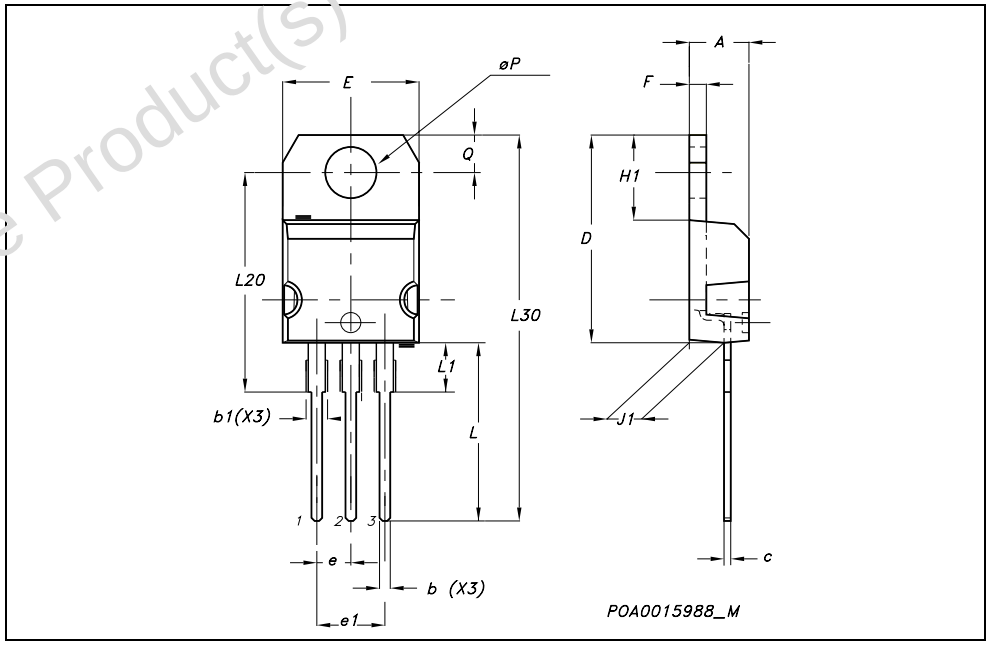
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

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TO-220 MECHANICAL DATA

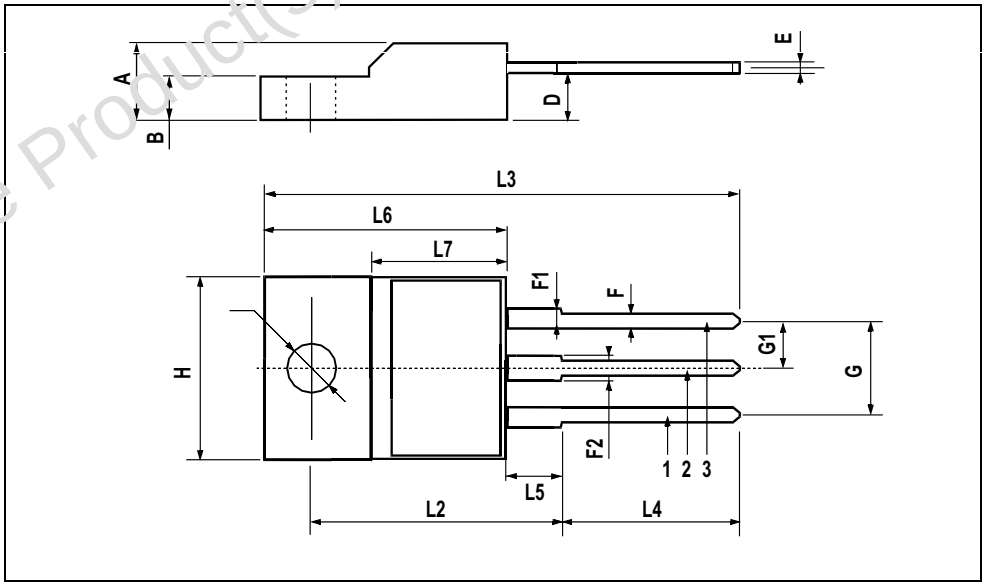
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
øP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



Obsolete Product(s) - Obsolete Product(s)

TO-220FP MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.7	0.017		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.7	0.045		0.067
F2	1.15		1.7	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	.0385		0.417
L5	2.9		3.6	0.114		0.141
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
Ø	3		3.2	0.118		0.126



Obsolete Product(s) - Obsolete Product(s)

5 Revision history

Table 8. revision history

Date	Revision	Changes
09-Sep-2004	8	Final version
04-Sep-2006	9	New template, no content change

Obsolete Product(s) - Obsolete Product(s)
Obsolete Product(s) - Obsolete Product(s)

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