M41T56

Serial real-time clock (RTC) with 56 bytes NVRAM

Features

- Counters for seconds, minutes, hours, day, date, month, years, and century
- 32 KHz crystal oscillator integrating load capacitance (12.5 pF) providing exceptional oscillator stability and high crystal series resistance operation
- Serial interface supports I^2C bus (100 kHz protocol)
- Ultra-low battery supply current of 450 nA (typ at 3 V)
- 5 V ±10% supply voltage
- Timekeeping down to 2.5 V
- Automatic power-fail detect and switch circuitry
- 56 bytes of general purpose RAM
- Software clock calibration to compensate crystal deviation due to temperature
- Automatic leap year compensation
- Operating temperature of –40 °C to 85 °C
- Available in an 8-lead, 150-mil, plastic SOIC (SO8)
- RoHS compliant
  - Lead-free second level interconnect



SO8
150-mil width

Contents

1 **Description** 5

2 **Operation** 7

2.1 2-wire bus characteristics 7

2.1.1 Bus not busy 7

2.1.2 Start data transfer 7

2.1.3 Stop data transfer 8

2.1.4 Data valid 8

2.1.5 Acknowledge 8

2.2 Read mode 10

2.3 Write mode 12

2.4 Data retention mode 12

3 **Clock operation** 13

3.1 Clock calibration 14

3.2 Output driver pin 15

3.3 Initial power-on defaults 15

4 **Maximum ratings** 16

5 **DC and AC parameters** 17

6 **Package mechanical data** 20

7 **Part numbering** 24

8 **References** 25

9 **Revision history** 26

List of tables

Table 1. Signal names . . . 6
Table 2. AC characteristics . . . 10
Table 3. Register map . . . 13
Table 4. Absolute maximum ratings . . . 16
Table 5. Operating and AC measurement conditions . . . 17
Table 6. Capacitance . . . 17
Table 7. DC characteristics . . . 18
Table 8. Crystal electrical characteristics . . . 18
Table 9. Power down/up mode AC characteristics . . . 19
Table 10. Power down/up trip points DC characteristics . . . 19
Table 11. SO8 – 8-pin plastic small outline, package mechanical data . . . 21
Table 12. Carrier tape dimensions for SO8 package (150-mil body width) . . . 22
Table 13. Reel dimensions for 12 mm carrier tape - SO8 package (150-mil body width) . . . 23
Table 14. Ordering information scheme . . . 24
Table 15. Document revision history . . . 26

List of figures

Figure 1. Logic diagram . . . 5
Figure 2. 8-pin SOIC connections . . . 6
Figure 3. M41T56 block diagram . . . 6
Figure 4. Serial bus data transfer sequence . . . 8
Figure 5. Acknowledge sequence . . . 9
Figure 6. Bus timing requirements sequence . . . 9
Figure 7. Slave address location . . . 11
Figure 8. Read mode sequence . . . 11
Figure 9. Alternative read mode sequence . . . 11
Figure 10. Write mode sequence . . . 12
Figure 11. Crystal accuracy across temperature . . . 15
Figure 12. Clock calibration . . . 15
Figure 13. AC measurement I/O waveform . . . 17
Figure 14. Power down/up mode AC waveforms . . . 18
Figure 15. SO8 – 8-pin plastic small package outline . . . 21
Figure 16. Carrier tape for SO8 package (150-mil body width) . . . 22
Figure 17. Reel schematic . . . 23

1 Description

The M41T56 is a low-power, serial real-time clock (RTC) with 56 bytes of NVRAM. A built-in 32,768 Hz oscillator (external crystal controlled) and the first 8 bytes of the RAM are used for the clock/calendar function and are configured in binary coded decimal (BCD) format. Addresses and data are transferred serially via a two-line, bidirectional bus. The built-in address register is incremented automatically after each WRITE or READ data byte.

The M41T56 clock has a built-in power sense circuit which detects power failures and automatically switches to the battery supply during power failures. The energy needed to sustain the RAM and clock operations can be supplied from a small lithium coin cell.

Typical data retention time is in excess of 10 years with a 50 mAh, 3 V lithium cell. The M41T56 is supplied in an 8-lead plastic SOIC package.

Figure 1. Logic diagram

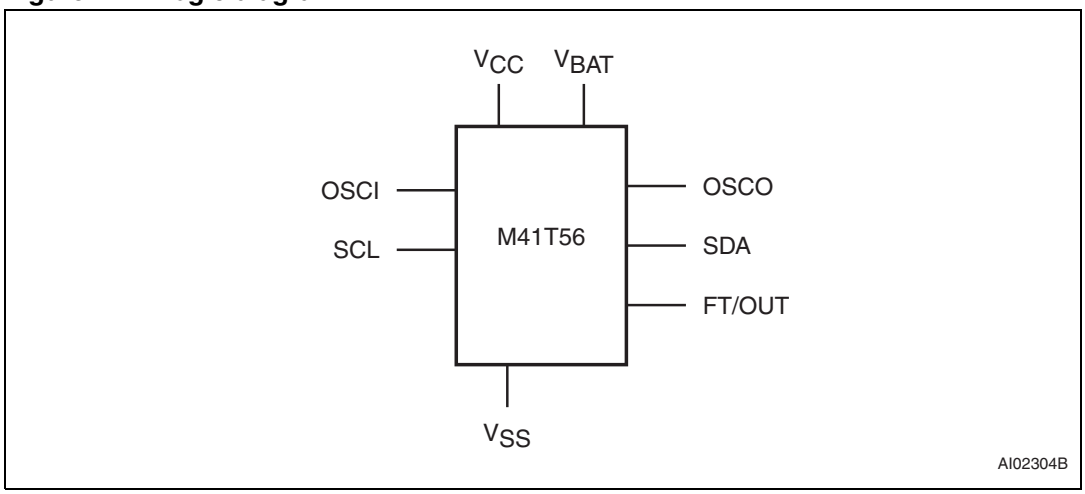


Table 1. Signal names

OSCI	Oscillator input
OCSO	Oscillator output
FT/OUT	Frequency test / output driver (open drain)
SDA	Serial data address input / output
SCL	Serial clock
V_{BAT}	Battery supply voltage
V_{CC}	Supply voltage
V_{SS}	Ground

Figure 2. 8-pin SOIC connections

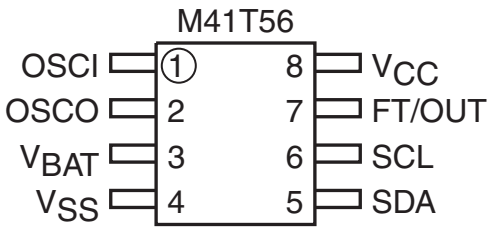
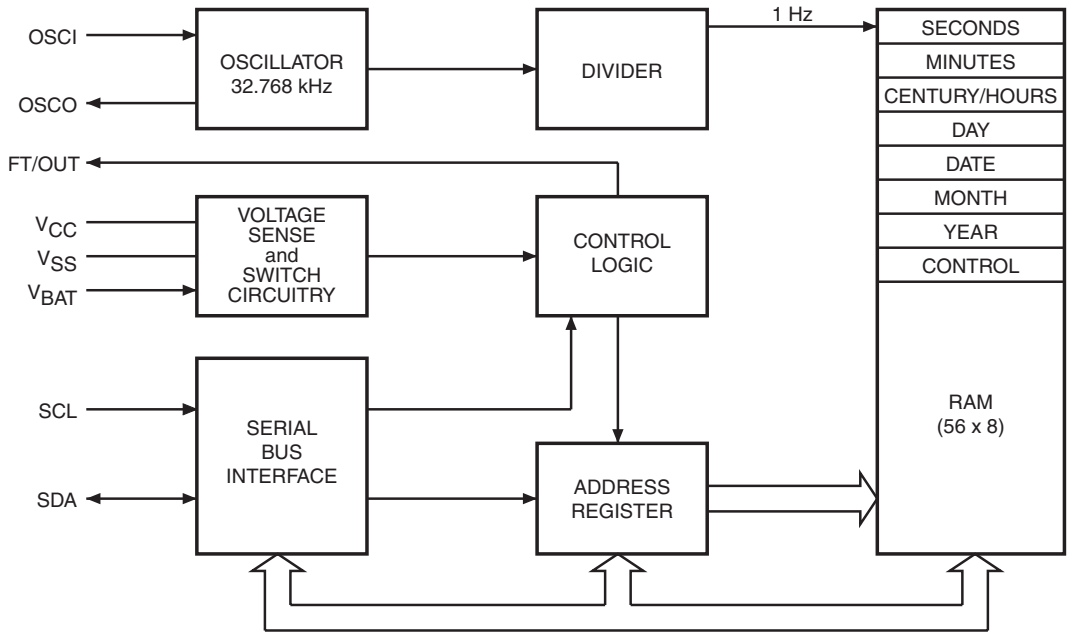


Figure 3. M41T56 block diagram



2 Operation

The M41T56 clock operates as a slave device on the serial bus. Access is obtained by implementing a start condition followed by the correct slave address (D0h). The 64 bytes contained in the device can then be accessed sequentially in the following order:

1. Seconds register
2. Minutes register
3. Century/hours register
4. Day register
5. Date register
6. Month register
7. Years register
8. Control register
9. RAM

The clock continually monitors V_{CC} for an out of tolerance condition. Should V_{CC} fall below V_{PFD}, the device terminates an access in progress and resets the device address counter. Inputs to the device will not be recognized at this time to prevent erroneous data from being written to the device from an out of tolerance system. When V_{CC} falls below V_{BAT}, the device automatically switches over to the battery and powers down into an ultra low current mode of operation to conserve battery life. Upon power-up, the device switches from battery to V_{CC} at V_{BAT} and recognizes inputs when V_{CC} goes above V_{PFD} volts.

2.1 2-wire bus characteristics

This bus is intended for communication between different ICs. It consists of two lines: one bidirectional for data signals (SDA) and one for clock signals (SCL). Both the SDA and the SCL lines must be connected to a positive supply voltage via a pull-up resistor.

The following protocol has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high.
- Changes in the data line while the clock line is high will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:

2.1.1 Bus not busy

Both data and clock lines remain high.

2.1.2 Start data transfer

A change in the state of the data line, from high to low, while the clock is high, defines the START condition.

2.1.3 Stop data transfer

A change in the state of the data line, from low to high, while the clock is high, defines the STOP condition.

2.1.4 Data valid

The state of the data line represents valid data when after a start condition, the data line is stable for the duration of the high period of the clock signal. The data on the line may be changed during the low period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a start condition and terminated with a stop condition. The number of data bytes transferred between the start and stop conditions is not limited. The information is transmitted byte-wide and each receiver acknowledges with a ninth bit.

By definition, a device that gives out a message is called “transmitter,” the receiving device that gets the message is called “receiver.” The device that controls the message is called “master.” The devices that are controlled by the master are called “slaves.”

2.1.5 Acknowledge

Each byte of eight bits is followed by one acknowledge bit. This acknowledge bit is a low level put on the bus by the receiver, whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed is obliged to generate an acknowledge after the reception of each byte. Also, a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is a stable low during the high period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master receiver must signal an end-of-data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this case, the transmitter must leave the data line high to enable the master to generate the STOP condition.

Figure 4. Serial bus data transfer sequence

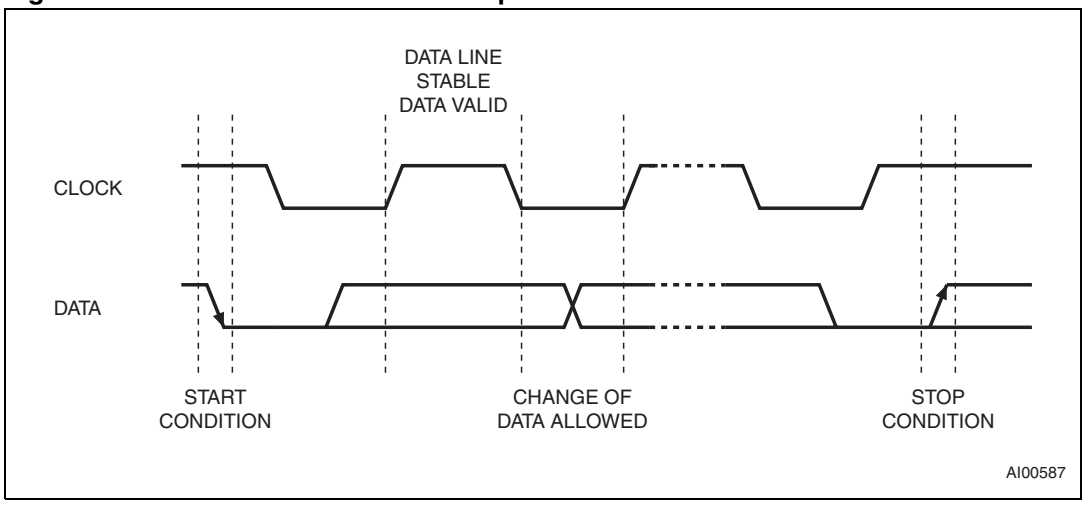


Figure 5. Acknowledge sequence

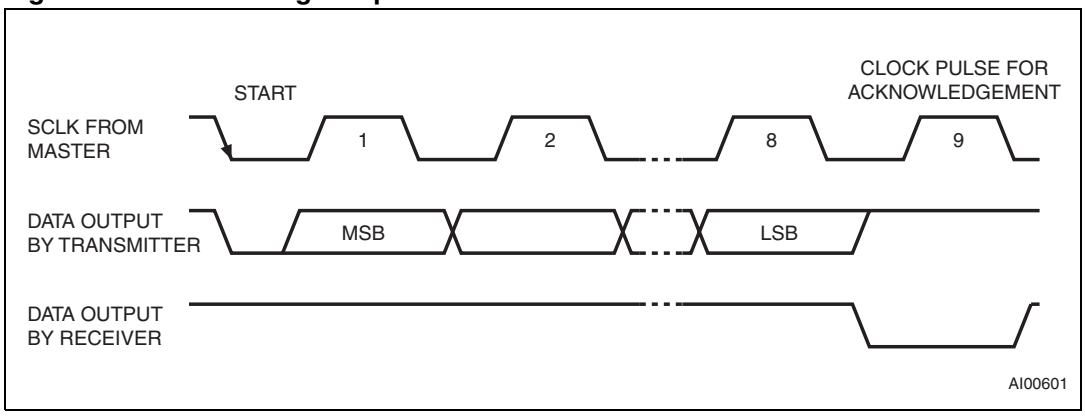


Figure 6. Bus timing requirements sequence

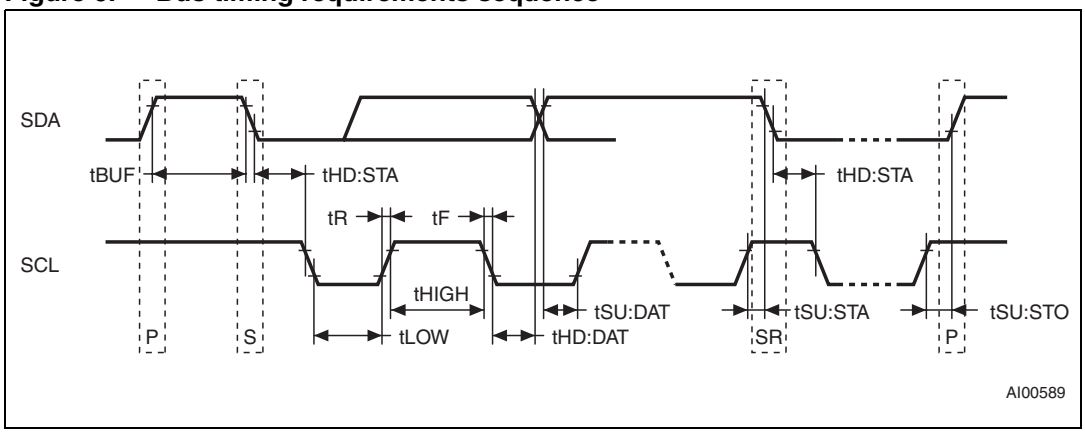


Table 2. AC characteristics

Symbol	Parameter[1]	Min	Max	Unit
f_{SCL}	SCL clock frequency	0	100	kHz
t_{LOW}	Clock low period	4.7		µs
t_{HIGH}	Clock high period	4		µs
t_R	SDA and SCL rise time		1	µs
t_F	SDA and SCL fall time		300	ns
$t_{HD:STA}$	START condition hold time (after this period the first clock pulse is generated)	4		µs
$t_{SU:STA}$	START condition setup time (only relevant for a repeated start condition)	4.7		µs
$t_{SU:DAT}$	Data setup time	250		ns
$t_{HD:DAT}$[2]	Data hold time	0		µs
$t_{SU:STO}$	STOP condition setup time	4.7		µs
t_{BUF}	Time the bus must be free before a new transmission can start	4.7		µs

1. Valid for ambient operating temperature: T_A = –40 to 85 °C; V_{CC} = 4.5 to 5.5 V (except where noted).
2. Transmitter must internally provide a hold time to bridge the undefined region (300 ns max.) of the falling edge of SCL.

2.2 Read mode

In this mode, the master reads the M41T56 slave after setting the slave address (see *Figure 7 on page 11* and *Figure 8 on page 11*). Following the WRITE mode control bit (R/$\overline{W}$ = 0) and the acknowledge bit, the word address A_n is written to the on-chip address pointer. Next the START condition and slave address are repeated, followed by the READ mode control bit (R/$\overline{W}$ = 1). At this point, the master transmitter becomes the master receiver. The data byte which was addressed will be transmitted and the master receiver will send an acknowledge bit to the slave transmitter. The address pointer is only incremented on reception of an acknowledge bit. The M41T56 slave transmitter will now place the data byte at address A_n + 1 on the bus. The master receiver reads and acknowledges the new byte and the address pointer is incremented to A_n + 2. This cycle of reading consecutive addresses will continue until the master receiver sends a STOP condition to the slave transmitter.

An alternate READ mode may also be implemented, whereby the master reads the M41T56 slave without first writing to the (volatile) address pointer. The first address that is read is the last one stored in the pointer, see *Figure 9 on page 11*.

Figure 7. Slave address location

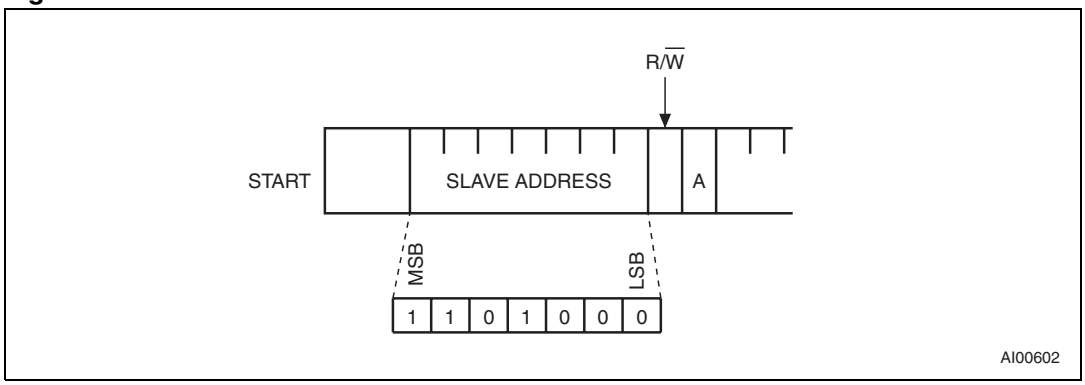


Figure 8. Read mode sequence

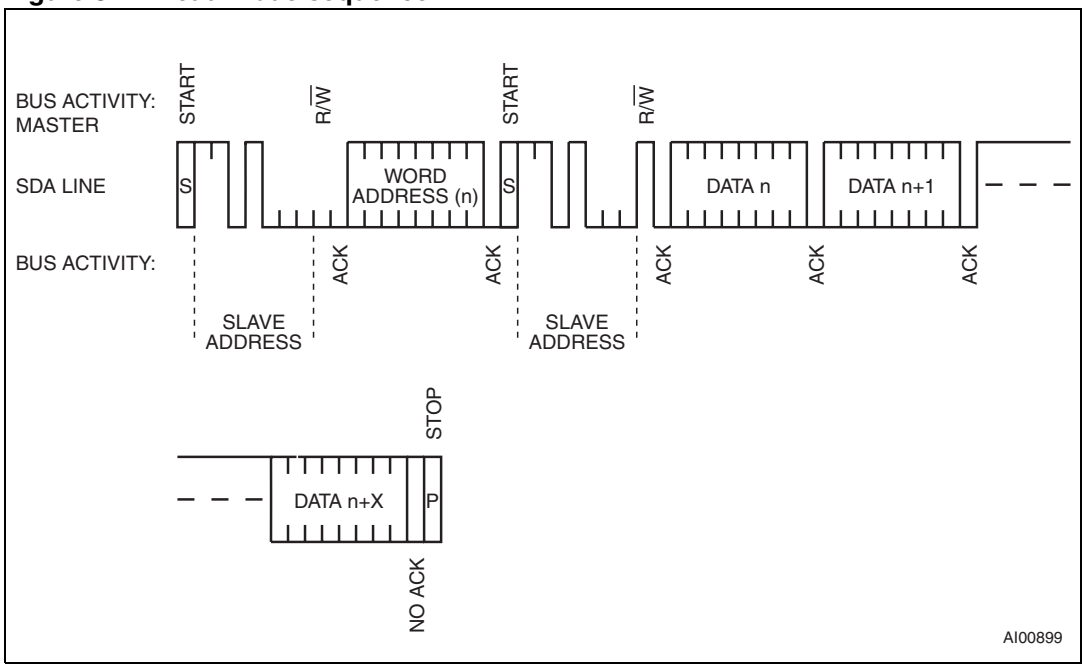
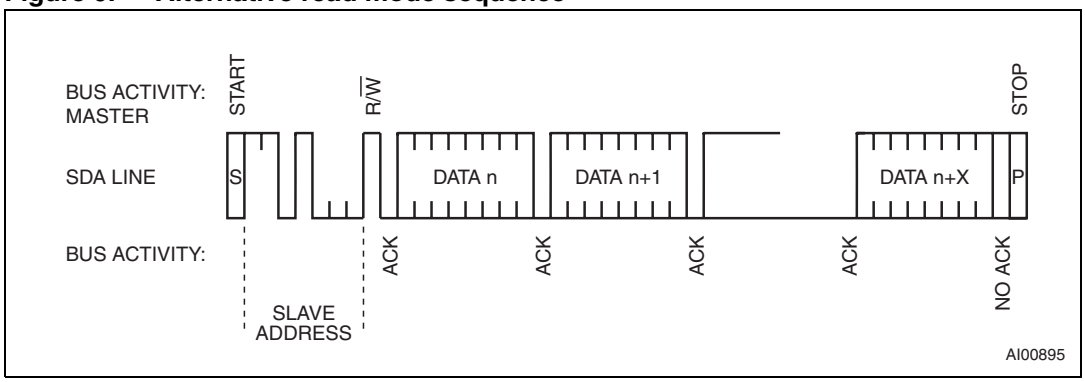


Figure 9. Alternative read mode sequence



2.3 Write mode

In this mode the master transmitter transmits to the M41T56 slave receiver. Bus protocol is shown in *Figure 10 on page 12*. Following the START condition and slave address, a logic '0' (R/$\overline{W}$ = 0) is placed on the bus and indicates to the addressed device that word address A_n will follow and is to be written to the on-chip address pointer. The data word to be written to the memory is strobed in next and the internal address pointer is incremented to the next memory location within the RAM on the reception of an acknowledge clock. The M41T56 slave receiver will send an acknowledge clock to the master transmitter after it has received the slave address and again after it has received the word address and each data byte (see *Figure 7 on page 11*).

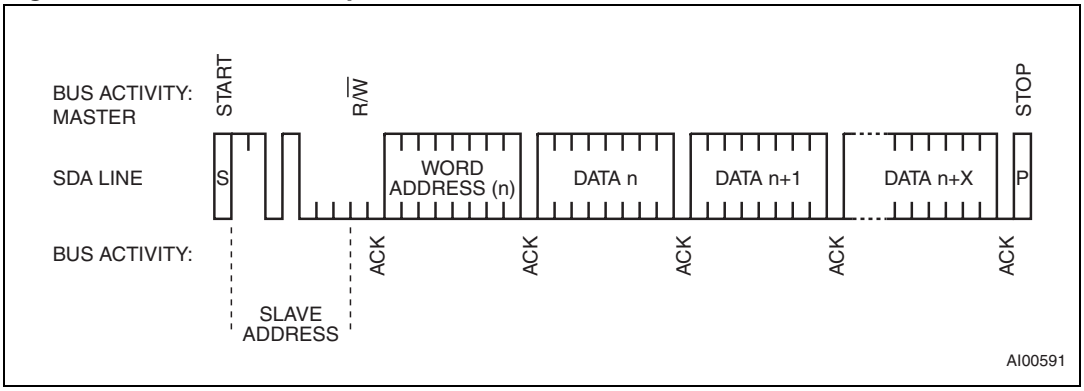
2.4 Data retention mode

With valid V_{CC} applied, the M41T56 can be accessed as described above with READ or WRITE cycles. Should the supply voltage decay, the M41T56 will automatically deselect, write protecting itself when V_{CC} falls between V_{PFD} (max) and V_{PFD} (min). This is accomplished by internally inhibiting access to the clock registers and SRAM. When V_{CC} falls below the battery backup switchover voltage (V_{SO}), power input is switched from the V_{CC} pin to the battery and the clock registers and SRAM are maintained from the attached battery supply.

All outputs become high impedance. On power up, when V_{CC} returns to a nominal value, write protection continues for t_{REC}.

For a further more detailed review of battery lifetime calculations, please see application note AN1012.

Figure 10. Write mode sequence



3 Clock operation

The eight byte clock register (see *Table 3*) is used to both set the clock and to read the date and time from the clock, in a binary coded decimal format. Seconds, minutes, and hours are contained within the first three registers. Bits D6 and D7 of clock register 2 (hours register) contain the century enable bit (CEB) and the century bit (CB). Setting CEB to a '1' will cause CB to toggle, either from '0' to '1' or from '1' to '0' at the turn of the century (depending upon its initial state). If CEB is set to a '0,' CB will not toggle. Bits D0 through D2 of register 3 contain the day (day of week). Registers 4, 5, and 6 contain the date (day of month), month, and years. The final register is the control register (this is described in the clock calibration section). Bit D7 of register 0 contains the stop bit (ST). Setting this bit to a '1' will cause the oscillator to stop.

If the device is expected to spend a significant amount of time on the shelf, the oscillator may be stopped to reduce current drain. When reset to a '0' the oscillator restarts within one second.

The seven clock registers may be read one byte at a time, or in a sequential block. The control register (address location 7) may be accessed independently. Provision has been made to assure that a clock update does not occur while any of the seven clock addresses are being read. If a clock address is being read, an update of the clock registers will be delayed by 250 ms to allow the READ to be completed before the update occurs. This will prevent a transition of data during the READ.

Note: This 250 ms delay affects only the clock register update and does not alter the actual clock time.

Table 3. Register map(1)

Address	Data								Function/range BCD format	
	D7	D6	D5	D4	D3	D2	D1	D0		
0	ST	10 Seconds			Seconds				Seconds	00-59
1	X	10 Minutes			Minutes				Minutes	00-59
2	CEB(2)	CB	10 hours		Hours				Century/hours	0-1/00-23
3	X	X	X	X	X	Day			Day	01-07
4	X	X	10 date		Date				Date	01-31
5	X	X	X	10 M.	Month				Month	01-12
6	10 years				Years				Year	00-99
7	OUT	FT	S	Calibration					Control	

1. Keys:
S = Sign bit
FT = Frequency test bit
ST = Stop bit
OUT = Output level
X = Don't care
CEB = Century enable bit
CB = Century bit

2. When CEB is set to '1,' CB toggles from '0' to '1' or from '1' to '0' every 100 years (dependent upon the initial value set). When CEB is set to '0,' CB does not toggle.

3.1 Clock calibration

The M41T56 is driven by a quartz-controlled oscillator with a nominal frequency of 32,768 Hz. The devices are tested not to exceed 35 ppm (parts per million) oscillator frequency error at 25 °C, which equates to about ±1.53 minutes per month. With the calibration bits properly set, the accuracy of each M41T56 improves to better than ±2 ppm at 25 °C.

The oscillation rate of any crystal changes with temperature (see *Figure 11 on page 15*). Most clock chips compensate for crystal frequency and temperature shift error with cumbersome “trim” capacitors. The M41T56 design, however, employs periodic counter correction. The calibration circuit adds or subtracts counts from the oscillator divider circuit at the divide by 256 stage, as shown in *Figure 11 on page 15*. The number of times pulses are blanked (subtracted, negative calibration) or split (added, positive calibration) depends upon the value loaded into the five-bit calibration byte found in the control register. Adding counts speeds the clock up, subtracting counts slows the clock down.

The calibration byte occupies the five lower order bits (D4-D0) in the control register (addr 7). This byte can be set to represent any value between 0 and 31 in binary form. Bit D5 is the sign bit; '1' indicates positive calibration, '0' indicates negative calibration. Calibration occurs within a 64 minute cycle. The first 62 minutes in the cycle may, once per minute, have one second either shortened by 128 or lengthened by 256 oscillator cycles. If a binary '1' is loaded into the register, only the first 2 minutes in the 64 minutes cycle will be modified; if a binary 6 is loaded, the first 12 will be affected, and so on.

Therefore, each calibration step has the effect of adding 512 or subtracting 256 oscillator cycles for every 125,829,120 actual oscillator cycles, that is +4.068 or –2.034 ppm of adjustment per calibration step in the calibration register. Assuming that the oscillator is in fact running at exactly 32,768Hz, each of the 31 increments in the calibration byte would represent +10.7 or –5.35 seconds per month which corresponds to a total range of +5.5 or –2.75 minutes per month.

Two methods are available for ascertaining how much calibration a given M41T56 may require. The first involves simply setting the clock, letting it run for a month and comparing it to a known accurate reference (like WWV broadcasts). While that may seem crude, it allows the designer to give the end user the ability to calibrate his clock as his environment may require, even after the final product is packaged in a non-user serviceable enclosure. All the designer has to do is provide a simple utility that accessed the calibration byte.

The second approach is better suited to a manufacturing environment, and involves the use of some test equipment. When the frequency test (FT) bit, the seventh-most significant bit in the control register, is set to a '1,' and the oscillator is running at 32,768 Hz, the FT/OUT pin of the device will toggle at 512 Hz. Any deviation from 512 Hz indicates the degree and direction of oscillator frequency shift at the test temperature.

For example, a reading of 512.01024 Hz would indicate a +20 ppm oscillator frequency error, requiring a –10(XX001010) to be loaded into the calibration byte for correction.

Note: Setting or changing the calibration byte does not affect the frequency test output frequency.

Figure 11. Crystal accuracy across temperature

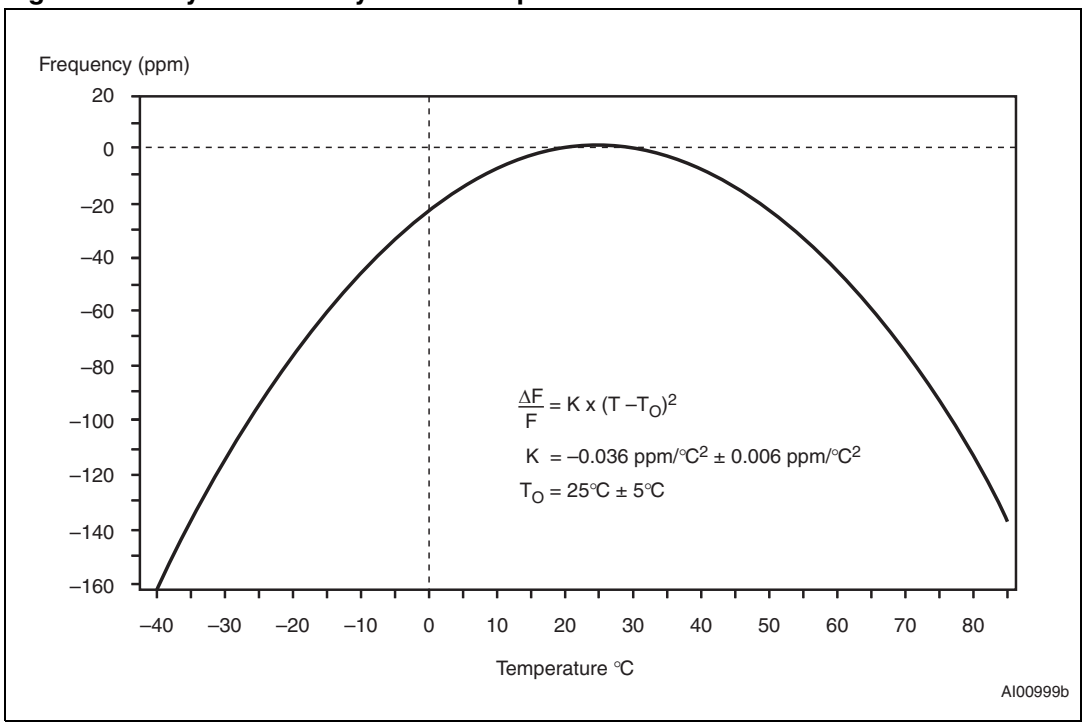
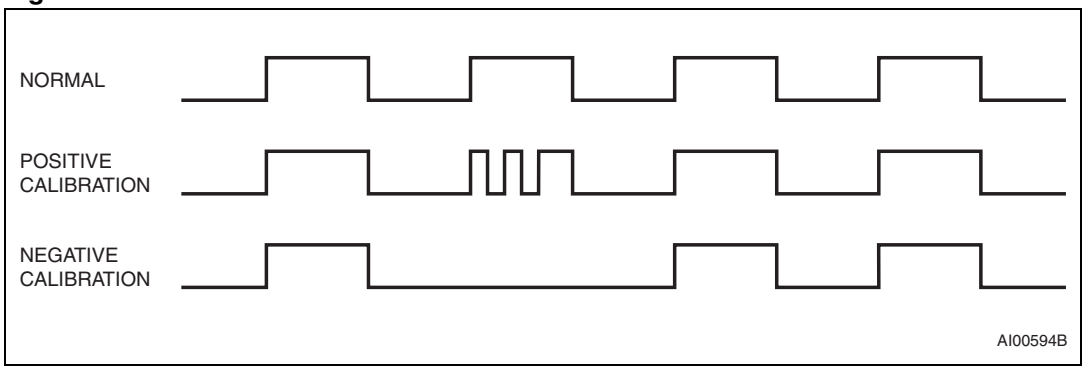


Figure 12. Clock calibration



3.2 Output driver pin

When the FT bit is not set, the FT/OUT pin becomes an output driver that reflects the contents of D7 of the control register. In other words, when D6 of location 7 is a '0' and D7 of location 7 is a '0' and then the FT/OUT pin will be driven low.

Note: The FT/OUT pin is open drain which requires an external pull-up resistor.

3.3 Initial power-on defaults

Upon initial application of power to the device, the FT bit will be set to a '0' and the OUT bit will be set to a '1.' All other register bits will initially power-on in a random state.

4 Maximum ratings

Stressing the device above the rating listed in the “absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
T_A	Ambient operating temperature	–40 to 85	°C
T_{STG}	Storage temperature (V_{CC} off, oscillator off)	–55 to 125	°C
T_{SLD} (1)	Lead solder temperature for 10 seconds	260	°C
V_{IO}	Input or output voltages	–0.3 to 7	V
V_{CC}	Supply voltage	–0.3 to 7	V
I_O	Output current	20	mA
P_D	Power dissipation	0.25	W

1. For SO package, Lead-free (Pb-free) lead finish: Reflow at peak temperature of 260 °C. The time above 255 °C must not exceed 30 seconds.

Caution: *Negative undershoots below –0.3 V are not allowed on any pin while in the battery backup mode.*

5 DC and AC parameters

This section summarizes the operating and measurement conditions, as well as the DC and AC characteristics of the device. The parameters in the following DC and AC characteristics tables are derived from tests performed under the measurement conditions listed in *Table 5: Operating and AC measurement conditions*. Designers should check that the operating conditions in their projects match the measurement conditions when using the quoted parameters.

Table 5. Operating and AC measurement conditions(1)

Parameter	Value	Unit
Supply voltage (V_{CC})	4.5 to 5.5	V
Ambient operating temperature (T_A)	–40 to 85	°C
Load capacitance (C_L)	100	pF
Input rise and fall times	≤ 5	ns
Input pulse voltages	0 to 3	V
Input and output timing ref. voltages	1.5	V

1. Output Hi-Z is defined as the point where data is no longer driven.

Figure 13. AC measurement I/O waveform



Table 6. Capacitance

Symbol	Parameter(1)(2)	Min	Max	Unit
C_{IN}	Input capacitance (SCL)		7	pF
C_{OUT}(3)	Output capacitance (SDA, FT/OUT)		10	pF
t_{LP}	Low-pass filter input time constant (SDA and SCL)	0.25	1	µs

1. Effective capacitance measured with power supply at 5V; sampled, not 100% tested.
2. At 25 °C, f = 1 MHz.
3. Outputs deselected.

Table 7. DC characteristics

Symbol	Parameter	Test condition(1)	Min	Typ	Max	Unit
I_{LI}	Input leakage current	$0V \le V_{IN} \le V_{CC}$			±1	µA
I_{LO}	Output leakage current	$0V \le V_{OUT} \le V_{CC}$			±1	µA
I_{CC1}	Supply current	Switch frequency = 100 kHz			300	µA
I_{CC2}	Supply current (standby)	SCL, SDA = V_{CC} – 0.3 V		100		µA
V_{IL}	Input low voltage		–0.3		1.5	V
V_{IH}	Input high voltage		3		V_{CC} + 0.8	V
V_{OL}	Output low voltage	I_{OL} = 5mA, V_{CC} = 4.5 V			0.4	V
V_{BAT}(2)	Battery supply voltage		2.5	3	3.5	V
I_{BAT}	Battery supply current	T_A = 25 °C, V_{CC} = 0 V, oscillator ON, V_{BAT} = 3 V		450	550	nA

1. Valid for ambient operating temperature: T_A = –40 to 85 °C; V_{CC} = 4.5 to 5.5 V (except where noted).
2. STMicroelectronics recommends the RAYOVAC BR1225 or BR1632 (or equivalent) as the battery supply.

Table 8. Crystal electrical characteristics

Symbol	Parameter(1)(2)	Min	Typ	Max	Unit
f_O	Resonant frequency		32.768		kHz
R_S	Series resistance			60	kΩ
C_L	Load capacitance		12.5		pF

1. These values are externally supplied for the SO8 package. STMicroelectronics recommends the KDS DT-38: 1TA/1TC252E127, Tuning Fork Type (thru-hole) or the DMX-26S: 1TJS125FH2A212, (SMD) quartz crystal for industrial temperature operations. For contact information on this crystal type, see *Section 8: References on page 25*.
2. Load capacitors are integrated within the M41T56. Circuit board layout considerations for the 32.768 kHz crystal of minimum trace lengths and isolation from RF generating signals should be taken into account.

Figure 14. Power down/up mode AC waveforms

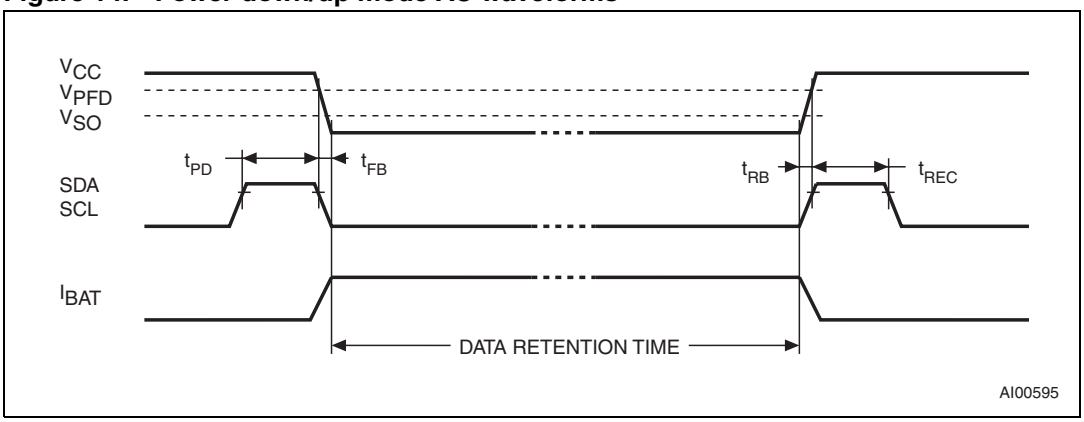


Table 9. Power down/up mode AC characteristics

Symbol	Parameter[1]	Min	Max	Unit
t_{PD}	SCL and SDA at V_{IH} before power-down	0		ns
t_{FB}	V_{PFD} (min) to V_{SS} V_{CC} fall time	300		µs
t_{RB}	V_{SS} to V_{PFD} (min) V_{CC} rise time	100		µs
t_{REC}	SCL and SDA at V_{IH} after power-up	10		µs

1. Valid for ambient operating temperature: T_A = –40 to 85 °C; V_{CC} = 4.5 to 5.5 V (except where noted).

Table 10. Power down/up trip points DC characteristics

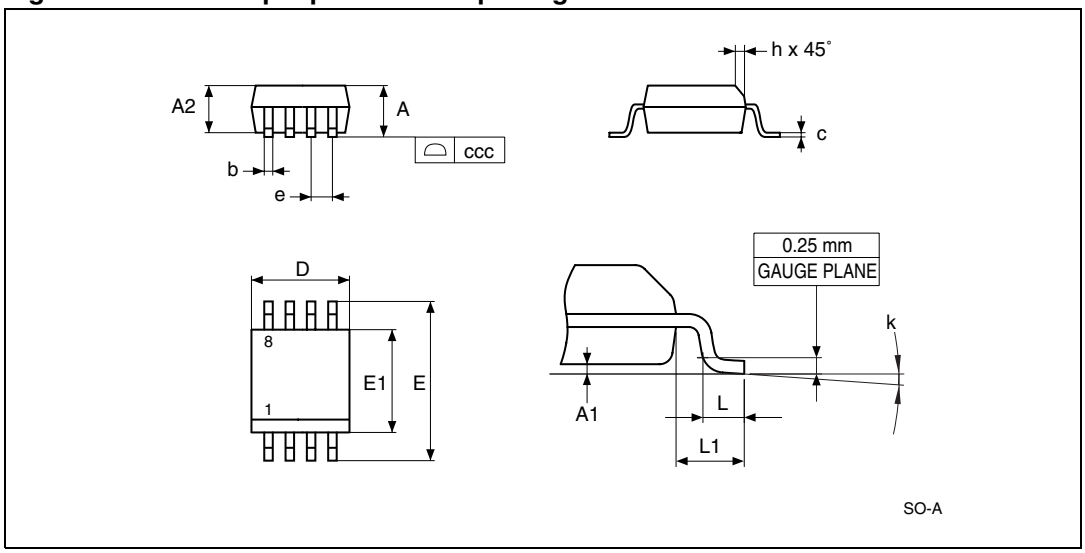
Symbol	Parameter[1][2]	Min	Typ	Max	Unit
V_{PFD}	Power-fail deselect voltage	1.2 V_{BAT}	1.25 V_{BAT}	1.285 V_{BAT}	V
V_{SO}	Battery back-up switchover voltage		V_{BAT}		V

1. All voltages referenced to V_{SS}.
2. Valid for ambient operating temperature: T_A = –40 to 85 °C; V_{CC} = 4.5 to 5.5 V (except where noted).

6 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 15. SO8 – 8-pin plastic small package outline



1. Drawing is not to scale.

Table 11. SO8 – 8-pin plastic small outline, package mechanical data

Symbol	millimetres			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.75			0.069
A1		0.10	0.25		0.004	0.010
A2		1.25			0.049	
b		0.28	0.48		0.011	0.019
c		0.17	0.23		0.007	0.009
ccc			0.10			0.004
D	4.90	4.80	5.00	0.193	0.189	0.197
E	6.00	5.80	6.20	0.236	0.228	0.244
E1	3.90	3.80	4.00	0.154	0.150	0.157
e	1.27	–	–	0.050	–	–
h		0.25	0.50		0.010	0.020
k		0°	8°		0°	8°
L		0.40	1.27		0.016	0.050
L1	1.04			0.041		

1. Drawing is not to scale.

Figure 16. Carrier tape for SO8 package (150-mil body width)

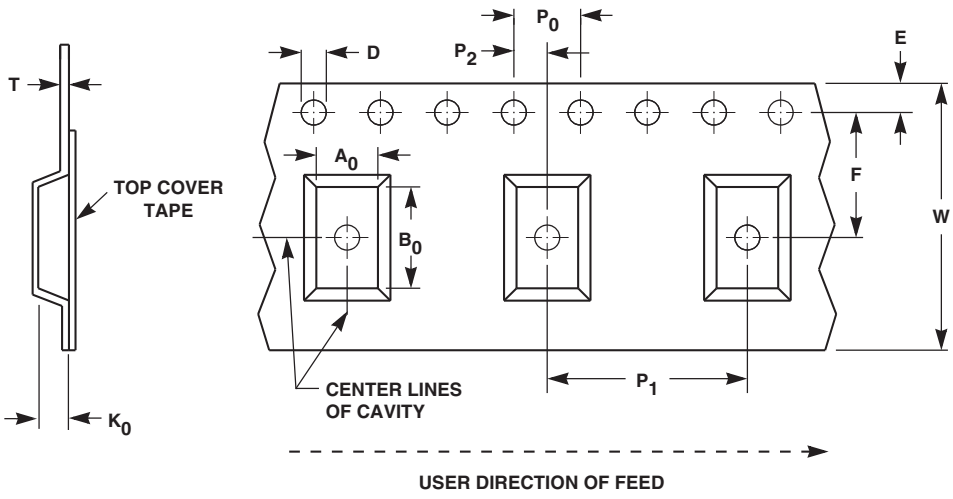


Table 12. Carrier tape dimensions for SO8 package (150-mil body width)

Package	W	D	E	P_0	P_2	F	A_0	B_0	K_0	P_1	T	Unit	Bulk Qty
SO8	12.00 ±0.30	1.50 +0.10/ −0.00	1.75 ±0.10	4.00 ±0.10	2.00 ±0.10	5.50 ±0.05	6.50 ±0.10	5.30 ±0.10	2.20 ±0.10	8.00 ±0.10	0.30 ±0.05	mm	2500

Figure 17. Reel schematic

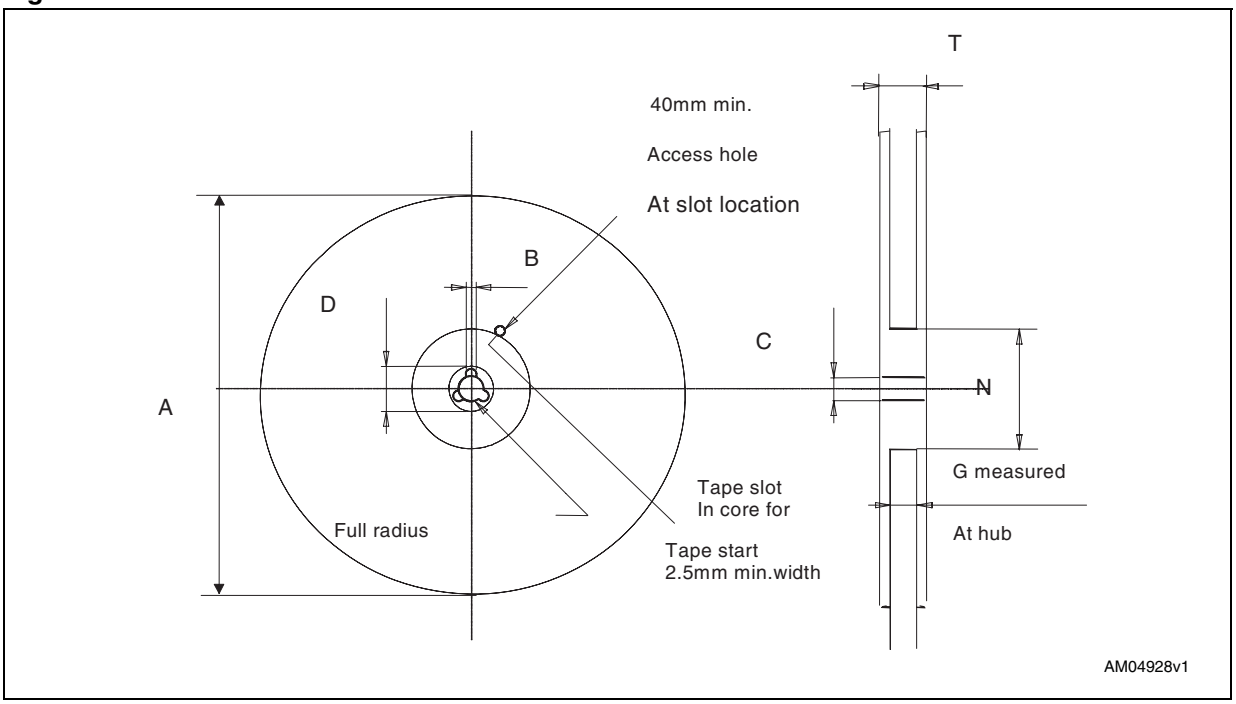


Table 13. Reel dimensions for 12 mm carrier tape - SO8 package (150-mil body width)

A (max)	B (min)	C	D (min)	N (min)	G	T (max)
330 mm (13-inch)	1.5 mm	13 mm ± 0.2 mm	20.2 mm	60 mm	12.4 mm + 2/–0 mm	18.4 mm

Note: The dimensions given in Table 13 incorporate tolerances that cover all variations on critical parameters.

7 Part numbering

Table 14. Ordering information scheme

Example: M41T 56 M 6 E

Device type

M41T

Supply voltage and write protect voltage

56 = V_{CC} = 4.5 to 5.5 V

Package

M = SO8

Temperature range

6 = –40 °C to 85 °C

Shipping method

E = Lead-free package (ECOPACK®), tubes(1)

F = Lead-free package (ECOPACK®), tape & reel

1. Not recommended for new design. Contact local ST sales office for availability.

8 References

- The crystal component supplier KDS as cited in *Table 8: Crystal electrical characteristics on page 18* can be contacted at **http://www.kds.info/index_en.htm**

9 Revision history

Table 15. Document revision history

Date	Revision	Changes
Mar-1999	1.0	First issue
23-Dec-1999	1.1	SOH28 package added
21-Mar-2000	1.2	Series resistance max value changed (*Table 8*)
30-Nov-2000	1.3	Added PSDIP8 package
25-Jan-2001	1.4	Corrected graphic, measurements of PSDIP8 (Figure 18, Table 14)
16-Feb-2001	2.0	Reformatted, table added (*Table 16*).
06-Apr-2001	2.1	Add temp./voltage information to characteristics (*Table 7*, *Table 2*); correct series resistance (*Table 8*)
17-Jul-2001	2.2	Basic formatting changes
02-Aug-2002	2.3	Modify reflow time and temperature footnote (*Table 4*); modify crystal electrical characteristics table footnotes (*Table 8*); removed PSDIP8 package
07-Nov-2002	2.4	Correct figure name (*Features on page 1*)
15-Jun-2004	3.0	Reformatted; add lead-free information; update characteristics (*Figure 11*; *Table 4*, *Table 14*)
11-Sep-2006	4	Changed document to new template; amalgamated diagrams in *Features on page 1*; amended footnotes in *Table 3: Register map*; updated Package mechanical data in *Section 6: Package mechanical data*; small text changes for entire document, removed lead packages from *Table 14*, ECOPACK compliant
09-Oct-2006	5	Updated package mechanical data in *Figure 15: SO8 – 8-pin plastic small package outline*.
10-Apr-2007	6	Updated package information references that only SO8 available (cover page, *Section 1*, *Section 4*, *Table 4*, *Table 8*, and *Table 14*).
06-Nov-2007	7	Added lead-free second level interconnect information to cover page and *Section 6: Package mechanical data*; updated *Table 4*, footnote 1 in *Table 8*; addition of *Section 8: References*.
13-Dec-2007	8	Updated cover page and *Section 8: References*.
06-Dec-2011	9	Updated footnote *1* of *Table 4: Absolute maximum ratings*; updated ECOPACK® text in *Section 6: Package mechanical data*; added footnote *1* to *Table 14: Ordering information scheme*; added *Figure 16*, *17*, *Table 12*, *13*; updated title; minor textual updates.

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