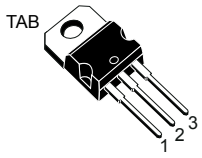
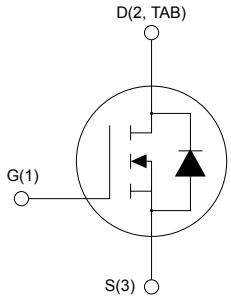
STP24NF10

Datasheet

N-channel 100 V, 55 mΩ typ., 26 A STripFET II Power MOSFET in a TO-220 package



TO-220



AM01475v1_noZen

Features

Type	V_{DS}	$R_{DS(on)}$ max.	I_D
STP24NF10	100 V	60 mΩ	26 A

- Exceptional dv/dt capability
- 100% avalanche tested
- Low gate charge

Applications

- Switching applications

Description

This Power MOSFET has been developed using STMicroelectronics' unique STripFET process, which is specifically designed to minimize input capacitance and gate charge. This renders the device suitable for use as primary switch in advanced high-efficiency isolated DC-DC converters for telecom and computer applications, and applications with low gate charge driving requirements.

Product status link
STP24NF10

Product summary	
Order code	STP24NF10
Marking	P24NF10
Package	TO-220
Packing	Tube

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	100	V
V_{DGR}	Drain-gate voltage (R_{GS} = 20 kΩ)	100	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current (continuous) at T_C = 25 °C	26	A
	Drain current (continuous) at T_C = 100 °C	18	
I_{DM}(1)	Drain current (pulsed)	104	A
P_{TOT}	Total power dissipation at T_C = 25 °C	85	W
E_{AS}(2)	Single-pulse avalanche energy	220	mJ
dv/dt(3)	Peak diode recovery voltage slope	9	V/ns
T_{stg}	Storage temperature range	-55 to 175	°C
T_J	Operating junction temperature range		°C

1. *Pulse width limited by safe operating area.*
2. *Starting T_J = 25 °C, I_D = 12 A, V_{DD} = 30 V.*
3. *I_{SD} ≤ 24 A, di/dt ≤ 300 A/µs, V_{DD} = 80%$V_{(BR)DSS}$.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	1.76	°C/W
R_{thJA}	Thermal resistance, junction-to-ambient	62.5	°C/W

2 Electrical characteristics

T_C = 25 °C unless otherwise specified.

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 250 µA	100			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 100 V			1	µA
		V_{GS} = 0 V, V_{DS} = 100 V, T_C = 125 °C(1)			10	
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 12 A		55	60	mΩ

1. *Specified by design, not tested in production.*

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} = 15 V, I_D = 12 A	-	10		S
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0 V	-	870		pF
C_{oss}	Output capacitance		-	125		pF
C_{rss}	Reverse transfer capacitance		-	50		pF
Q_g	Total gate charge	V_{DD} = 80 V, I_D = 24 A, V_{GS} = 10 V (see Figure 13. Test circuit for gate charge behavior)	-	30	41	nC
Q_{gs}	Gate-source charge		-	6		nC
Q_{gd}	Gate-drain charge		-	10		nC

1. *Pulsed: pulse duration=300 µs, duty cycle 1.5%.*

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 50 V, I_D = 12 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 12. Test circuit for resistive load switching times and Figure 17. Switching time waveform)	-	60	-	ns
t_r	Rise time		-	15	-	ns
$t_{d(off)}$	Turn-off delay time		-	50	-	ns
t_f	Fall time		-	20	-	ns

Table 6. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		26	A
I_{SDM}(1)	Source-drain current (pulsed)		-		104	A
V_{SD}(2)	Forward on voltage	I_{SD} = 24 A, V_{GS} = 0 V	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 24 A, di/dt = 100 A/µs,	-	100		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 30 V, T_J = 150 °C	-	375		nC
I_{RRM}	Reverse recovery current	(see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	7.5		A

1. *Pulse width limited by safe operating area.*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

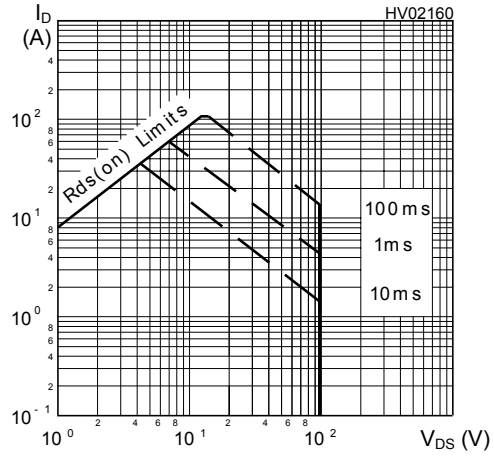


Figure 2. Thermal impedance

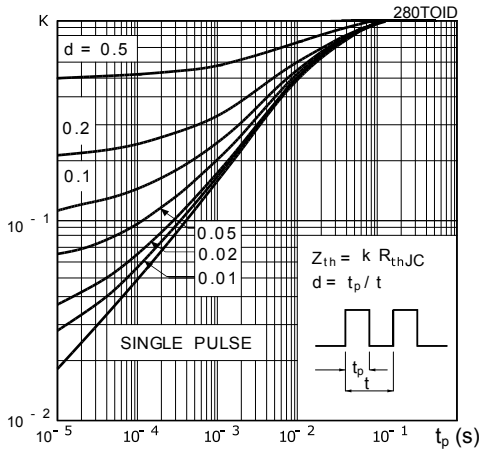


Figure 3. Output characteristics

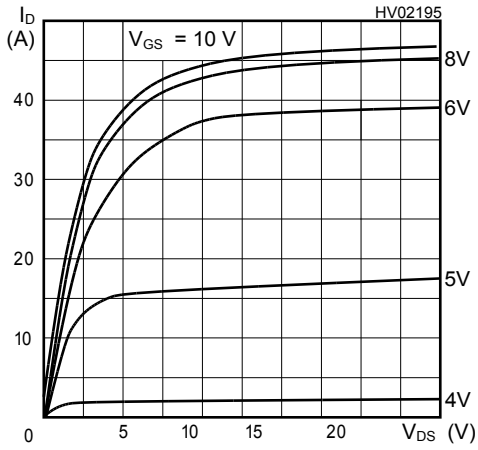


Figure 4. Transfer characteristics

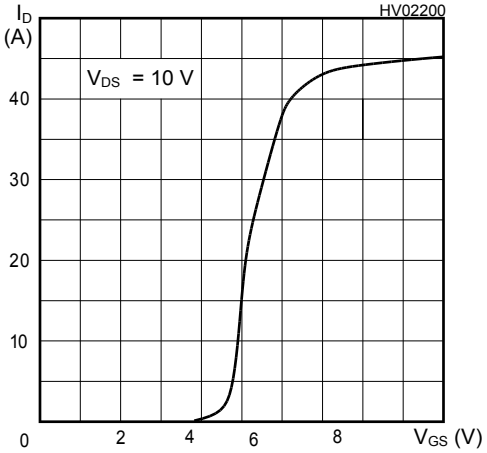


Figure 5. Trasconductance

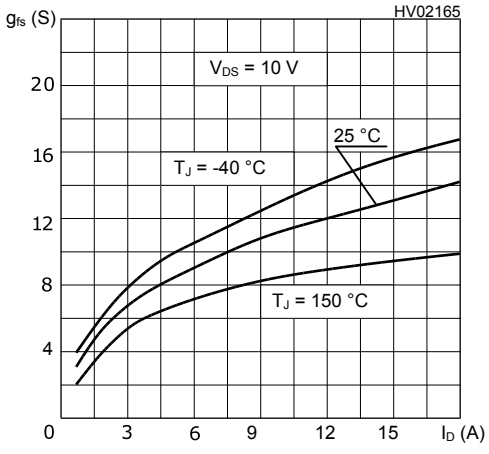


Figure 6. Static drain-source on-resistance

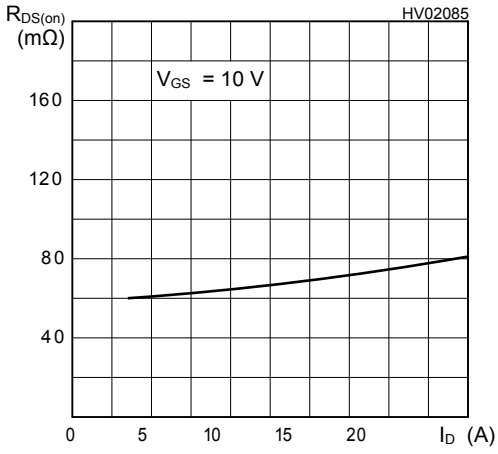


Figure 7. Gate charge vs gate-source voltage

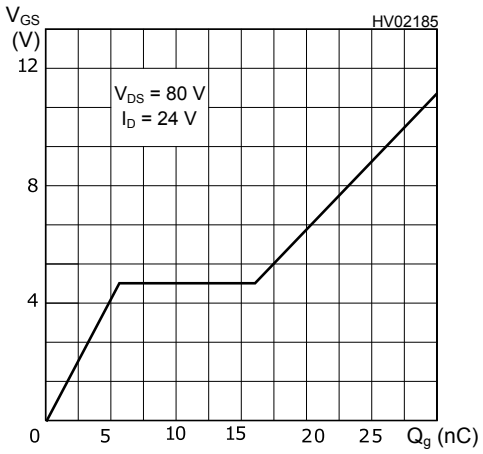


Figure 8. Capacitance variations

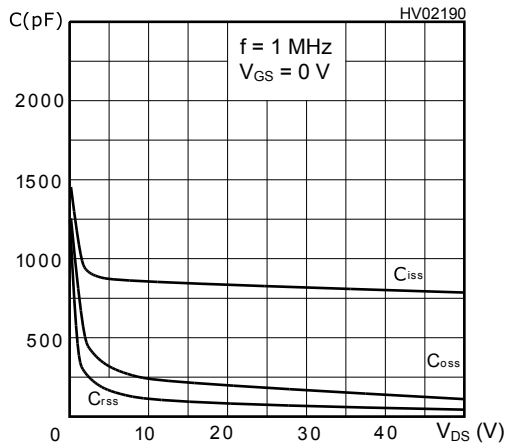


Figure 9. Normalized gate threshold voltage vs temperature

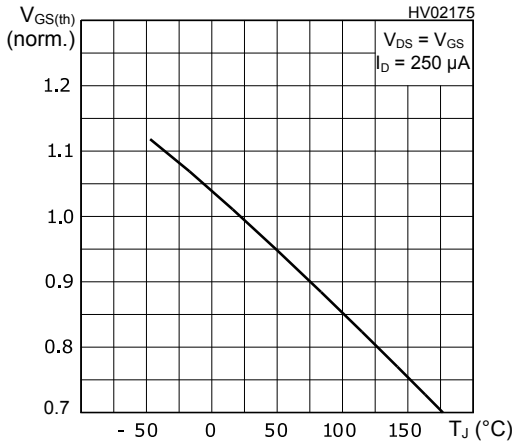


Figure 10. Normalized on-resistance vs temperature

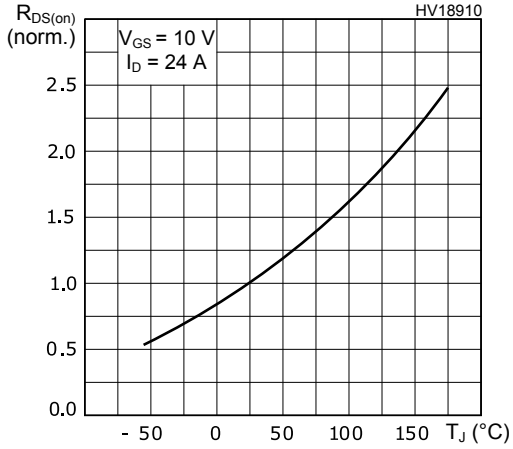
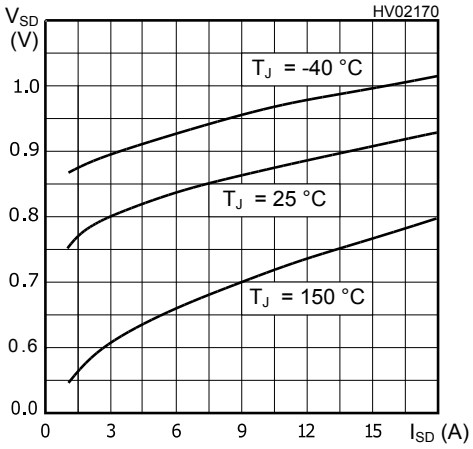
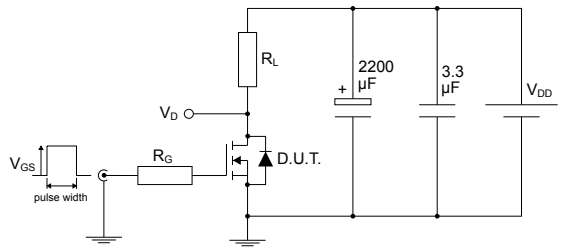


Figure 11. Source-drain diode forward characteristics



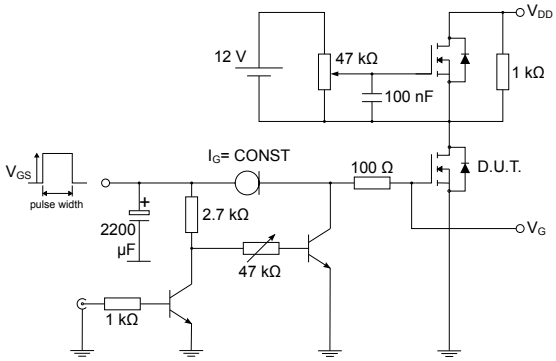
3 Test circuits

Figure 12. Test circuit for resistive load switching times



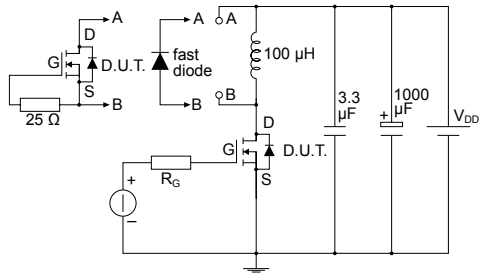
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Figure 13. Test circuit for gate charge behavior



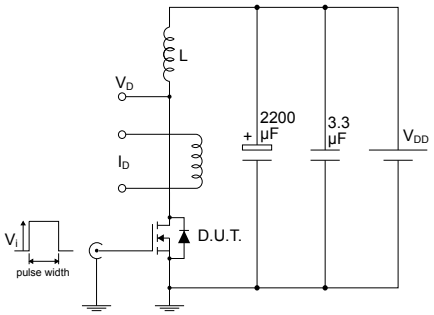
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Figure 14. Test circuit for inductive load switching and diode recovery times



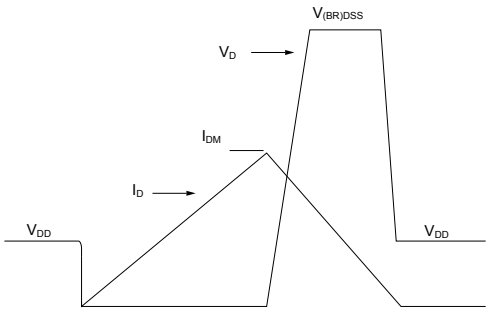
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Figure 15. Unclamped inductive load test circuit



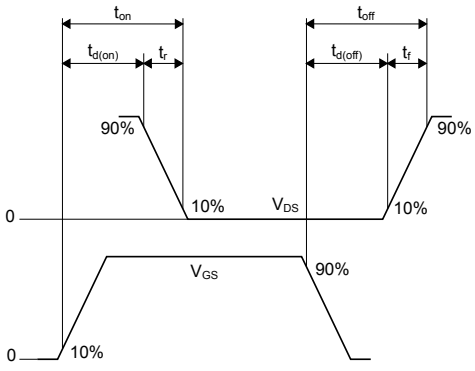
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Figure 16. Unclamped inductive waveform



AM01472v1

Figure 17. Switching time waveform



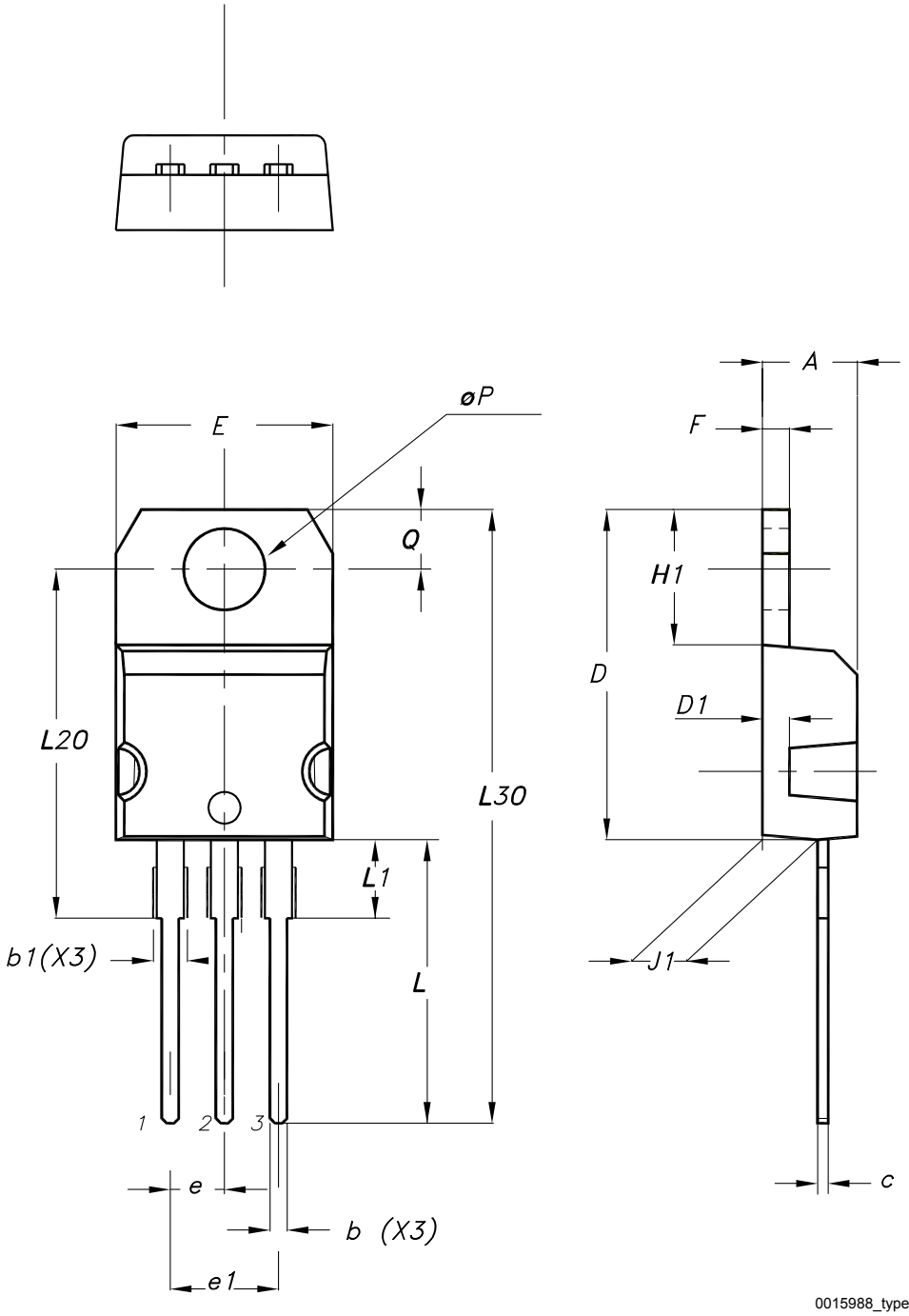
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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TO-220 type A package information

Figure 18. **TO-220 type A package outline**



0015988_typeA_Rev_23

Table 7. **TO-220 type A package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95
Slug flatness		0.03	0.10

Revision history

Table 8. **Document revision history**

Date	Revision	Changes
09-Sep-2004	6	Complete version.
09-Aug-2006	7	New template, no content change.
22-Feb-2022	8	The part number STB24NF10 have been removed and the document has been updated accordingly. Updated title and Internal schematic on cover page. Updated Section 3 Test circuits. Updated Section 4 Package information. Minor text changes.

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