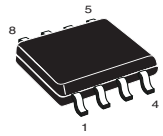
STS8DNF3LL

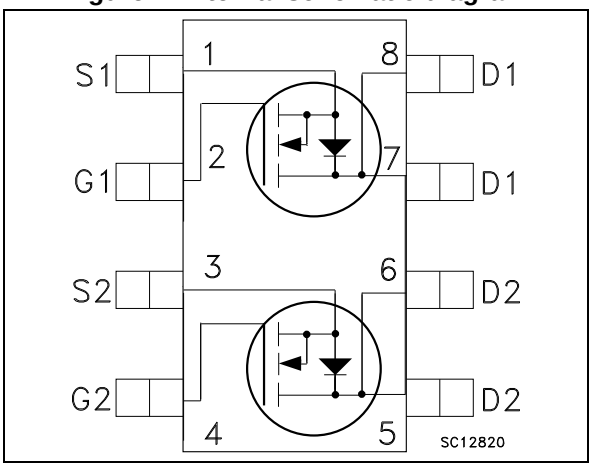
Dual N-channel 30 V, 0.017 Ω typ., 8 A, STripFET™ II Power MOSFET in a SO-8 package

Datasheet - production data



SO-8

Figure 1. Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$max	I_D
STS8DNF3LL	30 V	0.020 Ω	8 A

- Optimal $R_{DS(on)}$ x Q_g trade-off @ 4.5 V
- Conduction losses reduced
- Switching losses reduced

Applications

- Switching applications

Description

This Power MOSFET has been developed using STMicroelectronics' unique STripFET process, which is specifically designed to minimize input capacitance and gate charge. This renders the device suitable for use as primary switch in advanced high-efficiency isolated DC-DC converters for telecom and computer applications, and applications with low gate charge driving requirements.

Table 1. Device summary

Order code	Marking	Package	Packaging
STS8DNF3LL	8DF3LL	SO-8	Tape and reel

This is information on a product in full production. www.st.com

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2.1 Electrical characteristics (curves) 6

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	30	V
V_{GS}	Gate- source voltage	±16	V
I_D	Drain current (continuous) at T_C = 25 °C single operating	8	A
I_D	Drain current (continuous) at T_C = 100 °C single operating	5	A
I_{DM} (1)	Drain current (pulsed)	32	A
P_{TOT}	Total dissipation at T_C = 25 °C dual operating Total dissipation at T_C = 25 °C single operating	2 1.6	W W

1. Pulse width limited by safe operating area

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}amb}$ (1)	Thermal resistance junction-ambient single operating Thermal resistance junction-ambient dual operating	78 62.5	°C/W °C/W
T_J	Thermal operating junction-ambient	150	°C
T_{stg}	Storage temperature	-55 to 150	°C

1. Mounted on FR-4 board with 0.5 in^2 pad of Cu

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown voltage	I_D = 250 µA, V_{GS} = 0	30			V
I_{DSS}	Zero gate voltage Drain current (V_{GS} = 0)	V_{DS} = 30 V			1	µA
		V_{DS}=30 V, T_C=125°C			10	µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 16 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	1			V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 4 A V_{GS} = 4.5 V, I_D = 4 A		0.017 0.020	0.020 0.024	W W

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} = 15 V, I_D= 4 A	-	12.5		S
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0	-	800		pF
C^{oss}	Output capacitance		-	250		pF
C_{rss}	Reverse transfer capacitance		-	60		pF
Q_g	Total gate charge	V_{DD} = 15 V, I_D = 8 A, V_{GS} = 5 V (see *Figure 15*)	-	12.5	17	nC
Q_{gs}	Gate-source charge		-	3.2		nC
Q_{gd}	Gate-drain charge		-	4.5		nC

1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5.

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD}=15 V, I_D=4 A, R_G=4.7Ω, V_{GS}= 4.5V (see *Figure 14*)	-	18	-	ns
t_r	Rise time		-	32	-	ns
$t_{d(off)}$	Turn-off delay time	V_{DD}=15 V, I_D=4A, R_G=4.7 Ω, V_{GS}= 4.5 V (see *Figure 14*)	-	21	-	ns
t_f	Fall time		-	11	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
I_{SD}	Source-drain current		-		8	A
I_{SDM} (1)	Source-drain current (pulsed)		-		32	A
V_{SD} (2)	Forward on voltage	I_{SD} = 8 A, V_{GS} = 0	-		1.2	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 8 A, V_{DD} = 15 V di/dt = 100 A/µs, T_j = 150 °C (see *Figure 16*)	-	23 17 1.5		ns nC A

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

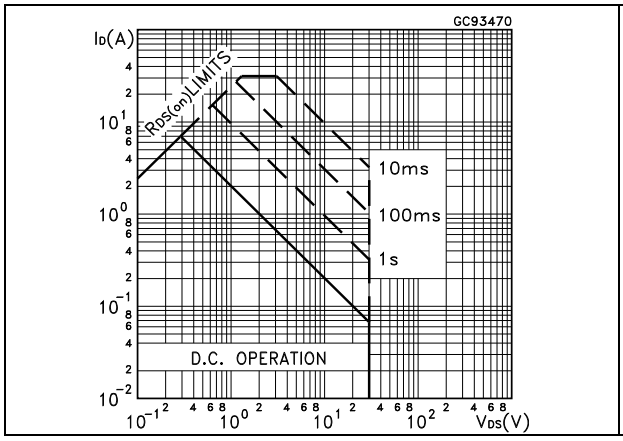


Figure 3. Thermal impedance

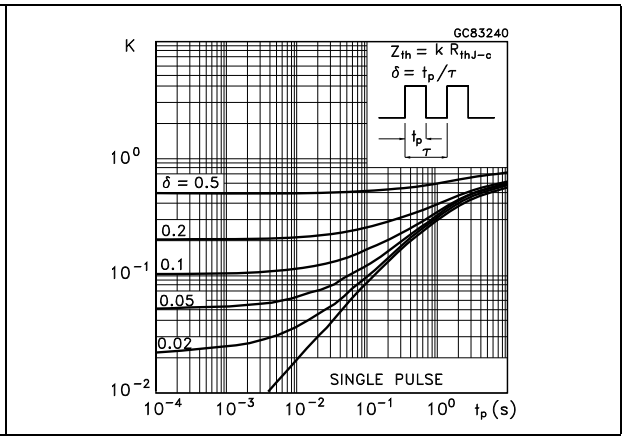


Figure 4. Output characteristics

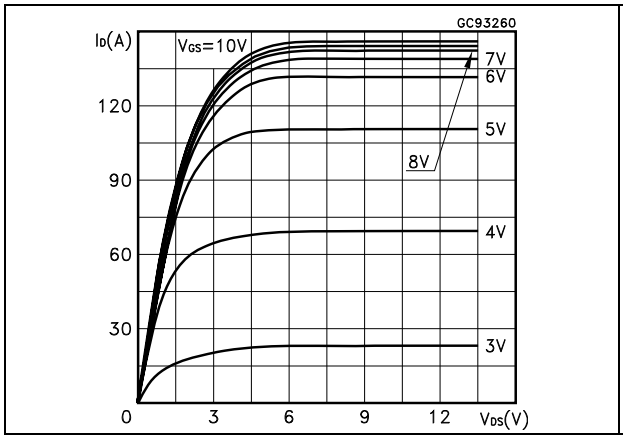


Figure 5. Transfer characteristics

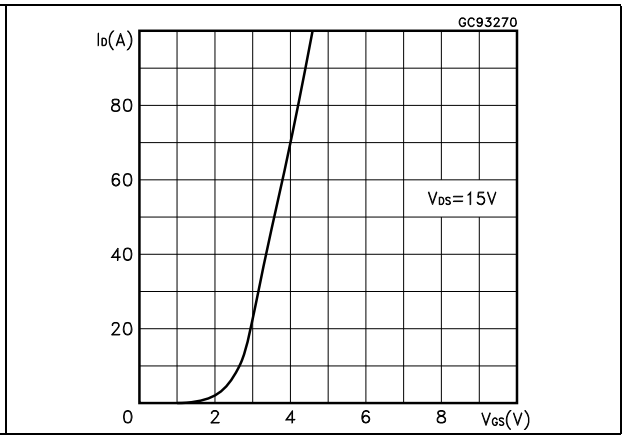


Figure 6. Transconductance

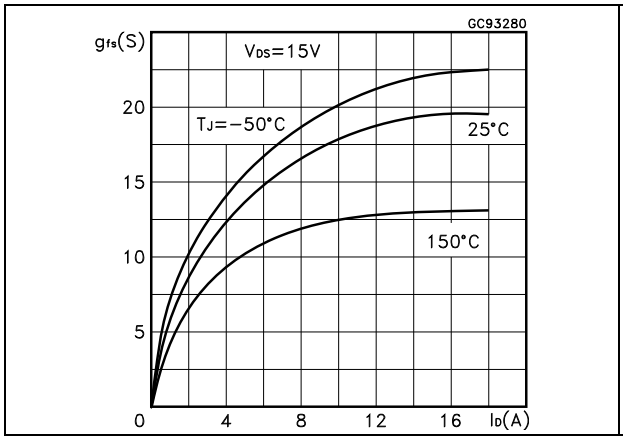


Figure 7. Static drain-source on-resistance

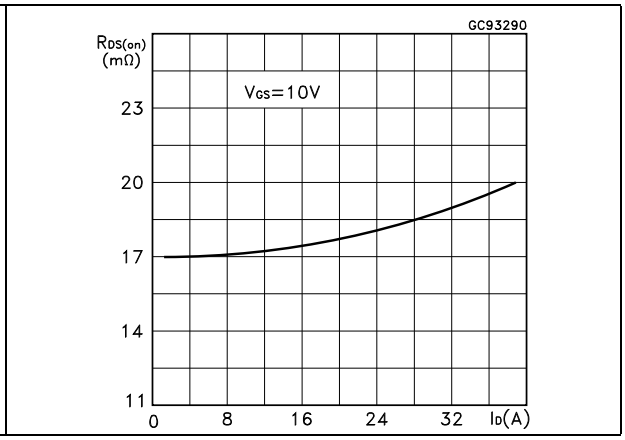


Figure 8. Gate charge vs. gate-source voltage

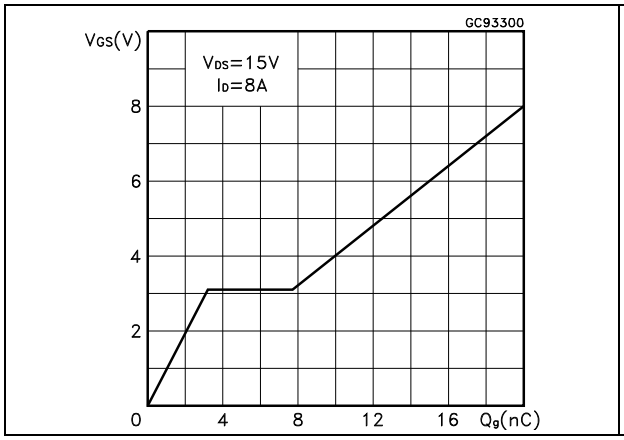


Figure 9. Capacitance variations

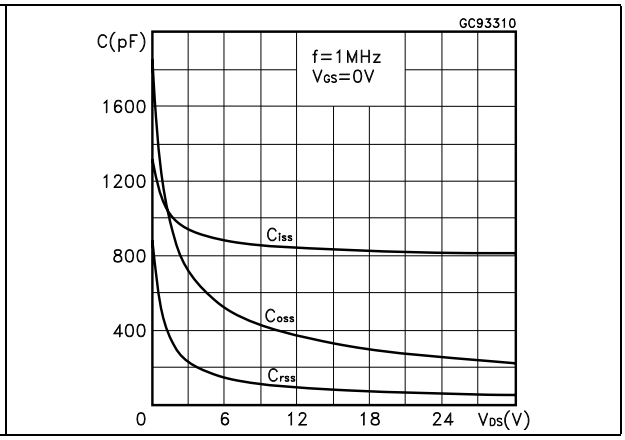


Figure 10. Normalized gate threshold voltage vs. temperature

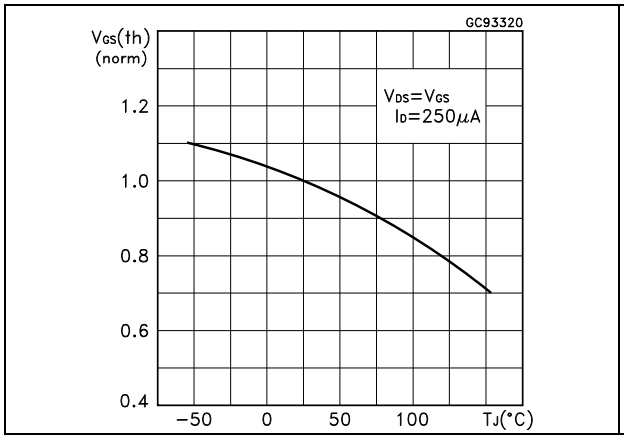


Figure 11. Normalized on-resistance vs. temperature

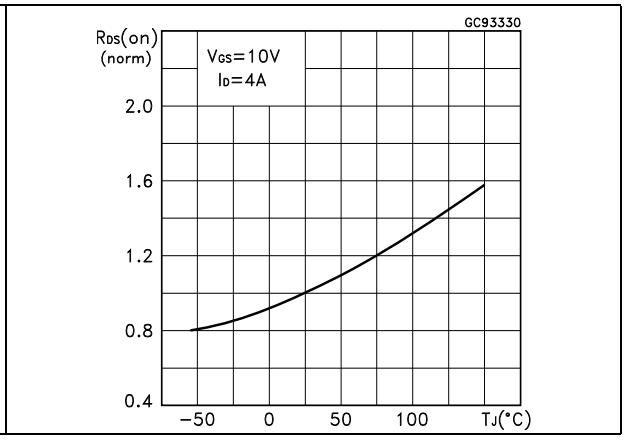


Figure 12. Source-drain diode forward characteristics

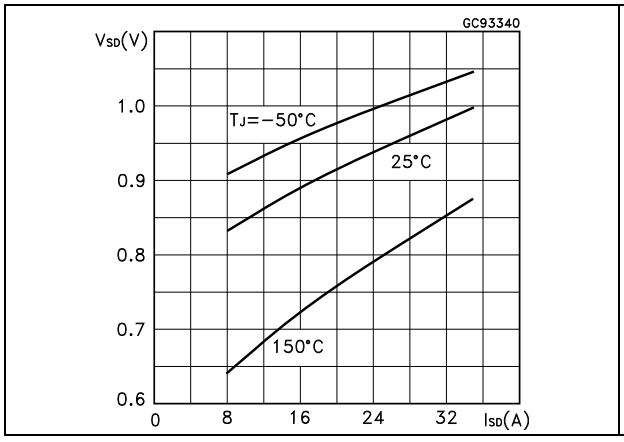
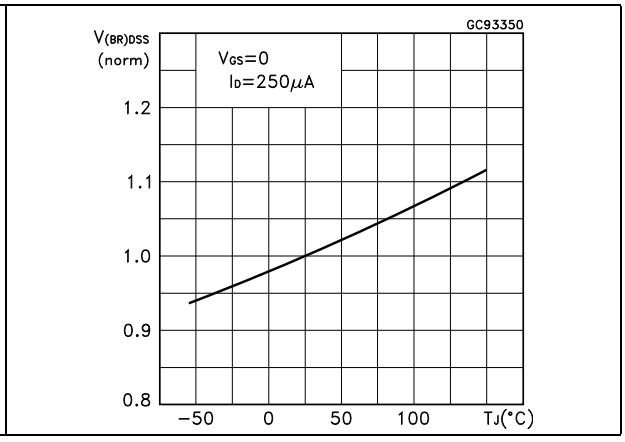


Figure 13. Normalized breakdown voltage vs. temperature



3 Test circuit

Figure 14. Switching times test circuit for resistive load

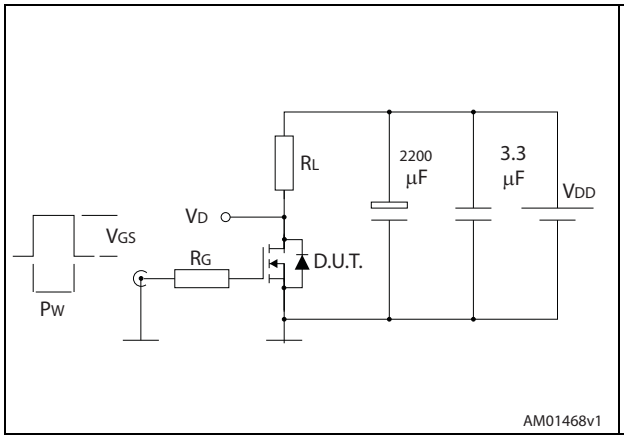


Figure 15. Gate charge test circuit

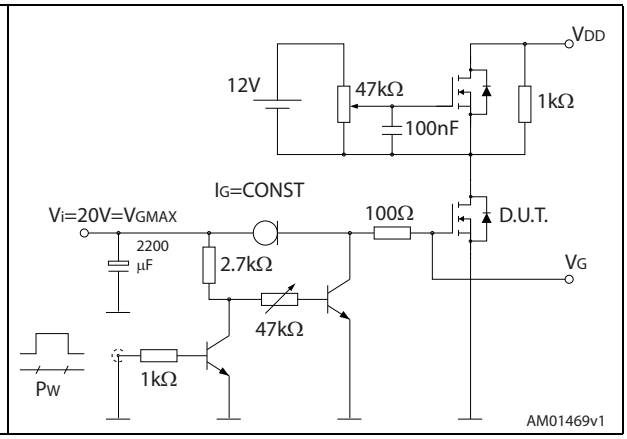


Figure 16. Test circuit for inductive load switching and diode recovery times

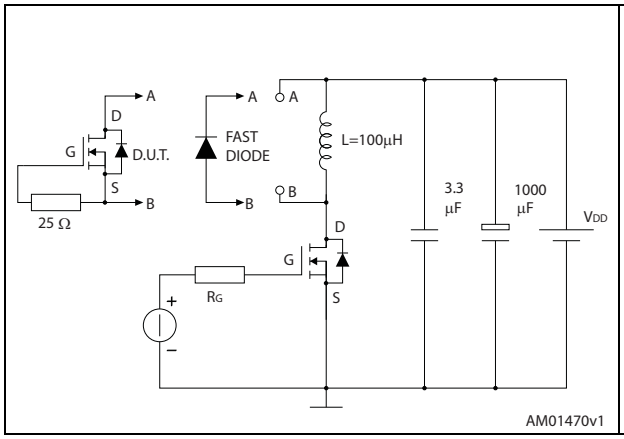


Figure 17. Unclamped Inductive load test circuit

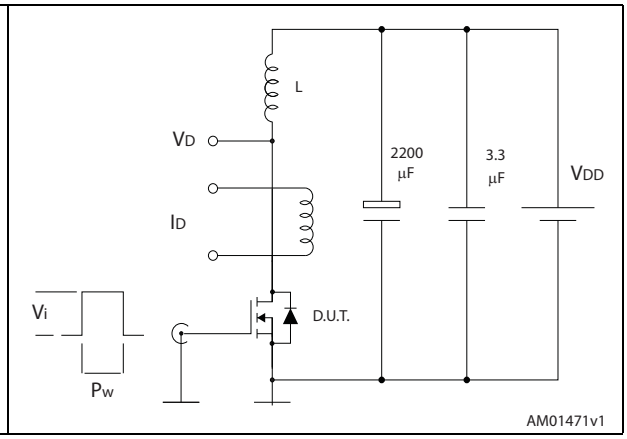


Figure 18. Unclamped inductive waveform

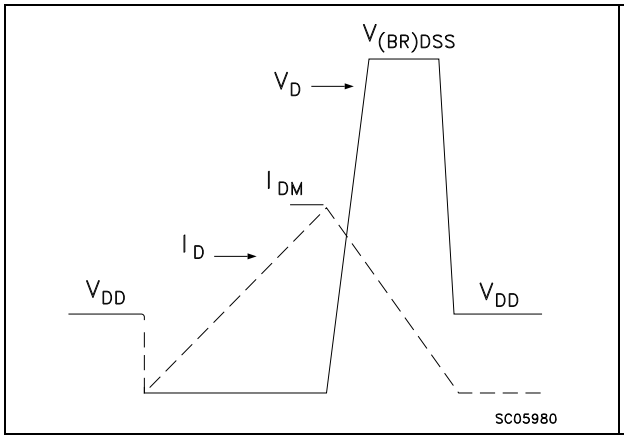
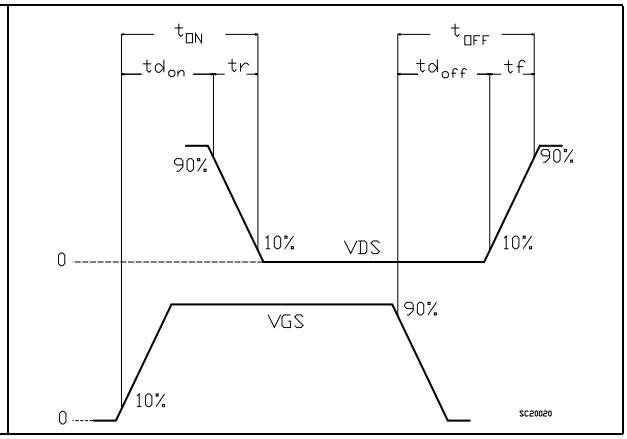


Figure 19. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Table 8. SO-8 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.31		0.51
b1	0.28		0.48
c	0.10		0.25
c1	0.10		0.23
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
L1		1.04	
L2		0.25	
k	0°		8°
ccc			0.10

Figure 20. SO-8 drawing

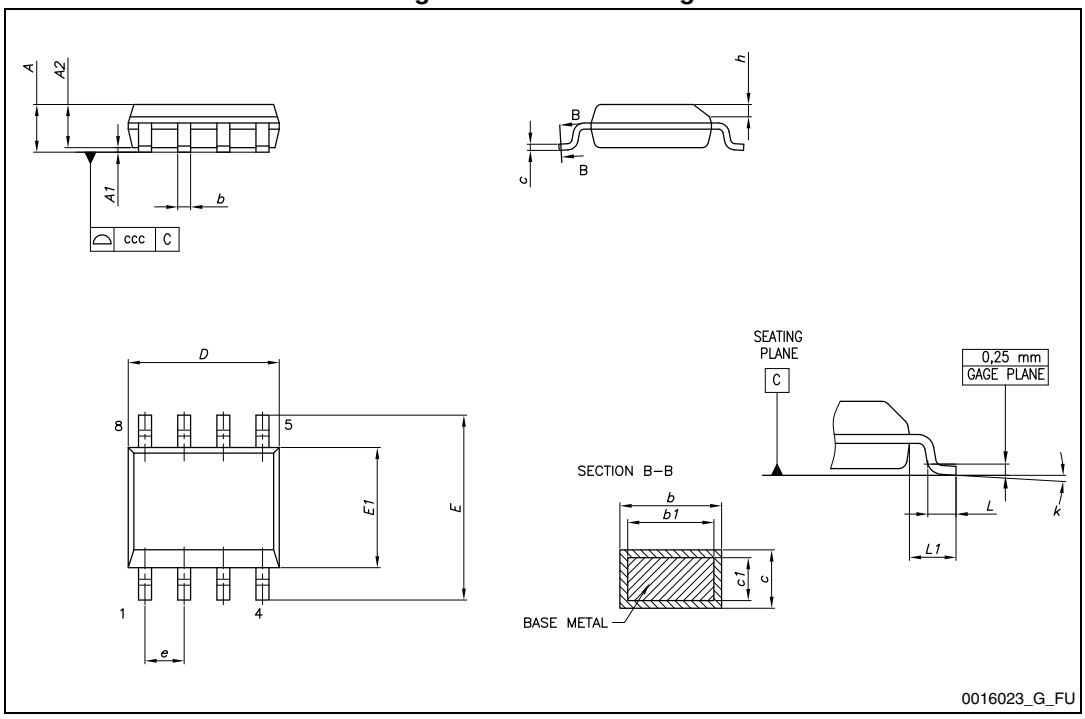
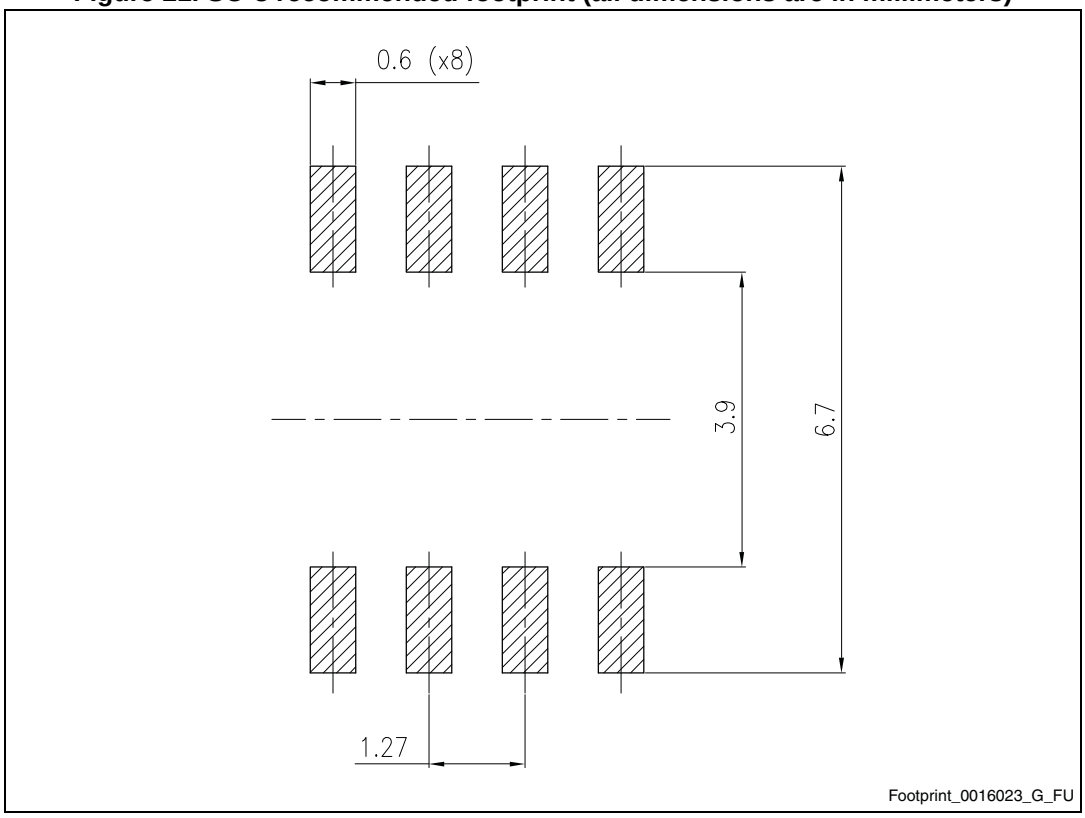


Figure 21. SO-8 recommended footprint (all dimensions are in millimeters)

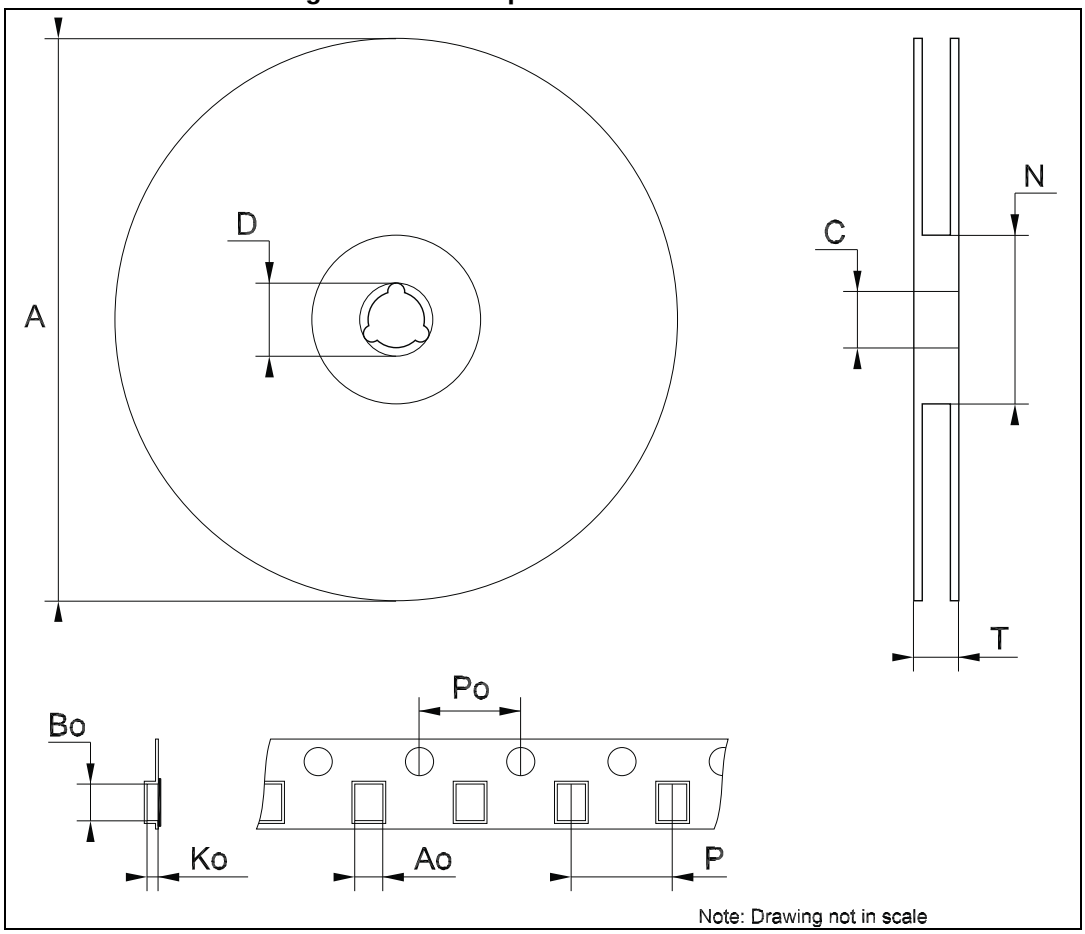


5 Packaging mechanical data

Table 9. SO-8 tape and reel mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			330
C	12.8		13.2
D	20.2		
N	60		
T			22.4
Ao	8.1		8.5
Bo	5.5		5.9
Ko	2.1		2.3
Po	3.9		4.1
P	7.9		8.1

Figure 22. SO-8 tape and reel dimensions



6 Revision history

Table 10. Revision history

Date	Revision	Changes
11-Sep-2006	8	Complete document
15-Nov-2006	9	The document has been reformatted
30-Jan-2007	10	Typo mistake on *Table 2*
14-Dec-2012	11	– Typo mistake on *Table 2* – Updated: *Section 4: Package mechanical data*
22-Jul-2013	12	– Updated *Table 1: Device summary*. – Minor text changes.

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