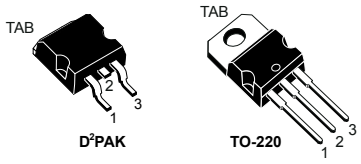
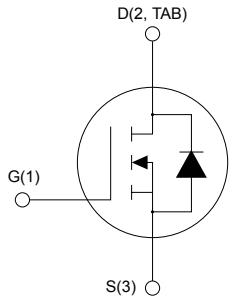
STB20NM50T4, STP20NM50

Datasheet

N-channel 500 V, 200 mΩ typ., 20 A MDmesh II Power MOSFETs in D²PAK and TO-220 packages





Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STB20NM50T4	500 V	250 mΩ	20 A
STP20NM50			

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

Applications

- Switching applications

Description

These devices are N-channel Power MOSFETs developed using the second generation of MDmesh technology. These revolutionary Power MOSFETs associate a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. They are therefore suitable for the most demanding high-efficiency converters.

Product status links
STB20NM50T4
STP20NM50

Product summary	
Order code	**STB20NM50T4**
Marking	B20NM50
Package	D²PAK
Packing	Tape and reel
Order code	**STP20NM50**
Marking	P20NM50
Package	TO-220
Packing	Tube

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	500	V
V_{GS}	Gate-source voltage	±30	V
I_D	Drain current (continuous) at T_C = 25 °C	20	A
I_D	Drain current (continuous) at T_C = 100 °C	12.6	A
I_{DM}(1)	Drain current (pulsed)	80	A
P_{TOT}	Total power dissipation at T_C = 25 °C	192	W
dv/dt(2)	Peak diode recovery voltage slope	15	V/ns
T_{stg}	Storage temperature range	-65 to 150	°C
T_J	Operating junction temperature range		°C

1. *Pulse width limited by safe operating area.*
2. *I_{SD} ≤ 20 A, di/dt ≤ 400 A/µs, $V_{DS}(peak)$ ≤ $V_{(BR)DSS}$, V_{DD} = 400 V.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	0.65	°C/W
R_{thJA}	Thermal resistance, junction-to-ambient	62.5	°C/W

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_J max.)	10	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	650	mJ

2 Electrical characteristics

T_C = 25 °C unless otherwise specified.

Table 4. On/off states

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0 V	500			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 500 V			1	µA
		V_{GS} = 0 V, V_{DS} = 500 V, T_C = 125 °C(1)			10	µA
I_{GSS}	Gate body leakage current	V_{DS} = 0 V, V_{GS} = ±30 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 10 A		200	250	mΩ

1. *Specified by design, not tested in production.*

Table 5. Dynamic

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
g_{fs}(1)	Forward transconductance	V_{DS} = 15 V, I_D = 10 A	-	10		S
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0 V	-	1480		pF
C_{oss}	Output capacitance		-	285		pF
C_{rss}	Reverse transfer capacitance		-	34		pF
$C_{oss\ eq.}$(2)	Equivalent output capacitance	V_{DS} = 0 to 400 V, V_{GS} = 0 V	-	130		pF
R_g	Gate input resistance	f = 1 MHz, open drain	-	1.6		Ω
Q_g	Total gate charge	V_{DD} = 400 V, I_D = 20 A, V_{GS} = 0 to 10 V (see the Figure 13. Test circuit for gate charge behavior)	-	40	56(3)	nC
Q_{gs}	Gate-source charge		-	13		nC
Q_{gd}	Gate-drain charge		-	19		nC

1. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%.*
2. *$C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.*
3. *Specified by design, not tested in production.*

Table 6. Switching times

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 250 V, I_D = 10 A, R_G = 4.7 Ω, V_{GS} = 10 V (see the Figure 12. Test circuit for resistive load switching times and Figure 17. Switching time waveform)	-	24	-	ns
t_r	Rise time		-	16	-	ns
$t_{d(off)}$	Turn-off delay time		-	40	-	ns
t_f	Fall time		-	12	-	ns
$t_{r(Voff)}$	Off-voltage rise time	V_{DD} = 400 V, I_D = 20 A, R_G = 4.7 Ω, V_{GS} = 10 V (see the Figure 14. Test circuit for inductive load switching and diode recovery times)	-	9	-	ns
t_f	Fall time		-	8.5	-	ns
t_c	Cross-over time		-	23	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-	-	20	A
I_{SDM}(1)	Source-drain current (pulsed)		-	-	80	A
V_{SD}(2)	Forward on voltage	I_{SD} = 20 A, V_{GS} = 0 V	-	-	1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 20 A, di/dt = 100 V, V_{DD} = 100 V (see the Figure 14. Test circuit for inductive load switching and diode recovery times)	-	350		ns
Q_{rr}	Reverse recovery charge		-	4.6		µC
I_{RRM}	Reverse recovery current		-	26		A
t_{rr}	Reverse recovery time	I_{SD} = 20 A, di/dt = 100 A/µs, V_{DD} = 100 V T_J = 150 °C (see the Figure 14. Test circuit for inductive load switching and diode recovery times)	-	435		ns
Q_{rr}	Reverse recovery charge		-	5.9		µC
I_{RRM}	Reverse recovery current		-	27		A

1. *Pulse width limited by safe operating area.*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

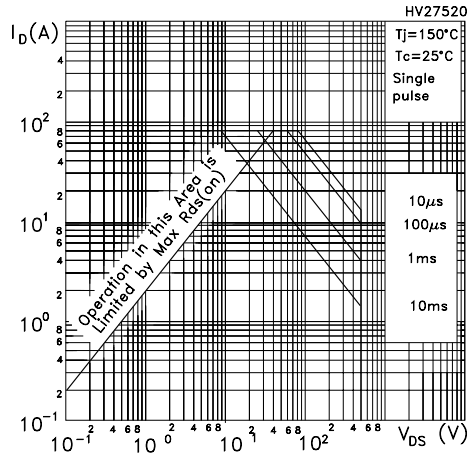


Figure 2. Normalized transient thermal impedance

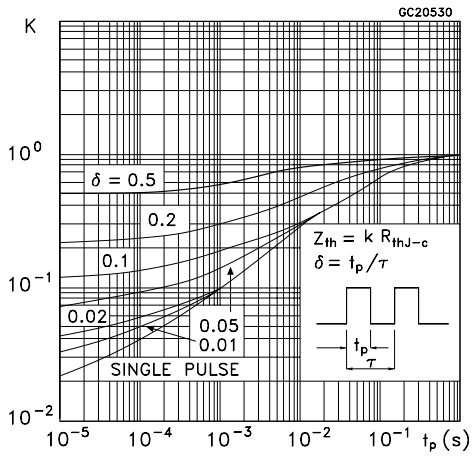


Figure 3. Typical output characteristics

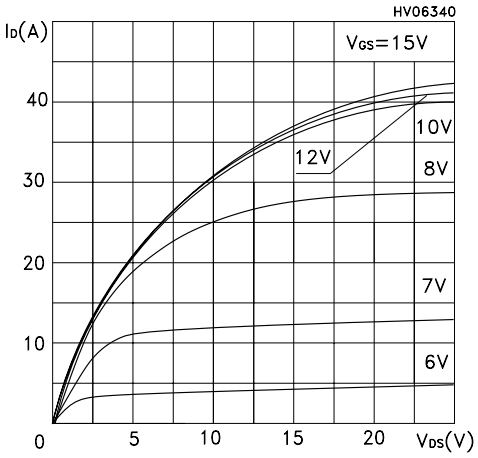


Figure 4. Typical transfer characteristics

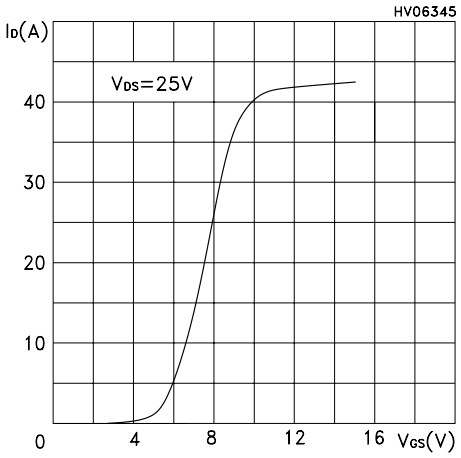


Figure 5. Typical transconductance characteristics

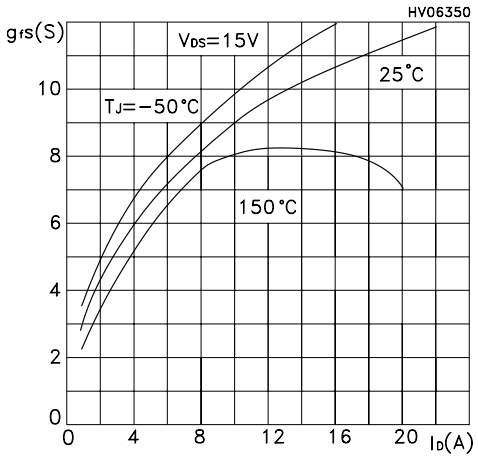


Figure 6. Typical gate charge vs gate-source voltage

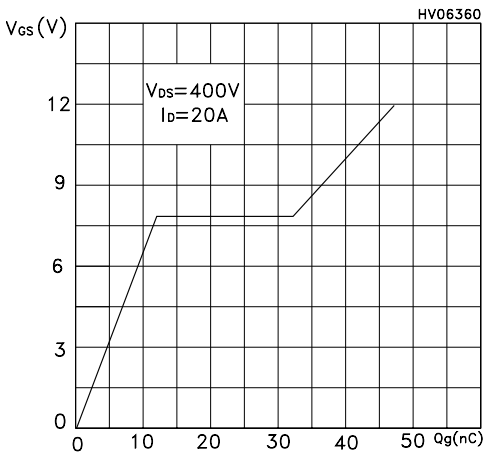


Figure 7. Typical drain-source on-resistance

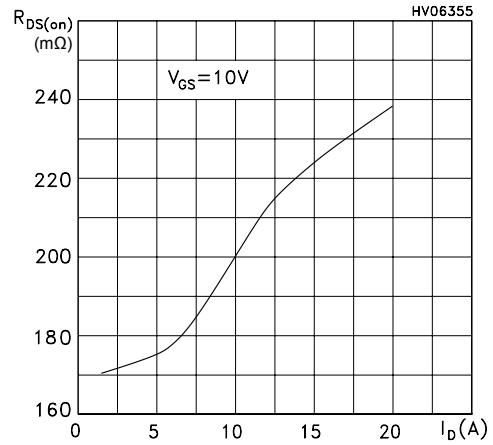


Figure 8. Typical capacitance characteristics

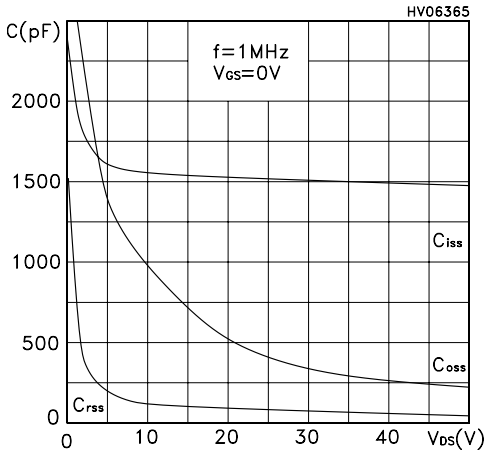


Figure 9. Normalized gate threshold vs temperature

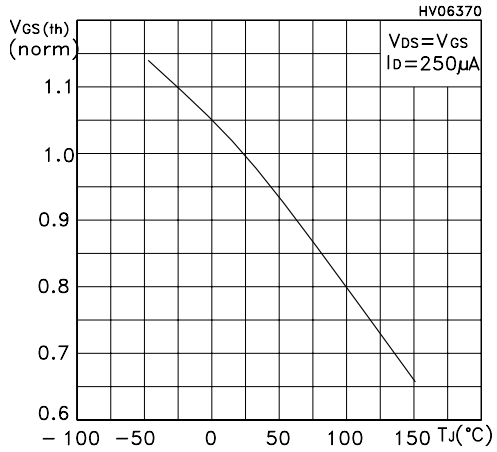


Figure 10. Normalized on-resistance vs temperature

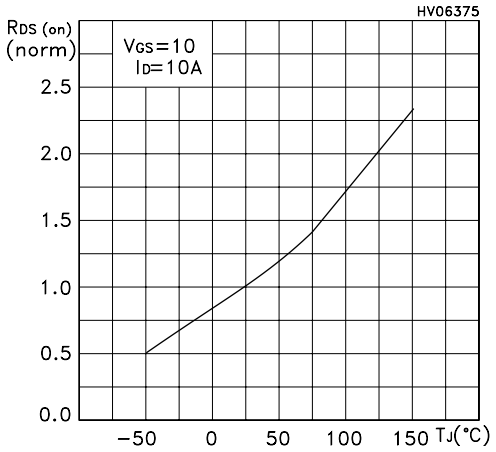
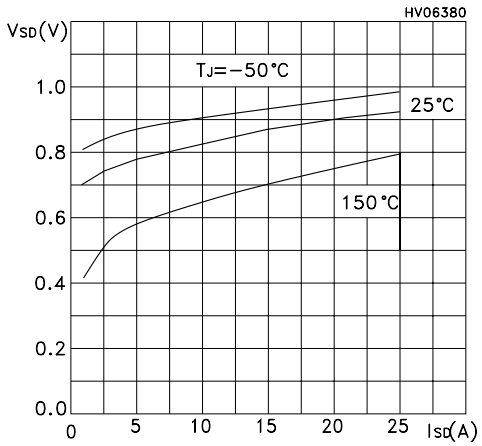
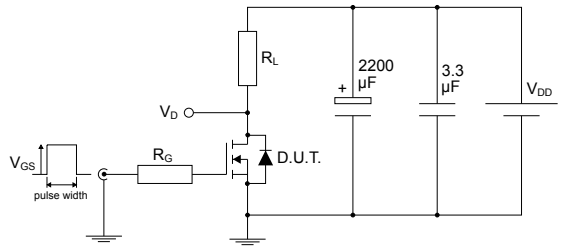


Figure 11. Typical reverse diode forward characteristics



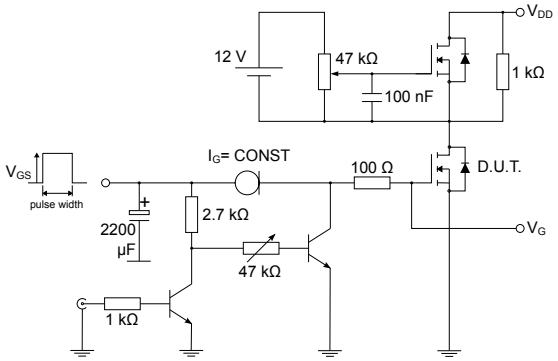
3 Test circuits

Figure 12. Test circuit for resistive load switching times



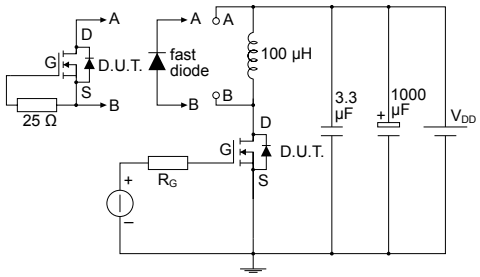
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Figure 13. Test circuit for gate charge behavior



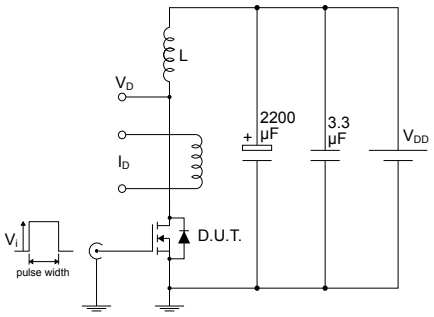
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Figure 14. Test circuit for inductive load switching and diode recovery times



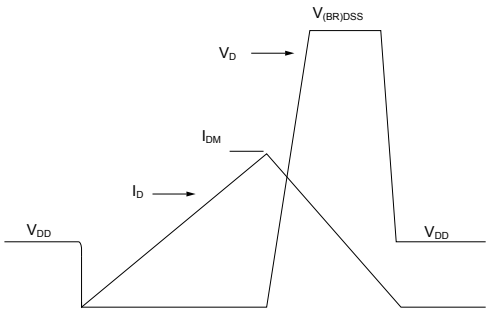
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Figure 15. Unclamped inductive load test circuit



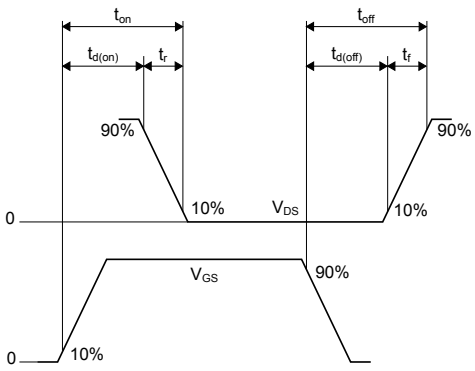
AM01471v1

Figure 16. Unclamped inductive waveform



AM01472v1

Figure 17. Switching time waveform



AM01473v1

4 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 D²PAK (TO-263) type A package information

Figure 18. **D²PAK (TO-263) type A package outline**

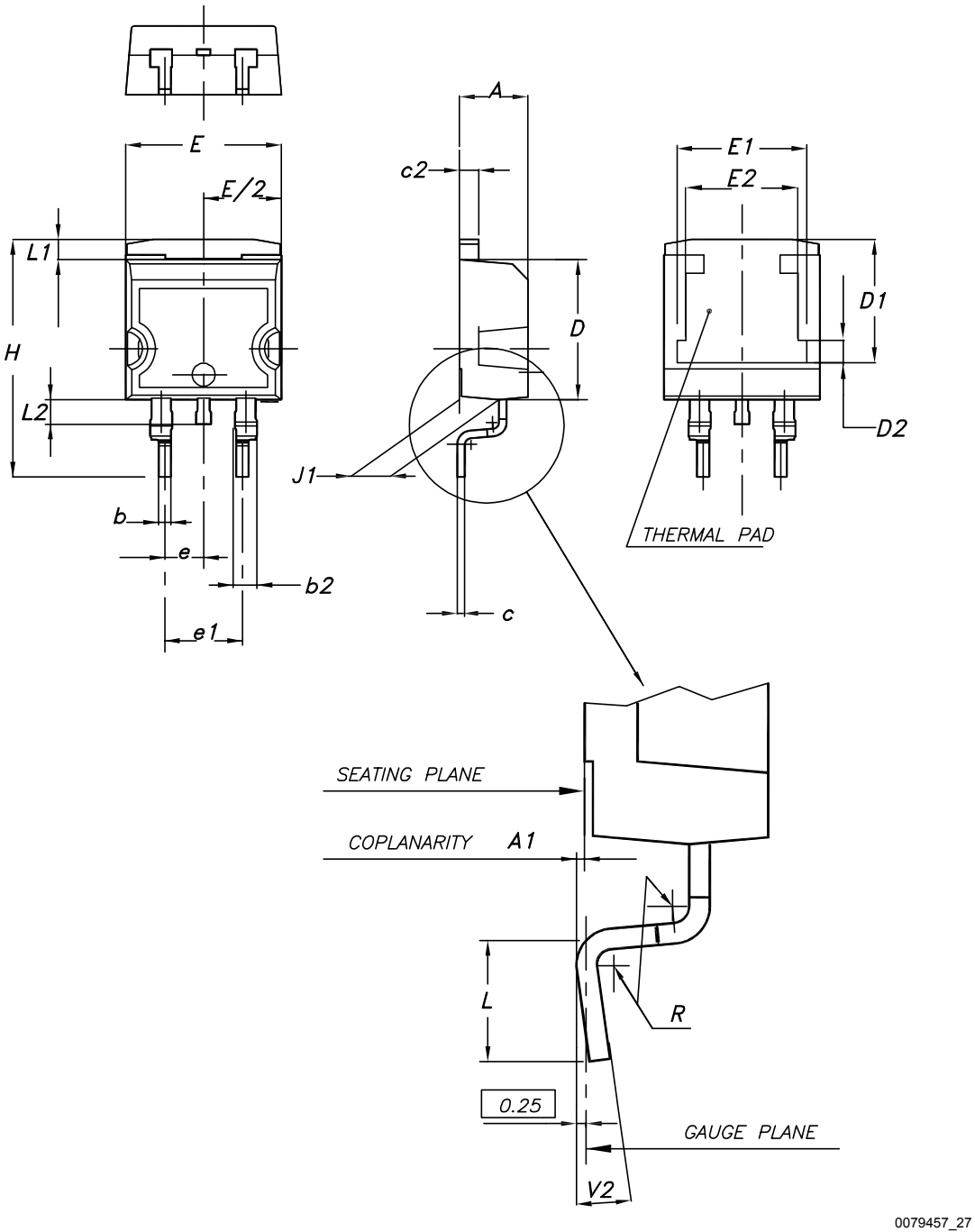
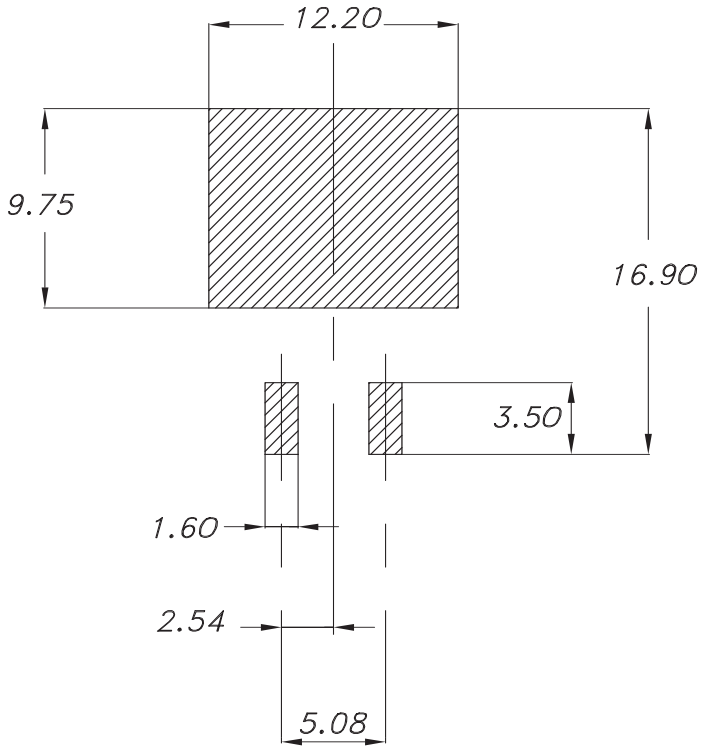


Table 8. D²PAK (TO-263) type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10.00		10.40
E1	8.30	8.50	8.70
E2	6.85	7.05	7.25
e		2.54	
e1	4.88		5.28
H	15.00		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.40	
V2	0°		8°

Figure 19. D²PAK (TO-263) recommended footprint (dimensions are in mm)



4.2 TO-220 type A package information

Figure 20. **TO-220 type A package outline**

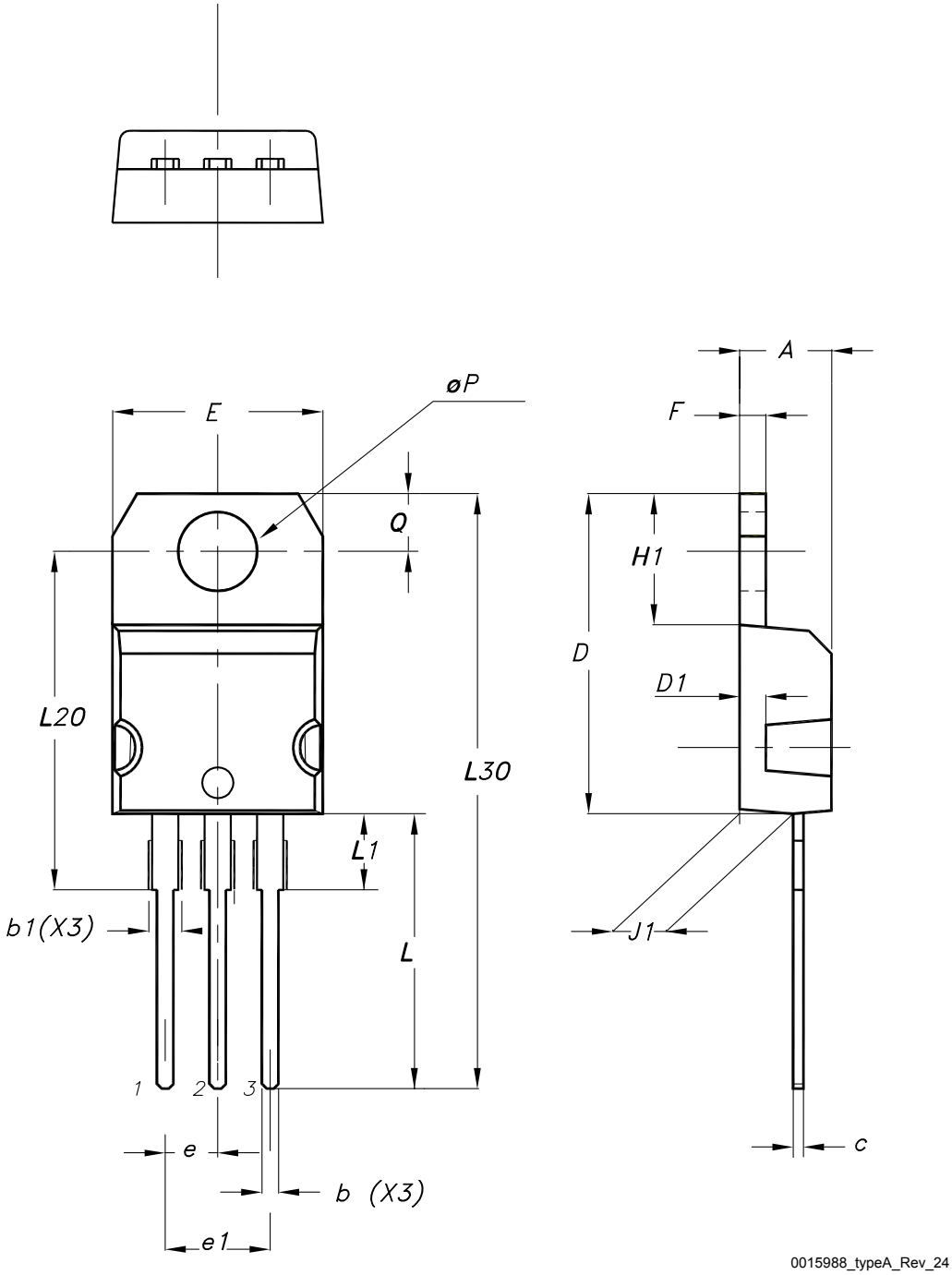
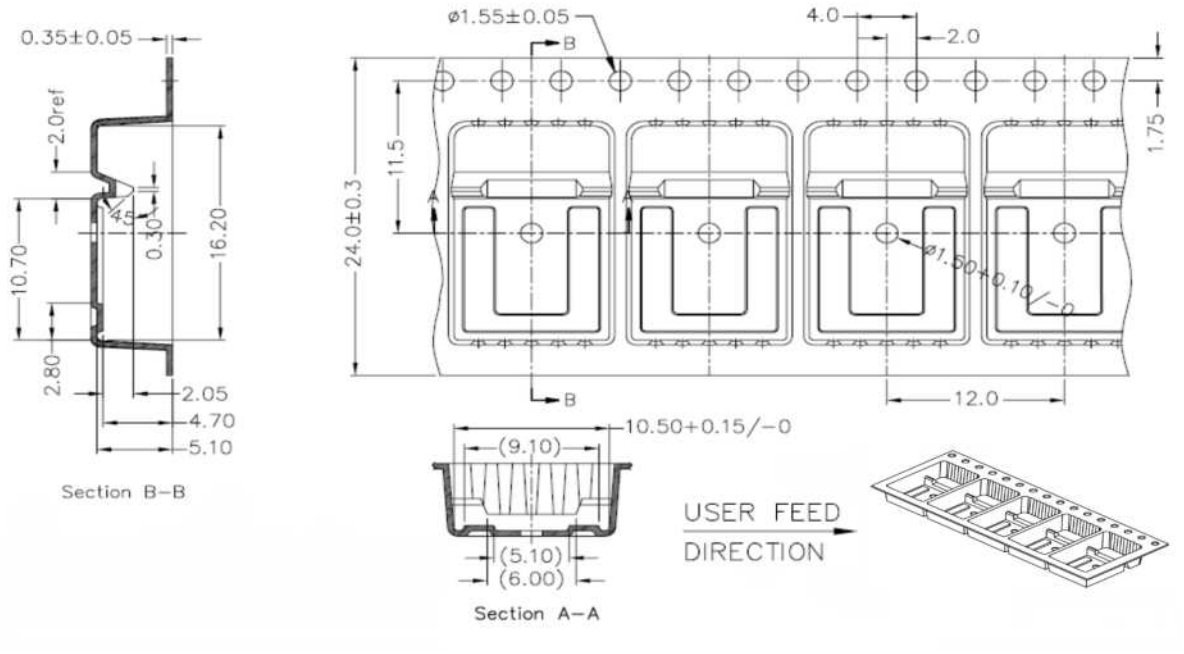


Table 9. **TO-220 type A package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95
Slug flatness		0.03	0.10

4.3 D²PAK packing information

Figure 21. **D²PAK tape drawing (dimensions are in mm)**



DM01095771_2

Revision history

Table 10. **Document revision history**

Date	Version	Changes
09-Sep-2004	9	Final version
04-Sep-2006	10	The document has been reformatted
15-Dec-2006	11	Modified *Table 7.: Source drain diode*
08-Jan-2007	12	Modified value in order code
26-Jan-2007	13	Modified *Table 6.: Switching times*
28-Jul-2025	14	The part numbers STB20NM50-1 and STP20NM50FP have been removed and the document has been updated accordingly. Updated Section 4: Package information. Minor text changes.

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