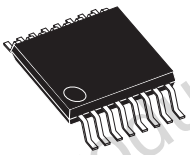
STLVDS31B

High speed differential line drivers

Features

- Meets or exceeds the requirements of ANSI TIA/EIA-644 standard
- Low voltage differential signaling with typical output voltage of 350 mV and a 100 Ω load
- Typical output voltage rise and fall times of 750 ps (400 Mbps)
- Typical propagation delay times of 1.7 ns
- Operates from a single 3.3 V supply
- Power dissipation 25 mW typical per driver at 200 MHz
- Driver at high impedance when disabled or with V_{CC} = 0 V
- Pin compatible with the AM26LS31, SN65LVDS31
- Low voltage TTL (LVTTL) logic input levels



TSSOP16

Description

The STLVDS31B is a quad differential line drivers that implements the electrical characteristics of low voltage differential signaling (LVDS). This signaling technique lowers the output voltage levels of 5 V differential standard levels (such as TIA/EIA-422B) to reduce the power, increase the switching speeds and allows operations with a 3.3 V supply rail. Any of the four current mode drivers will deliver a minimum differential output voltage magnitude of 247 mV into a 100 Ω load when enabled.

The intended application of this device and signalling technique is for point-to-point baseband data transmission over controlled impedancemedia approximately 100 Ω. The transmission media may be printed circuit board traces, backplanes or cables. The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media and noise coupling to the environment.

The STLVDS31B is characterized for operation from - 55 °C to 125 °C.

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Table 1. Device summary

Order code	Temperature range	Package	Packaging
STLVDS31BTR	- 40 to 85 °C	TSSOP16 (tape and reel)	2500 parts per reel

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Obsolete Product(s) - Obsolete Product(s)

1 Pin configuration

Figure 1. Pin connections and functional diagram

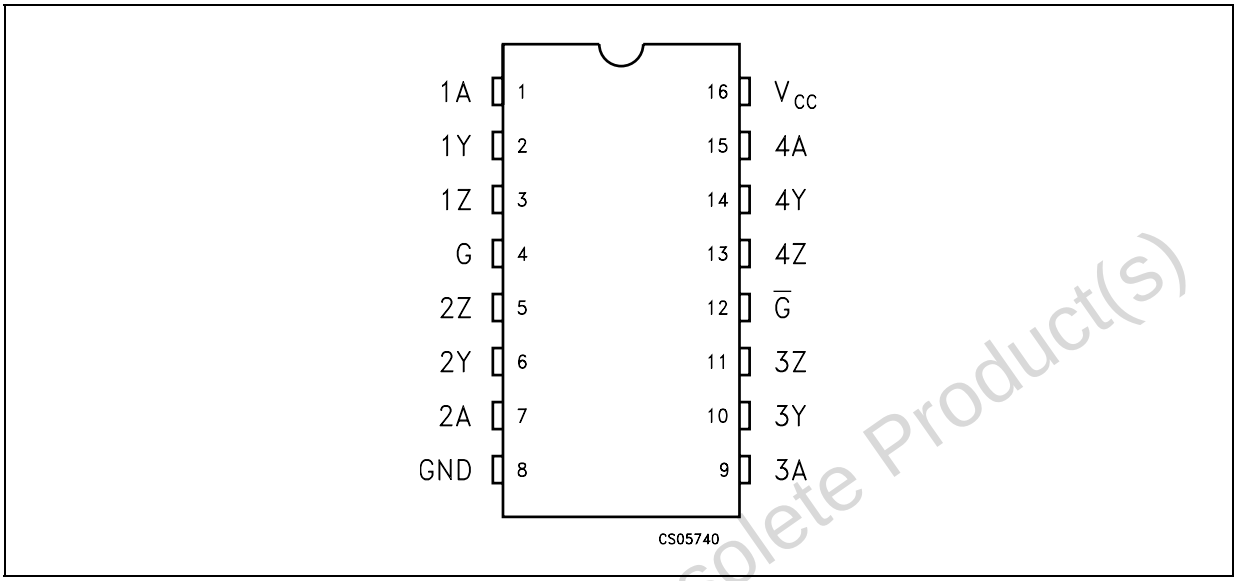

Table 2. Pin description

Pin n°	Symbol	Name and function
1, 7, 9, 15	1A to 4A	Driver inputs
2, 6, 10, 14	1Y to 4Y	Driver outputs
3, 5, 11, 13	1Z to 4Z	Driver outputs
4	G	Enable
12	G	Enable
8	GND	Ground
16	V_{CC}	Supply voltage

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Figure 2. Logic diagram and logic symbol

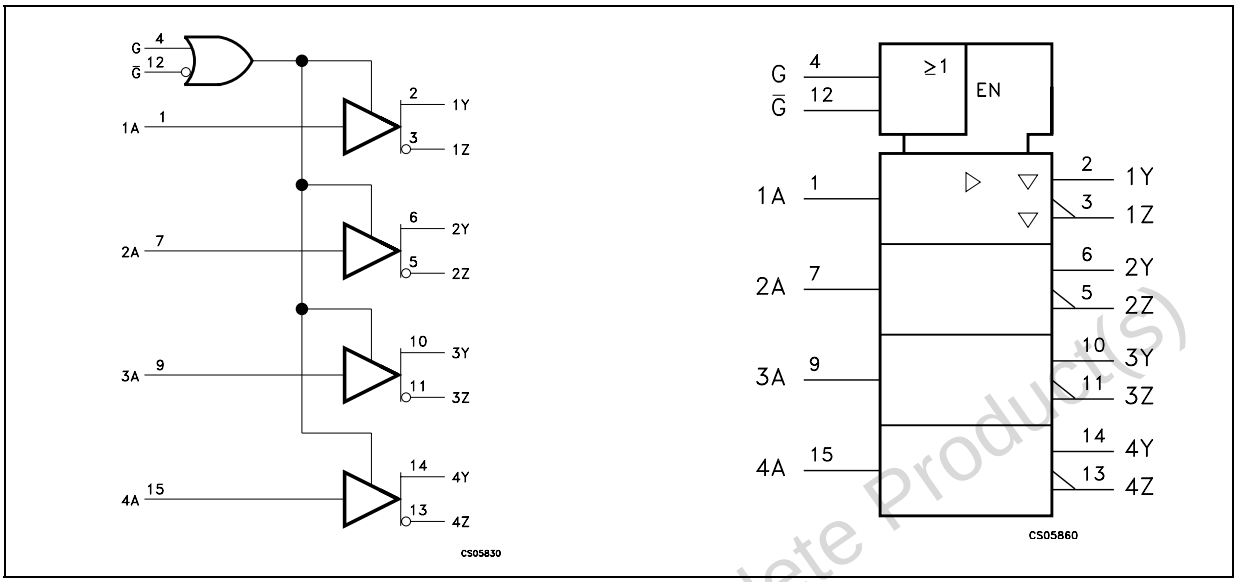

Table 3. Truth table for receiver

$V_{ID} = V_A - V_B$	R
$V_{ID} \geq 100$ mV	H
- 100 mV < V_{ID} < 100 mV	?
$V_{ID} \leq -100$ mV	L
OPEN	H

Table 4. Truth table

Input	Enables		Outputs	
A	G	$\overline{G}$	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z
OPEN	H	X	L	H
OPEN	X	L	L	H

L = Low level, H = High Level, X = Don't care, Z = High Impedance

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2 Maximum ratings

Table 5. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage (1)	-0.5 to 4.6	V
V_I	DC input voltage	-0.5 to (V_{CC} + 0.5)	V
T_{STG}	Storage temperature range	-65 to +150	°C

1. All voltages except differential I/O bus voltage, are with respect to the network ground terminal.

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

Table 6. Recommended operating conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage	3.0	3.3	3.6	V
V_{IH}	HIGH level input voltage	2.0			V
V_{ILI}	LOW level input voltage			0.8	V
T_A	Operating temperature range	-40		85	°C

Obsolete Product(s) - Obsolete Product(s)

3 Electrical characteristics

Over recommended operating conditions unless otherwise noted. All typical values are at T_A = 25 °C, and V_{CC} = 3.3 V.

Table 7. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{OD}	Differential output voltage	R_L = 100Ω, *Figure 2*	247	350	454	mV
ΔV_{OD}	Change in differential output voltage between logic state		-50		50	mV
$\Delta V_{OC(SS)}$	Change in steady-state common mode output voltage between logic state	*Figure 3*	1.125	1.2	1.375	V
$V_{OC(SS)}$	Steady-state common mode output voltage	*Figure 3*	-50		50	mV
$V_{OC(PP)}$	Peak to peak common mode output voltage			80	150	mV
I_{CC}	Supply current	V_{IN} = 0.8V or 2V, Enabled, No Load		11.5	20	mA
		V_{IN} = 0.8V or 2V, Enabled, R_L = 100Ω		25	35	mA
		V_{IN} = 0 or V_{CC}, Disabled		0.3	1	mA
I_{IH}	High level input current	V_{IH} = 2V		4	20	µA
I_{IL}	Low level input current	V_{IL} = 0.8V		0.6	10	µA
I_{SC}	Short circuit output current	$V_{O(Y)}$ or $V_{O(Z)}$ = 0V		6.1	- 24	mA
		V_{OD} = 0			± 12	mA
I_{OZ}	High impedance output current	V_O = 0 or 2.4V			± 1	µA
I_{CS}	Cold spare leakage current	V_I = 3.6V, V_{DD} = 0V			± 20	µA
I_{OFF}	Power OFF output current	V_{CC} = 0, V_O = 2.4V			± 1	µA
C_{IN}	Input capacitance			3		pF

Obsolete Product(s) - Obsolete Product(s)

Over recommended operating conditions unless otherwise noted. All typical values are at T_A = 25 °C, and V_{CC} = 3.3 V.

Table 8. Switching characteristics (1)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
t_{PLH}	Propagation delay time, low to high output	R_L = 100Ω, C_L = 10pF *Figure 2*	0.5	1.4	2	ns
t_{PHL}	Propagation delay time, high to low output		1	1.7	2.5	ns
t_r	Differential output signal rise time		0.4	0.5	0.6	ns
t_f	Differential output signal fall time		0.4	0.5	0.6	ns
$t_{sk(P)}$	Pulse skew ($\lvert t_{THL} = t_{TLH} \rvert$)			0.3	0.6	ns
$t_{sk(O)}$	Channel to channel output skew (2)			0	0.3	ns
t_{PZH}	Propagation delay time, high impedance to high level output	*Figure 4*		5.4	15	ns
t_{PZL}	Propagation delay time, high impedance to low level output			2.5	15	ns
t_{PHZ}	Propagation delay time, high level to high impedance output			8.1	15	ns
t_{PLZ}	Propagation delay time, low level to high impedance output			7.3	15	ns

1. RS-232 IN to TTL-CMOS OUT (from 50 % to 50 %).
2. $t_{sk(O)}$ is the maximum delay time difference between drivers on the same device.

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4 Typical characteristics

Figure 3. Voltage and current definitions

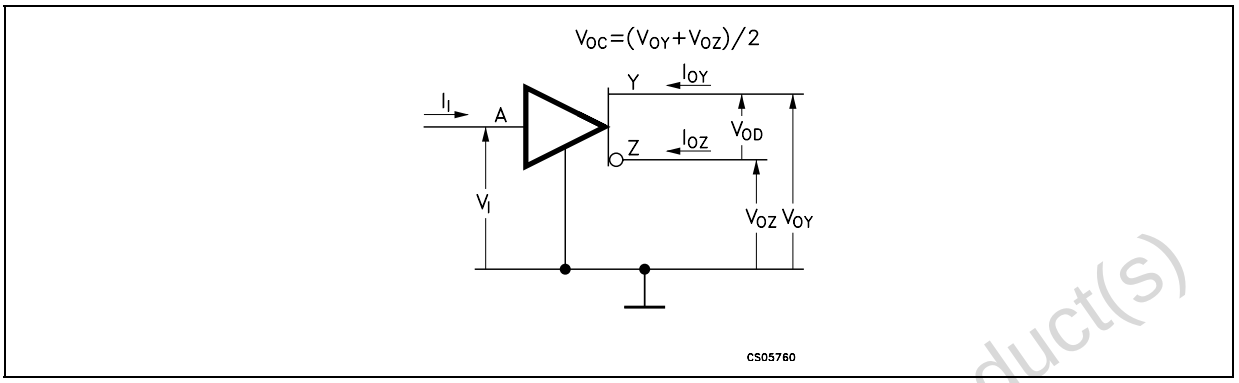
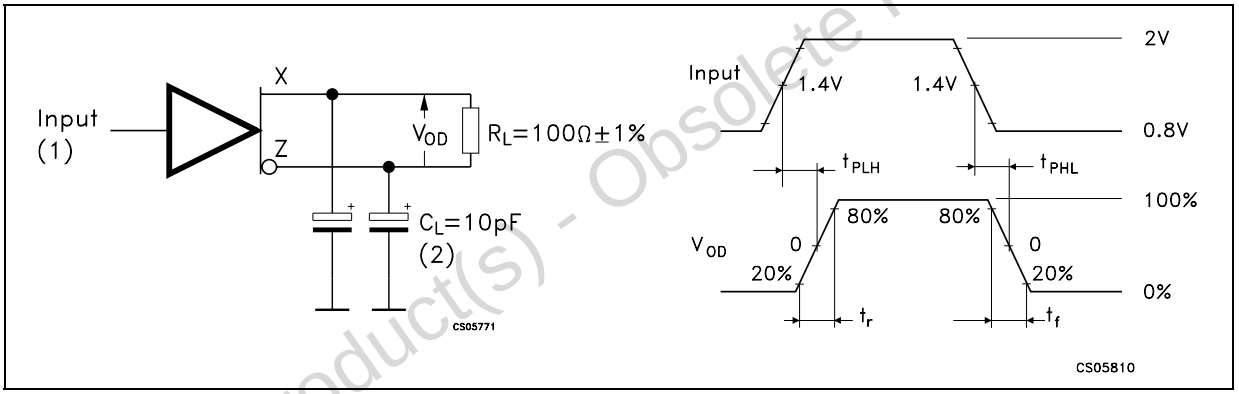
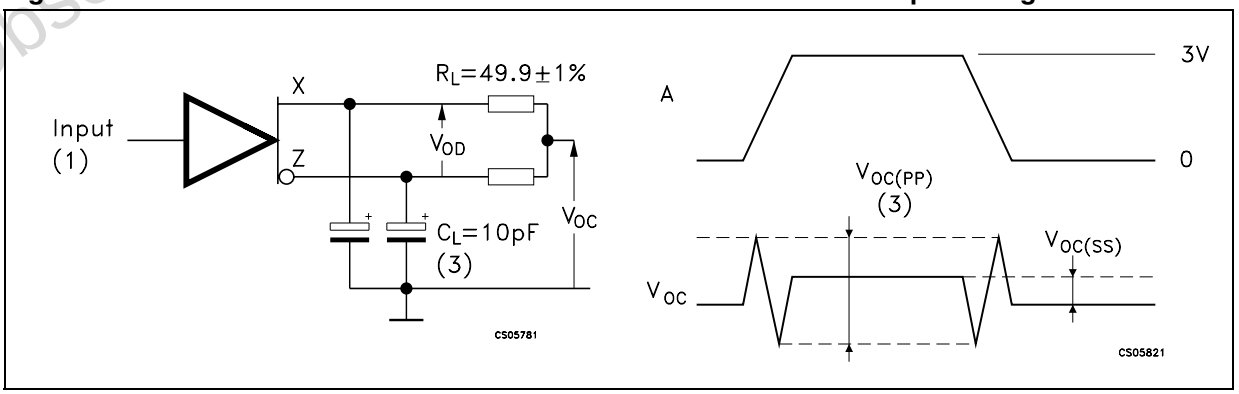


Figure 4. Test circuit, timing and voltage definitions for differential output signal



1. All input pulse are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ± 0.2 ns.
2. C_L includes instrumentation and fixture capacitance within 6 mm. of the D.U.T.

Figure 5. Test circuit and definitions for the driver common mode output voltage



1. All input pulse are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ± 0.2 ns.
2. C_L includes instrumentation and fixture capacitance within 6mm of the D.U.T
3. The measurement of $V_{OC(PP)}$ is made on test equipment with a -3 dB bandwidth of at least 300 MHz.

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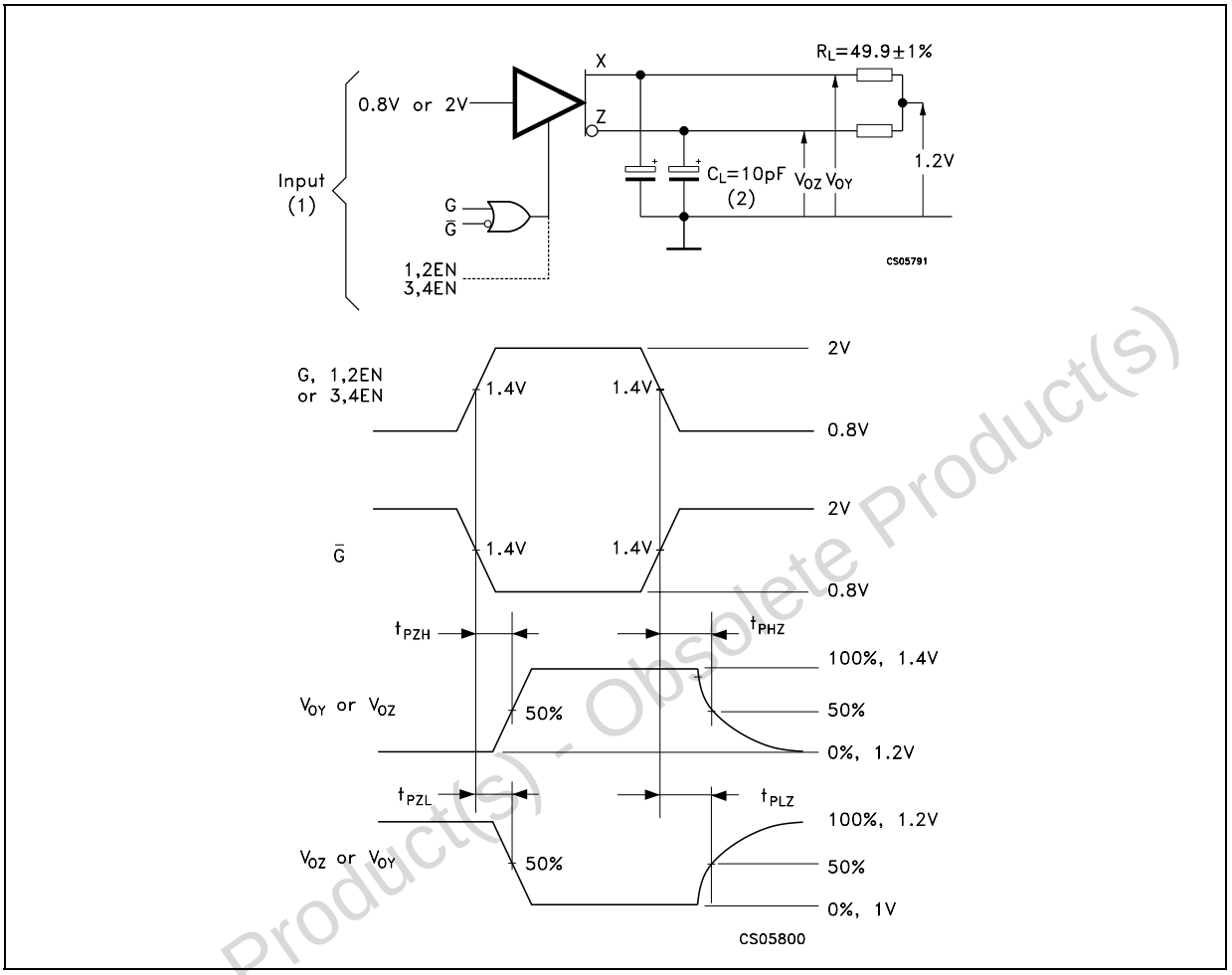
Figure 6. Enable and disable time test circuit and waveform



1. All input pulse are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ms.
2. C_L includes instrumentation and fixture capacitance within 6 mm. of the D.U.T.

Obsolete Product(s) - Obsolete Product(s)

5 Typical performance characteristics

Unless otherwise specified T_J = 25 °C

Figure 7. Supply current vs. temperature

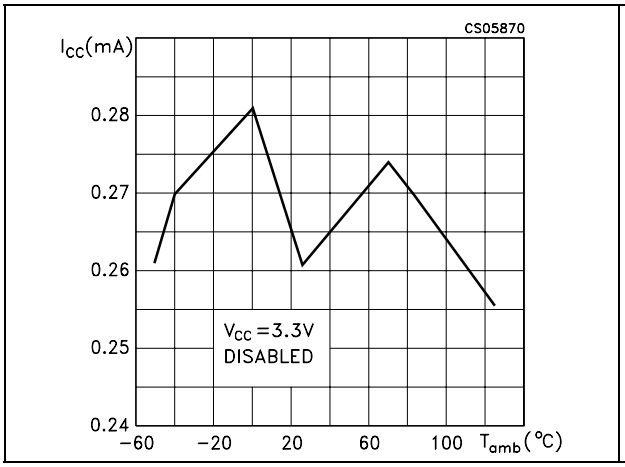


Figure 8. Supply current vs. temperature

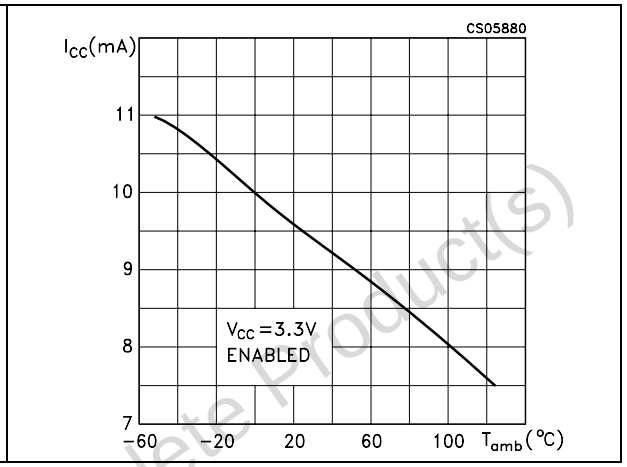


Figure 9. Propagation delay enable to output

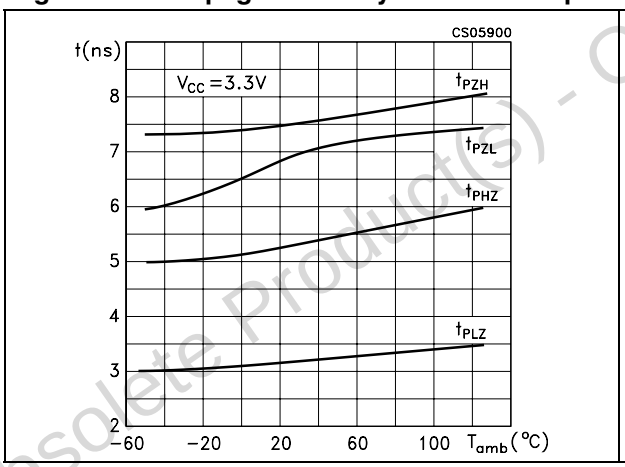


Figure 10. Propagation delay time

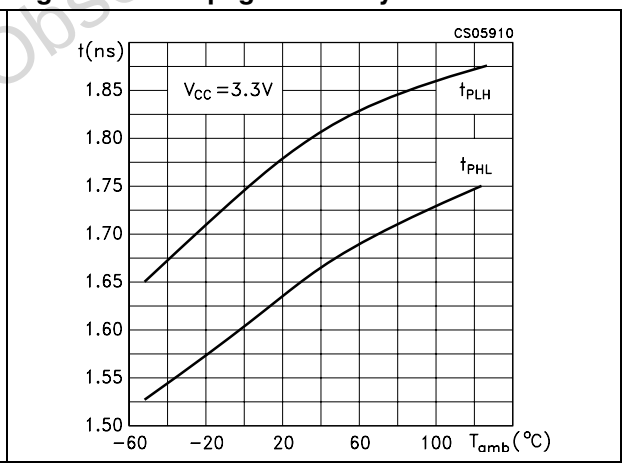
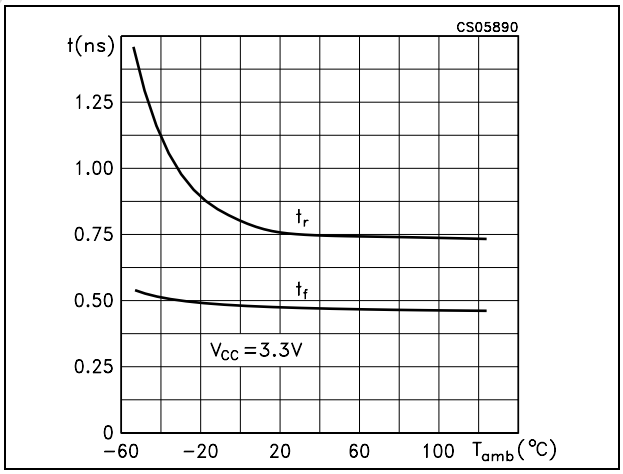


Figure 11. Differential output signal



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6 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

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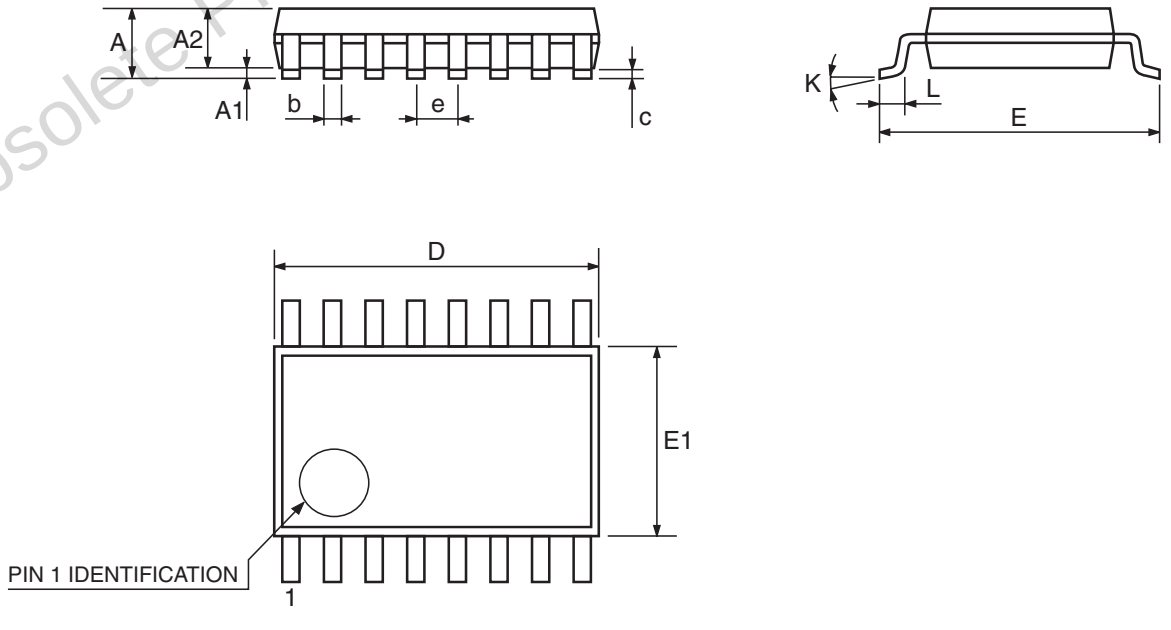
TSSOP16 mechanical data

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0079
D	4.9	5	5.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030



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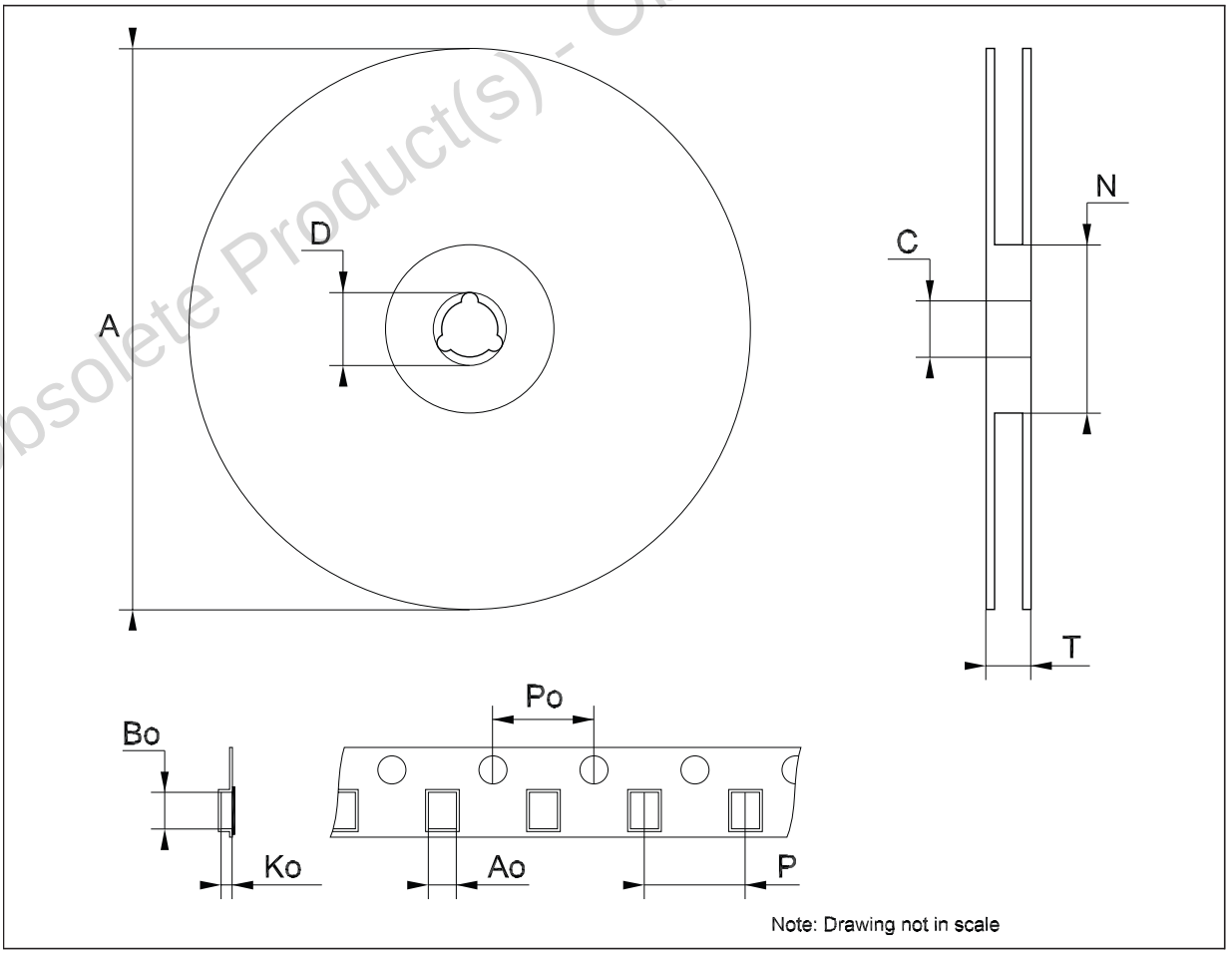
Tape & reel TSSOP16 mechanical data

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
Ao	6.7		6.9	0.264		0.272
Bo	5.3		5.5	0.209		0.217
Ko	1.6		1.8	0.063		0.071
Po	3.9		4.1	0.153		0.161
P	7.9		8.1	0.311		0.319



Note: Drawing not in scale

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7 Revision history

Table 9. Document revision history

Date	Revision	Changes
28-Mar-2006	5	Order codes updated.
15-Jul-2009	6	Modified: *Features on page 1*.

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