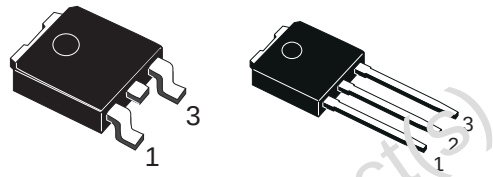
STD2NM60
STD2NM60-1

N-CHANNEL 600V - 2.8Ω - 2A DPAK/IPAK
Zener-Protected MDmesh™Power MOSFET

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
STD2NM60	600V	< 3.2 Ω	2 A
STD2NM60-1	600V	< 3.2 Ω	2 A

- TYPICAL $R_{DS}(on)$ = 2.8 Ω
- HIGH dv/dt AND AVALANCHE CAPABILITIES
- 100% AVALANCHE TESTED
- LOW INPUT CAPACITANCE AND GATE CHARGE
- LOW GATE INPUT RESISTANCE
- TIGHT PROCESS CONTROL AND HIGH MANUFACTORING YIELDS



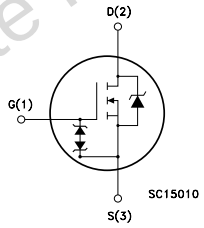
DPAK
TO-252

IPAK
TO-251

DESCRIPTION

The MDmesh™ is a new revolutionary MOSFET technology that associates the Multiple Drain process with the Company's PowerMESH™ horizontal layout. The resulting product has an outstanding low on-resistance, impressively high dv/dt and excellent avalanche characteristics. The adoption of the Company's proprietary strip technique yields overall dynamic performance that is significantly better than that of similar completition's products.

INTERNAL SCHEMATIC DIAGRAM



APPLICATIONS

The MDmesh™ family is very suitable for increase the power density of high voltage converters allowing system miniaturization and higher efficiencies.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage (V_{GS} = 0)	600	V
V_{DGR}	Drain-gate Voltage (R_{GS} = 20 kΩ)	600	V
V_{GS}	Gate- source Voltage	±30	V
I_D	Drain Current (continuous) at T_C = 25°C	2	A
I_D	Drain Current (continuous) at T_C = 100°C	1.26	A
I_{DM} (●)	Drain Current (pulsed)	8	A
P_{TOT}	Total Dissipation at T_C = 25°C	46	W
	Derating Factor	0.37	W/°C
$V_{ESD(G-S)}$	Gate source ESD(HBM-C=100pF, R=1.5KΩ)	1	kV
dv/dt(1)	Peak Diode Recovery voltage slope	15	V/ns
T_{stg}	Storage Temperature	–65 to 150	°C
T_j	Max. Operating Junction Temperature	150	°C

(•)Pulse width limited by safe operating area

(1)I_{SD}<2A, di/dt<400A/µs, V_{DD}<$V_{(BR)DSS}$, T_J<T_{JMAX}

Obsolete Product(s) - Obsolete Product(s)
Obsolete Product(s) - Obsolete Product(s)

THERMAL DATA

Rthj-case	Thermal Resistance Junction-case Max	2.73	°C/W
Rthj-amb	Thermal Resistance Junction-ambient Max	62.5	°C/W
T_l	Maximum Lead Temperature For Soldering Purpose	300	°C

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max)	0.5	A
E_{AS}	Single Pulse Avalanche Energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	250	mJ

ELECTRICAL CHARACTERISTICS (T_{CASE} = 25 °C UNLESS OTHERWISE SPECIFIED)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 1 mA, V_{GS} = 0	600			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating			1	µA
		V_{DS} = Max Rating, T_C = 125 °C			10	µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ± 20V			± 5	µA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250µA	3	4	5	V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10V, I_D = 1 A		2.8	3.2	Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward Transconductance	V_{DS} > $I_{D(on)}$ x $R_{DS(on)max}$, I_D = 2 A		1.4		S
C_{iss}	Input Capacitance	V_{DS} = 25V, f = 1 MHz, V_{GS} = 0		160		pF
C_{oss}	Output Capacitance			67		pF
C_{rss}	Reverse Transfer Capacitance			4		pF
R_G	Gate Input Resistance	f=1 MHz Gate DC Bias = 0 Test Signal Level = 20mV Open Drain		3.5		Ω

Note: 1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.

Obsolete Product(s) - Obsolete Product(s)

ELECTRICAL CHARACTERISTICS (CONTINUED)
SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	V_{DD} = 300V, I_D = 1 A R_G = 4.7Ω V_{GS} = 10V (see test circuit, Figure 3)		13 8		ns ns
Q_g	Total Gate Charge	V_{DD} = 480V, I_D = 2 A, V_{GS} = 10V		6	8.4	nC
Q_{gs}	Gate-Source Charge			1.8		nC
Q_{gd}	Gate-Drain Charge			3.3		nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$	Off-voltage Rise Time	V_{DD} = 480 V, I_D = 2 A, R_G = 4.7Ω, V_{GS} = 10V (see test circuit, Figure 5)		12		ns
t_f	Fall Time			25		ns
t_c	Cross-over Time			30		ns

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				2	A
I_{SDM} (2)	Source-drain Current (pulsed)				8	A
V_{SD} (1)	Forward On Voltage	I_{SD} = 2 A, V_{GS} = 0			1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} = 2 A, di/dt = 100A/µs, V_{DD} = 100 v, T_j = 25°C (see test circuit, Figure 5)		516 516 2		ns nC A
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} = 2 A, di/dt = 100A/µs, V_{DD} = 100 V, T_j = 150°C (see test circuit, Figure 5)		808 890 2.2		ns nC A

Note: 1. Pulsed: Pulse duration = 300 us, duty cycle 1.5 %.
2. Pulse width limited by safe operating area.

GATE-SOURCE ZENER DIODE

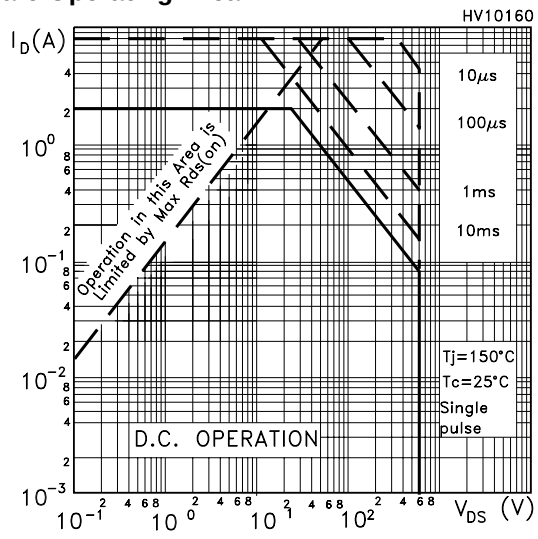
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BV_{GSO}	Gate-Source Breakdown Voltage	Igs=± 1mA (Open Drain)	30			V

PROTECTION FEATURES OF GATE-TO-SOURCE ZENER DIODES

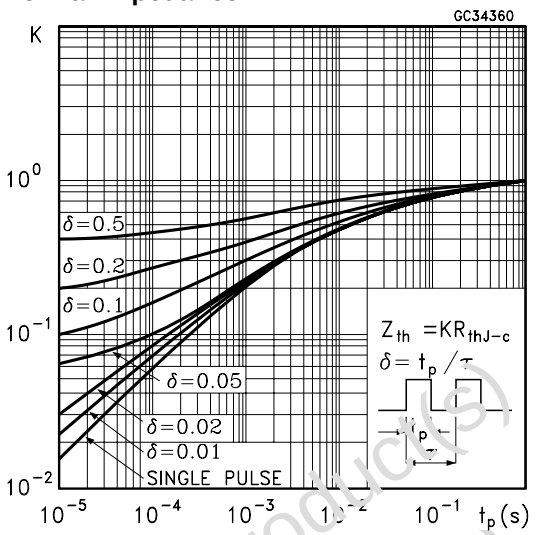
The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

Obsolete Product(s) - Obsolete Product(s)

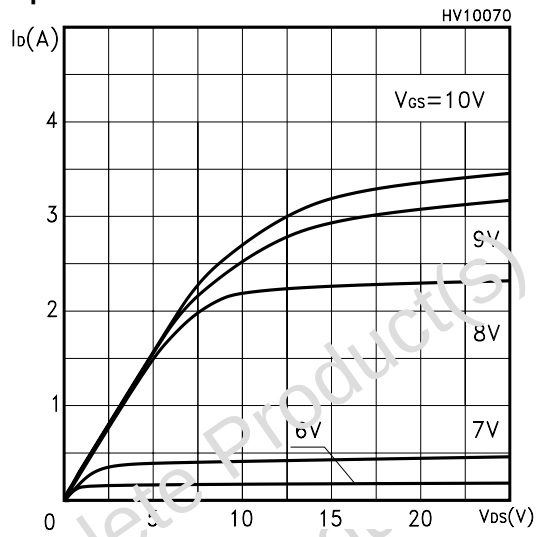
Safe Operating Area



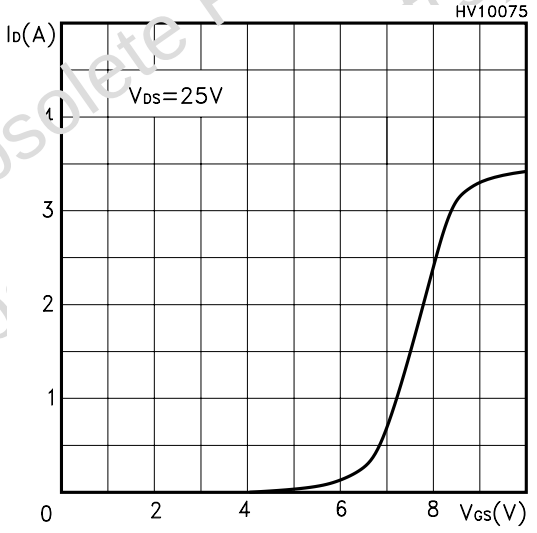
Thermal Impedance



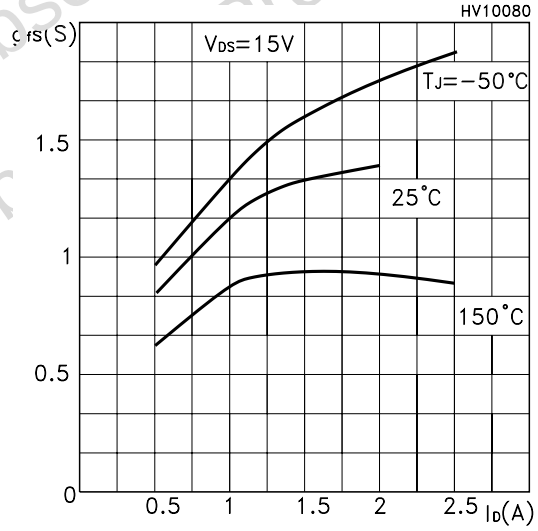
Output Characteristics



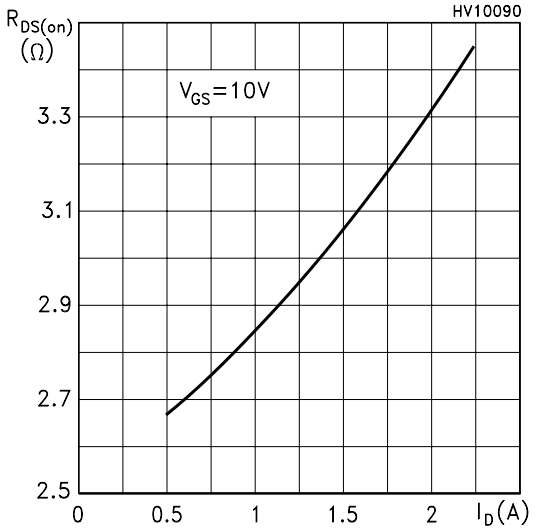
Transfer Characteristics



Transconductance

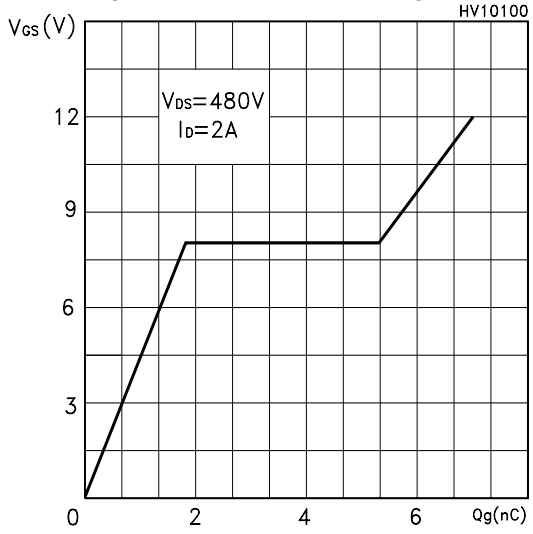


Static Drain-source On Resistance

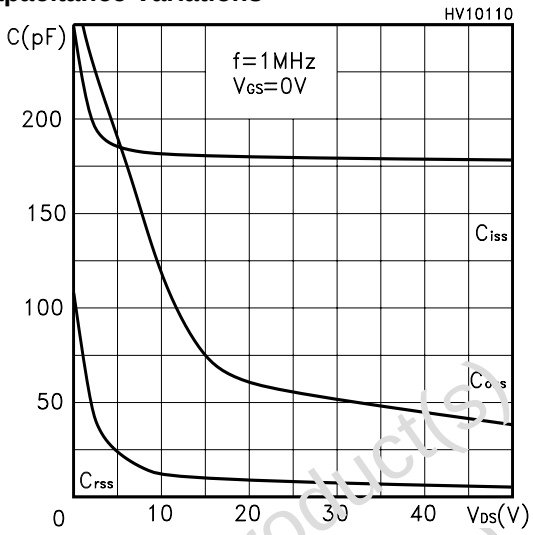


Obsolete Product(s) - Obsolete Product(s)

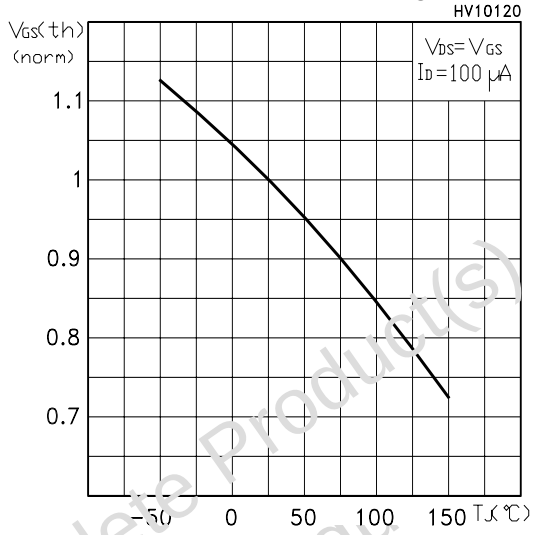
Gate Charge vs Gate-source Voltage



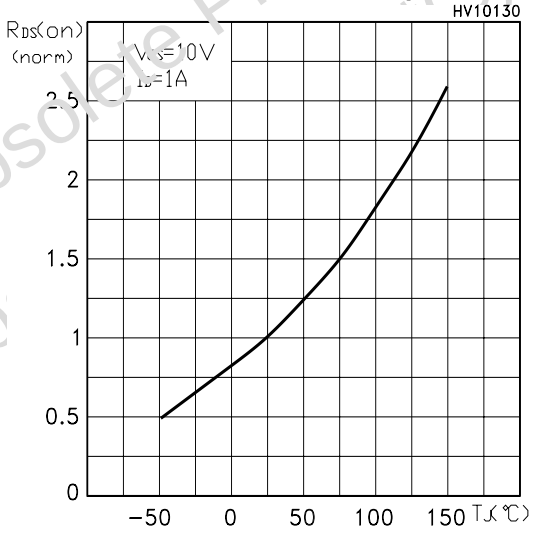
Capacitance Variations



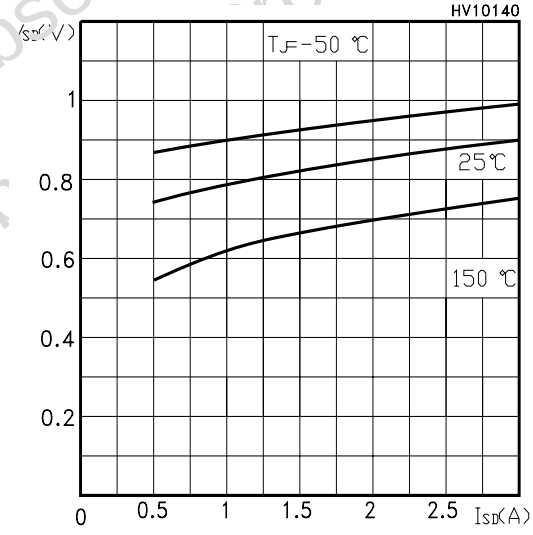
Normalized Gate Thereshold Voltage vs Temp.



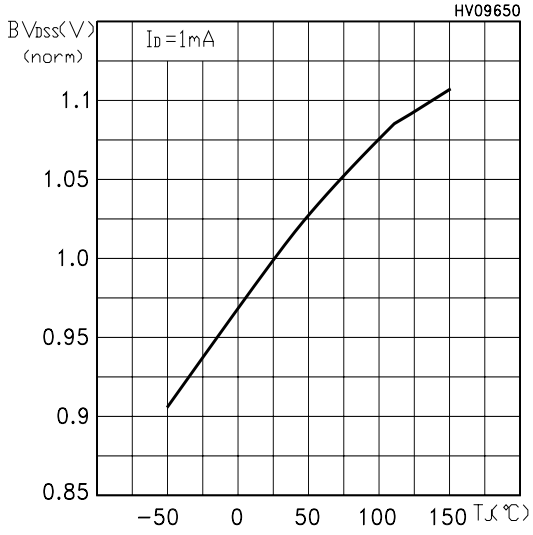
Normalized On Resistance vs Temperature



Source-drain Diode Forward Characteristics



Normalized BVDSS vs. Temperature



Obsolete Product(s) - Obsolete Product(s)

Fig. 1: Unclamped Inductive Load Test Circuit

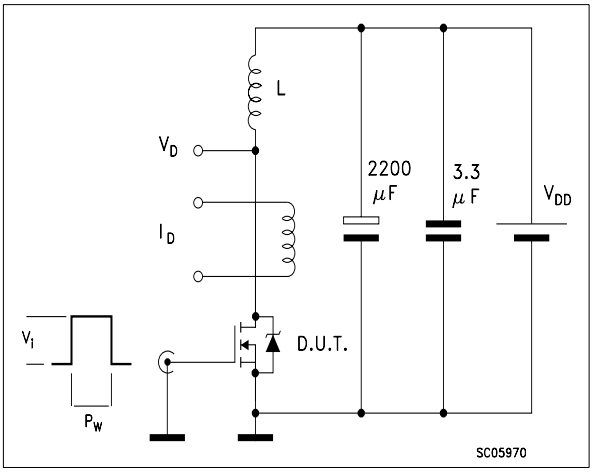


Fig. 2: Unclamped Inductive Waveform

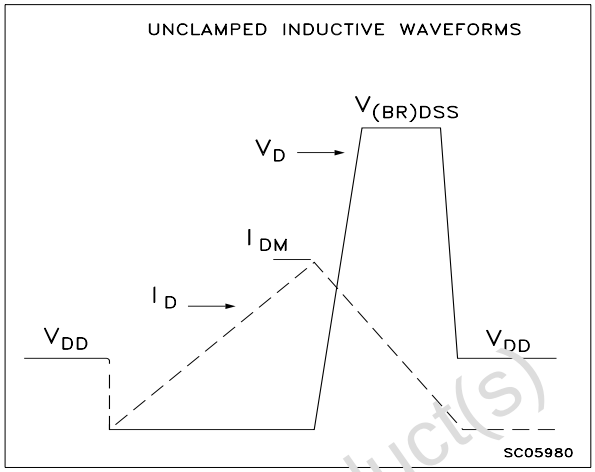


Fig. 3: Switching Times Test Circuit For Resistive Load

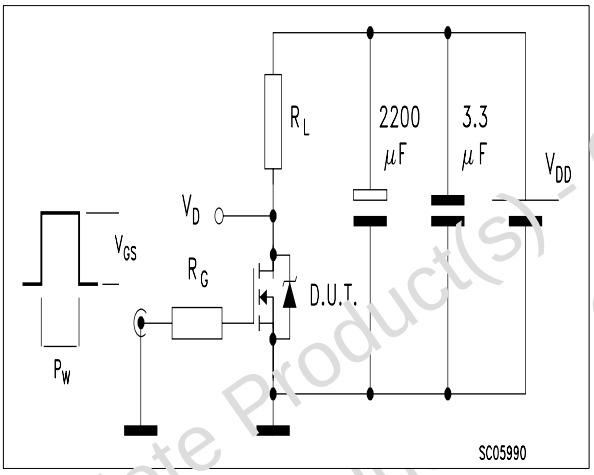


Fig. 4: Gate Charge test Circuit

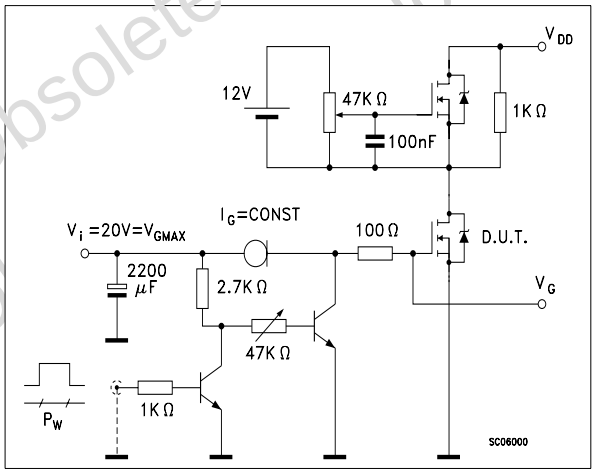
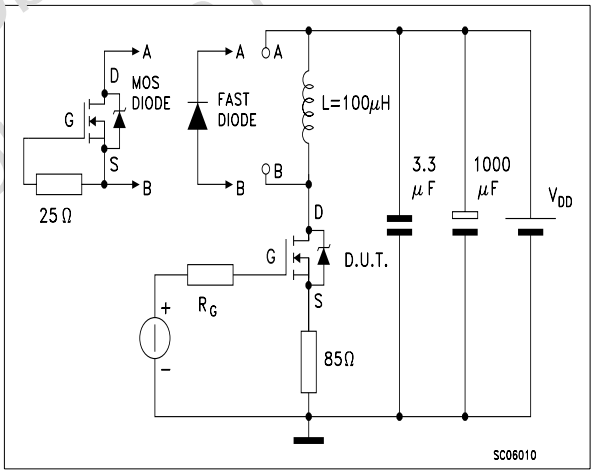


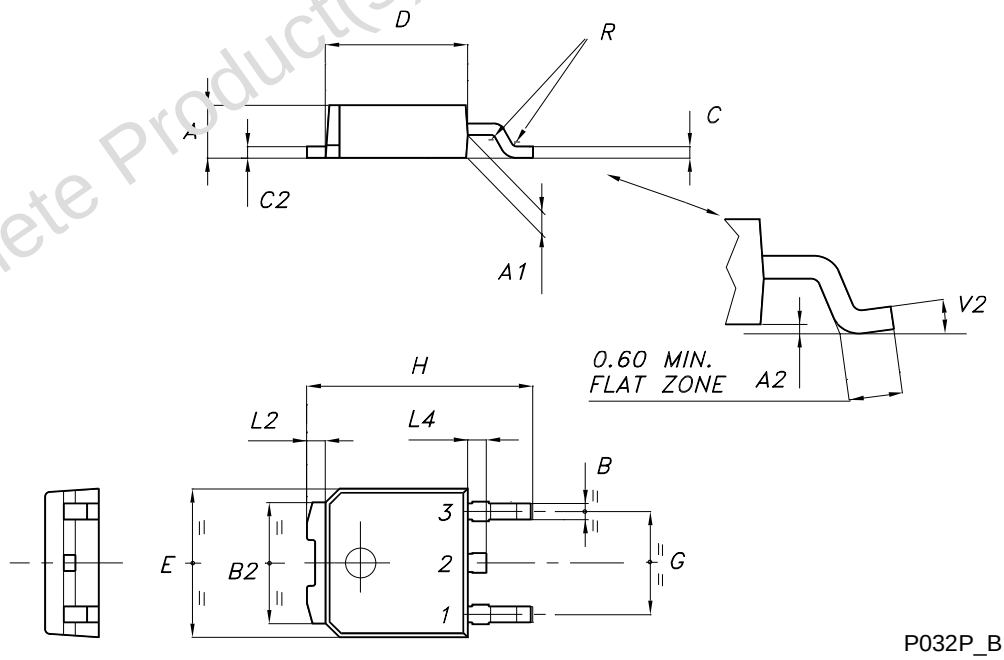
Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



Obsolete Product(s)

TO-252 (DPAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.20		2.40	0.087		0.094
A1	0.90		1.10	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.90	0.025		0.035
B2	5.20		5.40	0.204		0.213
C	0.45		0.60	0.018		0.024
C2	0.48		0.60	0.019		0.024
D	6.00		6.20	0.236		0.244
E	6.40		6.60	0.252		0.260
G	4.40		4.60	0.173		0.181
H	9.35		10.10	0.368		0.398
L2		0.8			0.031	
L4	0.60		1.00	0.024		0.039
V2	0°		8°	0°		0°

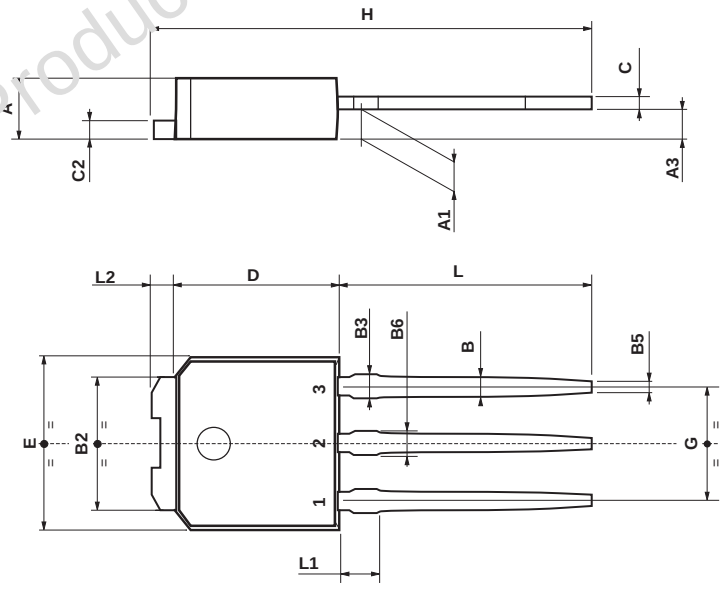


P032P_B

Obsolete Product(s) - Obsolete Product(s)

TO-251 (IPAK) MECHANICAL DATA

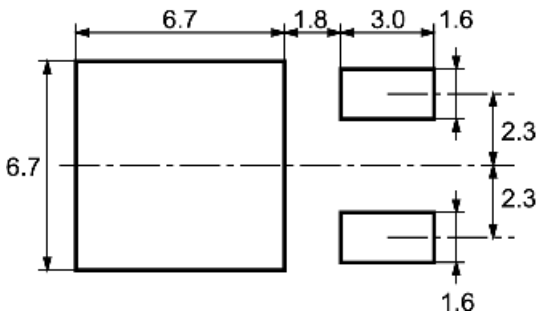
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A3	0.7		1.3	0.027		0.051
B	0.64		0.9	0.025		0.031
B2	5.2		5.4	0.204		0.212
B3			0.85			0.033
B5		0.3			0.012	
B6			0.95			0.037
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	15.9		16.3	0.626		0.641
L	9		9.4	0.354		0.370
L1	0.8		1.2	0.031		0.047
L2		0.8	1		0.031	0.039



0068771-E

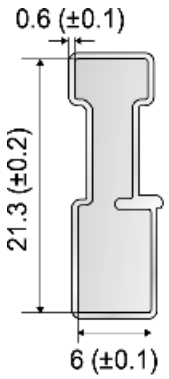
Obsolete Product(s) - Obsolete Product(s)

DPAK FOOTPRINT



All dimensions are in millimeters

TUBE SHIPMENT (no suffix)*



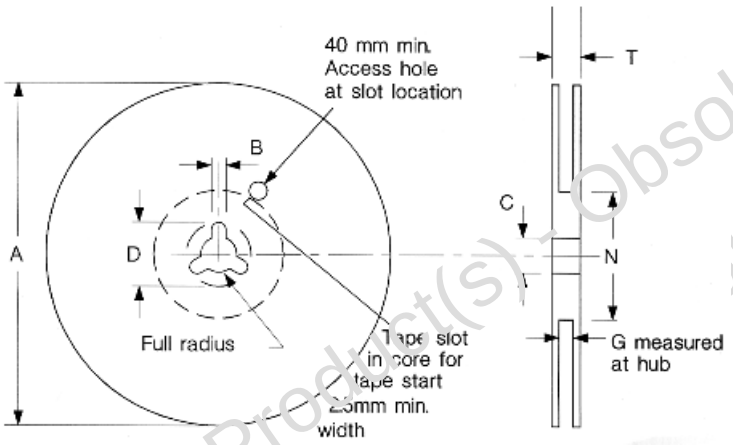
BASE QTY
75

BULK QTY
3000

Tube length 532 (±0.5)

All dimensions are in millimeters

TAPE AND REEL SHIPMENT (suffix "T4")*



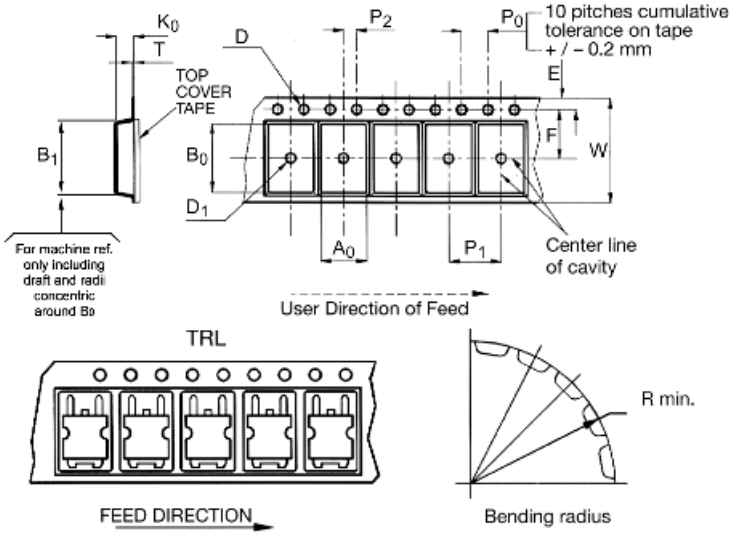
REEL MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0.795	
G	16.4	18.4	0.645	0.724
N	50		1.968	
T		22.4		0.881

BASE QTY	BULK QTY
2500	2500

TAPE MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	6.8	7	0.267	0.275
B0	10.4	10.6	0.409	0.417
B1		12.1		0.476
D	1.5	1.6	0.059	0.063
D1	1.5		0.059	
E	1.65	1.85	0.065	0.073
F	7.4	7.6	0.291	0.299
K0	2.55	2.75	0.100	0.108
P0	3.9	4.1	0.153	0.161
P1	7.9	8.1	0.311	0.319
P2	1.9	2.1	0.075	0.082
R	40		1.574	
W	15.7	16.3	0.618	0.641



Obsolete Product(s) - Obsolete Product(s)

* on sales type

Obsolete Product(s) - Obsolete Product(s)

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