STB150NF55
STP150NF55 - STW150NF55

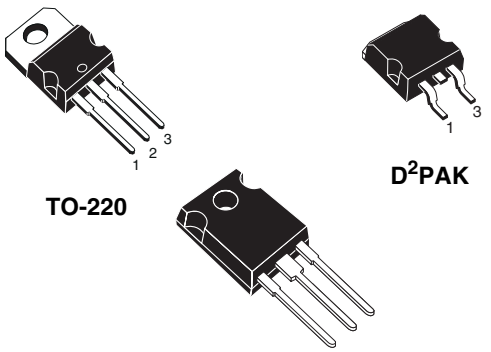
N-channel 55V - 0.005Ω - 120A - D²PAK/TO-220/TO-247
STripFET™ II Power MOSFET

General features

Type	V_{DSS}	$R_{DS(on)}$	I_D
STB150NF55	55V	<0.006Ω	120A(1)
STP150NF55	55V	<0.006Ω	120A(1)
STW150NF55	55V	<0.006Ω	120A(1)

1. Current limited by package

- 100% avalanche tested



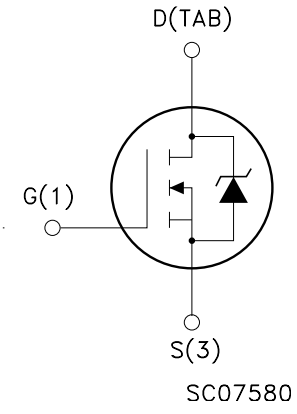
Description

This Power MOSFET is the latest development of STMicroelectronis unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

Applications

- Switching application

Internal schematic diagram



Order codes

Sales type	Marking	Package	Packaging
STB150NF55T4	B150NF55	D²PAK	Tape & reel
STP150NF55	P150NF55	TO-220	Tube
STW150NF55	W150NF55	TO-247	Tube

Contents

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2 Electrical characteristics 4

2.1 Electrical characteristics (curves) 6

3 Spice thermal model 10

4 Test circuit 11

5 Package mechanical data 13

6 Packaging mechanical data 17

7 Revision history 18

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = 0)	55	V
V_{DGR}	Drain-gate voltage (R_{GS} = 20 kΩ)	55	V
V_{GS}	Gate- source voltage	± 20	V
I_D (1)	Drain current (continuous) at T_C = 25°C	120	A
I_D (1)	Drain current (continuous) at T_C = 100°C	106	A
I_{DM} (2)	Drain current (pulsed)	480	A
P_{tot}	Total dissipation at T_C = 25°C	300	W
	Derating Factor	2	W/°C
dv/dt (3)	Peak diode recovery voltage slope	8	V/ns
E_{AS} (4)	Single pulse avalanche energy	850	mJ
T_{stg}	Storage temperature	-55 to 175	°C
T_j	Max. operating junction temperature		

1. Value limited by wire bonding
2. Pulse width limited by safe operating area.
3. $I_{SD} \leq 120A$, di/dt ≤200A/µs, $V_{DD} \leq V_{(BR)DSS}$, Tj ≤T_{JMAX}
4. Starting T_j = 25 °C, I_D = 60A, V_{DD} = 30V

Table 2. Thermal data

		TO-220	D²PAK	TO-247	
Rthj-case	Thermal resistance junction-case max	0.5			°C/W
Rthj-amb	Thermal resistance junction-ambient max	62.5	--	50	°C/W
Rthj-pcb	Thermal resistance junction-pcb max	see *Figure 15* and *Figure 16*			°C/W
T_J	Maximum lead temperature for soldering purpose (1)	300			°C

1. for 10 sec. 1.6mm from case

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250µA, V_{GS} =0	55			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = max ratings V_{DS} = max ratings, T_C = 125°C			1 10	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 20V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250µA	2		4	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10V, I_D = 60A		0.005	0.006	Ω

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} = 15V, I_D = 60A		160		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25V, f = 1MHz, V_{GS} = 0		4400 1050 350		pF pF pF
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off delay time Fall time	V_{DD} = 27.5V, I_D = 60A R_G = 4.7Ω V_{GS} = 10V (see *Figure 19*)		35 180 140 80		ns ns ns ns
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 27.5V, I_D = 120A, V_{GS} = 10V (see *Figure 20*)		140 35 70	190	nC nC nC

1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.

Table 5. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)				120 480	A A
V_{SD} (2)	Forward on voltage	I_{SD} = 120A, V_{GS} = 0			1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 120A, di/dt = 100A/µs, V_{DD} = 25V, T_j = 150°C (see *Figure 21*)		130 350 7.5		ns nC A

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

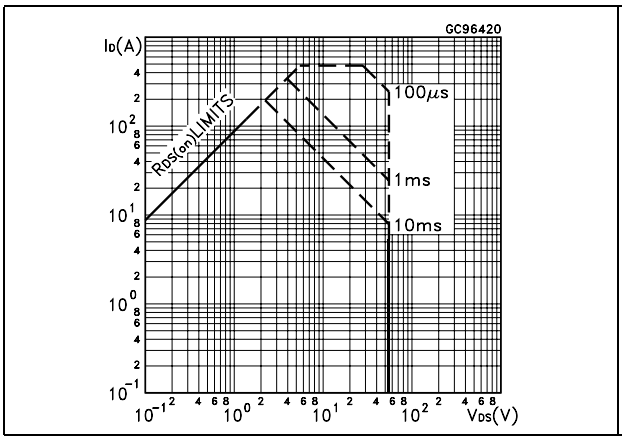


Figure 2. Thermal impedance

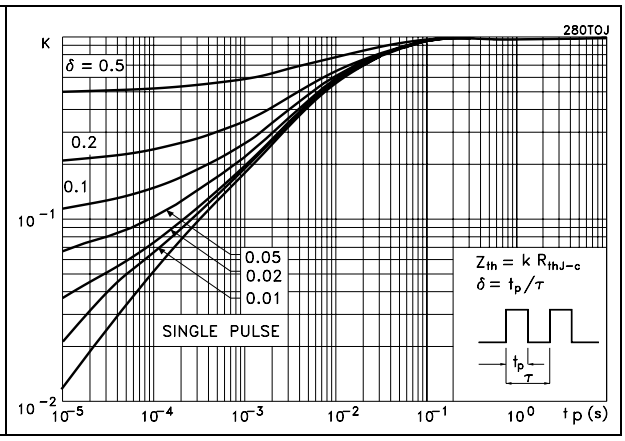


Figure 3. Output characterisics

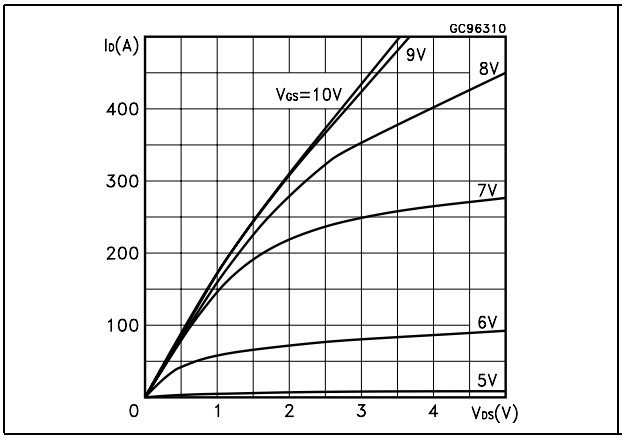


Figure 4. Transfer characteristics

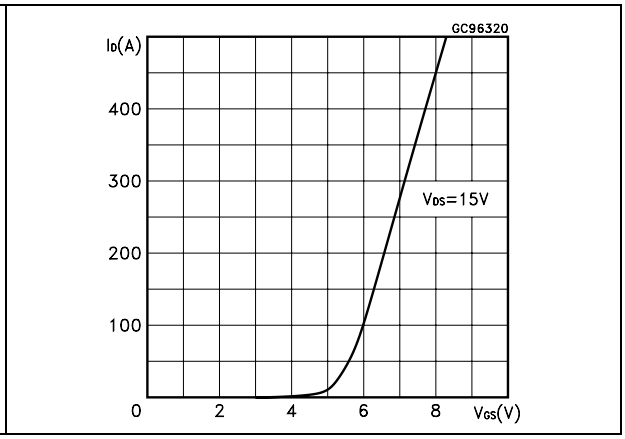


Figure 5. Transconductance

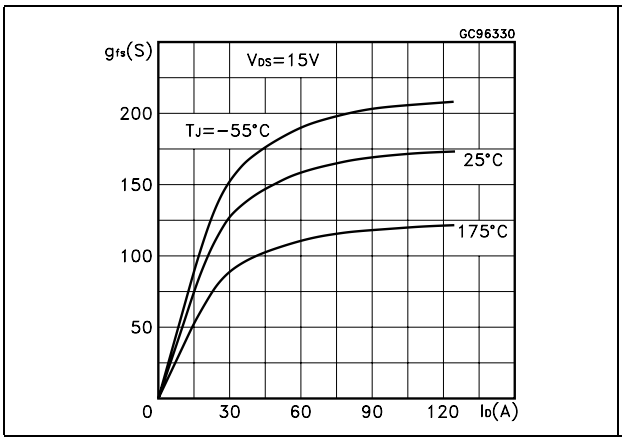


Figure 6. Static drain-source on resistance

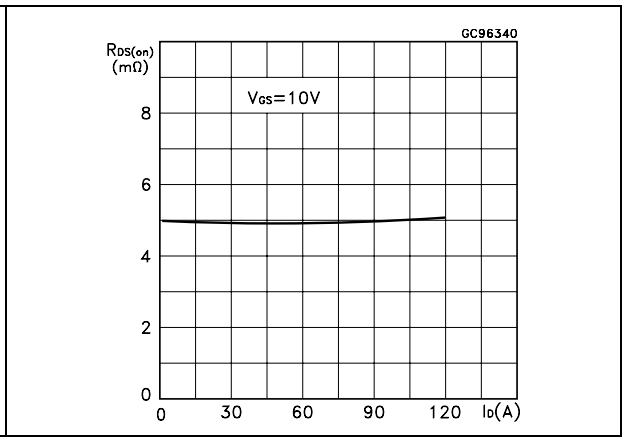


Figure 7. Gate charge vs gate-source voltage

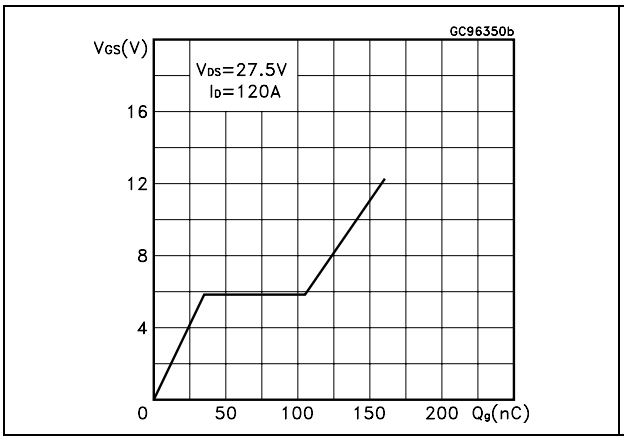


Figure 8. Capacitance variations

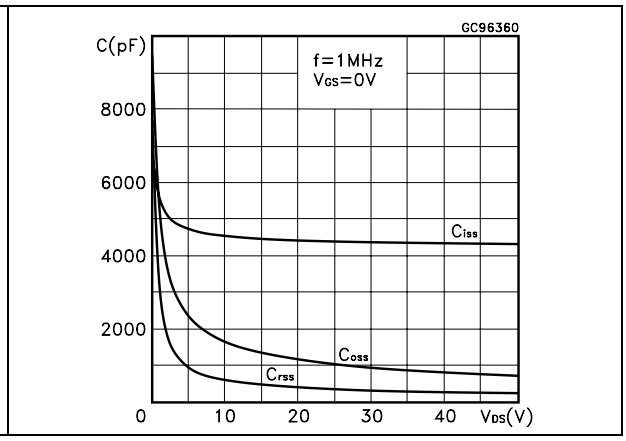


Figure 9. Normalized gate threshold voltage vs temperature

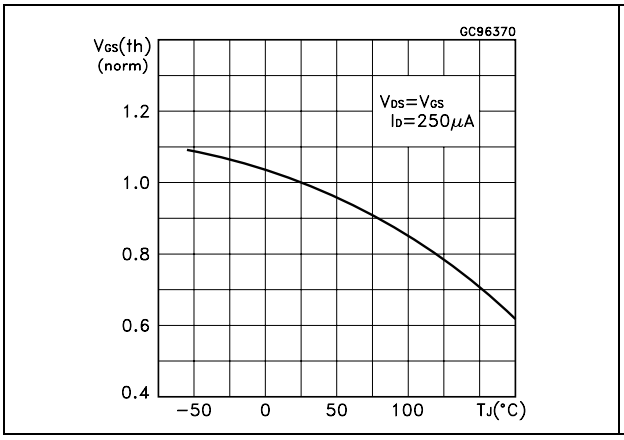


Figure 10. Normalized on resistance vs temperature

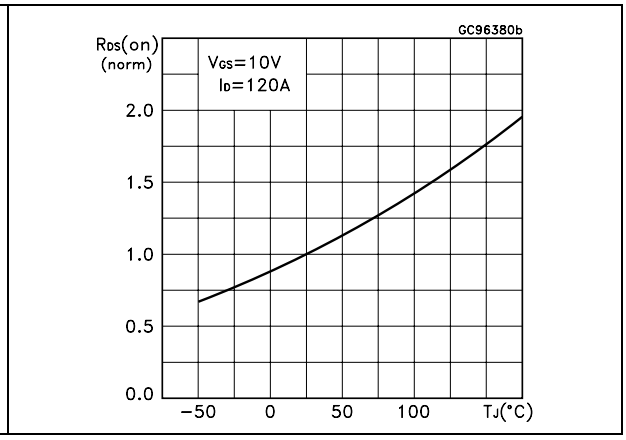


Figure 11. Source-drain diode forward characteristics

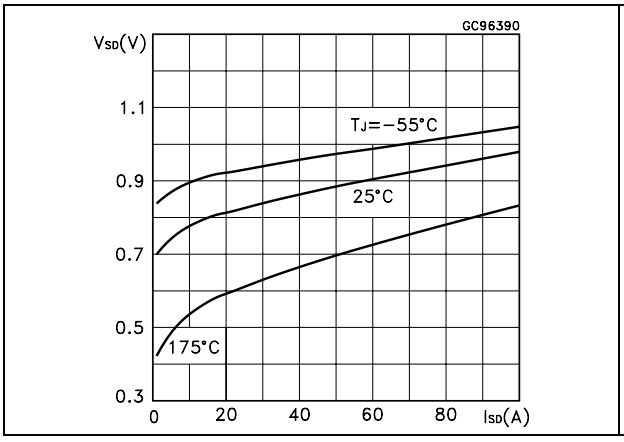


Figure 12. Normalized B_{VDSS} vs temperature

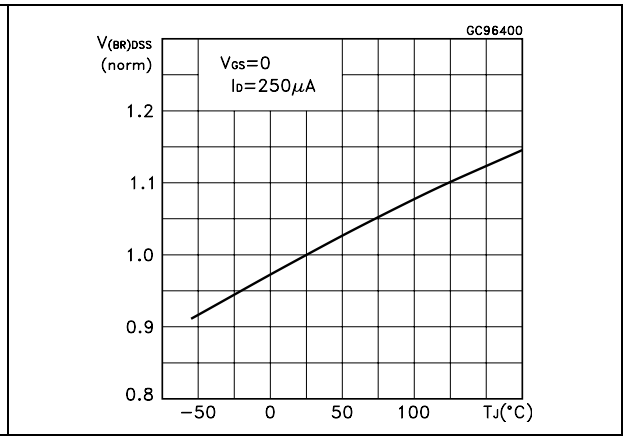


Figure 13. Power derating vs Tc

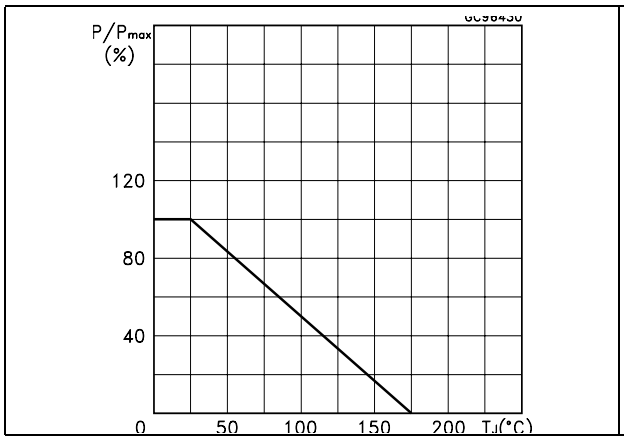


Figure 14. Max I_D current vs Tc

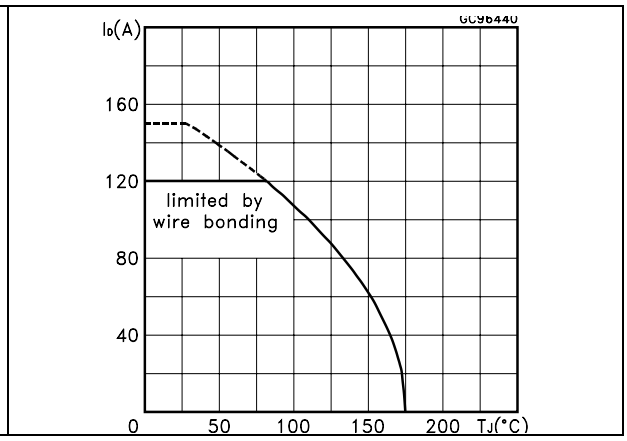


Figure 15. Thermal resistance R_{thj-a} vs PCB copper area

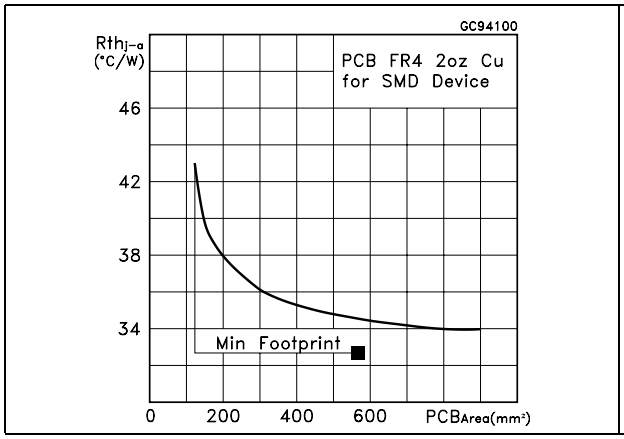


Figure 16. Max power dissipation vs PCB copper area

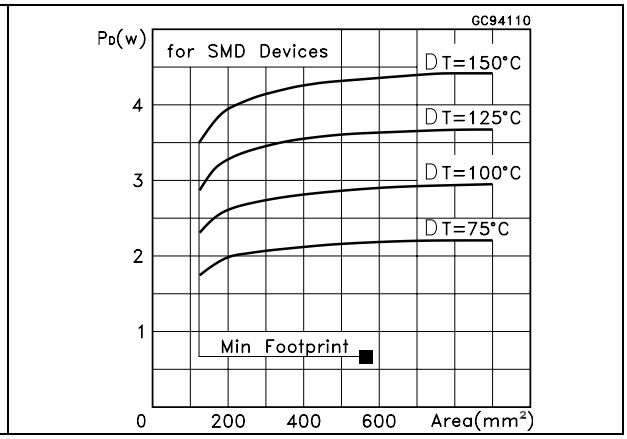
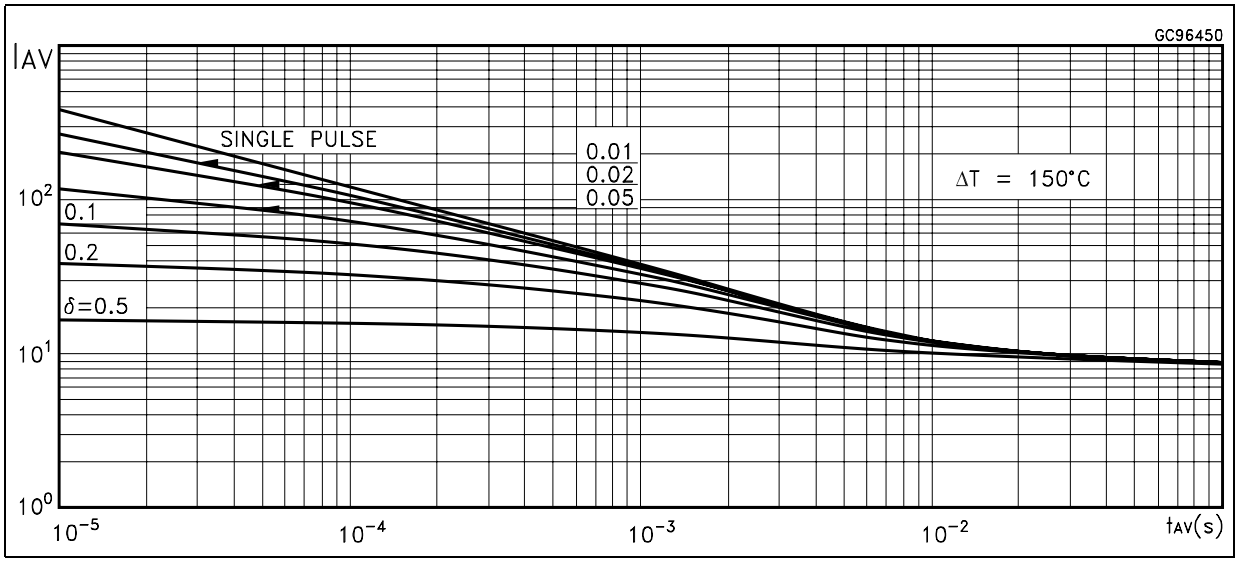


Figure 17. Allowable Iav vs time in avalanche



The previous curve gives the safe operating area for unclamped inductive loads, single pulse or repetitive, under the following conditions:

$P_{D(AVE)} = 0.5 * (1.3 * B_{VDSS} * I_{AV})$

$E_{AS(AR)} = P_{D(AVE)} * t_{AV}$

Where:

I_{AV} is the allowable current in avalanche

$P_{D(AVE)}$ is the average power dissipation in avalanche (single pulse)

t_{AV} is the time in avalanche

To derate above 25 °C, at fixed I_{AV} , the following equation must be applied:

$I_{AV} = 2 * (T_{jmax} - T_{CASE})/ (1.3 * B_{VDSS} * Z_{th})$

Where:

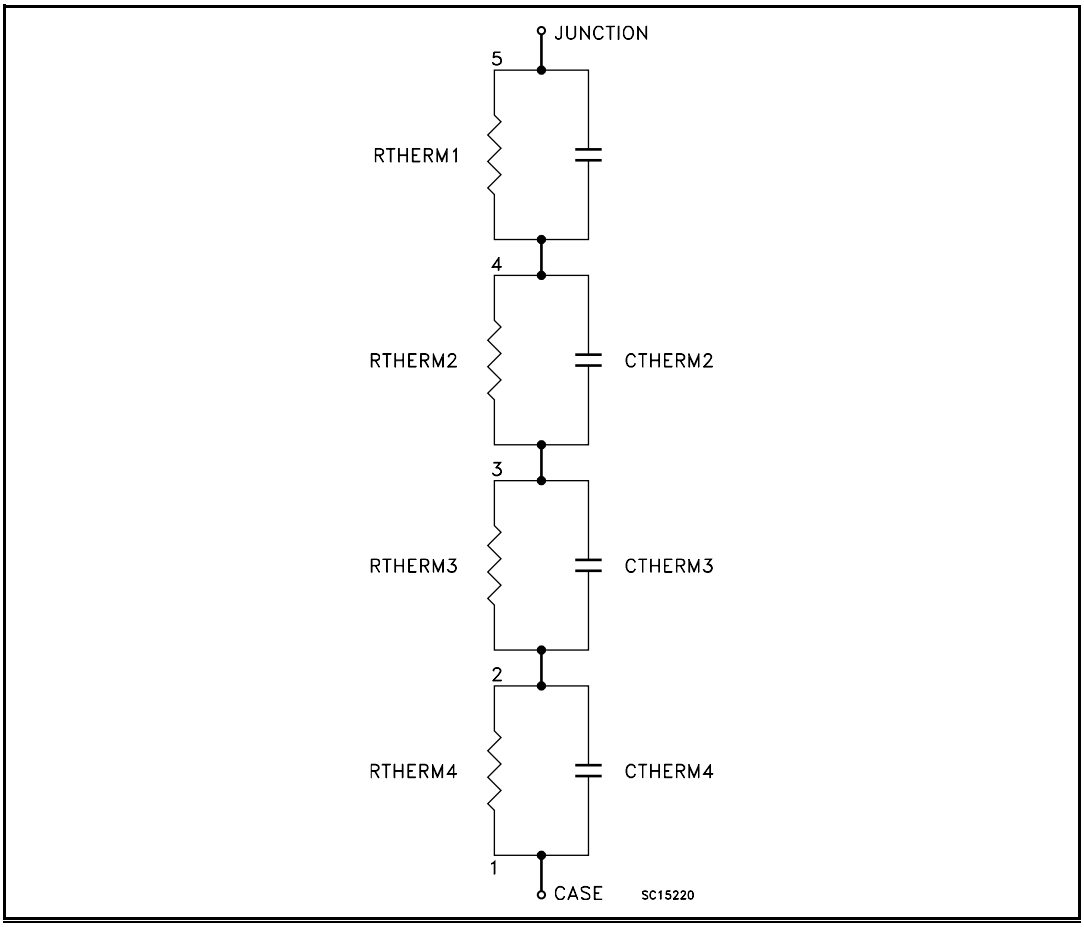
$Z_{th} = K * R_{th}$ is the value coming from normalized thermal response at fixed pulse width equal to T_{AV} .

3 Spice thermal model

Table 6. Parameters

Parameter	Node	Value
CTHERM1	5 - 4	0.011
CTHERM2	4 - 3	0.0012
CTHERM3	3 - 2	0.05
CTHERM4	2 - 1	0.1
RTHERM1	5 - 4	0.09
RTHERM2	4 - 3	0.02
RTHERM3	3 - 2	0.11
RTHERM4	2 - 1	0.17

Figure 18. Scheme



4 Test circuit

Figure 19. Switching times test circuit for resistive load

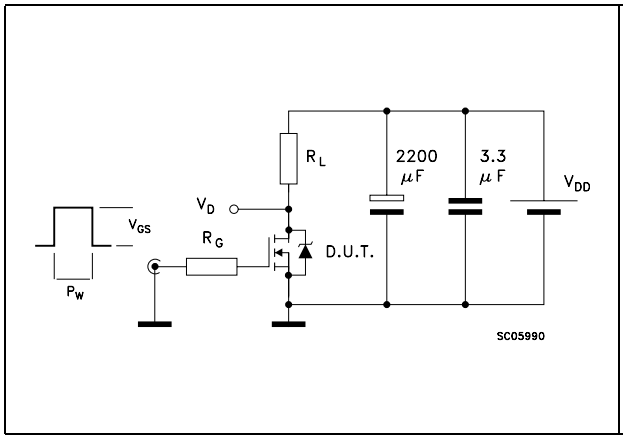


Figure 20. Gate charge test circuit

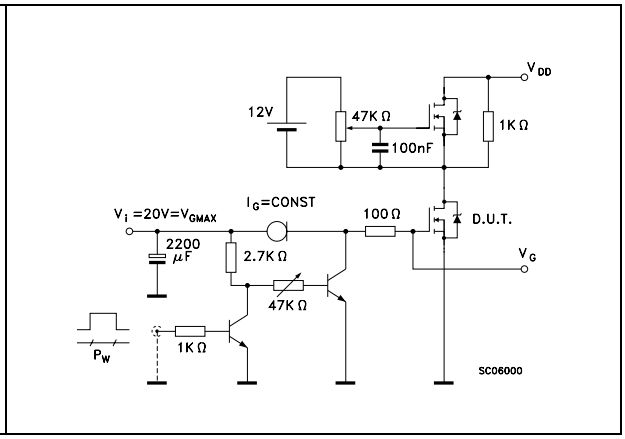


Figure 21. Test circuit for inductive load switching and diode recovery times

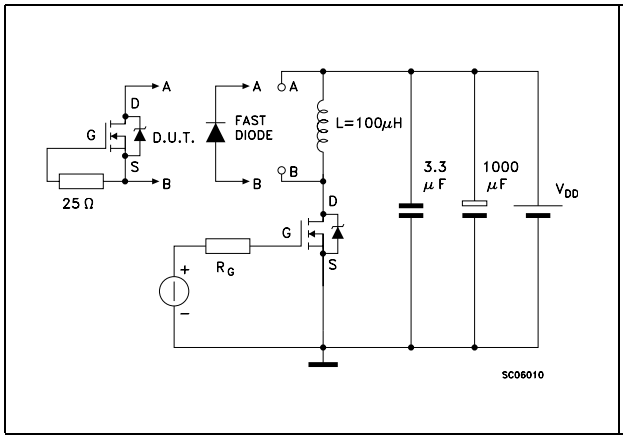


Figure 22. Unclamped Inductive load test circuit

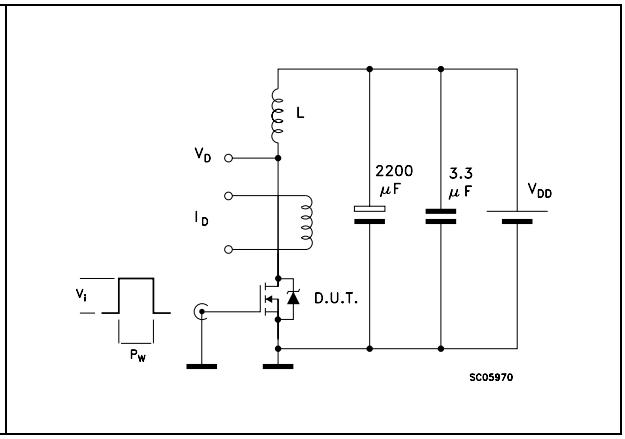


Figure 23. Unclamped inductive waveform

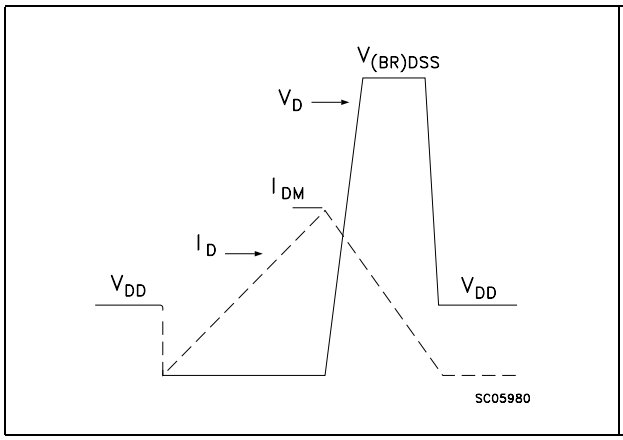


Figure 24. Switching time waveform

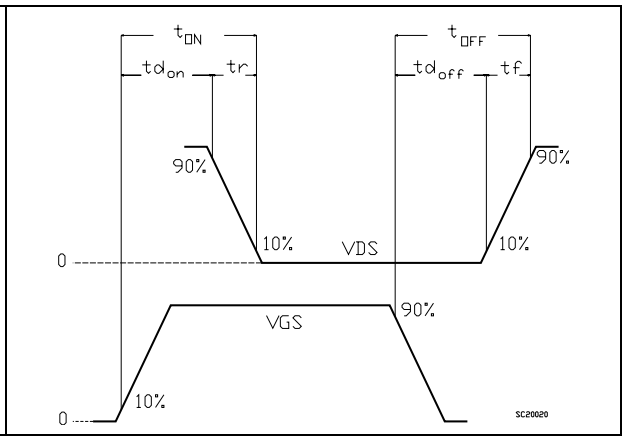
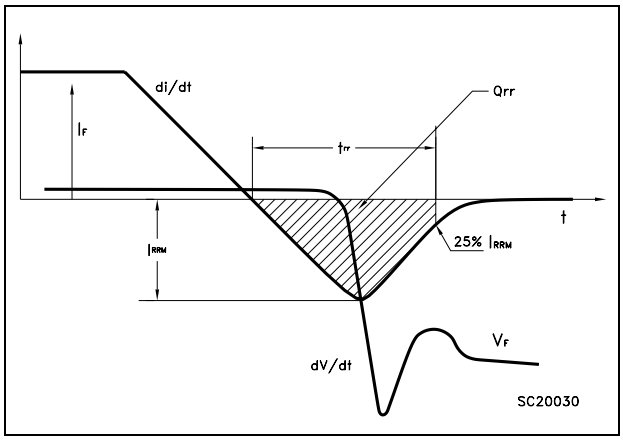


Figure 25. Diode recovery times waveform

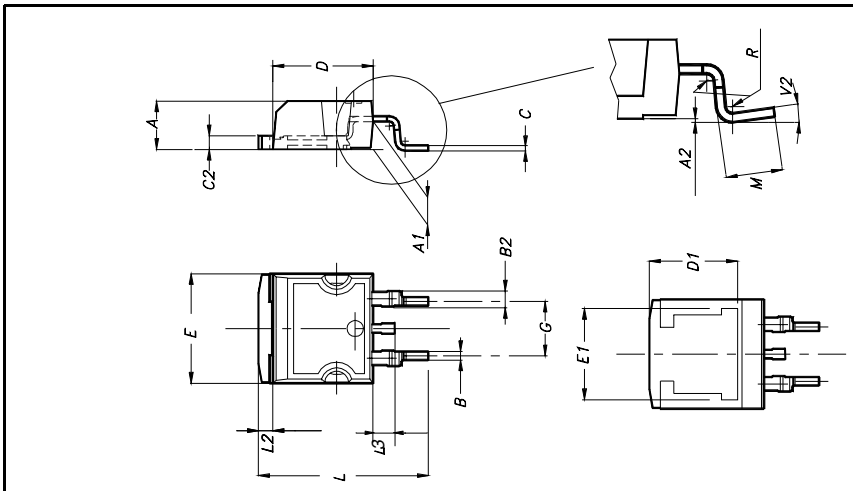


5 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

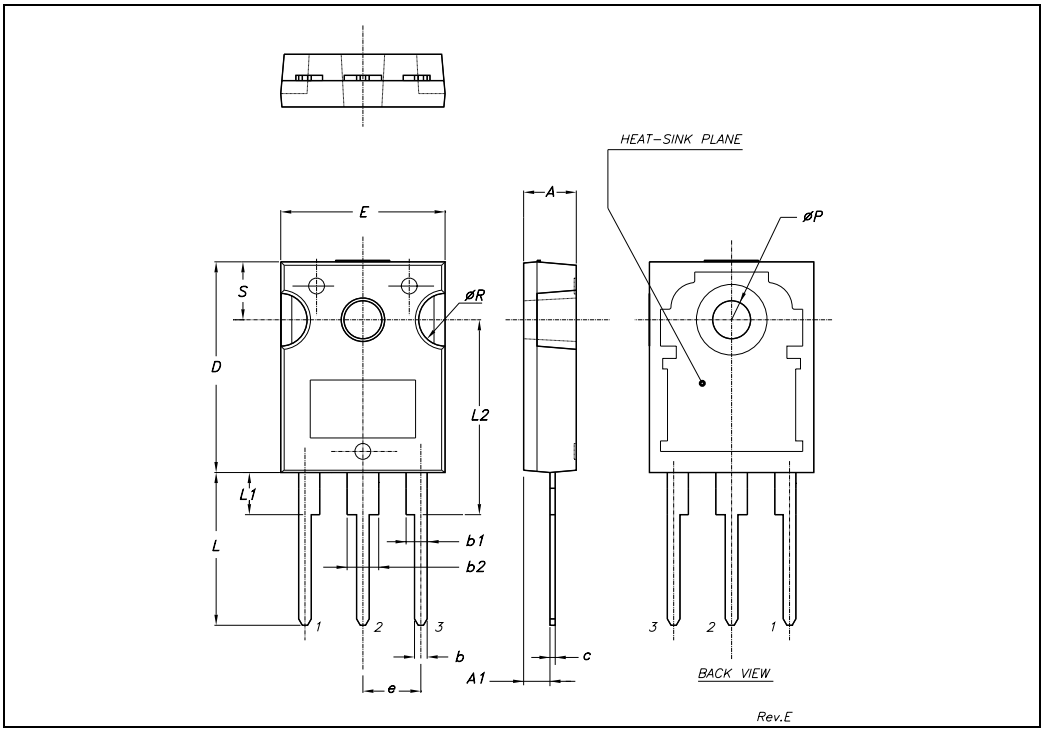
D²PAK MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
D1		8			0.315	
E	10		10.4	0.393		
E1		8.5			0.334	
G	4.88		5.28	0.192		0.208
L	15		15.85	0.590		0.625
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.068
M	2.4		3.2	0.094		0.126
R		0.4			0.015	
V2	0º		4º			



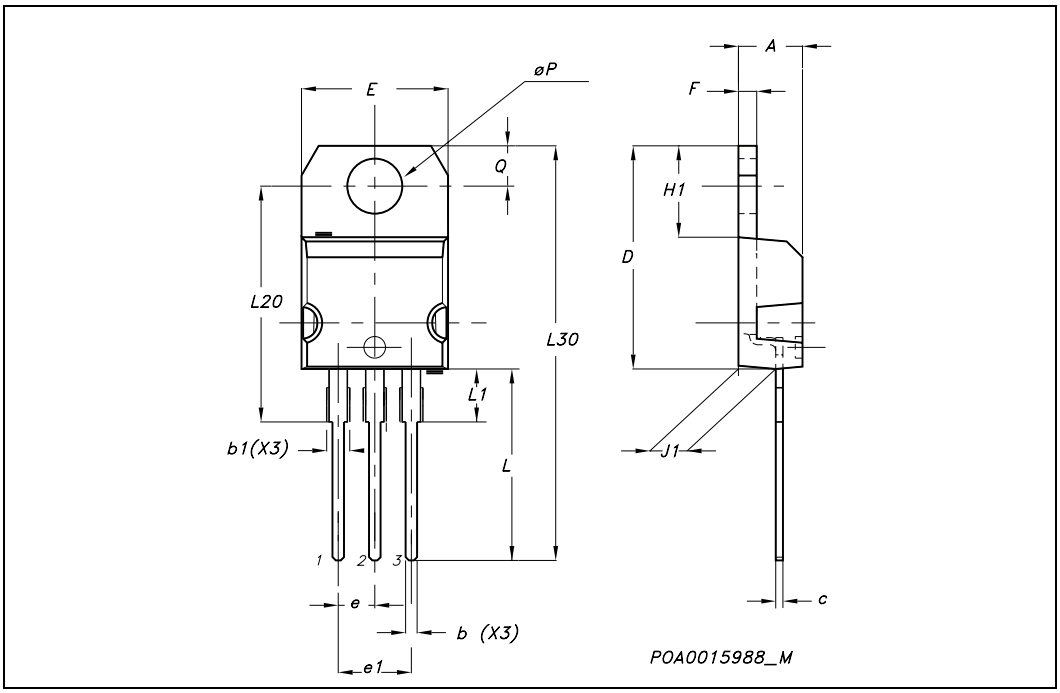
TO-247 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.85		5.15	0.19		0.20
A1	2.20		2.60	0.086		0.102
b	1.0		1.40	0.039		0.055
b1	2.0		2.40	0.079		0.094
b2	3.0		3.40	0.118		0.134
c	0.40		0.80	0.015		0.03
D	19.85		20.15	0.781		0.793
E	15.45		15.75	0.608		0.620
e		5.45			0.214	
L	14.20		14.80	0.560		0.582
L1	3.70		4.30	0.14		0.17
L2		18.50			0.728	
øP	3.55		3.65	0.140		0.143
øR	4.50		5.50	0.177		0.216
S		5.50			0.216	



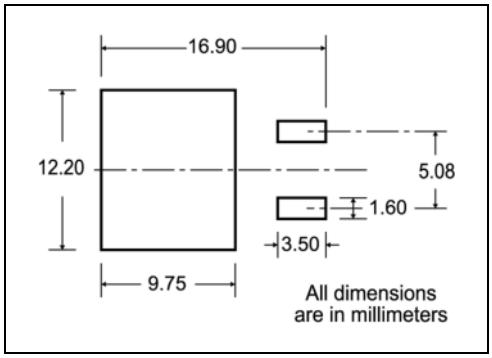
TO-220 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
øP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116

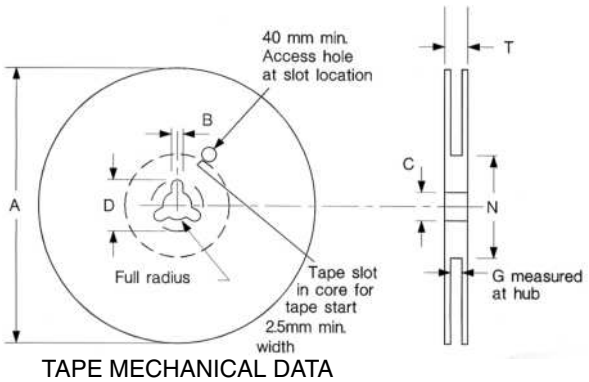


6 Packaging mechanical data

D²PAK FOOTPRINT



TAPE AND REEL SHIPMENT



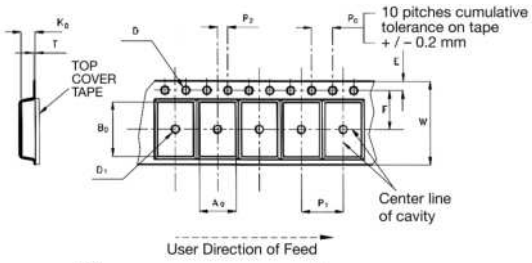
REEL MECHANICAL DATA

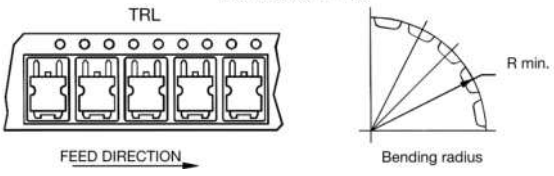
DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0795	
G	24.4	26.4	0.960	1.039
N	100		3.937	
T		30.4		1.197

BASE QTY	BULK QTY
1000	1000

TAPE MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	10.5	10.7	0.413	0.421
B0	15.7	15.9	0.618	0.626
D	1.5	1.6	0.059	0.063
D1	1.59	1.61	0.062	0.063
E	1.65	1.85	0.065	0.073
F	11.4	11.6	0.449	0.456
K0	4.8	5.0	0.189	0.197
P0	3.9	4.1	0.153	0.161
P1	11.9	12.1	0.468	0.476
P2	1.9	2.1	0.075	0.082
R	50		1.574	
T	0.25	0.35	0.0098	0.0137
W	23.7	24.3	0.933	0.956





* on sales type

7 Revision history

Table 7. Revision history

Date	Revision	Changes
21-Jun-2004	2	Preliminary version
26-Jun-2006	3	New template, no content change

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