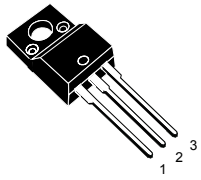
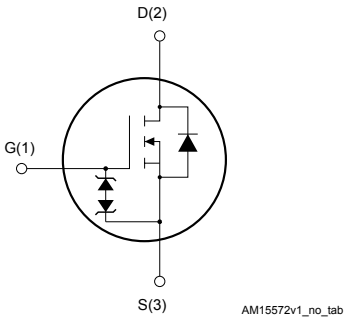
STP17NK40ZFP

Datasheet

N-channel 400 V, 220 mΩ typ., 15 A SuperMESH Power MOSFET in a TO-220FP package



TO-220FP



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STP17NK40ZFP	400 V	250 mΩ	15 A

- Extremely high dv/dt capability
- Improved ESD capability
- 100% avalanche tested
- Gate charge minimized
- Very low intrinsic capacitance
- Zener-protected

Applications

- Switching applications

Description

This high-voltage device is a Zener-protected N-channel Power MOSFET developed using the SuperMESH technology by STMicroelectronics, an optimization of the well-established PowerMESH. In addition to a significant reduction in on-resistance, this device is designed to ensure a high level of dv/dt capability for the most demanding applications.

Product status link
STP17NK40ZFP

Product summary	
Order code	STP17NK40ZFP
Marking	P17NK40ZFP
Package	TO-220FP
Packing	Tube

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	400	V
V_{GS}	Gate-source voltage	±30	V
I_D	Drain current (continuous) at T_C = 25 °C	15(1)	A
	Drain current (continuous) at T_C = 100 °C	9.4(1)	
I_{DM}(2)	Drain current (pulsed)	60(1)	A
P_{TOT}	Total power dissipation at T_C = 25 °C	35	W
ESD	Gate-source human body model (C = 100 pF, R = 1.5 kΩ)	4.5	kV
dv/dt(3)	Peak diode recovery voltage slope	4.5	V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s, T_C = 25 °C)	2.5	kV
T_{stg}	Storage temperature range	-55 to 150	°C
T_J	Operating junction temperature range		

1. *Limited by maximum junction temperature.*
2. *Pulse width is limited by safe operating area.*
3. *I_{SD} ≤ 15 A, di/dt ≤ 200 A/µs, V_{DS} (peak) < $V_{(BR)DSS}$.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	3.6	°C/W
R_{thJA}	Thermal resistance, junction-to-ambient	62.5	°C/W

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width is limited by T_J max.)	15	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	450	mJ

2 Electrical characteristics

T_C = 25 °C unless otherwise specified.

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0 V	400	-	-	V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 400 V	-	-	1	µA
		V_{GS} = 0 V, V_{DS} = 400 V, T_C = 125 °C(1)	-	-	50	
I_{GSS}	Gate-body leakage current	V_{GS} = ±20 V, V_{DS} = 0 V	-	-	±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 100 µA	3.00	3.75	4.50	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 7.5 A	-	220	250	mΩ

1. *Specified by design, not tested in production.*

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0 V	-	1900	-	pF
C_{oss}	Output capacitance		-	271	-	pF
C_{rss}	Reverse transfer capacitance		-	63	-	pF
$C_{oss\ eq.}$(1)	Equivalent output capacitance	V_{GS} = 0 V, V_{DS} = 0 to 400 V	-	175	-	pF
Q_g	Total gate charge	V_{DD} = 320 V, I_D = 15 A, V_{GS} = 0 to 10 V (see the Figure 14. Test circuit for gate charge behavior)	-	65	-	nC
Q_{gs}	Gate-source charge		-	13	-	nC
Q_{gd}	Gate-drain charge		-	35	-	nC

1. *$C_{oss\ eq.}$ is defined as the constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.*

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 200 V, I_D = 7.5 A, R_G = 4.7 Ω, V_{GS} = 10 V (see the Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	25	-	ns
t_r	Rise time		-	23	-	ns
$t_{d(off)}$	Turn-off delay time		-	55	-	ns
t_f	Fall time		-	13	-	ns
$t_{r(Voff)}$	Off-voltage rise time	V_{DD} = 320 V, I_D = 15 A, R_G = 4.7 Ω, V_{GS} = 10 V (see the Figure 15. Test circuit for inductive load switching and diode recovery times)	-	12	-	ns
t_f	Fall time		-	13	-	ns
t_c	Cross-over time		-	25	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-	-	15	A
I_{SDM}(1)	Source-drain current (pulsed)		-	-	60	A
V_{SD}(2)	Forward on voltage	I_{SD} = 15 A, V_{GS} = 0 V	-	-	1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 15 A, di/dt = 100 A/µs, V_{DD} = 100 V, T_J = 150 °C. (see the Figure 15. Test circuit for inductive load switching and diode recovery times)	-	332	-	ns
Q_{rr}	Reverse recovery charge		-	2.65	-	µC
I_{RRM}	Reverse recovery current		-	16	-	A

1. *Pulse width is limited by safe operating area.*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

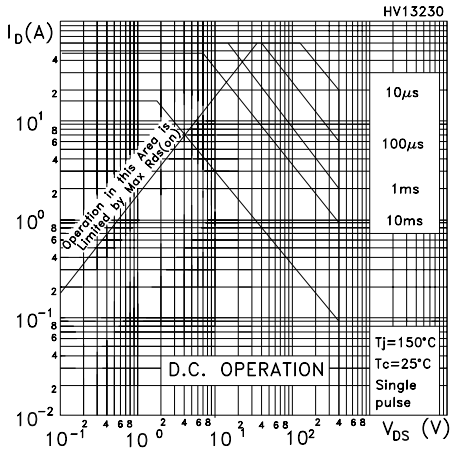


Figure 2. Normalized transient thermal impedance

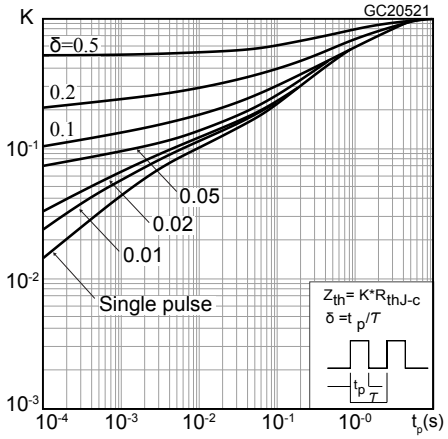


Figure 3. Typical output characteristics

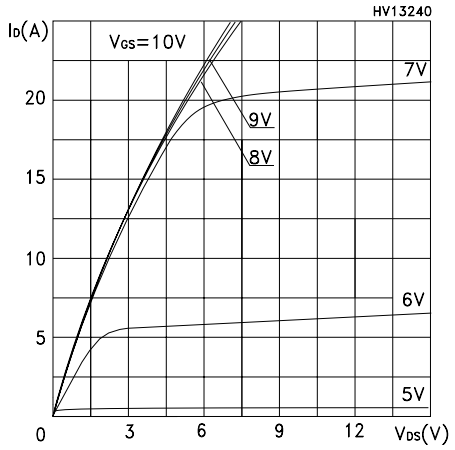


Figure 4. Typical transfer characteristics

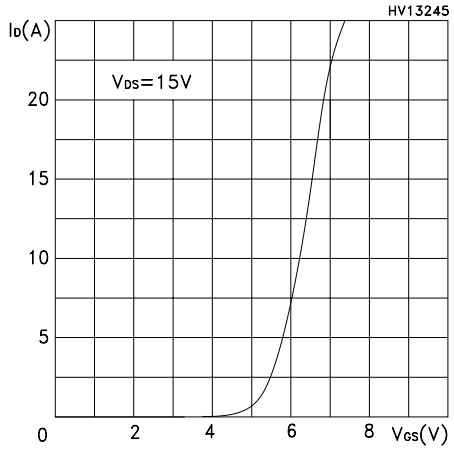


Figure 5. Typical drain-source on-resistance

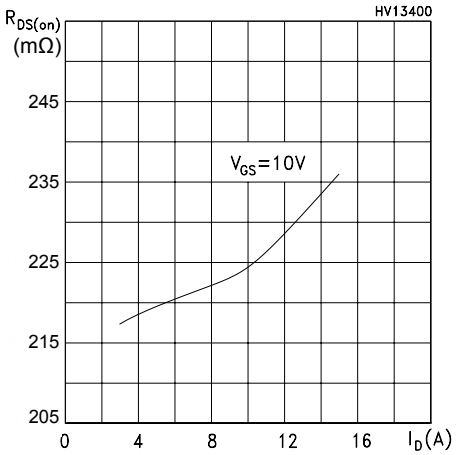


Figure 6. Typical gate charge characteristics

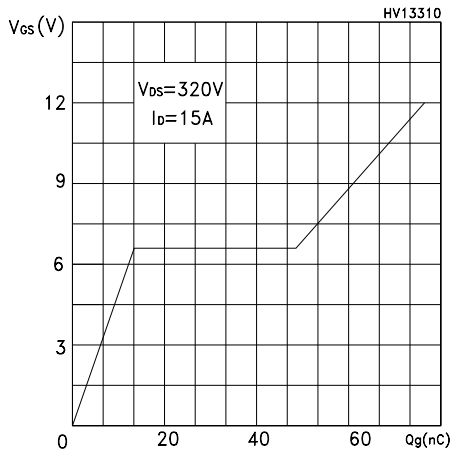


Figure 7. Typical capacitance characteristics

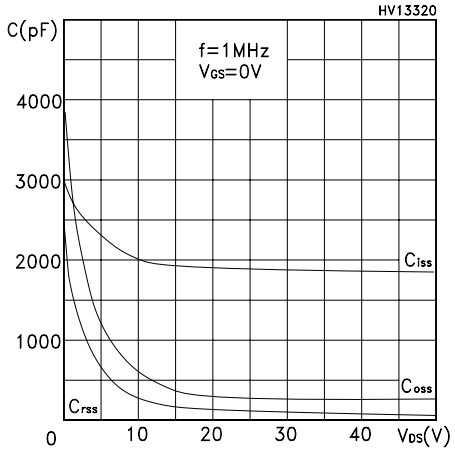


Figure 8. Normalized gate threshold vs temperature

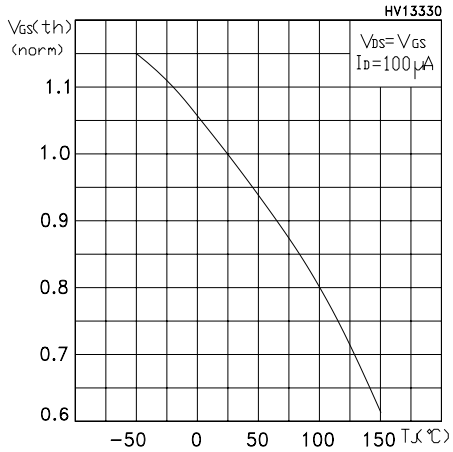


Figure 9. Normalized on-resistance vs temperature

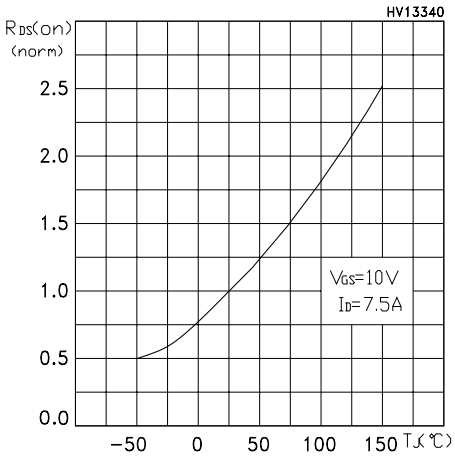


Figure 10. Typical reverse diode forward characteristics

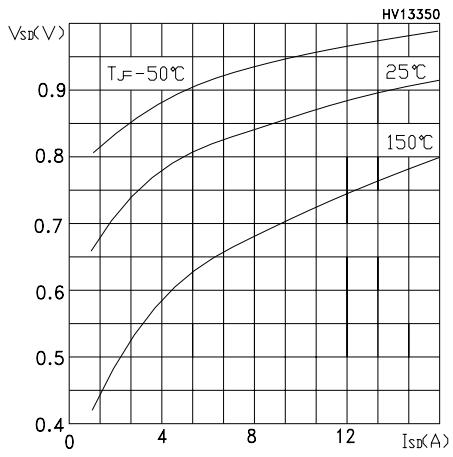


Figure 11. Normalized breakdown voltage vs temperature

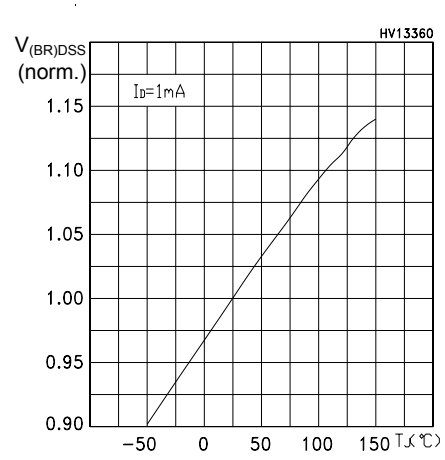
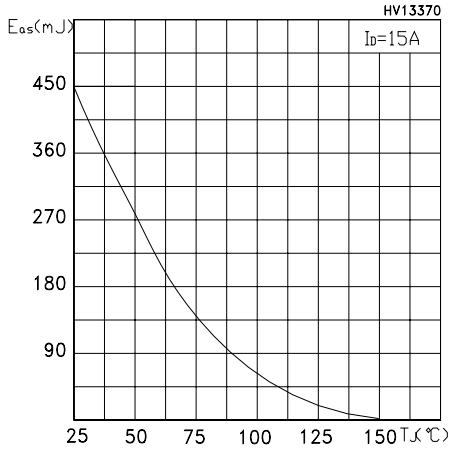
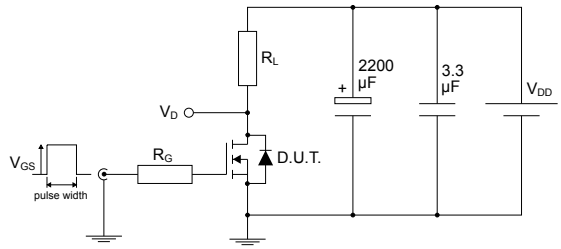


Figure 12. Maximum avalanche energy vs temperature



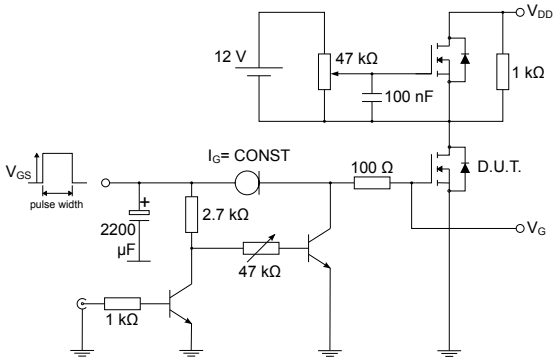
3 Test circuits

Figure 13. Test circuit for resistive load switching times



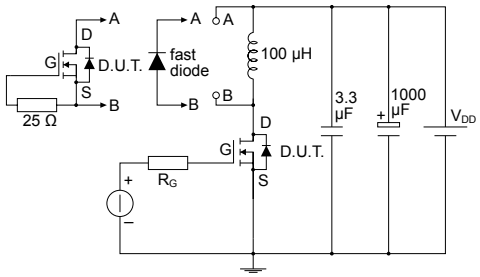
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Figure 14. Test circuit for gate charge behavior



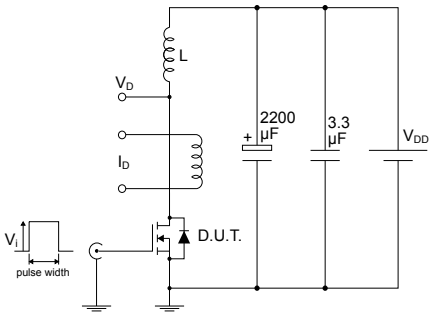
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Figure 15. Test circuit for inductive load switching and diode recovery times



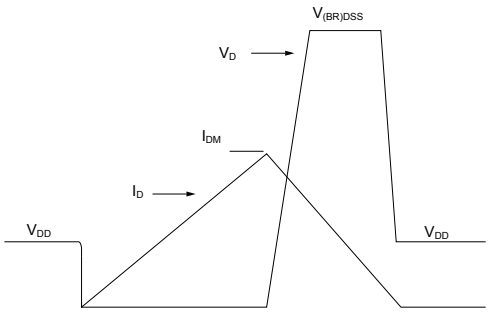
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Figure 16. Unclamped inductive load test circuit



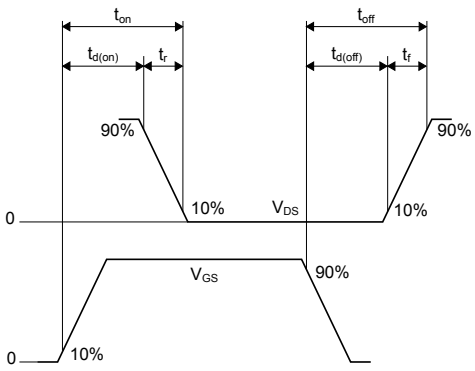
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Figure 17. Unclamped inductive waveform



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Figure 18. Switching time waveform



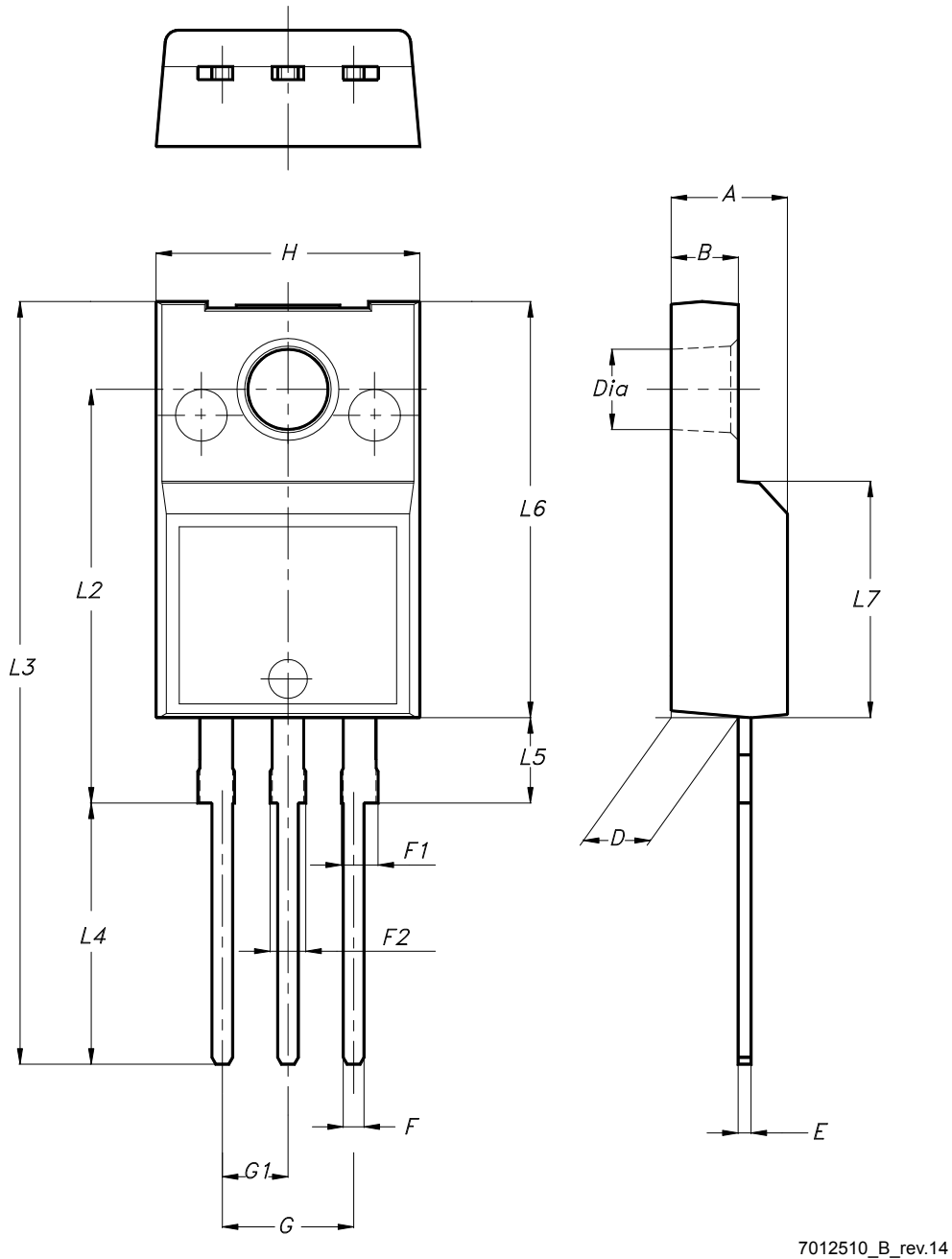
AM01473v1

4 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TO-220FP type B package information

Figure 19. TO-220FP type B package outline



7012510_B_rev.14

Table 8. **TO-220FP type B package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
B	2.50		2.70
D	2.50		2.75
E	0.45		0.70
F	0.75		1.00
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.20
G1	2.40		2.70
H	10.00		10.40
L2		16.00	
L3	28.60		30.60
L4	9.80		10.60
L5	2.90		3.60
L6	15.90		16.40
L7	9.00		9.30
Dia	3.00		3.20

Revision history

Table 9. **Document revision history**

Date	Revision	Changes
14-Oct-2002	1	First release.
02-Feb-2026	2	The part number STP17NK40Z has been removed and the document has been updated accordingly. Updated Section 4: Package information. Minor text changes.

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