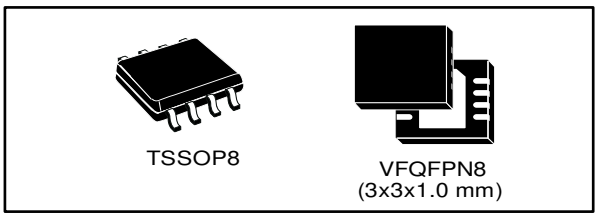
L6926

High efficiency monolithic synchronous step-down regulator

Datasheet - production data



Features

- 2 V to 5.5 V battery input range
- High efficiency: up to 95%
- Internal synchronous switch
- No external Schottky diode required
- Extremely low quiescent current
- 1 µA max. shutdown supply current
- 800 mA max. output current
- Adjustable output voltage from 0.6 V
- Low-dropout operation: up to 100% duty cycle
- Selectable low noise/low consumption mode at light load
- Power Good signal
- ± 1% output voltage accuracy
- Current mode control
- 600 kHz switching frequency
- Externally synchronized from 500 kHz to 1.4 MHz
- OVP
- Short-circuit protection

Applications

- Battery-powered equipment
- Portable instruments
- Cellular phones
- PDAs and handheld terminals
- DSC
- GPS

Description

The device is a DC-DC monolithic regulator specifically designed to provide high efficiency. The L6926 supply voltage can be as low as 2 V to be used in single Li-Ion cell supplied applications. Output voltage can be selected by an external divider down to 0.6 V. Duty cycle can saturate 100% allowing low-dropout operation. The device is based on a 600 kHz fixed frequency, current mode architecture. Low consumption mode operation can be selected at light load conditions, allowing switching losses to be reduced. The L6926 is externally synchronized by a clock, which makes it useful in noise sensitive applications. Other features like Power Good, overvoltage protection, short-circuit protection and thermal shutdown (150 °C) are also present.

Table 1: Device summary

Order code	Package	Packing
L6926	TSSOP8	Tube
L6926013TR	TSSOP8	Tape and reel
L6926Q1	VFQFPN8	Tube
L6926Q1TR	VFQFPN8	Tape and reel

This is information on a product in full production. www.st.com

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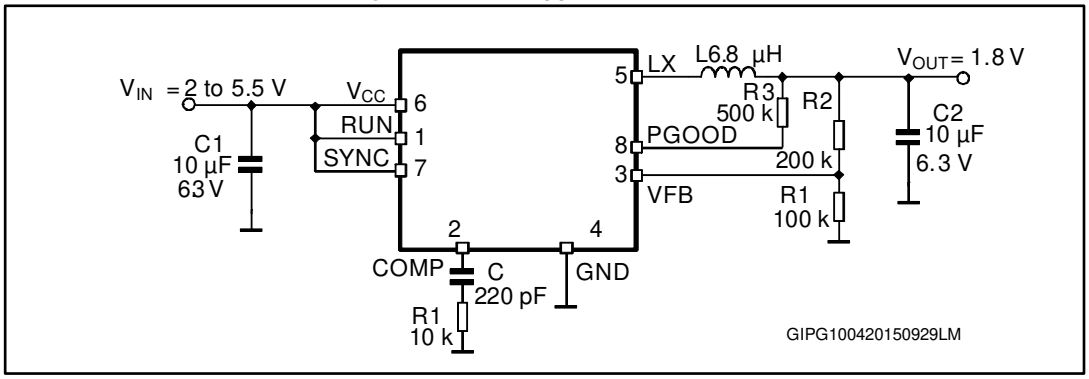
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1 Application circuit

Figure 1: L6926 application circuit



2 Pin configuration

Figure 2: Pin connections (top view)

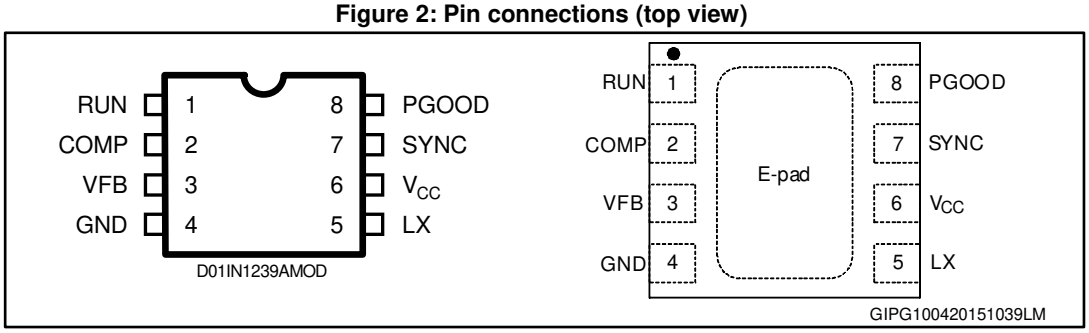


Table 2: Pin description

Pin	Name	Description
1	RUN	Shutdown input. When connected to a low level (lower than 0.4 V) the device stops working. When high (higher than 1.3 V) the device is enabled
2	COMP	Error amplifier output. A compensation network has to be connected to this pin. The loop stability usually is well-guaranteed by a 220 pF capacitor
3	VFB	Error amplifier inverting input. The output voltage can be adjusted from 0.6 V up to the input voltage by connecting this pin to an external resistor divider
4	GND	Ground
5	LX	Switch output node. This pin is internally connected to the drain of the internal switches
6	V_{CC}	Input voltage. The start-up input voltage is 2.2 V (typ.) while the operating input voltage range is from 2 V to 5.5 V. An internal UVLO circuit gives a 100 mV (typ.) hysteresis
7	SYNC	Operating mode selector input. When high (higher than 1.3 V) the low consumption mode is selected. When low (lower than 0.5 V) the low noise mode is selected. If connected with an appropriate external synchronization signal (from 500 kHz up to 1.4 MHz) the internal synchronization circuit is active and the device works at the same switching frequency
8	PGOOD	Power Good comparator output. It is an open drain output. A pull-up resistor should be connected between PGOOD and V_{OUT} (or V_{CC} depending on the requirements). The pin is forced low when the output voltage is lower than 90% of the regulated output voltage and goes high when the output voltage is greater than 90% of the regulated output voltage. If it is not used the pin can be left floating
-	E-pad	To be connected to GND plane for optimal thermal performance

3 Maximum ratings

Table 3: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_6	Input voltage	- 0.3 to + 6.0	V
V_5	Output switching voltage	- 1 to V_{CC}	V
V_1	Shutdown	-0.3 to V_{CC}	V
V_3	Feedback voltage	-0.3 to V_{CC}	V
V_2	Error amplifier output voltage	-0.3 to V_{CC}	V
V_8	PGOOD	-0.3 to V_{CC}	V
V_7	Synchronization mode selector	-0.3 to V_{CC}	V
P_{TOT}	Power dissipation at T_A = 70 °C	0.45	W
T_J	Junction operating temperature range	-40 to 150	°C
T_{STG}	Storage temperature range	-65 to 150	
LX pin	Maximum withstanding voltage range test condition: CDF-AEC-Q100-002 “human body model” acceptance criteria: “normal performance"	±1000	V
Other pins		±2000	

Table 4: Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction-ambient for TSSOP8	180	°C/W
	Thermal resistance junction-ambient for VFQFPN8	56	

4 Electrical characteristics

V_{IN} = 3.6 V, T_J = 25 °C unless otherwise specified.

Table 5: Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating input voltage	After turn-on(1)	2		5.5	V
V_{CC} ON	Turn-on threshold			2.2		V
V_{CC} OFF	Turn-off threshold				2	V
V_{CC_hys}	Hysteresis			100		mV
R_p	High-side Ron	V_{CC} = 3.6 V, I_{LX} = 100 mA		240	300	mΩ
					400	
R_n	Low-side Ron	V_{CC} = 3.6 V, I_{LX} = 100 mA		215	300	
					400	
I_{LIM}	Peak current limit	V_{CC} = 3.6 V	1	1.2	1.5	A
			0.85		1.65	
	Valley current limit		1	1.4	1.7	
			0.9		1.85	
V_{OUT}	Output voltage range		V_{FB}		V_{CC}	V
f_{OSC}	Oscillator frequency		450	600	700	kHz
			400	600	800	
f_{sync}	Sync mode clock		500		1400	
DC characteristics						
I_q	Quiescent current (low noise mode)	V_{sync} = 0 V, no-load, V_{FB} > 0.6 V		200	300	µA
					300	
	Quiescent current (low consumption mode)	V_{sync} = V_{CC}, no-load, V_{FB} > 0.6 V		25	50	
I_{sh}	Shutdown current	RUN to GND, V_{CC} = 5.5 V		0.2		
I_{LX}	LX leakage current	RUN to GND, V_{LX} = 5.5 V, V_{CC} = 5.5 V		1		
		RUN to GND, V_{LX} = 0 V, V_{CC} = 5.5 V		1		
Error amplifier characteristics						
V_{FB}	Voltage feedback		0.593	0.600	0.607	V
			0.590	0.600	0.610	V
I_{FB}	Feedback input current	V_{FB}		25		nA
Run						

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{RUN_H}	Run threshold high				1.3	V
V_{RUN_L}	Run threshold low		0.4			V
I_{RUN}	RUN input current			25		nA
SYNC/MODE function						
V_{sync_H}	Sync mode threshold high				1.3	V
V_{sync_L}	Sync mode threshold low		0.5			V
Power Good section						
V_{PGOOD}	Power Good threshold	$V_{OUT} = V_{FB}$		90		$\%V_{OUT}$
ΔV_{PGOOG}	Power Good hysteresis	$V_{OUT} = V_{FB}$		4		
$V_{PGOOD(low)}$	Power Good low voltage	RUN to GND			0.4	V
$I_{LK-PGOOD}$	Power Good leakage current	V_{PGOOD} = 3.6 V		50		nA
Protections						
HOVP	Hard overvoltage threshold	$V_{OUT} = V_{FB}$		10		$\%V_{OUT}$

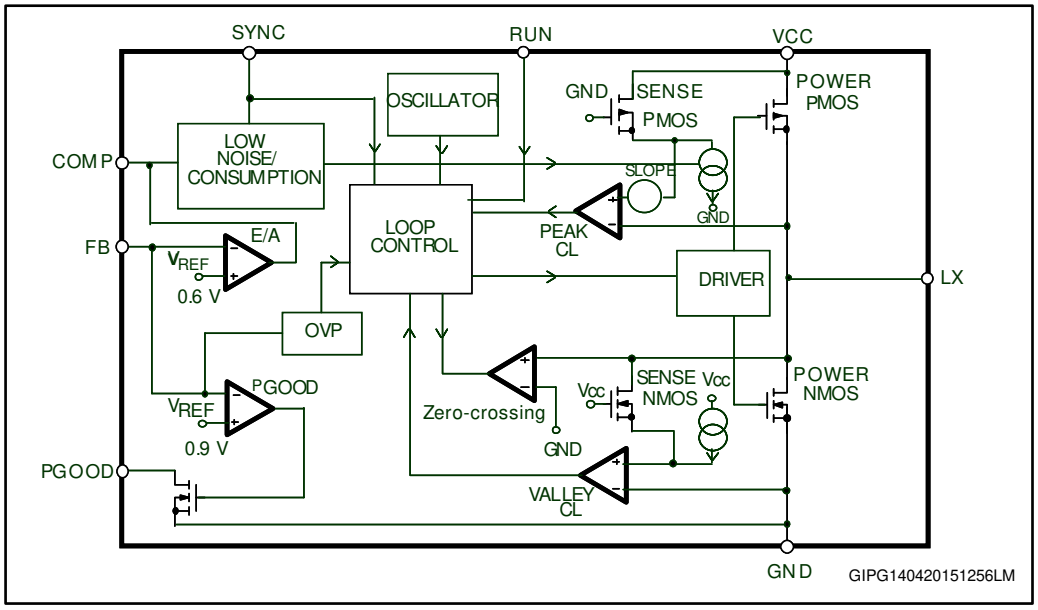
Notes:

(1)Specification referred to T_J from -40 °C to +125 °C. Specification over the -40 to +125 °C T_J temperature range is assured by design, characterization and statistical correlation.

5 Detailed description

The main loop uses slope compensated PWM current mode architecture. For each cycle, the high-side MOSFET is turned on, triggered by the oscillator, so that the current, flowing through it (the same as the inductor current), increases. When this current reaches the threshold (set by the output of the error amplifier E/A), the peak current limit comparator PEAK_CL turns off the high-side MOSFET and turns on the low-side one until the next clock cycle begins or the current, flowing through it, goes down to zero (zero-crossing comparator). The peak inductor current required to trigger PEAK_CL depends on the slope compensation signal and on the output of the error amplifier. In particular, the error amplifier output depends on the VFB pin voltage. When the output current increases, the output capacitor is discharged and the VFB pin decreases. This produces the error amplifier output rise, so to allow a higher value for the peak inductor current. For the same reason, when the output current decreases, due to a load transient, the error amplifier output goes low, so to reduce the peak inductor current to meet the new load requirements. The slope compensation signal allows the loop stability in high duty cycle conditions.

Figure 3: Device block diagram



5.1 Modes of operation

Depending on the SYNC pin value, the device can operate in low consumption or low noise mode. If the SYNC pin is high (higher than 1.3 V) the low consumption mode is selected while the low noise mode is selected if the SYNC pin is low (lower than 0.5 V).

5.1.1 Low consumption mode

In this mode of operation, at light load, the device operates discontinuously based on the COMP pin voltage, in order to keep the efficiency very high in these conditions. While the device doesn't switch, the load discharges the output capacitor and the output voltage goes down. When the feedback voltage goes lower than the internal reference, the COMP pin voltage increases and when an internal threshold is reached, the device starts switching and the output capacitor is recharged. In these conditions, the peak current limit is set approximately in the range of 200 mA to 400 mA, depending on the slope compensation.

The feedback pin increases and, when it reaches a value slightly higher than the reference voltage, the output of the error amplifier goes down until a clamp is active. At this point, the device stops switching. In this phase, the internal circuitries are off, so to reduce the device consumption to a typical value of 25 µA.

5.1.2 Low noise mode

If the low frequencies of the low consumption mode are undesidered, the low noise mode can be selected. In low noise mode, the efficiency is a little bit lower compared with the low consumption mode in very light load conditions but for medium and high load currents the efficiency values are very similar. Basically, the device switches with its internal free running frequency of 600 kHz. Obviously, in very light load conditions, the device could skip some cycles in order to keep the output voltage in regulation.

5.1.3 Synchronization

The device can also be synchronized by an external signal from 500 kHz up to 1.4 MHz. In this case the low noise mode is automatically selected. The device skips some cycles in very light load conditions. The internal synchronization circuit is inhibited in short-circuit and overvoltage conditions in order to keep the protection effective.

5.2 Short-circuit protection

During the device operation, the inductor current increases during the high-side turn-on phase and decreases during the high-side turn-off phase based on the following equations:

Equation 1:

$$\Delta I_{ON} = \frac{(V_{IN} - V_{OUT})}{L} \cdot T_{ON}$$

Equation 2:

$$\Delta I_{OFF} = \frac{(V_{OUT})}{L} \cdot T_{OFF}$$

In strong overcurrent or short-circuit conditions, the V_{OUT} can be very close to zero. In this case ΔI_{ON} increases and ΔI_{OFF} decreases. When the inductor peak current reaches the current limit, the high-side MOSFET turns off and so the T_{ON} is reduced to the minimum value (250 ns typ.) in order to reduce as much as possible ΔI_{ON}. Anyway, if V_{OUT} is low enough, the inductor peak current increases furtherly because during the T_{OFF} the current decays very slowly. Due to this reason a second protection, fixing the maximum inductor valley current, has been introduced. This protection doesn't allow the high-side MOSFET to turn on if the current, flowing through the inductor, is higher than a specified threshold (valley current limit). Basically the T_{OFF} increases as much as required to lead the inductor current down to this threshold. So, the maximum peak current in worst case conditions is:

Equation 3:

$$I_{PEAK} = I_{VALLEY} + \frac{V_{IN}}{L} \cdot T_{ON_MIN}$$

where I_{PEAK} is the valley current limit (1.4 A typ.) and T_{ON_MIN} is the minimum T_{ON} of the high-side MOSFET.

5.3 Slope compensation

In current mode architecture, when the duty cycle of the application is higher than approximately 50%, a pulse-by-pulse instability (so-called subharmonic oscillation) can occur. In these conditions, to allow loop stability, a slope compensation is present by reducing the current flowing through the inductor to trigger the COMP comparator (with a fixed value for the COMP pin voltage). With a given duty cycle higher than 50%, the stability problem is particularly present with a higher input voltage (due to the increased current ripple across the inductor), so the slope compensation effect increases as the input voltage increases. From an application point of view, the final effect is that the peak current limit depends both on the duty cycle (if higher than approximately 40%) and on the input voltage.

5.4 Loop stability

Since the device is developped by a current mode architecture, the loop stability is not an issue. For most of applications, a 220 pF connected between the COMP pin and ground can guarantee the stability. Very low ESR capacitors are used for the output filter, such as multilayer ceramic capacitors, the zero introduced by the capacitor itself can shift to very high frequency and the transient loop response could be affected. A series resistor added to the 220 pF capacitor can solve this problem. The right value for the resistor (in the range of 50 k) can be given by checking the load transient response of the device. Basically, the output voltage has to be checked after the load steps required by the application. In case of stability problems, the output voltage could oscillate before than the regulated value is reached after a load step.

6 Additional features and description

6.1 Dropout operation

The Li-Ion battery voltage ranges from approximately 3 V and 4.1 V to 4.2 V (depending on the anode material). If the regulated output voltage is from 2.5 V and 3.3 V, close to the end of the battery life, the battery voltage goes down to the regulated value. In this case the device stops switching, working at 100% of duty cycle, so to minimize the dropout voltage and the device losses.

6.2 PGOOD

A Power Good output signal is available. The VFB pin is internally connected to a comparator with a threshold set at 90% of the reference voltage (0.6 V). Since the output voltage is connected to the VFB pin by a resistor divider, when the output voltage goes lower than the regulated value, the VFB pin voltage goes lower than 90% of the internal reference value. The internal comparator is triggered and the PGOOD pin is pulled down. The pin is an open drain output and so, a pull-up resistor should be connected to it. If the feature is not required, the pin can be left floating.

6.3 Adjustable output voltage

The output voltage can be adjusted by an external resistor divider from a minimum value of 0.6 V up to the input voltage. The output voltage value is given by the below equation:

Equation 4:

$$V_{OUT} = 0.6 \cdot \left(1 + \frac{R_2}{R_1}\right)$$

6.4 OVP (overvoltage protection)

The device has an internal overvoltage protection circuit to protect the load. If the voltage on the feedback pin goes higher than an internal threshold set 10% (typ.) higher than the reference voltage, the low-side power MOSFET turns on until the feedback voltage goes lower than the reference one. During the overvoltage circuit intervention, the zero-crossing comparator is disabled so that the device is also able to sink current.

6.5 Thermal shutdown

The device has also a thermal shutdown protection active when the junction temperature reaches 150 °C. In this case both the high-side MOSFET and the low-side turn off. Once the junction temperature goes back lower than 95 °C, the device restarts the normal operation.

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

7.1 TSSOP8 package information

Figure 4: TSSOP8 package outline

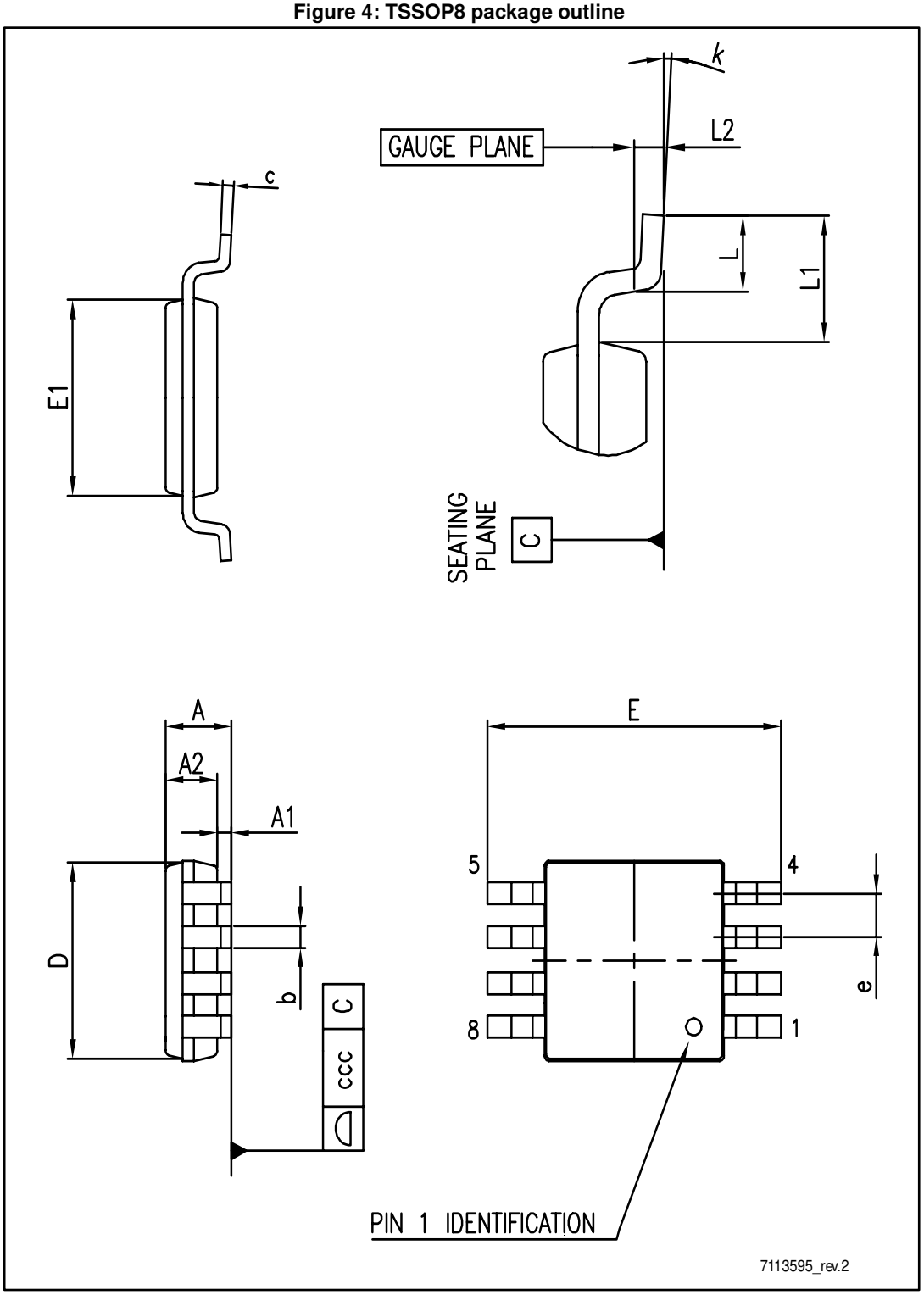


Table 6: TSSOP8 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			1.10
A1			0.15
A2	0.75	0.85	0.95
b	0.22		0.40
c	0.08		0.23
D	2.80	3.00	3.20
E	4.65	4.90	5.15
E1	2.80	3.00	3.10
e		0.65	
L	0.40	0.60	0.80
L1		0.95	
L2		0.25	
k	0		8
ccc			0.10

Dimensions D and E1 don't include mold flash or protrusions. Mold flash or protrusions do not exceed 0.15 mm per side.

7.2 VFQFPN8 package information

Figure 5: VFQFPN8 package outline

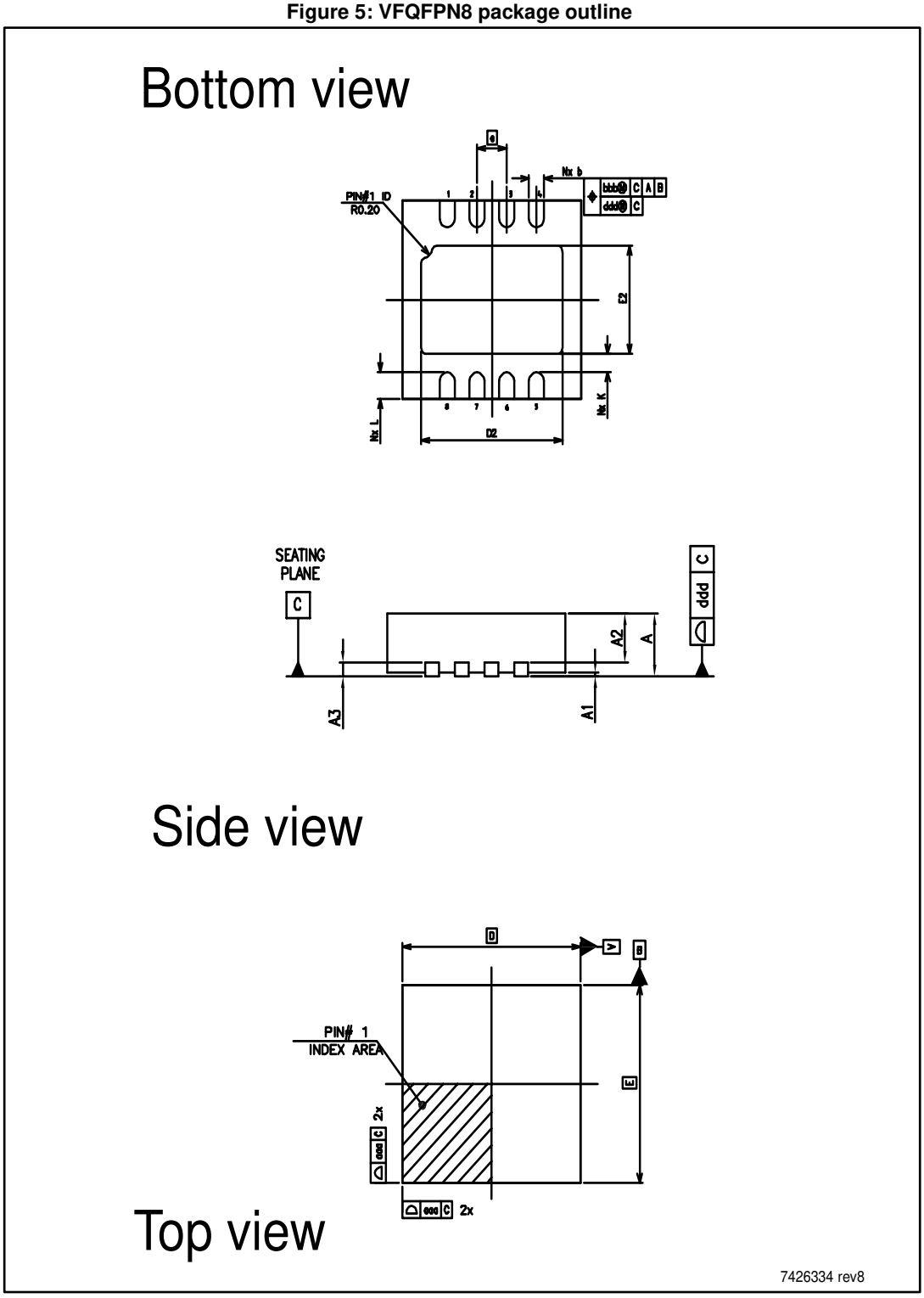


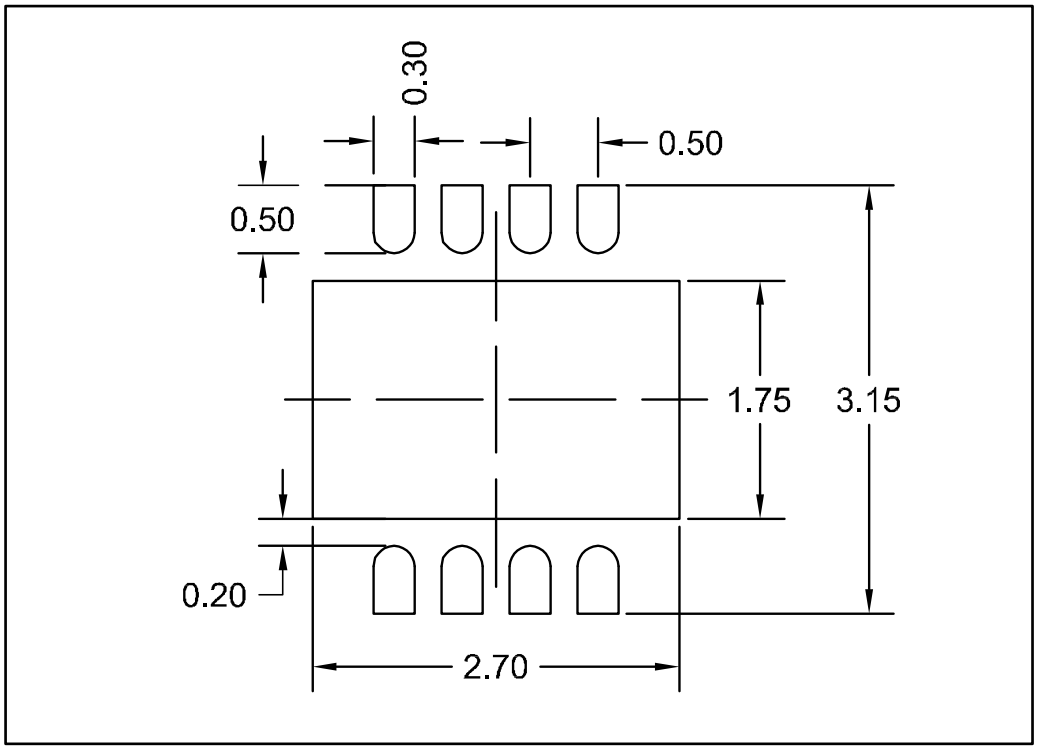
Table 7: VFQFPN8 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1		0.02	
A2	0.55	0.65	0.80
A3		0.20	
b	0.18	0.25	0.30
D	2.85	3.00	3.15
D2 (P1C7)	2.20		2.70
D2 (9957/996H)	2.234	2.384	2.484
E	2.85	3.00	3.15
E2(P1C7)	1.40		1.75
E2 (9957/996H)	1.496	1.646	1.746
e		0.50	
K	0.20		
L	0.30	0.40	0.50
aaa	0.05		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		
N	8		
ND	4		



VFQFPN8 is a standard for thermally enhanced plastic, very thin fine pitch quad flat package, no leads.

Figure 6: VFQFPN8 recommended footprint



8 Revision history

Table 8: Document revision history

Date	Revision	Changes
07-Jan-2004	1	Initial release.
15-Jan-2004	2	Issues in EDOCS.
04-Sep-2004	3	Changed the template and added the new package VFSON8.
27-Nov-2004	4	Updated the order code table.
24-Sep-2005	5	Updated the electrical characteristic table.
20-Nov-2005	6	Added VFQFPN8 package.
27-Oct-2006	7	Added R_{thJA} for VFQFPN8 in Table 3.
16-Sep-2008	8	VFSON8 package no longer available.
11-Apr-2011	9	Updated TSSOP8 package mechanical data.
20-Dec-2011	10	Updated figure 1 and added figure 2
21-Apr-2015	11	Updated features. Deleted note 2 in table 5. Updated package information section.

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