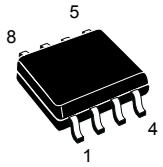
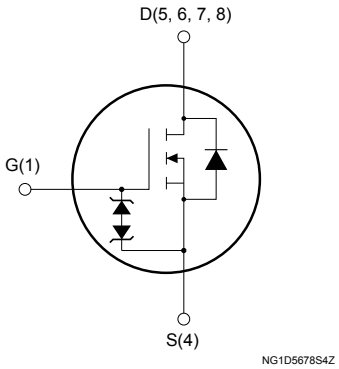
STS1NK60Z

Datasheet

N-channel 600 V, 11 Ω typ., 0.25 A SuperMESH Power MOSFET in a SO-8 package



SO-8



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STS1NK60Z	600 V	15 Ω	0.25 A

- Extremely high dv/dt capability
- Improved ESD capability
- 100% avalanche tested
- Gate charge minimized
- Very low intrinsic capacitance
- Zener-protected

Application

- AC adaptors and battery chargers
- Switch mode low-power supplies (SMPS)

Description

This high-voltage device is a Zener-protected N-channel Power MOSFET developed using the SuperMESH technology by STMicroelectronics, an optimization of the well-established PowerMESH. In addition to a significant reduction in on-resistance, this device is designed to ensure a high level of dv/dt capability for the most demanding applications.

Product status link
STS1NK60Z

Product summary	
Order code	STS1NK60Z
Marking	1NK60Z)
Package	SO-8
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	600	V
V_{GS}	Gate-source voltage	±30	V
I_D	Drain current (continuous) at T_C = 25 °C	0.25	A
	Drain current (continuous) at T_C = 100 °C	0.16	
I_{DM}(1)	Drain current (pulsed)	1	A
P_{TOT}	Total power dissipation at T_A = 25 °C	2	W
ESD	Gate-source, human body model (R = 1.5 kΩ, C = 100 pF)	0.8	kV
dv/dt(2)	Peak diode recovery voltage slope	4.5	V/ns
T_{stg}	Storage temperature range	-55 to 150	°C
T_J	Operating junction temperature range		°C

1. *Pulse width limited by safe operating area.*
2. *I_{SD} ≤ 250 mA, di/dt ≤ 200 A/µs, V_{DD} (peak) ≤ $V_{(BR)DSS}$.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance, junction-to-ambient	62.5	°C/W

2 Electrical characteristics

T_C = 25 °C unless otherwise specified.

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	600			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 600 V			1	µA
		V_{GS} = 0 V, V_{DS} = 600 V, T_C = 125 °C(1)			50	
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±20 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 50 µA	3.00	3.75	4.50	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 0.4 A		11	15	Ω

1. *Specified by design, not tested in production.*

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0 V	-	94		pF
C_{oss}	Output capacitance		-	17.6		pF
C_{rss}	Reverse transfer capacitance		-	2.8		pF
$C_{oss\ eq.}$ (1)	Equivalent output capacitance	V_{GS} = 0 V, V_{DS} = 0 V to 480 V	-	11		pF
Q_g	Total gate charge	V_{DD} = 480 V, I_D = 0.8 A, V_{GS} = 0 to 10 V (see Figure 13. Test circuit for gate charge behavior)	-	4.9	6.9(2)	nC
Q_{gs}	Gate-source charge		-	1		nC
Q_{gd}	Gate-drain charge		-	2.7		nC

1. *$C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS}increases from 0 to 80% V_{DSS}.*
2. *Specified by design, not tested in production.*

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 300 V, I_D = 0.4 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 12. Test circuit for resistive load switching times and Figure 17. Switching time waveform)	-	5.5	-	ns
t_r	Rise time		-	5	-	ns
$t_{d(off)}$	Turn-off delay time		-	13	-	ns
t_f	Fall time		-	28	-	ns
$t_{r(v)}$	Voltage rise time	V_{DD} = 480 V, I_D = 0.8 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	28	-	ns
$t_{f(i)}$	Fall time		-	12.5	-	ns
$t_{c(off)}$	Crossing time		-	48	-	ns

Table 6. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		0.25	A
I_{SDM}(1)	Source-drain current (pulsed)		-		1	A
V_{SD}(2)	Forward on voltage	I_{SD} = 0.25 A, V_{GS} = 0 V	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 0.8 A, di/dt = 100 A/µs	-	140		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 20 V, T_J = 150 °C	-	224		nC
I_{RRM}	Reverse recovery current	(see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	3.2		A

1. *Pulse width is limited by safe operating area.*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

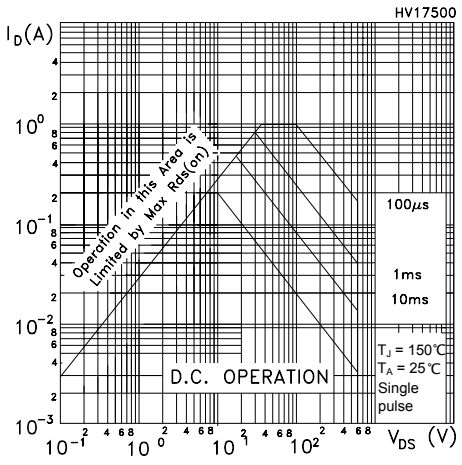


Figure 2. Normalized transient thermal impedance

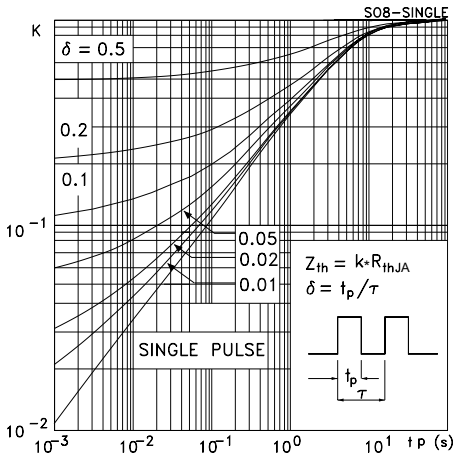


Figure 3. Typical output characterisics

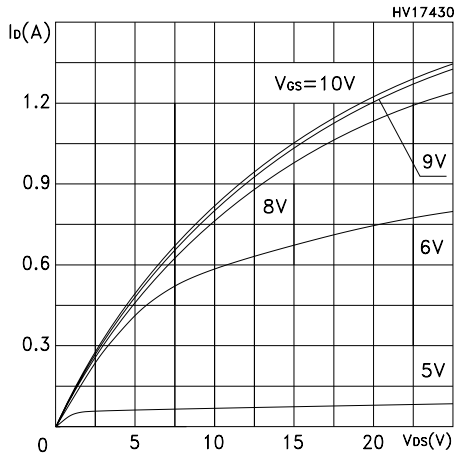


Figure 4. Typical transfer characteristics

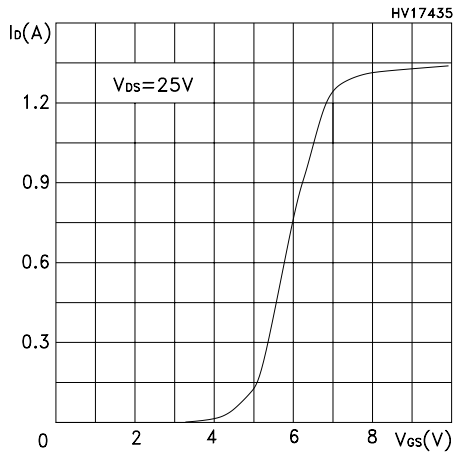


Figure 5. Normalized breakdown voltage vs temperature

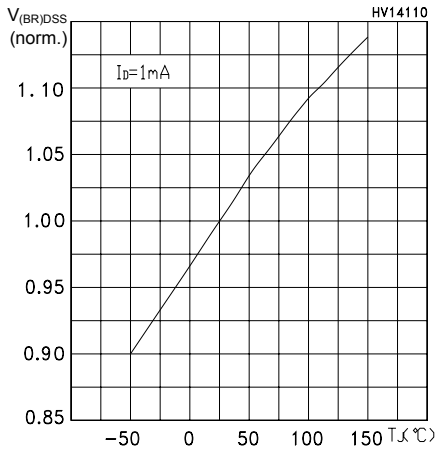


Figure 6. Typical drain-source on-resistance

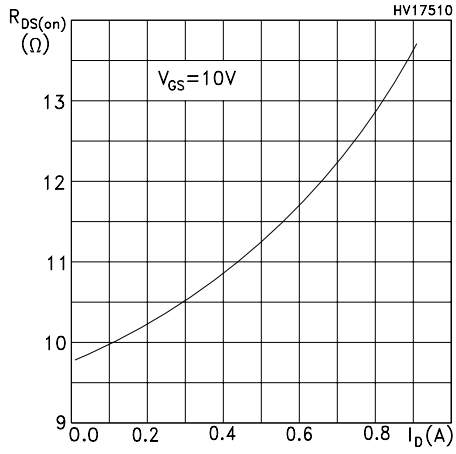


Figure 7. Typical gate charge characteristics

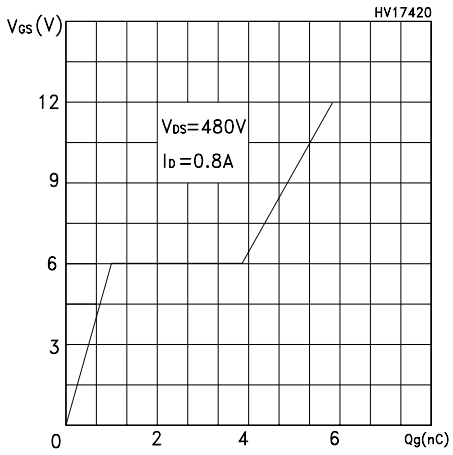


Figure 8. Typical capacitance characteristics

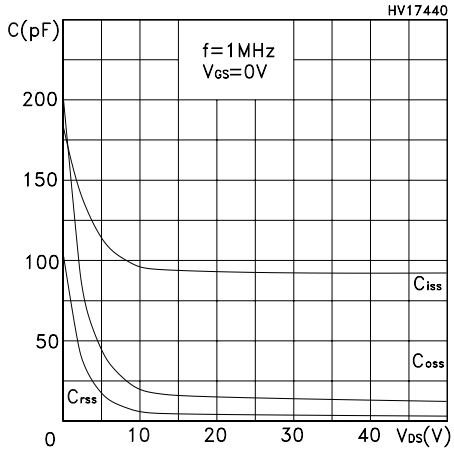


Figure 9. Normalized gate threshold vs temperature

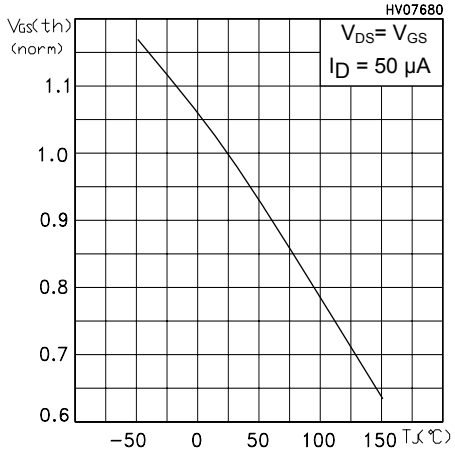


Figure 10. Normalized on-resistance vs temperature

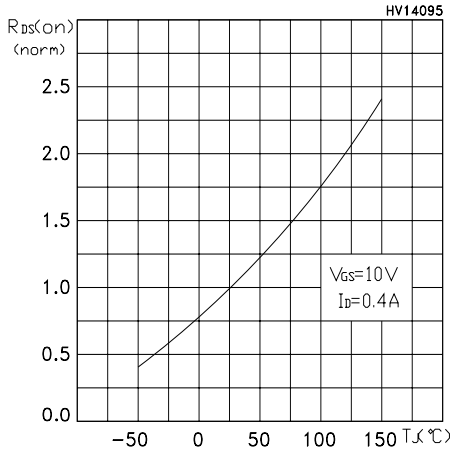
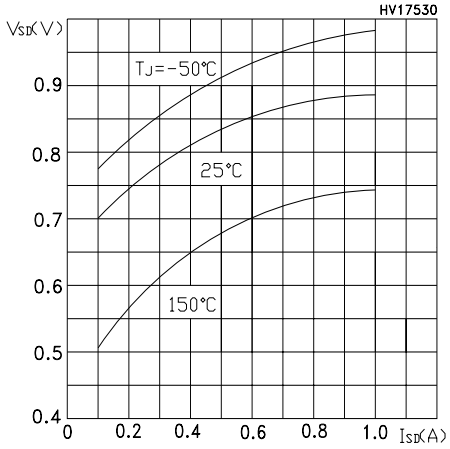
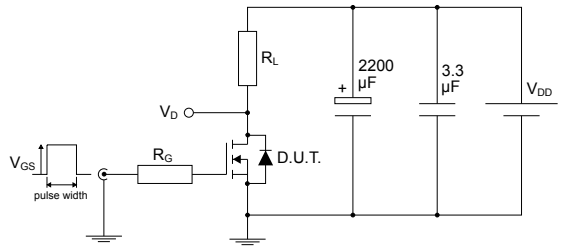


Figure 11. Typical reverse diode forward characteristics



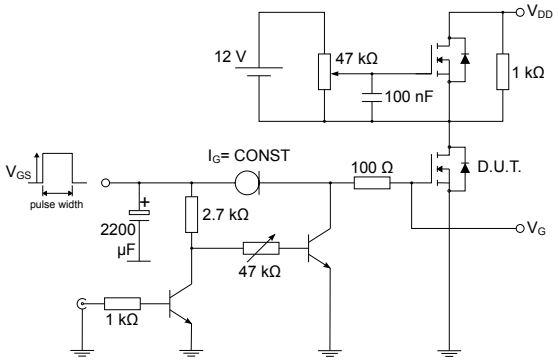
3 Test circuits

Figure 12. Test circuit for resistive load switching times



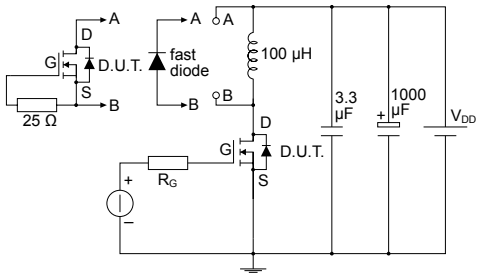
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Figure 13. Test circuit for gate charge behavior



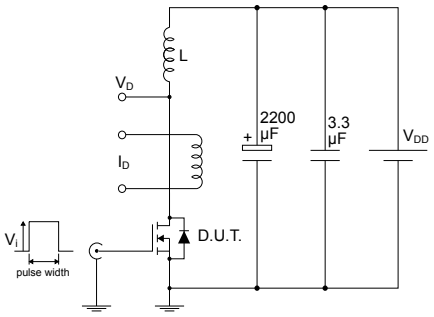
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Figure 14. Test circuit for inductive load switching and diode recovery times



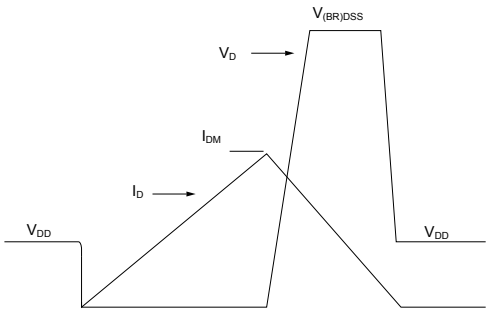
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Figure 15. Unclamped inductive load test circuit



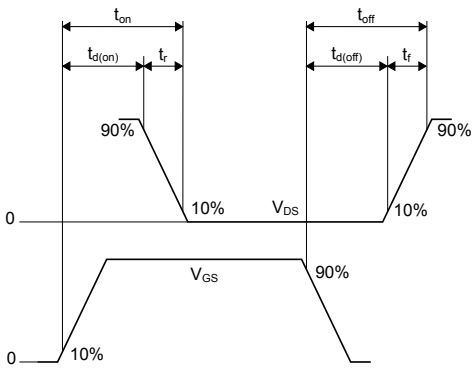
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Figure 16. Unclamped inductive waveform



AM01472v1

Figure 17. Switching time waveform



AM01473v1

4 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 SO-8 package information

Figure 18. SO-8 package outline

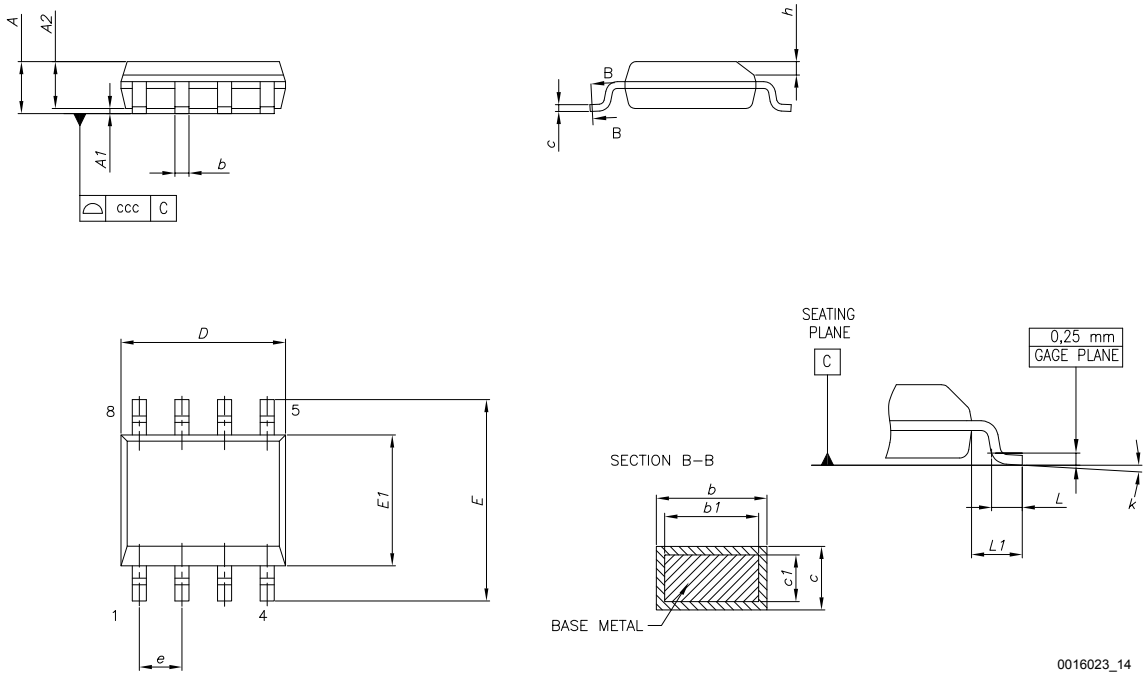
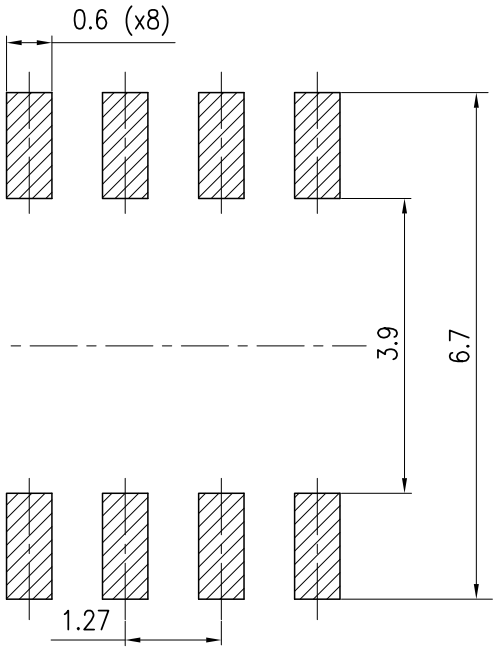


Table 7. **SO-8 mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.31		0.51
b1	0.28		0.48
c	0.10		0.25
c1	0.10		0.23
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
L1		1.04	
L2		0.25	
k	0°		8°
ccc			0.10

Figure 19. **SO-8 recommended footprint (dimensions are in mm)**



4.2 SO-8 packing information

Figure 20. **SO-8 tape and reel dimensions**

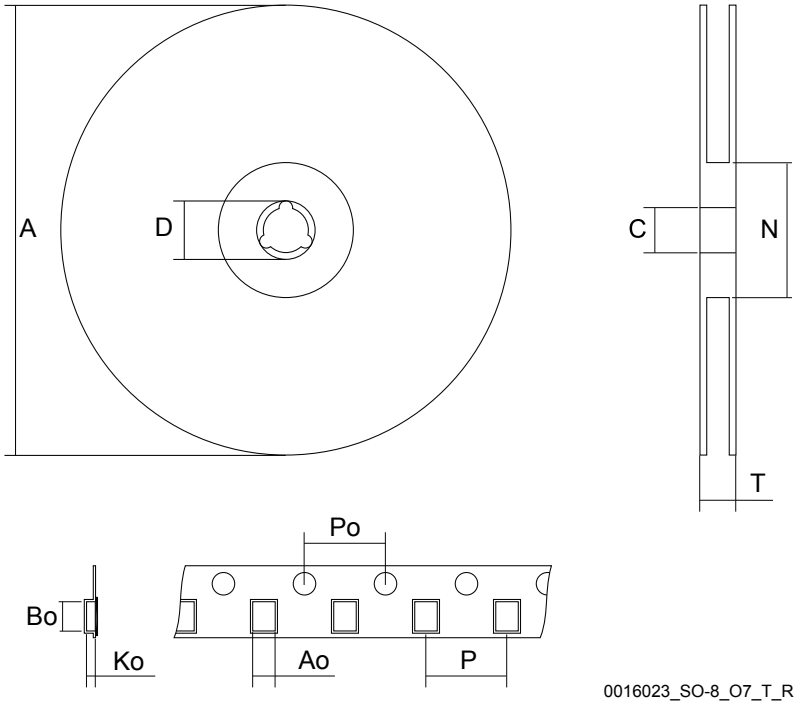


Figure 21. **Tape orientation**

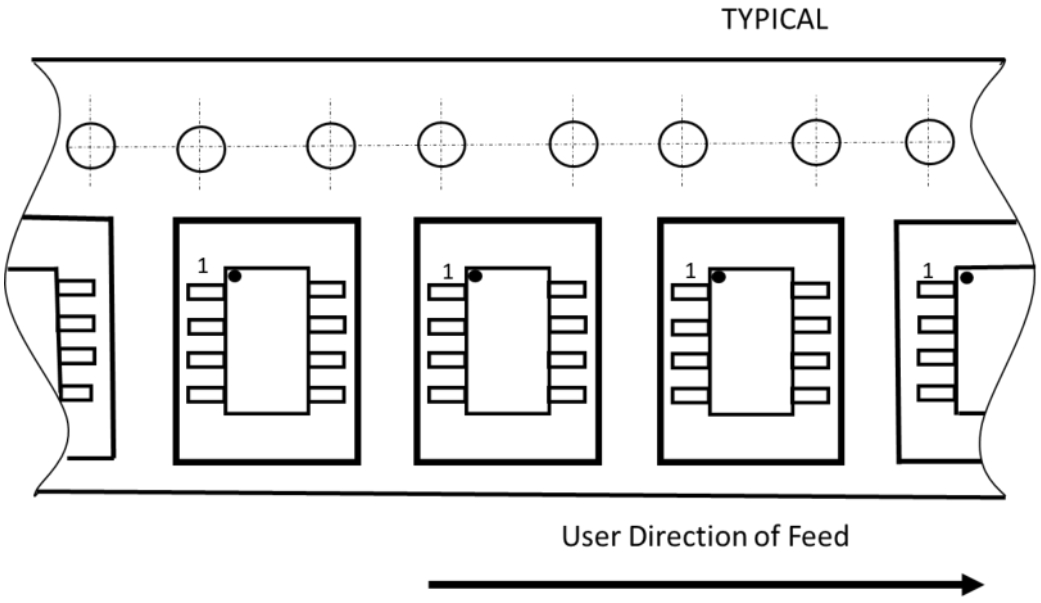


Table 8. **SO-8 tape and reel mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A		-	330
C	12.8		13.2
D	20.2		
N	60		
T			22.4
Ao	6.5		6.7
Bo	5.4		5.6
Ko	2.0		2.2
Po	3.9		4.1
P	7.9		8.1

Revision history

Table 9. **Document revision history**

Date	Revision	Changes
11-Nov-2025	3	Updated marking on cover page. Updated Section 4: Package information. Minor text changes.

Contents

1 **Electrical ratings** 2
2 **Electrical characteristics** 3
2.1 Electrical characteristics (curves) 5
3 **Test circuits** 7
4 **Package information** 8
4.1 SO-8 package information 8
4.2 SO-8 packing information 10
Revision history 12

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