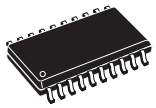
L6382D

Power management unit for LED drivers

Datasheet - production data



SO-20

Features

- Integrated high voltage startup
- 4 drivers for PFC, half-bridge and auxiliary MOSFETs
- 3.3 V microcontroller compatible
- Fully integrate power management for all operating modes
- Internal two point V_{CC} regulator
- Overcurrent protection with digital output signal
- Cross conduction protection (interlocking)
- Undervoltage lockout
- Integrated bootstrap diode

Applications

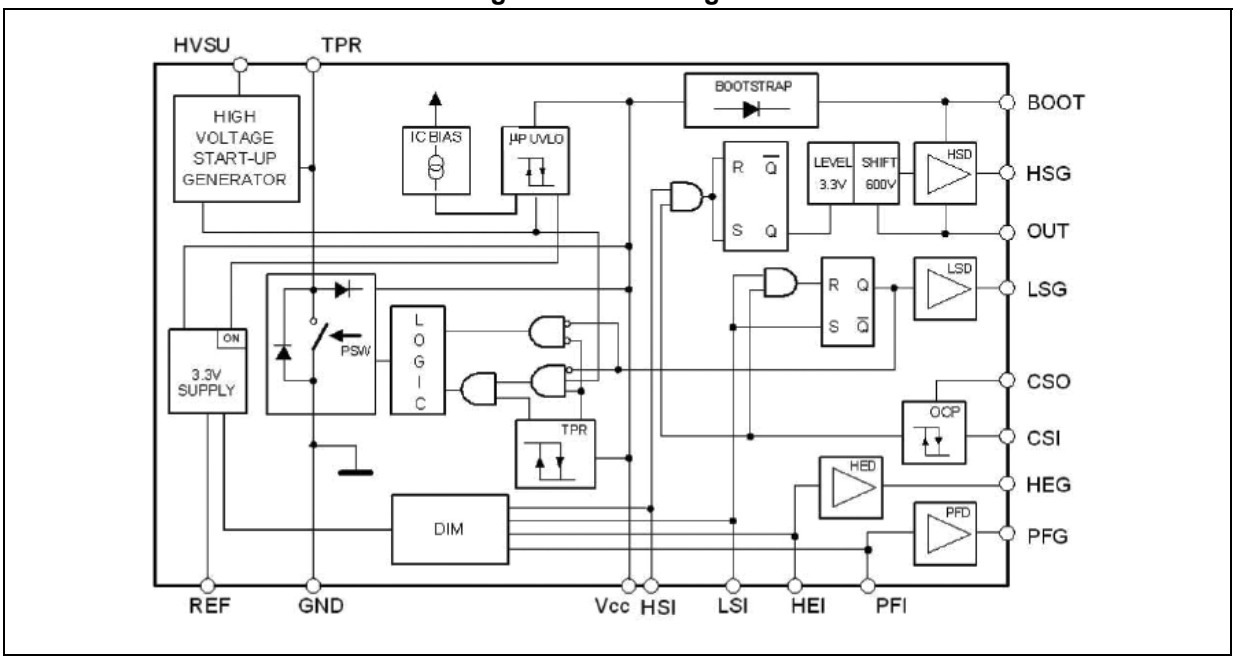
- Dimmable / non-dimmable LED drivers

Description

The L6382D device is suitable for LED drivers embedding a PFC stage and a half-bridge stage. The L6382D includes 4 MOSFET driving stages (for the PFC, for the half-bridge, and for the auxiliary MOSFET) plus a power management unit (PMU) featuring also a reference able to supply the microcontroller in any condition.

In addition to increasing application efficiency, the L6382D device reduces the bill of materials as different tasks (regarding drivers and power management) are performed by a single IC, which improves application reliability.

Figure 1. Block diagram



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1 Device description

Designed in high voltage BCD off-line technology, the L6382D is a PFC and a half-bridge stage LED drivers controller equipped with 4 input pins and a high voltage startup generator conceived for applications managed by a microcontroller, providing maximum flexibility. It allows the designer to use the same LED drivers circuit for different lamp wattages/types simply by changing the mC software.

The digital input pins - capable of receiving signals up to 400 KHz - are connected to level shifters that provide the control signals to their relevant drivers. In particular, the L6382D embeds one driver for the PFC pre-regulator stage, two drivers for the LED drivers half-bridge stage (high voltage, and also including the bootstrap function) and the last one to provide supplementary features.

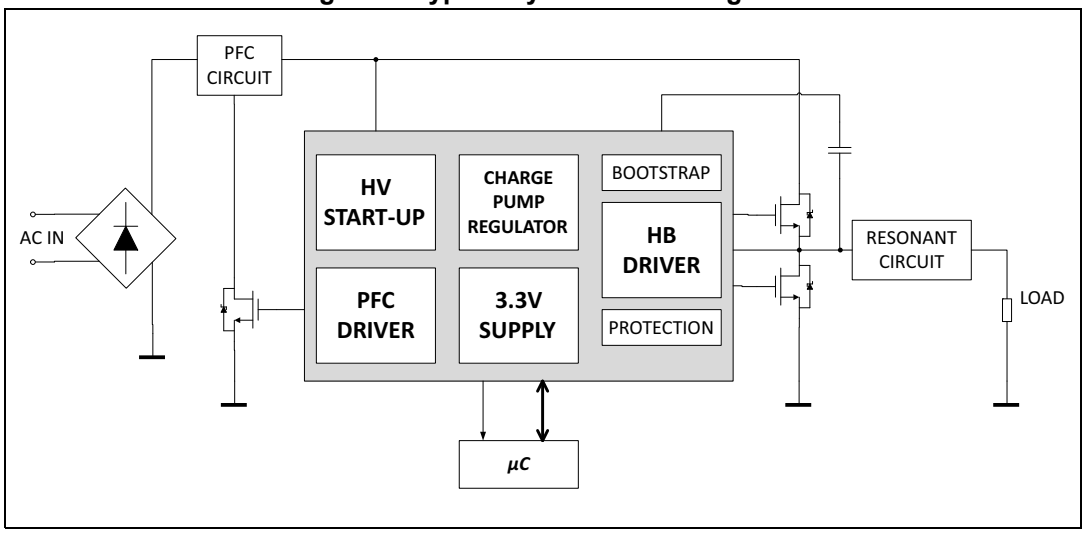
A precise reference voltage (+3.3 V ± 1%) able to provide up to 30 mA is available to supply the mC: this current is obtained thanks to the on-chip high voltage startup generator which, moreover, keeps the consumption before startup below 150 µA.

The chip was designed with advanced power management logic to minimize power losses and increase application reliability.

In the half-bridge section, a patented integrated bootstrap section replaces the external bootstrap diode.

The L6382D also integrates a function that regulates the IC supply voltage (without the need for an external charge pump) and optimizes the current consumption.

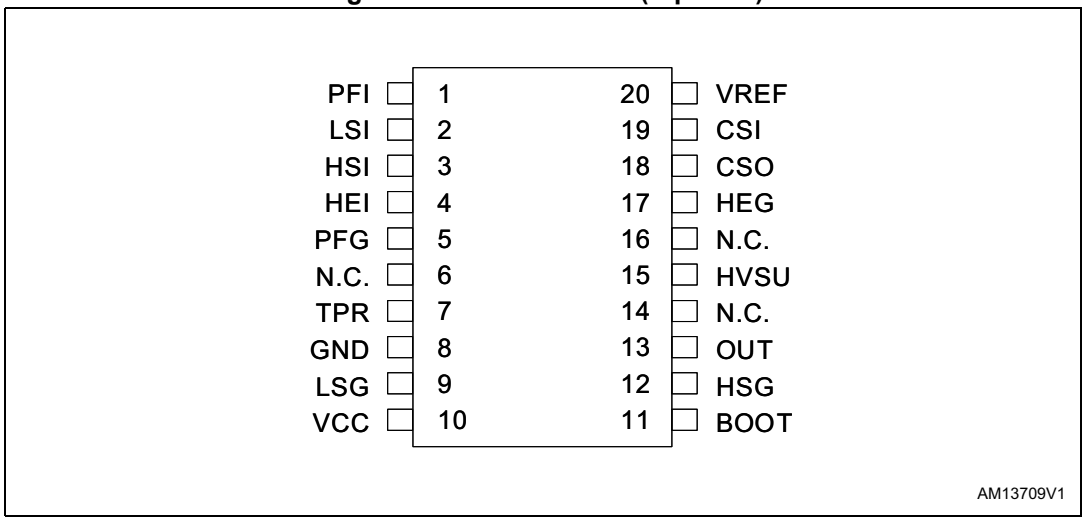
Figure 2. Typical system block diagram



2 Pin settings

2.1 Pin connection

Figure 3. Pin connection (top view)



2.2 Pin description

Table 1. Pin description

Name	Pin no.	Description
1	PFI	Digital input signal to control the PFC gate driver. This pin must be connected to a TTL compatible signal.
2	LSI	Digital input signal to control the half-bridge low-side driver. This pin must be connected to a TTL compatible signal.
3	HSI	Digital input signal to control the half-bridge high-side driver. This pin must be connected to a TTL compatible signal.
4	HEI	Digital input signal to control the HEG output. This pin must be connected to a TTL compatible signal.
5	PFG	PFC driver output. This pin is intended to be connected to the PFC power MOSFET gate. A resistor connected between this pin and the power MOS gate can be used to reduce the peak current. An internal 10 kΩ resistor toward ground avoids spurious and undesired MOSFET turn-on. The totem pole output stage is able to drive the power MOS with a peak current of 120 mA source and 250 mA sink.
6	N.C.	Not connected.
7	TPR	Input for two point regulator; by coupling the pin with a capacitor to a switching circuit, it is possible to implement a charge circuit for the Vcc.
8	GND	Chip ground. Current return for both the low-side gate drive currents and the bias current of the IC. All of the ground connections of the bias components should be tied to a trace going to this pin and kept separate from any pulsed current return.

Table 1. Pin description (continued)

Name	Pin no.	Description
9	LSG	Low-side driver output. This pin must be connected to the gate of the half-bridge low-side power MOSFET. A resistor connected between this pin and the power MOS gate can be used to reduce the peak current. An internal 20 kΩ resistor toward ground avoids spurious and undesired MOSFET turn-on. The totem pole output stage is able to drive power with a peak current of 120 mA source and 120 mA sink.
10	Vcc	Supply voltage for the signal part of the IC and for the drivers.
11	BOOT	High-side gate drive floating supply voltage. The bootstrap capacitor connected between this pin and pin 13 (OUT) is fed by an internal synchronous bootstrap diode driven in phase with the low-side gate drive. This patented structure normally replaces the external diode.
12	HSG	High-side driver output. This pin must be connected to the gate of the half bridge high-side power MOSFET. A resistor connected between this pin and the power MOS gate can be used to reduce the peak current. An internal 20 kΩ resistor toward OUT pin avoids spurious and undesired MOSFET turn-on The totem pole output stage is able to drive the power MOS with a peak current of 120 mA source and 120 mA sink.
13	OUT	High-side gate drive floating ground. Current return for the high-side gate drive current. Layout carefully the connection of this pin to avoid too large spikes below ground.
14	N.C.	Not connected.
15	HVSU	High voltage startup. The current flowing into this pin charges the capacitor connected between pin Vcc and GND to start up the IC. While the chip is in save mode, the generator is cycled on-off between turn-on and *save* mode voltages. When the chip works in *operating* mode the generator is shut down and it is re-enabled when the Vcc voltage falls below the UVLO threshold. According to the required V_{REF} pin current, this pin can be connected to the rectified mains voltage either directly or through a resistor.
16	N.C.	High voltage spacer. The pin is not connected internally to isolate the high voltage pin and comply with safety regulations (creepage distance) on the PCB.
17	HEG	Output for the HEI block; this driver can be used to drive the MOS. An internal 20 kΩ resistor toward ground avoids spurious and undesired MOSFET turn-on.
18	CSO	Output of current sense comparator, compatible with TTL logic signal; during operating mode, the pin is forced low whereas whenever the OC comparator is triggered (CSI > 0.5 V typ.) the pin latches high.
19	CSI	Input of current sense comparator, it is enabled only during operating mode; when the pin voltage exceeds the internal threshold, the CSO pin is forced high and the half bridge drivers are disabled. It exits from this condition by either cycling the Vcc below the UVLO or with LGI = HGI = low simultaneously.
20	VREF	Voltage reference. During normal mode an internal generator provides an accurate voltage reference that can be used to supply up to 30 mA (during operating mode) to an external circuit. A small film capacitor (0.22 µF min.), connected between this pin and GND is recommended to ensure the stability of the generator and to prevent noise from affecting the reference.

3 Maximum ratings

3.1 Absolute maximum ratings

Table 2. Absolute maximum ratings

Symbol	Pin	Parameter	Value	Unit
V_{CC}	10	IC supply voltage (ICC = 20 mA)	Self-limited	
V_{HVSU}	15	High voltage startup generator voltage range	-0.3 to 600	V
V_{BOOT}	11	Floating supply voltage	-1 to V_{HVSU} +V_{CC}	V
V_{OUT}	13	Floating ground voltage	-1 to 600	V
$I_{TPR(RMS)}$	7	Maximum TPR RMS current	± 200	mA
$I_{TPR(PK)}$	7	Maximum TPR peak current	± 600	mA
V_{TPR}	7	Maximum TPR voltage(1)	14	V
	19	CSI input voltage	-0.3 to 7	V
	1, 2, 3, 4	Logic input voltage	-0.3 to 7	V
	9, 12, 17	Operating frequency	15 to 400	KHz
	5	Operating frequency	15 to 600	KHz
Tstg		Storage temperature	-40 to +150	°C
T_J		Junction temperature operating range	-40 to +150	°C

1. Excluding operating mode.

3.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Maximum thermal resistance junction ambient	120	°C/W

4 Electrical characteristics

(T_J = 25 °C, V_{CC} = 13 V, C_{DRIVER} = 1 nF unless otherwise specified).

Table 4. Electrical characteristics

Symbol	Pin	Parameter	Test condition	Min.	Typ.	Max.	Unit
Supply voltage							
V_{CCON}	10	Turn-on voltage		13	14	15	V
V_{CCOFF}	10	Turn-off voltage		7.5	8.25	9.2	V
V_{CCSM}	10	Save mode voltage		12.75	13.8	14.85	V
VSMhys	10	Save mode hysteresis		0.12	0.16	0.2	V
$V_{REF(OFF)}$	10	Reference turn-off		5.7	6	6.4	V
IvccON	10	Startup current				150	µA
IvccSM	10	Save mode current consumption				190	µA
			Tj = -40 °C to 150 °C		150	230	µA
Ivcc	10	Quiescent current in operating mode	LGI = HGI = high; no load on V_{REF}			2	mA
Vz	10	Internal clamp voltage		16.5		18	V
High voltage startup							
IMSS	15	Maximum current	V_{HVSU} > 50 V	20			mA
ILSS	15	Leakage current off state	V_{HVSU} = 600 V			40	µA
Two point regulator (TPR) protection							
TPR_{st}	10	Vcc protection level	Operating mode	14.0	14.5	15.0	V
$TPR_{(ON)}$	10	Vcc turn-on level	Operating mode; after the first falling edge on LSG	12.5	13	13.5	V
$TPR_{(OFF)}$	10	Vcc turn-off level	Operating mode; after the first falling edge on LSG	12.45	12.95	13.48	V
	7	Output voltage on state	ITPR = 200 mA			2	V
	7	Forward voltage drop diode	At 600 mA forward current			2.3	V
	7	Leakage current off state	VTPR = 13 V			5	µA

Table 4. Electrical characteristics (continued)

Symbol	Pin	Parameter	Test condition	Min.	Typ.	Max.	Unit
LSG, HEG and PFG drivers							
$V_{OH(LS)}$	5, 9	HIGH output voltage	ILSG = IPFG = 10 mA		12.5		V
	17		IHEG = 2.5 mA				
$V_{OL(LS)}$	5, 9	LOW output voltage	ILSG = IPFG = 10 mA		0.5		V
	17		IHEG = 2.5 mA				
		Source current capability	LSG and PFG	120			mA
			HEG	50			mA
		Sink current capability	LSG	120			mA
			HEG	70			
			PFG	250			
T_{RISE}		Rise time	LSG		115		ns
			HEG		300		ns
			PFG		60		ns
T_{FALL}		Fall time	LSG		75		ns
			HEG		110		ns
			PFG		40		ns
T_{DELAY}		Propagation delay (input to output)	LSG; high to low and low to high			300	ns
			HEG; high to low and low to high			200	ns
			PFG; high to low			250	ns
			PFG; low to high			200	ns
R_B		Pull-down resistor	LSG		20		KΩ
			HEG		50		KΩ
			PFG		10		KΩ
HSG driver (voltages referred to OUT)							
$V_{OH(HS)}$	12	HIGH output voltage	IHSG = 10 mA		12.5		V
$V_{OL(HS)}$	12	LOW output voltage	IHSG = 10 mA		0.5		V
	12	Sink current capability		120			mA
	12	Source current capability		120			mA
T_{RISE}	12	Rise time	C_{load} = 1 nF		115		ns
T_{FALL}	12	Fall time	C_{load} = 1 nF		75		ns

Table 4. Electrical characteristics (continued)

Symbol	Pin	Parameter	Test condition	Min.	Typ.	Max.	Unit
T_{DELAY}	12	Propagation delay (LGI to LSG)	High to low and low to high			300	ns
R_B	12	Pull-down resistor	To OUT		20		KΩ
High-side floating gate driver supply							
I_{LKBOOT}	11	V_{BOOT} pin leakage current	V_{BOOT} = 580 V			5	µA
I_{LKOUT}	13	OUT pin leakage current	V_{OUT} = 562 V			5	µA
$R_{DS(on)}$		Synchronous bootstrap diode on-resistance	V_{LVG} = HIGH		150		Ω
		Forward voltage drop	At 10 mA forward current		2.4		V
		Forward current	At 5 V forward voltage drop	20			mA
V_{REF}							
V_{REF}	20	Reference voltage	15 mA load	3.267	3.3	3.366	V
	20	Load regulation	I_{REF} = -3 to +30 mA	-20		2	mV
	20	Voltage change	15 mA load; Vcc = 9 V to 15 V			15	mV
V_{REF_LATCH}	20	V_{REF} latched protection				2	V
	20	V_{REF} clamp at 3 mA	V_{CC} from 0 to V_{CCON} during startup; Vcc from $V_{REF(OFF)}$ to 0 during shutdown; V_{REF} < 2 V		1.2	1.4	V
I_{REF}	20	Current drive capability		-3		+30	mA
			Save mode	-3		+10	mA
Overcurrent buffer stage							
V_{CSI}	19	Comparator level		0.537	0.56	0.582	V
I_{CSI}	19	Input bias current				500	nA
		Propagation delay	CSO turn off to LSG low			200	ns
	18	High output voltage	I_{CSO}= 200 µA	V_{REF} -0.5 V			
	18	Low output voltage	I_{CSO} = -150 µA			0.5	V

Table 4. Electrical characteristics (continued)

Symbol	Pin	Parameter	Test condition	Min.	Typ.	Max.	Unit
DIM							
		Normal mode time out		70	100	130	µs
		V_{REF} enabling drivers			3.0		V
T_{ED}		Time enabling drivers			10		µs
Logic input							
	1 to 4	Low level logic input voltage				0.8	V
	1 to 4	High level logic input voltage		2.2			V
	LGI	Pull-down resistor			100		KΩ

5 Typical electrical performance

Figure 4. UVLO thresholds [V] vs. T_J

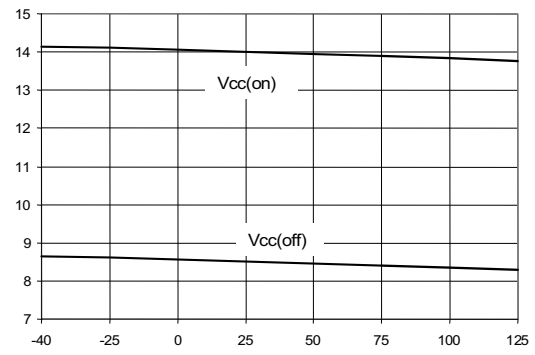


Figure 5. V_{CC} Zener voltage [V] vs. T_J

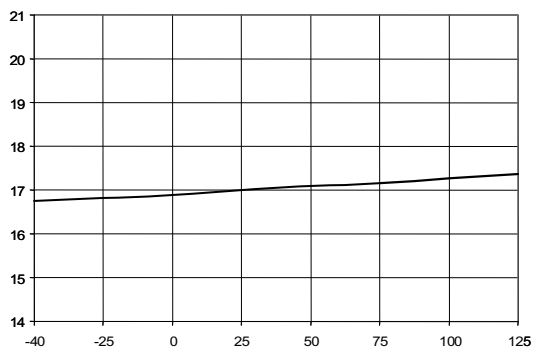


Figure 6. V_{REF} [V] vs. T_J

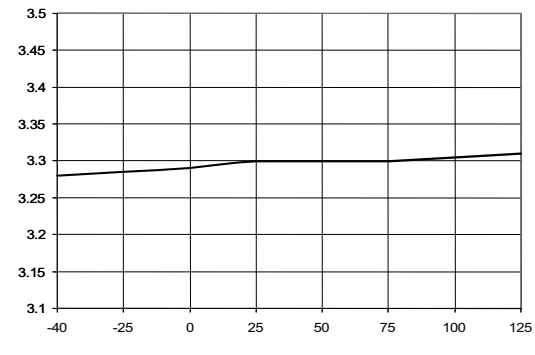


Figure 7. Overcurrent protection threshold [V] vs. T_J

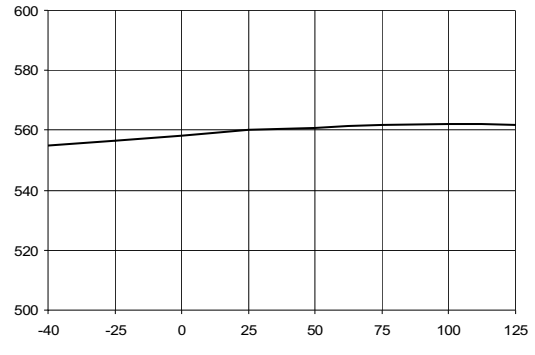


Figure 8. Propagation delays [ns] high to low vs. T_J

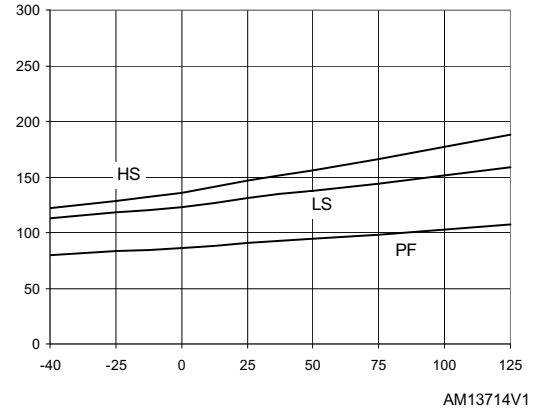
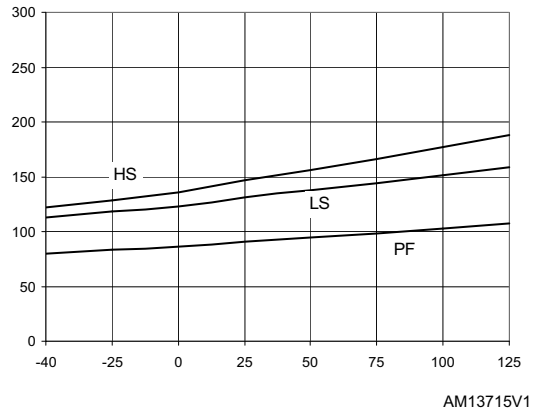


Figure 9. Propagation delays [ns] low to high vs. T_J



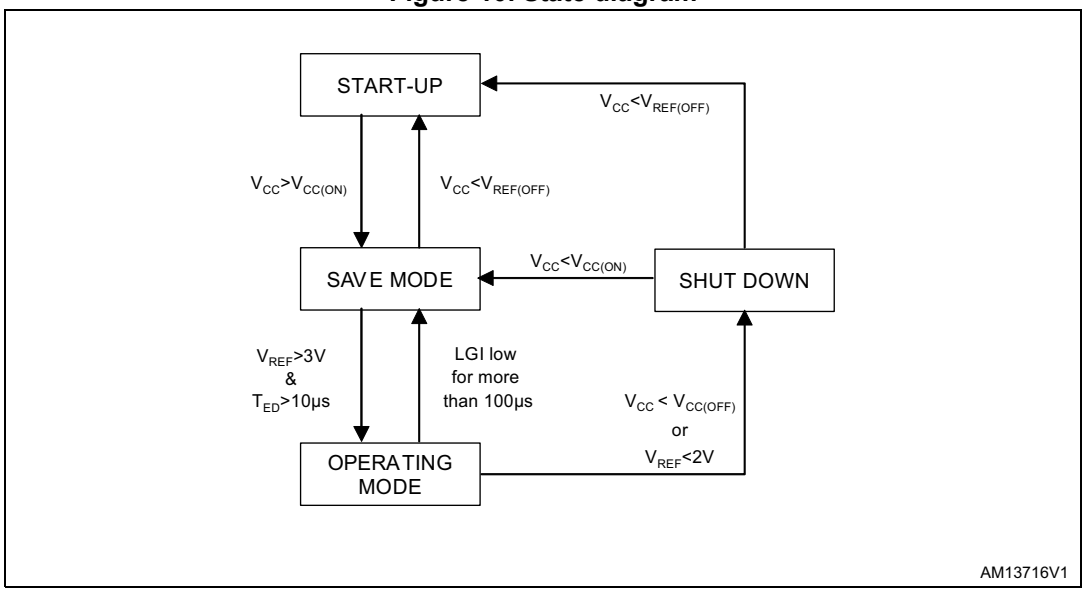
6 Application information

6.1 Power management

The L6382D has two stable states (save mode and operating mode) and two additional states that manage the startup and fault conditions (*Figure 10*): the overcurrent protection is a parallel asynchronous process enabled when in operating mode.

The following paragraphs describe each mode and the condition necessary to shift between them.

Figure 10. State diagram



6.2 Startup mode

With reference to the timing diagram in *Figure 11*, when power is first applied to the converter, the voltage on the bulk capacitor builds up and the HV generator is enabled to operate, drawing about 10 mA. This current, diminished by the IC consumption (less than 150 µA), charges the bypass capacitor connected between pin Vcc and ground and makes its voltage rise almost linearly.

During this phase, all IC functions are disabled except for:

- the current sinking circuit on the V_{REF} pin maintains the voltage low by keeping the microcontroller connected to this pin disabled;
- the high voltage startup (HVSU) that is ON (conductive) to charge the external capacitor on pin Vcc.

As the Vcc voltage reaches the startup threshold (14 V typ.) the chip starts operating and the HV generator is switched off.

To summarize:

– the high voltage startup generator is active
– VREF is disabled with an additional sinking circuit on pin V_{REF} enabled
– TPR is disabled
– OCP is disabled
– the drivers are disabled

6.2.1 Save mode

This mode is entered after the Vcc voltage reaches the turn-on threshold; the V_{REF} is enabled in low current source mode to supply the μC connected to it, the required wakeup current of which must be less than 10 mA: if no switching activity is detected at the LGI input, the high voltage startup generator cycles ON-OFF, keeping the Vcc voltage between VccON and VccSM.

Summarizing:

– the high voltage startup generator is cycling
– VREF is enabled in low source current capability ($I_{REF} \leq 10$ mA)
– TPR circuit is disabled
– OCP is disabled

the drivers are disabled.

If the Vcc voltage falls below the $V_{REF(OFF)}$ threshold, the device enters the startup mode.

6.2.2 Operating mode

After 10 μs in save mode and only if the voltage at V_{REF} is higher than 3.0 V, on the falling edge on the HGI input, the drivers are enabled as well as all the IC functions; this is the mode corresponding to the proper lamp behavior.

To summarize:

– HVSU is OFF
– VREF is enabled in high source current mode ($I_{REF} < 30$ mA)
– TPR circuit is enabled
– OCP is enabled
– the drivers are enabled

If there is no switching activity on LGI for more than 100 μs, the IC returns to save mode.

6.2.3 Shutdown

This state permits to manage the fault conditions in operating mode and it is entered by the occurrence on one of the following conditions:

1. Vcc < VccOff (undervoltage fault on supply)
2. V_{REF} < 2.0 V (undervoltage fault on V_{REF})

   In this state the functions are:
   - The HVSU generator is ON
   - VREF is enabled in low source current mode (I_{REF} < 10 mA)
   - TPR is disabled
   - OCP is disabled
   - the drivers are disabled

In this state if Vcc reaches VccOn, the device enters the save mode otherwise, if Vcc < $V_{REF(OFF)}$, also the µC is turned off and the device will be ready to execute the startup sequence.

Figure 11. Timing sequences: TPR behavior

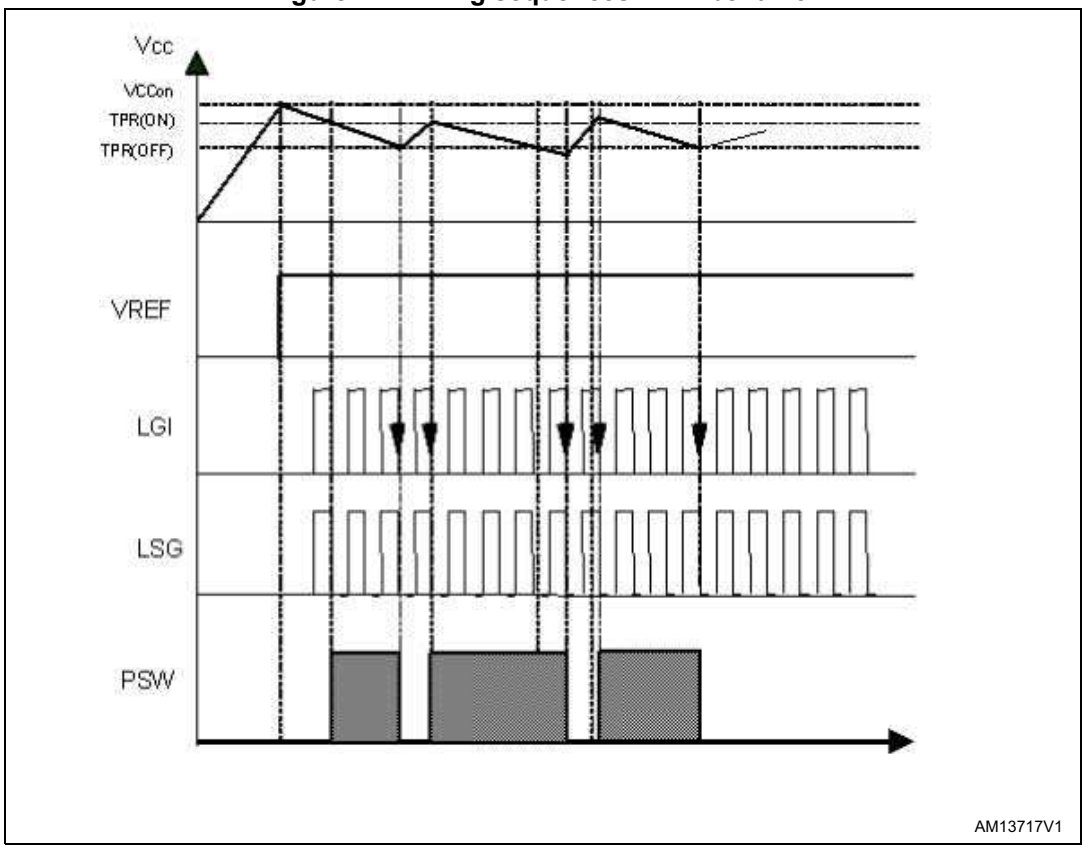
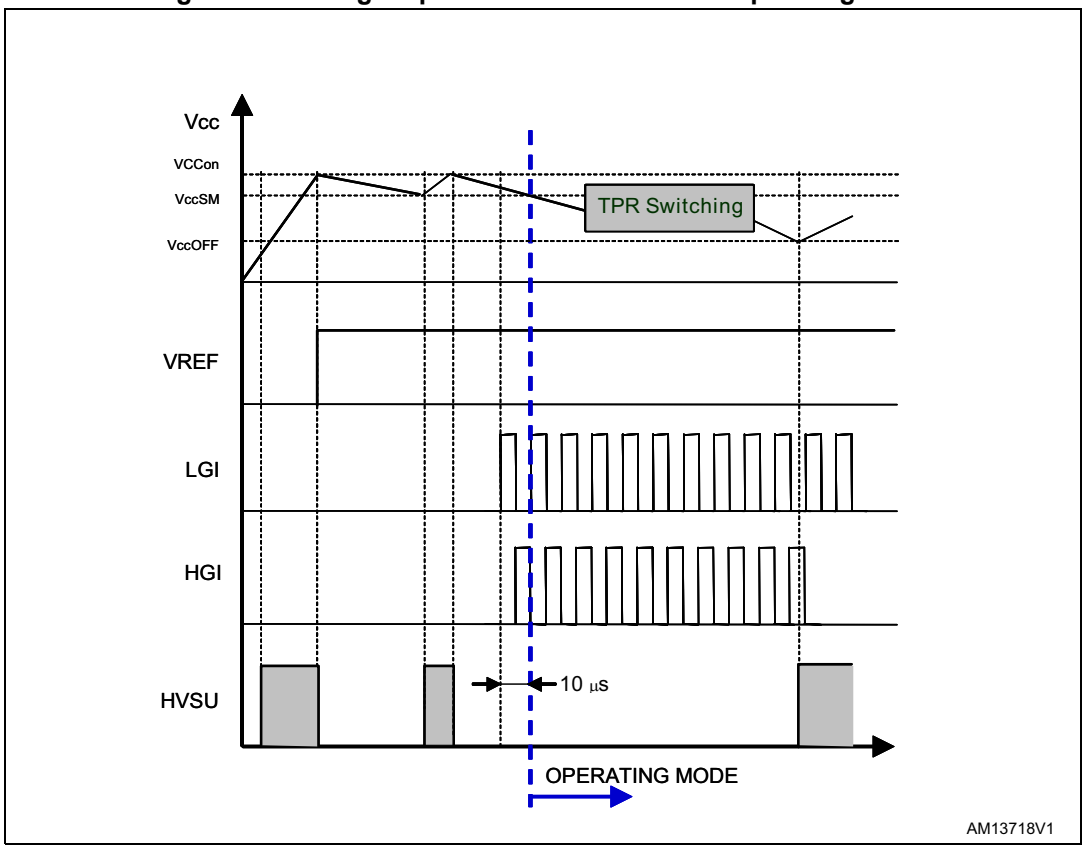


Figure 12. Timing sequences: save mode and operating mode



7 Block description

7.1 Supply section

µPUVLO (µpower undervoltage lockout): This block controls the power management of the L6382D, ensuring the correct current consumption in each operating state, the correct V_{REF} current capability, driver enabling and high voltage startup generator switching. During startup, the device sinks the current necessary to charge the external capacitor on pin V_{CC} from the high voltage bus. In this state, the other IC functions are disabled and the current consumption of the whole IC is less than 150 µA.

When the voltage on VCC pin reaches VccON, the IC enters the save mode where the µPUVLO block controls Vcc between VccON and VccSM by switching ON/OFF the high voltage startup generator.

- **HVSU (high voltage startup generator)**: a 600 V internal MOS transistor structure controls the Vcc supply voltage during startup and save mode conditions and it reduces the power losses during operating Mode by switching OFF the MOS transistor. The transistor has a source current capability of up to 30 mA.
- **TPR (two point regulator) and PWS**: during normal mode, the TPR block controls the PSW switch in order to regulate the IC supply voltage (VCC) to a value in the range between TPR(ON) and TPR(OFF) by switching ON and OFF the PSW transistor *Figure 11*.
  - Vcc > TPRst: the PSW is switched ON immediately
  - TPR(ON) < Vcc < TPRst: the PSW is switched ON at the following falling edge of LGI
  - Vcc < TPR(OFF): the PSW is switched OFF at the following falling edge on LGI

When the PSW switch is OFF, the diodes build a charge pump structure so that, connecting the TPR pin to a switching voltage (through a capacitor) it is possible to supply the low voltage section of the chip without adding any further external components. The diodes and the switch are designed to withstand a current of at least 200 mA_{RMS}.

7.2 3.3 V reference voltage

This block is used to supply the microcontroller; this source is able to supply 10 mA in save mode and 30 mA in operating mode. Moreover, during startup when V_{REF} is not yet available, an additional circuit ensures that, even sinking 3 mA, the pin voltage will not exceed 1.2 V.

The reference is available until Vcc is above $V_{REF(OFF)}$; below that it turns off and the additional sinking circuit is enabled again.

7.3 Drivers

- **LSD (low-side driver)**: it consists of a level shifter from 3.3 V logic signal (LSI) to Vcc MOS driving level; conceived for the half-bridge low-side power MOS, it is able to source and sink 120 mA (min).
- **HSD (level shifter and high-side driver)**: it consists of a level shifter from 3.3 V logic signal (HGI) to the high-side gate driver input up to 600 V. Conceived for the half-bridge high-side power MOS, the HSG is able to source and sink 120 mA.
- **PFD (power factor driver)**: it consists of a level shifter from 3.3 V logic signal (PFI) to Vcc MOS driving level: the driver is able to source 120 mA from Vcc to PFG (turn-on) and to sink 250 mA to GND (turn-off). It is suitable to drive the MOS of the PFC pre-regulator stage.
- **HED (auxiliary driver)**: it consists of a level shifter from 3.3 V logic signal (HEI) to Vcc MOS driving level; the driver is able to source 30 mA from Vcc to HEG and to sink 75 mA to GND.
- **Bootstrap circuit**: it generates the supply voltage for the high-side driver (HSD). A patented integrated bootstrap section replaces an external bootstrap diode. This section together with a bootstrap capacitor provides the bootstrap voltage to drive the high-side power MOSFET. This function is achieved using a high voltage DMOS driver which is driven synchronously with the low-side external power MOSFET. For safe operation, current flow between the BOOT pin and Vcc is always inhibited, even though ZVS operation may not be ensured.

7.4 Internal logic, overcurrent protection (OCP) and interlocking function

The DIM (digital input monitor) block manages the input signals delivered to the drivers ensuring that they are low during the described startup procedure; the DIM block controls the L6382D behavior during both save and operating modes.

When the voltage on pin CSI exceeds the internal reference of 0.5 V (typ.) the block latches the fault condition: in this state the OCP block forces low both HSG and LSG signals while CSO will be forced high. This condition remains latched until LSI and HSI are simultaneously low and CSI is below 0.5 V.

This function is suitable to implement overcurrent protection or hard-switching detection by using an external sense resistor.

As the voltage on pin CSI can go negative, the current must be limited below 2 mA by external components.

Another feature of the DIM block is the internal interlocking that prevents cross conduction in the half-bridge FETs. If by chance both HGI and LGI inputs are brought high at the same time, then LSG and HSG are forced low as long as this critical condition persists.

8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

Figure 13. SO-20 package outline

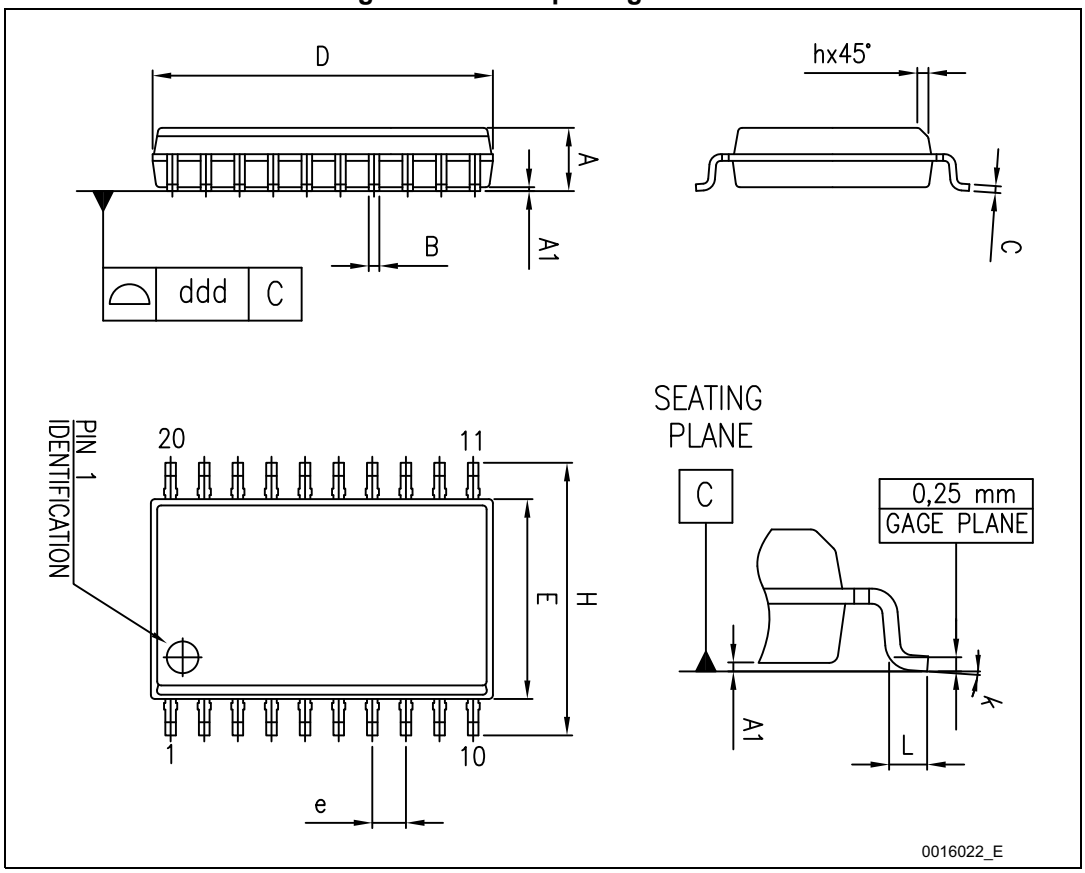


Table 5. SO-20 package mechanical data

Symbol	Dimensions (mm)		
	Min.	Typ.	Max.
A	2.35		2.65
A1	0.10		0.30
B	0.33		0.51
C	0.23		0.32
D (1)	12.60		13.00
E	7.40		7.60
e		1.27	
H	10.0		10.65
h	0.25		0.75
L	0.40		1.27
k	0°		8°
ddd			0.10

9 Order codes

Table 6. Order codes

Part number	Package	Packaging
L6382D	SO-20	Tube
L6382DTR	SO-20	Tape and reel

10 Revision history

Table 1. Document revision history

Date	Revision	Changes
15-Nov-2004	1	First Issue
03-Jan-2005	2	Changed from “Preliminary Data” to “Final Datasheet”
23-Oct-2005	3	Many modified
19-Apr-2006	4	New template
22-May-2006	5	Typo error in block diagram, updated values in electrical characteristics *Table 6.*
21-Mar-2007	6	Typo on *Table 3*
06-Jun-2013	7	Updated *Table 3: Thermal data*, *Table 4: Electrical characteristics*, *Table 5: SO-20 package mechanical data* and *Figure 9: Order codes*. Minor text changes.
01-Sep-2014	8	Updated main title *on page 1* (replaced “microcontrolled ballast” by “LED drivers”). Updated *Section : Features on page 1* (replaced “preheating” by “auxiliary). Updated *Section : Applications on page 1* (replaced “ballast” by “LED drivers”). Updated *Section : Description on page 1* (replaced “microcontrolled electronic ballast” by “LED drivers” and “preheating” by “auxiliary). Updated *Section 1: Device description on page 3* (replaced “ ballast” by “LED drivers”, added “half-bridge stage”, removed “like preheating of filaments supplied through isolated windings in dimmable applications.”, replaced *Figure 2* by new figure). Updated *Table 1: Pin description on page 4* (removed “employed in preheating isolated filaments”). Updated *Table 4: Electrical characteristics on page 7* (updated Min. value of Vz symbol, replaced “Zener” by “clamp voltage”). Updated *Section 7.3: Drivers on page 17* (removed “and it is suitable for the filament heating when they are supplied by independent winding.”, replaced “heat” by “auxiliary”). Updated *Section 8: Package information on page 18* (updated titles, reversed order of *Figure 13 on page 19* and *Table 5 on page 19*, minor modifications). Minor modifications throughout document.

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