STL100NH3LL

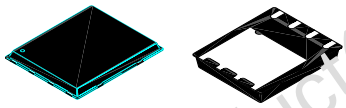
N-channel 30 V - 0.0032 Ω - 25 A - PowerFLAT™ (6x5) STripFET™ III Power MOSFET

Features

Type	V_{DSS}	$R_{DS(on)}$ max	I_D
STL100NH3LL	30 V	<0.0035 Ω	25A (1)

1. The value is rated according $R_{thj\text{-}pcb}$

- Improved die-to-footprint ratio
- Very low profile package (1 mm max)
- Very low thermal resistance
- Conduction losses reduced
- Switching losses reduced



PowerFLAT™ (6x5)

Application

- Switching applications

Description

This series utilizes the last advanced design rules of ST's proprietary STripFET™ technology. This process complete to unique metallization technique realised the most advanced low voltage Power MOSFET in PowerFLAT™(6x5). The chip-scaled PowerFLAT™ package allows a significant board space saving, still boosting the performance.

Figure 1. Internal schematic diagram

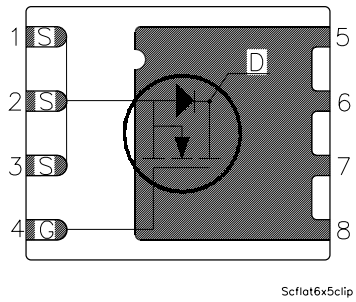


Table 1. Device summary

Order code	Marking	Package	Packaging
STL100NH3LL	L100NH3LL	PowerFLAT™ (6x5)	Tape and reel

Obsolete Product(s) - Obsolete Product(s)

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2 Electrical characteristics 4

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3 Test circuit 8

4 Package mechanical data 9

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Obsolete Product(s) - Obsolete Product(s)
Obsolete Product(s) - Obsolete Product(s)

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = 0)	30	V
V_{GS}(1)	Gate-source voltage	± 16	V
V_{GS}(2)	Gate-source voltage	± 18	V
I_D(3)	Drain current (continuous) at T_C = 25 °C	100	A
I_D (3)	Drain current (continuous) at T_C = 100 °C	71	A
I_D (5)	Drain current (continuous) at T_C=100 °C	15.6	A
I_{DM}(4)	Drain current (pulsed)	100	A
I_D(5)	Drain current (continuous) at T_C = 25 °C	25	A
P_{TOT} (3)	Total dissipation at T_C = 25 °C	80	W
P_{TOT} (5)	Total dissipation at T_C = 25 °C	4	W
	Derating factor	0.03	W/°C
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 150	°C

1. Continuous mode
2. Guaranteed for test time ≤15ms
3. The value is rated according R_{thj-c}
4. Pulse width limited by safe operating area
5. The value is rated according $R_{thj-pcb}$

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case (drain) (steady state)	1.56	°C/W
$R_{thj-pcb}$ (1)	Thermal resistance junction-ambient	31.3	°C/W

1. When mounted on FR-4 board of 1inch², 2oz Cu, t < 10 sec

Table 4. Avalanche data

Symbol	Parameter	Value	Unit
I_{AV}	Not-repetitive avalanche current	7.5	A
E_{AS}	Single pulse avalanche energy (starting T_J=25 °C, I_D=7.5 A)	150	mJ

Obsolete Product(s) - Obsolete Product(s)

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250 µA, V_{GS}= 0	30			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max rating, V_{DS} = Max rating @125 °C			1 10	µA µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ±16 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS}= V_{GS}, I_D = 250 µA	1		2.5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS}= 10 V, I_D= 12.5 A V_{GS}= 4.5 V, I_D= 12.5 A		0.0032 0.004	0.0035 0.005	Ω Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} =10 V, I_D = 12.5 A		30		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} =25 V, f=1 MHz, V_{GS}=0		4450 655 50		pF pF pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD}=15 V, I_D = 25 A V_{GS} =4.5 V *(see Figure 8)*		30 12.5 10	40	nC nC nC
R_G	Gate input resistance	f=1 MHz Gate DC Bias = 0 Test signal level = 20 mV open drain	1	2	3	Ω

1. Pulsed: pulse duration=300 µs, duty cycle 1.5%

Obsolete Product(s) - Obsolete Product(s)
Obsolete Product(s) - Obsolete Product(s)

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off delay time Fall time	V_{DD}=15 V, I_D= 12.5 A, R_G=4.7 Ω, V_{GS}=10 V *(see Figure 14)*		18 50 75 8		ns ns ns ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current				25	A
I_{SDM}(1)	Source-drain current (pulsed)				100	A
V_{SD}(2)	Forward on voltage	I_{SD}=25 A, V_{GS}=0			1.3	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD}=25 A, di/dt = 100 A/µs, V_{DD}=25 V, T_j=150 °C		32 34 2.1		ns nC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300µs, duty cycle 1.5%

Obsolete Product(s) - Obsolete Product(s)
Obsolete Product(s) - Obsolete Product(s)

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

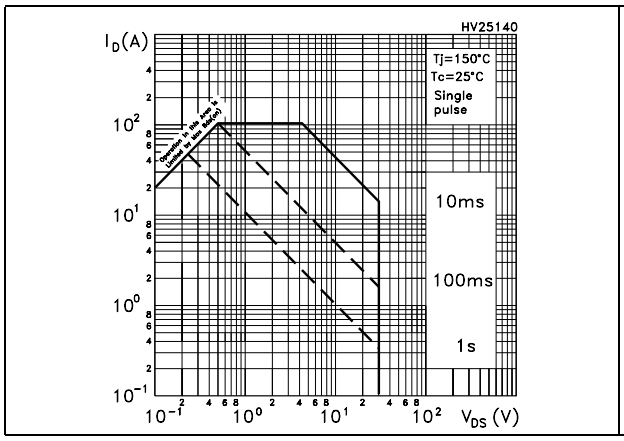


Figure 3. Thermal impedance

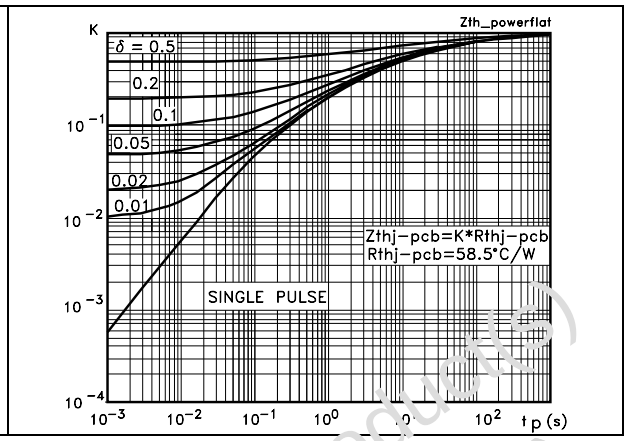


Figure 4. Output characteristics

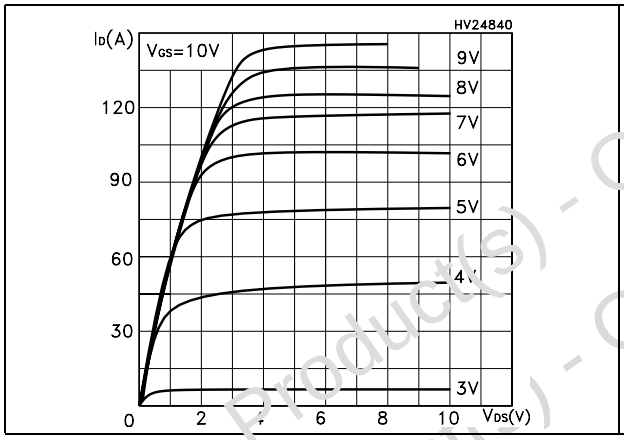


Figure 5. Transfer characteristics

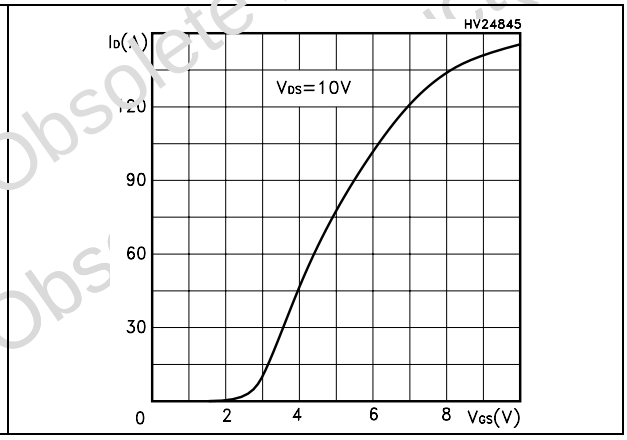


Figure 6. Transconductance

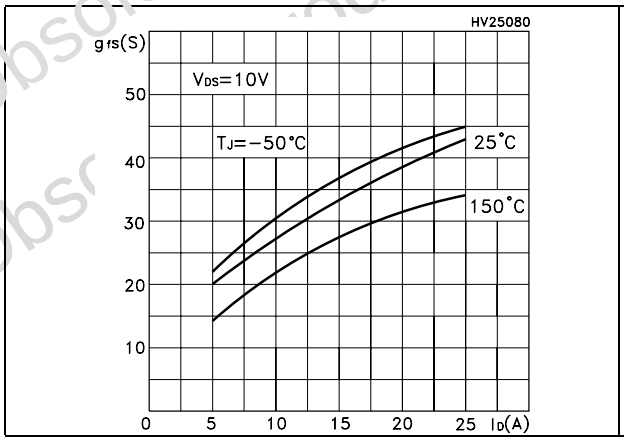
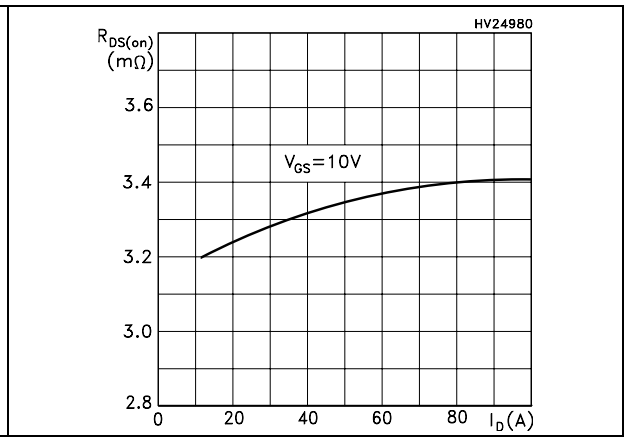


Figure 7. Static drain-source on resistance



Obsolete Product(s) - Obsolete Product(s)

Figure 8. Gate charge vs gate-source voltage

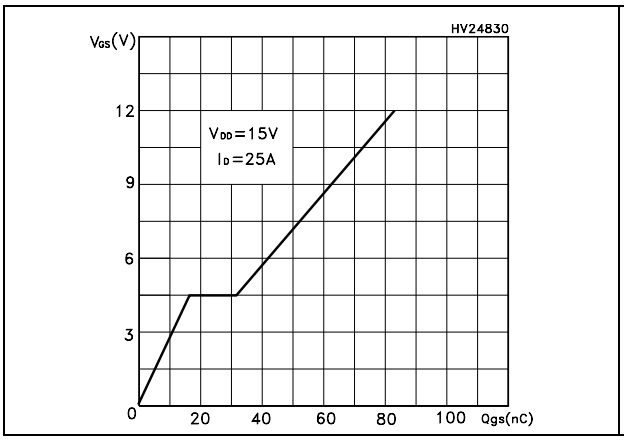


Figure 9. Capacitance variations

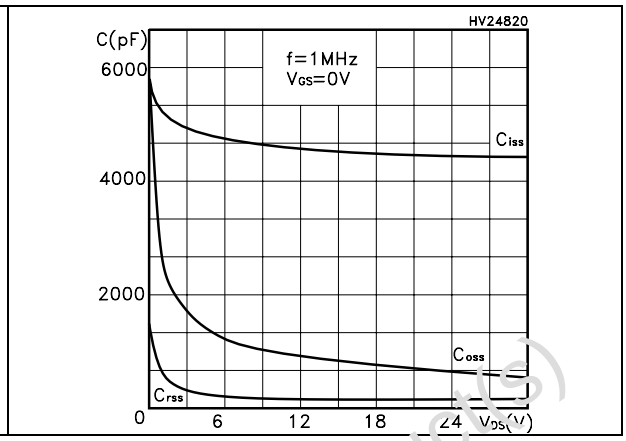


Figure 10. Normalized gate threshold voltage vs temperature

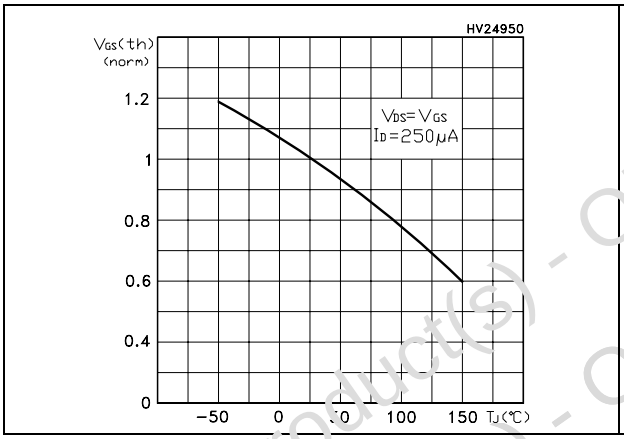


Figure 11. Normalized on resistance vs temperature

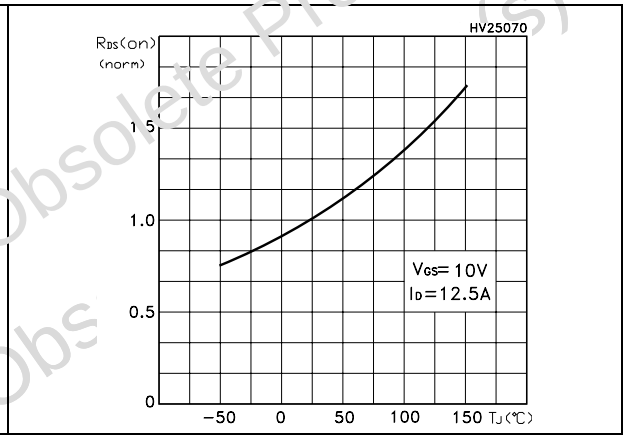


Figure 12. Source-drain diode forward characteristics

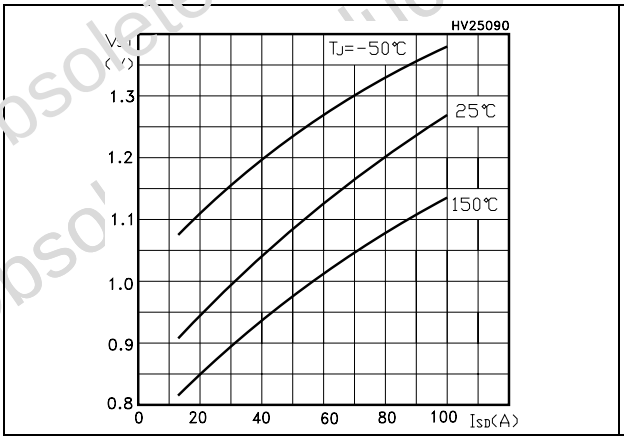
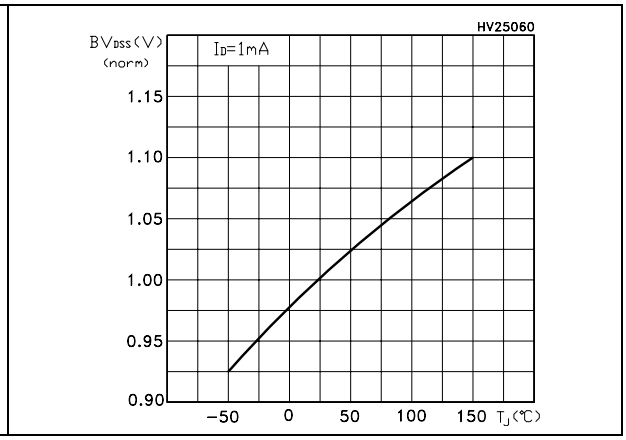


Figure 13. Normalized B_{VDSS} vs temperature



Obsolete Product(s) - Obsolete Product(s)

3 Test circuit

Figure 14. Switching times test circuit for resistive load

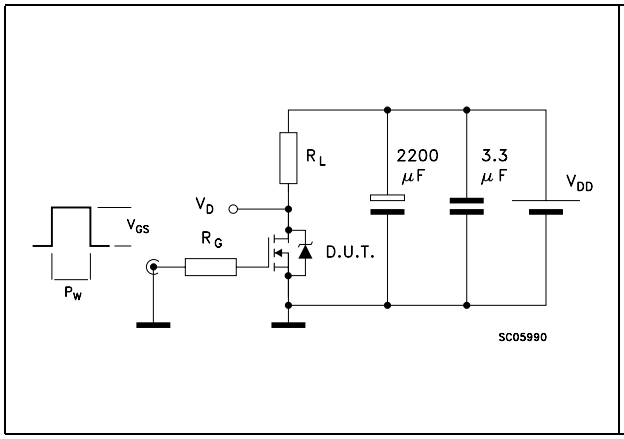


Figure 15. Gate charge test circuit

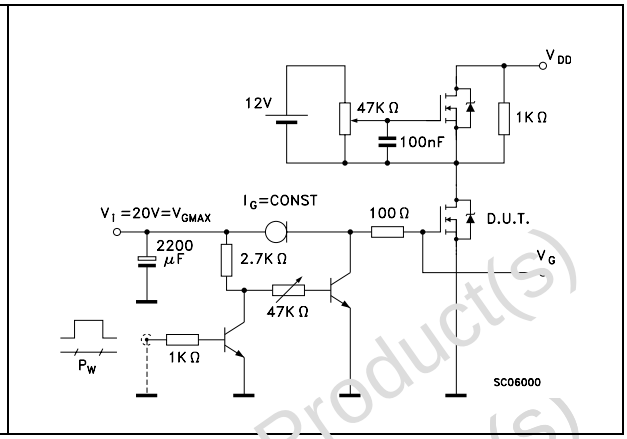


Figure 16. Test circuit for inductive load switching and diode recovery times

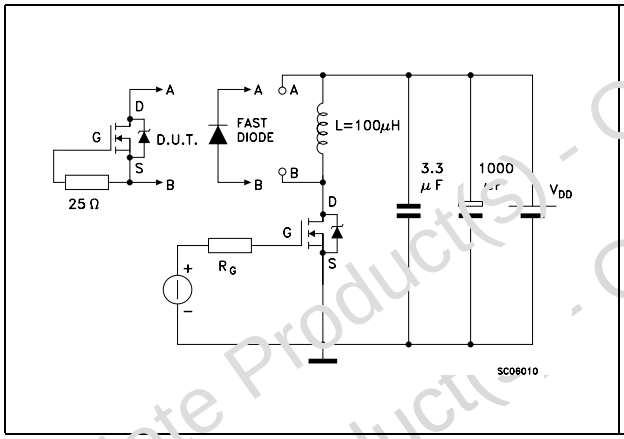


Figure 17. Unclamped inductive load test circuit

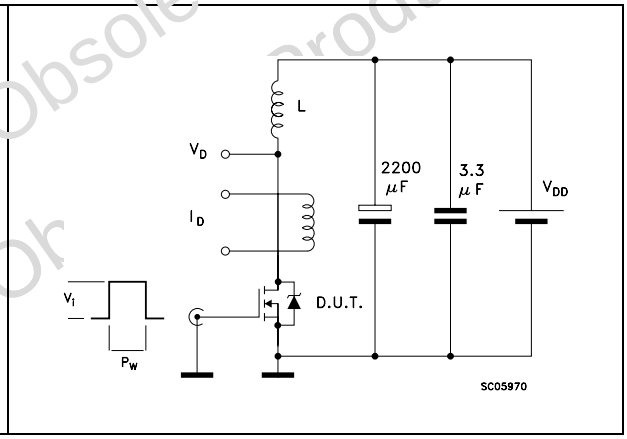


Figure 18. Unclamped inductive waveform

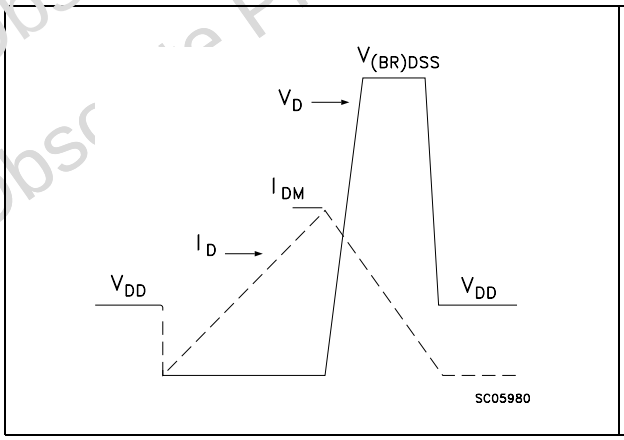
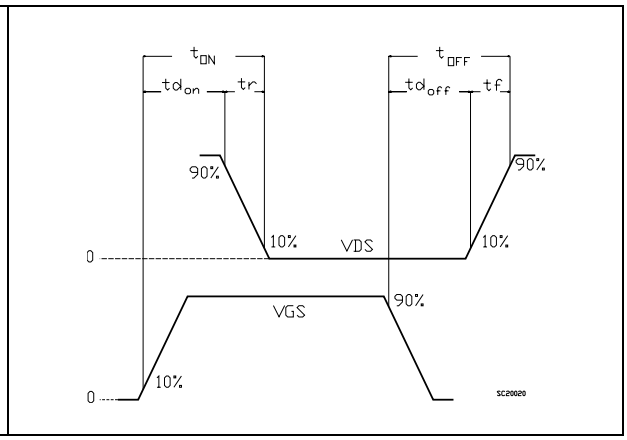


Figure 19. Switching time waveform



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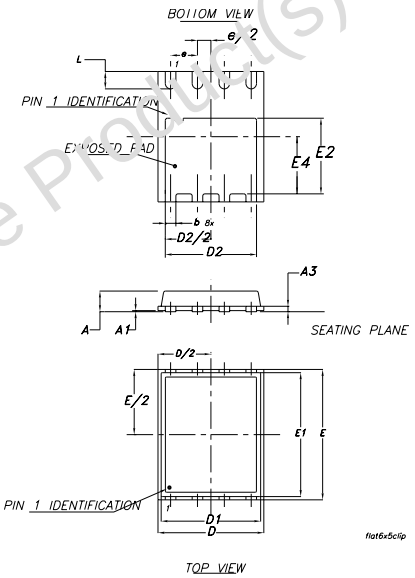
4 Package mechanical data

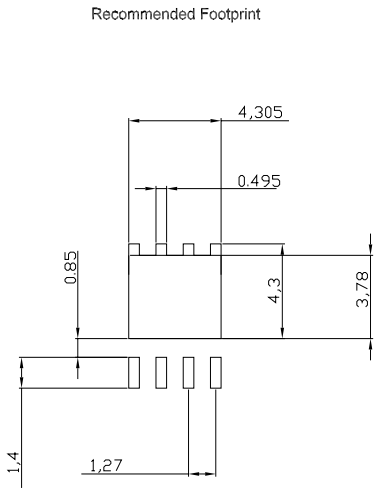
In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: *www.st.com*

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PowerFLAT™ (6x5) MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	0.80	0.83	0.93	0.031	0.032	0.036
A1		0.02	0.05		0.0007	0.0019
A3		0.20			0.007	
b	0.35	0.40	0.47	0.013	0.015	0.018
D		5.00			0.196	
D1		4.75			0.187	
D2	4.15	4.20	4.25	0.163	0.165	0.167
E		6.00			0.236	
E1		5.75			0.226	
E2	3.43	3.48	3.53	0.135	0.137	0.139
E4	2.58	2.63	2.68		0.103	0.105
e		1.27			0.050	
L	0.70	0.80	0.90	0.027	0.031	0.035





Note: all dimentions are in mm.

Obsolete Product(s) - Obsolete Product(s)

5 Revision history

Table 9. Document revision history

Date	Revision	Changes
18-Apr-2005	1	First Release
20-Jun-2005	2	Updated mechanical data
22-Jun-2005	3	New Rg value on *Table 7*
10-Oct-2005	4	Inserted ecopack indication
09-Jan-2006	5	New footprint
08-Mar-2006	6	New template
29-Jun-2006	7	Modified curves, see *Figure 2* and *Figure 3*
04-Sep-2006	8	The document has been reformatted, no content change
04-Jan-2007	9	New updated on *Table 2*
10-Dec-2007	10	Updated data on *Table 4: Avalanche data*
20-Mar-2008	11	New V_{GS} max. value inserted on *Table 4: Avalanche data*

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