VN5050J-E

Single channel high side driver for automotive applications

Features

Max supply voltage	V_{CC}	41V
Operating voltage range	V_{CC}	4.5 to 36V
Max On-State resistance (per ch.)	R_{ON}	50 mΩ
Current limitation (typ)	I_{LIMH}	19 A
Off state supply current	I_S	2 µA(1)

(1) Typical value with all loads connected.

- Main
  - Inrush current active management by power limitation
  - Very low stand-by current
  - 3.0V CMOS compatible input
  - Optimized electromagnetic emission
  - Very low electromagnetic susceptibility
  - In compliance with the 2002/95/EC European directive
- Diagnostic functions
  - Open drain status output
  - On state open load detection
  - Off state open load detection
  - Thermal shutdown indication
- Protections
  - Undervoltage shut-down
  - Overvoltage clamp
  - Output stuck to V_{CC} detection
  - Load current limitation
  - Self limiting of fast thermal transients
  - Protection against loss of ground and loss of V_{CC}
  - Thermal shut down
  - Reverse battery protection (see *Figure 27*)
  - Electrostatic discharge protection



PowerSSO-12

Application

- All types of resistive, inductive and capacitive loads

Description

The VN5050J-E is a monolithic device made using STMicroelectronics VIPower technology. It is intended for driving resistive or inductive loads with one side connected to ground. Active V_{CC} pin voltage clamp protects the device against low energy spikes (see ISO7637 transient compatibility table). The device detects open load condition both in on and off state, when STAT_DIS is left open or driven low. Output shorted to V_{CC} is detected in the off state.

When STAT_DIS is driven high, the STATUS pin is in a high impedance condition.Output current limitation protects the device in overload condition. In case of long duration overload, the device limits the dissipated power to safe level up to thermal shut-down intervention.Thermal shut-down with automatic restart allows the device to recover normal operation as soon as fault condition disappears.

Table 1. Device summary

Package	Order codes	
	Tube	Tape & Reel
PowerSSO-12	VN5050J-E	VN5050JTR-E

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1 Block diagram and pin description

Figure 1. Block diagram

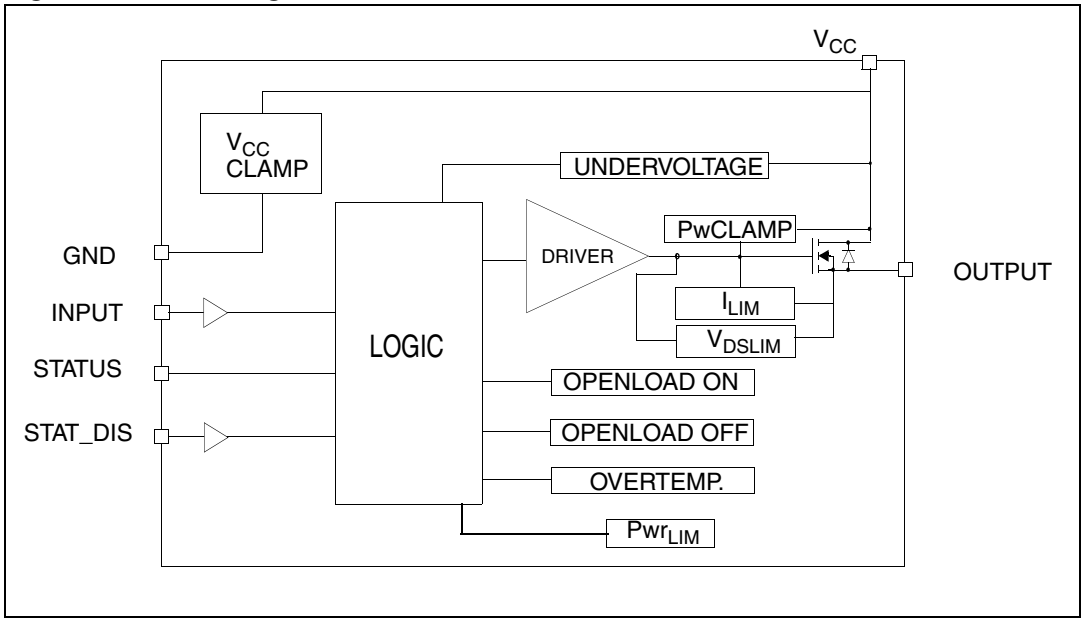
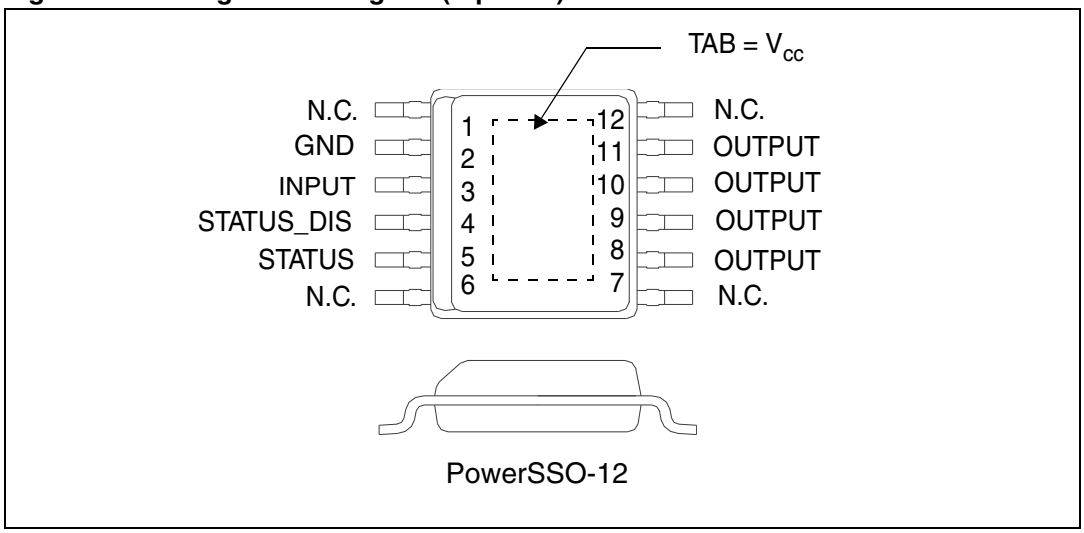


Table 2. Pin function

Name	Function
V_{CC}	Battery connection.
OUTPUT	Power output.
GND	Ground connection. Must be reverse battery protected by an external diode/resistor network.
INPUT	Voltage controlled input pin with hysteresis, CMOS compatible. Controls output switch state.
STATUS	Open drain digital diagnostic pin.
STAT_DIS	Active high CMOS compatible pin, to disable the STATUS pin.

Figure 2. Configuration diagram (top view)



Note: The above pin configuration reflects the changes notified with PCN-APG-BOD/07/2886. The new pinout is backaward compatible with existing PCB layouts where pins #1 and #6 are connected to Vcc and/or pins #7 and 12 are connected to OUTPUT. For new PCB designs, these pins should be left unconnected.

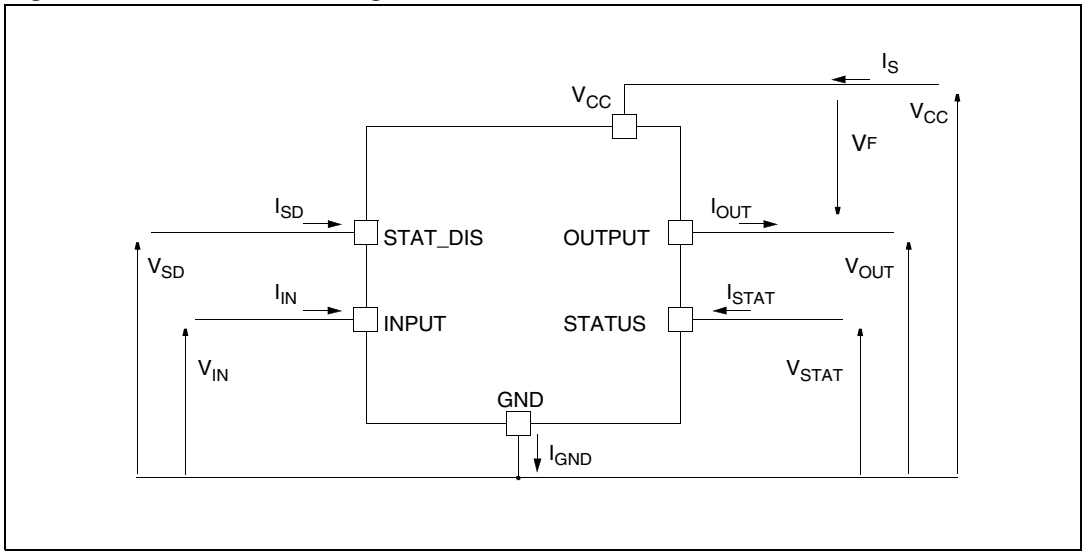
Table 3. Suggested connections for unused and N.C. pins

Connection / Pin	STATUS	N.C.	OUTPUT	INPUT	STAT_DIS
Floating	X	X	X	X	X
To ground	N.R.(1)	X	N.R.	Through 10KΩ resistor	Through 10KΩ resistor

(1) Not recommended.

2 Electrical specifications

Figure 3. Current and voltage conventions



Note: *$V_F = V_{OUT} - V_{CC}$ during reverse battery condition.*

2.1 Absolute maximum ratings

Stressing the device above the rating listed in the “Absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to the conditions in table below for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality document.

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	41	V
- V_{CC}	Reverse DC supply voltage	0.3	V
- I_{GND}	DC reverse ground pin current	200	mA
I_{OUT}	DC output current	Internally limited	A
- I_{OUT}	Reverse DC output current	12	A
I_{IN}	DC input current	+10 / -1	mA
I_{STAT}	DC status current	+10 / -1	mA
I_{STAT_DIS}	DC status disable current	+10 / -1	mA
E_{MAX}	Maximum switching energy (L=3mH; R_L=0Ω; V_{bat}=13.5V; T_{jstart}=150ºC; I_{OUT} = I_{limL}*(Typ.)*)	104	mJ

Table 4. Absolute maximum ratings (continued)

Symbol	Parameter	Value	Unit
V_{ESD}	Electrostatic discharge (Human Body Model: R=1.5KΩ; C=100pF)		
V_{ESD}	Charge device model (CDM-AEC-Q100-011)	750	V
T_j	Junction operating temperature	-40 to 150	°C
T_{stg}	Storage temperature	- 55 to 150	°C

2.2 Thermal data

Table 5. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case (Max.) (with one channel ON)	2.7	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient (Max.)	See *Figure 31*	°C/W

2.3 Electrical characteristics

Values specified in this section are for 8V<V_{CC}<36V; -40°C<T_j<150°C, unless otherwise specified.

Table 6. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		4.5	13	36	V
V_{USD}	Undervoltage shutdown			3.5	4.5	V
$V_{USDhyst}$	Undervoltage shut-down hysteresis			0.5		V
R_{ON}	On state resistance(2)	I_{OUT}=1A; T_j=25°C I_{OUT}=1A; T_j=150°C I_{OUT}=1A; V_{CC}=5V; T_j=25°C			50 100 65	mΩ mΩ mΩ
V_{clamp}	Clamp voltage	I_S=20mA	41	46	52	V
I_S	Supply current	Off State; V_{CC}=13V; T_j=25°C; V_{IN}=V_{OUT}=V_{SENSE}=V_{CSD}=0V On State; V_{CC}=13V; V_{IN}=5V; I_{OUT}=0A		2(1) 1.9	5(1) 3.5	µA mA
$I_{L(off1)}$	Off state output current(2)	V_{IN}=V_{OUT}=0V; V_{CC}=13V; T_j=25°C V_{IN}=V_{OUT}=0V; V_{CC}=13V; T_j=125°C	0 0	0.01	3 5	µA
$I_{L(off2)}$	Off state output current(2)	V_{IN}=0V; V_{OUT}=4V	-75		0	
V_F	Output - V_{CC} diode voltage(2)	-I_{OUT}=2A; T_j=150°C			0.7	V

(1) PowerMOS leakage included.

(2) For each channel.

Table 7. Switching (V_{CC} = 13V; T_j = 25°C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn- On delay time	R_L= 6.5Ω (see *Figure 5*)		20		µs
$t_{d(off)}$	Turn- Off delay time	R_L= 6.5Ω (see *Figure 5*)		35		µs
$dV_{OUT}/dt_{(on)}$	Turn- On voltage slope	R_L= 6.5Ω	See *Figure 21*			V/µs
$dV_{OUT}/dt_{(off)}$	Turn- Off voltage slope	R_L= 6.5Ω	See *Figure 23*			V/µs
W_{ON}	Switching energy losses during t_{won}	R_L= 6.5Ω (see *Figure 5*)		0.2		mJ
W_{OFF}	Switching energy losses during t_{woff}	R_L= 6.5Ω (see *Figure 5*)		0.2		mJ

Table 8. Status pin (V_{SD}=0V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{STAT}	Status low output voltage	I_{STAT}= 1.6 mA, V_{SD}=0V			0.5	V
I_{LSTAT}	Status leakage current	Normal Operation or V_{SD}=5V, V_{STAT}= 5V			10	µA
C_{STAT}	Status pin input capacitance	Normal Operation or V_{SD}=5V, V_{STAT}= 5V			100	pF
V_{SCL}	Status clamp voltage	I_{STAT}= 1mA I_{STAT}= -1mA	5.5	 -0.7	7	V V

Table 9. Protections (1)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{limH}	DC short circuit current	V_{CC}= 13V 5V<V_{CC}<36V	13.5	19	26.5 26.5	A A
I_{limL}	Short circuit current during thermal cycling	V_{CC}= 13V T_R<T_j<T_{TSD}		7		A
T_{TSD}	Shutdown temperature		150	175	200	°C
T_R	Reset temperature		T_{RS} + 1	T_{RS} + 5		°C
T_{RS}	Thermal reset of STATUS		135			°C
T_{HYST}	Thermal hysteresis (T_{TSD}-T_R)			7		°C
t_{SDL}	Status delay in overload conditions	T_j>T_{TSD} (see *Figure 4*)			20	µs
V_{DEMAG}	Turn-Off output voltage clamp	I_{OUT}=2A; V_{IN}=0; L=6mH	V_{CC}-41	V_{CC}-46	V_{CC}-52	V
V_{ON}	Output voltage drop limitation	I_{OUT} = 0.1A; T_j= -40°C...+150°C (see *Figure 6*)		25		mV

(1) To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles.

Table 10. Openload detection

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{OL}	Openload On State detection threshold	V_{IN} = 5V ,8V<V_{CC}<18V	10	See *Figure 18*	50	mA
$t_{DOL(on)}$	Openload On State detection delay	I_{OUT} = 0A, V_{CC}=13V (see *Figure 4*)			200	µs
t_{POL}	Delay between INPUT falling edge and STATUS rising edge in Openload condition	I_{OUT} = 0A (see *Figure 4*)	200	500	1000	µs
V_{OL}	Openload Off State voltage detection threshold	V_{IN} = 0V, 8V<V_{CC}<16V	2	See *Figure 19*	4	V
t_{DSTKON}	Output short circuit to V_{CC} detection delay at turn Off	See *Figure 4*	180		t_{POL}	µs

Table 11. Logic input

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input low level				0.9	V
I_{IL}	Low level Input current	V_{IN} =0.9 V	1			µA
V_{IH}	Input high level		2.1			V
I_{IH}	High level Input current	V_{IN} = 2.1 V			10	µA
$V_{I(hyst)}$	Input hysteresis voltage		0.25			V
V_{ICL}	Input clamp voltage	I_{IN} = 1mA I_{IN} = -1mA	5.5	 -0.7	7	V V
V_{SDL}	STAT_DIS low level voltage				0.9	V
I_{SDL}	Low level STAT_DIS current	V_{SD} = 0.9 V	1			µA
V_{SDH}	STAT_DIS high level voltage		2.1			V
I_{SDH}	High level STAT_DIS current	V_{SD} = 2.1 V			10	µA
$V_{SD(hyst)}$	STAT_DIS hysteresis voltage		0.25			V
V_{SDCL}	STAT_DIS clamp voltage	I_{SD}=1mA I_{SD}=-1mA	5.5	 -0.7	7	V V

Figure 4. Status timings

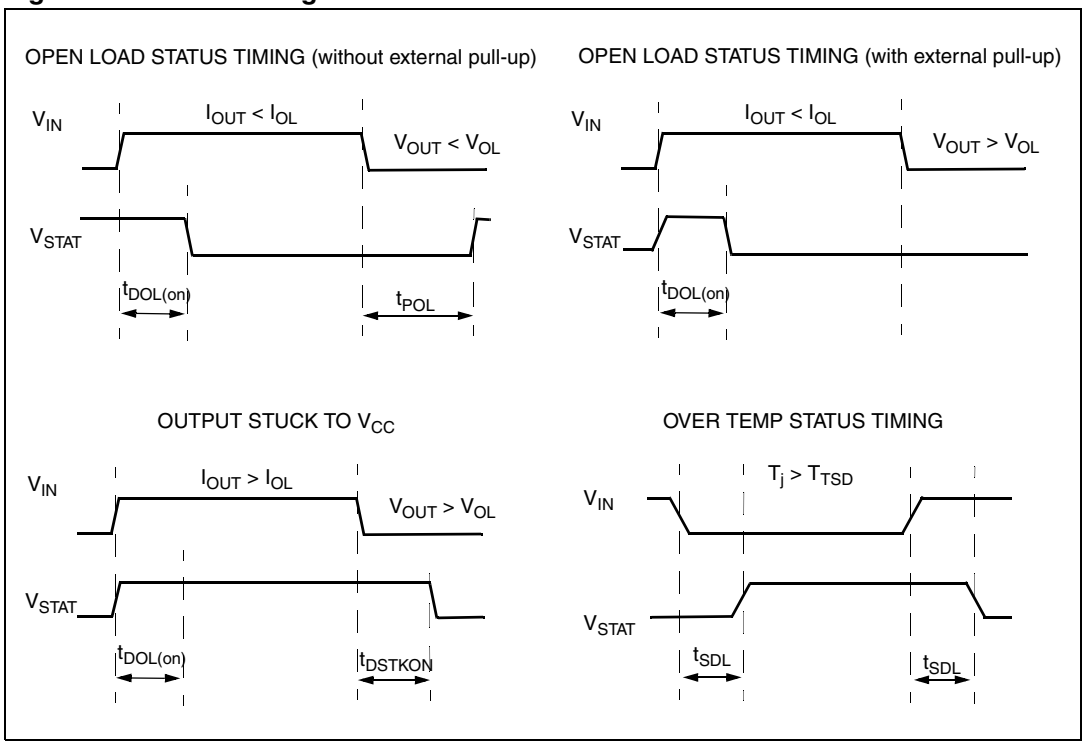


Table 12. Truth table

Conditions	INPUT	OUTPUT	STATUS (V_{SD}=0V)(1)
Normal operation	L H	L H	H H
Current limitation	L H	L X	H H
Overtemperature	L H	L L	H L
Undervoltage	L H	L L	X X
Output voltage > V_{OL}	L H	H H	Lv H
Output current < I_{OL}	L H	L H	H(2) L

(1) If the V_{SD} is high, the STATUS pin is in a high impedance.

(2) The STATUS pin becomes high with a delay equal to t_{POL} after INPUT falling edge.

Figure 5. Switching characteristics

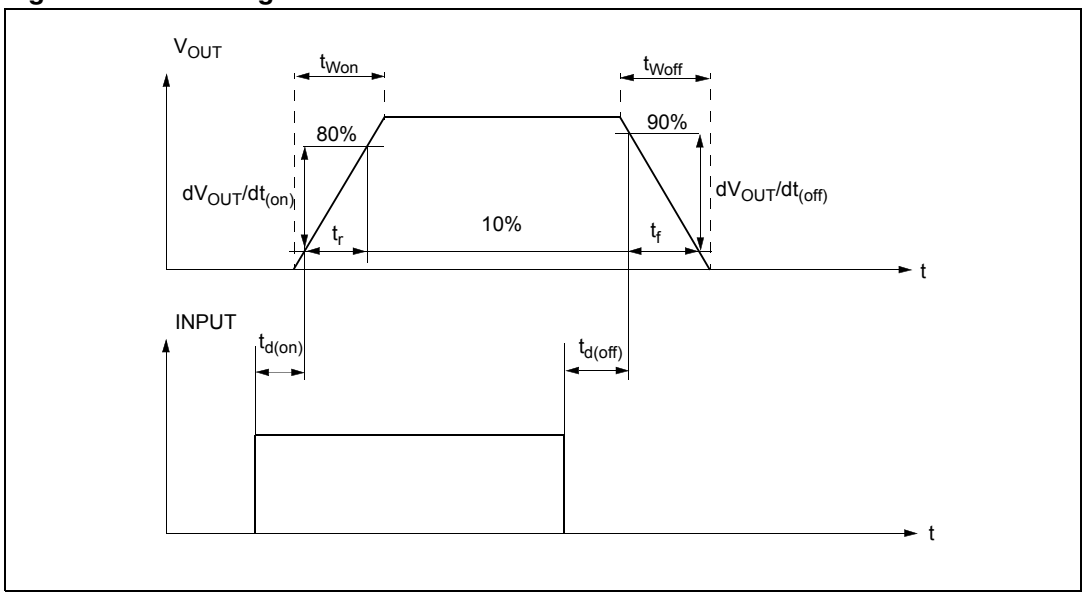


Figure 6. Output voltage drop limitation

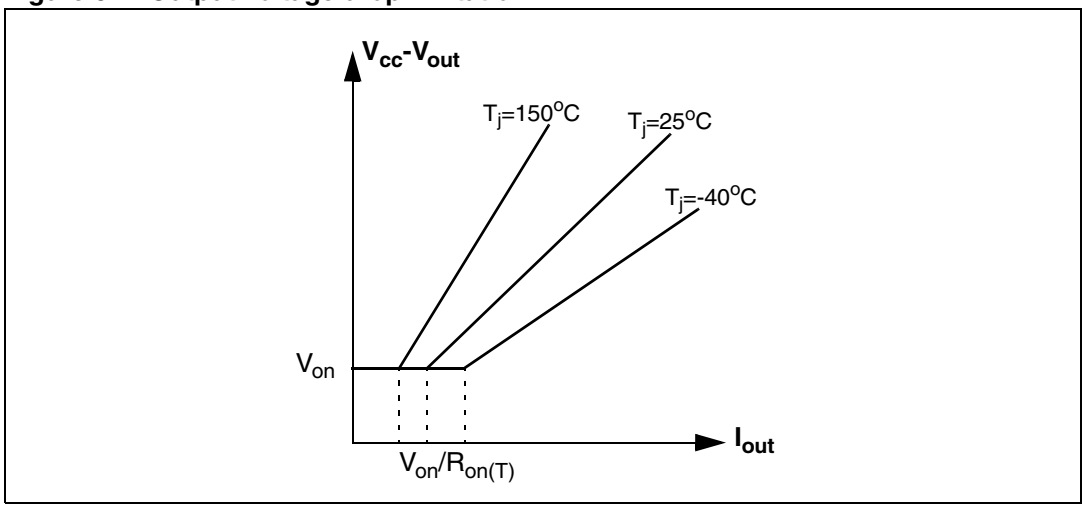


Table 13. Electrical transient requirements

ISO 7637-2: 2004(E) Test pulse	Test levels		Number of pulses or test times	Burst cycle/pulse repetition time		Delays and Impedance
	III	IV				
1	-75V	-100V	5000 pulses	0.5 s	5 s	2 ms, 10 Ω
2a	+37V	+50V	5000 pulses	0.2 s	5 s	50 µs, 2 Ω
3a	-100V	-150V	1h	90 ms	100 ms	0.1 µs, 50 Ω
3b	+75V	+100V	1h	90 ms	100 ms	0.1 µs, 50 Ω
4	-6V	-7V	1 pulse			100 ms, 0.01Ω
5b(2)	+65V	+87V	1 pulse			400 ms, 2 Ω

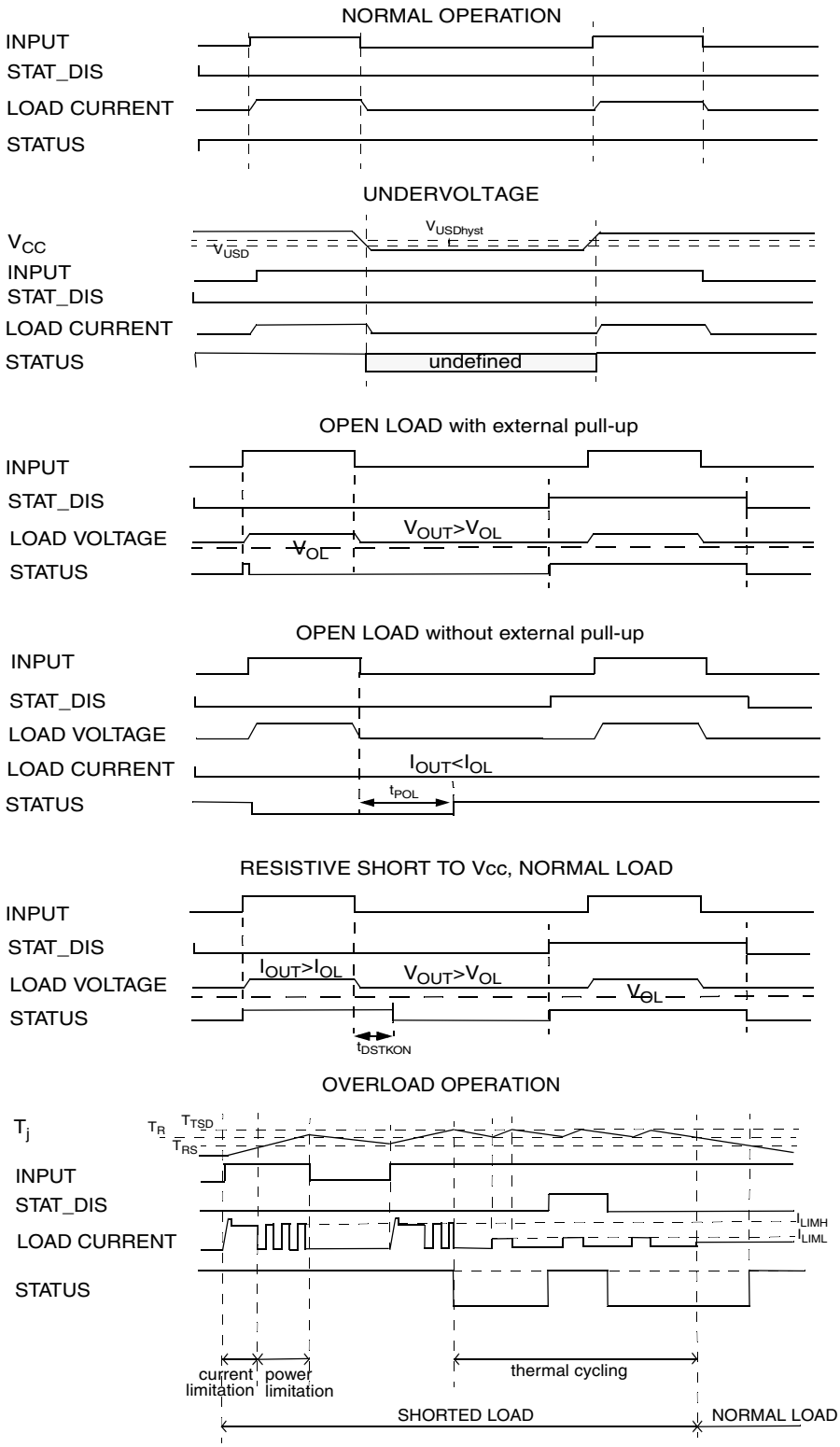
ISO 7637-2: 2004(E) Test pulse	Test level results(1)	
	III	IV
1	C	C
2a	C	C
3a	C	C
3b	C	C
4	C	C
5b(2)	C	C

(1) The above test levels must be considered referred to V_{CC} = 13.5V except for pulse 5b.

(2) Valid in case of external load dump clamp: 40V maximum referred to ground.

Class	Contents
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device are not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

Figure 7. Waveforms



2.4 Electrical characteristics curves

Figure 8. Off state output current

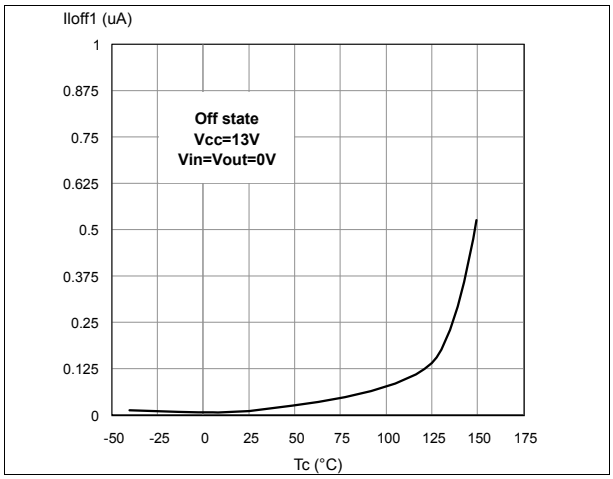


Figure 9. High level input current

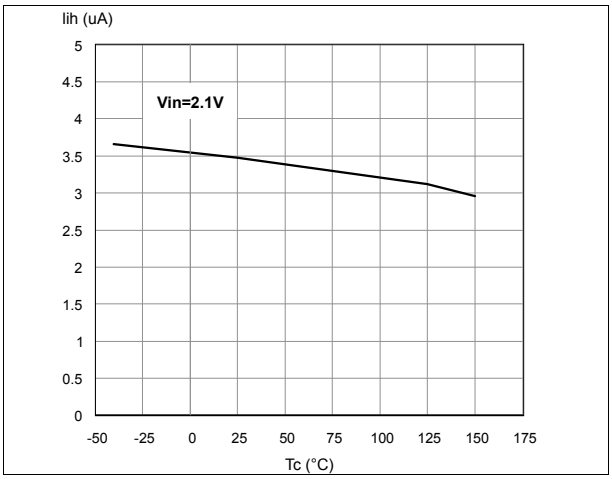


Figure 10. Input clamp voltage

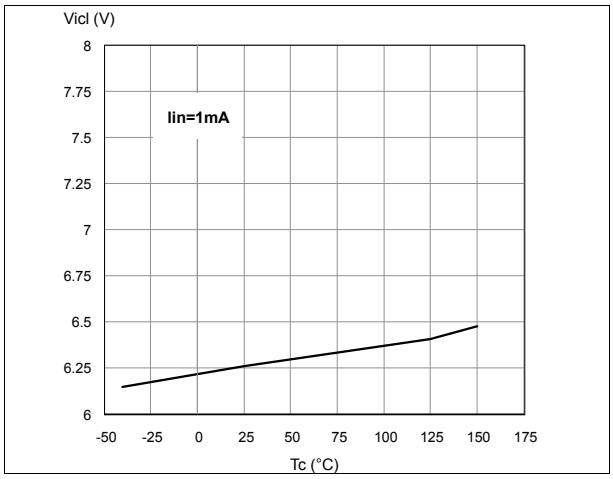


Figure 11. Input high level

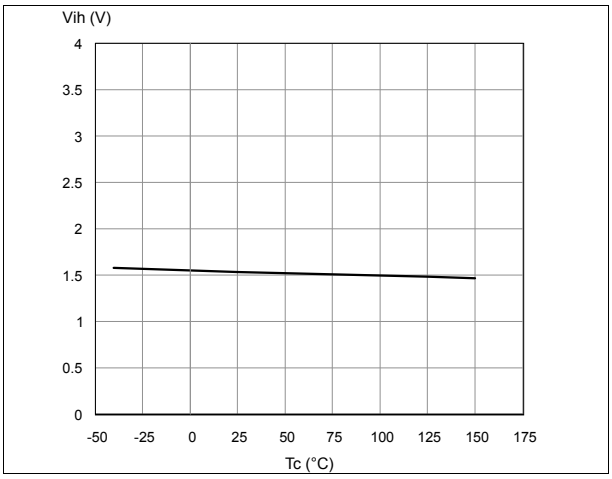


Figure 12. Input low level

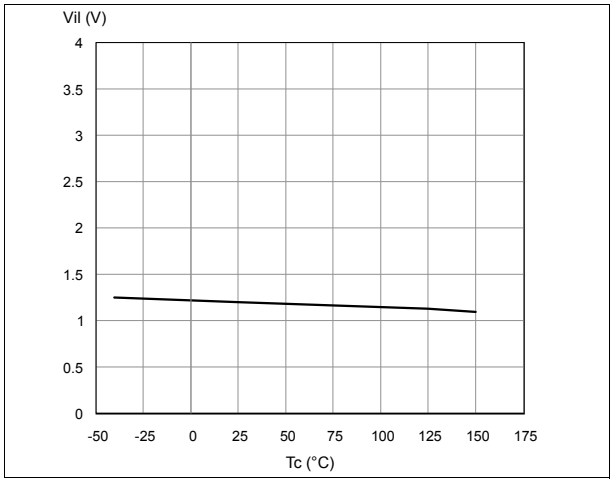


Figure 13. Input hysteresis voltage

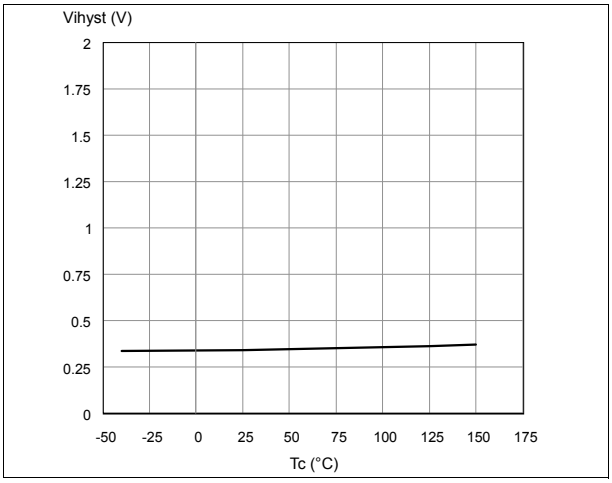
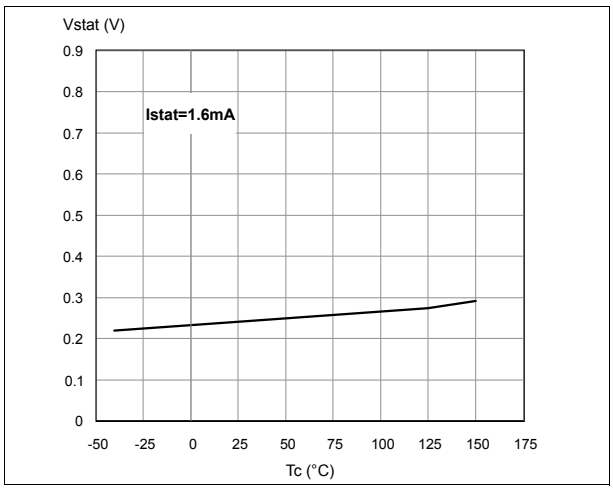


Figure 14. Status low output voltage



On state resistance vs T_{case}

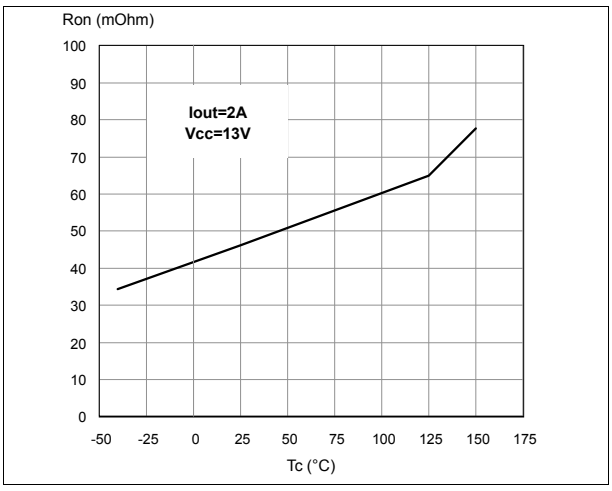


Figure 15. Status leakage current

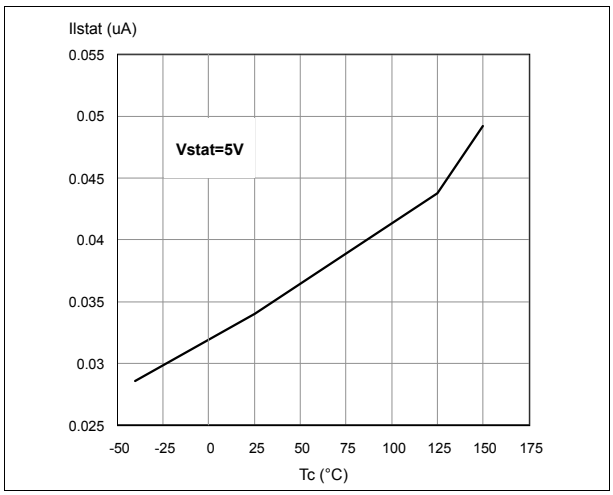


Figure 16. On state resistance vs V_{CC}

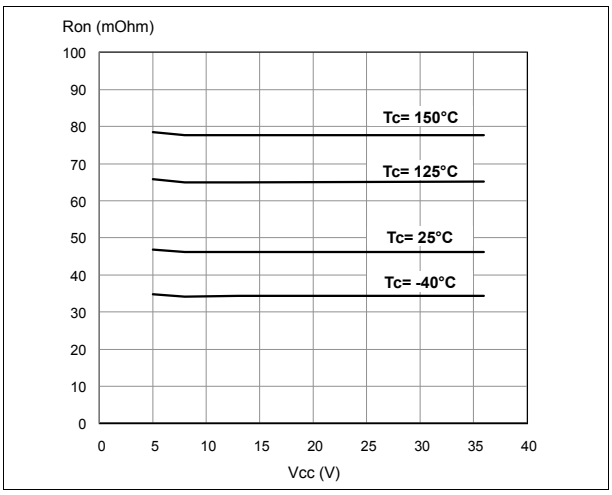


Figure 17. Status clamp voltage

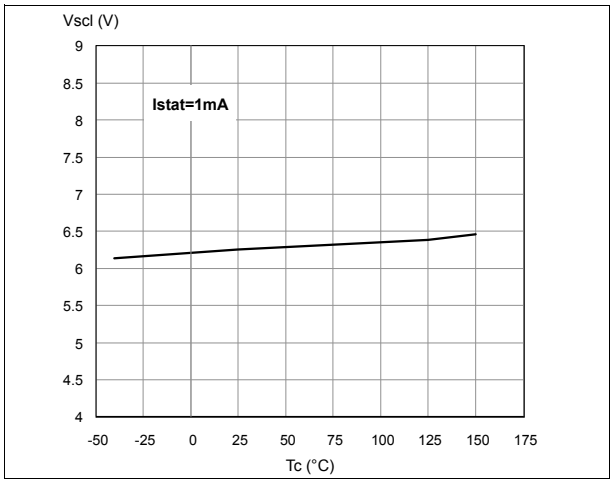


Figure 18. Openload On state detection threshold

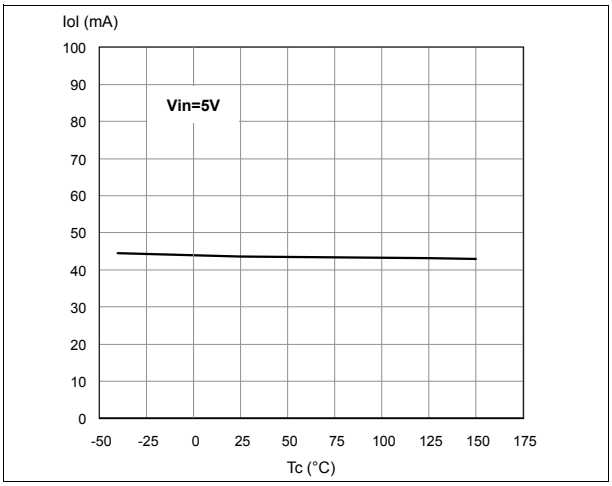


Figure 19. Openload Off state voltage detection threshold

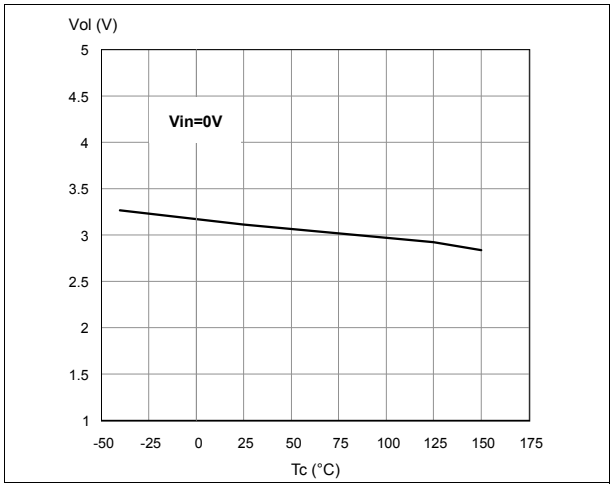


Figure 20. I_{LIM} vs T_{case}

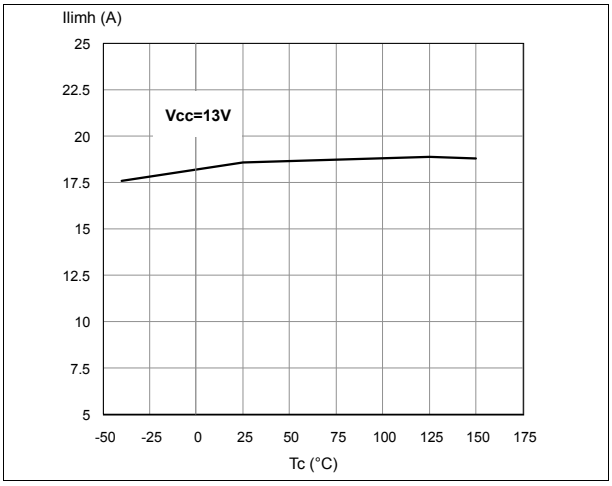


Figure 21. Turn-On voltage slope

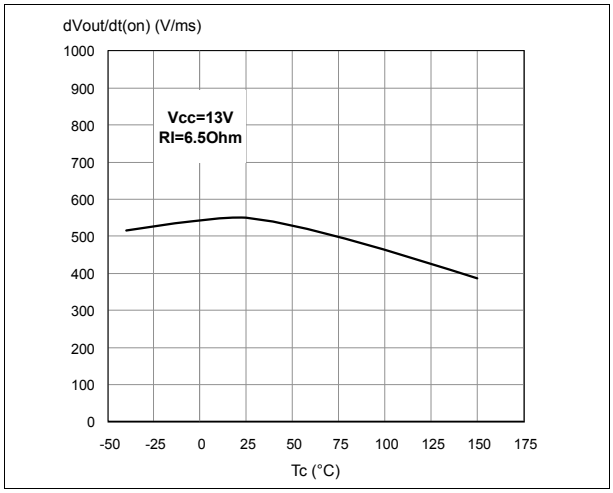


Figure 22. Undervoltage shutdown

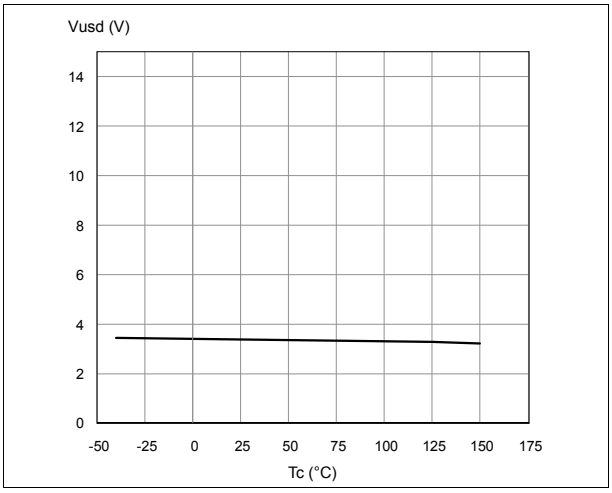


Figure 23. Turn-Off voltage slope

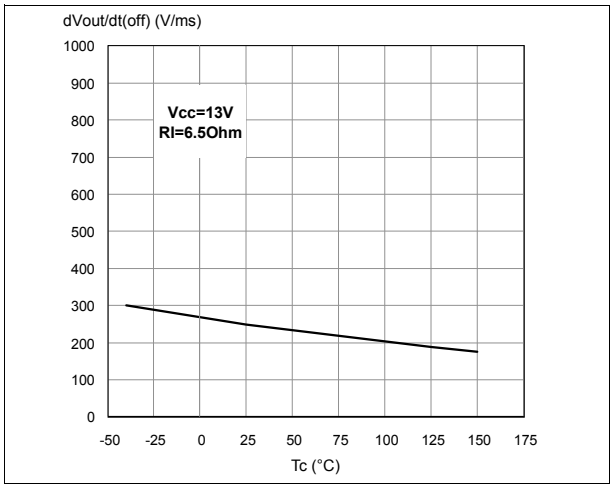


Figure 24. STAT_DIS clamp voltage

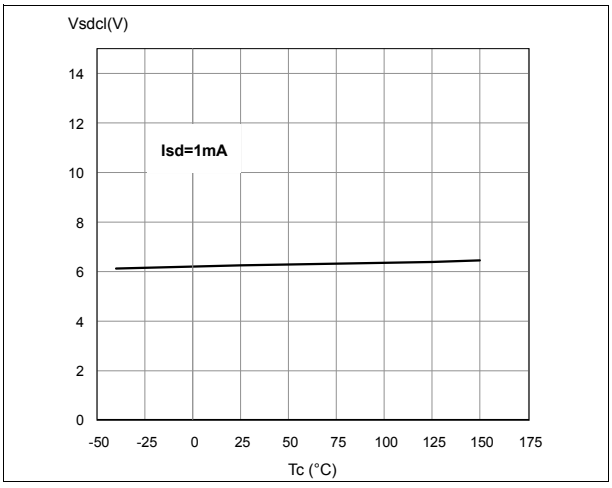


Figure 25. High level STAT_DIS voltage

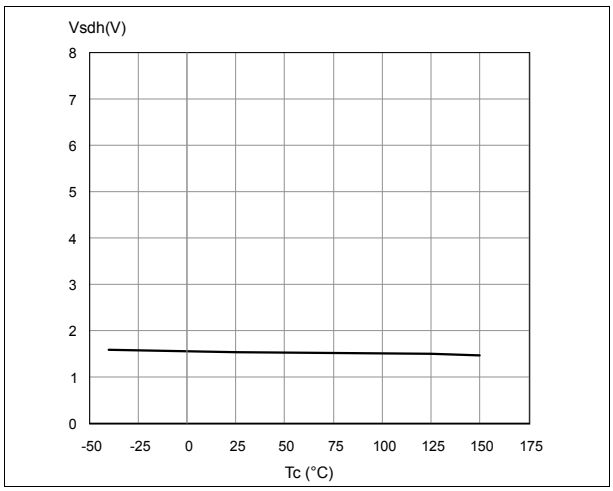
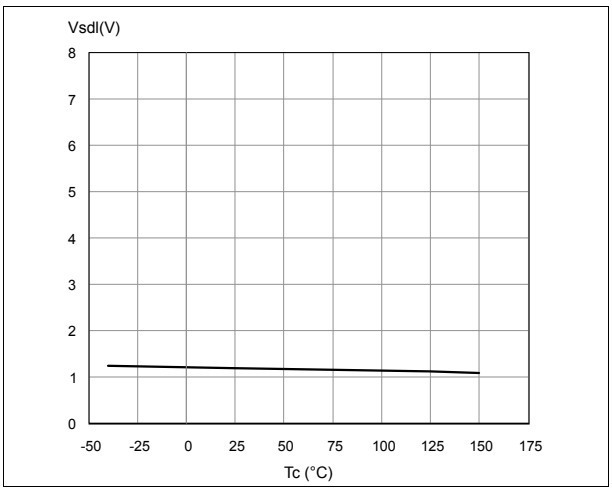
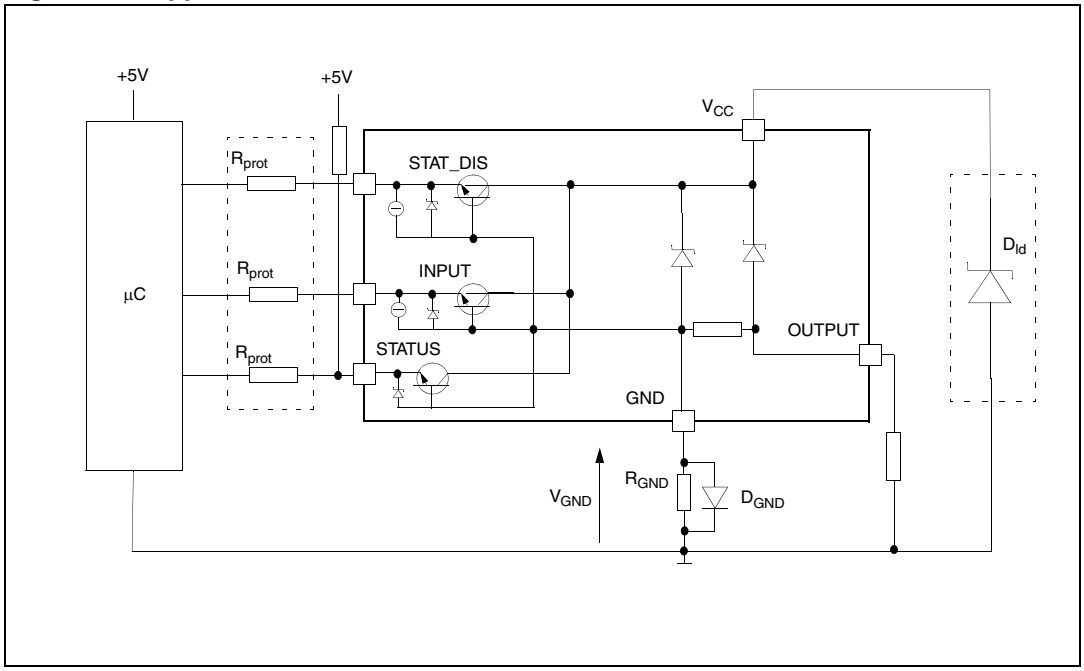


Figure 26. Low level STAT_DIS voltage



3 Application information

Figure 27. Application schematic



3.1 GND protection network against reverse battery

3.1.1 Solution 1: resistor in the ground line (R_{GND} only)

This can be used with any type of load.

The following is an indication on how to dimension the R_{GND} resistor.

1. $R_{GND} \leq 600mV / (I_{S(on)max})$.
2. $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where $-I_{GND}$ is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device datasheet.

Power Dissipation in R_{GND} (when V_{CC}<0: during reverse battery situations) is:

$P_D= (-V_{CC})^2/R_{GND}$

This resistor can be shared amongst several different HSDs. Please note that the value of this resistor should be calculated with formula (1) where $I_{S(on)max}$ becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not shared by the device ground then the R_{GND} will produce a shift ($I_{S(on)max}$ * R_{GND}) in the input thresholds and the status output values. This shift will vary depending on how many devices are ON in the case of several high side drivers sharing the same R_{GND}.

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then ST suggests to utilize Solution 2 (see below).

3.1.2 Solution 2: diode (D_{GND}) in the ground line

A resistor (R_{GND}=1kΩ) should be inserted in parallel to D_{GND} if the device drives an inductive load.

This small signal diode can be safely shared amongst several different HSDs. Also in this case, the presence of the ground network will produce a shift (≈600mV) in the input threshold and in the status output values if the microprocessor ground is not common to the device ground. This shift will not vary if more than one HSD shares the same diode/resistor network.

3.2 Load dump protection

D_{ld} is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds the V_{CC} max DC rating. The same applies if the device is subject to transients on the V_{CC} line that are greater than the ones shown in the ISO 7637-2: 2004(E) table.

3.3 MCU I/Os protection

If a ground protection network is used and negative transient are present on the V_{CC} line, the control pins will be pulled negative. ST suggests to insert a resistor (R_{prot}) in line to prevent the µC I/Os pins to latch-up.

The value of these resistors is a compromise between the leakage current of µC and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of µC I/Os.

$-V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C}-V_{IH}-V_{GND}) / I_{IHmax}$

Calculation example:

For V_{CCpeak}= - 100V and $I_{latchup} \geq$ 20mA; $V_{OH\mu C} \geq$ 4.5V

5kΩ ≤ R_{prot} ≤ 180kΩ.

Recommended values: R_{prot} =10kΩ .

3.4 Open load detection in Off state

Off state open load detection requires an external pull-up resistor (R_{PU}) connected between OUTPUT pin and a positive supply voltage (V_{PU}) like the +5V line used to supply the microprocessor.

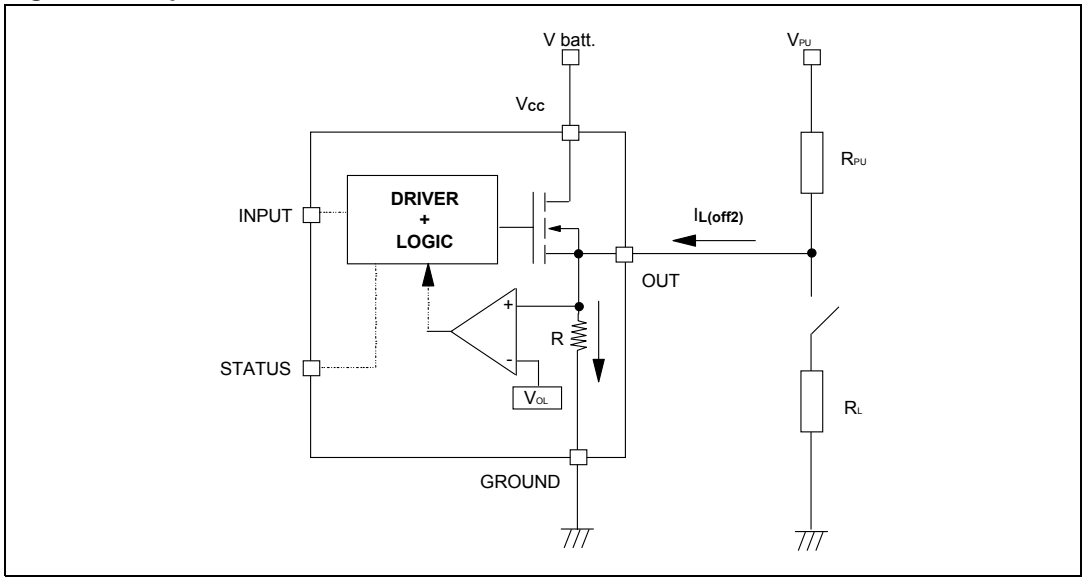
The external resistor has to be selected according to the following requirements:

1. no false open load indication when load is connected: in this case we have to avoid V_{OUT} to be higher than V_{Olmin}; this results in the following condition $V_{OUT}=(V_{PU}/(R_L+R_{PU}))R_L<V_{Olmin}$.
2. no misdetection when load is disconnected: in this case the V_{OUT} has to be higher than V_{OLmax}; this results in the following condition $R_{PU}<(V_{PU}–V_{OLmax})/I_{L(off2)}$.

Because $I_{s(OFF)}$ may significantly increase if V_{out} is pulled high (up to several mA), the pull-up resistor R_{PU} should be connected to a supply that is switched OFF when the module is in standby.

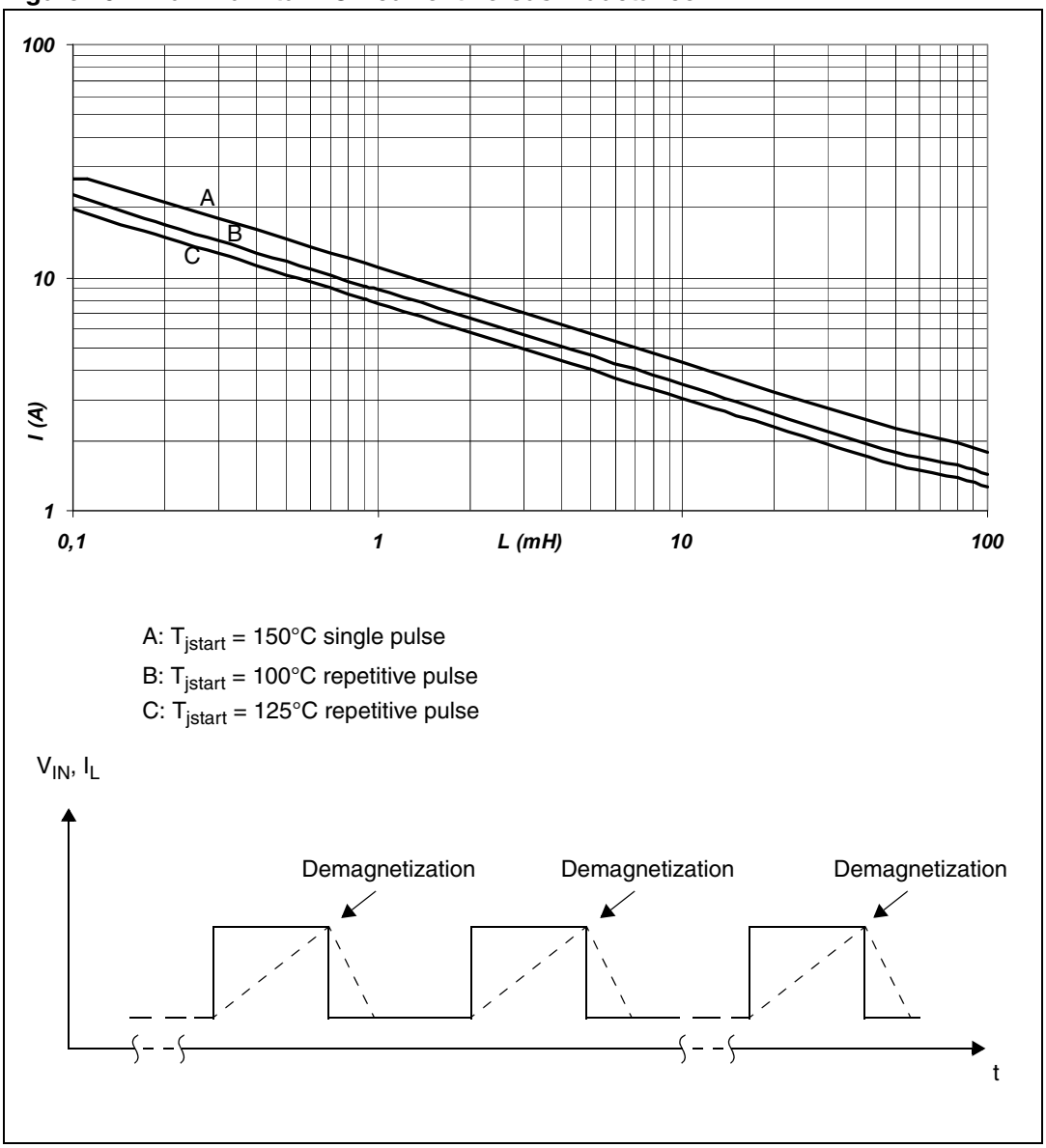
The values of V_{OLmin}, V_{OLmax} and $I_{L(off2)}$ are available in the Electrical characteristics section.

Figure 28. Open load detection in Off state



3.5 Maximum demagnetization energy (V_{CC} = 13.5V)

Figure 29. Maximum turn Off current versus inductance

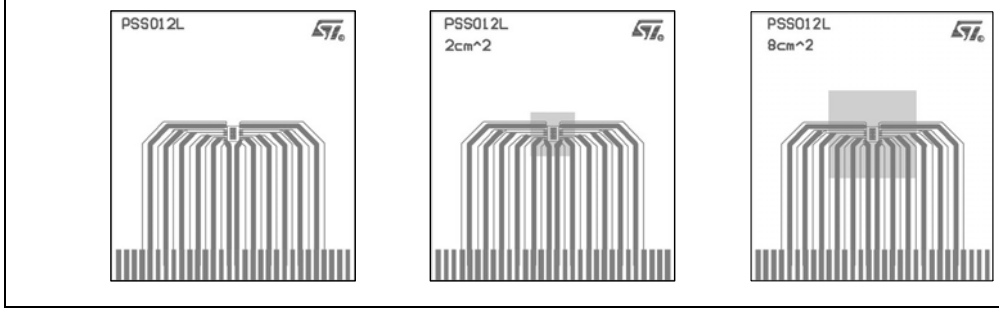


Note: Values are generated with R_L =0 Ω.In case of repetitive pulses, T_{jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

4 Package and PCB thermal data

4.1 PowerSSO-12™ thermal data

Figure 30. PowerSSO-12™ PC Board



Note: Layout condition of R_{th} and Z_{th} measurements (PCB: Double layer, Thermal Vias, FR4 area= 77mm x 86mm,PCB thickness=1.6mm, Cu thickness=70 µm (front and back side), Copper areas: from minimum pad lay-out to 8cm^2).

Figure 31. $R_{thj\text{-}amb}$ Vs. PCB copper area in open box free air condition

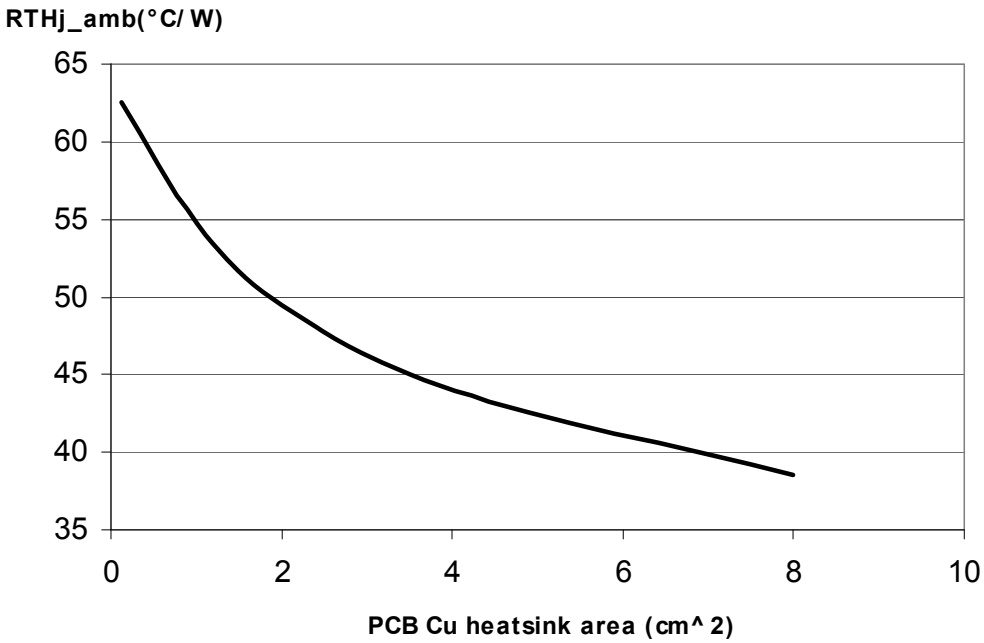
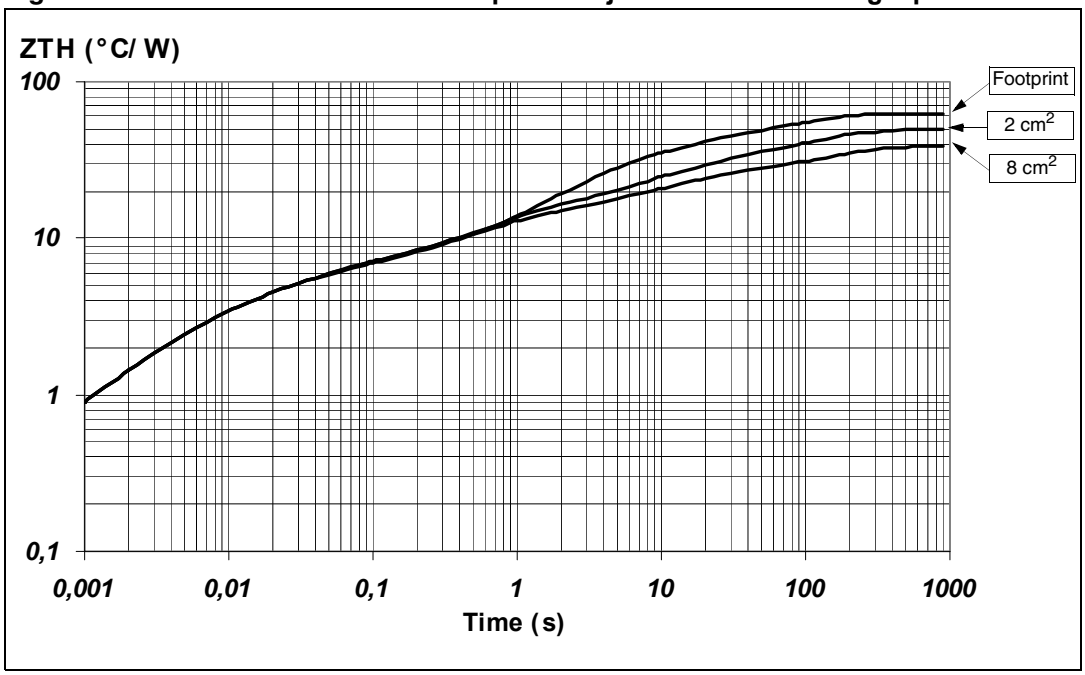


Figure 32. PowerSSO-12™ thermal impedance junction ambient single pulse

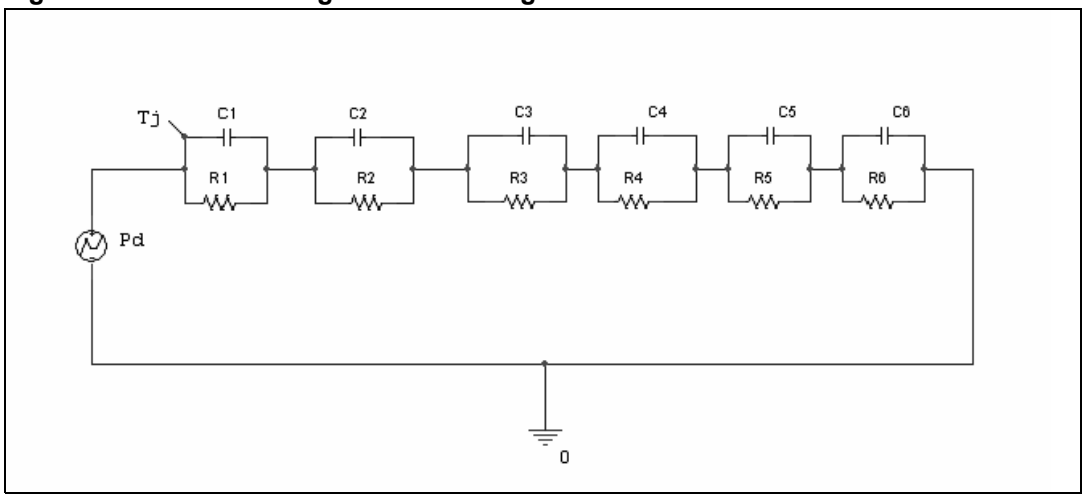


Equation 1: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_P/T$

Figure 33. Thermal fitting model of a single channel HSD in PowerSSO-12™ (a)



(a)The fitting model is a semplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Table 14. Thermal parameter

Area/island (cm^2)	Footprint	2	8
R1 (°C/W)	0.7		
R2 (°C/W)	2.8		
R3 (°C/W)	3		
R4 (°C/W)	8	8	7
R5 (°C/W)	22	15	10
R6 (°C/W)	26	20	15
C1 (W.s/°C)	0.001		
C2 (W.s/°C)	0.0025		
C3 (W.s/°C)	0.0166		
C4 (W.s/°C)	0.2	0.1	0.1
C5 (W.s/°C)	0.27	0.8	1
C6 (W.s/°C)	3	6	9

5 Package and packing information

5.1 ECOPACK® packages

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second-level interconnect. The category of Second-Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97.
The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

5.2 Package mechanical data

Figure 34. PowerSSO-12™ package dimensions

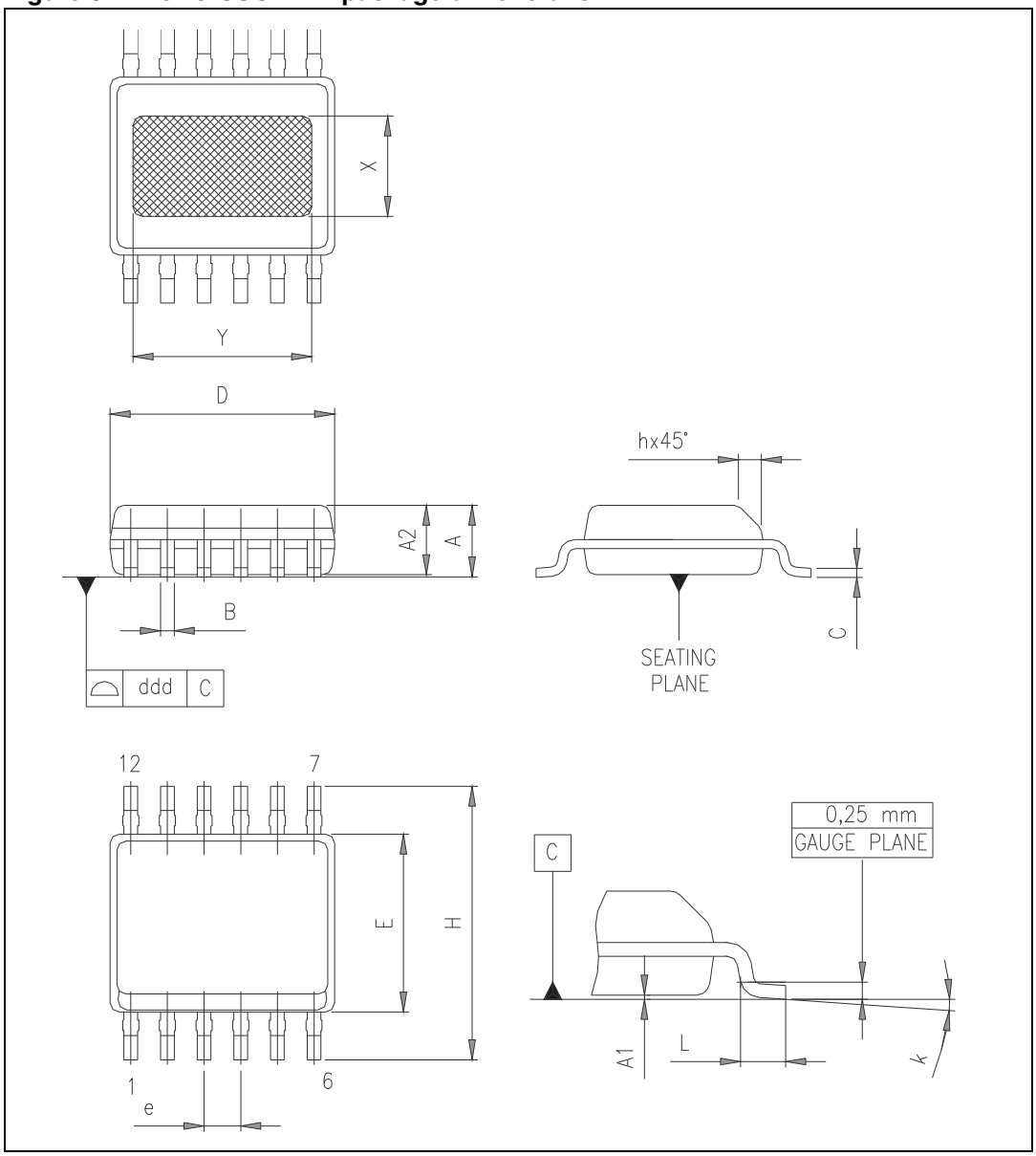
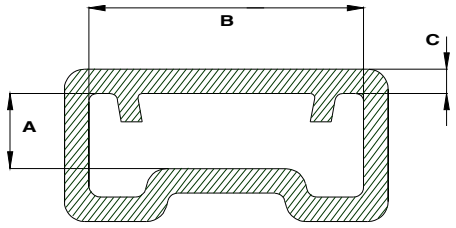


Table 15. PowerSSO-12™ mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A	1.250		1.620
A1	0.000		0.100
A2	1.100		1.650
B	0.230		0.410
C	0.190		0.250
D	4.800		5.000
E	3.800		4.000
e		0.800	
H	5.800		6.200
h	0.250		0.500
L	0.400		1.270
k	0°		8°
X	2.200		2.800
Y	2.900		3.500
ddd			0.100

5.3 Packing information

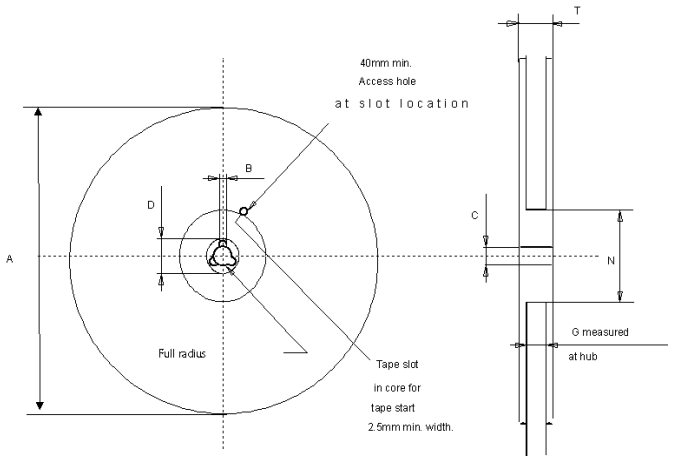
Figure 35. PowerSSO-12™ tube shipment (no suffix)



Base Q.ty	100
Bulk Q.ty	2000
Tube length (± 0.5)	532
A	1.85
B	6.75
C (± 0.1)	0.6

All dimensions are in mm.

Figure 36. PowerSSO-12™ tape and reel shipment (suffix "TR")



REEL DIMENSIONS

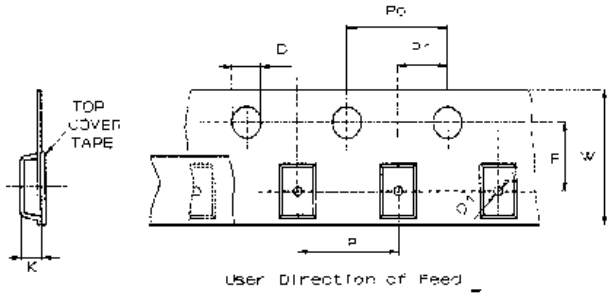
Base Q.ty	2500
Bulk Q.ty	2500
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	12.4
N (min)	60
T (max)	18.4

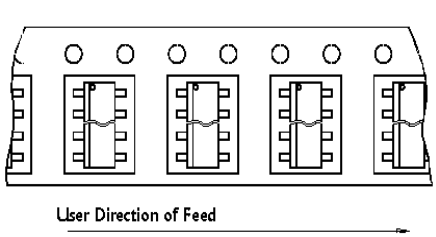
TAPE DIMENSIONS

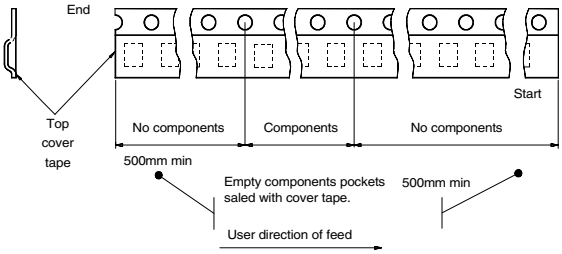
According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb. 1986

Tape width	W	12
Tape Hole Spacing	P0 (± 0.1)	4
Component Spacing	P	8
Hole Diameter	D (± 0.05)	1.5
Hole Diameter	D1 (min)	1.5
Hole Position	F (± 0.1)	5.5
Compartment Depth	K (max)	4.5
Hole Spacing	P1 (± 0.1)	2

All dimensions are in mm.







6 Revision history

Table 16. Document revision history

Date	Revision	Changes
30-Mar-2006	1	Initial release.
13-Sep-2007	2	Document reformatted and restructured. Contents and lists of tables and figures added. *Figure 2: Configuration diagram (top view)* updated: pins 1-6-7-12 N.C. (not connected). *Table 4: Absolute maximum ratings*: EMAX entries updated. *Table 13: Electrical transient requirements* :Test level values III and IV for test pulse 5b and notes updated. *Section 3.5: Maximum demagnetization energy (VCC = 13.5V)* added. *Figure 33: Thermal fitting model of a single channel HSD in PowerSSO-12™* : note added *Table 15: PowerSSO-12™ mechanical data* : slug dimensions (X,Y) corrected
10-Dec-2007	3	*Figure 2: Configuration diagram (top view)*: added note. Updated *Section 4.1: PowerSSO-12™ thermal data*: – changed *Figure 31: Rthj-amb Vs. PCB copper area in open box free air condition*. – changed *Figure 32: PowerSSO-12™ thermal impedance junction ambient single pulse*. – updated *Table 14: Thermal parameter*. R1 value changed from 0.6 to 0.7 °C/W. R3 value changed from 6.5 to 3 °C/W. R4 values changed from 10 /10 /9 to 8 /8 /7 °C/W. C3 value changed from 0.022 to 0.0166 W.s/°C.
25-Sep-2013	4	Updated disclaimer.

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