ESDALC6V1-1M2

Single line low capacitance Transil™, transient surge voltage suppressor (TVS) for ESD protection

Datasheet – production data

Features

- Single line low capacitance Transil diode
- Unidirectional ESD protection
- ESD protection > 30 kV (IEC 61000-4-2 contact discharge)
- Breakdown voltage V_{BR} = 6.1 V min.
- Low diode capacitance (22 pF @ 0 V)
- Low leakage current (< 100 nA @ 3 V)
- Very small PCB area (0.6 mm^2)
- RoHS compliant

Benefits

- High ESD robustness of the equipment
- Suitable for high density boards

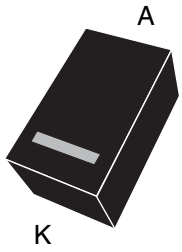
Complies with the following standards:

- IEC 61000-4-2 level 4:
  - 15 kV (air discharge)
  - 8 kV (contact discharge)
- MIL STD 883G - Method 3015-7: class 3B
  - HBM (Human body model)

Applications

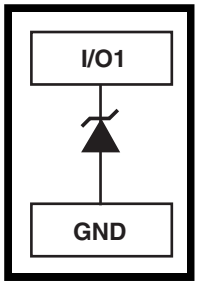
Where transient overvoltage protection in ESD sensitive equipment is required, such as:

- Computers
- Printers
- Communication systems
- Cellular phone handsets and accessories
- Video equipment



SOD882

Figure 1. Functional diagram



Description

The ESDALC6V1-1M2 is a unidirectional single line TVS diode designed to protect the data lines or other I/O ports against ESD transients.

The device is ideal for applications where both reduced line capacitance and board space saving are required.

TM: Transil is a trademark of STMicroelectronics

This is information on a product in full production. www.st.com

1 Characteristics

Table 1. Absolute maximum ratings (T_{amb} = 25 °C)

Symbol	Parameter		Value	Unit
V_{PP}	Peak pulse voltage - IEC 61000-4-2 contact discharge		±30	kV
P_{PP}	Peak pulse power dissipation (8/20 µs) (1)	$T_{j\ initial} = T_{amb}$	50	W
I_{PP}	Peak pulse current (8/20 µs)		6	A
T_j	Operating junction temperature range		-40 to +125	°C
T_{stg}	Storage temperature range		- 55 to +150	°C
T_L	Maximum lead temperature for soldering during 10 s at 5 mm for case		260	°C

1. For a surge greater than the maximum values, the diode will fail in short-circuit

Figure 2. Electrical characteristics (definitions)

Symbol		Parameter
V_{BR}	=	Breakdown voltage
I_{RM}	=	Leakage current @ V_{RM}
V_{RM}	=	Stand-off voltage
V_{CL}	=	Clamping voltage
R_d	=	Dynamic impedance
I_{PP}	=	Peak pulse current
I_R	=	Breakdown current
αT	=	Voltage temperature coefficient
V_F	=	Forward voltage drop

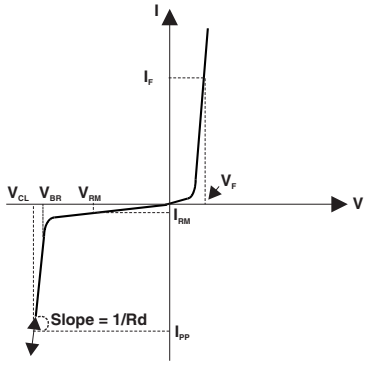


Table 2. Electrical characteristics (T_{amb} = 25 °C)

Order code	V_{BR} @ I_R			I_{RM} @ V_{RM}		V_F @ 10 mA	αT	C @ 0 V
	V min.	V max.	mA	nA max.	V	V	10-4/°C max.	pF typ.
ESDALC6V1-1M2	6.1	7.2	1	100	3	1	4.5	22

Figure 3. Peak pulse power dissipation versus initial junction temperature

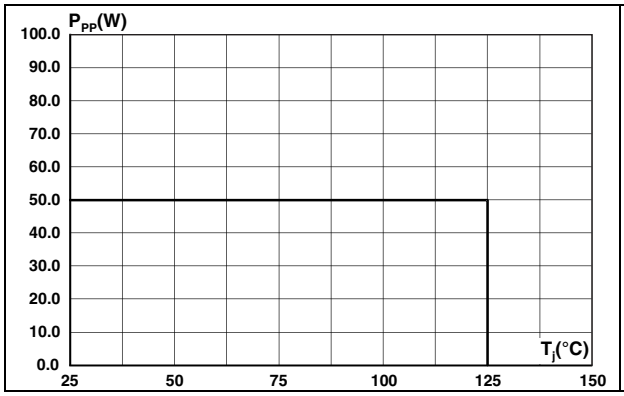


Figure 4. Peak pulse power versus exponential pulse duration

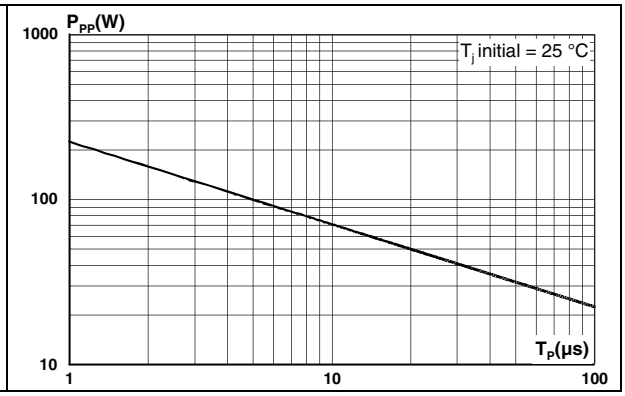


Figure 5. Clamping voltage versus peak pulse current (typical values)

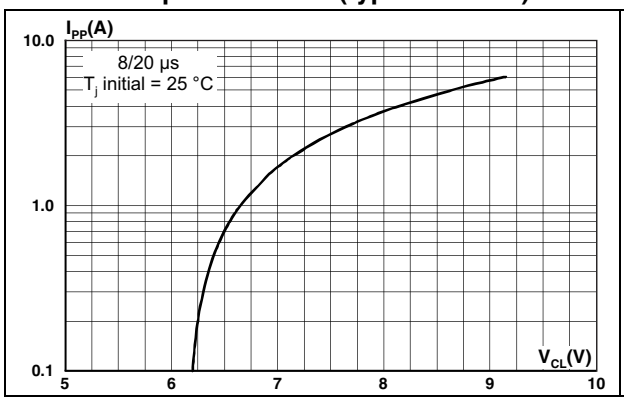


Figure 6. Forward voltage drop versus peak forward current (typical values)

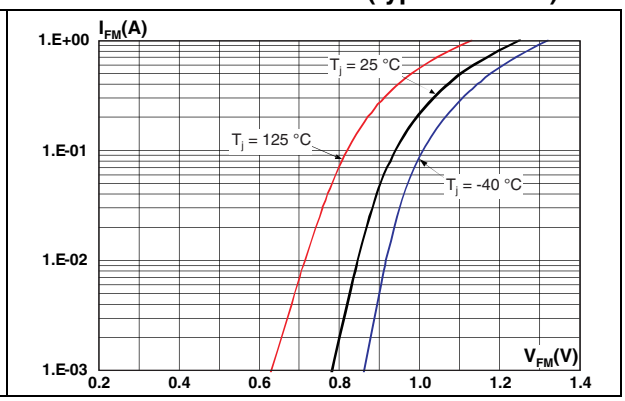


Figure 7. Junction capacitance versus reverse voltage applied (typical values)

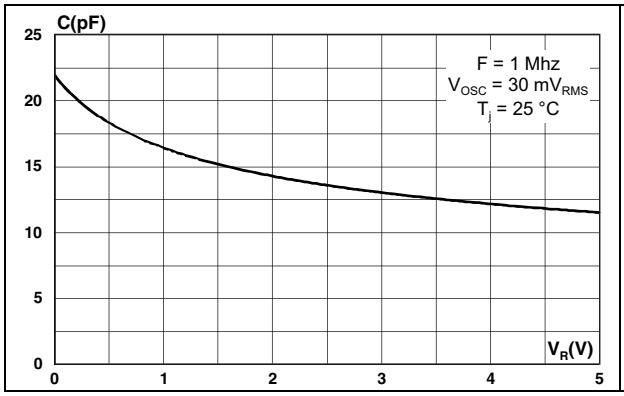


Figure 8. Leakage current versus junction temperature (typical values)

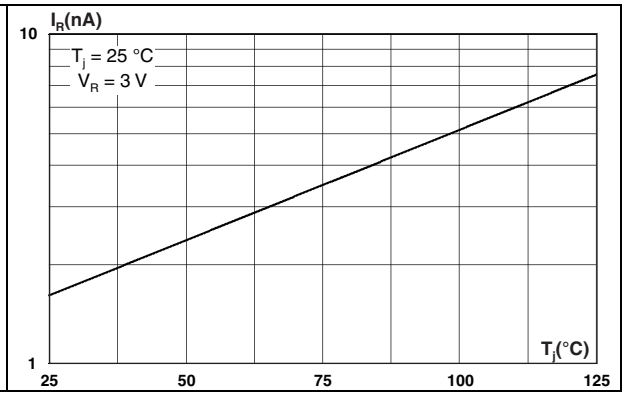


Figure 9. ESD response to IEC 61000-4-2 (+15 kV air discharge) on each channel

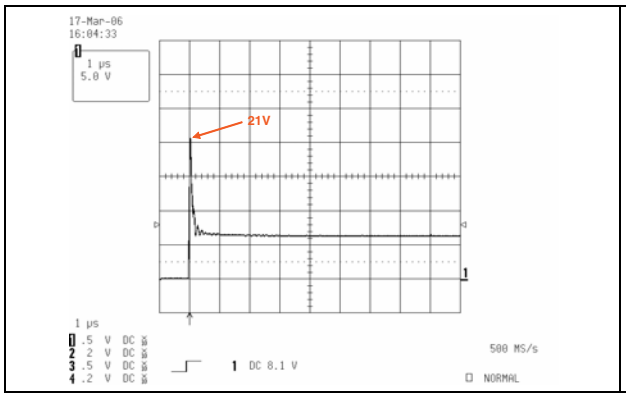


Figure 10. ESD response to IEC 61000-4-2 (-15 kV air discharge) on each channel

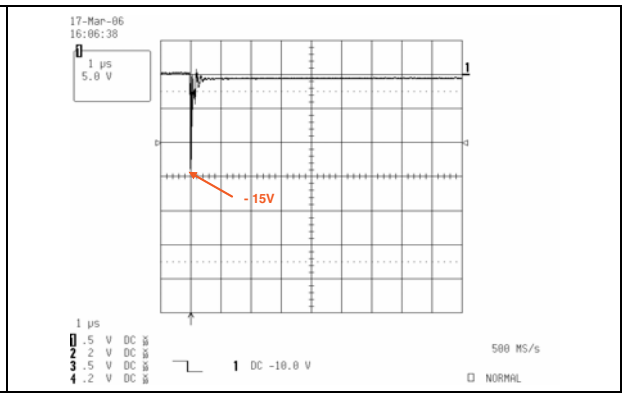
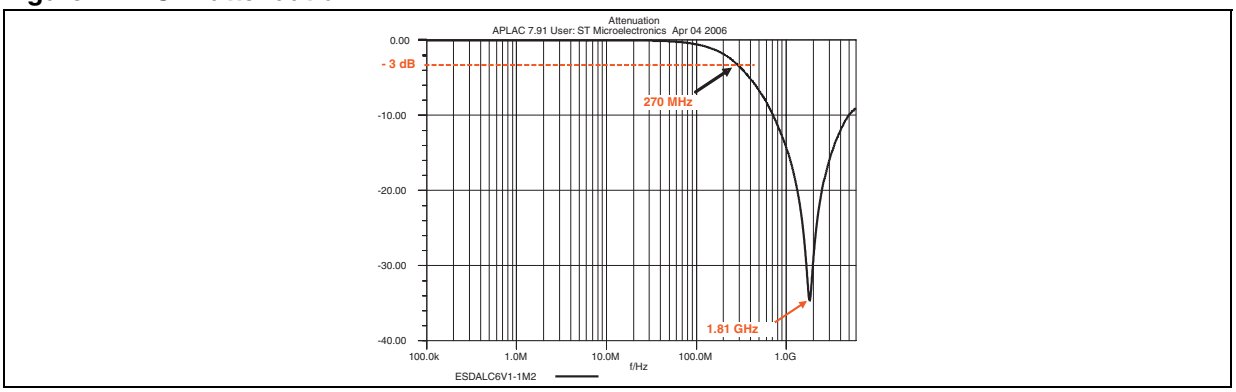
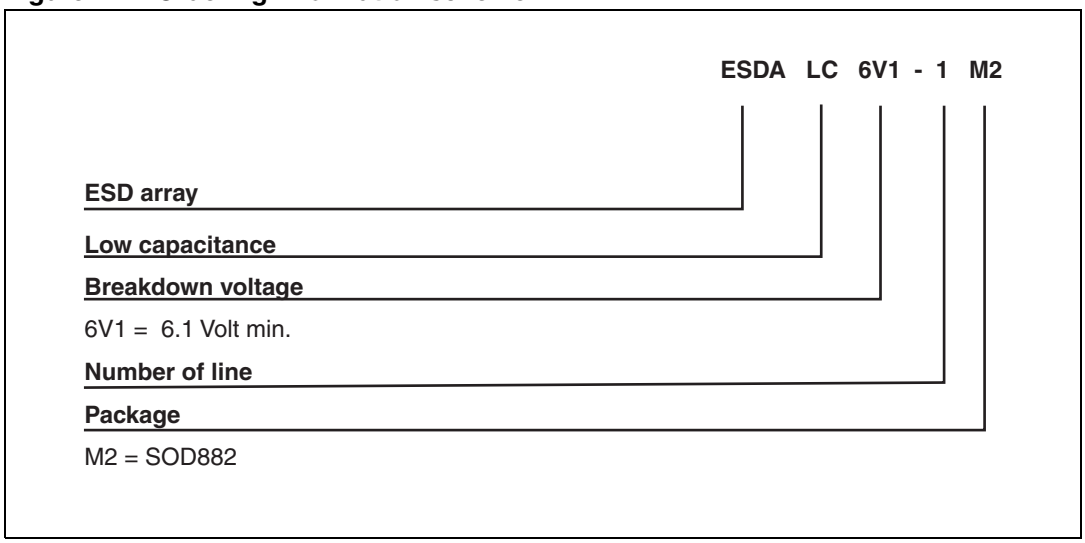


Figure 11. S21 attenuation



2 Ordering information scheme

Figure 12. Ordering information scheme



3 Package information

- Epoxy meets UL94, V0
- Lead-free package

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Figure 13. SOD882 dimension definitions

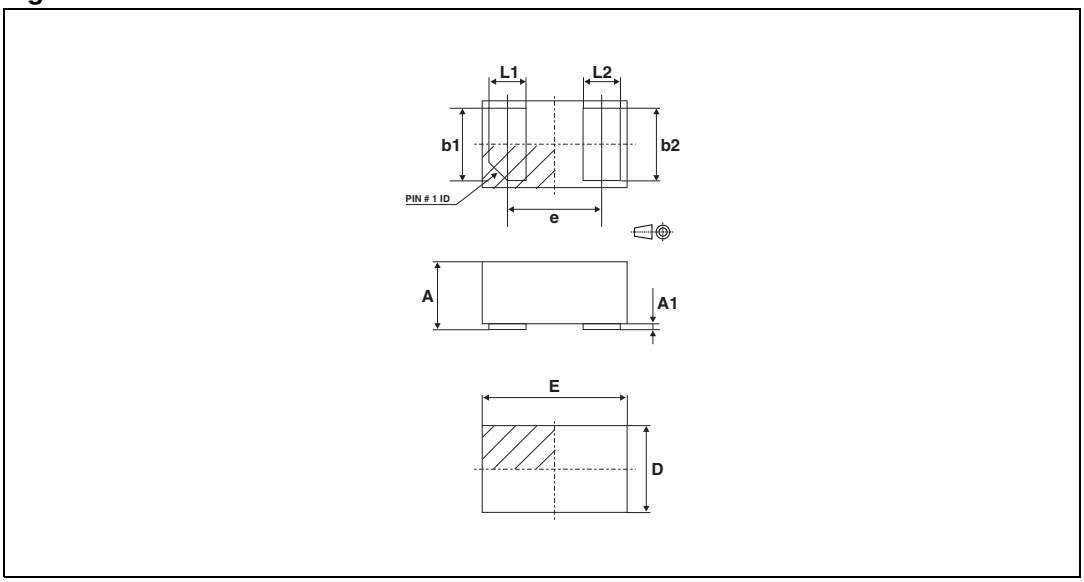


Table 3. SOD882 dimension values

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.40	0.47	0.50	0.016	0.019	0.020
A1	0.00		0.05	0.000		0.002
b1	0.45	0.50	0.55	0.018	0.020	0.022
b2	0.45	0.50	0.55	0.018	0.020	0.022
D	0.55	0.60	0.65	0.022	0.024	0.026
E	0.95	1.00	1.05	0.037	0.039	0.041
e	0.60	0.65	0.70	0.024	0.026	0.028
L1	0.20	0.25	0.30	0.008	0.010	0.012
L2	0.20	0.25	0.30	0.008	0.010	0.012

Figure 14. SOD882 footprint in mm (inches)

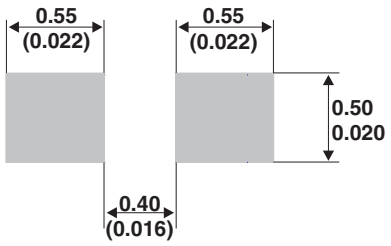
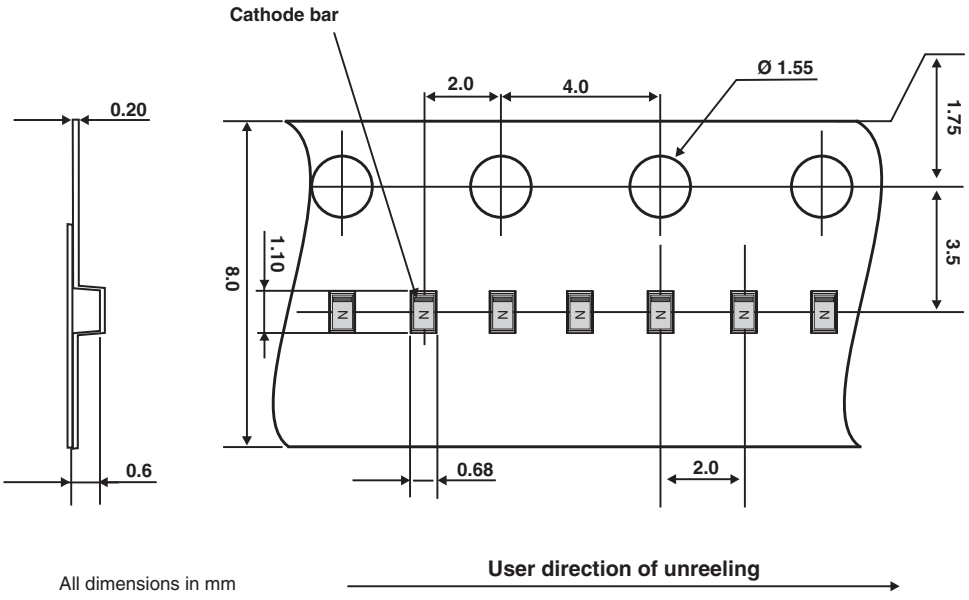


Figure 15. Marking



Note: Product marking may be rotated by multiples of 90° for assembly plant differentiation. In no case should this product marking be used to orient the component for its placement on a PCB. Only pin 1 mark is to be used for this purpose.

Figure 16. Tape and reel specifications

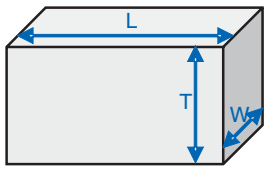


4 Recommendation on PCB assembly

4.1 Stencil opening design

1. General recommendation on stencil opening design
   a) Stencil opening dimensions: L (Length), W (Width), T (Thickness).

Figure 17. Stencil opening dimensions



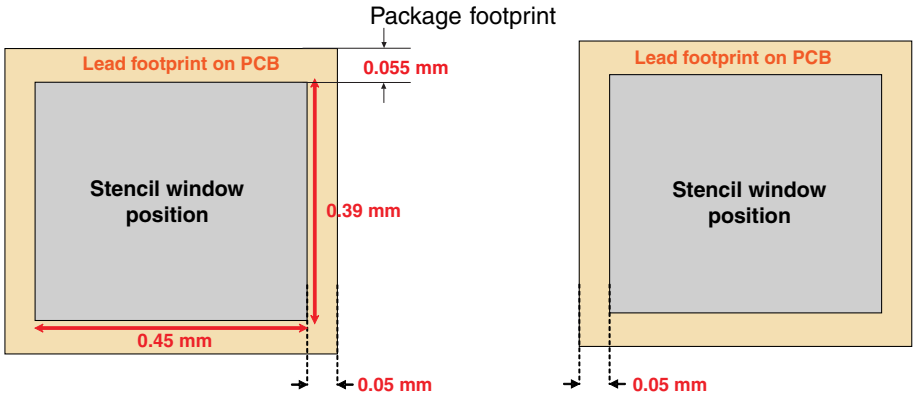
   b) General design rule
   Stencil thickness (T) = 75 ~ 125 µm

$$\text{Aspect Ratio} = \frac{W}{T} \geq 1.5$$

$$\text{Aspect Area} = \frac{L \times W}{2T(L+W)} \geq 0.66$$

2. Reference design
   a) Stencil opening thickness: 100 µm
   b) Stencil opening for leads: Opening to footprint ratio - between 60% and 65%.

Figure 18. Recommended stencil windows position



4.2 Solder paste

1. Halide-free flux qualification ROL0 according to ANSI/J-STD-004.
2. “No clean” solder paste is recommended.
3. Offers a high tack force to resist component movement during high speed.
4. Solder paste with fine particles: powder particle size is 20-45 µm.

4.3 Placement

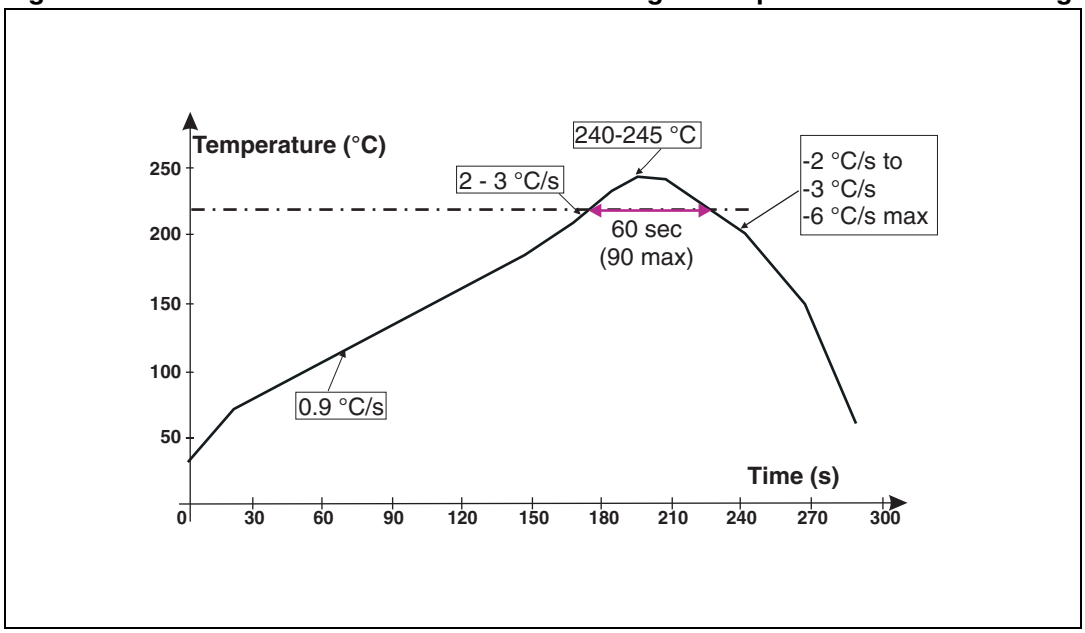
1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering
3. Standard tolerance of ± 0.05 mm is recommended.
4. 3.5 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

4.4 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. The symmetrical layout is recommended, in case any tilt phenomena caused by asymmetrical solder paste amount due to the solder flow away.

4.5 Reflow profile

Figure 19. ST ECOPACK® recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement.

5 Ordering information

Table 4. Ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
ESDALC6V1-1M2	N(1)	SOD882	0.92 mg	12000	Tape and reel

1. The marking can be rotated by multiples of 90° to differentiate assembly location

6 Revision history

Table 5. Document revision history

Date	Revision	Changes
23-May-2006	1	Initial release
16-Jun-2006	2	Updated tape and reel illustration (*Figure 16*).
11-Oct-2006	3	Corrected formatting errors on page 1. No technical changes.
10-May-2007	4	Updated *Functional diagram* to single diode. Added *Section 4: Recommendation on PCB assembly*.
26-Nov-2007	5	Corrected *2: Ordering information scheme*. Updated *Figure 16: Tape and reel specifications*. Added *Figure 18: Recommended stencil windows position*. Reformatted to current standards.
02-Nov-2010	6	Updated *Table 1*, *Table 2*, base quantity change on *Table 4* and updated graphics.
24-Jan-2012	7	Updated *Table 3* and added *Figure 13*.

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